(vi) The need of the additional voltage source V^1 can be eliminated by modifying the circuit as shown.

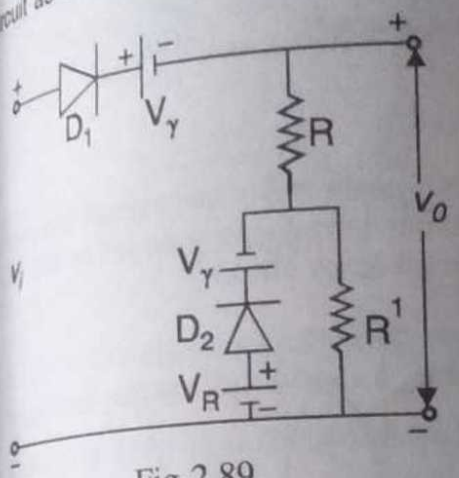

Fig.2.89

In this arrangement the battery V_R not only acts as the reference voltage, but it also keeps diode D_2 conducting.

(vii) Yet another circuit which provides for temperature compensation is as shown.

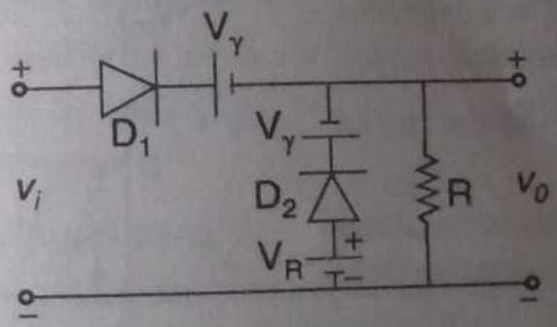

Fig.2.90

In this arrangement, the clipping level V_R is quite independent of V_γ and hence is not affected by changes of temperature.

2.11 *Clamping circuits*

We know that a capacitor blocks the passage of direct current. Hence when a nonsinusoidal, periodic signal is transmitted through a capacitive coupling circuit, it loses its d.c. component. If it is necessary to restore to the signal its d.c. component at a later stage, the signal needs to be passed through a ***clamping circuit***. Since the clamping circuit restores or reinserts the lost d.c. component, it is also termed as '*d.c. restorer*' or '***d.c. inserter***' circuit.

A clamping circuit also finds use when the d.c. value of a signal is to be shifted from one level to another level.

Basically clamping circuits use reactive elements like capacitors in conjunction with resistors and nonlinear elements like diodes.

2.12 *Classification of clamping circuits*

Primarily clamps are of two types :

(i) Negative clamp (or positive peak clamper)

(ii) Positive clamp (or negative peak clamper).

These are studied in the following paragraphs.

2.12.1 *Negative clamp*

This is also termed as ***positive peak clamper***, since the circuit clamps the positive peak of a signal to zero level. This type of clamper introduces a negative d.c. level. Hence the name ***negative clamp***. The basic circuit is as shown.

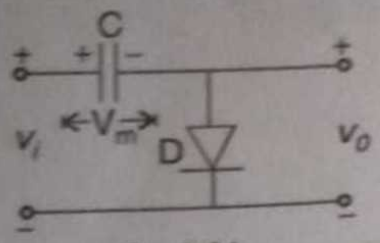

Fig. 2.91

D is an ideal diode and C is a capacitor. [$R_f = 0$ and $V_\gamma = 0$ for the ideal diode].

Let the input be a sinusoidal signal given as $v_i = V_m \sin \omega t$.

During the first quarter cycle of the input wave, when v_i goes positive, it is seen that the diode gets forward-biased and hence conducts. The capacitor C gets charged. At the end of the quarter cycle, $v_i = V_m$. The capacitor charges to V_m volts, with polarity as shown.

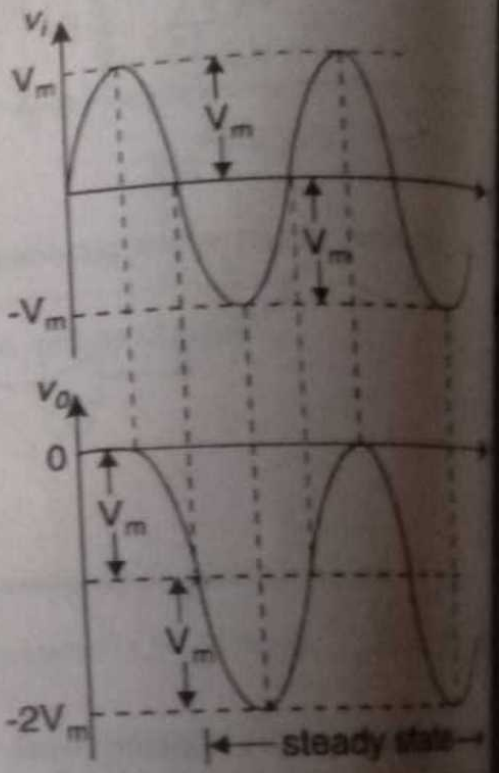

Fig. 2.92

Since $R_f = 0$, there is no voltage drop across the diode, with the result that

As the instantaneous amplitude decreases during the second quarter cycle, we expect the capacitor to discharge. But this cannot happen, since there is no resistance through which it can discharge. The voltage across C remains V_m.

The output voltage is $v_0 = v_i - V_m$.

During the negative half-cycle, the diode gets reverse-biased and does not conduct. During the subsequent positive half-cycles, the voltage across the capacitor is fixed at V_m, and when steady state is reached, we have :

$$v_0 = v_i - V_m$$

The charged capacitor acts as a voltage source V_m. The equivalent circuit is as shown.

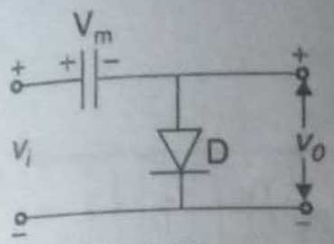

Fig.2.93

For $v_i = 0$, $v_0 = -V_m$,
For $v_i = V_m$, $v_0 = 0$,
For $v_i = -V_m$, $v_0 = -2\ V_m$.

Based upon the above equation, at steady state (after about 5 cycles), the wave form of the output voltage is plotted. It is as shown.

It can be seen that the positive extremities of the output voltage are clamped to zero level.

The peak-to-peak amplitude of the input wave = $2V_m$.

The peak-to-peak amplitude of the output wave = $2V_m$.

The output wave is also seen to be sinusoidal.

Thus there is no distortion of wave-form. The circuit merely clamps (i.e. limits) the positive peaks to zero level.

2.12.2 *Modified clamping circuit*

As studied earlier, the capacitor charges to voltage V_m at the end of the first quarter cycle, during which the diode conducts. During the subsequent positive excursions of the input signal, the capacitor cannot discharge as and when the amplitude goes below V_m.

This is due to the absence of resistance through which the capacitor can discharge. In order to enable the capacitor to discharge, either the capacitor or the diode must be shunted by a suitable resistance. The more usual practice is to have a resistance across the diode as shown in the modified clamping circuit of fig.2-94.

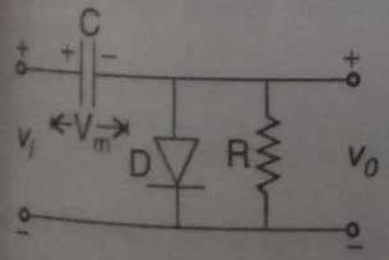

Fig.2.94

If, after attaining steady state, the amplitude of the input signal is abruptly decreased, as $t = t_1$ in the figure, it is found that a transient state results, and the positive peaks which were hitherto clamped at zero level, no longer attain zero.

However, as the capacitor discharges due to the diminuation of the signal amplitude, the voltage across C decreases exponentially; the positive peaks approach zero progressively as shown,

until after a few cycles, steady state is again reached and the positive peaks are clamped to zero level thereafter.

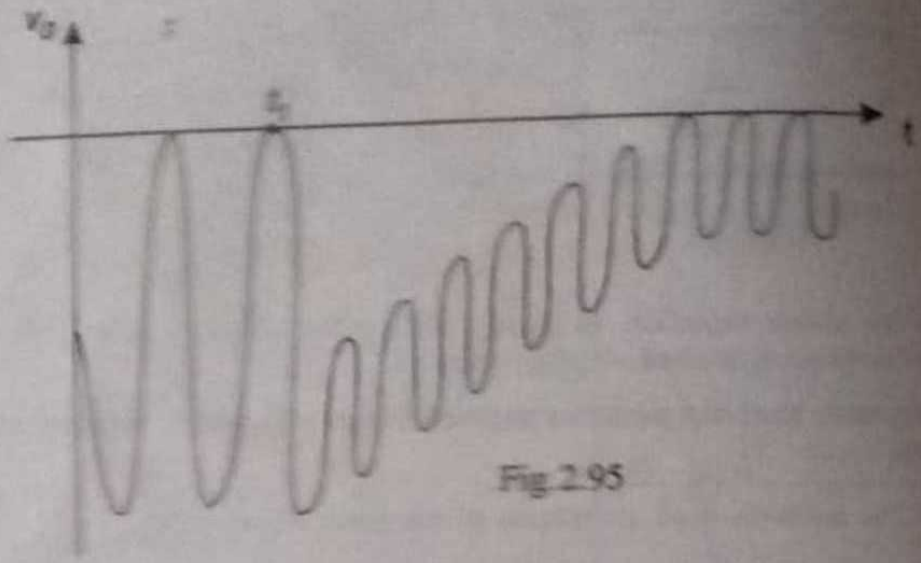

Fig.2.95

2.12.3 *Positive clamp*

This is also termed as ***negative peak clamper***, since this circuit clamps the negative peaks of a signal. The negative peak clamper introduces a positive d.c. value; hence the name ***positive clamp***.

The basic circuit is as shown.

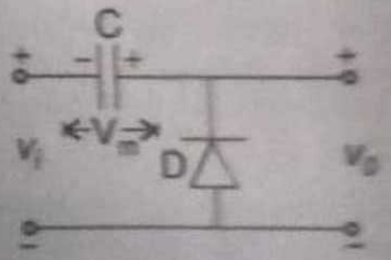

Fig.2.96

Let the input signal be $v_i = V_m \sin \omega t$.

It is clear that the diode gets forward-biased and conducts, as v_i goes negative. The capacitor charges to voltage V_m, with polarity as shown.

Just like for the negative clamp we studied earlier, under steady state conditions, we have for the positive clamp :

$$v_o = v_i - (-V_m) \quad \text{or} \quad v_o = v_i + V_m$$

Based on the above relationship between v_o and v_i, the output voltage wave form is plotted. It is as shown.

It is seen from fig.2-97, that the negative peaks of the input signal are clamped to zero level. Peak-to-peak amplitude of output voltage = $2V_m$, which is the same as that of the input signal.

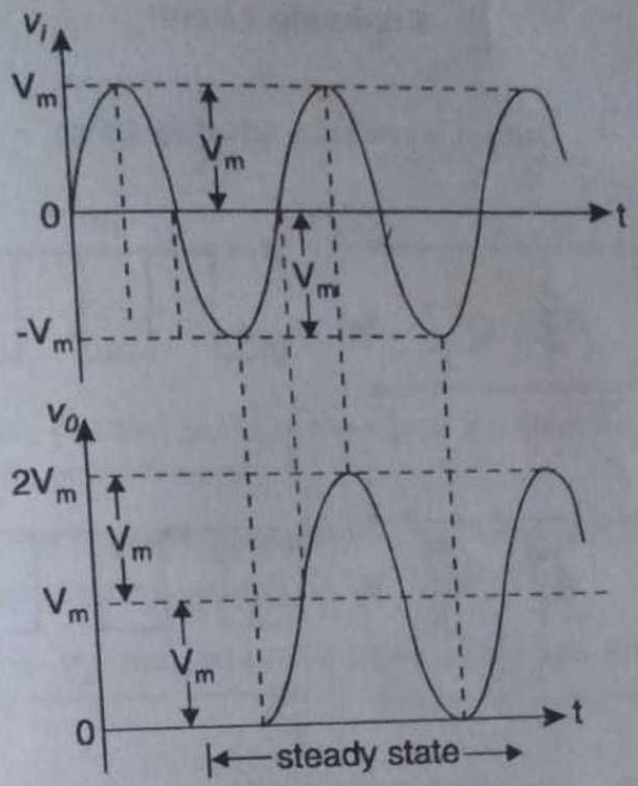

Fig.2.97

There is no distortion of wave form. The circuit merely clamps the negative peaks of the signal to zero level.

The modified positive clamp, with the inclusion of the shunt resistance, is as shown.

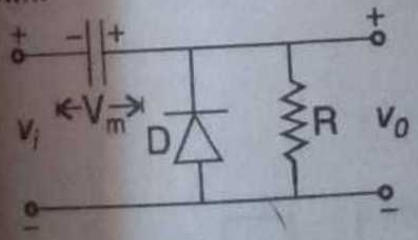

Fig.2.98

At steady state, the charged capacitor behaves like a voltage source V_m.

Example :

When the input is a symmetrical square wave, the output wave forms, in respect of different clamping circuits are as shown.

Input wave form

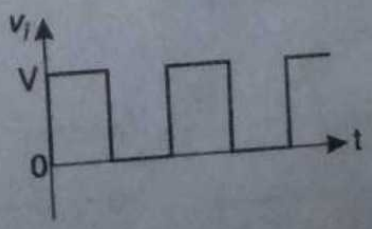

Fig.2.99