Digital System Design: Assignment 3 Part B

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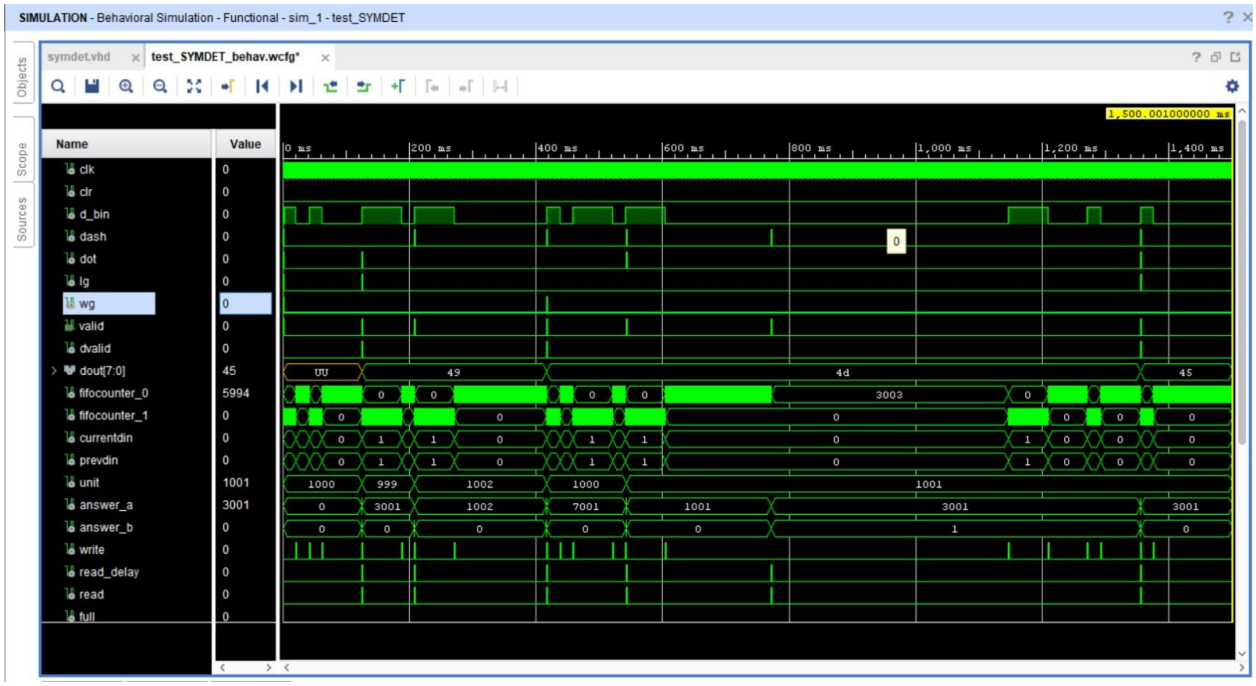
Overview:

- **B.1** ✔
- **B.2** ✔
- **B.3** ✔
- **B.4**
- **B.5** ✔

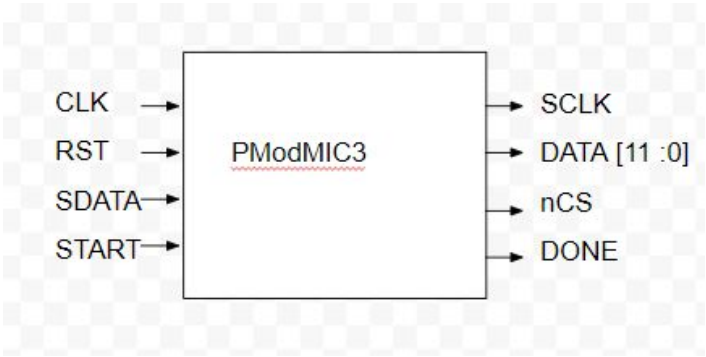
Milestone 1 Output:



We are getting the output HKU EEE on the hardware serial interface.

Audio Processing Module Top Level Diagram:

PART 1: ADC Converter Top Level Diagram (PModMIC3)

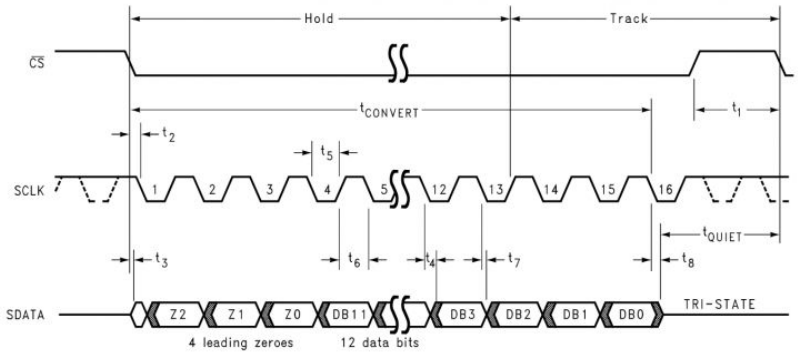


Function:

To implement this we've modelled the problem as an FSM for the shift counter.
We store the 16 bit input in "temp".
Data outputs the 12 bits (not including the leading 0's).

Timing Diagram

A sample timing diagram taken from the ADCS7476 datasheet representing the data that will be received by the system board from the Pmod is provided below:

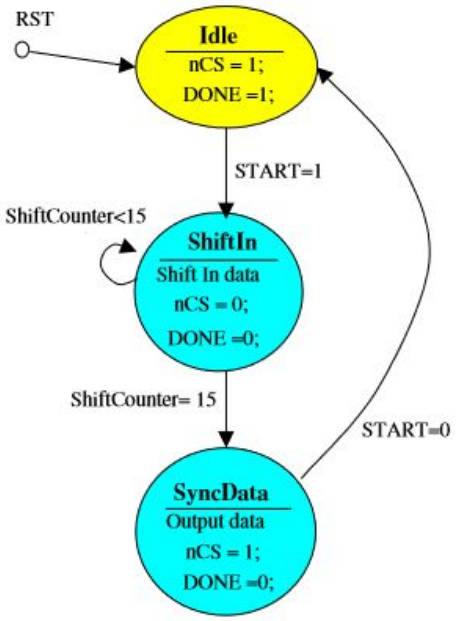


Now we need to make sure nCS stays 0 for 15 cycles and that sclk toggles for 15 cycles with half the frequency of the input clock (6.14 Hz -> 3.07 Hz). To reduce the clock frequency we create a signal clk_div1 which is the highest of a 2 bit clock counter.

```
        elsif (clk = '1' and clk'event) then
            clk_counter <= clk_counter + '1';
        end if;
    end process;

    clk_div1 <= clk_counter(0);
```

Finally we need to make the FSM. Below is the flowchart of the implementation of the FSM: (Sync_Proc + Proc_Output + Proc_Next_State)



This completes the PmodMIC3 component.

PART 2: Signal Processing (Audio_Proc)

For this part we first take the absolute value. Here since 000000000000 is most negative number and 111111111111 is most positive, we know 011111111111 is when pressure is 0. So here we take a variable called “absolute_val” to be the lower 11 bits of the input.

```
absolute_val <= conv_integer(data_in(10 downto 0));
-- We now have the absolute value
```

We now need to find the moving average. The moving average is calculated for a fixed window size. After which the parameters are reset. If the value of the avg during this time exceeds the threshold value = "00000001111" Then we set out_data = 1. If not, the value becomes 0. After experimentation we found 2^7 (128) to be an appropriate window size.

PART 3: Connecting all the components

Due to paucity of time we were unable to edit the testbench to connect all the components. However, the final top level diagram is the same as figure B.3 in the HW3 Assignment.