

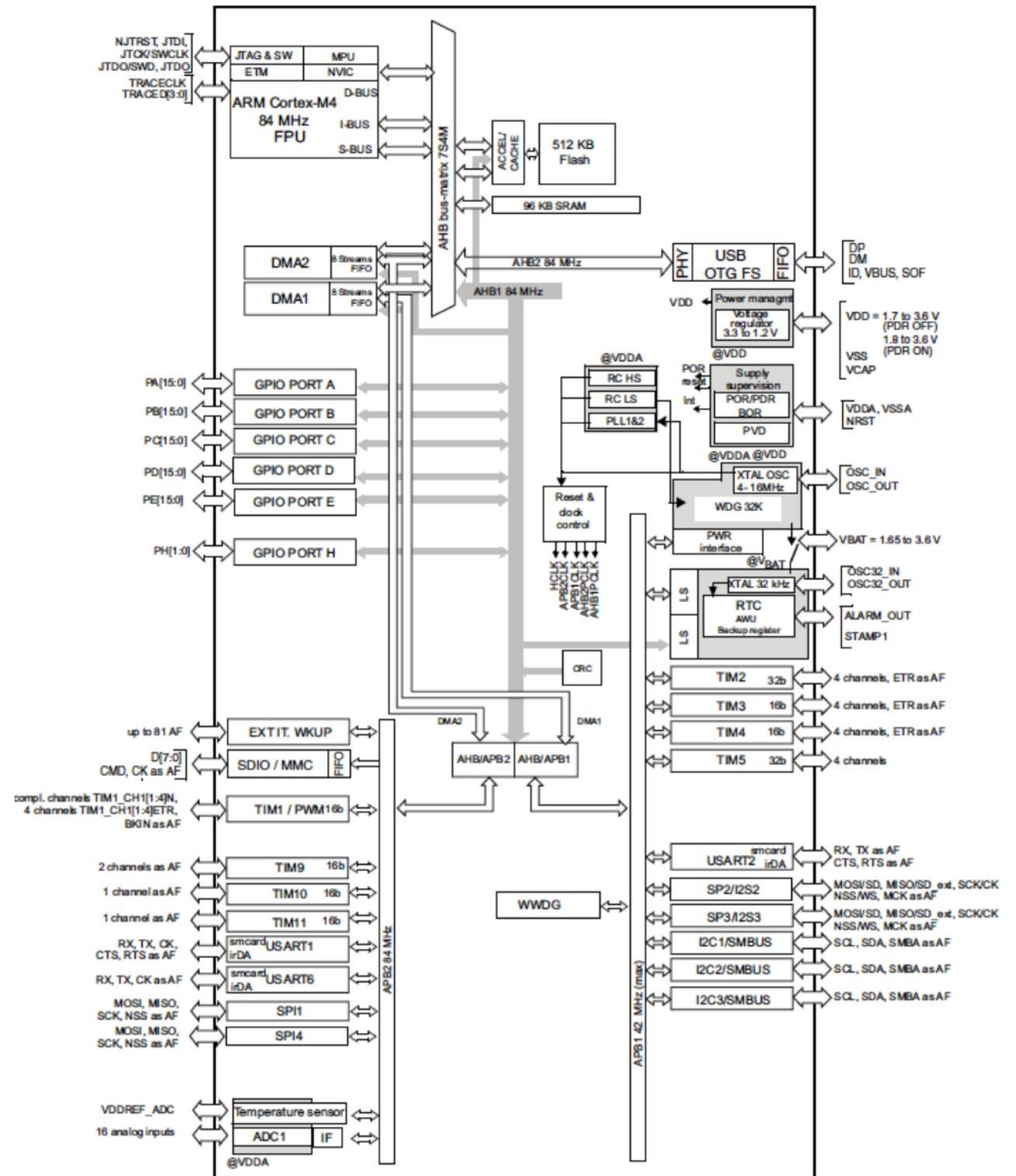
General Purpose Timers

Chapter 15

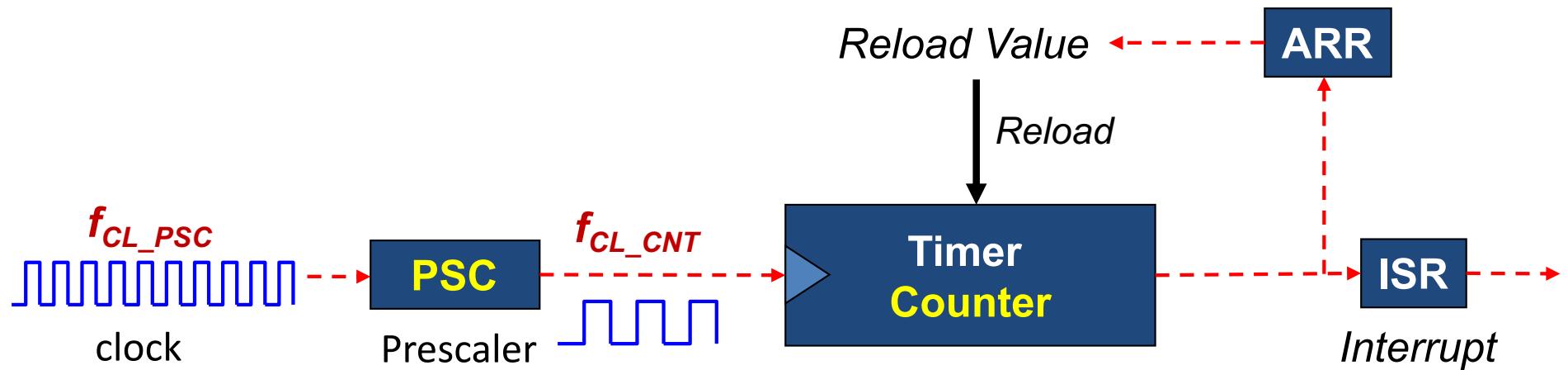
Timer

- Free-run counter (independent of processor)
- Functions
 - Input capture
 - Output compare
 - Pulse-width modulation (PWM) generation

Block Diagram

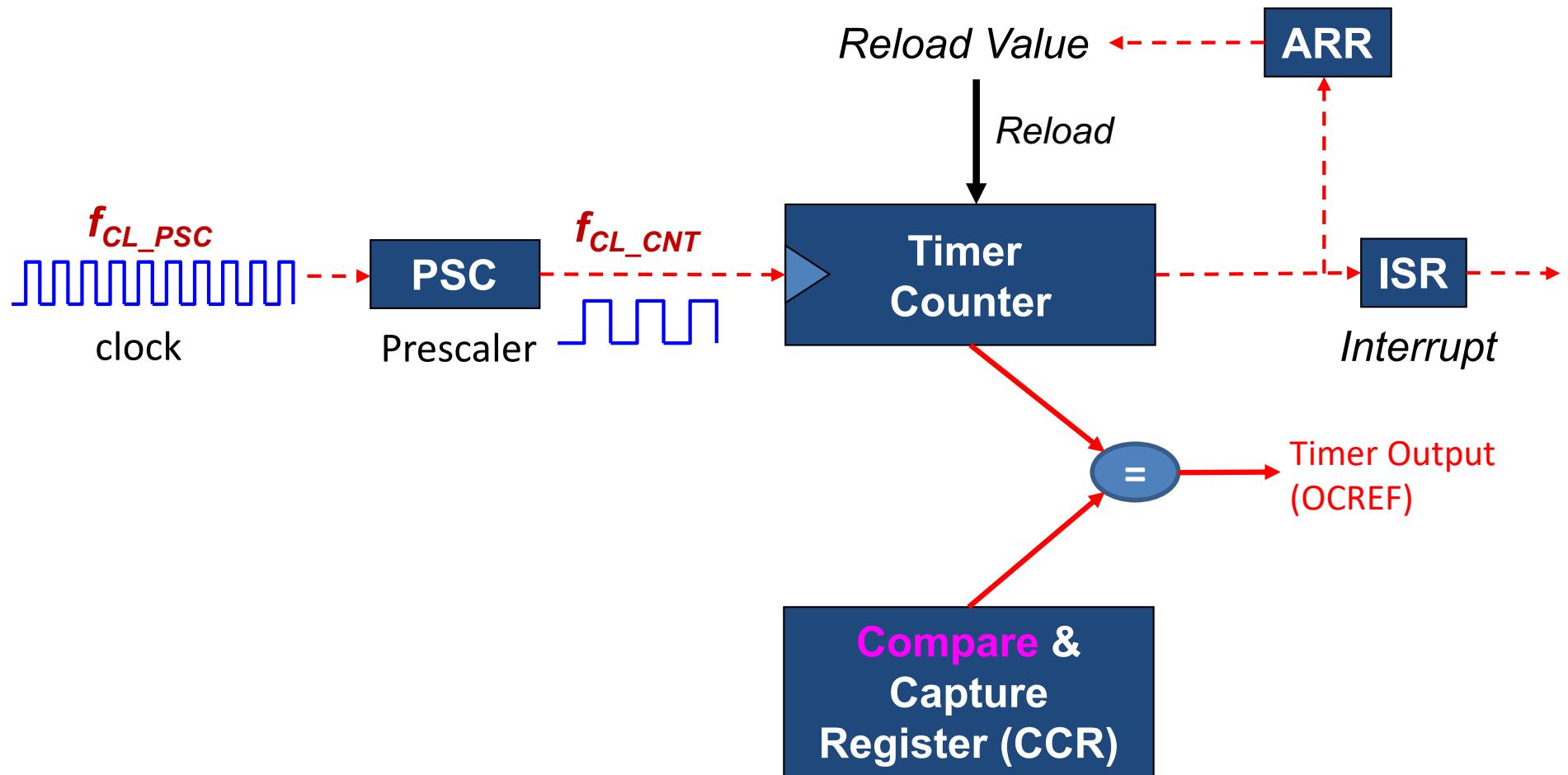


Timer: Clock

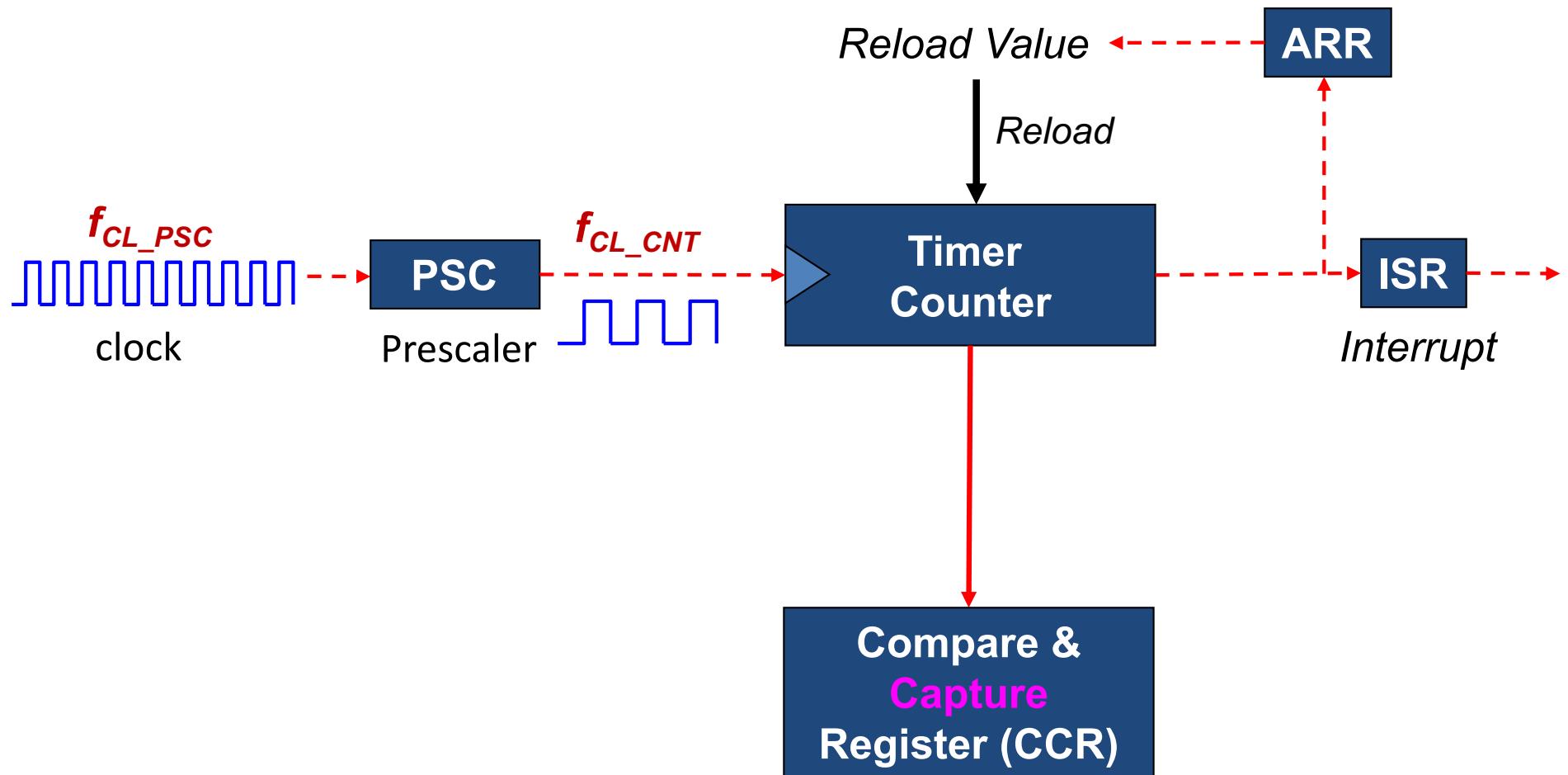


$$f_{CK_CNT} = \frac{f_{CL_PSC}}{PSC + 1}$$

Timer: Output

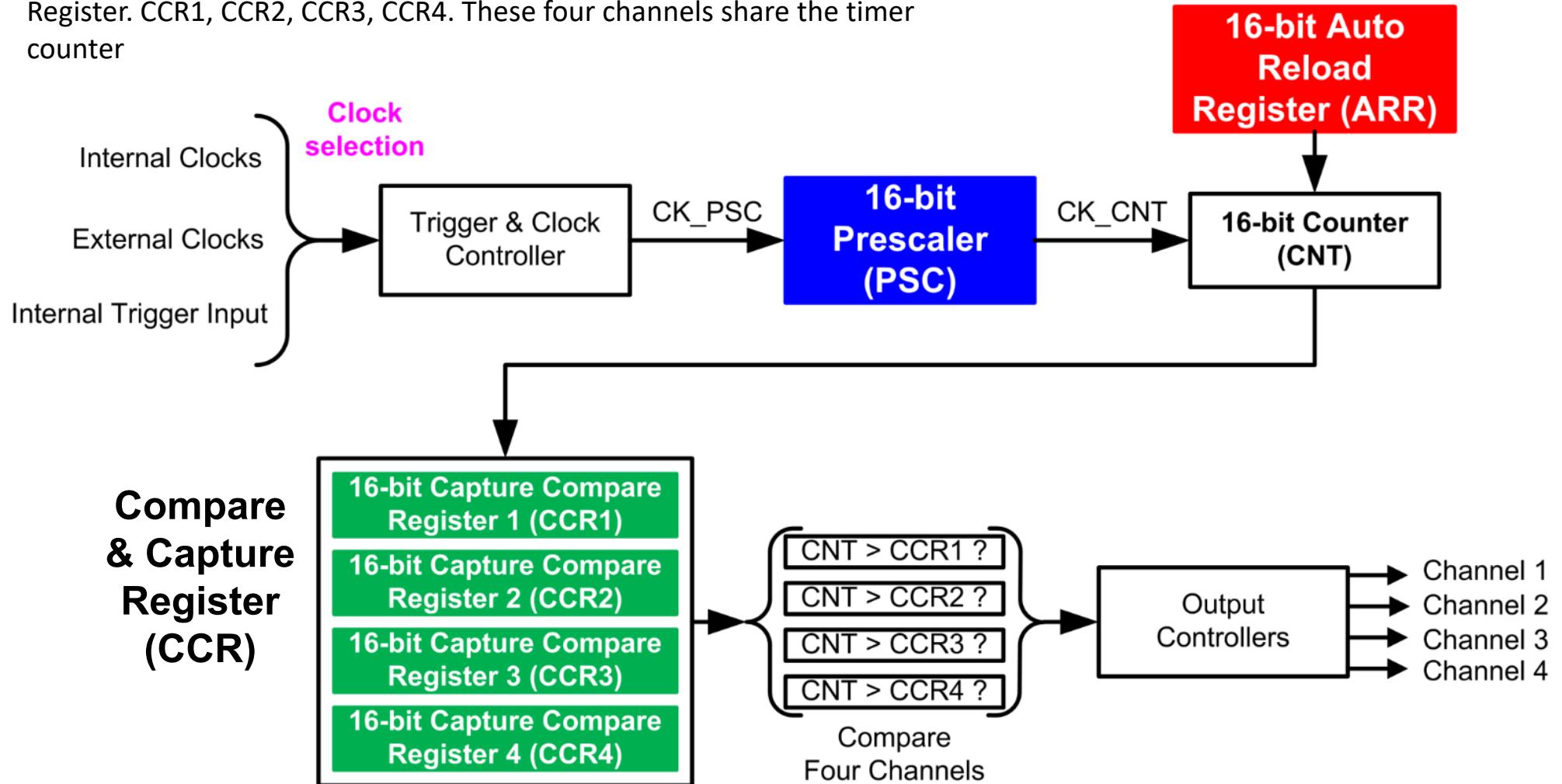


Timer: Input Capture



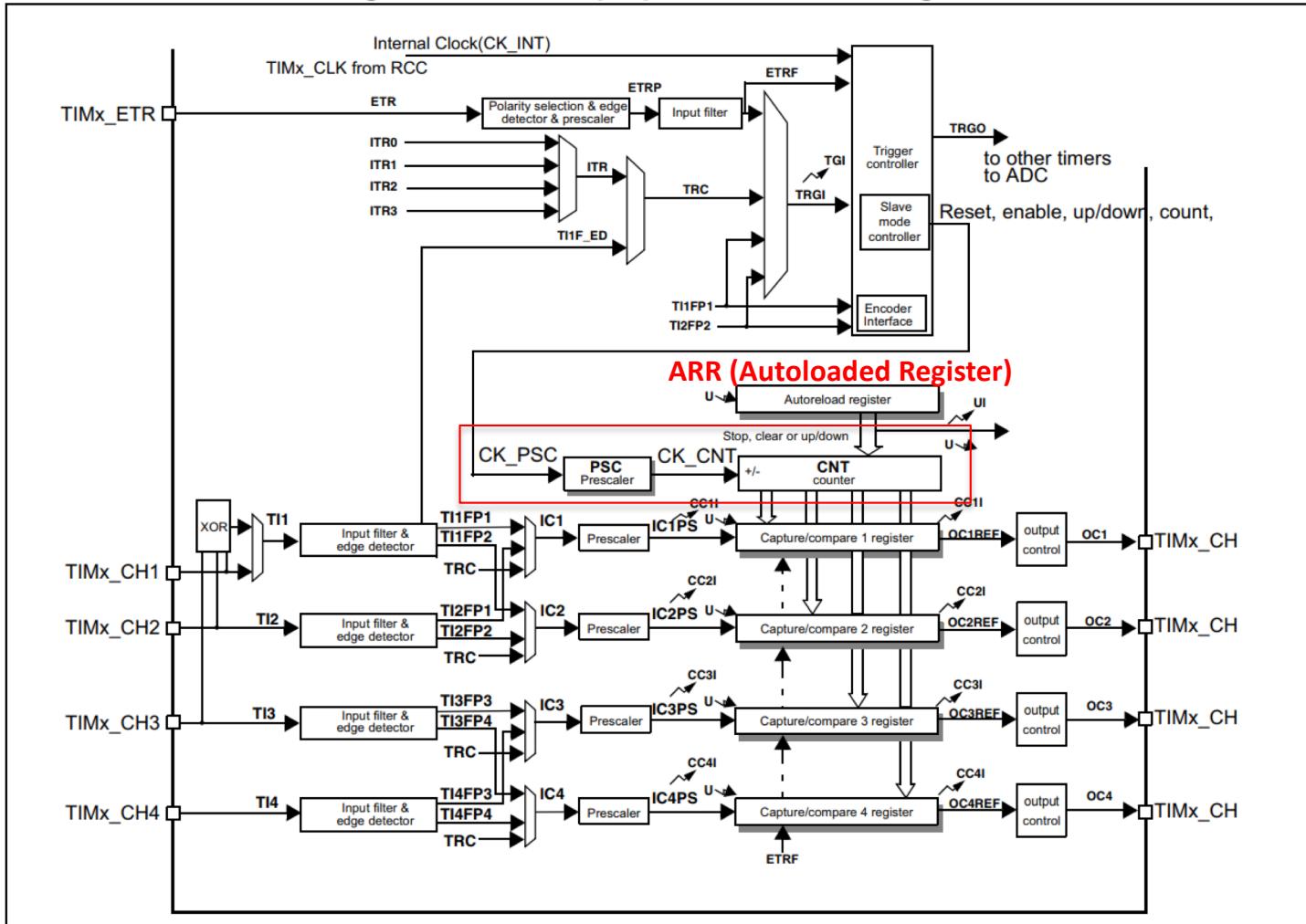
Multi-Channel Outputs

Each timer has four channels. Each channel has its own Compare and Capture Register. CCR1, CCR2, CCR3, CCR4. These four channels share the timer counter

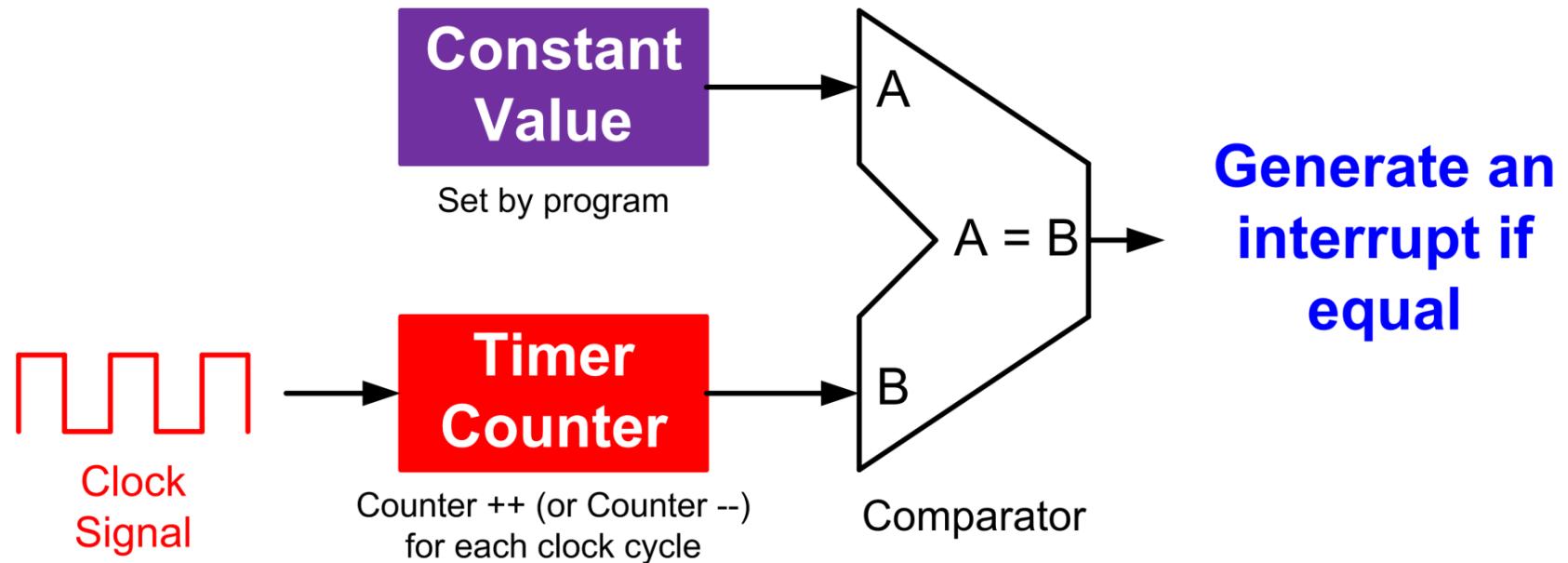


GP Timer Block Diagram

Figure 87. General-purpose timer block diagram

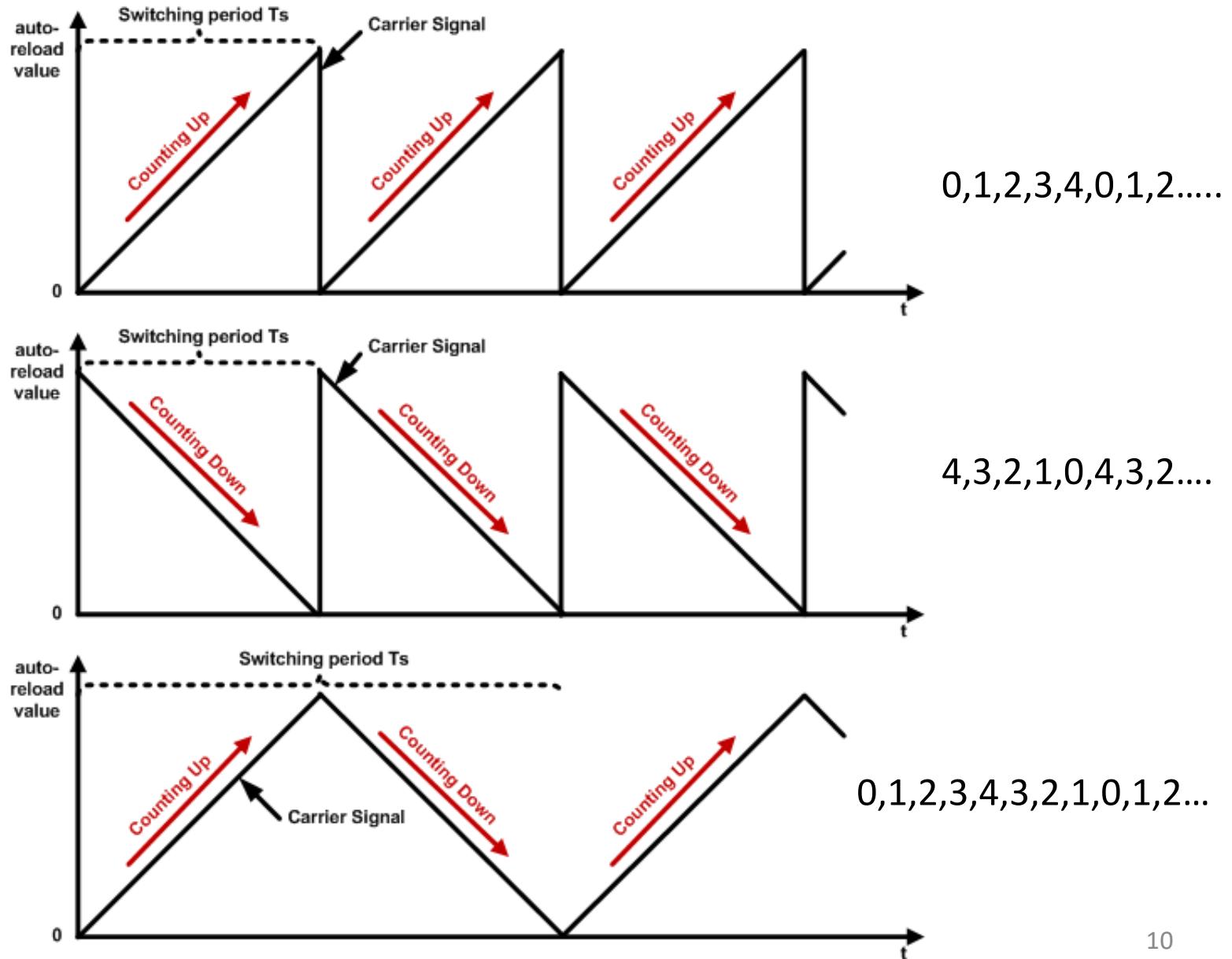


Output Compare

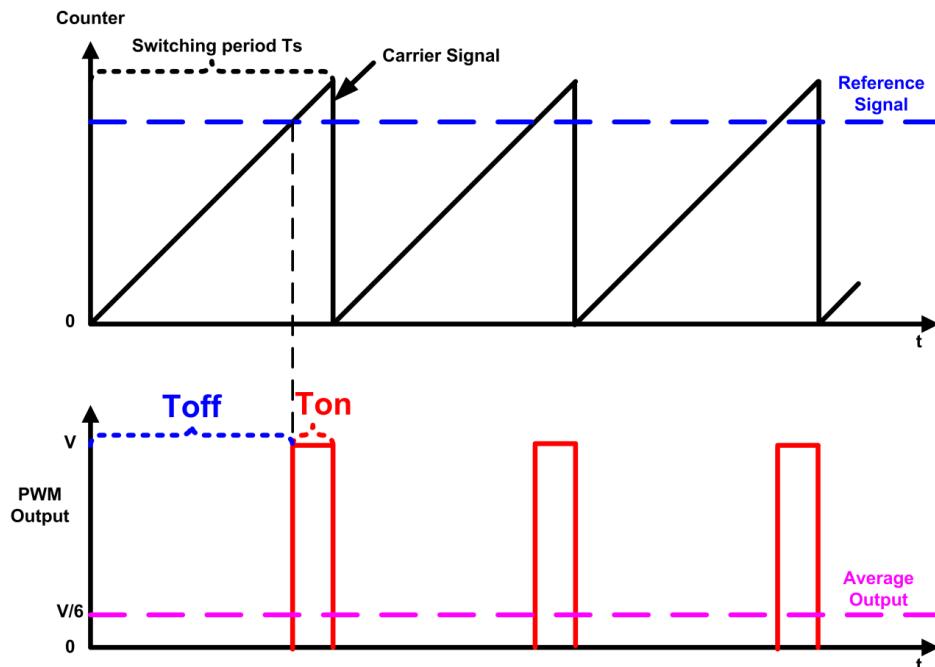


Output Compare Mode (OCM)	Timer Output (OCREF)
000	Frozen
001	High if CNT == CCR
010	Low if CNT == CCR
011	Toggle if CNT == CCR
100	Forced low (always low)
101	Forced high (always high)

Counting up, down, center



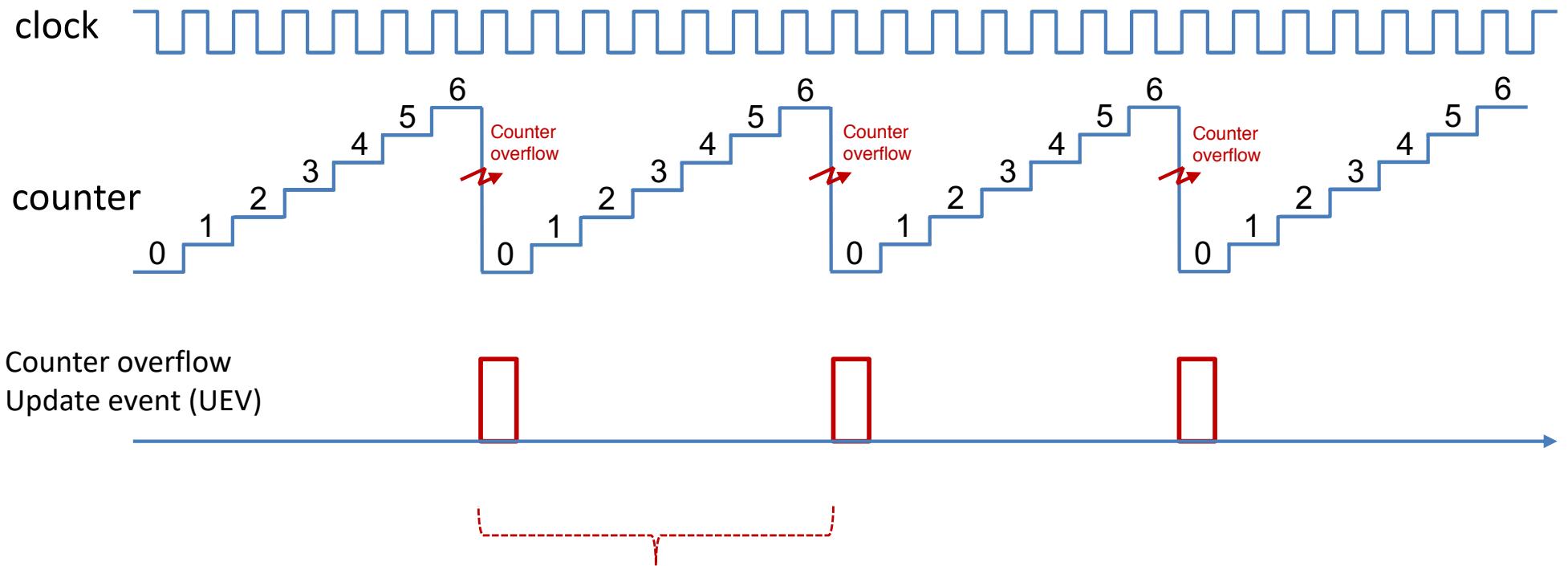
PWM Mode



Mode	Counter < Reference	Counter \geq Reference
PWM mode 1 (Low True)	Active	Inactive
PWM mode 2 (High True)	Inactive	Active

Edge-aligned Mode (Up-counting)

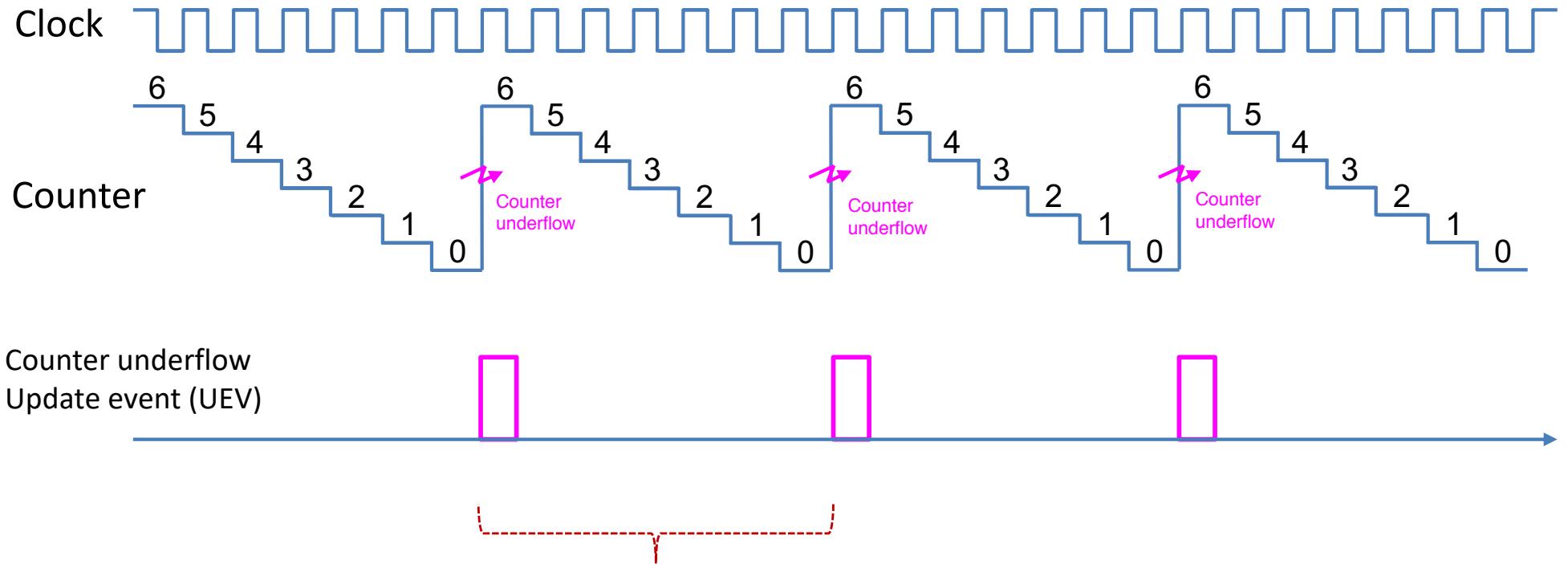
ARR = 6, RCR = 0



$$\begin{aligned}\text{Period} &= (1 + \text{ARR}) * \text{Clock Period} \\ &= 7 * \text{Clock Period}\end{aligned}$$

Edge-aligned Mode (down-counting)

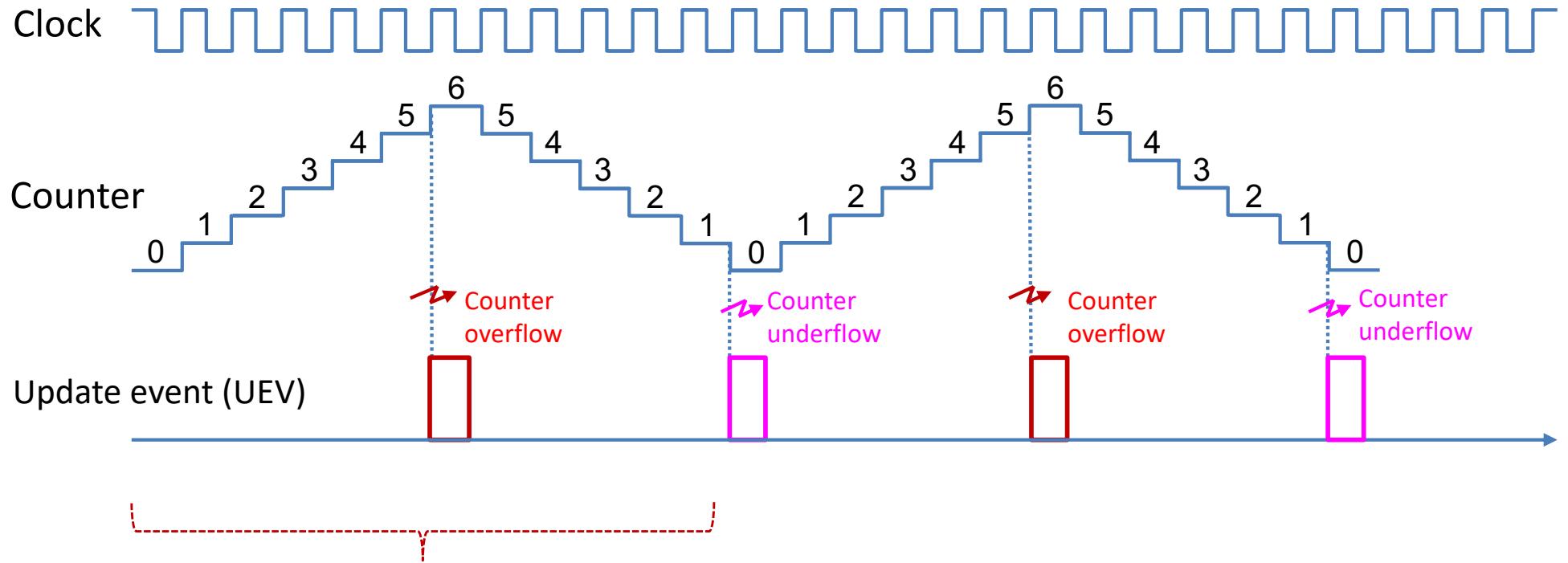
ARR = 6, RCR = 0



$$\begin{aligned}\text{Period} &= (1 + \text{ARR}) * \text{Clock Period} \\ &= 7 * \text{Clock Period}\end{aligned}$$

Center-aligned Mode

ARR = 6, RCR = 0



$$\begin{aligned}\text{Period} &= 2 * \text{ARR} * \text{Clock Period} \\ &= 12 * \text{Clock Period}\end{aligned}$$

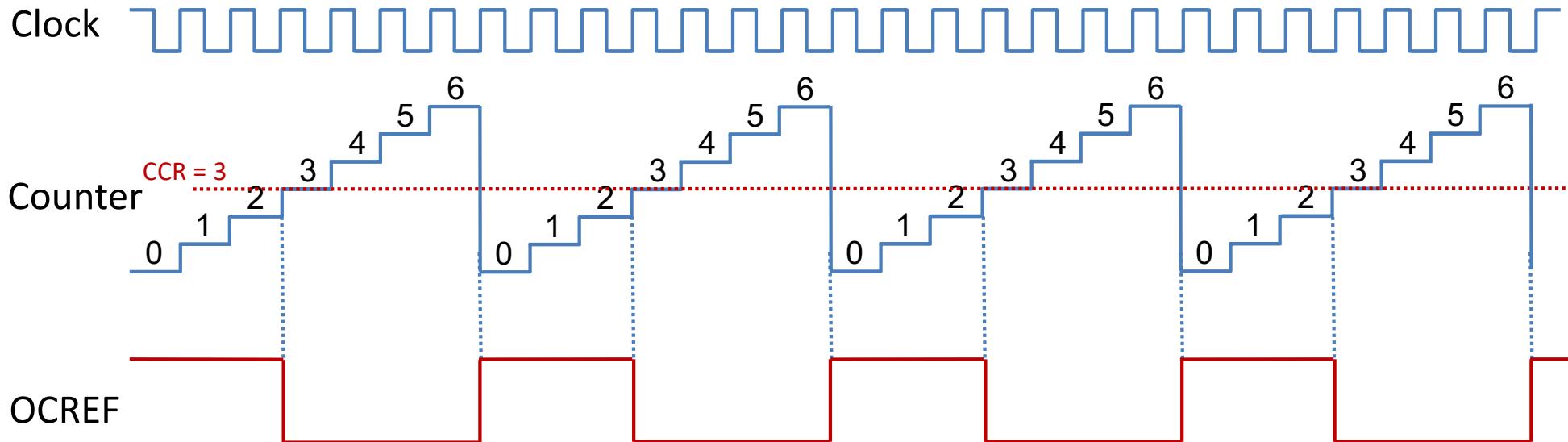
PWM Mode 1 (Low-True)

Mode 1

Timer Output =

$\begin{cases} \text{High if counter} < \text{CCR} \\ \text{Low if counter} \geq \text{CCR} \end{cases}$

Upcounting mode, ARR = 6, CCR = 3, RCR = 0



$$\begin{aligned}\text{Duty Cycle} &= \frac{\text{CCR}}{\text{ARR} + 1} \\ &= \frac{3}{7}\end{aligned}$$

$$\begin{aligned}\text{Period} &= (1 + \text{ARR}) * \text{Clock Period} \\ &= 7 * \text{Clock Period}\end{aligned}$$

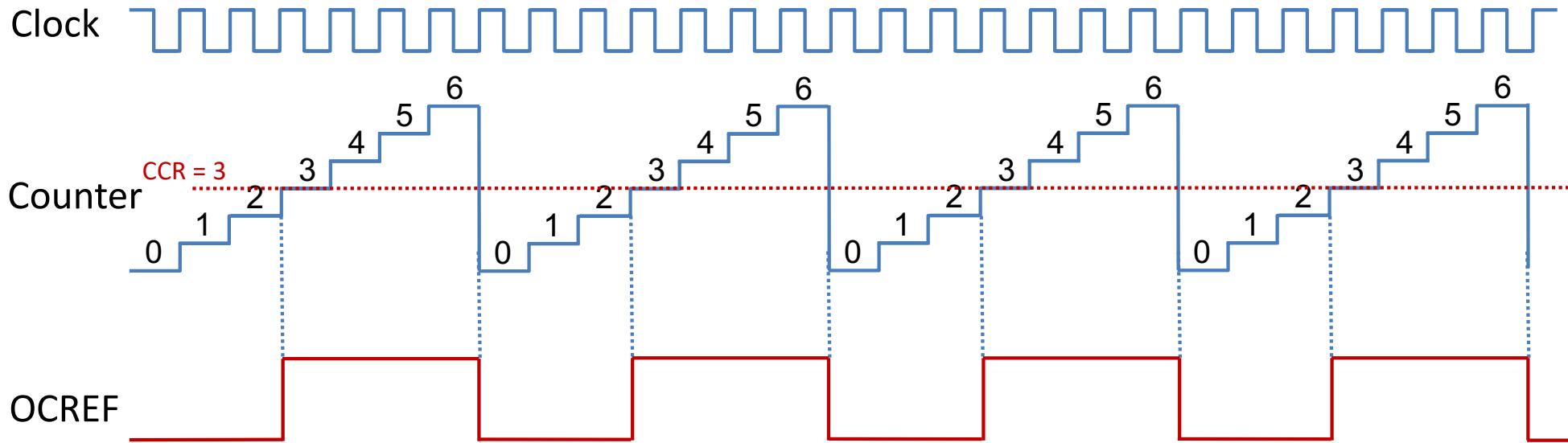
PWM Mode 2 (High-True)

Mode 2

Timer Output =

$\begin{cases} \text{Low if counter} < \text{CCR} \\ \text{High if counter} \geq \text{CCR} \end{cases}$

Upcounting mode, ARR = 6, CCR = 3, RCR = 0



$$\begin{aligned}\text{Duty Cycle} &= 1 - \frac{\text{CCR}}{\text{ARR} + 1} \\ &= \frac{4}{7}\end{aligned}$$

$$\begin{aligned}\text{Period} &= (1 + \text{ARR}) * \text{Clock Period} \\ &= 7 * \text{Clock Period}\end{aligned}$$

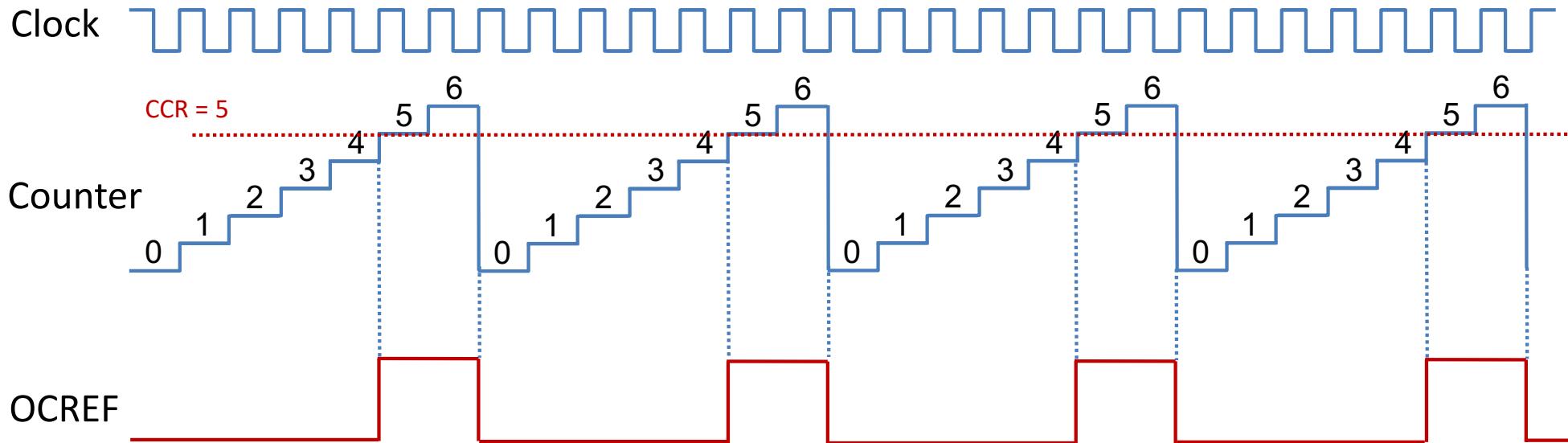
PWM Mode 2 (High-True)

Mode 2

Timer Output =

$\begin{cases} \text{Low if counter} < \text{CCR} \\ \text{High if counter} \geq \text{CCR} \end{cases}$

Upcounting mode, ARR = 6, CCR = 3, RCR = 0



$$\begin{aligned}\text{Duty Cycle} &= 1 - \frac{\text{CCR}}{\text{ARR} + 1} \\ &= \frac{2}{7}\end{aligned}$$

$$\begin{aligned}\text{Period} &= (1 + \text{ARR}) * \text{Clock Period} \\ &= 7 * \text{Clock Period}\end{aligned}$$

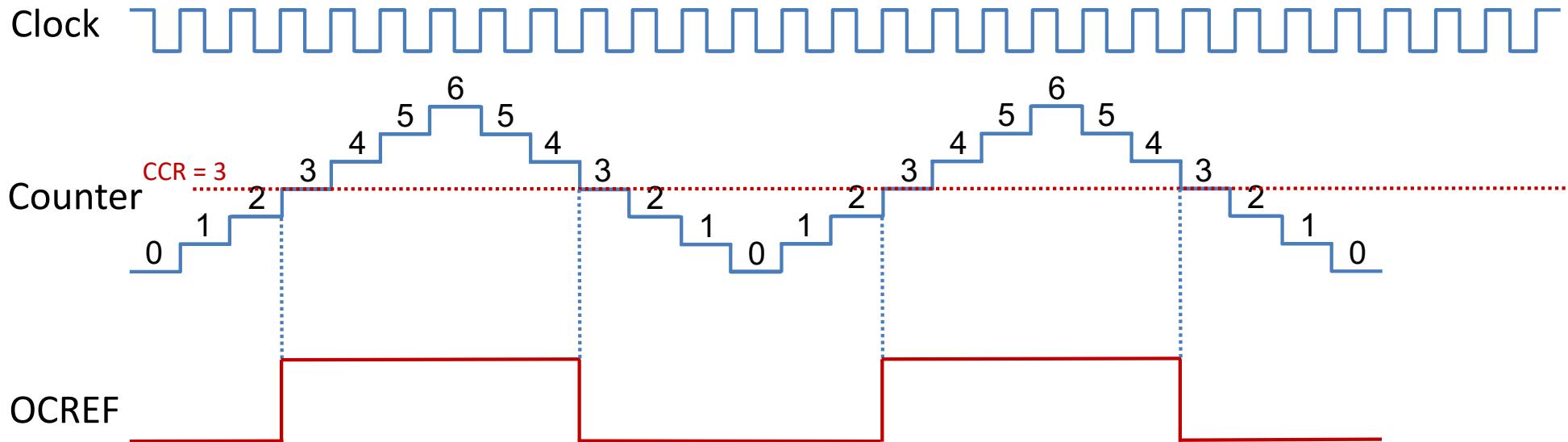
PWM Mode 2 (High-True)

Mode 2

Timer Output =

$\begin{cases} \text{Low if counter} < \text{CCR} \\ \text{High if counter} \geq \text{CCR} \end{cases}$

Center-aligned mode, ARR = 6, CCR = 3, RCR = 0



$$\begin{aligned} \text{Duty Cycle} &= 1 - \frac{\text{CCR}}{\text{ARR}} \\ &= \frac{1}{2} \end{aligned}$$

$$\begin{aligned} \text{Period} &= 2 * \text{ARR} * \text{Clock Period} \\ &= 12 * \text{Clock Period} \end{aligned}$$

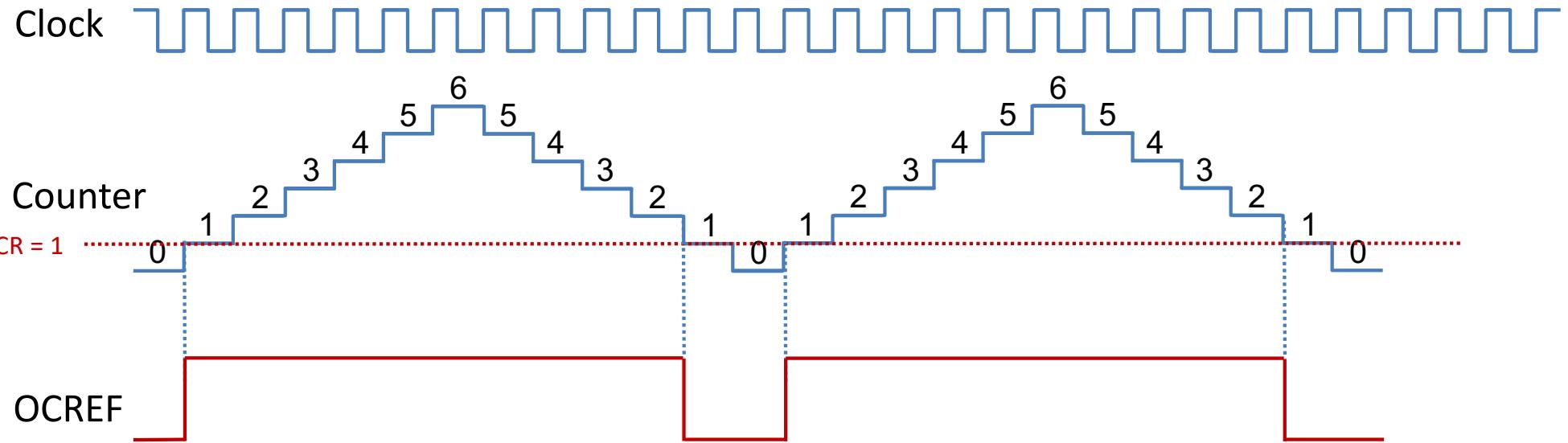
PWM Mode 2 (High-True)

Mode 2

Timer Output =

$$\begin{cases} \text{Low if counter} < \text{CCR} \\ \text{High if counter} \geq \text{CCR} \end{cases}$$

Center-aligned mode, ARR = 6, CCR = 3, RCR = 0

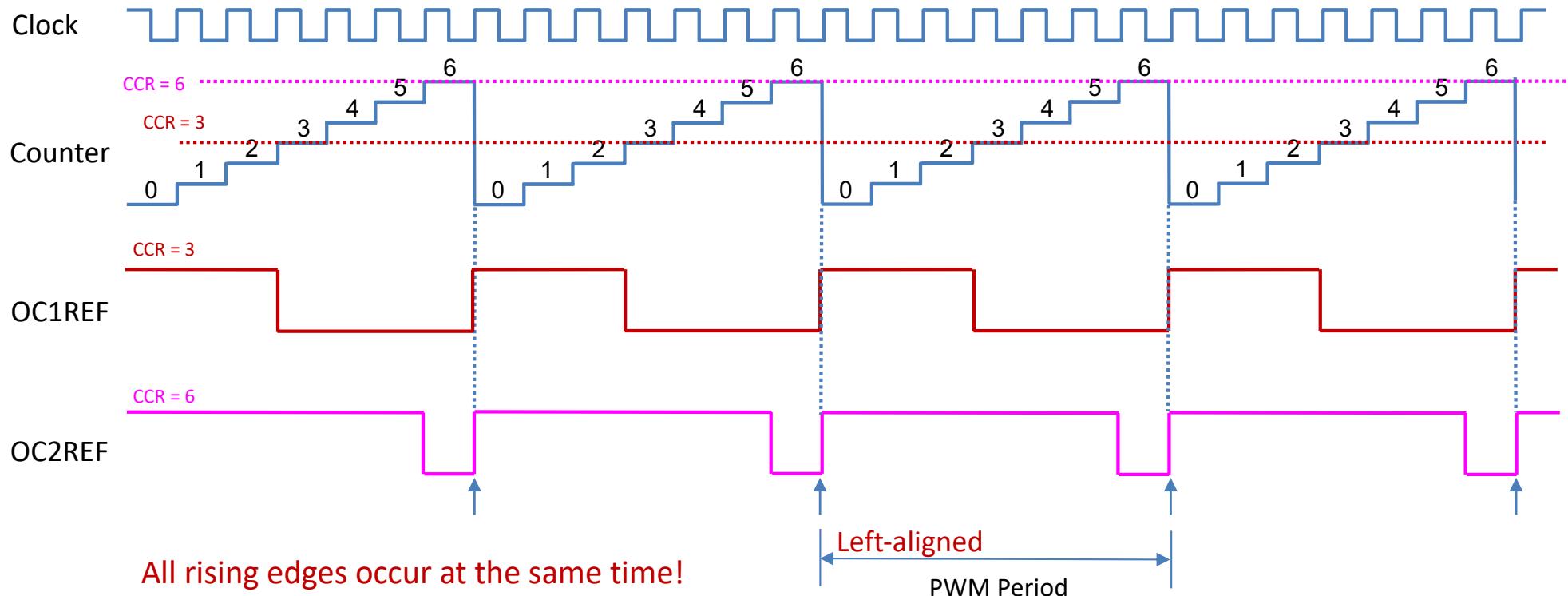


$$\begin{aligned} \text{Duty Cycle} &= 1 - \frac{\text{CCR}}{\text{ARR}} \\ &= \frac{5}{6} \end{aligned}$$

$$\begin{aligned} \text{Period} &= 2 * \text{ARR} * \text{Clock Period} \\ &= 12 * \text{Clock Period} \end{aligned}$$

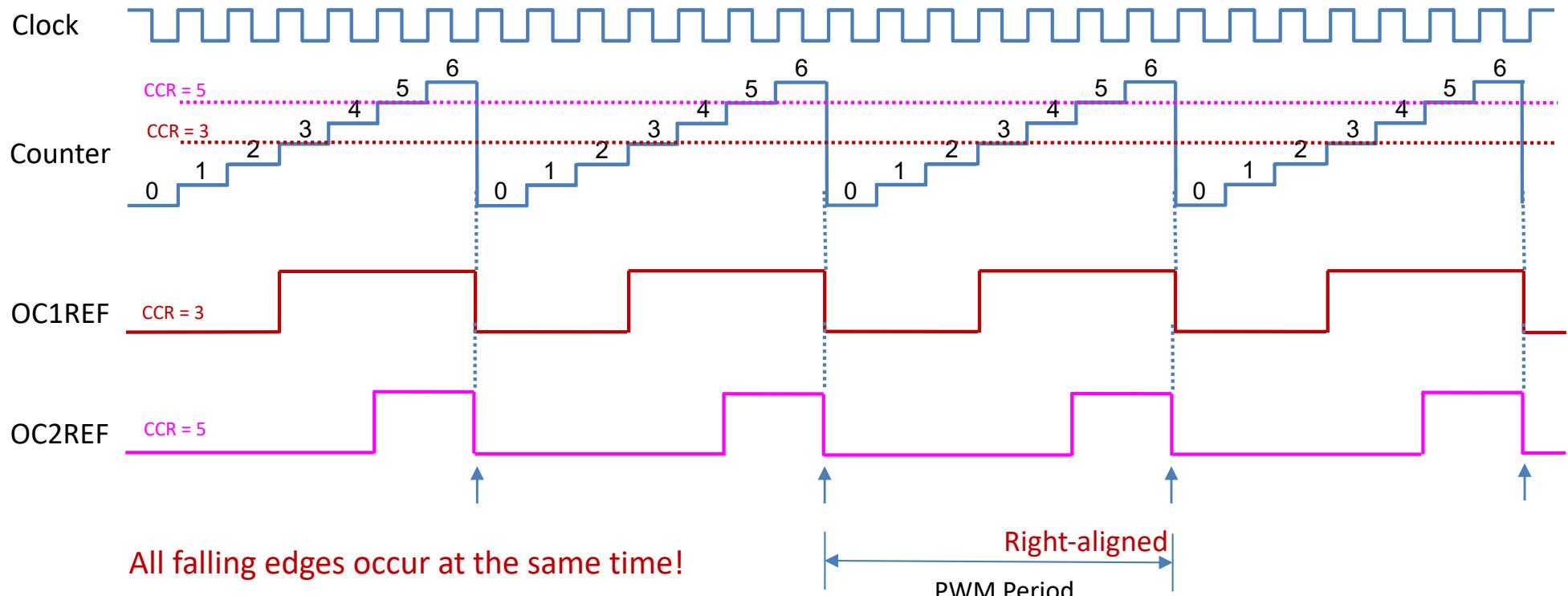
Up-Counting: Left Edge-aligned

Upcounting mode, ARR = 6, CCR = 3, RCR = 0

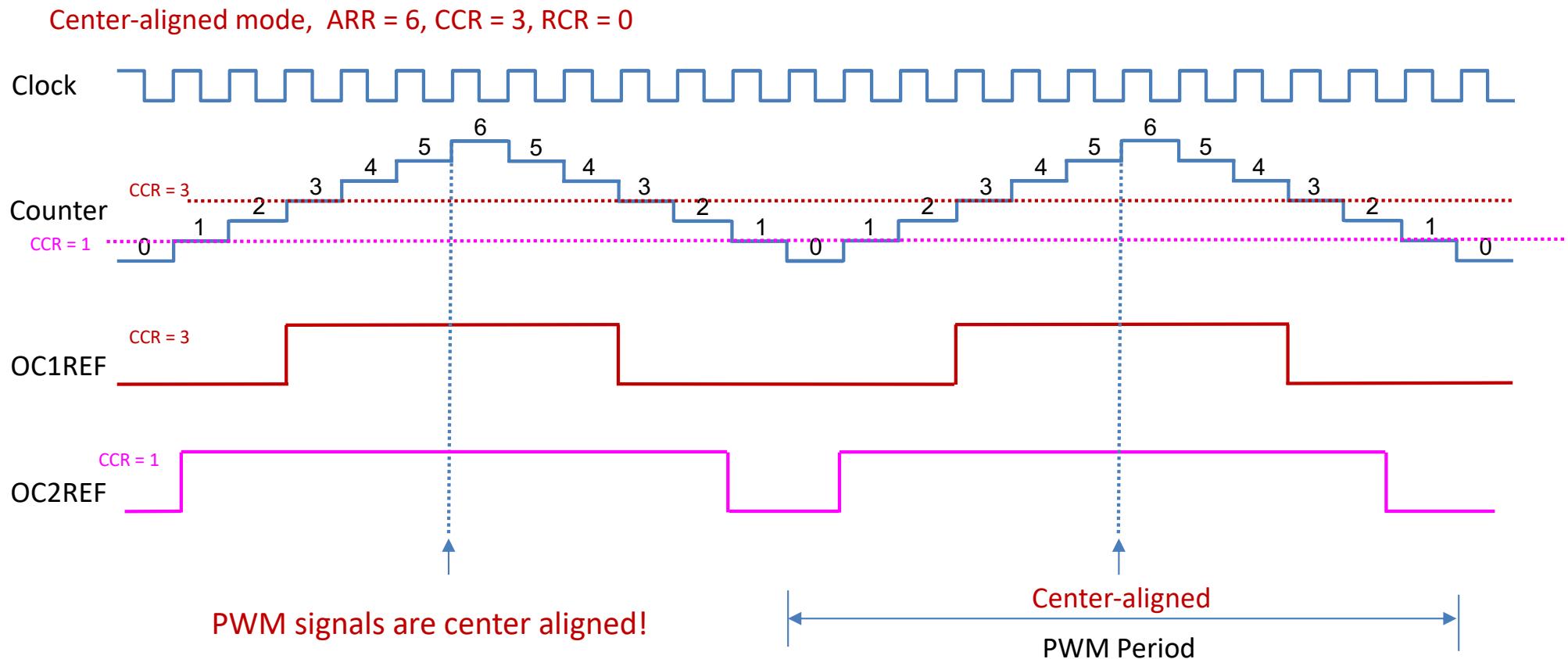


PWM Mode 2: Right Edge-aligned

Upcounting mode, ARR = 6, CCR = 3, RCR = 0



PWM Mode 2: Center Aligned



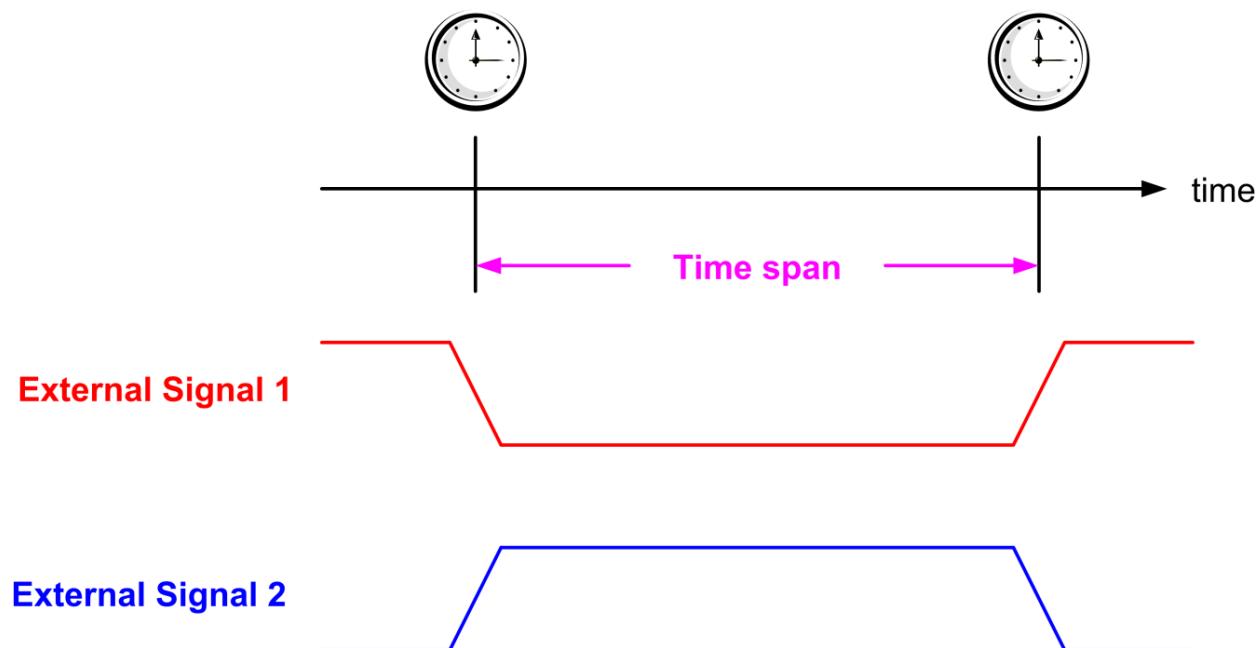
The devil is in the detail

- Timer output control
- Enable Timer Output
 - **MOE**: Main output enable
 - **OSSI**: Off-state selection for Idle mode
 - **OSSR**: Off-state selection for Run mode
 - **CCxE**: Enable of capture/compare output for channel x
 - **CCxNE**: Enable of capture/compare complementary output for channel x

Control bits					Output states ⁽¹⁾	
MOE bit	OSSI bit	OSSR bit	CCxE bit	CCxNE bit	OCx output state	OCxN output state
1	X	X	0	0	Output disabled (not driven by the timer: Hi-Z) OCx=0, OCxN=0	
		0	0	1	Output disabled (not driven by the timer: Hi-Z) OCx=0	OCxREF + Polarity OCxN = OCxREF xor CCxNP
		0	1	0	OCxREF + Polarity OCx=OCxREF xor CCxP	Output Disabled (not driven by the timer: Hi-Z) OCxN=0
		X	1	1	OCREF + Polarity + dead-time	Complementary to OCREF (not OCREF) + Polarity + dead-time
		1	0	1	Off-State (output enabled with inactive state) OCx=CCxP	OCxREF + Polarity OCxN = OCxREF x or CCxNP
		1	1	0	OCxREF + Polarity OCx=OCxREF xor CCxP	Off-State (output enabled with inactive state) OCxN=CCxNP
0	X	0	X	X	Output Disabled (not driven by the timer: Hi-Z) OCx=CCxP, OCxN=CCxNP	
		0	0			
		0	1		Off-State (output enabled with inactive state) Asynchronously: OCx=CCxP, OCxN=CCxNP (if BRK or BRK2 is triggered).	
		1	0			
		1	1		Then (this is valid only if BRK is triggered), if the clock is present: OCx=OISx and OCxN=OISxN after a dead-time, assuming that OISx and OISxN do not correspond to OCX and OCxN both in active state (may cause a short circuit when driving switches in half-bridge configuration). Note: BRK2 can only be used if OSSI = OSSR = 1.	

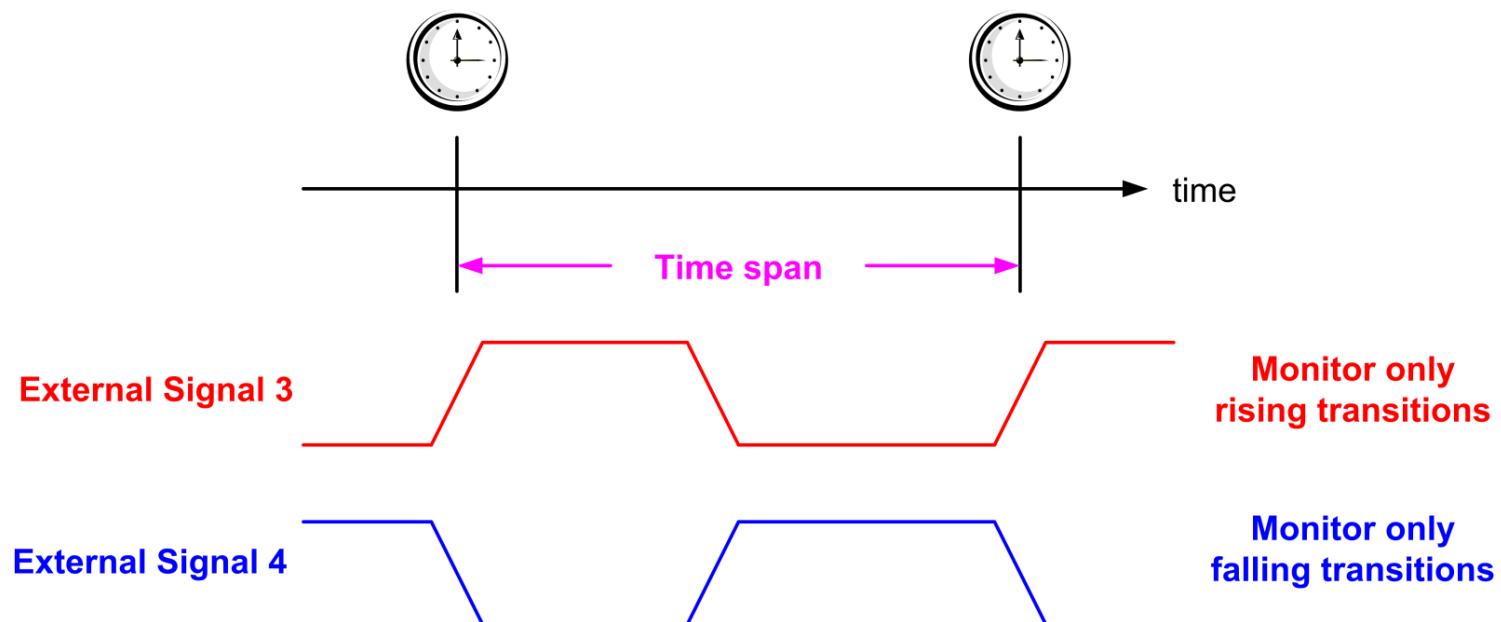
Input Capture

- Monitor both rising and falling edge

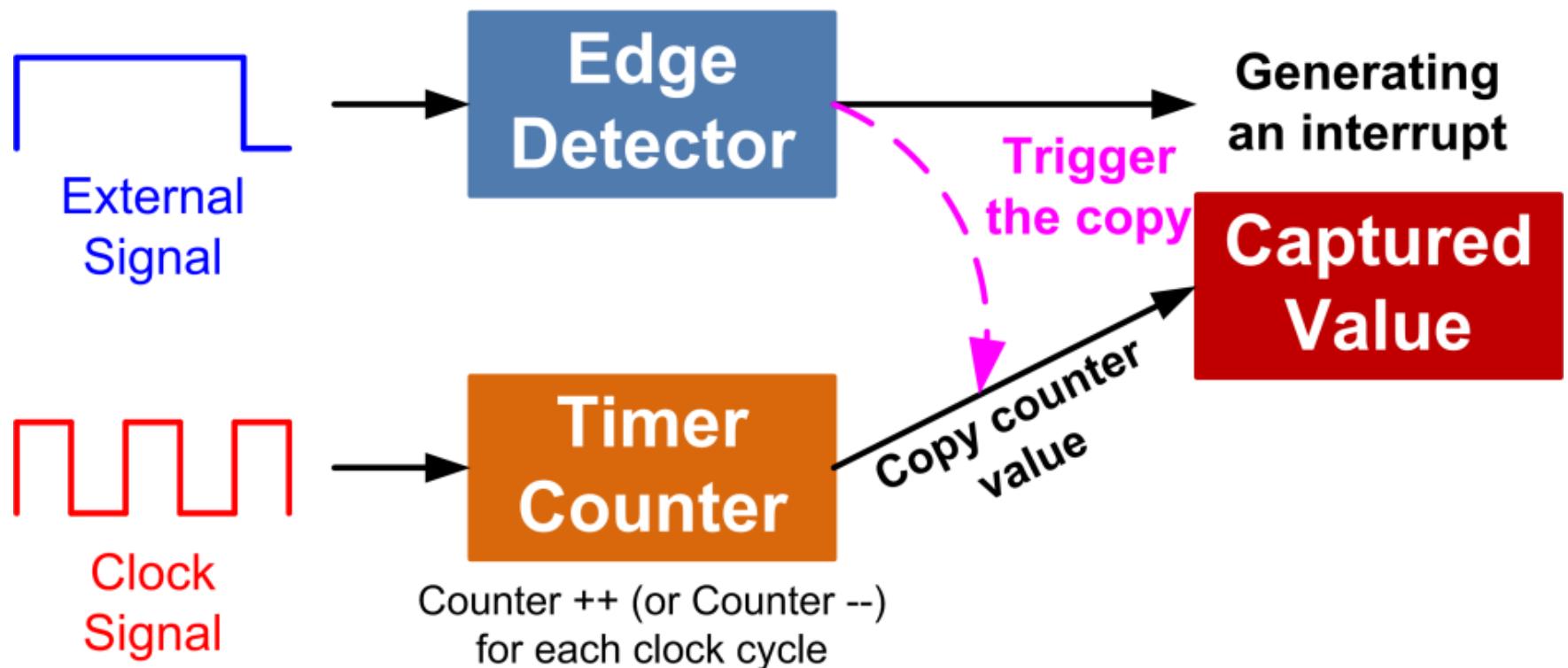


Input Capture

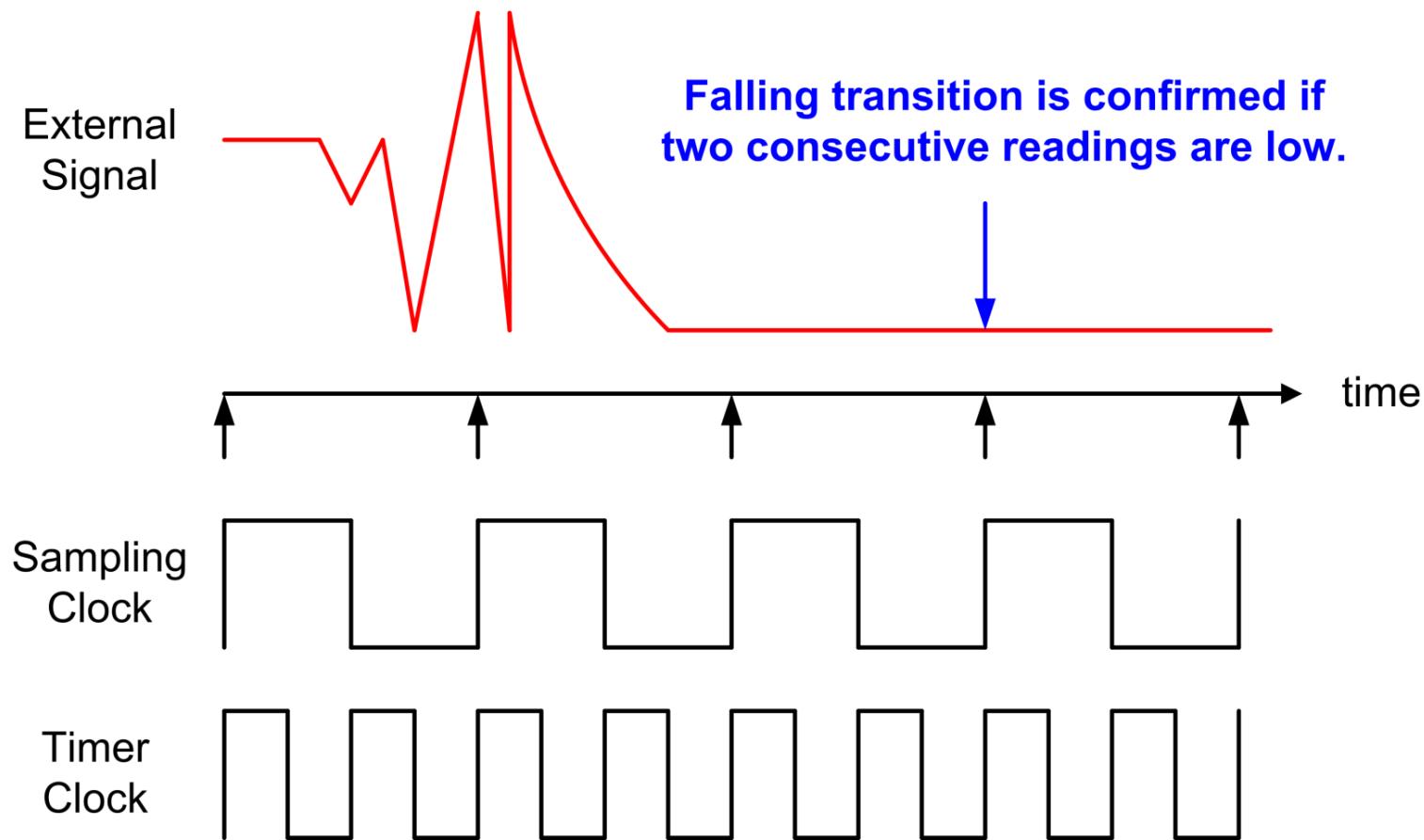
- Monitor only rising edges or only falling edge



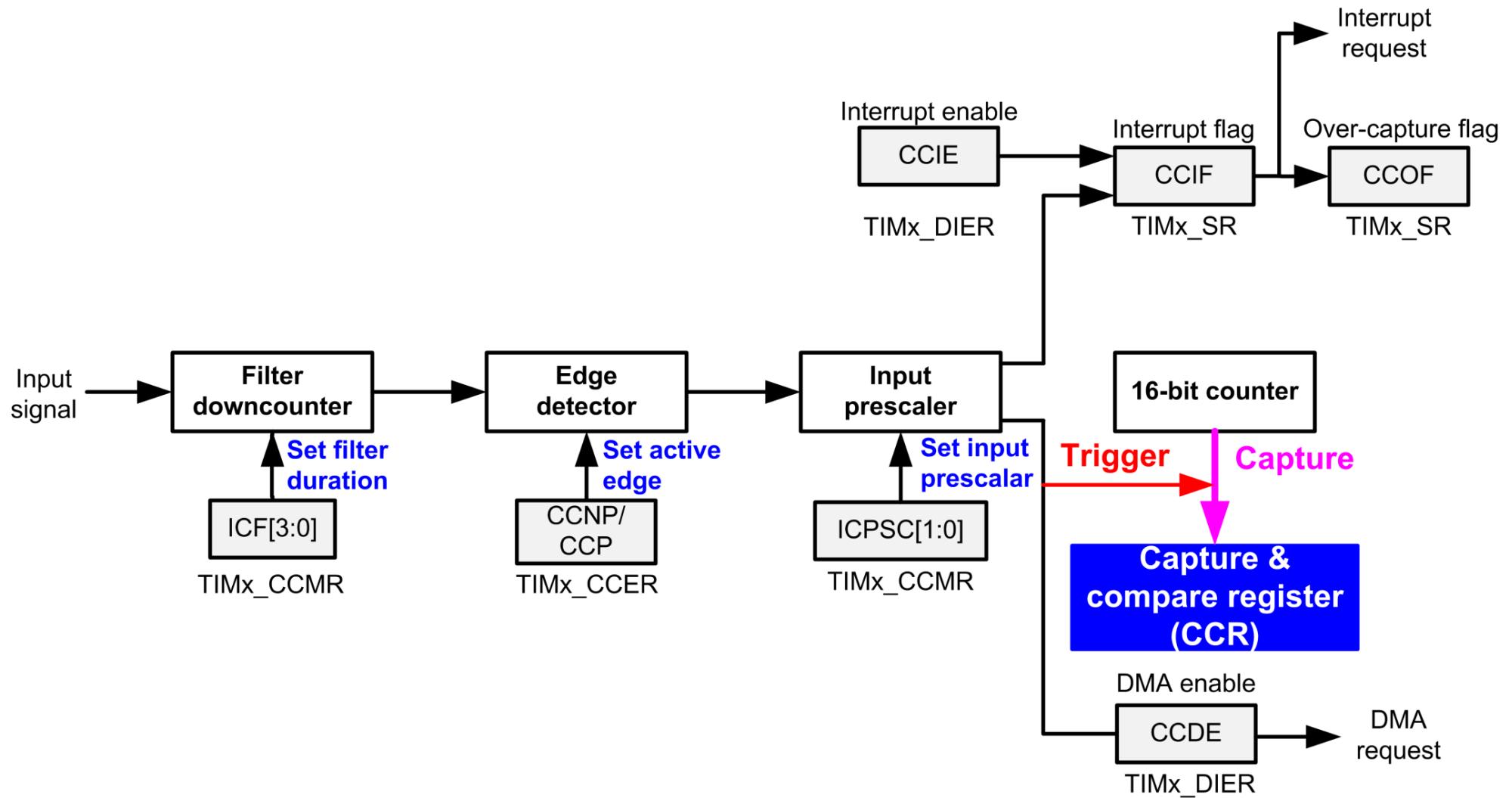
Input Capture



Input Filtering



Input Capture Diagram

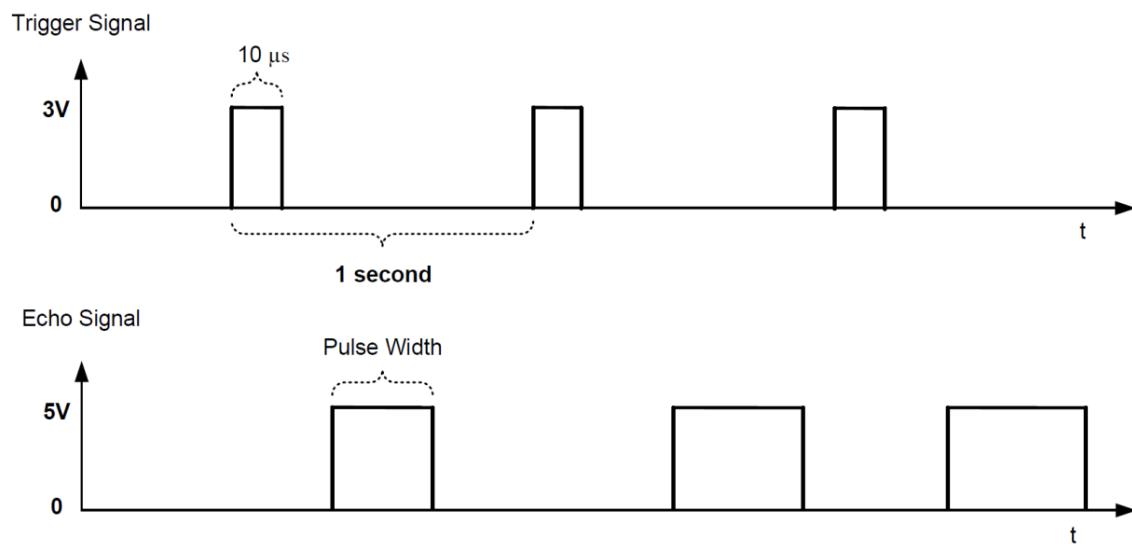


Ultrasonic Distance Sensor



$$\begin{aligned} \text{Distance} &= \frac{\text{Round Trip Time} \times \text{Speed of Sound}}{2} \\ &= \frac{\text{Round Trip Time}(\mu\text{s}) \times 10^{-6} \times 340\text{m/s}}{2} \\ &= \frac{\text{Round Trip Time}(\mu\text{s})}{58} \end{aligned}$$

Ultrasonic Distance Sensor



The echo pulse width corresponds to round-trip time.

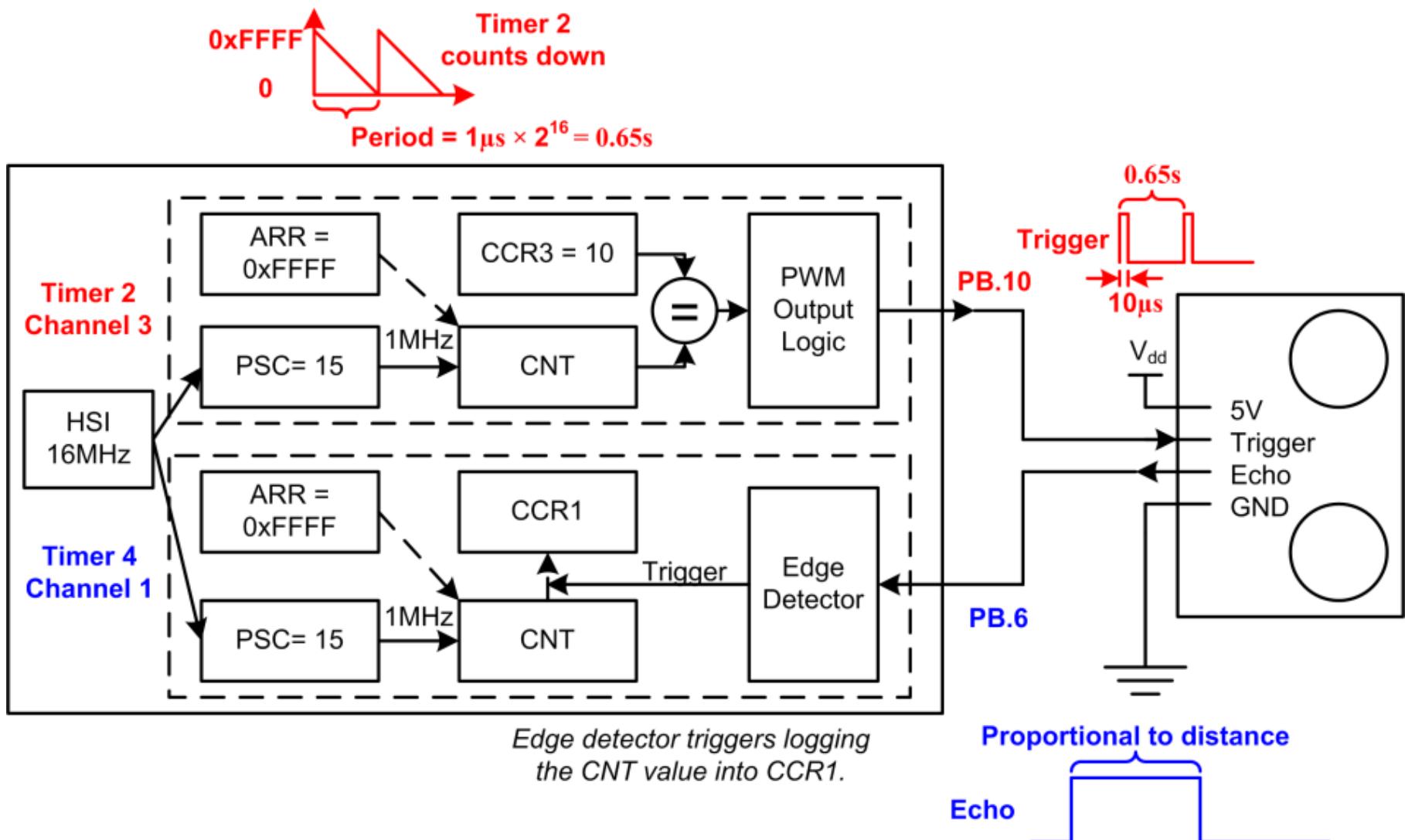
$$\text{Distance (cm)} = \frac{\text{Pulse Width} (\mu\text{s})}{58}$$

or

$$\text{Distance (inch)} = \frac{\text{Pulse Width} (\mu\text{s})}{148}$$

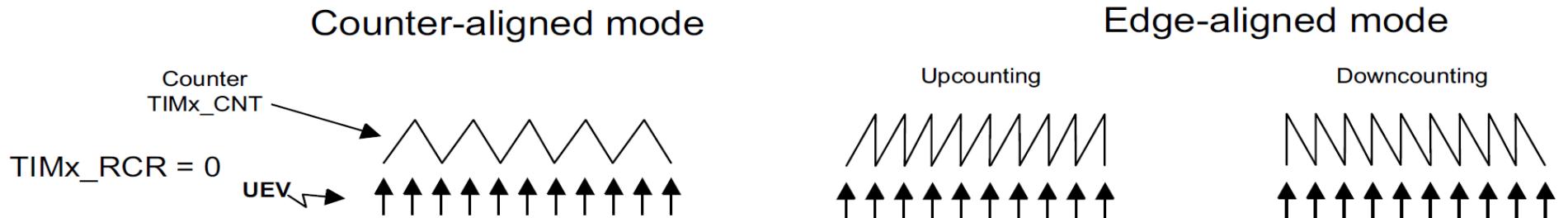
If pulse width is 38ms,
no obstacle is detected.

Ultrasonic Distance Sensor

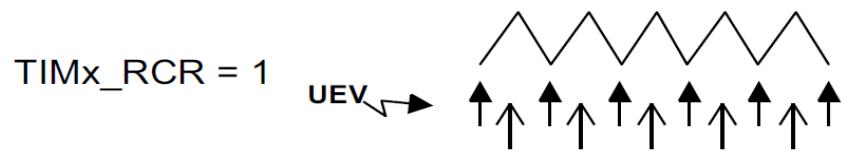
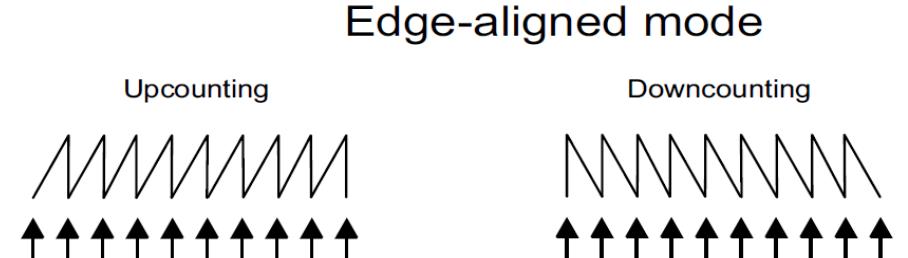
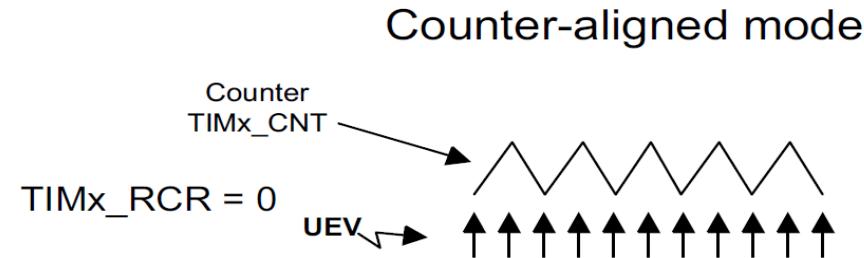


Later

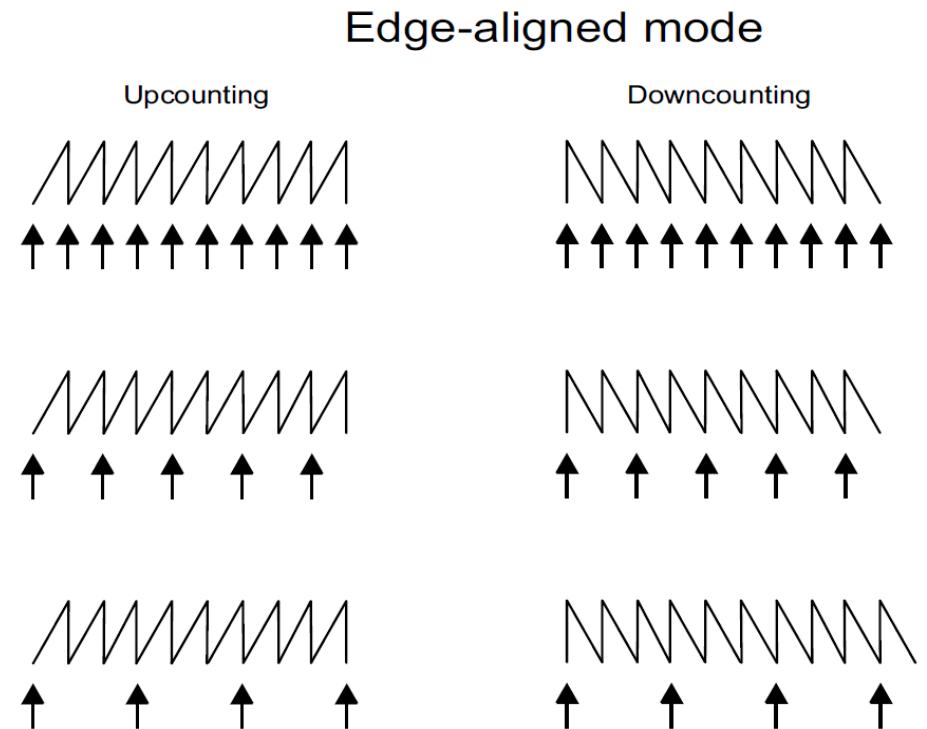
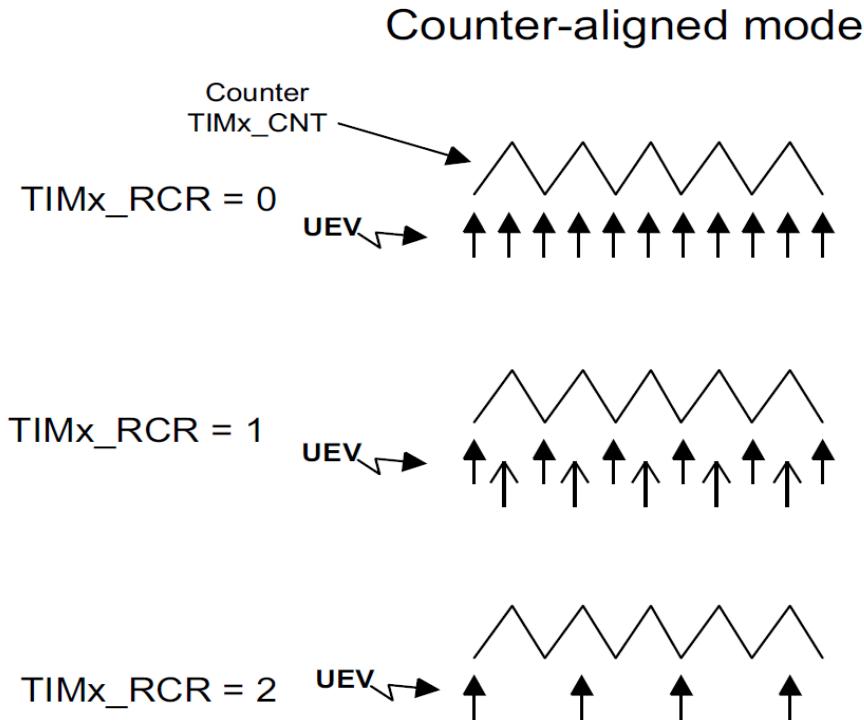
Repetition Counter Register (PCR)



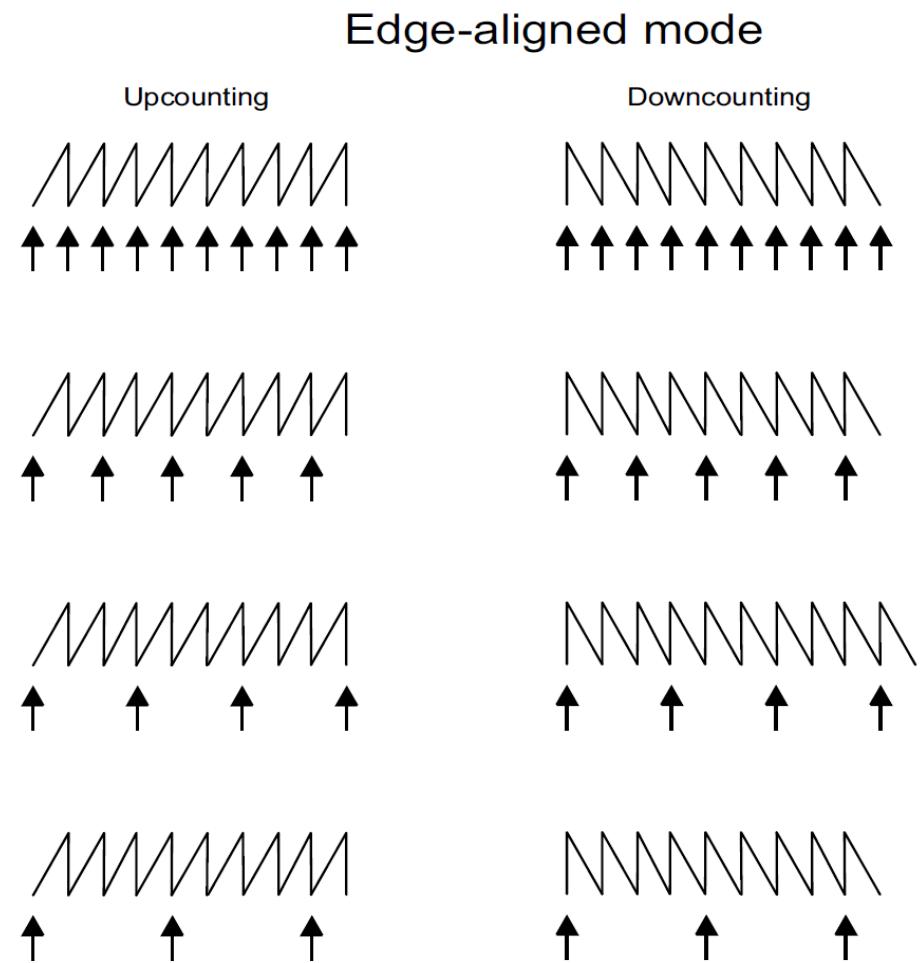
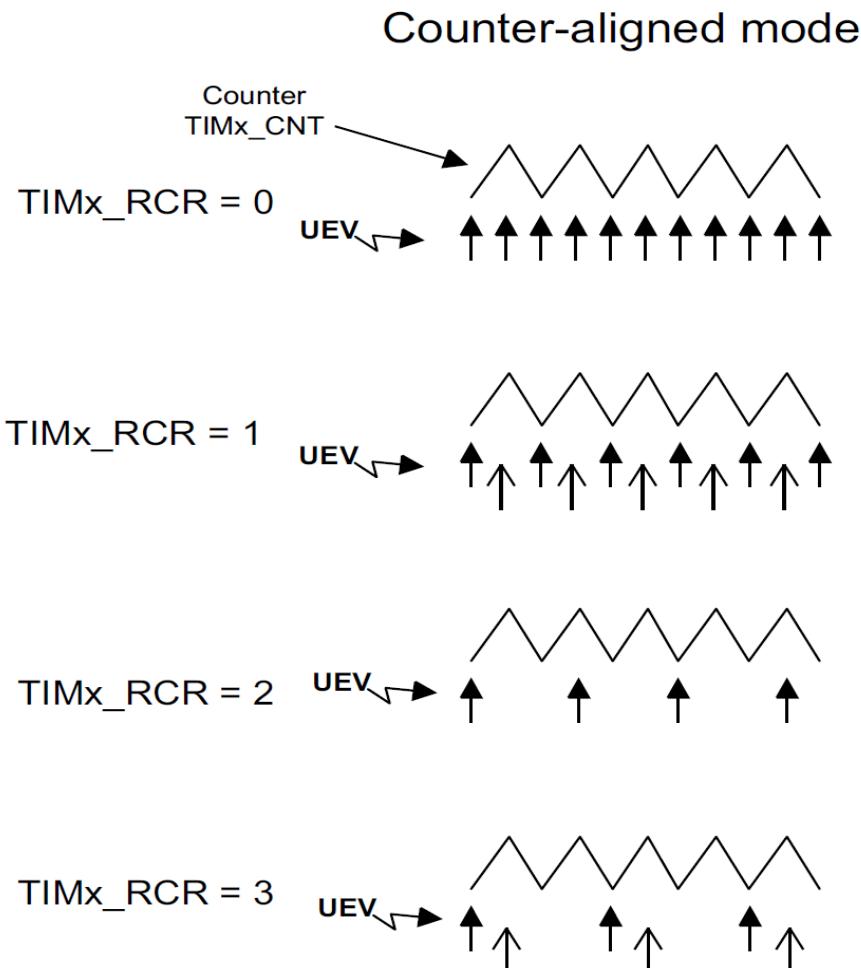
Repetition Counter Register (PCR)



Repetition Counter Register (RCR)



Repetition Counter Register (PCR)



Repetition Counter Register (PCR)

