Batch2

SRM Institute of Science and Technology
College of Engineering and Technology
School of Computing

Mode of Exam
ONLINE

Common to Computing Technologies/Networking and Communication/Computational Intelligence/Data science and Business systems

SRM Nagar, Kattankulathur – 603203, Chengalpattu District, Tamilnadu

Academic Year: 2021-22 (ODD)

Test: CLAT-3 **Date:** 31/01/2022
Course Code & Title: 18CSS201J – Analog and Digital Electronics **Duration:** 100 Mins
Year & Sem: II & III **Max. Marks:** 50

Course Articulation Matrix:

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	H	H													
CO2	H	H													
CO3	H		H	H											
CO4	H	H	H	H	H							H			
CO5	H		H	H	H										
CO6			H	H		H			H						

Part - A
(30 x 1 Marks = 30 Marks)

Instructions: Answer all the questions

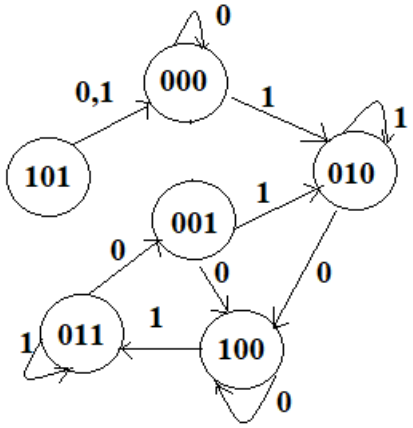
Q. No	Question	Marks	BL	CO	PO	PI Code
1	In a SR Flip-Flop, indeterminate state means (A) Set Q = 1 and Q = 0. (B) Set Q = 0 and Q = 1. (C) input SR are equal to 0 (D) input SR are equal to 1 ANS: D	1	2	4	1	1.6.1
2	The output of JK flip flop when J=1, K=0 is (A) 1 (B) 0 (C) No change (D) High impedance ANS: A	1	1	4	1	1.6.1
3	The fastest operation among the given circuits is (A) counter (B) shift register (C) Synchronous circuit (D) multiplexer ANS: D	1	2	4	1	1.6.1
4	Which of the following statement is FALSE with respect to synchronous circuit (A) The flip flops are used as delays (B) The output of the system may/ may not depend on the states (C) The same clock is shared by all the flip flops (D) State diagram and state table are a part of the system design ANS: A	1	2	4	1	1.6.1

5	The present output Qn of an edge triggered JK flip-flop is logic 1. If K=1, then Qn+1 will be (A) 0 (B) 1 (C) don't care (D) can't be determined ANS: A	1	3	4	1,2	1.6.1
6	The input and control signals to a T flip flop are T= 1, $\overline{\text{PRESET}}$ = 0, $\overline{\text{CLEAR}}$ = 1, (assume Q=1) then the output of the flip flop will be (A) 0 (B) 1 (C) don't care (D) can't be determined ANS: B	1	2	4	1,2	1.6.1
7	A 'T' flip-flop with T= 1 has an 80 kHz clock input. The output Q will have _____ (A) constant low (B) frequency 20kHz (C) frequency 40kHz (D) constant high ANS: C	1	3	4	1,2	1.6.1 2.5.1
8	Connecting a _____ gate at the inputs of SR flip flop eliminates the indeterminate state. (A) OR Gate (B) AND Gate (C) Inverter (D) NOR ANS: C	1	2	4	2	1.6.1
9	Any two states of a synchronous sequential circuit is said to be 'Equivalent' if (A) for every input the outputs are the same (B) for every input the outputs and next states are the same (C) for every input the next states are the same (D) for every input the outputs may be different but the next states are the same ANS: B	1	1	4	1	1.6.1
10	Identifying the equivalent states and eliminating then while designing a synchronous sequential circuit can help (A) reduce the complexity in design (B) increasing the number of flip flops used (C) understand the circuit (D) reducing the number of flip flops used ANS: A	1	2	4	1	1.6.1
11	In SR flip-flop, "no change" condition appears when (A) S = 1, R = 1 (B) S = 1, R = 0 (C) S = 0, R = 1 (D) S = 0, R = 0	1	1	4	1,2	1.6.1

	ANS: D					
12	In a edge triggered T flip-flop, if clock input is level high and the input is 1, the output will be (A) the same (B) high (C) low (D) don't care ANS: A	1	2	4	1,2	1.6.1
13	The characteristic equation of J-K flip-flop is (A) Q(n+1)=JQ(n)+K'Q(n) (B) Q(n+1)=J'Q(n)+KQ'(n) (C) Q(n+1)=JQ'(n)+KQ(n) (D) Q(n+1)=JQ'(n)+K'Q(n) ANS: D	1	1	4	1	1.6.1
14	If JK flip flop toggles more than once in a cycle, it is called (A) Toggling (B) Racing (C) Bouncing (D) Cycle ANS: B	1	2	4	1	1.6.1
15	_____ is an example of sequential circuit. (A) ROM (B) Shift register (C) PLA (D) CPLD ANS: B	1	1	4	1	1.6.1
16	A four-bit serial in serial out right shift register is initialized to a value 1000. Identify the minimum number of clock pulses required to obtain 1011 from the initial value. A. 2 B. 3 C. 4 D. 5 Ans: B	1	3	5	1,3	1.6.1 2.5.1
17	"Shift-Left" operation can be performed in a universal shift register by selecting ____ for S_0S_1 selection lines. A. 00 B. 01 C. 10 D. 11 Ans: B	1	3	5	1,3	1.6.1
18	How many flip-flops are required to design a Modulus – 11 counters? A. 2 B. 3 C. 4 D. 5	1	2	5	1,2	1.6.1

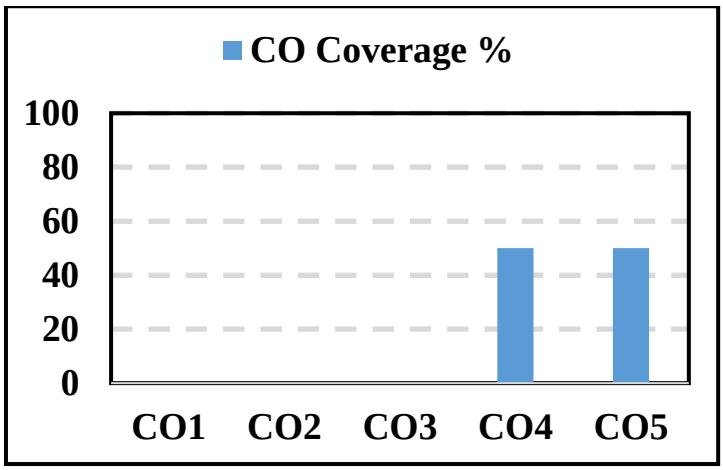
	Ans: C					
19	A 3-bit counter has a maximum modulus of _____ . A. 3 B. 6 C. 8 D. 16 Ans: C	1	2	5	1	1.6.1
20	The full form of PISO in PISO shift register is _____ . A. Peripheral In Serial Out B. Parallel In Serial Out C. Parallel Out Serial In D. Serial Out Parallel In Ans: B	1	1	5	1	1.6.1
21	The final decimal number count in a counter designed with 8 flip-flops is A. 255 B. 256 C. 31 D. 32 Ans: A	1	2	5	1,2	1.6.1 2.5.1
22	Which is not an analog to digital converter? A. Flash type converter B. Counter type converter C. R – 2R ladder converter D. Successive approximation converter Ans: C	1	1	5	1	1.6.1
23	How many numbers of op-amp comparators are required in 3-bit flash type analog to digital converter? A. 3 B. 6 C. 7 D. 8 Ans: C	1	2	5	1	1.6.1
24	The main disadvantage of dual slope ADC is A. Low accuracy B. High maintenance C. Long conversion time D. Better efficiency Ans: C	1	1	5	1	1.6.1
25	What is the smallest change in voltage which may be produced at the output due to the step change in the input of the digital to analog converter? A. Linearity B. Accuracy C. Monotonicity D. Resolution	1	1	5	1	1.6.1

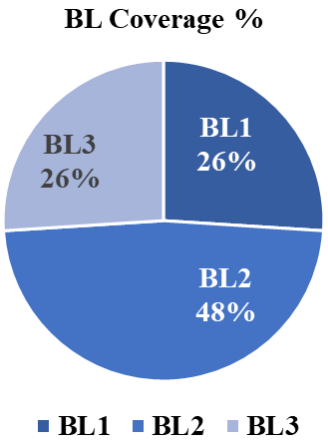
	Ans: D					
26	In the flash type ADC, each comparator output is connected to an input of _____. A. priority encoder B. multiplexer C. demultiplexer D. decoder Ans: A	1	2	5	1	1.6.1
27	The final count of a modulus-12 binary counter is__. A. 1000 B. 1100 C. 1010 D. 1011 Ans: D	1	2	5	1,2	1.6.1 2.5.1
28	A digital volt meter uses a _____ . A. Flash ADC B. Dual slope ADC C. successive approximation ADC D. sigma-delta ADC Ans: B	1	1	5	1	1.6.1
29	Binary weighted DACs are limited to _____ resolution. A. 4-bit B. 6-bit C. 8-bit D. 16-bit Ans: C	1	3	5	1,2	1.6.1
30	In a seven-segment common anode display, anodes of all LEDs are connected to A. Logic 0 B. Logic 1 C. Ground D. Minus 5 V Ans: B	1	1	5	1	1.6.1
Part – B **(10 x 2 Marks = 20 Marks)** **Instructions: Answer all the questions**						
31	The input to a JK flip flop is given as J=1 and K=Q'. Assume Q=0 initially. The sequence at the output of the flip flop upon application of 4 clock pulses will be _____. (A) 1010 (B) 1111 (C) 1000 (D) 1100 ANS: B	2	3	4	1,3	1.6.1 2.5.1
32	The relation between the output Q and the inputs SR is given by (A) Qn(S+R') + SQn'	2	1	4	1	1.6.1

	(B) Qn'(S+R') + RQn (C) Qn'(S+R') + SQn (D) Qn(S'+R) + SQn' ANS: A					
33	To design the synchronous circuit shown in the figure with JK flip flops, _____ number of Kmaps are required.  (A) 3 (B) 6 (C) 4 (D) 5 ANS: B	2	2	4	1,3	1.6.1
34	The state table of a synchronous circuit is given. As a part of the logic circuit design with T flip flops, the input to flip flop B is given as Present state | Next state A B C | A+ B+ C+ 0 0 0 | 1 1 1 1 1 0 | 1 0 0 0 1 1 | 1 1 0 1 0 0 | 0 1 1 1 1 1 | 0 0 0 (A) TB = A+C' (B) TB = C' (C) TB = A'+B' (D) TB = C+B' ANS: A	2	3	4	1,3	1.6.1 2.5.1
35	A JK flip flop can be made to work as D flip flop when (A) J=K (B) J=K=0 (C) J=K' (D) J=K=1 ANS: C	2	2	4	1	1.6.1
36	A five-bit serial in parallel out (right) shift register is initially cleared with 00000. Input binary number to the same is 11011. After three clock pulses, what will be the output of the shift register?	2	3	5	1,2	1.6.1 2.5.1

	A. 11000 B. 11011 C. 01100 D. 00110 Ans: C					
37	Input binary number to the 4-bit parallel in parallel out shift register is 1001. How many minimum number of clock pulses required to obtain same 1001 at the output? A. 1 B. 2 C. 3 D. 4 Ans: A	2	2	5	1	1.6.1 2.5.1
38	Initial count of the four bit up-counter is 0101. What will be the output of the counter after four clock pulses? A. 0111 B. 1000 C. 1001 D. 1010 Ans: C	2	2	5	1,2	1.6.1 2.5.1
39	Which counters are used for minutes in digital clock? A. Mod 2 & Decade counters B. Mod 8 & Decade counters C. Mod 6 & Decade counters D. Mod 5 & Decade counters Ans: C	2	2	5	1,2	1.6.1
40	What is the step size of 5- bit DAC operating with a full-scale voltage of 10 V? A. 0.32 V B. 0.31 V C. 0.62 V D. 0.2 V Ans: A	2	3	5	1,3	1.6.1 2.5.1

Course Outcome (CO) and Bloom's level (BL) Coverage in Questions





Approved by the Audit Professor/Course Coordinator