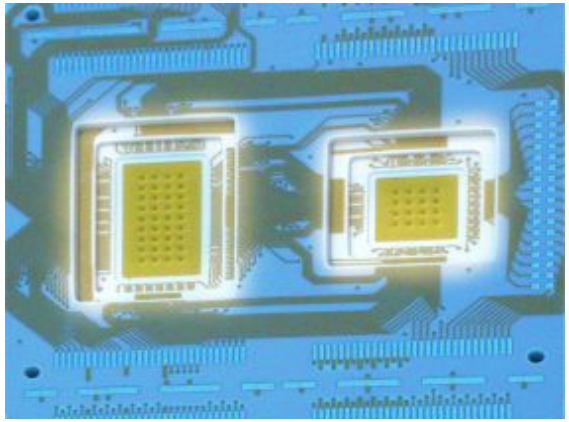
UNIT-II

LOGIC FAMILIES

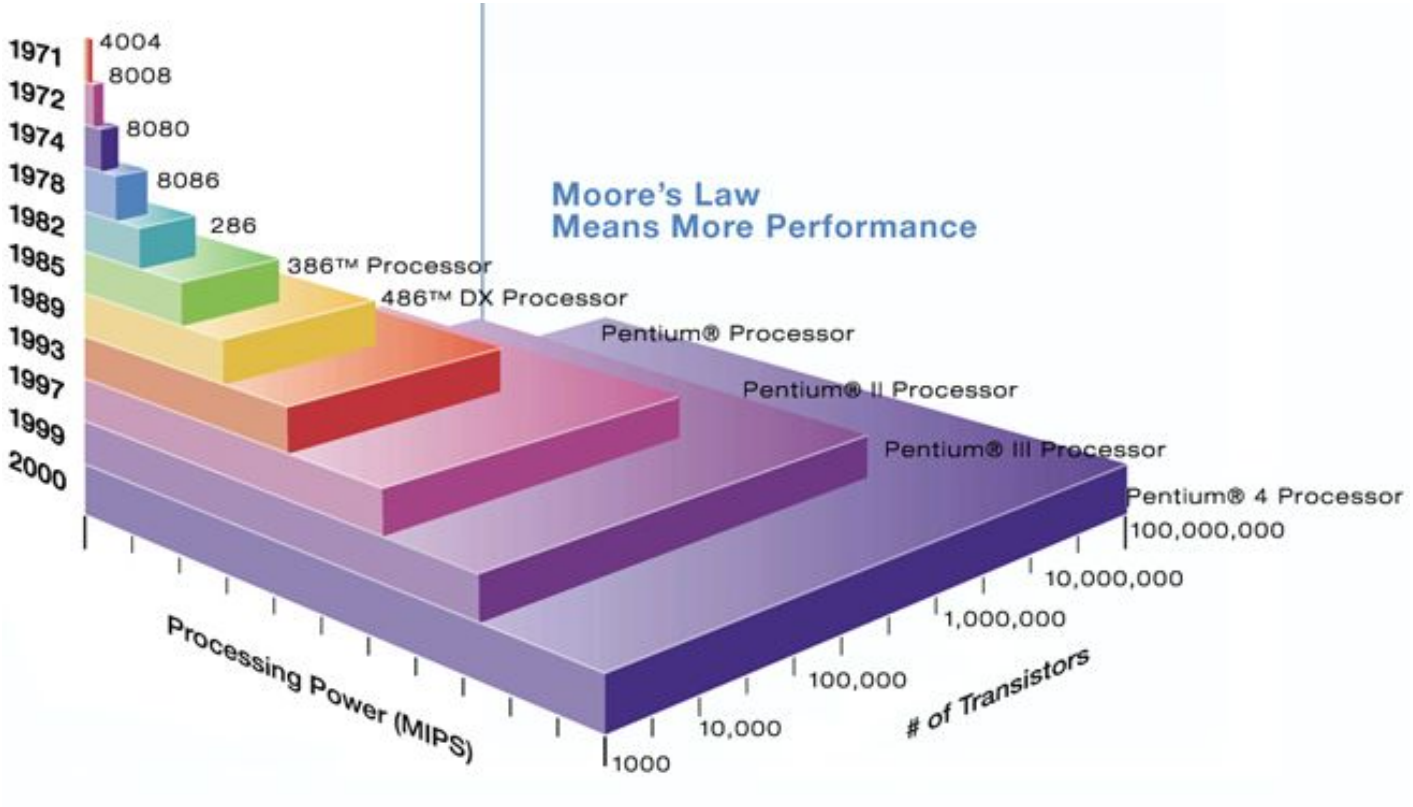
Integration Levels

- Gate/transistor ratio is roughly 1/10
  - SSI(Small Scale Integration) < 12 gates/chip
  - MSI(Medium Scale Integration) < 100 gates/chip
  - LSI(Large Scale Integration) …1K gates/chip
  - VLSI(Very Large Scale Integration)…10K gates/chip
  - ULSI(Ultra Large Scale Integration)…100K gates/chip
  - GSI(Giant Scale Integration) …1Meg gates/chip



Moore's law

- A prediction made by Moore (a co-founder of Intel) in 1965: "a number of transistors to double every 2 years."



Positive logic

Positive logic: H is set to be binary 1

L is set to be binary 0

Inputs		Output
x	y	z
L	L	H
L	H	H
H	L	H
H	H	L

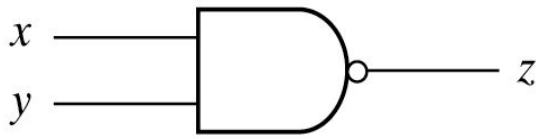


Fig. 10-1 Positive Logic NAND Gate

Negative logic

Negative logic: L is set to be binary 1

H is set to be binary 0

INPUT		OUTPUT
X	Y	Z
H	H	L
H	L	L
L	H	L
L	L	H

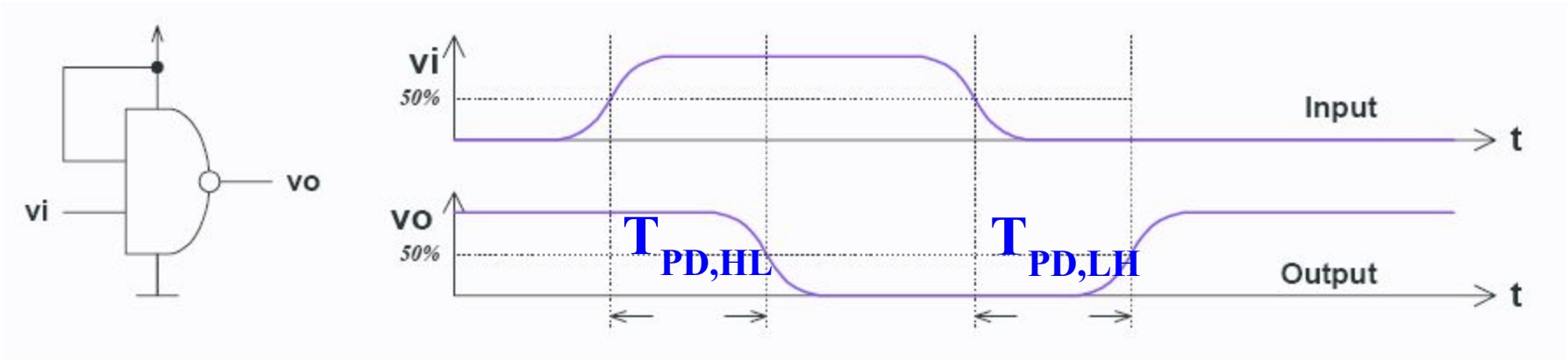
Digital IC specifications (or) characteristics of digital logic families

- The most useful specifications or feature to be concerned of IC logic families:
  - Threshold voltage
  - Propagation delay
  - Power dissipation
  - Fan-in
  - Fan-out
  - Voltage and current requirement
  - Noise Margin
  - Operating temperature
  - Speed power product

Digital IC Specifications

- Threshold voltage: The voltage at the input of a gate which causes a change in the state of the output from one logic level to the other.
- Propagation delay: Time interval b/w the application of an i/p pulse & occurrence of resulting o/p pulse.
  - The average *transition-delay time* for the signal to propagate from input to output when the binary signal changes in value.
  - A pulse through a gate takes a certain amount of time to propagate from input to output. This interval of time is known as the propagation delay of the gate.
  - Average transition delay time tpd = (tPLH + tPHL) /2

Logic families: propagation delay



$T_{PD,HL}$ – input-to-output propagation delay from HI to LO output

$T_{PD,LH}$ – input-to-output propagation delay from LO to HI output

Power dissipation

- Every logic gate draws some current from the supply for its operation
- The current drawn in HIGH state is different from that drawn in LOW state.
- Power dissipation of a logic gate is the power required by the gate to operate with 50% duty cycle at specified frequency.
- The power needed by the gate expressed in mW
- Pd=Vcc*Icc(avg)/n. where Vcc is the gate supply voltage, Icc(avg) is the average current drawn from the supply by the entire IC, n is the number of gates in the IC.
- Icc(avg) = (ICCH+ICCL)/2
- ICCH-current drawn by the IC when all the gates in the IC are in HIGH state, ICCL-current drawn by the IC when all the gates in the IC are in LOW state,
- Total power consumed by an IC is equal to the product of the power dissipated by each gate and the no. of gates in that IC.

Fan-in and Fan-out

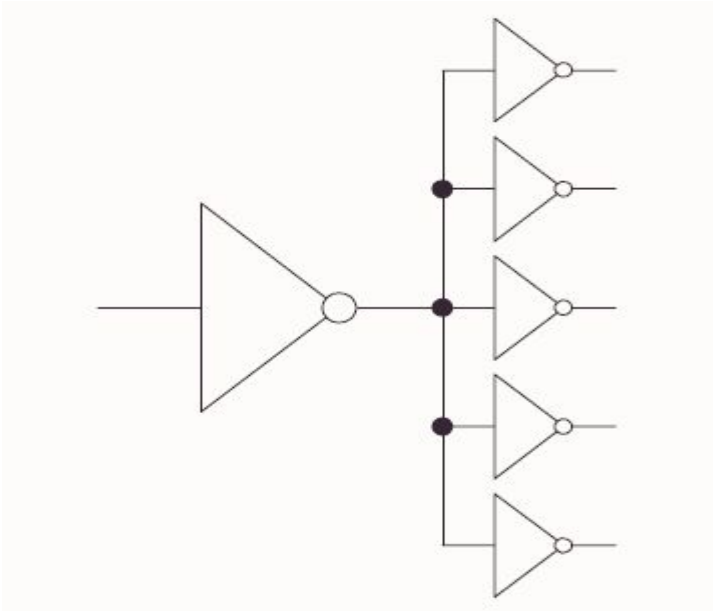
- Fan-in :The fan-in of a logic gate is defined as the number of inputs that the gate is designed to handle.

- Fan-out: The number of standard loads can be connected to the output of the gate without degrading its normal operation. Sometimes the term *loading* is used

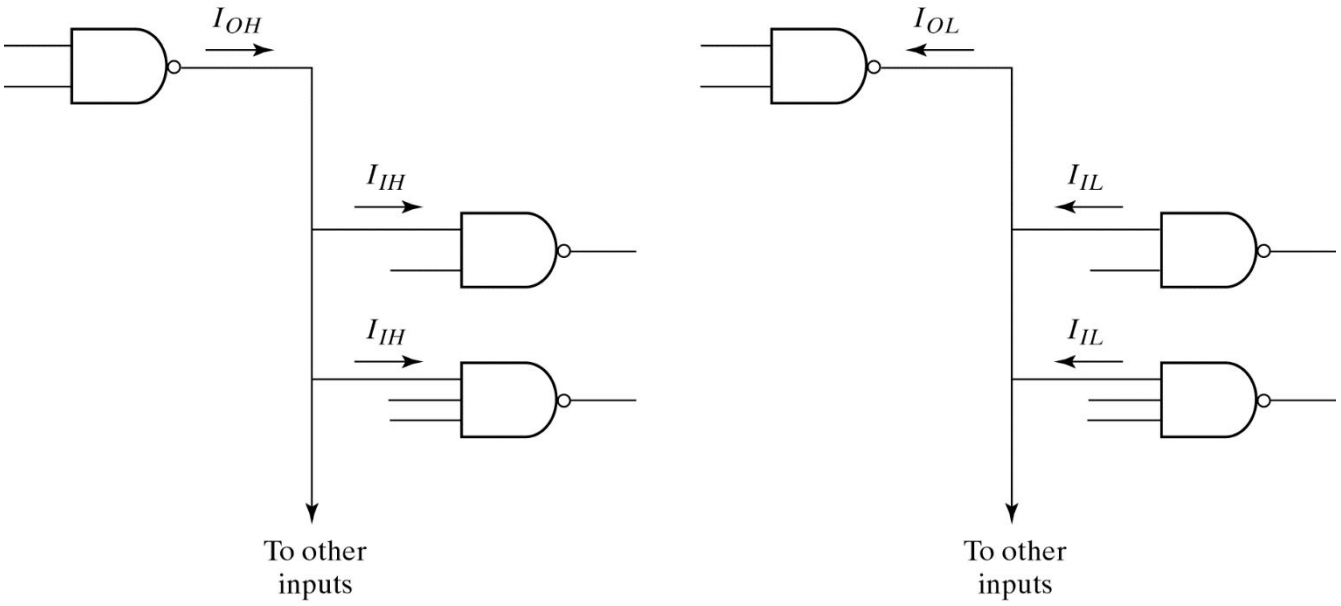
  - High state fan-out : the fan-out of the gate when its output is logic 1-driving gate sources current
  - Low state fan-out : the fan-out of the gate when its output is logic 0- driving gate sinks current
  - Actual fan out is smaller of these two numbers.

Logic families: fanout

Fanout: the maximum number of logic inputs (of the same logic family) that an output can drive reliably



Computing fan-out



(a) High-level output

(b)Low-level output

Fig. 10-3 Fan-Out Computation

$$Fan\text{-}out = \min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$$

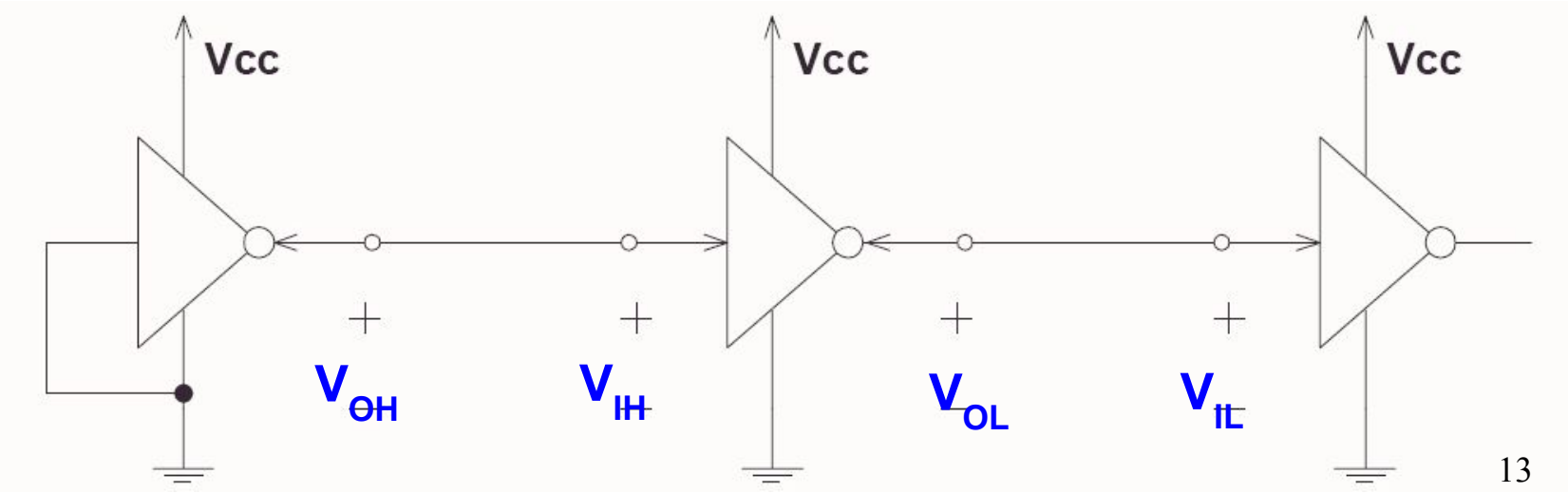
Logic families: Voltage levels

V_{OH}(min) – The minimum voltage level at an output in the logical "1" state under defined load conditions

V_{OL}(max) – The maximum voltage level at an output in the logical "0" state under defined load conditions

V_{IH}(min) – The minimum voltage required at an input to be recognized as "1" logical state

V_{IL}(max) – The maximum voltage required at an input that still will be recognized as "0" logical state



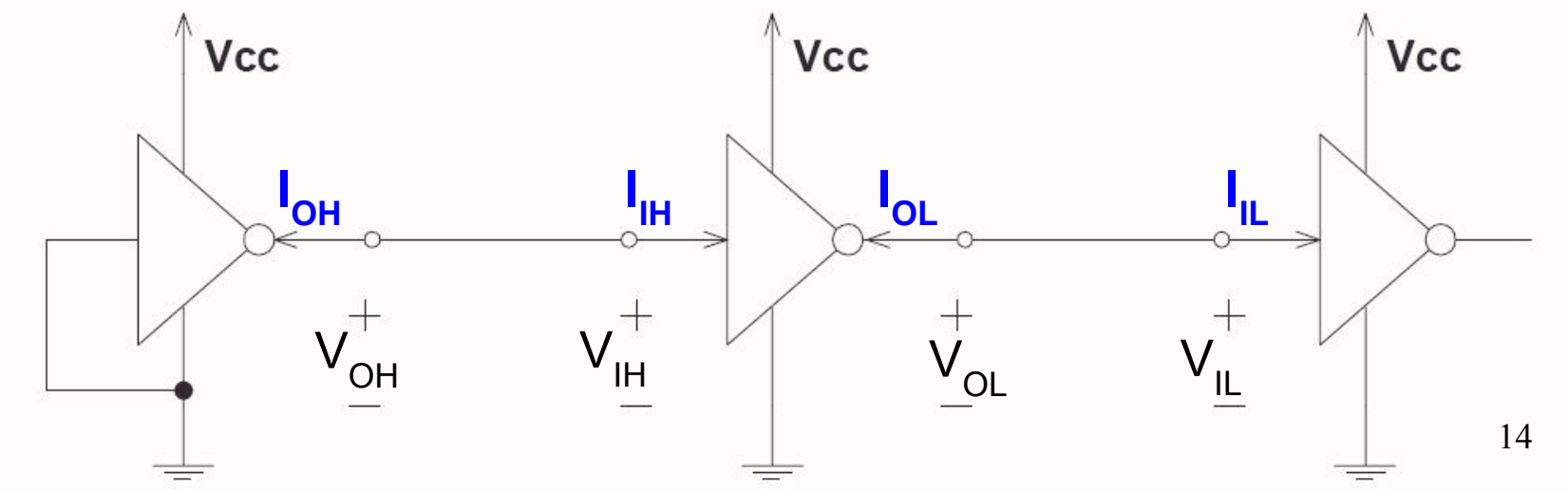
Logic families: current requirements

I_{OH} – Current flowing into an output in the logical "1" state under specified load conditions

I_{OL} – Current flowing into an output in the logical "0" state under specified load conditions

I_{IH} – Current flowing into an input when a specified HI level is applied to that input

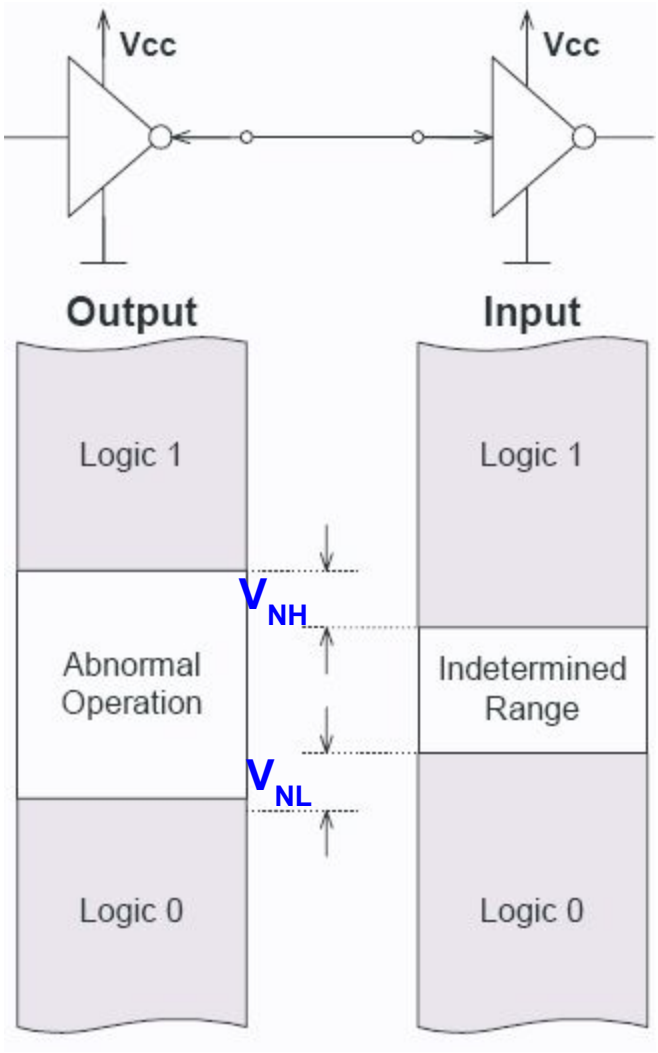
I_{IL} – Current flowing into an input when a specified LO level is applied to that input



Noise margin

- The unwanted signals are referred to as *noise*
- Noise margin is the *maximum noise* added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output .
- High state noise margin is the difference between the lowest possible high output and the minimum input voltage required for a HIGH.
- Low state noise margin is the difference between the largest possible low output and the maximum input voltage required for a LOW.

DC Noise margins



HI state noise margin:

$V_{NH} = V_{OH}(min) - V_{IH}(min)$

LO state noise margin:

$V_{NL} = V_{IL}(max) - V_{OL}(max)$

Noise margin:

$V_N = min(V_{NH}, V_{NL})$

Digital IC Specifications

- operating temperature

- The IC gates and other circuits are temperature sensitive.
- They are designed to operate satisfactorily over a specified range of temperature.
- Range for commercial application is 0° to70° C, industrial 0° to85° C and for military applications -55° to 125° C.

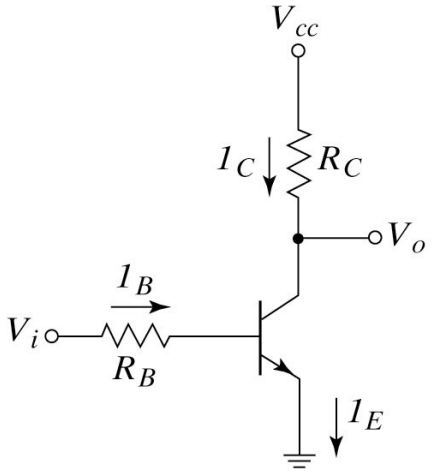
– Speed power product

- Multiply the gate propagation delay by the gate power dissipation
- Smaller value is desirable. The smaller value gives better overall performance.
- It has the units of energy and expressed in picco-joules
- The IC has an average propagation delay of 10ns and an average power dissipation of 5mw, the speed power product is
  10 ns*5mw=50*10^-12 watts-seconds= 50 picco-joules

Typical npn Transistor Parameters

Region	V_{BE} (V)	V_{CE} (V)	Current Relation
Cutoff	< 0.7	Open circuit	$I_B=I_C=0$
Active	0.7-0.8	> 0.8	$I_C=h_{FE}I_B$
Saturation	0.8-0.9	0.2	$I_B \geq I_C/h_{FE}$

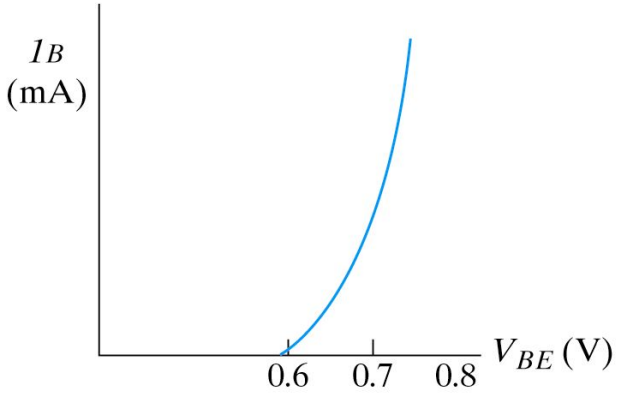
Feature of npn-type BJT



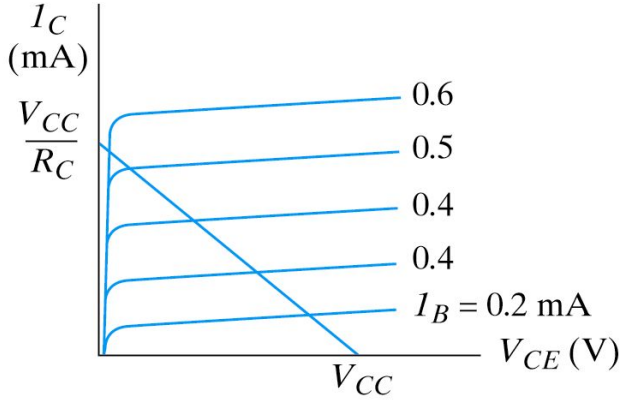
(a) Inverter circuit

Find V_o = ?

for $V_i = L$ and $V_i = H$



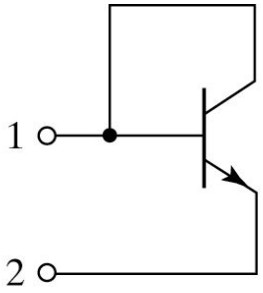
(b) Transistor-base characteristic



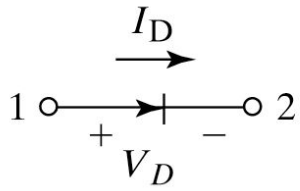
(c) Transistor-collector characteristic

Fig. 10-6 Silicon *npn* Transistor Characteristics

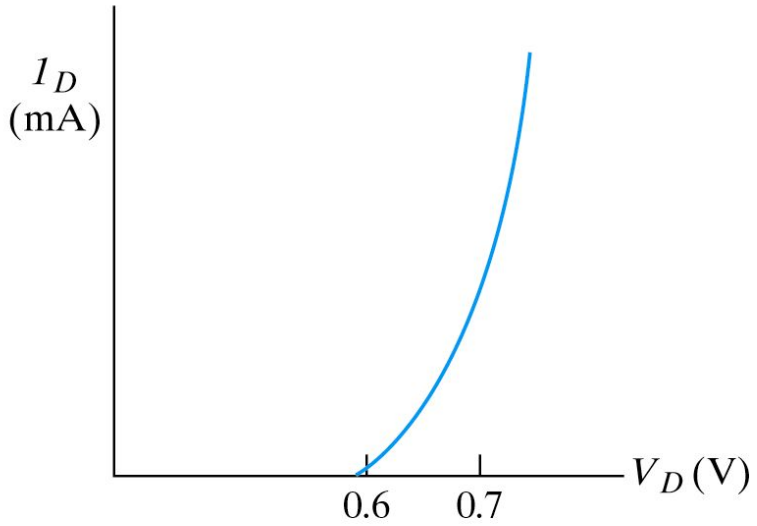
Diode – symbol and characteristic



(a) Transistor adapted for use as a diode



(b) Diode graphic symbol



(c) Diode characteristic

Fig. 10-7 Silicon Diode Symbol and Characteristic

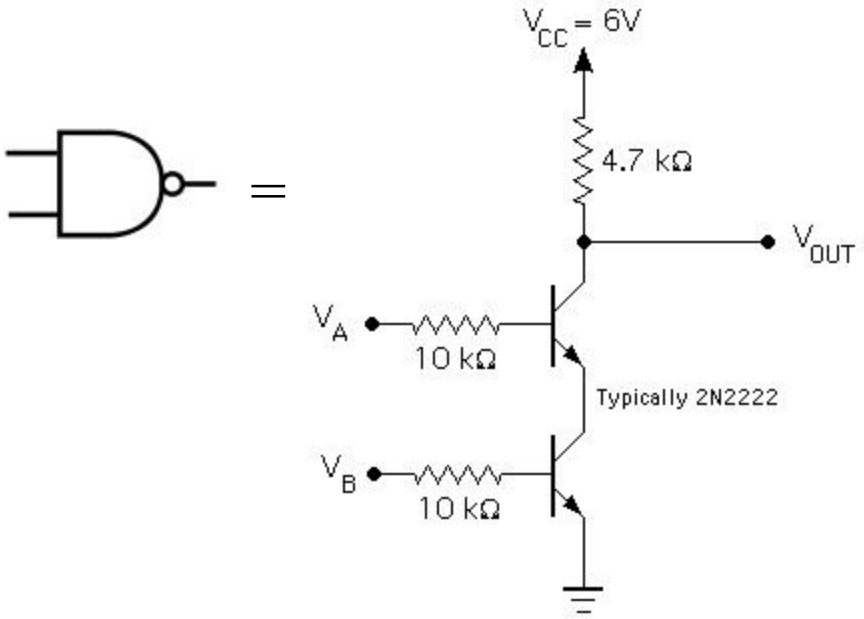
IC digital logic families

- IC digital logic families
  - RTL(Resistor-transistor logic)
  - DTL(Diode-transistor logic)
  - TTL(Transistor -transistor logic)
  - ECL(Emitter-coupled logic)
  - CMOS(Complementary Metal-oxide semiconductor)

Resistor-Transistor Logic (RTL)

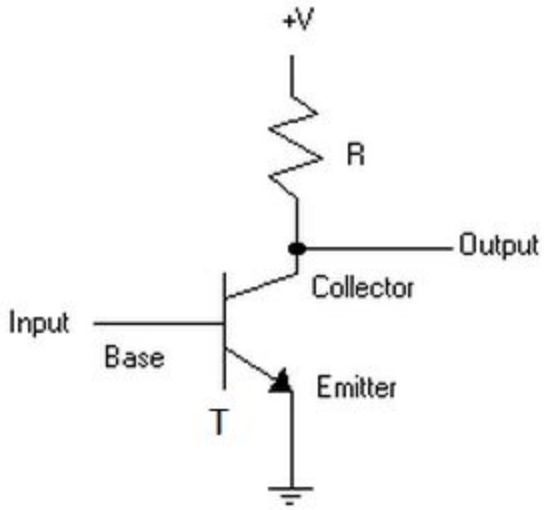
RTL NAND circuits

- Transistor as a switch
- can be cascaded
- large power draw



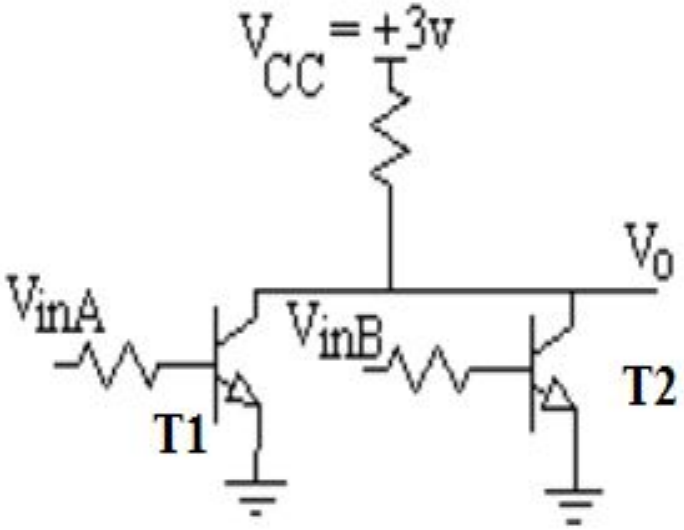
A	B	NAND o/p
0	0	1
0	1	1
1	0	1
1	1	0

RTL-NOT Gate-CE configuration



Vin	T	Vo
1	Sat (closed switch)	0
0	CUT-OFF (open switch)	1

RTL--NOR



Vina	Vinb	T1	T2	Y
0	0	CUT-OFF	CUT-OFF	1
0	1	CUT-OFF	SAT	0
1	0	SAT	CUT-OFF	0
1	1	SAT	SAT	0

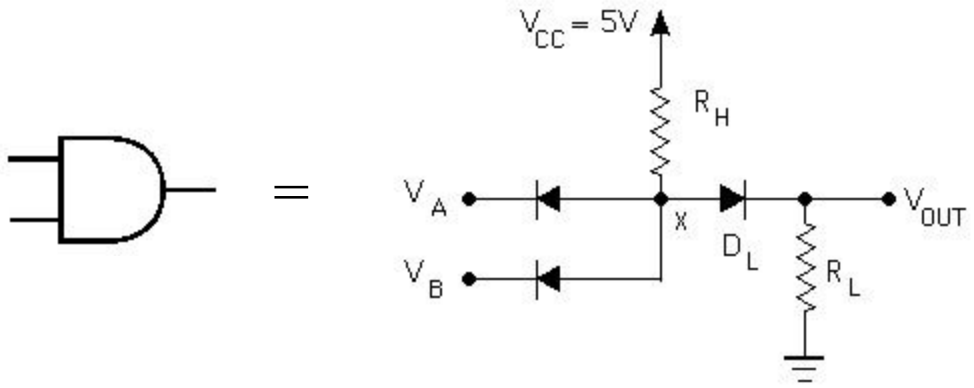
Resistor-Transistor Logic (RTL)

- O/p voltage drops about 1v when the fan-out is 5
- Power dissipation is about 12mw.
- Propagation delay averages 25ns.

Diode Logic (DL)

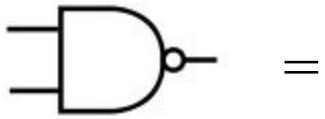
- simplest; does not scale
- NOT not possible (need an active element)

A	B	AND o/p
0	0	0
0	1	0
1	0	0
1	1	1



Diode-Transistor Logic (DTL)

- essentially diode logic with transistor amplification
- reduced power consumption
- faster than RTL



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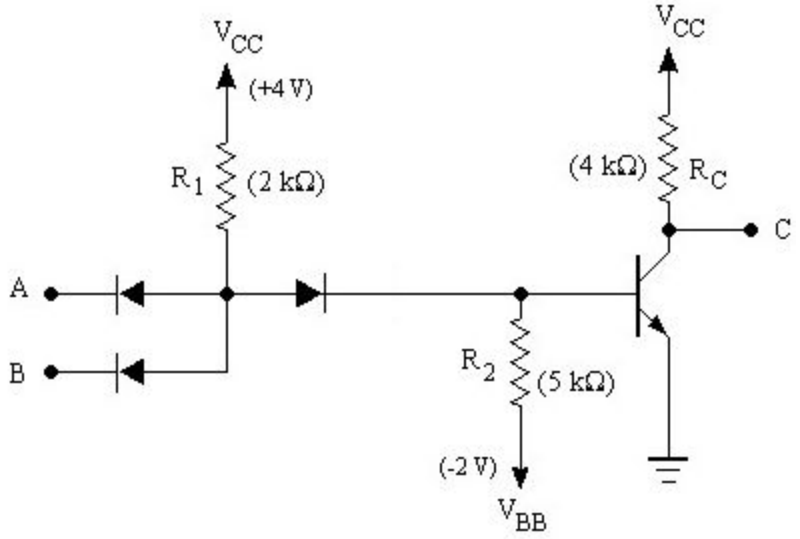
A	B	NAND o/p
0	0	1
0	1	1
1	0	1
1	1	0



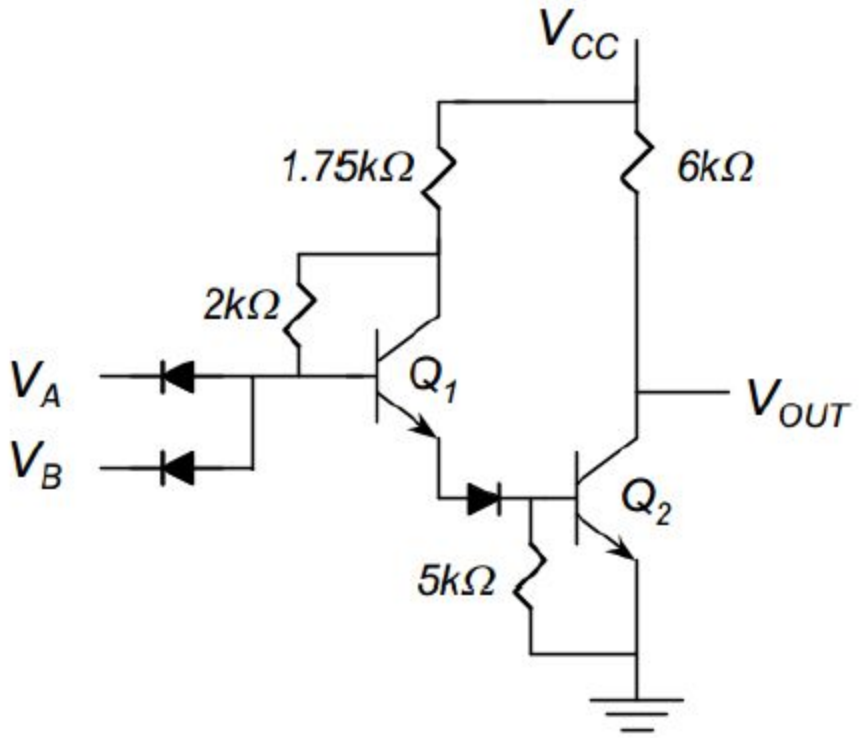
DL AND gate

inverter

DTL-NAND

- Input Diodes Da,Db,Dc conduct through resistor R, if the corresponding input is in the LOW state, while the corresponding to HIGH state the is non conducting.
- If at least one of the input is LOW, the diode connected to their input conducts and the voltage at the output is one diode drop above the low level voltage at the input. this voltage keep the transistor in cut-off. The output of transistor is Vcc.
- If all the three i/ps are in High state ,the i/p diodes are cut-off and current flowing from Vcc through R should be sufficient to drive transistor in saturation. Therefore the o/p of transistor is Vce(sat).
- Voltage corresponds to logic 1 and logic 0 as Vcc and Vce(sat).
- Delays are associated with the turning on and off of the output transistor.
- While turning on, any capacitance shunting the output of the gate discharges rapidly through the low impedance of the o/p transistor in saturation
- At turn off, the shunt capacitor must charge through the pull-up resistor Rc in addition to the storage time delay. Turn off delay is larger than turn on delay by a factor of 2 or 3.
- Propagation delay of DTL gates are 30 to 80ns.

Modified DTL-this increases fan out capability



TTL

- The original basic TTL gate was a slight improvement over the DTL gate.
- There are several TTL subfamilies or series of the TTL technology.
- first introduced by in 1964 (Texas Instruments)
- TTL has shaped digital technology in many ways
- Transistor alone performs the logical operation
- Transistors operated in saturated mode.
- Fastest of the saturated logic families
- Good speed
- Low manufacturing cost
- Wide range of circuits
- Availability in SSI & MSI
- Relatively high power consumption

TTL(Transistor-Transistor Logic)

TTL subfamilies

- Standard TTL
- High speed TTL
- Low power TTL
- Schottky TTL
- Low power Schottky TTL
- Fast TTL

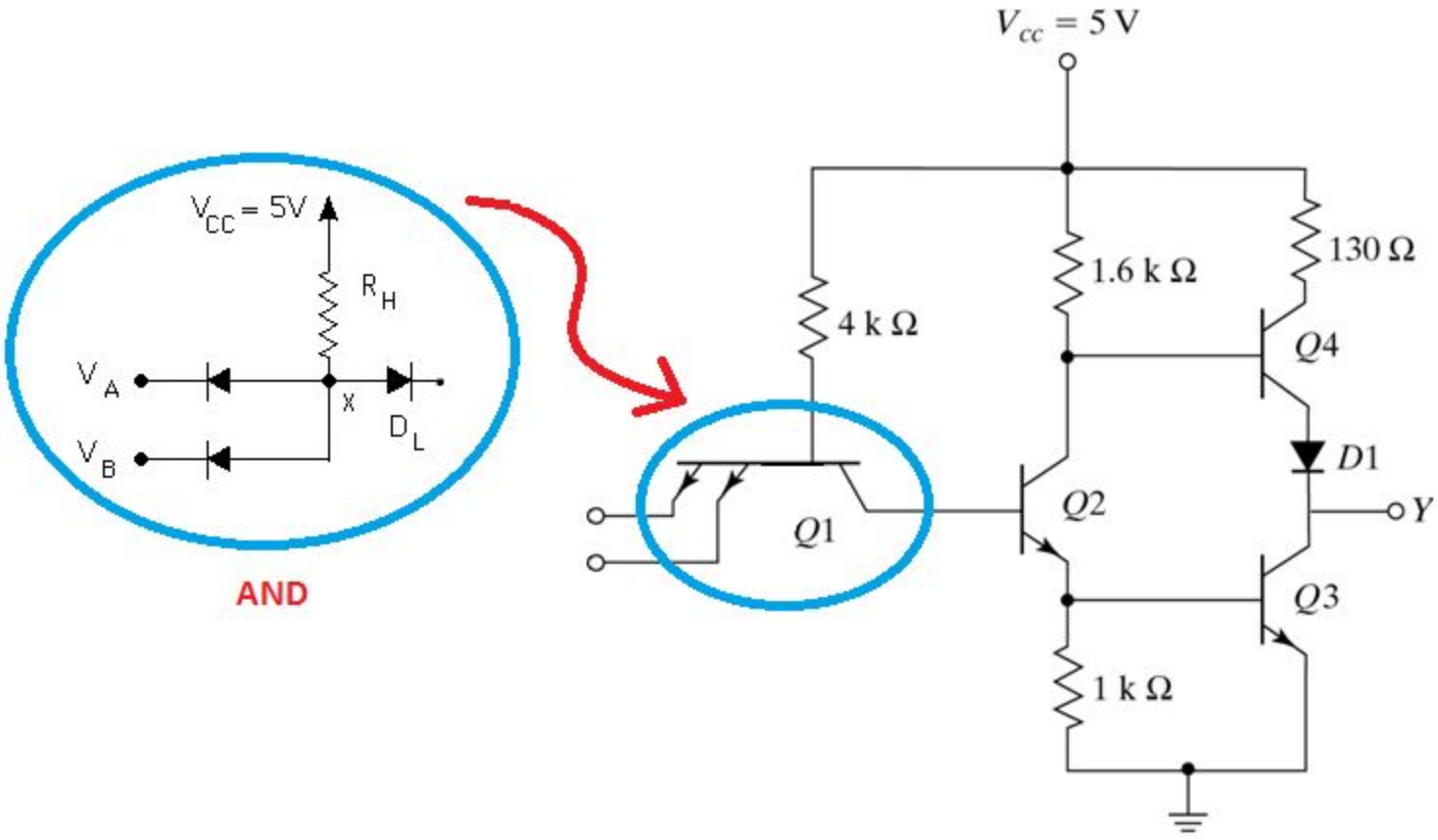
Three different types of output configurations:

1. open-collector output
2. Totem-pole output
3. Three-state (or tristate) output

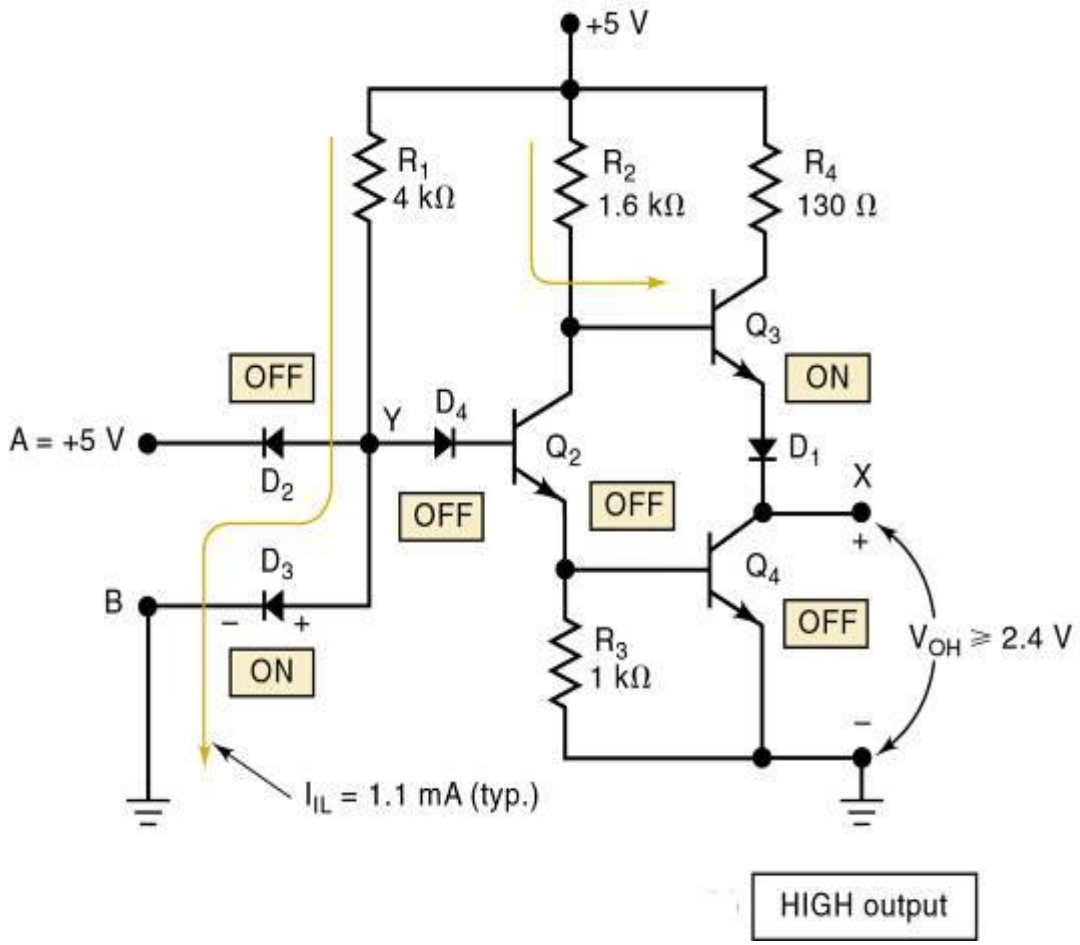
TTL(Transistor-Transistor Logic)

- The basic gate was constructed with different resistor value to produce gate with lower dissipation or higher speed.
- The propagation delay of a saturated logic family depends largely on storage time and RC time constants.
- Reduce the storage time decrease the propagation delay.
- Reduce the resistor values in the circuit, decreases the time constant (RC) and decreases the propagation delay. But power dissipation is high due to lower resistance draw more current from the supply.
- Speed of the gate is inversely proportional to propagation delay.
- In low power TTL the resistor values are higher than standard TTL gate to reduce power dissipation, but increase propagation delay.
- In high speed TTL resistor values are lowered to reduce the propagation delay but the power dissipation is increased.

TTL Gate with Totem-Pole Output



TTL Gate with Totem-Pole Output



Input conditions	Output conditions
A or B or both are LOW ($\leq$ 0.8 V)	Q_4 OFF
Current flows back to ground through LOW input terminal. I_{IL} = 1.1 mA	Q_3 acts as emitter-follower and $V_{OH} \geq$ 2.4 V, typically 3.6 V

TTL Gate with Totem-Pole Output

- o/p impedance of the gate normally resistive &capacitive loads.
- Capacitive load consist of capacitance of o/p transistor, capacitance of fan-out gates and any stray wiring capacitances.
- When o/p changes from low to high, the o/p transistor of the gate goes from saturation to cut-off and the total load capacitance 'C' charges from low to high with time constant RC.
- For open collector gate Rl=4kohm, c=15pf ,tpd=35ns. With active pull-up is replaced by passive pull-up circuit tpd is reduced to 10ns. This is called totem pole output.
- When o/p Y=low, Q2&Q3 are in saturation. VcQ2=Vbe(Q3)+Vce(Q2)=0.7+0.2=0.9v, Vce(Q3)=0.2V
- Q4 is cut-off bcos base of Q4 require 2*0..6=1.2V.

TTL Gate with Totem-Pole Output

- When o/p Y=high, one of the i/p drops to low ,Q2&Q3 are in cut-off. o/p remains low bcos the voltage across the load capacitance cannot change instantaneously. As soon as Q2 turns off Q4 conducts bcos base is connected to Vcc through 1.6Kohm.
- The current needed to charge the load ' C' causes Q4 to saturate, o/p voltage rises with time constant RC.
- R=130ohm+Rsat(Q4)+Rd~=150ohm less compare to passive pull up resistor, so transition from low to high is faster.
- When C charges ,o/p voltage rises and current in Q4 decreases so Q4 comes to active region. Final o/p=5v-Vbedrop in Q4-D1 drop=3.6v Q3 goes cut-off very fast. But initial transition Both Q3 &Q4 are on ,peak ct' is drawn from the supply. This ct' spikes generates noise.
- Change of state is frequent current spikes increases and PD also increases.
- Wired connection is not allowed.

Open-collector TTL Gate

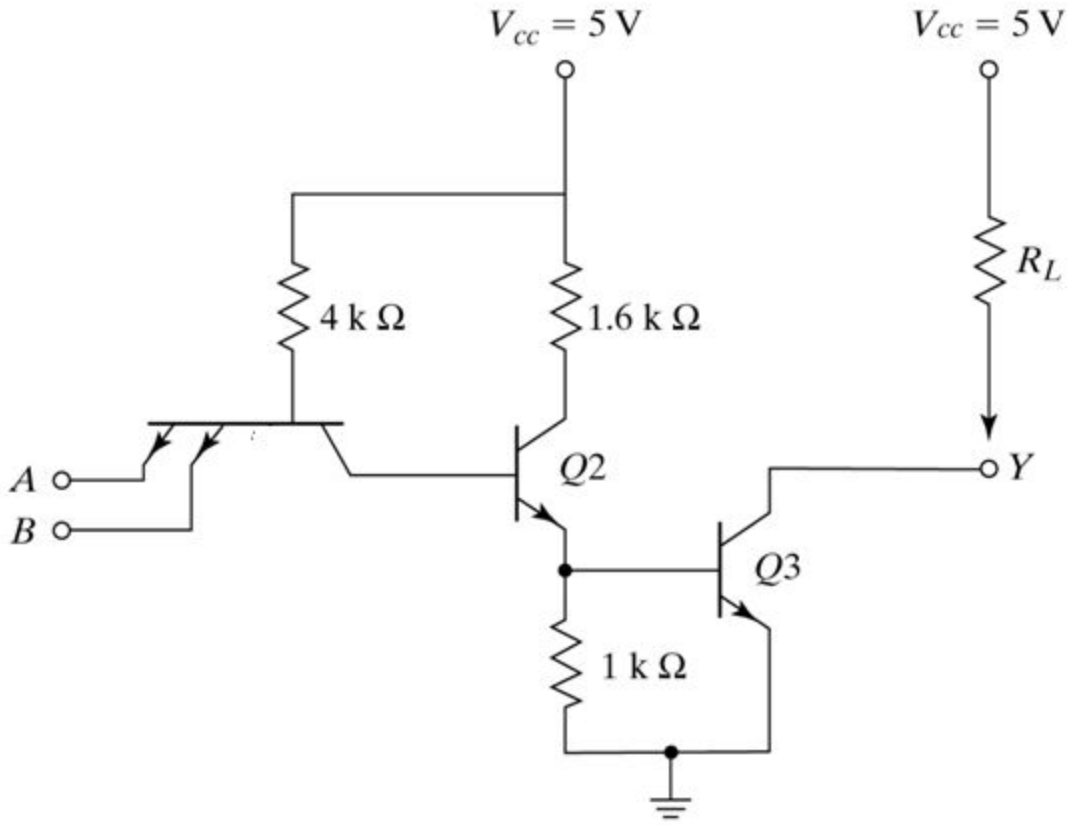
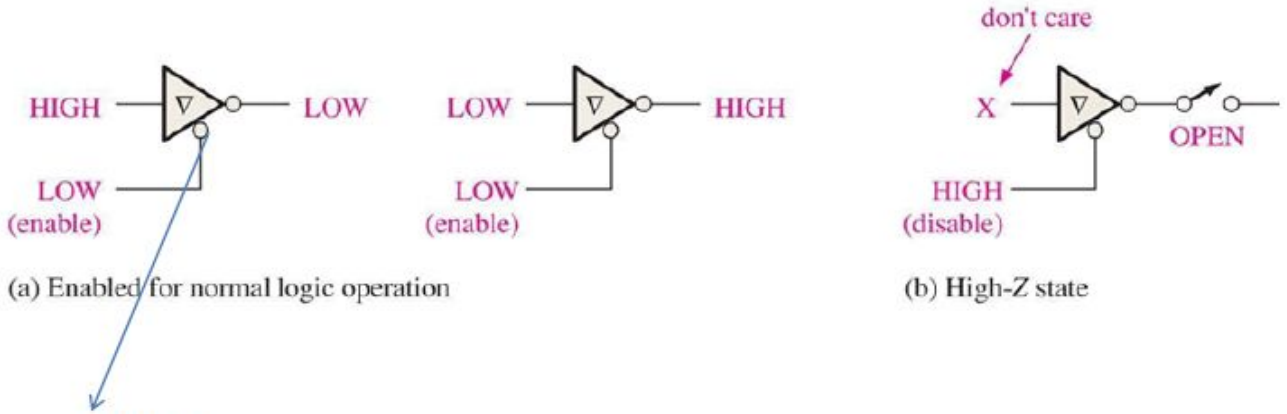


Fig. 10-11 Open-Collector TTL Gate

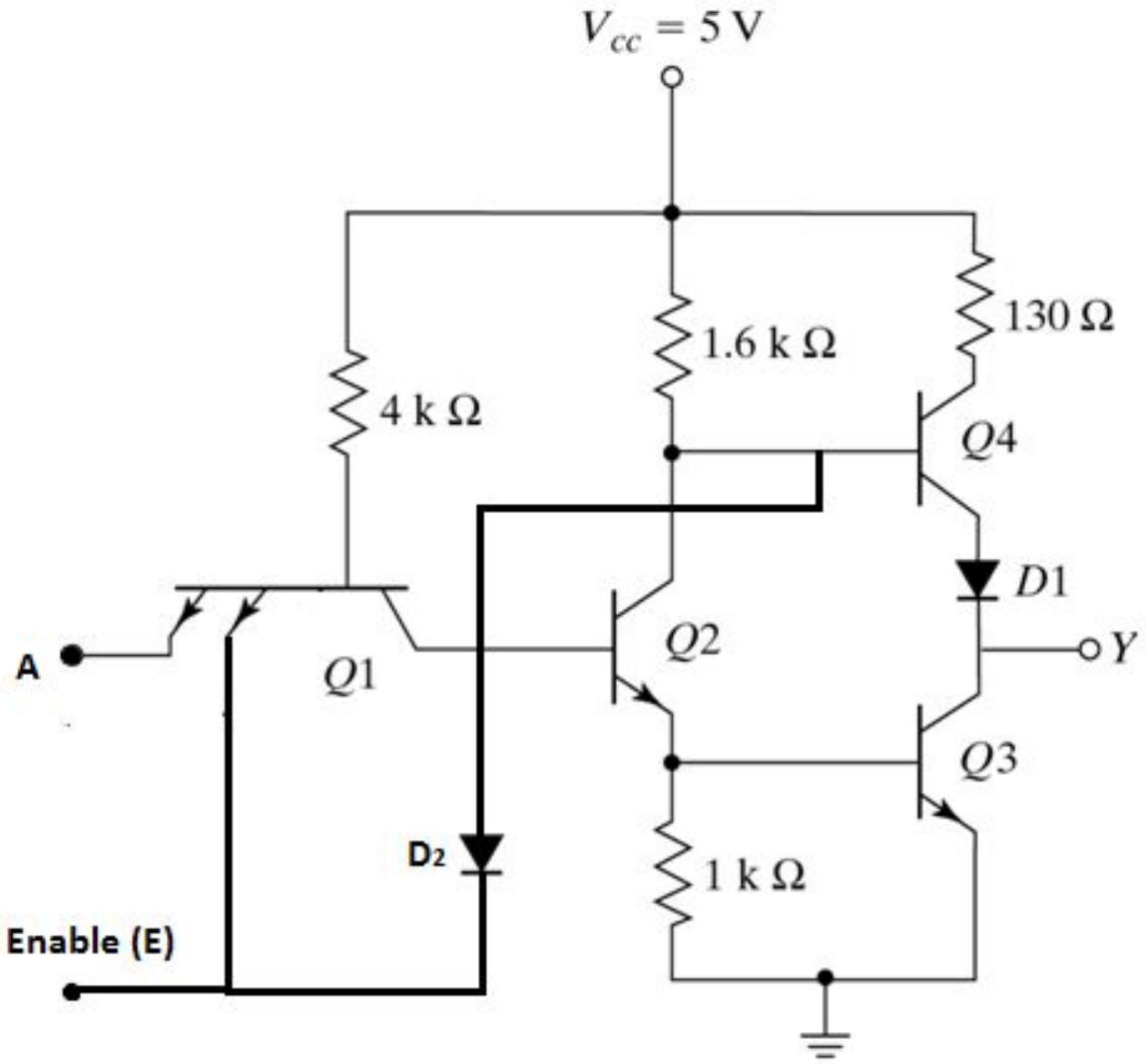
Open-collector TTL Gate

- Multiple emitter of Q1 connected to i/ps. Compare to DTL ,i/p diodes--Q1, D1--B-C jn, D2—Q2.
- o/p is taken from open collector of Q3.
- Pull up resistor connected to Vcc, to pull up the o/p to high level when Q3 is off. Otherwise the o/p acts as an open circuit.
- 0.2v for low level,2.4 to 5v for high level.
- If any i/p is low , corresponding B-E jn of Q1 is F.B. the voltage at base of Q1 is 0.9v(i/p 0.2+Vbe drop 0.7).
- In order for Q3 to start conducting the path from Q1-Q3 must overcome the potential 1.8v (Diode drop in B-C jn drop+ two Vbe drop of Q2,Q3). But at Q1 is 0.9v so Q3 is cut-off , o/p is high.
- If all i/ps are high Q2, Q3 conduct and saturate. B-E jns of Q1 are all R.B. when Q3 saturates o/p goes low to 0.2v.
- Applications are driving a lamp or relay, performing wired logic and construction of common bus system

The three states of a tristate circuit.



Three-state TTL with Inverter operation



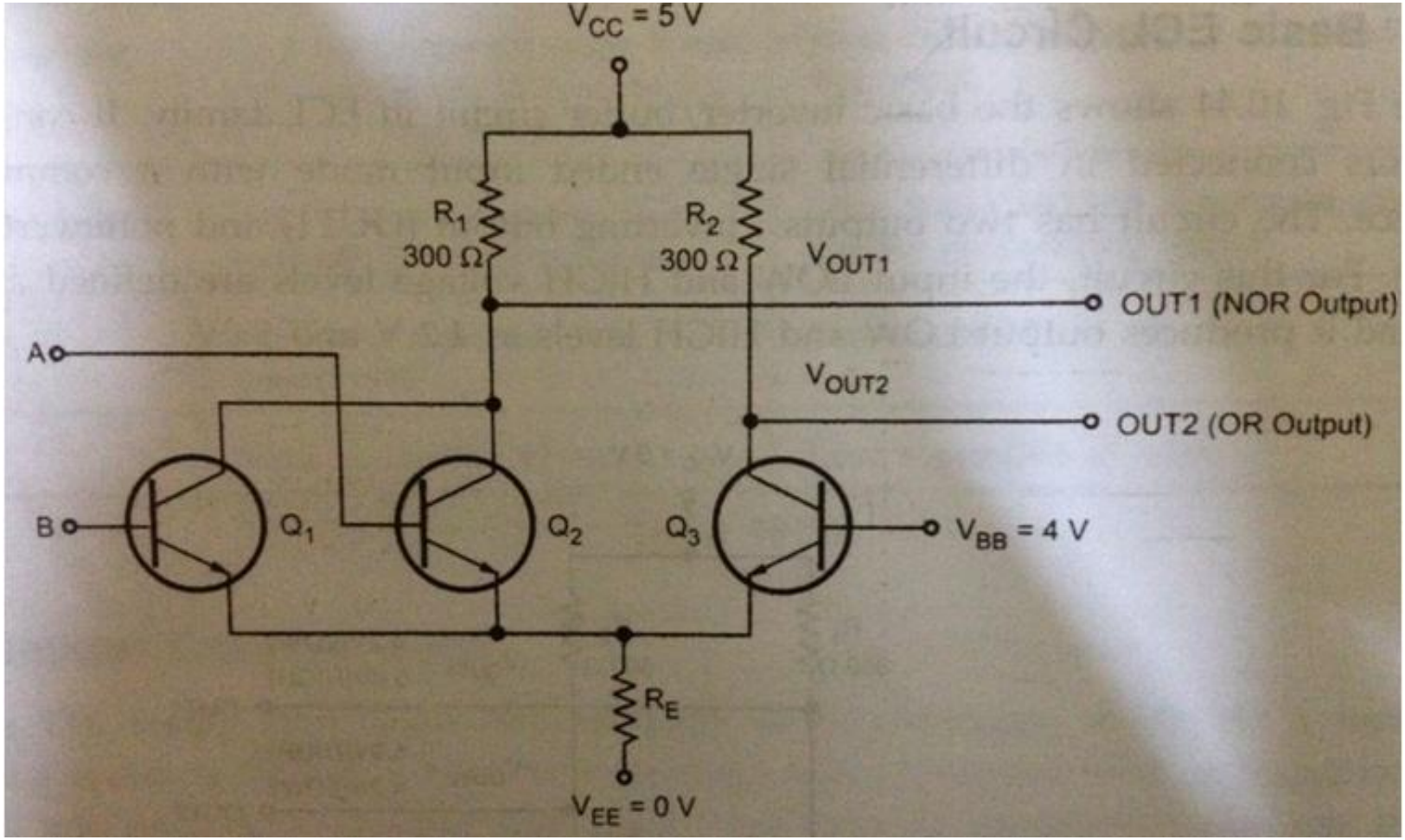
Emitter-Coupled Logic (ECL)

- Non saturated digital logic family & Used in **high speed circuits**
- **Propagation rate as low as 1-2ns**
- **Noise immunity and power dissipation is high compare of all logic families.**
- Including
  - Differential input amplifier
  - Internal temperature and voltage compensated bias network
  - Emitter-follower outputs

ECL NOR / OR

- The circuit has 2 outputs- inverting and non inverting output, input low is 3.6 V, input high is 4.4V.
- When A=B=0, so Q1, Q2 are OFF, then Out1=High and Out2=Low.
- When A=B=1, so Q1, Q2 are ON, then Out1= low and Out2=High.

ECL (NOR/OR GATE)



Classes of Field Effect Transistors

- **Metal-Oxide-Semiconductor Field Effect Transistor**
  - Which will be the type that we will study in this course.
- Metal-Semiconductor Field Effect Transistor
  - MESFET
- Junction Field Effect Transistor
  - JFET
- High Electron Mobility Transistor or Modulation Doped Field Effect Transistor
  - HEMT or MODFET
- Fast Reverse/Fast Recovery Epitaxial Diode
  - FREDFET
- DNA Field Effect Transistor
  - The conduction path is through a strand of DNA

Types of MOSFETS

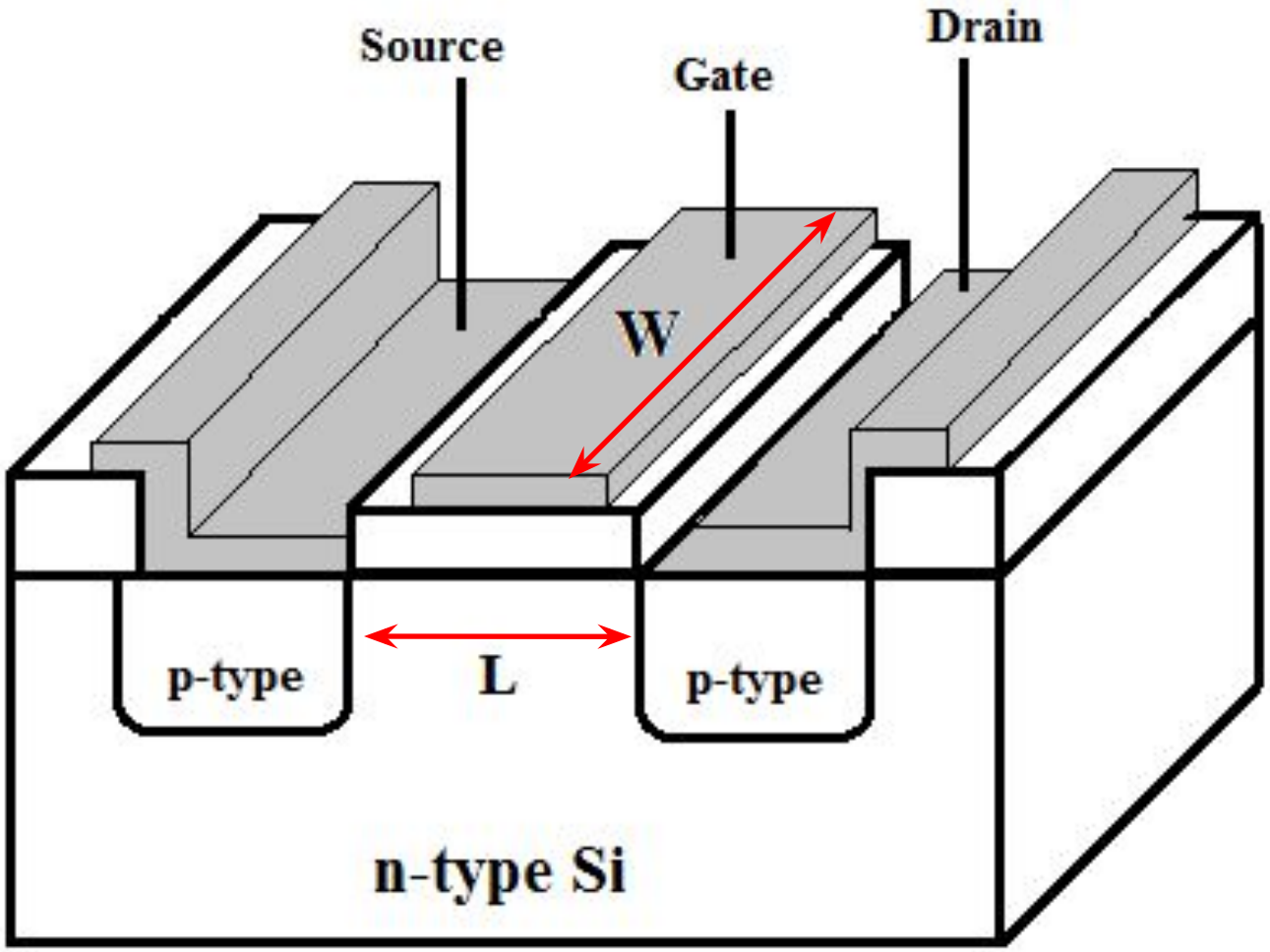
MOSFET: N-Channel
Enhancement Type

MOSFET: P-Channel
Enhancement Type

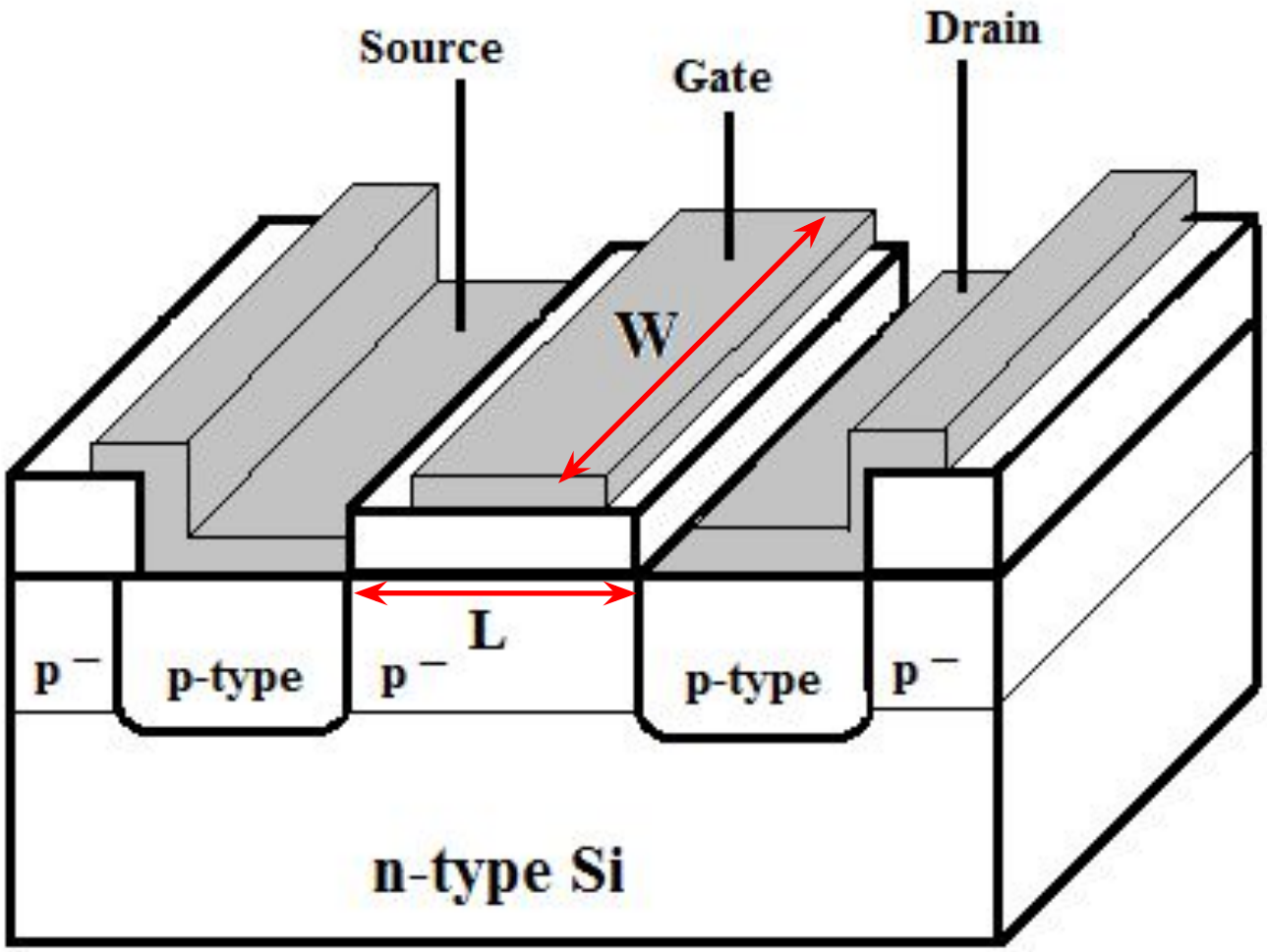
MOSFET: N-Channel
Depletion Type

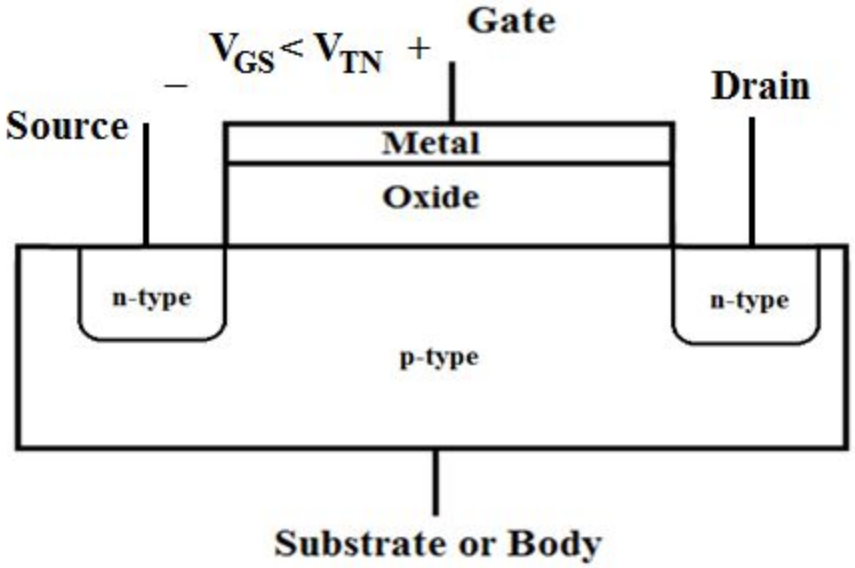
MOSFET: P-Channel
Depletion Type

P-channel
Enhancement Mode Transistor

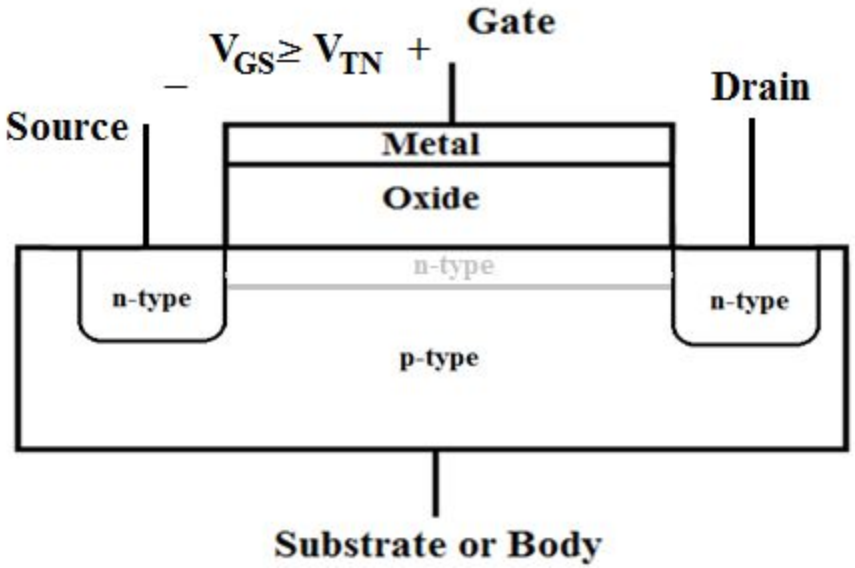


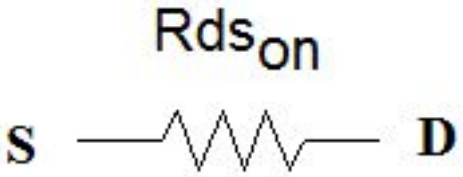
P-channel
Depletion Mode Transistor





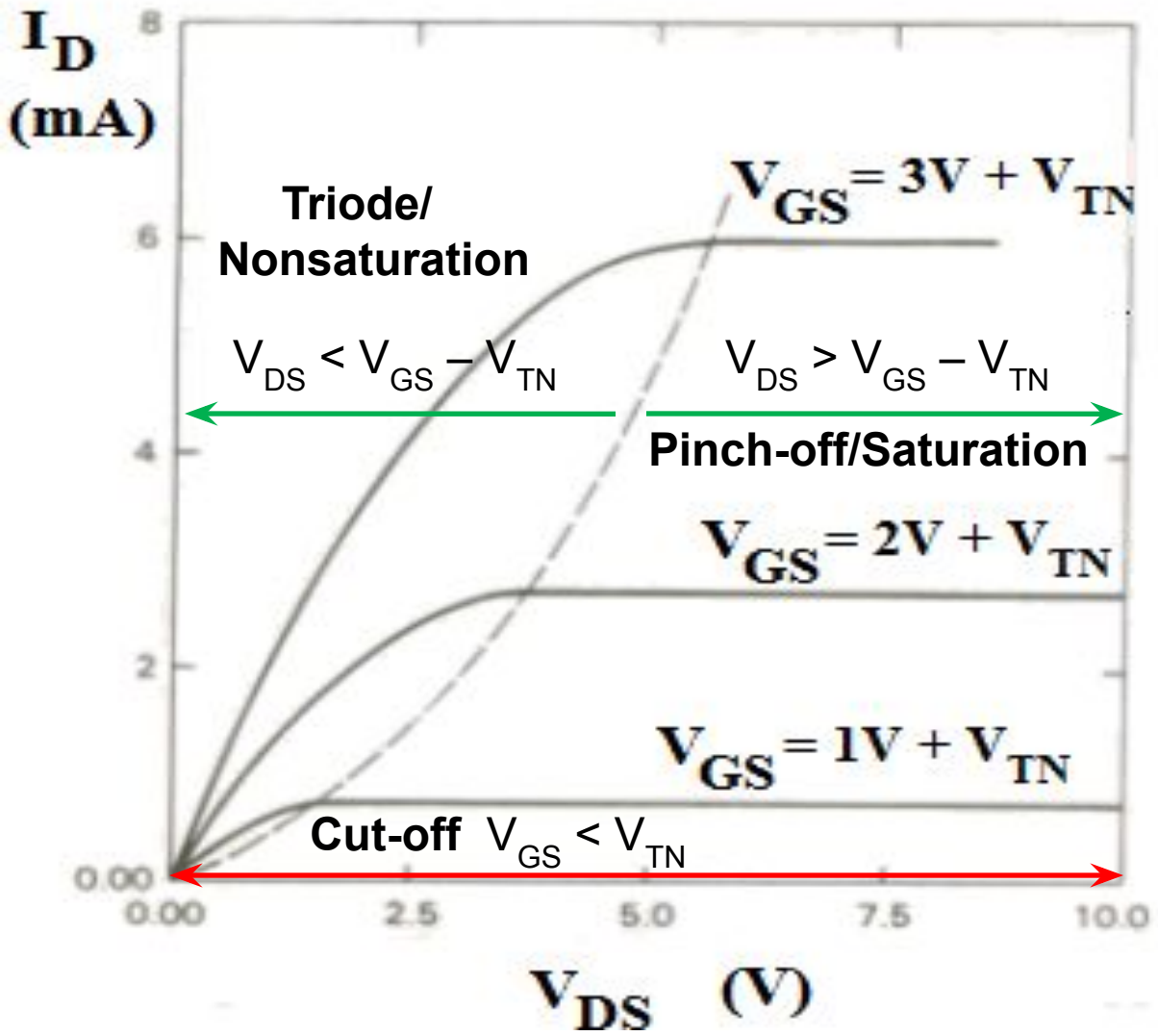
Before electron inversion layer is formed



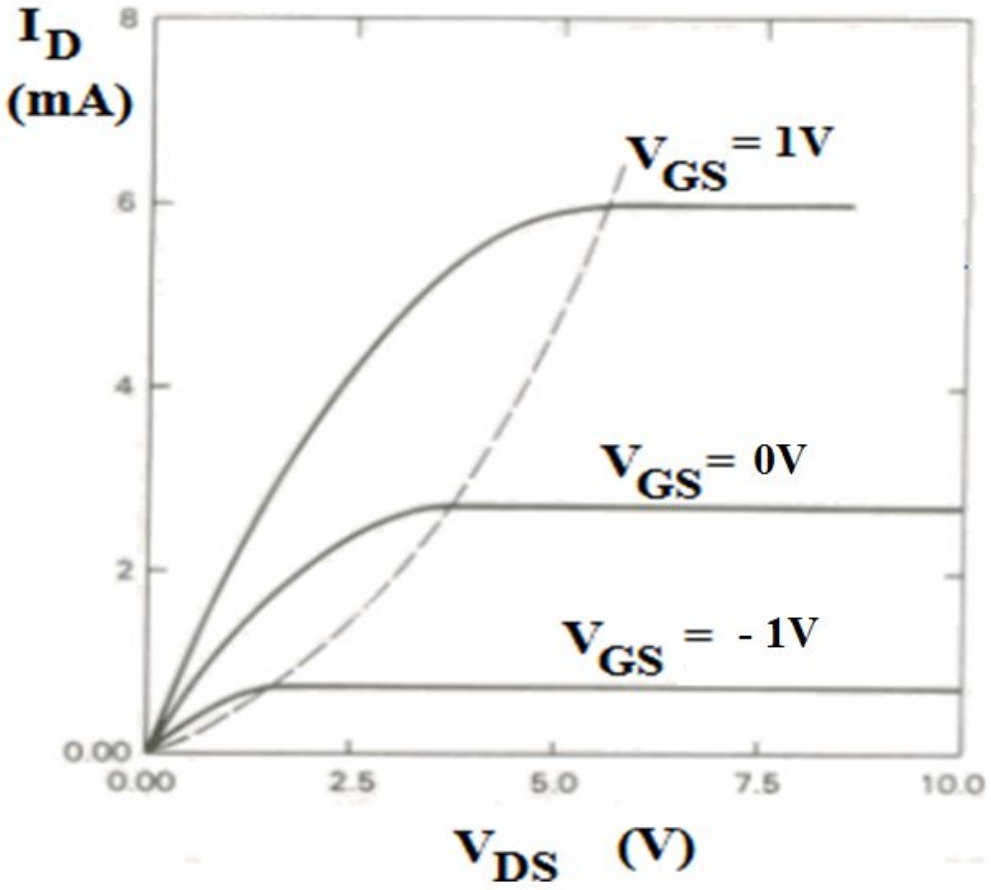


After electron inversion layer is formed

I_D Versus V_{DS} Curves
Enhancement-Mode nMOSFET



i_D Versus v_{DS} Curves
Depletion-Mode nMOSFET



Assuming that $V_{TN} < -1V$

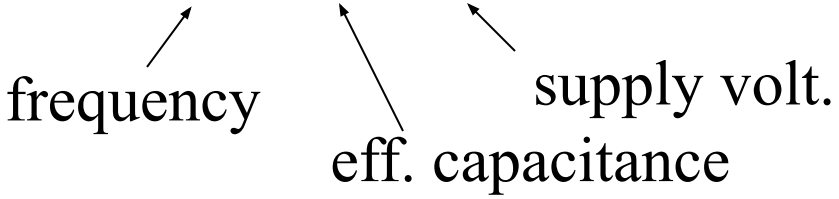
CMOS

Complimentary MOS (CMOS)

- Other variants: NMOS, PMOS (obsolete)
- Very low static power consumption
- Scaling capabilities (large integration all MOS)
- Full swing: rail-to-rail output
- Things to watch out for:
  - don't leave inputs floating (in TTL these will float to HI, in CMOS you get undefined behaviour)
  - susceptible to electrostatic damage (finger of death)
- Open LTspice example: CMOS NOT and NAND…

CMOS power requirements

- TTL power essentially constant (no frequency dependence)
- CMOS power scales as $\propto f \times C \times V^2$

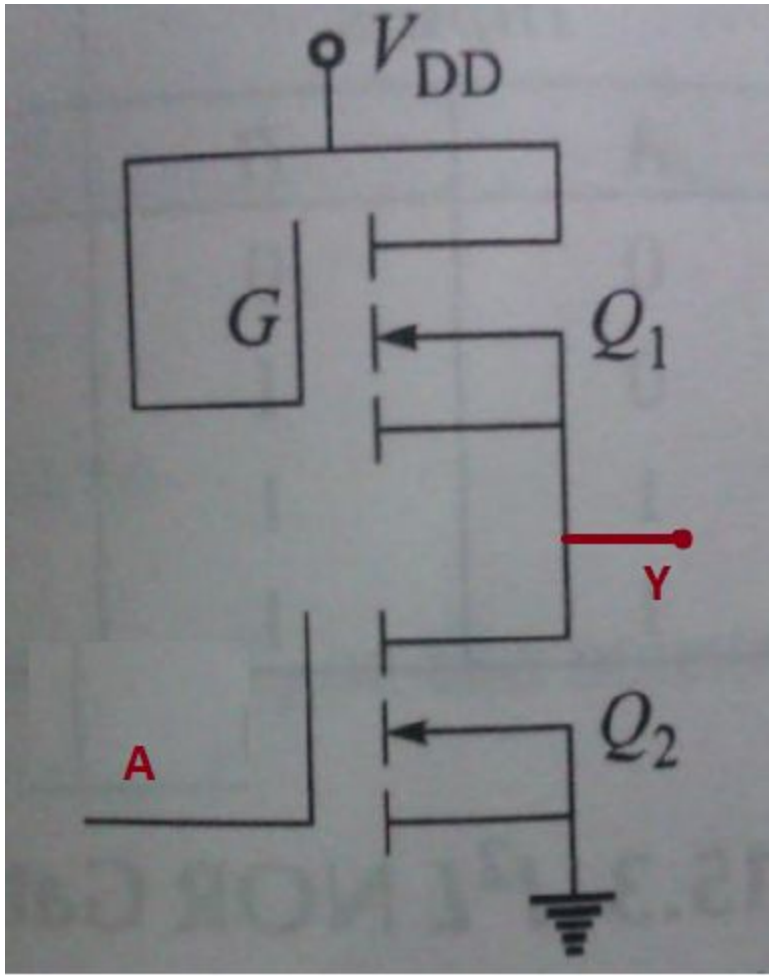


- At high frequencies (>> MHz) CMOS dissipates more power than TTL
- Overall advantage is still for CMOS even for very fast chips – only a relatively small portion of complicated circuitry operates at highest frequencies

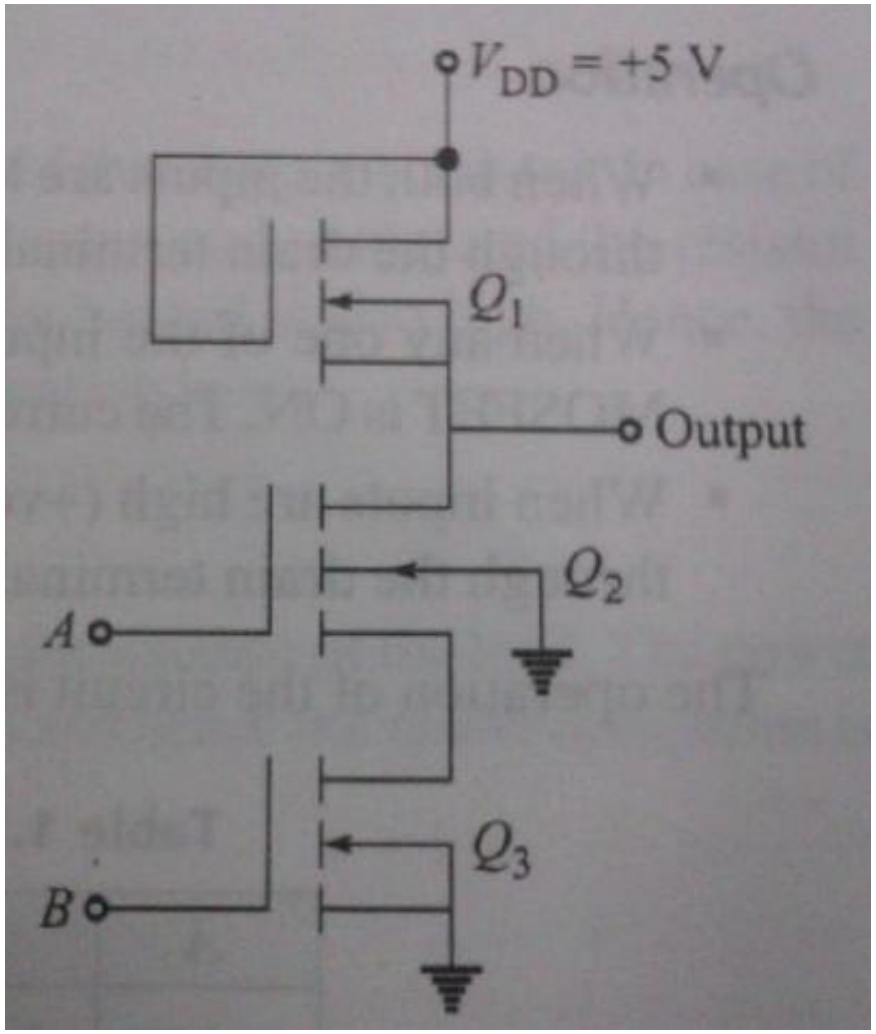
MOSFET Logic

- Low power dissipation and high density of fabrication.
- PMOS
- NMOS
  - INVERTER, NAND, NOR
- CMOS
  - INVERTER, NAND, NOR

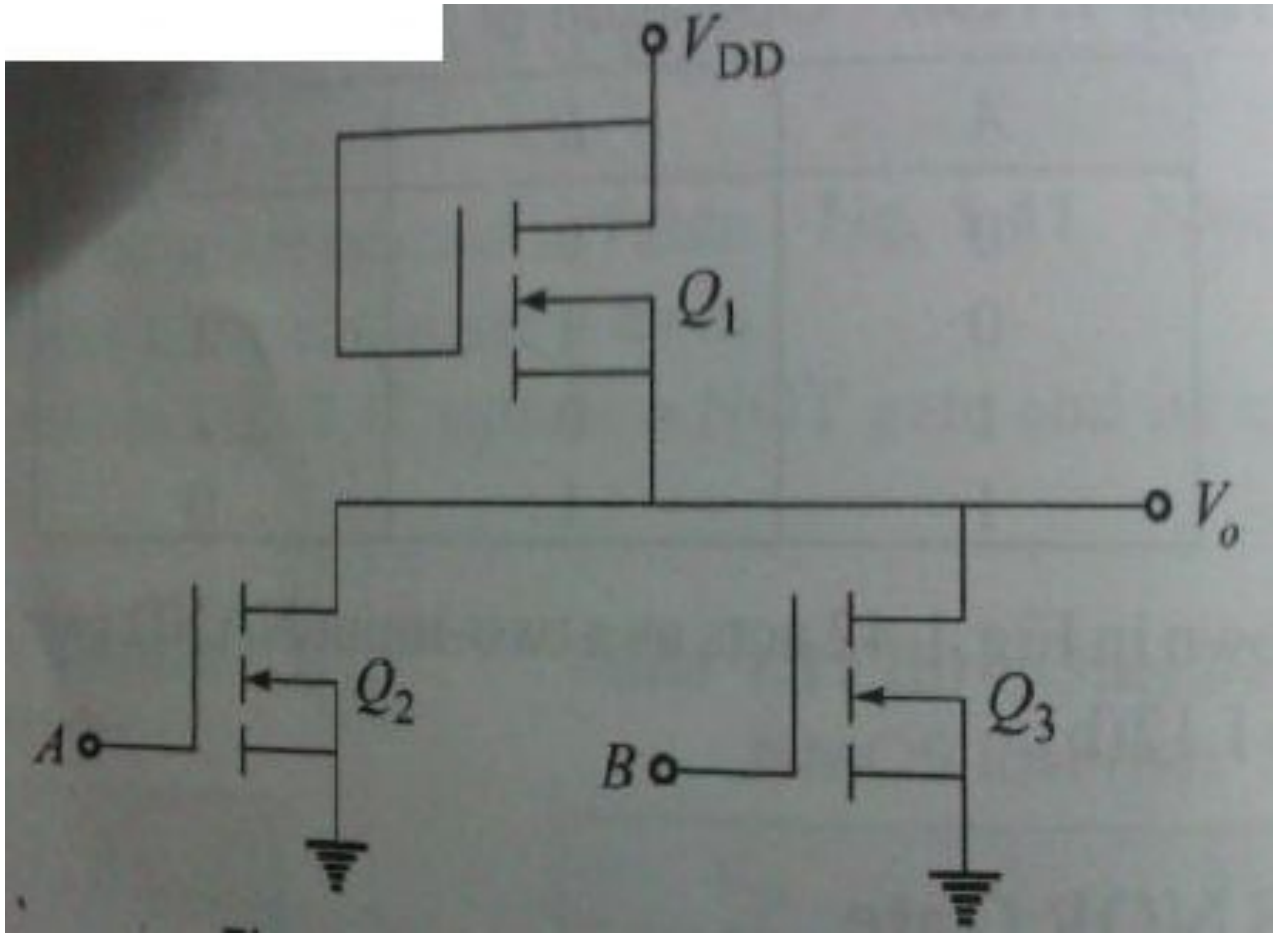
NMOS INVERTER (NOT)



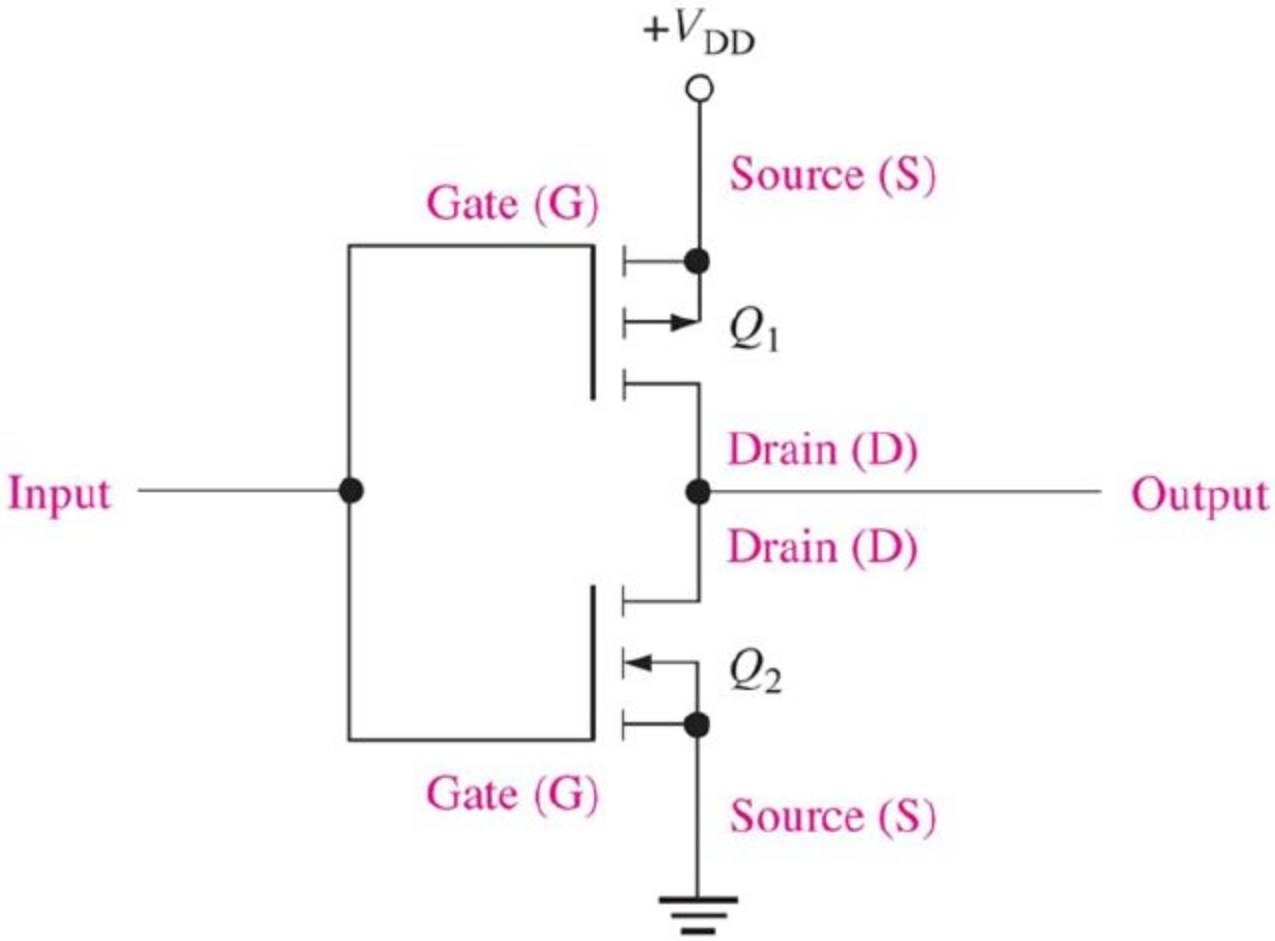
NMOS NAND



NMOS NOR

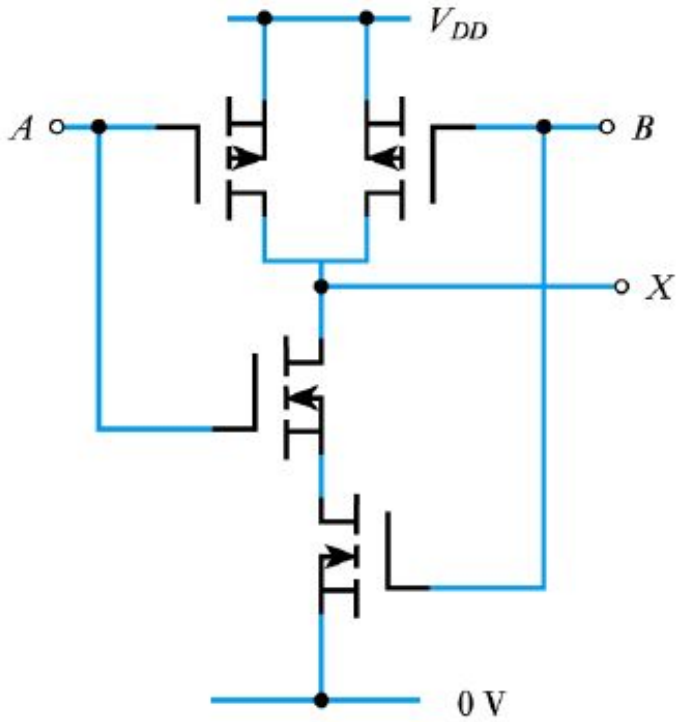


A CMOS inverter circuit.

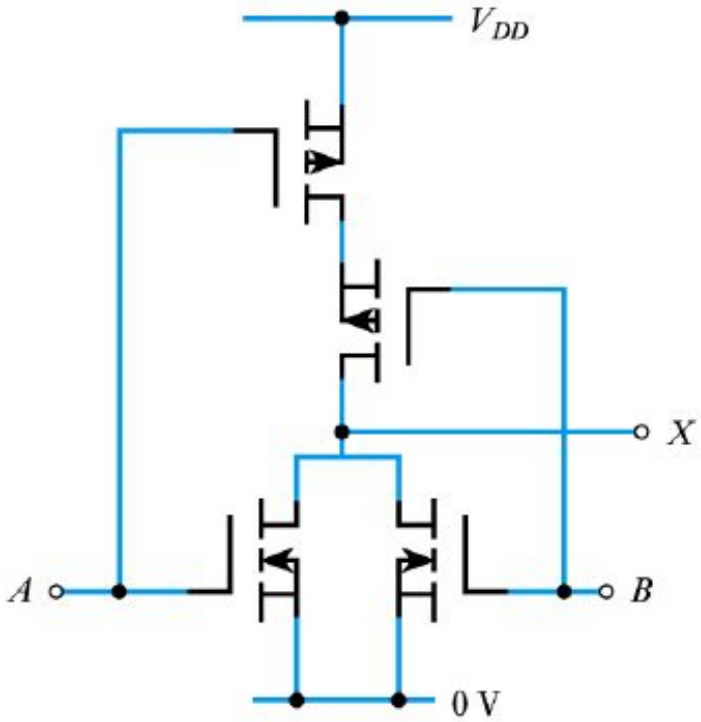


CMOS

- **CMOS gates**



(a) NAND gate

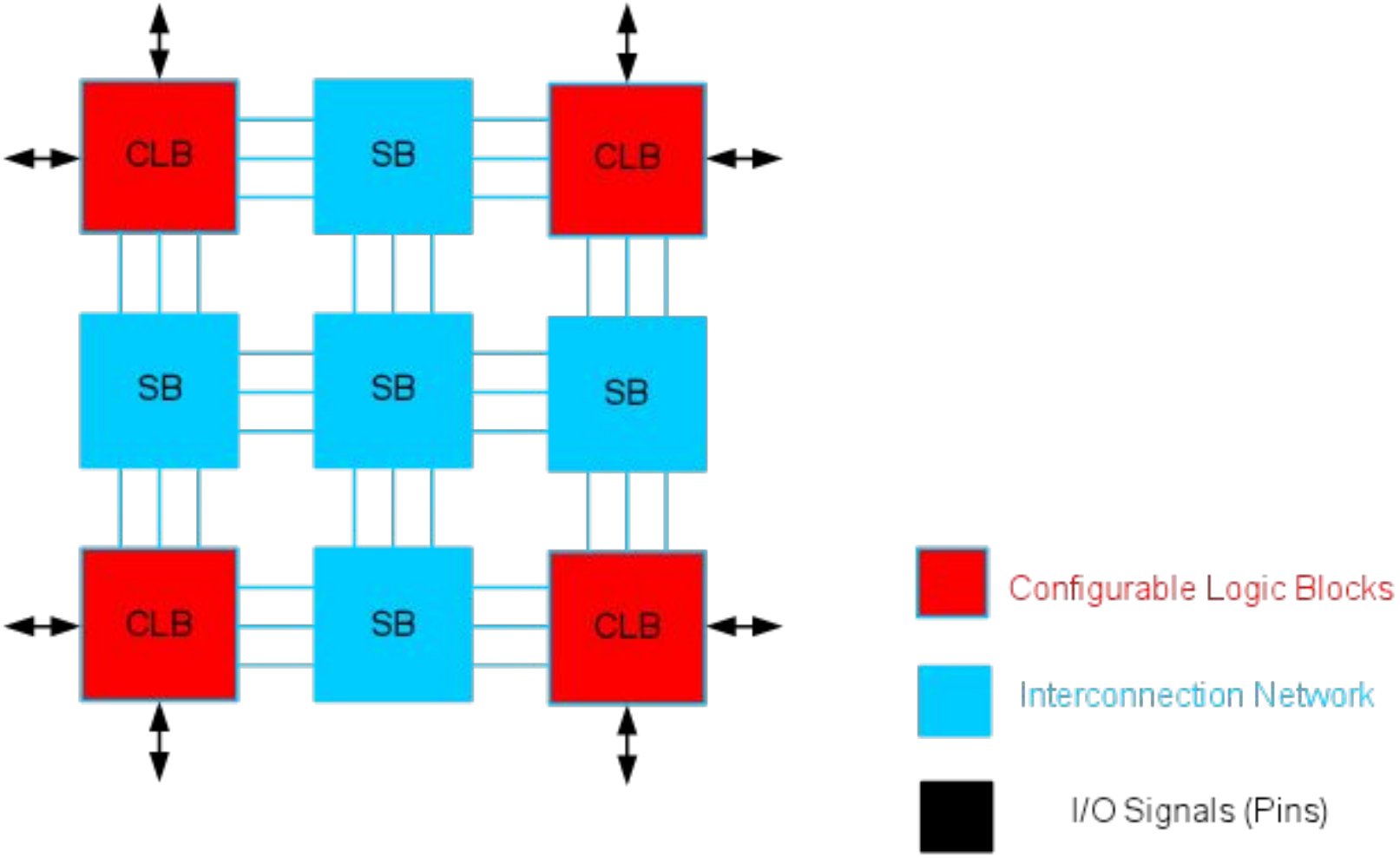


(b) NOR gate

FPGA

- A Field-Programmable Gate Array (FPGA) is an integrated circuit that can be configured by the user to emulate any digital circuit as long as there are enough resources.
- The FPGA configuration is generally specified using a hardware description language (HDL)
- An FPGA can be seen as an array of Configurable Logic Blocks (CLBs) connected through programmable interconnect (Switch Boxes).

FPGA structure



Simplified CLB Structure