31. a. Explain the following mapping technique used for cache mapping.
    (i) Direct mapping cache
    (ii) Associative mapping cache
    (iii) Block set associative mapping cache

(OR)

b. What is virtual memory? With the help of neat sketch explain the method of virtual to physical address translation.

32. a. Describe the data transfer method using DMA.

(OR)

b. What is the importance of I/O interface? Compare the features of SCSI and PCI interfaces.

* * * * *

Reg. No.														

B.Tech. DEGREE EXAMINATION, NOVEMBER 2018
3rd to 7th Semester

15CS203 – COMPUTER SYSTEM ARCHITECTURE
(For the candidates admitted during the academic year 2015-2016 to 2017-2018)

Note:
(i) **Part - A** should be answered in OMR sheet within first 45 minutes and OMR sheet should be handed over to hall invigilator at the end of 45th minute.
(ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: Three Hours Max. Marks: 100

PART – A (20 × 1 = 20 Marks)
Answer **ALL** Questions

1. During the execution of a program, which gets initialized first?
   (A) MDR (B) IR
   (C) PC (D) MAR

2. The control unit controls other units by generating
   (A) Control signals (B) Timing signals
   (C) Transfer signals (D) Command signals

3. In multiple bus organization, the registers are collectively placed and referred as _____.
   (A) Set registers (B) Register file
   (C) Register block (D) Map registers

4. In the following indexed addressing mode instruction, MOV $5(R_1)$, LOC the effective address is _____.
   (A) $EA = 5 + R_1$ (B) $EA = R_1$
   (C) $EA = [R_1]$ (D) $EA = 5 + [R_1]$

5. For the addition of large integers, most of the systems make use of _____.
   (A) Fast adders (B) Full adders
   (C) Carry-look ahead adders (D) Parallel adders

6. We make use of _____ circuits to implement multiplication.
   (A) Flip flops (B) Combinational
   (C) Fast adder (D) Serial adder

7. The multiplier −6(11010) is recorded as
   (A) 0 −1 −2 (B) 0 −1 +1 −10
   (C) −2 −10 (D) −2 −2

8. How many main approaches are available to algorithm for division?
   (A) 2 (B) 3
   (C) 4 (D) 5

9. When arithmetic logic and control unit of a computer are combined into a single unit, it is known as
   (A) Central processing unit (B) Memory unit
   (C) I/O unit (D) Operating unit

10. The pipelining process is also called as
   (A) Super scalar operation (B) Assembly line operation
   (C) Von Neumann cycle (D) Field lining

11. Processor without structural hazard is
   (A) Faster (B) Slower
   (C) Have longer clock cycle (D) Have larger clock rate

12. The disadvantages of the hardwired approach is that
   (A) It is less flexible (B) It cannot be used for complex instructions
   (C) It is costly (D) Less flexible and cannot be used for complex instructions

13. How many address lines are needed to address each memory location in a 2048× 4 memory chip?
   (A) 8 (B) 10
   (C) 11 (D) 12

14. A hard disk with 20 surfaces will have _____ heads.
   (A) 10 (B) 5
   (C) 1 (D) 20

15. The contents of the EPROM are erased by
   (A) Overcharging the chip (B) Exposing the chip to UV rays
   (C) Exposing the chip to IR rays (D) Discharging the chip

16. MFC is used to
   (A) Issue a read signal (B) Signal to the device that the memory read operation is complete
   (C) Signal the processor that the memory operation is complete (D) Assign a device to perform the read operations

17. To overcome the lag in the operating speeds of the I/O device and the processor we use
   (A) Buffer spaces (B) Status flags
   (C) Interrupt signals (D) Exceptions

18. Once the bus is granted to a device it _____.
   (A) Activates the bus busy line (B) Performs the required operation
   (C) Raises an interrupt (D) Bus ready line is activated

19. The device connected to USB is assigned an _____ address.
   (A) 9 bit (B) 16 bit
   (C) 4 bit (D) 7 bit

20. PCI stands for
   (A) Peripheral component interconnect (B) Peripheral computer internet
   (C) Processor computer interconnect (D) Processor cable interconnect

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

21. Define the term
   (i) Computer architecture
   (ii) Multiprocessing

22. Write down the steps for restoring division and non-restoring division.

23. What is known as multiphase clocking? Mention the drawback of assigning one bit position to each control signal.

24. Calculate the maximum size of the memory that can be used in a 16-bit computer and 32 bit computer.

25. Differentiate between static RAM and dynamic RAM.

26. State the differences between memory mapped I/O and I/O mapped I/O.

27. Why is program controlled I/O unsuitable for high speed data transfer?

PART – C (5 × 12 = 60 Marks)
Answer **ALL** Questions

28. a.i. Mention the factors influencing performance of a system. (4 Marks)

ii. Assume a two address format specified as source, destination. Examine the following sequence of instructions and explain the addressing modes used and operation done in every instruction
- Move $(R_5)+,R_0$
- Move $16(R_5), R_3$
- Add # 40, R_5
- MVI # 5, R_1 (8 Marks)

(OR)

b. Illustrate one, two, three and zero address instruction formats with example.

29. a. Show the step by step multiplication process using Booth algorithm when the following binary numbers are multiplied $(-15)*(-13)$. Assume 5 bit registers that hold signed numbers.

(OR)

b. Add the numbers 0.510 and −0.4375 using binary floating point addition algorithm.

30. a. List and explain the steps involved in the execution of complete instruction.

(OR)

b. What is data hazard? How do you overcome it? Discuss its side effects.