Course Code	18CSS201J	Course Name	ANALOG AND DIGITAL ELECTRONICS	Course Category	S	*Engineering Sciences*	L	T	P	C
							3	0	2	4

Pre-requisite Courses	18EES101J	Co-requisite Courses	*Nil*	Progressive Courses	*Nil*
Course Offering Department	*Computer Science and Engineering*	**Data Book / Codes/Standards**	*Nil*		

Course Learning Rationale (CLR): *The purpose of learning this course is to:*

		Learning			Program Learning Outcomes (PLO)														
		1	*2*	*3*	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CLR-1 :	*Identify the applications of analog electronics*	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
CLR-2 :	*Identify the applications of digital logic families*																		
CLR-3 :	*Design the combinational and sequential logic circuits*																		
CLR-4 :	*Implement the combinational and sequential logic circuits*																		
CLR-5 :	*Analyze the design of counters and registers*																		
CLR-6 :	*Utilize the concepts in real time scenarios*																		
Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*																		
CLO-1 :	*Identify the analog and digital components in circuit design*	*1*	*80*	*70*	*H*	*H*	-	-	-	-	-	-	-	-	-	-	-	-	-
CLO-2 :	*Analyze the combinational and sequential logic circuits*	*2*	*85*	*75*	*H*	*H*	-	-	-	-	-	-	-	-	-	-	-	-	-
CLO-3 :	*Apply gates and flip-flops in circuit design*	*2*	*75*	*70*	*H*	-	*H*	*H*	-	-	-	-	-	-	-	-	-	-	-
CLO-4 :	*Use simulation package and realize*	*2*	*85*	*80*	*H*	*H*	*H*	*H*	*H*	-	-	-	-	-	-	*H*	-	-	-
CLO-5 :	*Apply HDL code and synthesize*	*2*	*85*	*75*	*H*	-	*H*	*H*	*H*	-	-	-	-	-	-	-	-	-	-
CLO-6 :	*Build the circuits in bread board and demonstrate and FGPA*	*3*	*80*	*70*	-	-	*H*	*H*	-	*H*	-	-	*H*	-	*H*	-	-	-	-

		Introduction to Analog electronics	Logic Families	Combinational Logic Circuits	Sequential Logic circuits	Registers & Counters
Duration (hour)		**15**	**15**	**15**	**15**	**15**
S-1	**SLO-1**	Characteristics of BJT (CB, CE and CCconfigurations) and DC biasing	Transistor as Switch	Quine-McCluskey minimization technique	Introduction to Sequential circuits,Latch and Flip-Flops	Registers and Types of Registers- Serial In - Serial Out, Serial In - Parallel out
	SLO-2	***BJT Uses***	Characteristics of Digital ICs	Introduction to Combinational Circuits	RS Flip-Flops,	Parallel In - Serial Out, Parallel In - Parallel Out
S-2	**SLO-1**	Characteristics of JFET (CS, Common Drain and Common Gate configurations) and uses	***DL, RTL***	Multiplexer	Gated Flip-Flops	Universal Shift Register
	SLO-2	Differences between BJT and JFET	DTL,TTL	Demultiplexer	Edge-triggered RS FLIP-FLOP	Applications of Shift Registers
S-3	**SLO-1**	Transistor Amplifier: CE amplifier	ECL	***Decoder***	Edge-triggered D FLIP-FLOPs	Synchronous Counters
	SLO-2	Transistor Amplifier: CC ,CB amplifier	IIL	***Encoder***	Edge-triggered T FLIP-FLOPs	Asynchronous Counters
S 4-5	**SLO-1**	Introduction to Spice simulation software **Lab 1:**Design and Implementation of Half Wave and Full Wave Rectifiers using simulation package and demonstrate its working	***Lab 4: Design and implementation of transistor as aswitch***	**Lab 7**:Design and implementation of code converters using logic gates using simulation package	***Lab 10:HDL implementation of Flip-Flop***	**Lab 13**:Implementation of SISO, SIPO, PISO and PIPO shift registers using Flip- flops
	SLO-2					

S-6	**SLO-1**	Power Amplifiers: Different classes of Amplifiers and its operation-Class A	Characteristics of MOSFET *(CS ,* Common drain and Common gate configurations*)* and uses	Binary adder	Edge-triggered JK FLIPFLOPs	Changing the Counter Modulus
	SLO-2	Class B, AB and C	MOSFET Logic	***Binary adder as subtractor***	JK Master-slave FLIP-FLOP	Decade Counters
S-7	**SLO-1**	Operational Amplifiers: Ideal v/s practical Op-amp,	PMOS,NMOS	***Carry look ahead adder***	*Analysis of Synchronous Sequential Circuit,* ***State Equation, State table***	Presettable counters
	SLO-2	Performance Parameters	***CMOS Logic***	*Decimal adder*	***State Diagram***	Counter Design as a Synthesis problem
S-8	SLO-1	Op-Amp Applications –Peak detector circuit ,Comparator, Inverting and Non-Inverting Amplifiers	*Propagation delay*	Magnitude Comparator	*Synthesis of sequential circuit using Flip-Flops*	Seven segment Display and A Digital Clock.
	SLO-2	*Problem solving session*	*Problem solving session*	*Problem solving session*	*Problem solving session*	*Problem solving session*
S 9-10	SLO-1 SLO-2	**Lab 2:**Design and implement a Schmitt trigger using Op-Amp using a simulation package and demonstrate its working	**Lab 5:** Design CMOS Inverter and measure its propagation delay for both the rising edge and the falling edge.	***Lab 8:****Design and implementation of combinational circuits using simulation package*	***Lab 11:****Design and implementation of Synchronous sequential circuits using Simulation Package*	**Lab 14**:HDL for Registers and Counters
S-11	SLO-1	Effect of positive and Negative Feedback Amplifiers,	Tristate Logic	Read –only Memory	*Asynchronous sequential circuit*	D/A Conversion
	SLO-2	*Analysis of Practical Feedback Amplifiers*	It's Applications.	*Arithmetic Logic Unit*	*Transition Table*	*Types of D/A Converters*
S-12	SLO-1	*Oscillator Operation*	*FPGA Basics*	Programmable Logic Arrays	*State table*	*Problem*
	SLO-2	*Crystal Oscillator*	Introduction to HDL and logic simulation	*HDL Gate*and Data Flow modeling	*Flow table*	A/D Conversion
S-13	SLO-1	*Overview of UJT, Relaxation Oscillator,555 Timer*	*HDL System primitives, user defined primitives, Stimulus to the design*	HDL Behavioral modeling	*Analysis of asynchronous sequential circuits*	*Types of A/D conversion*
	SLO-2	*Problem solving session*	*Problem solving session*	*Problem solving session*	*Problem solving session*	*Problem solving session*
S 14-15	SLO-1 SLO-2	**Lab 3:**Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and demonstrate the working of it	**Lab 6**:HDLProgram to realize delay and stimulus in simple circuit	***Lab 9:*** *HDL program for combinational circuits*	***Lab 12:*** *HDL program for Sequential circuits*	***Lab 15:*** *Design and Implement an A/D Converter.*

Learning Resources	1. Robert L. Boylestad& Louis Nashelsky, Electronic Devices & Circuit Theory, 11th Edition,Pearson, 2013 2. Anil K Maini, Varsha Agarwal: Electronic Devices and Circuits, Wiley, 2012 3. *SPICE: A Guide to Circuit Simulation and Analysis Using PSpice*, Paul Tuinenga, 3rd Edition, Prentice-Hall, 1995, ISBN 0-13-158775-7.	4. G.K. Kharate," Digital Electronics", Oxford university Press,2012 5. M. Morris R. Mano&Michael D. Ciletti ," Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog, 6th Edition,Pearson, 2018 6. A.P. Malvino, Electronic Principles,7th Edition, Tata Mcgraw Hill Publications, 2013

Learning Assessment

	Bloom's Level of Thinking	Continuous Learning Assessment (50% weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (15%)		CLA – 3 (15%)		CLA – 4 (10%)#			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember Understand	*20%*	*20%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*	*15%*
Level 2	Apply	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*	*20%*