Unit V – Registers & Counters

Part – B

1. Design a Serial in Serial out (SISO) and Serial in Parallel out (SIPO) shift register using D flip flops.
2. Design a Parallel in parallel out shift register using D flip flops.
3. Briefly explain about universal shift register.
4. Explain the 3-bit Asynchronous ripple up counter
5. Design the binary to gray code converter
6. Design & explain the MOD 4 synchronous counter with the help of circuit diagram & truth table.
7. Design a decade counter using T FF
8. Design 3 bit up counter using SR FF
9. Design 4 bit down counter using T FF
10. Design a mod -5 counter for sequence: $2 \rightarrow 3 \rightarrow 5 \rightarrow 1 \rightarrow 7 \rightarrow 2$, using D flip-flop. The counter must be self starting with count states 0 to 1, 4 to 5,and 6 to 7.
11. Design & explain the MOD 6 synchronous counter with the help of circuit diagram & truth table.
12. Design synchronous counter for the sequence $0 \rightarrow 5 \rightarrow 3 \rightarrow 2 \rightarrow 6 \rightarrow 7 \rightarrow 0$ using D flip-flop.
13. Design 3 bit synchronous binary up/down counter using T flip-flop.
14. Design synchronous counter for the sequence $0 \rightarrow 1 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 7 \rightarrow 0$ using T flip-flop.
15. Explain the weighted resistor type digital to analog converter. Obtain the transfer characteristics of 3-bit DAC. Also discuss the advantages and disadvantages.
16. Show how successive approximation type ADC can be used to convert analog signal into digital form with circuit diagram
17. Explain R-2R ladder network of DAC with suitable circuit diagram & expression and list its merits.
18. Explain Flash type ADC with suitable circuit diagram and list its merits.