18CSC203J - COMPUTER ORGANIZATION AND ARCHITECTURE

UNIT – 1 - Question Bank

PART A

1. _____ Signals determine when a given action is to take place
a. Input
b. Output
c. Input/Output
d. Timing

Ans: d

1. A computer must have instructions which are capable to perform _____types of operations
a. Two
b. Three
c. Four
d. Five

Ans: c

1. ADD R2, LOCA -When this instruction gets executed
a. Adds the operand in Stack pointer
b. Adds the operand at Memory location LOCA
c. Adds the content of R0 and R2
d. Adds the operand and place the sum into LOCA

Ans: b

1. In multi bus structure $2^x = n$, where x is number of _____ lines and n is number of _____
a. Data, address
b. Control, address
c. Address, location
d. Data, location

Ans: c

1. In one address instruction format, when you execute the instruction ADD D, it executes the instruction as follows
a. Ac<-AC+ M[D]
b. AC->AC+M[D]
c. AC<-AC+D
d. AC->AC+D

Ans: a

1. In _____architectecture designer can decide the amount of ROM, RAM and I/O Ports
a. Microcontroller
b. Microprocessor
c. Either Microprocessor or Microcontroller
d. Neither Microprocessor nor Microcontroller

Ans: b

1. Microprocessors are characterized based on _____
a. The word size only
b. Instruction set structure only
c. Functions only
d. Word size, Instruction set structure and Functions

Ans : d

1. 16-bit Microprocessor are represented by Intel's 8086,Zilog Z800 and 80286 in _____

a. First Generation
b. Second Generation
c. Third Generation
d. Fourth Generation

Ans: c

1. 8086 uses _____stages of pipelining

a. Three
b. Four
c. Two
d. Either Three or Four

Ans: c

1. RCR represents

a. Rotate right byte
b. Rotate right through carry byte or word
c. Rotate right byte AND carry
d. Rotate right byte OR carry

Ans : b

11. Which cores helps to execute java byte codes?

A. ARM
B. Thumb
C. 8085
D. Jazella

Ans: D.

12. In ARM, _____ processor modes is used to handle the violation in accessing the memory

A. Undef

B. Abort

C. System

D. User

Ans: B.

13. How many registers are available in ARM Microprocessor?

A. 15

B. 16

C. 37

D. 36

Ans: C.

14. How many bit constants are allowed to load into the memory directly in the barrel shifter?

A. 32

B. 36

C. 16

D. 5

Ans: A.

15. Which I/O mechanism faces the issues of two wait loop?

A. Memory mapped I/O

B. Program Controlled I/O

C. Processor Controlled I/O

D. Instruction Controlled I/O

Ans: B.

16. _____ causes exception trap to the hardware vector?

A. Software Interrupt

B. Exception handling

C. Hardware Handling

D. Processor Interrupt

Ans: A.

17. Which conditional codes helps to track the overflow occurrence?

A. V

B. Z

C. N

D. C

Ans: A.

18. Which instruction is used to switch between ARM and thumb?

A. AX

B. BX

C. CX

D. DX

Ans: B.

19. Which state helps to execute the instructions of 8 bits wide?

A. ARM

B. Thumb

C. Jazella

D. 8085

Ans: C.

20. _____ registers contain the control bit status to store the temporary data?

A. SPSR

B. CPSR

C. Both CPSR and SPSR

D. LR mode

Ans: C.

21. What is computer organization?
a. structure and behaviour of a computer system as observed by the user
b. structure of a computer system as observed by the developer
c. structure and behaviour of a computer system as observed by the developer
d. All of the mentioned

Ans : a

22. Which of the following allows simultaneous write and read operations?

a. ROM
b. EROM
c. RAM
d. None of the above

Ans: c

23. Which of the following is not considered as a peripheral device?
a. CPU
b. Keyboard
c. Monitor
d. All of the above

Ans: a

24. The addressing mode used in an instruction of the form ADD XY, is
a) Absolute
b) Indirect
c) Index
d) None of these

Ans: c

25. _____ register keeps tracks of the instructions stored in program stored in memory.
a. AR (Address Register)
b. XR (Index Register)
c. (PC (Program Counter)
d. (AC (Accumulator)

Ans: c

26. An interface that provides a method for transferring binary information between internal storage and external devices is called
a. I/O interface
b. Input interface

c. Output interface
d. I/O bus

Ans: a

27. In Assembly language programming, minimum number of operands required for an instruction is/are

a. Zero
b. One
c. Two
d. Both (b) & (c)

Ans: a

28. In which addressing mode the operand is given explicitly in the instruction

a. Absolute
b. Immediate
c. Indirect
d. Direct

Ans b

29. A stack organized computer has

a. Three-address Instruction
b. Two-address Instruction
c. One-address Instruction
d. Zero-address Instruction

Ans d

30. The load instruction is mostly used to designate a transfer from memory to a processor register known as_____.

a. Accumulator
b. Instruction Register
c. Program counter
d. Memory address Register

Ans a

PART B

1. **Which part of the functional unit of the computer is known as "Brain" ? Justify your answer**

   Ans:CPU. Responsible for carrying out computational task

   Contains ALU, CU, Registers

   ALU Performs Arithmetic and logical operations

   CU Provides control signals in accordance with some timings which in turn controls the execution process

   Register Stores data and result and speeds up the operation

1. **List the step for instruction fetch technique**

   Program gets into the memory through an input device.
   Execution of a program starts by setting the PC to point to the first instruction of the program.

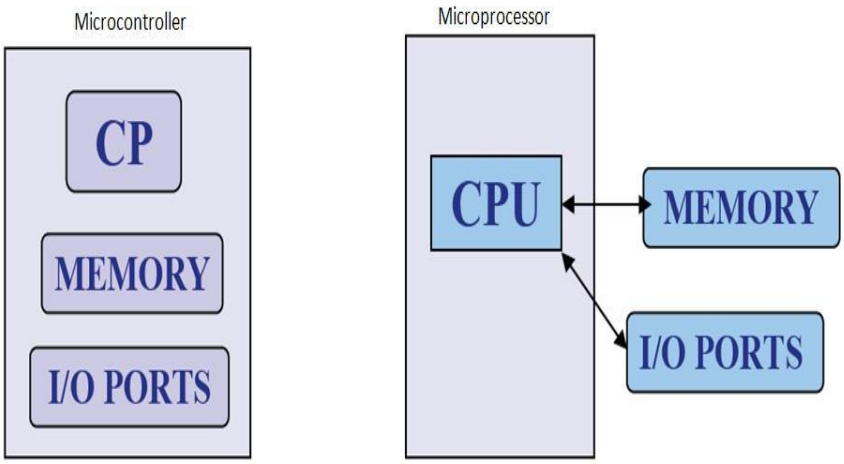
The contents of PC are transferred to the MAR and a Read control signal is sent to the memory.
The addressed word (here it is the first instruction of the program) is read out of memory and loaded into the MDR.
The contents of MDR are transferred to the IR for instruction decoding

1. **In zero address instruction evaluate (A+B) *(c+D)**

Using Zero-Address instruction

```
PUSH  A      ; TOS ← A
PUSH  B      ; TOS ← B
ADD          ; TOS ← (A + B)
PUSH  C      ; TOS ← C
PUSH  D      ; TOS ← D
ADD          ; TOS ← (C + D)
MUL          ; TOS ← (C+D)*(A+B)
POP   X      ; M[X] ← TOS
```

1. **Depict the difference between Microcontroller and Microprocessor**



5. **Differentiate Microprocessor and Microcontroller?**

S.No	Microprocessor	Microcontroller
1.	CPU is stand-alone, RAM, ROM, I/O, timer are separate	CP, RAM, ROM, I/O and timer are all on single chip
2.	Expansive	Not Expansive
3.	The instruction set of microprocessors is complex with the large number of instructions.	The instruction set of microprocessors is very simple with the less number of instrcution
4.	General Purpose	Single Purpose

6. **List the reserved Register in ARM and explain the special fucntions?**

The reserved registers are

• Stack Pointer (SP).
• Link Register (LR).
• Program Counter (PC).
• Current Program Status Register (CPSR).
• Saved Program Status Register (SPSR).

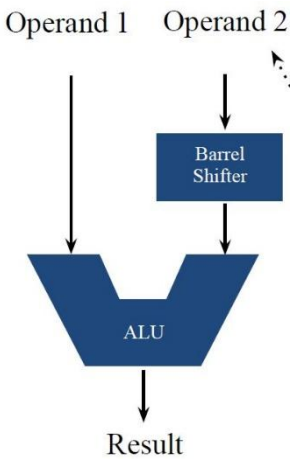
- The SPSR and CPSR contain the status control bits which are used to store the temporary data.
- The SPSR and CPSR register have some properties that are defined operating modes, Interrupt enable or disable flags and ALU status flag.
- The ARM core operates in two states 32-bit state or THUMBS state

7. How exception occurs in ARM processor?

- When an exception occurs, the ARM:
    1. Copies CPSR into SPSR_<mode>
    2. Sets appropriate CPSR bits
        - Change to ARM state
        - Change to exception mode
        - Disable interrupts (if appropriate)
    1. Stores the return address in
    1. LR_<mode>
    1. Sets PC to vector address

8. How barrel shifter is used while performing any ALU operation with two operands with a diagram?

- It can perform shit or rotate operations and it is applicable for processor and digital signal processor
- Its natural size of 4, 8, 16 , ….
- It can perform Logical Left Shift, Arithmetic Right Shift, Logical Shift Right, Rotate Right and Rotate Right Extended.



9. Mention the use of registers and List it types.

Registers are fast stand-alone storage locations that hold data temporarily. Multiple registers are needed to facilitate the operation of the CPU. Some of these registers are:

- Two registers-MAR (Memory Address Register) and MDR (Memory Data Register) : To handle the data transfer between main memory and processor. MAR-Holds addresses, MDR-Holds data
- Instruction register (IR) : Hold the Instructions that is currently being executed
- Program counter (PC) : Points to the next instructions that is to be fetched from memory
- General-purpose Registers: are used for holding data, intermediate results of operations. They are also known as scratch-pad registers.

10. Describe Logical and bit manipulation instructions.

Some instructions are:
AND bitwise AND operation
OR bitwise AND operation
NOT invert each bit of a byte or word
XOR Exclusive-OR operation over each bit

11. Evaluate (A+B) * (C+D) using Two address instruction.

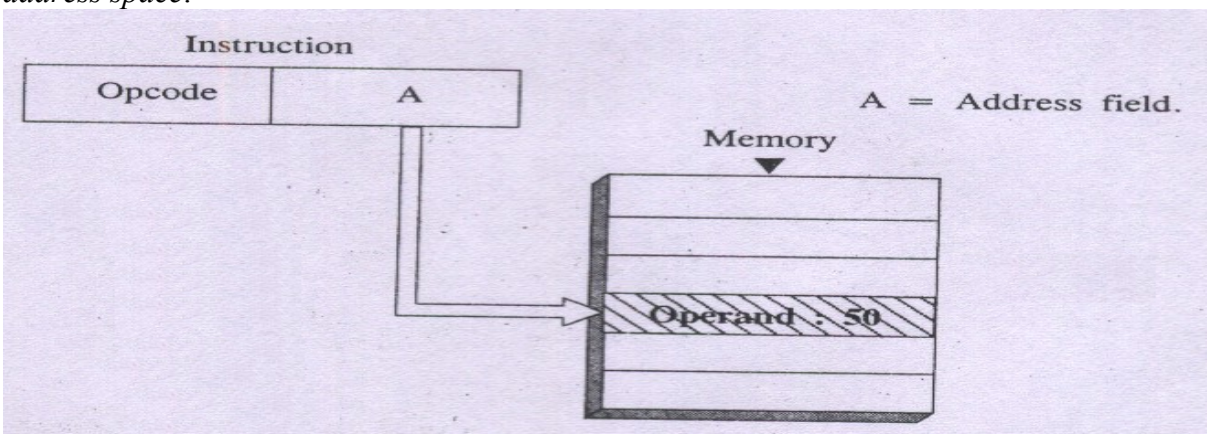
Two-Address

a. MOV A,R1 ; R1 ← M[A]
b. ADD B,R1 ; R1 ← R1 + M[B]
c. MOV C,R2 ; R2 ← M[C]
d. ADD D,R2 ; R2 ← R2 + M[D]
e. MUL R2, R1 ; R1 ← R1 * R2
f. MOV R1,X ; M[X] ← R1

12. Explain Absolute address mode.

Here operand resides in Memory and its address is given explicitly in the address field of an instruction. This scheme need only one memory reference in addition to instruction fetch cycle and no further calculation is required to compute operand address.

Direct addressing scheme is simple to use. However it offers only *limited memory address space*.



PART C

1. **Mention the need for Addressing Modes? List any seven types of addressing modes with proper example.**

Different ways in which the location of the operand is specified in an instruction is referred as addressing modes.The purpose of using addressing mode is:

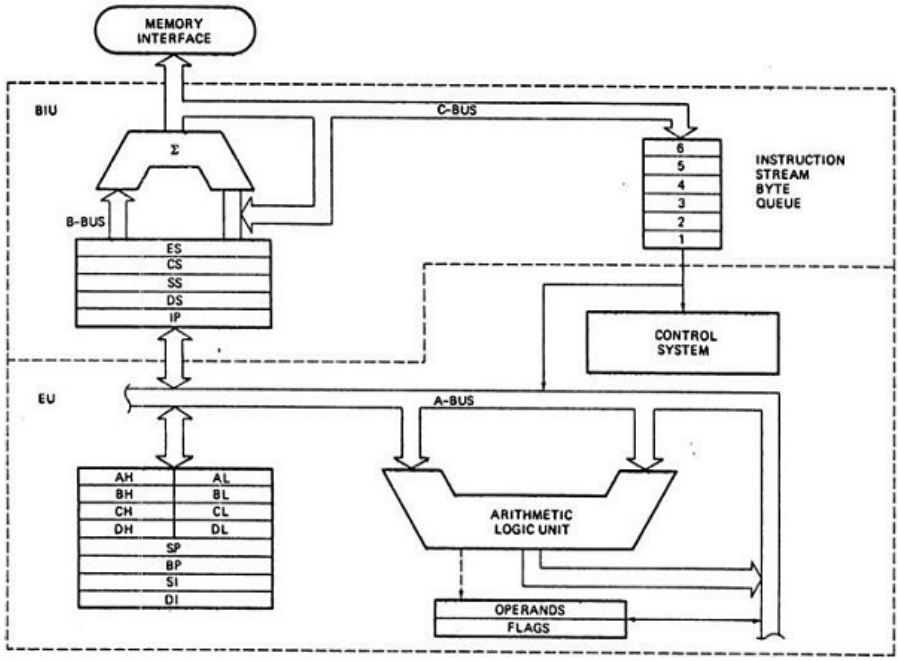
To give the programming versatility to the user.

To reduce the number of bits in addressing field of instruction.

Types of addressing modes

- Immediate Addressing
- Direct Addressing
- Indirect Addressing
- Register Addressing
- Register Indirect Addressing
- Relative Addressing
- Indexed Addressing
- Auto Increment
- Auto Decrement

1. **Draw the architecture of 8086 and describe the registers in detail**



AX – Accumulator

16 bit register

divided into two 8-bit registers AH and AL to perform 8-bit instructions also

generally used for arithmetical and logical instructions

BX – Base register

16 bit register

divided into two 8-bit registers BH and BL to perform 8-bit instructions also

Used to store the value of the offset.

CX – Counter register

16 bit register

divided into two 8-bit registers CH and CL to
perform 8-bit instructions also
Used in looping and rotation

DX – Data register
16 bit register
divided into two 8-bit registers DH and DL to
perform 8-bit instructions alsoSP – Stack pointer
16 bit register
points to the topmost item of the stack
If the stack is empty the stack pointer will be (FFFE)H
It's offset address relative to stack segment

BP –Base pointer
16 bit register
used in accessing parameters passed by the stack
It's offset address relative to stack segment
Used in multiplication an input/output port addressing

SI – Source index register
16 bit register
used in the pointer addressing of data and
as a source in some string related operations
It's offset is relative to data segment

DI – Destination index register
16 bit register
used in the pointer addressing of data and
as a destination in string related operations
It's offset is relative to extra segment.

IP - Instruction Pointer
16 bit register
stores the address of the next instruction
to be executed
also acts as an offset for CS register.

Segment Registers

CS - Code Segment Register:
user cannot modify the content of these registers
Only the microprocessor's compiler can do this

DS - Data Segment Register:
The user can modify the content of the data segment.

SS - Stack Segment Registers:
used to store the information about the memory segment.
operations of the SS are mainly Push and Pop.

ES - Extra Segment Register:
By default, the control of the compiler remains in the DS where the user can add and modify the instructions
If there is less space in that segment, then ES is used
Also used for copying purpose

Flag or Status Register
16-bit register
contains 9 flags
remaining 7 bits are idle in this register

These flags tell about the status of the processor after any arithmetic or logical operation
IF the flag value is 1, the flag is set, and if it is 0, it is said to be reset.

3. **Write a program to add two 16 bit numbers**

```
DATA SEGMENT                ; Data Segment
N1 DB 0802H
N2 DB 0206H
RES DB ?
DATA ENDS

CODE SEGMENT                ; Code segment
ASSUME CS: CODE, DS: DATA
START:
MOV AX, DATA
MOV DS, AX
MOV AL, N1
MOV BL, N2
ADD AL, BL
MOV RES, AL
INT 21H
CODE ENDS
END START
```

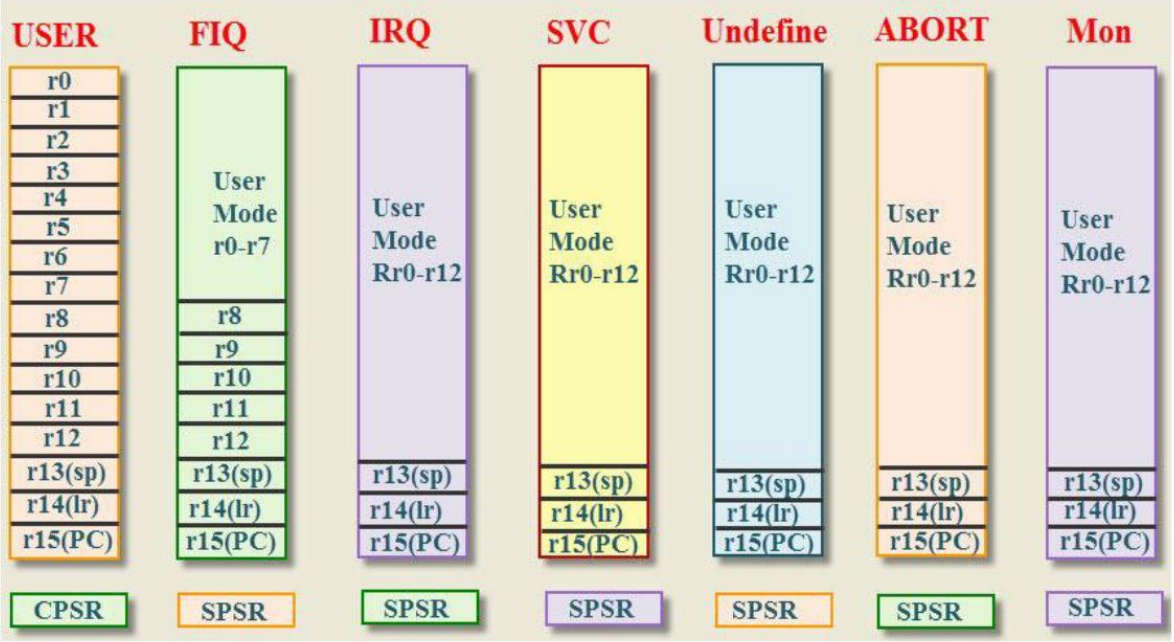
4. **Explain ARM Microcontroller by listing various processing modes with an diagram?**

ARM micrcontroller is a load store reducing instruction set computer architecture means the core cannot directly operate with the memory.

- The data operations must be done by the registers and the information is stored in the memory by an address.
- The ARM cortex-M3 consists of 37 register sets wherein 31 are general purpose registers and 6 are status registers.

The ARM uses seven processing modes to run the user task.

- USER Mode
- FIQ Mode
- IRQ Mode
- SVC Mode
- UNDEFINED Mode
- ABORT Mode
- Monitor Mode

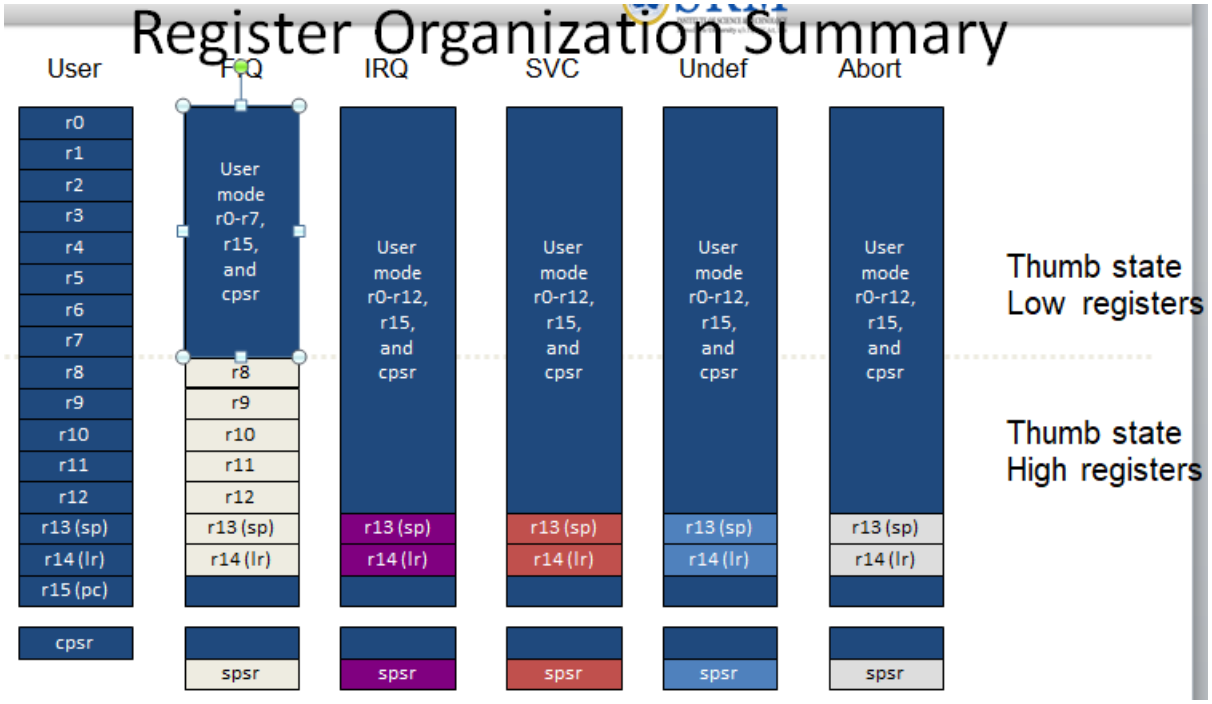


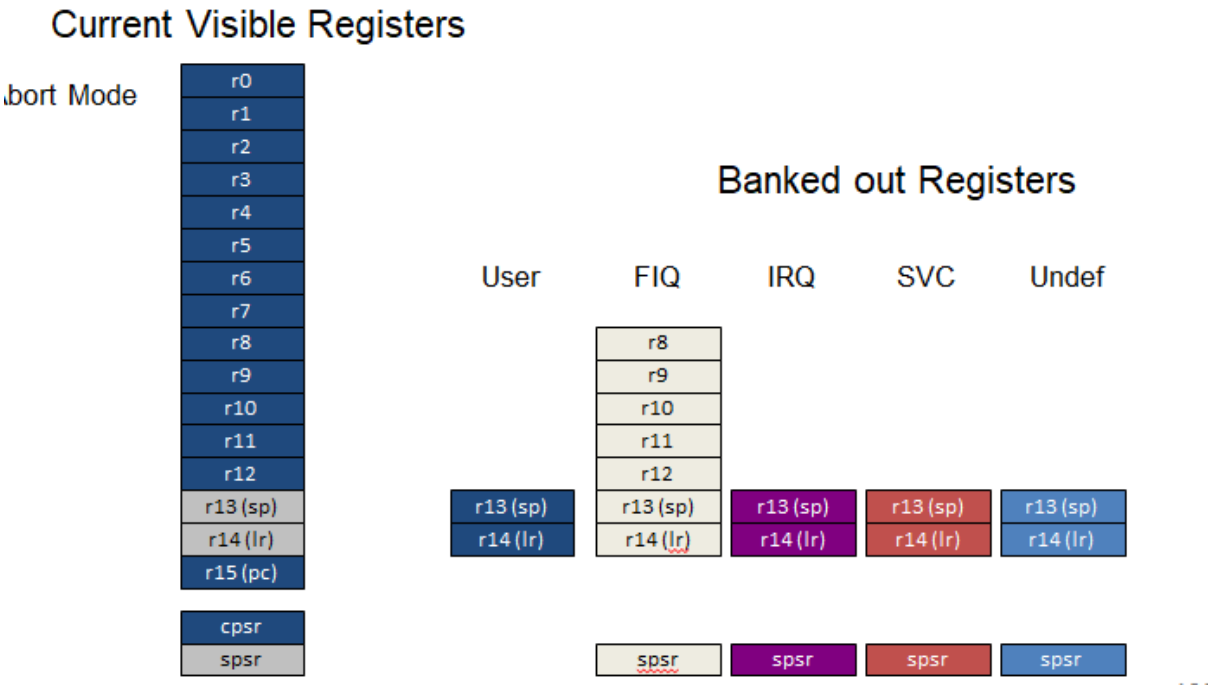
5. Explain about ARM processor Register set and Exception handling with examples.

- ARM has 37 registers all of which are 32-bits long.
    - 1 dedicated program counter
    - 1 dedicated current program status register
    - 5 dedicated saved program status registers
    - 30 general purpose registers
    - The current processor mode governs which of several banks is accessible. Each mode can access
    - a particular set of r0-r12 registers
    - a particular r13 (the stack pointer, sp) and r14 (the link register, lr)
    - the program counter, r15 (pc)
    - the current program status register, cpsr

  Privileged modes (except System) can also access

    - a particular spsr (saved program status register)





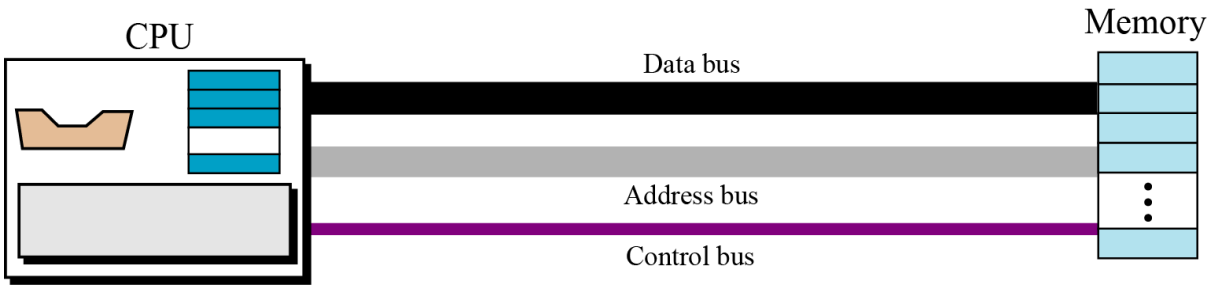
- Condition code flags
  - N = **N**egative result from ALU
  - Z = **Z**ero result from ALU
  - C = ALU operation **C**arried out
  - V = ALU operation o**V**erflowed
- Sticky Overflow flag - Q flag
  - Architecture 5TE/J only
  - Indicates if saturation has occurred
- J bit
  - Architecture 5TEJ only

- J = 1: Processor in Jazelle state

- Interrupt Disable bits.
  - I = 1: Disables the IRQ.
  - F = 1: Disables the FIQ.
  - T Bit
  - Architecture xT only
  - T = 0: Processor in ARM state
  - T = 1: Processor in Thumb state
- Mode bits
  - Specify the processor mode

6. Mention the use of Bus structure? List the types of Bus structures and explain with diagram.

The CPU and memory are normally connected by three groups of connections, each called a bus: data bus, address bus and control bus



BUS STRUCTURE

- Group of wires which carries information from CPU to peripherals or vice – versa
- **Single bus structure**: Common bus used to communicate between peripherals and microprocessor

Drawbacks of the Single Bus Structure

- The devices connected to a bus vary widely in their speed of operation.
  - Some devices are relatively slow, such as printer and keyboard.
  - Some devices are considerably fast, such as optical disks.
  - Memory and processor units operate are the fastest parts of a computer.
- Efficient transfer mechanism thus is needed to cope with this problem.
  - A common approach is to include buffer registers with the devices to hold the information during transfers .

- An another approach is to use two-bus structure and an additional transfer mechanism

TWO BUS STRUCTURE:

- **In two – bus structure** : One bus can be used to fetch instruction other can be used to fetch data, required for execution. The bus is said to perform two distinct functions The main advantage of this structure is good operating speed but on account of more cost.

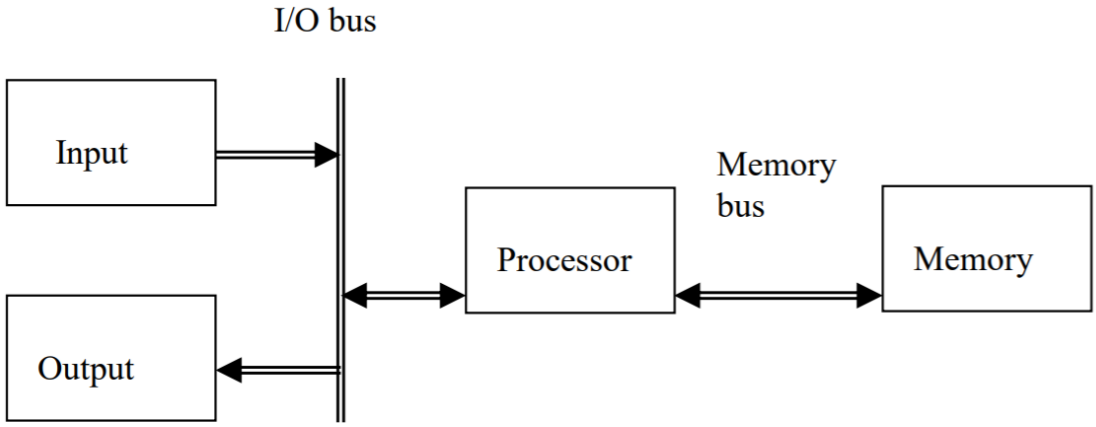


Figure 2.2 Two-bus Structure

MULTI BUS STRUCTURE

To improve performance **multi bus** structure can be used.