

UM10883

PN7462AU Quick Start Guide - Development Kit

Rev. 1.4 — 07 September 2017
319814

User manual
COMPANY PUBLIC

Document information

Info	Content
Keywords	PN7462AU, Development Kit, Customer board, Quick Start Guide, functional description of the customer board, NFC Cockpit
Abstract	This document describes PN7462 Controller Development Kit. It also describes PN7462 software stack, gives directions to run example application using the MCUXpresso IDE. Document provides PN7462 customer board configuration instructions, gives board hardware overview and provides basic steps how to use NFC Cockpit application.



Revision history

Rev	Date	Description
1.4	20170907	Updated Getting started description PN7462 plugin for MCUXpresso not needed from version 10.0.2 Reworked NFC Cockpit installation description
1.3	20170511	Development Kit description added MCUXpresso IDE support added Board description and schematic updated SW examples description updated Abbreviation section added
1.2	20170216	PNEV7462B customer demo board V2.2 added SW examples description updated Guidelines how to upgrade firmware are updated Figures updated
1.1	20161124	SW examples description updated Guidelines how to import projects are updated Figures updated
1.0	20160329	First release

Contact information

For more information, please visit: <http://www.nxp.com>

1. Getting started

This document gives information about how to start software and hardware development with PN7462 NFC Controller Development Kit (OM27462CDK). Development kit ensures easy and quick development of NFC applications running on the PN7462. Main part of the development kit is PN7462 Customer board - PNEV7462B. This guide gives extensive board hardware overview and describes board configuration options.

Document further describes PN7462AU FW and SW examples package. It gives step by step instruction to install MCUXpresso Integrated Development Environment and to run example application. It is also provided extensive introduction to the PN7462 software stack and describes each example in details.

Finally, document describes NFC Cockpit, custom windows application used in prototyping and optimization.

1.1 Introduction to PN7462 NFC Controller Development Kit

This kit is a part of the product support package. It is designed to demonstrate all functionalities of the PN7462 family and eases development of customized applications and antenna design.



Fig 1. PN7462 NFC Controller Development Kit

Kit contains:

- (1) PNEV7462B with standard 65x65mm antenna
- (2) 30x50mm antenna with matching components

- (3) 3 PCBs for individual antenna matching
- (4) Sample NFC cards and tags
- (5) 2 USB cables; A to mini and micro
- (6) 10 PN7462 samples
- (7) 7.5V DC power supply
- (8) LPC-Link 2 debug adapter (OM13054)

1.2 First steps with development kit

PN7462 Customer board contained in this kit is preloaded with USB CCID reader application. Reader supports contact and contactless interface. The USB Stack and CCID class is implemented in the PN7462AU. For the operation, the default Windows CCID driver is used. The USB CCID reader can be tested with any PC/SC application running on the PC with Windows OS.

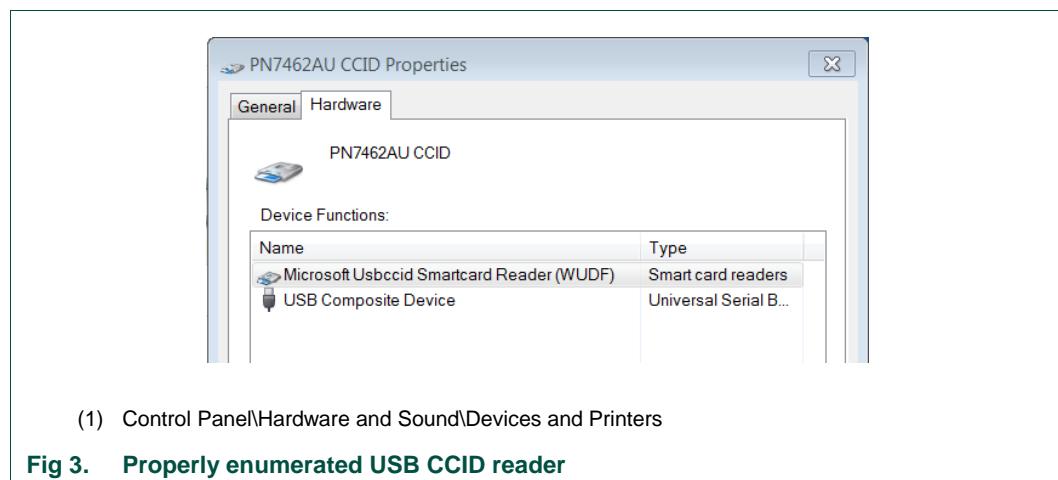
To start CCID reader:

1. Connect provided power supply to the board DC socket
2. Connect the customer demo board via USB (A to micro) to the PC running Windows OS



Fig 2. Connecting the board to the USB host and DC power supply

Customer board gets powered and CCID reader application starts. Board's LED8-LED10 start to light in circular pattern. Windows starts device detection, identification and driver loading.



At this point a favorite PC/SC application can be started and tested with cards contained in the kit.

2. Hardware overview of the PN7462AU Customer Demo Board

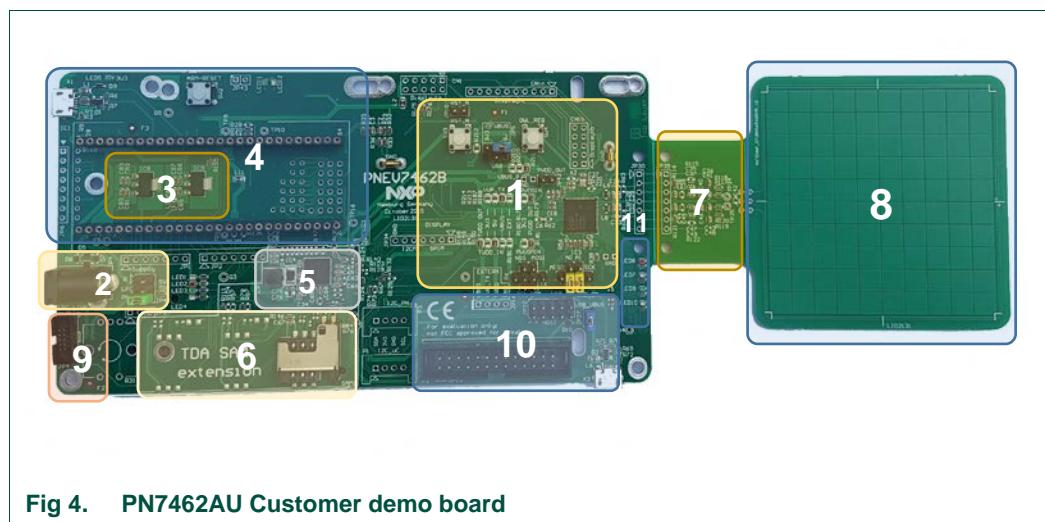
2.1 PNEV7462B concept

The basic concept of the PNEV7462B board is to enable hardware and software evaluation of typical PN7462AU design and to support prototyping own antenna circuitry. The supporting NFC Cockpit tool enables antenna tuning, DPC calibration and the related TX and RX optimization in run time.

After successful optimization, register settings can be stored in the PN7462AU EEPROM as well as saved in configuration file and used as input in design time.

PN7462AU FW and SW Examples available on the product page, ranging from POS demo, contact and contactless CCID reader, P2P application, NFC forum related examples, are customized primarily for customer board and supported by MCUXpresso, Keil or IAR development tools.

2.2 PN7462AU Customer Demo Board



The board consists of the following blocks:

- (1) PN7462AU circuitry with reset and download pushbuttons,
- (2) External power supply connector (5.5/2.1 socket) and power supply selector,
- (3) LDO regulator circuit for 3.3V and 5V
- (4) LPCXpresso m-bed expansion circuit
- (5) TDA8026 multiple smart card interface circuit
- (6) Antenna coil and related matching circuit (marked in green and orange)
- (7) Smart card socket (main slot on bottom PCB layer) and SIM size slots on top layer
- (8) 65x65mm antenna coil

- (9) 10-pin Cortex debug connector
- (10) 26-pin shroud GPIO header and USB micro B female connector
- (11) Diagnostic LED block connected to PN7462AU

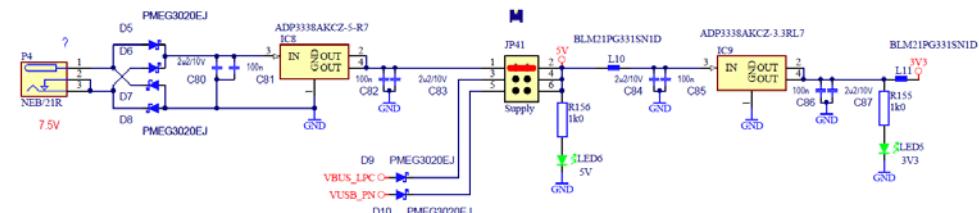
2.2.1 Power circuitry

The power circuit consists of the power socket, diode bridge, selection jumper JP41 and two low dropout linear voltage regulators. Power options include USB and LPC-Link 2 but for the best performance external power source is recommended.

Note:

PN7462B v2.1: external power supply 7.5V max.

PN7462B v2.2: external power supply 13.5V max.



- (2) USB supply, external supply & and LPC supply

Fig 5. PNEV7462B supply

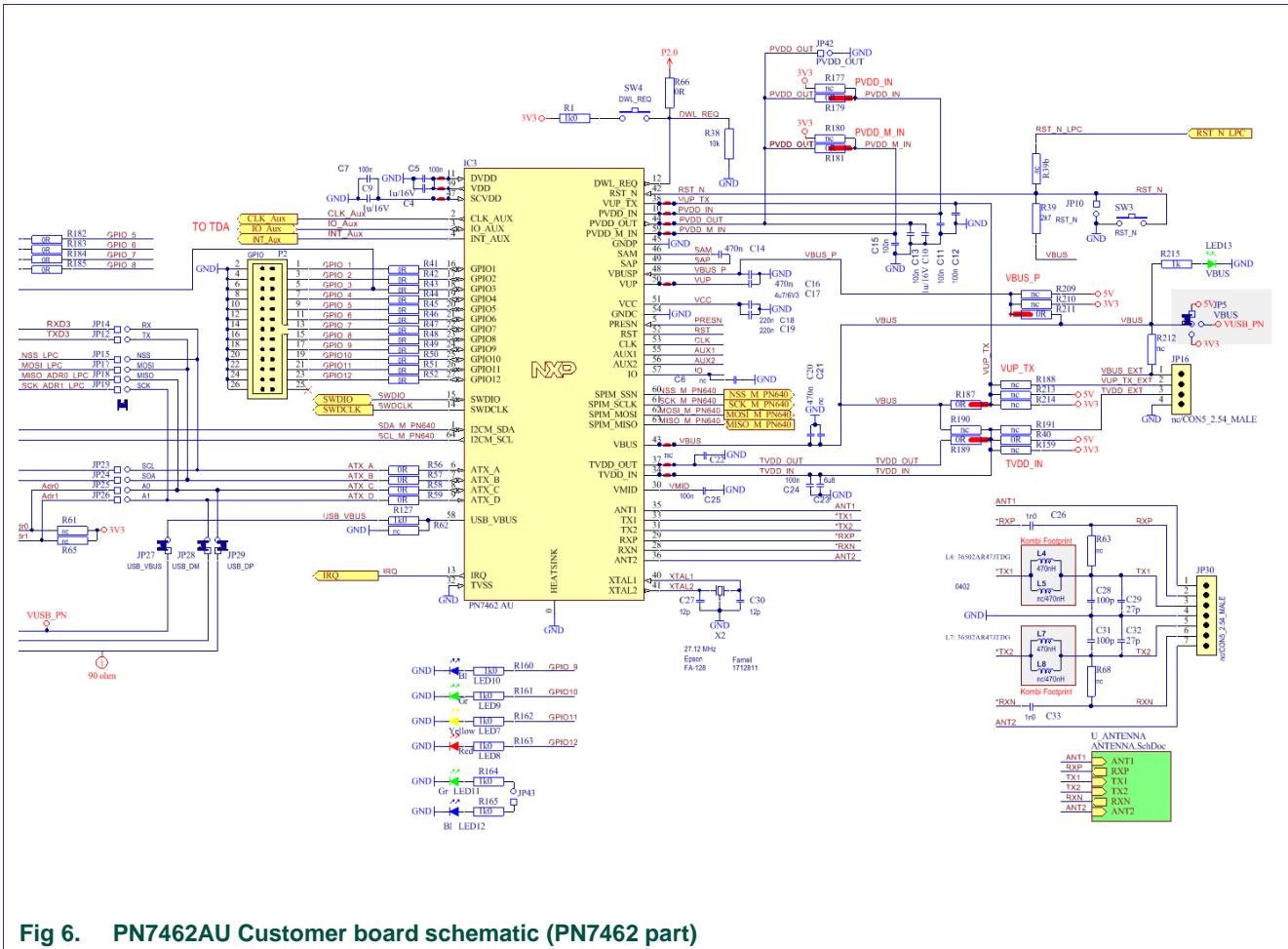
2.2.2 PN7462AU block

The main part on the evaluation board is PN7462AU. It features a 32-bit ARM Cortex-M0-based NFC microcontroller offering a one chip solution to build contact and contactless applications.

Key features are:

- 20 MHz Cortex-M0 core
 - 80/160 kB Flash, 12 kB RAM, 4 kB EEPROM
- State-of-the-art RF interface: Full NFC, EMVCo 2.6
 - Read/Write, Card Emulation & Peer-to-Peer Modes
 - Transmitter current up to 250 mA
 - Full MIFARE family support,
- DPC for optimized antenna performance
- Extensive host and peripheral interfaces

- Host/slave & master interfaces: I2C, SPI, USB, HSUART, I2CM, SPIM
- Optional contact interface (PN7462): UART, ISO/IEC 7816, EMVCo 4.3
- 12 to 21 GPIOs



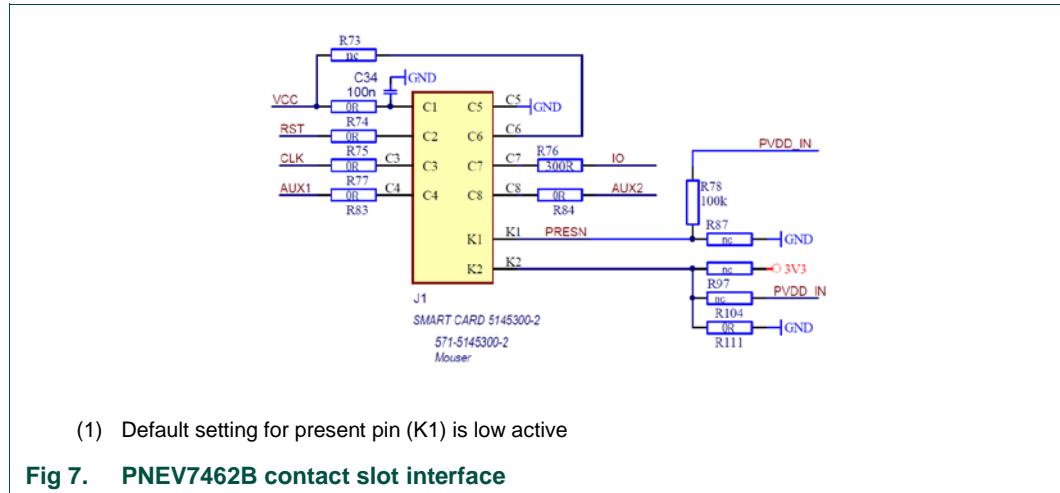
2.2.3 LPCXpresso block

This block provides expansion interface for LPCXpresso board providing standard LPCXpresso/m-bed expansion connector (DIL54). LPCXpresso SPIM and I2CM interfaces are routed to the PN7462AU host interface selector.

Additionally, board features a USB micro B connector routed to the LPC board USB interface and the LPC board reset circuit. Diagnostic LED1-4 are connected to LPC port pins.

2.2.4 Smartcard interface

The PN7462AU integrates contact interface to enable communication with ISO7816 and EMVCo contact smart cards, without the need for an external contact front end. It offers a high level of security for the cards by performing current limitation, short-circuit detection, ESD protection as well as supply supervision. Card slot/contactor is located on the customer board bottom layer.



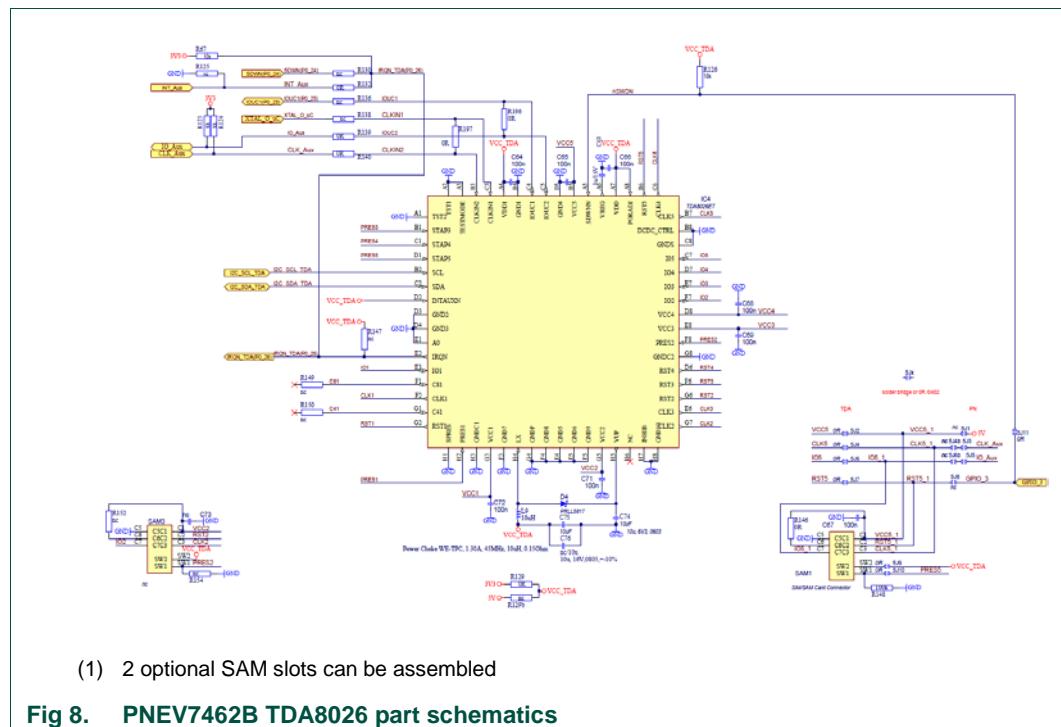
2.2.5 TDA SAM extension interfaces

The PN7462AU can handle more than one smart card by controlling an extra contact interface TDA8026 product from NXP. In this use case, the PN7462AU is the main controller for the electrical and protocol part for the main card slot, while the secondary slots are electrically controlled by an extra contact front-end interface (TDA), the PN7462AU being the protocol controller for these extra slots. TDA8026 I₂C port is connected to the PN7462 I₂CM to enable IC configuration.

In this case, several smart cards can be activated at the same time, but the communication with each smart card has to go sequentially: it is not possible to communicate with two smart cards at the same time as there is only one protocol control block for all cards.

TDA8026 is required to handle the smart card electrical interface. The connection between the PN7462AU and the TDA is composed of 2 parts:

- The host interface control, where the PN7462AU is the master, controlling the TDA behavior: card activation, deactivation, TDA configuration (voltage level, clock division, slew rates...)
- The ISO7816 link: the PN7462AU handles the ISO7816 communication protocol and uses the TDA as a level shifter for the clock and I/O signals.



2.2.6 Antenna coil and related matching circuit

In general, there are two antenna tunings possible with PN7462 customer board:

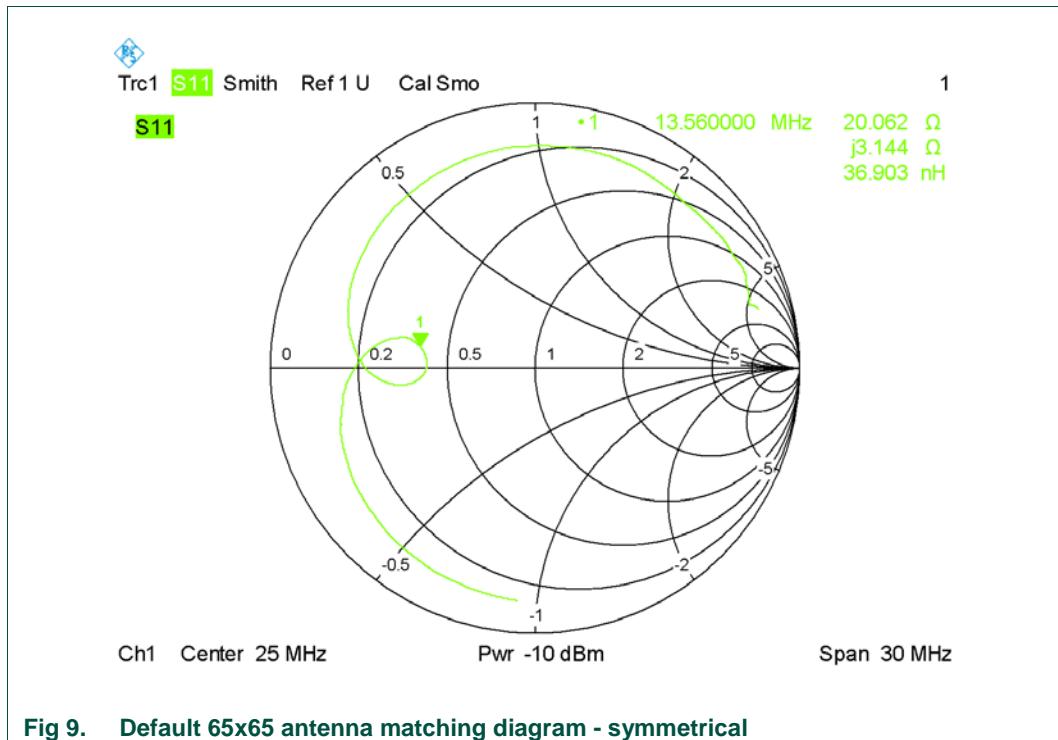
- asymmetrical
- symmetrical

The asymmetrical tuning is the standard tuning as taken from the existing NXP NFC frontend design recommendations. It uses EMC cut off frequencies >17MHz, which results in an asymmetrical transfer function, but shows a good detuning and loading behavior. The asymmetrical transfer function has some disadvantages regarding the pulse shapes and receiver performance, and requires a slightly reduced Q factor of the antenna coil circuit itself.

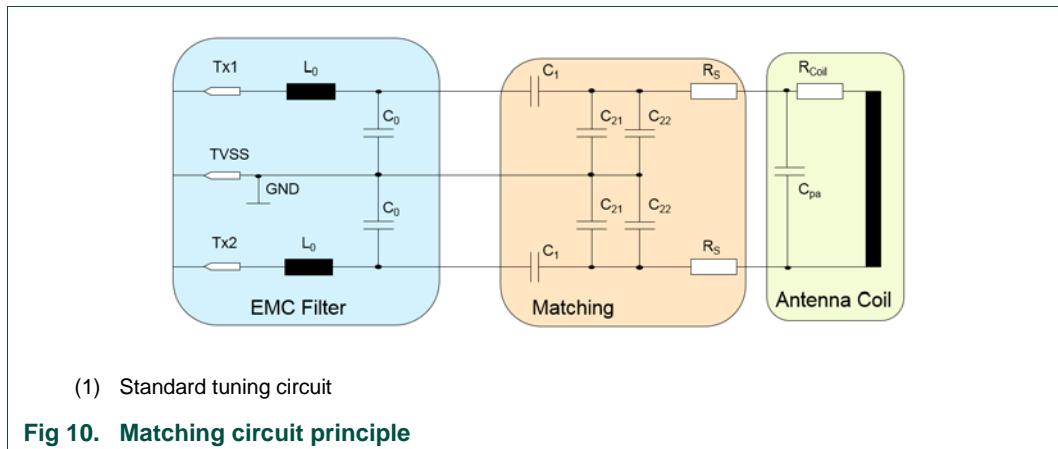
Symmetrical coupling is used with DPC (Dynamic Power Control) feature of the PN7462 and offers an improved overall RF performance. This requires the antenna to be "symmetrically" tuned and it requires the AGC to correlate with the driver current ITVDD, and it requires the dynamic power control to be properly calibrated. The DPC Antenna tuning ("symmetrical tuning with DPC") combines the advantages of enough field strength at 4cm with the automatic power control to limit the maximum field strength at a close distance. This tuning assures passing related EMVCo tests.

2.2.6.1 Default board antenna

Default 65x65 mm board antenna is designed to use symmetrical tuning (see Fig 9). This antenna is not an optimal antenna as such, but intends to demonstrate the performance and register settings of the PN7462 under typical design constraints like LCD or other metallic object (e.g. PCB) inside the antenna area. Inside of the antenna area is filled of 10x10 fields simulating metallic object in real application.



The antenna connection uses the standard tuning circuit Fig 10. The EMC filter is typically a second order low pass filter as shown in Fig 18, and contains an inductor (L_0) and a capacitor (C_0). The cut off frequency defines the overall detuning behavior as well as the transfer function of the antenna circuit. For symmetrical (DPC) tuning, EMC filter is designed with a cut off frequency of $f_{EMC} = 14.8$ MHz, and the antenna impedance is tuned to $Z = 20\Omega$.



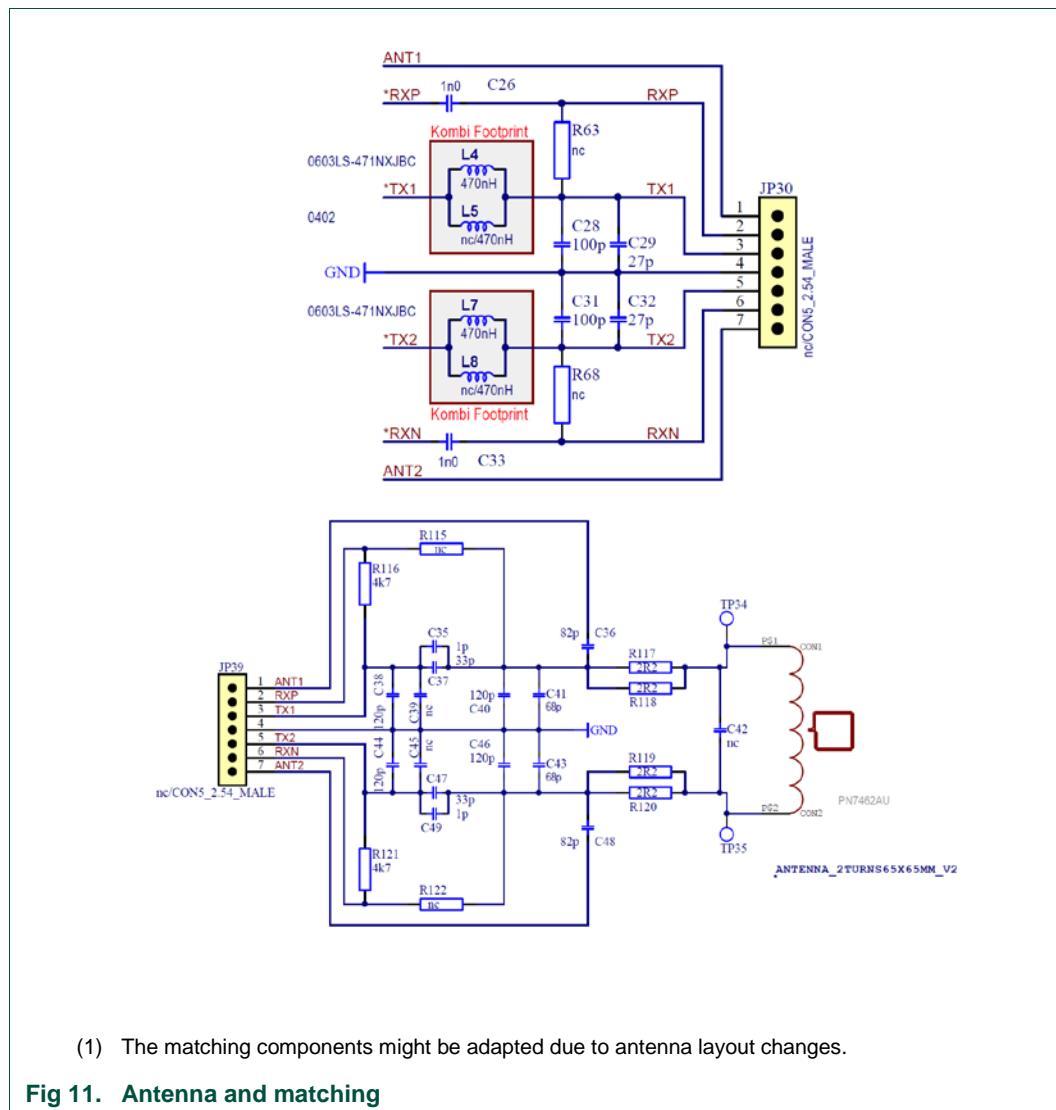


Table 1 lists components for the “symmetric” matching.

Table 1. Assembled matching components

General component	Component PNEV7462B	Value	Comment
L0	L4/ L7	470nH	PNEV7462B V2.1->0603LS-471NXJBC PNEV7462B V2.2->36502AR47JTDG
C0	C28/ C31	100pF	C0 split in 3 parallel capacitors
	C29/ C32	27pF	
	C38/ C44	120pF	
C1	C35/ C49	33pF	

General component	Component PNEV7462B	Value	Comment
	C37/ C47	1pF	C1 split in 2 parallel capacitors
C21	C40/ C46	120pF	
C22	C41/ C43	68pF	
R _s	R117/ R119	2,2Ω	R _s split in 2 parallel resistors
	R118/ R120	2,2Ω	

Note: Without proper DPC calibration the loading and detuning might exceed the ITVDD limit, if the symmetrical tuning is used. This might destroy the NFC reader IC

2.2.6.2 PCB for individual antenna matching

Development kit contains 3 PCB boards for individual antenna matching. This boards are intended for prototyping custom asymmetrical or symmetrical (DPC) antenna design. Default matching circuit can be replaced by individual antenna matching PCB.

2.3 Customer demo board available versions

Following Versions of the PNEV7462B are available

- PNEV7462B V2.1
- PNEV7462B V2.2

2.3.1 PNEV7462B V2.1

The V2.1 of the customer evaluation board is the initial version of the board that comes with the launch of the PN7462AU chip.



Fig 12. PNEV746B V2.1

2.3.2 PNEV7462B V2.2

The V2.2 of the customer evaluation board is the replacement and latest version of the customer evaluation board incl. FCC certification. Functionality of the V2.2 is the same as of V2.1.

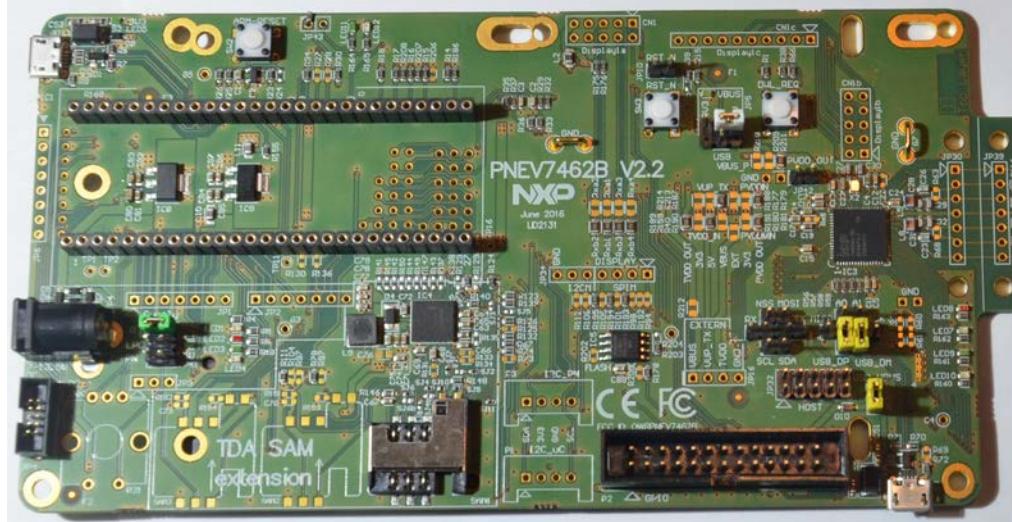


Fig 13. PNEV7462B V2.2

2.3.2.1 Design changes V2.1 to V2.2:

- External supply maximum value increased from 7.5V to 12V
- Different routing (PNEV7462B V2.1 stays the board reference design which can be obtained from the NXP DocStore). Layout recommendations for NFC readers can be found in AN11090.
- Changed EMC filter components

3. Configuration of the PN7462AU Customer board

3.1 Board power settings

There are three power supply options on the PNEV7462B board. It can be powered either from an external off-board power supply on DC power connector, from LPC USB connector X1 and from USB port on connector X3.

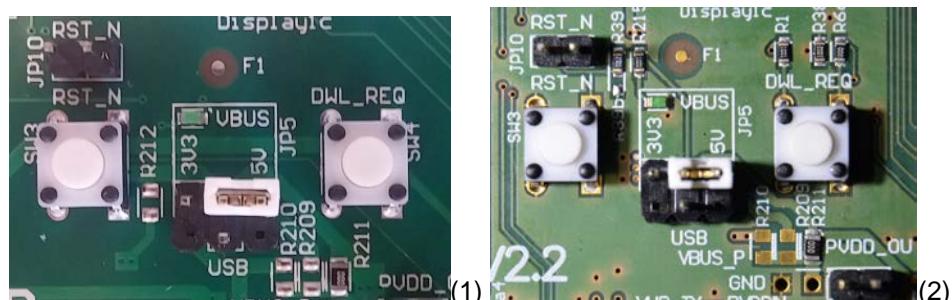
Jumper JP41 setting (Fig 14) needs to be done to prepare the board for one of the power supply options.



Fig 14. Board Power settings

3.1.1 PN7462AU supply options

The boards offer several ways of supplying the PN7462AU IC. The main chip supply (VBUS) can be set to 5V, 3.3 V or USB supply. The corresponding setting is described in Fig 15



- (1) PNEV7462B V2.1
- (2) PNEV7462B V2.2

Fig 15. VBUS supply jumper setting

3.1.2 Power supply status LED

If all jumpers are set correctly, the following LEDs should light green:

3V3, 5 V and VBUS. In Fig 16 the position of the three different LED's is shown.

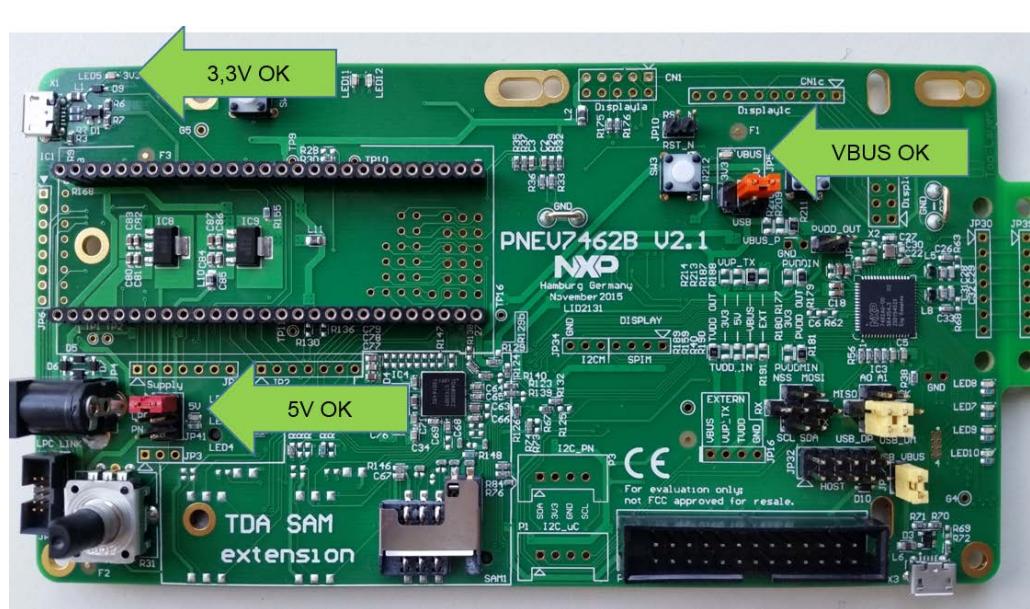


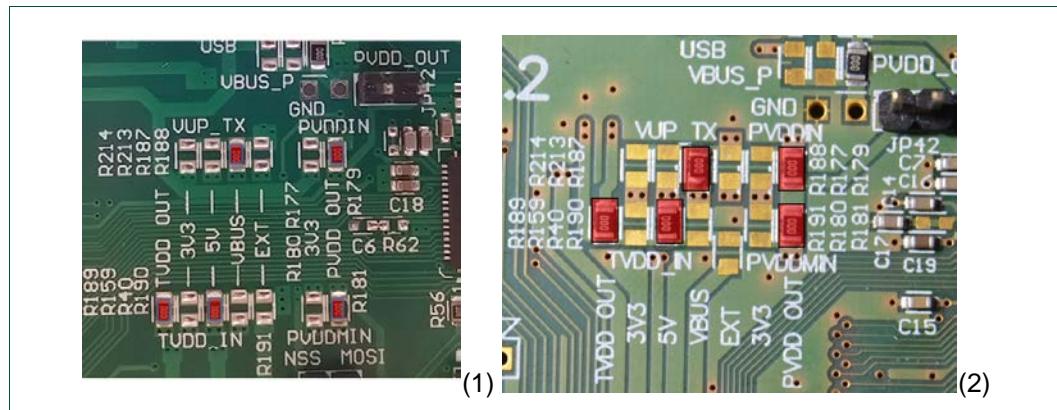
Fig 16. Supply indicator

3.1.3 Supply options for PVDD, VUP_TX and TVDD

The PN7462AU allows different options of supplying PVDD_IN, PVDDM_IN as well as for TVDD_IN and VUP_TX.

The default setting is to use the internal supply for PVDD as well as TVDD. That means default setting is PVDD_IN connected to PVDD_OUT, and TVDD_IN connected to TVDD_OUT.

The default setting on the customer board is marked in Fig 17.



- (1) PNEV7462B V2.1 (red marked are the default settings)
- (2) PNEV7462B V2.2 (red marked are the default settings)

Fig 17. Default supply connection of the PN7462AU using all blocks

To change settings, the corresponding shortcut resistors (marked in Fig 17) needs to be placed to the corresponding position (default settings are marked in green):

Table 2. Supply options

Supply options

VUP_TX	3V3
	5V
	VBUS
	EXT
TVDD_IN	TVDD_OUT
	3V3
	5V
	VBUS
	EXT
PVDD_IN	3V3
	PVDD_OUT
PVDDM_IN	3V3
	PVDD_OUT

Note:

If PVDD is externally supplied, the Jumper 42 (PVDD_OUT) needs to be set. By setting this Jumper the PVDD_OUT is shorted to GND and the PN7462AU turns off the PVDD LDO.

3.2 Host interface configuration

The PN7462AU supports interfacing one out of the four different host: USB 2.0 full speed with USB 3.0 hub connection capability, HSUART for serial communication, supporting standards speeds from 9600 bit/s to 115200 bit/s, and faster speed up to 1.288 Mbit/s, SPI with half duplex and full duplex capability with speeds up to 7 Mbit/s and I2C supporting standard mode, fast mode and high-speed mode with multiple address support.

The PN7462AU connects to host through four pads with alternate function: ATX_A, ATX_B, ATX_C and ATX_D. These pads are routed at the JP32 10-pin header, according to the following table:

Table 3. PN7462 HIF pins

Pin name	Description	JP32 pin
ATX_A	HSU_RX/I2C_SCL/SPI_NSS	1
ATX_B	HSU_TX/I2C_SDA/SPI_MOSI	3
ATX_C	HSU_RTS_N/SPI_MISO/USB_DP	5
ATX_D	HSU_CTS_N/SPI_MOSI/USB_DM	7

3.2.1.1 USB Host Interface configuration

The yellow marked jumpers on the following picture shows how the board needs to be set for using the USB host interface of the chip. The USB micro connector X3 is located in the lower right corner of the board.

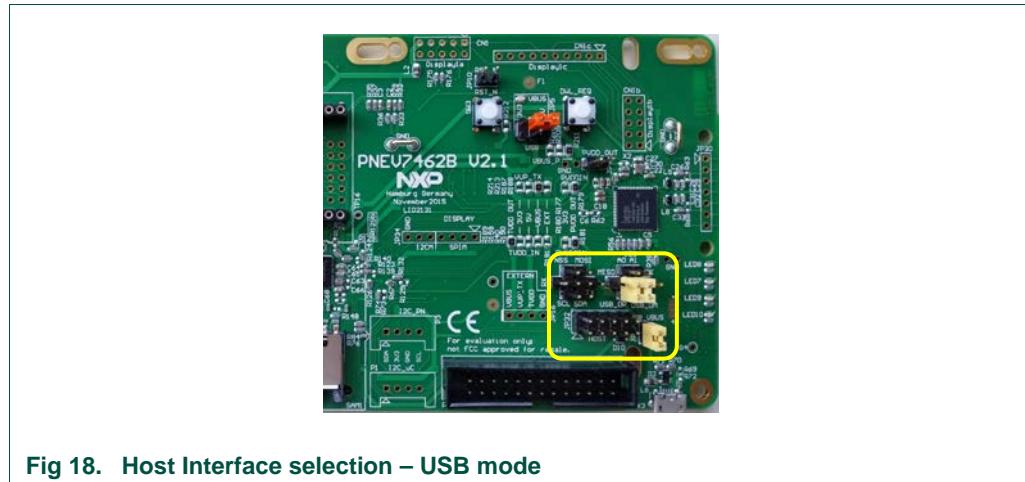


Fig 18. Host Interface selection – USB mode

3.2.1.2 I2C Host Interface configuration

The yellow marked jumpers (Fig 18) need to be set for using the I2C host interface of the chip with LPCXpresso expansion board. This will connect the I²C SCL of the PN7462AU to the I/O P0 (28) and also the I²C SDA of the PN7462AU to the I/O P0(27) of the LPCXpresso board.



Fig 19. Host Interface selection - I2C mode

In case that external host needs to be connected to the PN7462 over I2C interface then corresponding I2C interface lines can be accessed directly on the JP32 according the Table 3 and additional jumper configuration is not needed.

3.2.1.3 SPI Host Interface configuration

The yellow marked jumpers (Fig 20) needs to be set for using the SPI host interface of the chip. This will connect the SPI_MOSI of the PN7462AU to the I/O P0(18), SPI_MISO to the I/O P0(17), SCK to the I/O P0(15), and also the NSS of the PN7642AU to the I/O P0(16) of the LPCXpresso board.

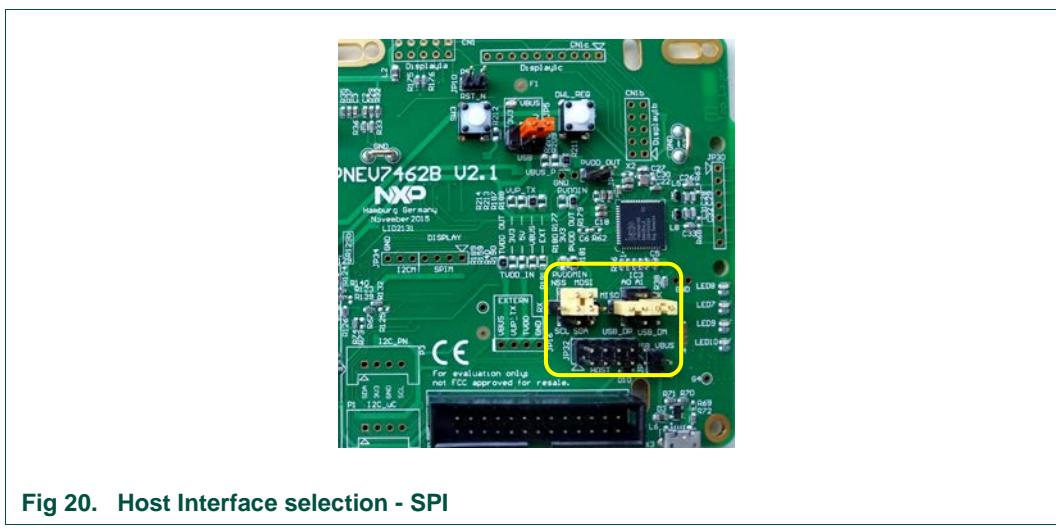


Fig 20. Host Interface selection - SPI

In case that external host needs to be connected to the PN7462 over SPI interface then corresponding SPI interface lines can be accessed directly on the JP32 according the Table 3 and additional jumper configuration is not needed.

3.2.1.4 HSUART Interface configuration

The yellow marked jumpers (Fig 21) needs to be set to select HSUART host interface. This will connect the UART_RX of the PN7462AU to the I/O P0(0), UART_TX of the PN7462AU to the I/O P0(1) of the LPCXpresso board extension m-bed connector.

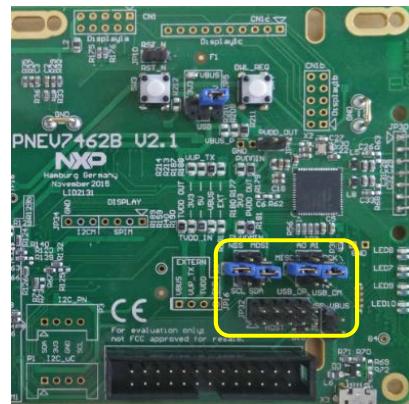


Fig 21. Host Interface selection - HSU

In case that external host needs to be connected to the PN7462 over HSUART interface then corresponding HSUART interface lines (RX, TX, CTS, RTS) can be accessed directly on the JP32 according the Table 3 and additional jumper configuration is not needed.

3.2.2 Debug interface

The PN7462 Customer Board is equipped with a SWD interface. The SWD 10-pin Cortex connector is placed in the bottom left corner of the board. LPC-Link 2 standalone debug probe can be used to flash or debug application on the PN7462AU as illustrated on the Fig 22.

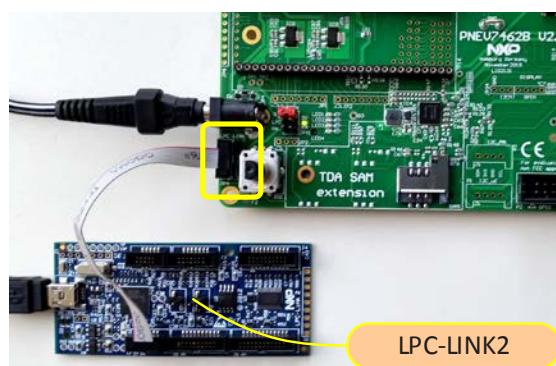


Fig 22. JTAG/SWD debug probe connector

4. NFC Cockpit getting started

The NFC Cockpit is a Windows application designed to help explore the functionality of the PN7462AU and execute RF and antenna design related tests and parametrization. It allows a direct register access as well as EEPROM read and write access, and it allows to test and to calibrate the DPC and other features.

4.1 Board preparation

To use NFC Cockpit the PNEV7462B board must be configured to use USB host interface as described in Fig 18, which is the default configuration. The use of an external power supply is recommended as described in chapter 3.1.

4.2 NFC Cockpit installation

The NFC Cockpit can be downloaded from the NFC Cockpit product web page [4]. After successful download, follow the installation wizard and finish the installation. The default installation directory is C:\nxp\NxpNfcCockpit_vx.x.x.x, where is x.x.x.x is version number.

4.3 Firmware, EEPROM settings and driver

NFC Cockpit requires a dedicated firmware running on the PN7462AU. This firmware application implements CDC USB class device (VCOM). The NFC Cockpit directs commands to the VCOM port and dedicated firmware executes commands on the hardware level.

NFC Cockpit firmware can be updated by using primary downloader functionality (see chapter 6.8). Firmware binary is available with NFC Cockpit installation and located in “<installation directory>\firmware\PN7462AU”.

Additionally, appropriate EEPROM settings needs to be updated, the EEPROM settings binary is located in “<installation directory>\firmware\PN7462AU”. The EEPROM binary is also updated by using primary downloader functionality (see chapter 6.8).

USB drivers are needed for NFC Cockpit are part of the installation package and are automatically installed.

4.4 NFC Cockpit getting started

After starting the NFC Cockpit Windows application, the communication link between the PC and the PNEV7462B (via USB interface) is established automatically.

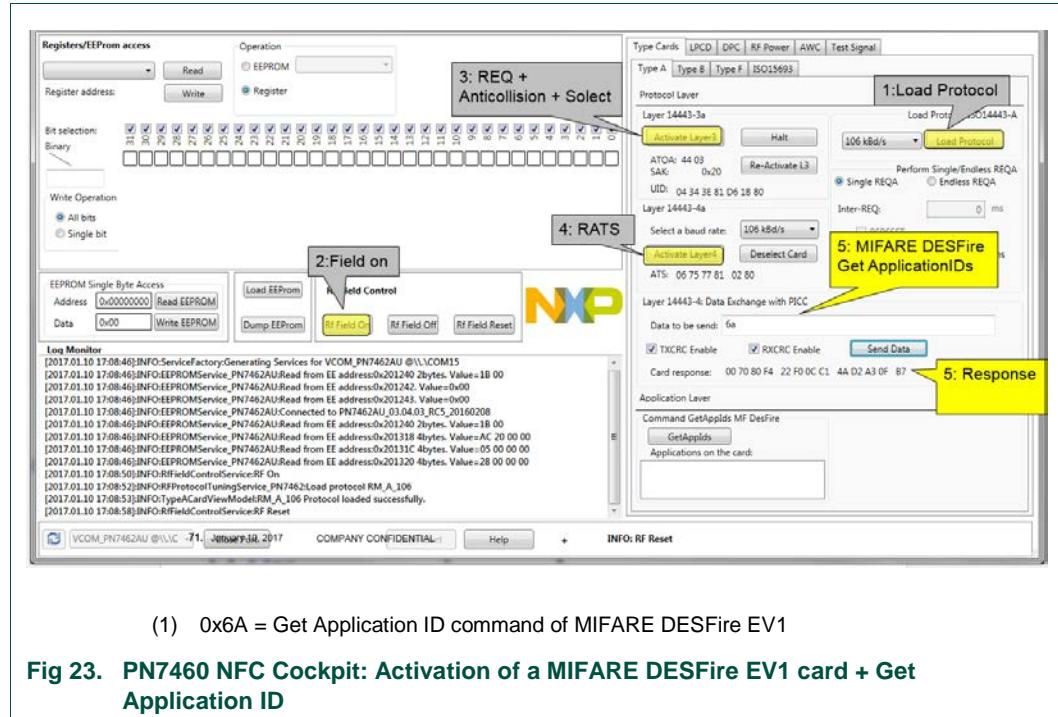
Fig 23 shows the activation of a MIFARE DESFire card with the following steps:

1. click the <Load Protocol> button
2. click the <Field On> button
3. click the <Activate Layer3> button
4. click <Activate Layer4> button

The PN7462 NFC Cockpit shows the card responses like ATQA, SAK, and ATS.

Afterwards the ISO/IEC 14443-4 protocol can be used to exchange data. The Fig 23 shows the MIFARE DESFire command “Get Application ID” (0x6A), which returns the AIDs.

Note: Make sure that either the CRC is enabled or added manually in the data field.



(1) 0x6A = Get Application ID command of MIFARE DESFire EV1

Fig 23. PN7460 NFC Cockpit: Activation of a MIFARE DESFire EV1 card + Get Application ID

Similar functionality exists for ISO/IEC 14443 A and B, for NFC type F and for ISO/IEC 15693 communication.

LOAD_RF_CONFIG command must be executed manually before the corresponding protocol settings are loaded from the EEPROM into the registers. This allows an easy and quick optimization of Tx and Rx parameters before changing the EEPROM. Typical usage scenario is as follows:

- (1) Click the <Load Protocol> button and chose “type A 106”
- (2) Click the <Field On> button
- (3) Click the <Single REQQA> button
- (4) Select a TX register, e.g. RF_CONTROL_TX, enable TX_SET_BYPASS_SC_SHAPING
- (5) Change registers of interest and write back into RAM
- (6) <Single REQQA> shows the register changes (probing the field and checking the envelop)
- (7) Click the <Load Protocol> button (e.g. type A 106)
- (8) Click the <Single REQQA> button (using again the EEPROM settings)

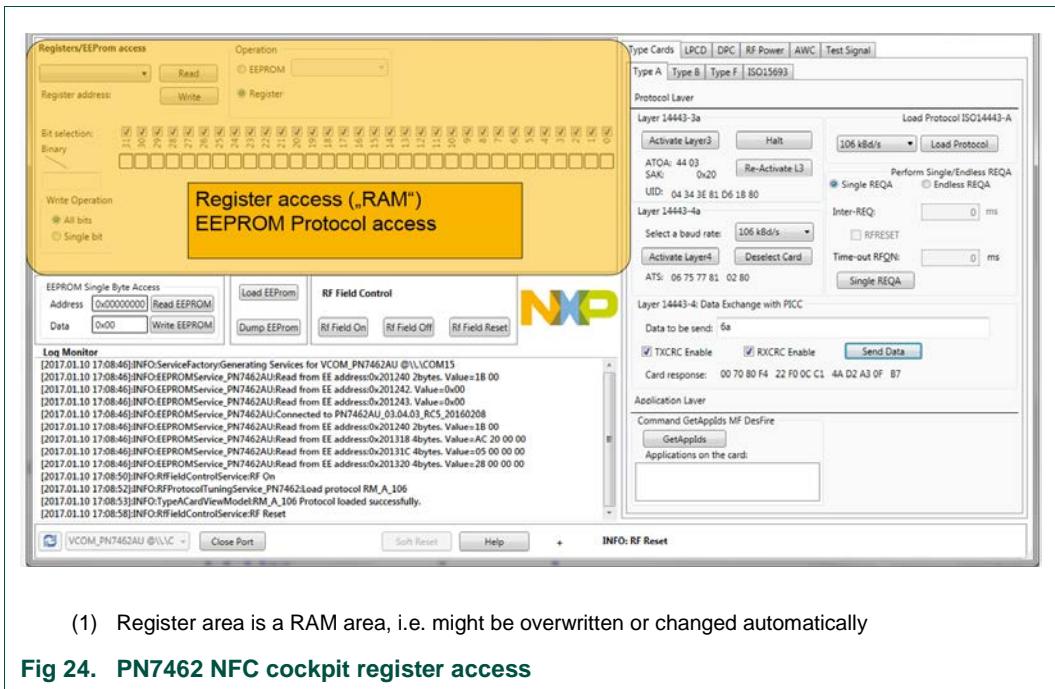
4.5 PN7462AU register access

The NFC Cockpit allows the reading and writing of all the PN7462AU registers (see Fig 24).

Selecting a register reads and shows the hexadecimal value as well as the corresponding bit values. The input allows to change each bit separately as well as writing hexadecimal values. Writing back the value changes the PN7462AU register.

On “mouse over”, the application displays a short description of the register parts..

Note: Some register content cannot be changed manually (“read only”) and some content might be overwritten by the PN7462 firmware.



All registers, which are used in the LOAD_RF_CONFIG command, can be read from the EEPROM. The user must select the register and the protocol.

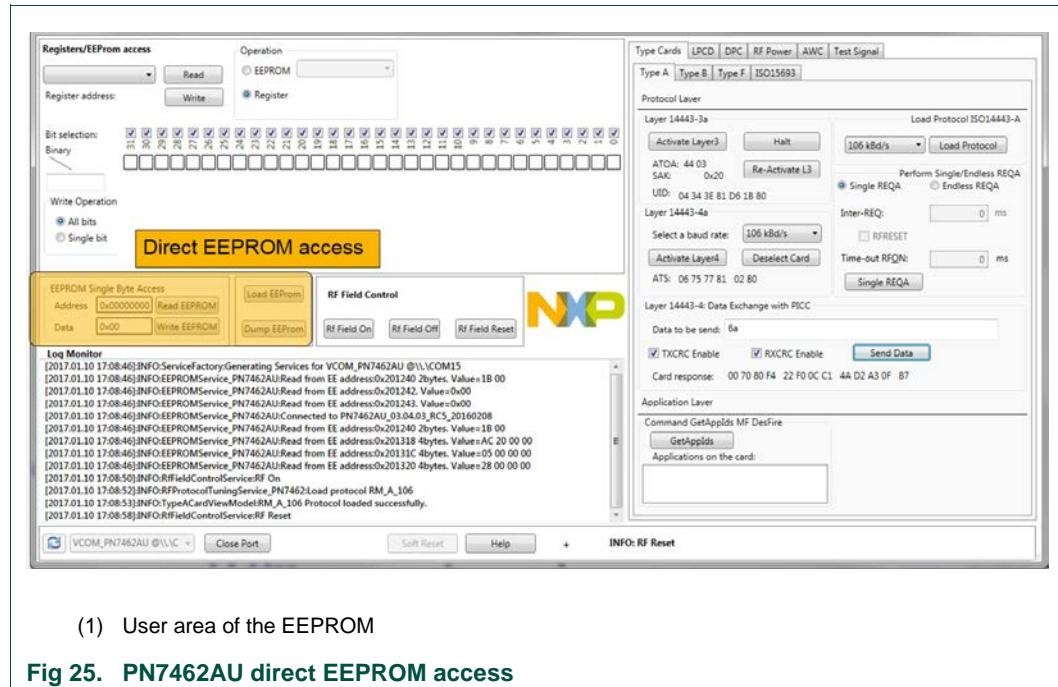
All registers, which are used in the LOAD_RF_CONFIG command, can be written into the EEPROM. The user must select the register and the protocol.

This allows an easy EEPROM update of the relevant Tx and Rx registers after optimization in RAM.

4.6 PN7462AU EEPROM access

The NFC Cockpit allows four options for accessing EEPROM (see Fig 25):

- Read EEPROM - reads a single byte from EEPROM using byte address
- Write EEPROM - writes a single byte into EEPROM using byte address
- Dump EEPROM - stores the complete user area of the PN7462 EEPROM into a binary file. This can be used to generate a backup of all settings or to transfer optimized settings onto another board or into own software.
- Load EEPROM - loads a binary file and stores it into the user area of the PN7462AU EEPROM.



4.7 PN7462AU analog and digital test signals

The NFC cockpit allows to use the PN7462AU internal test bus, to route digital and analog test signals to the given test pins (GPIO1/2 and GPIO4/5), as shown in. All details on the test signals can be found in [3].

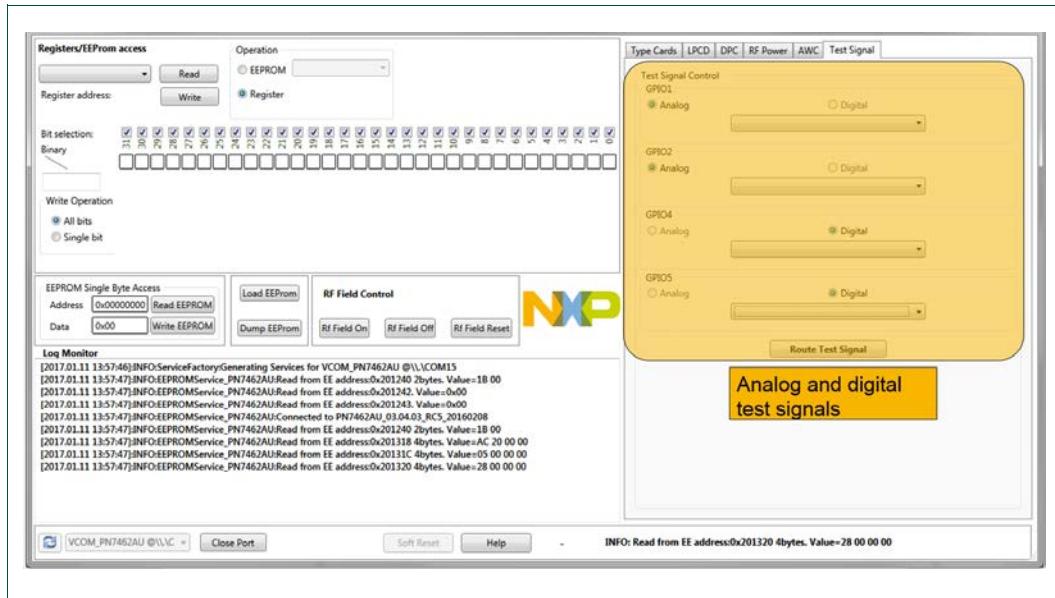


Fig 26. PN7462 analog and digital test signals

The analog test signals can be directly selected at GPIO1 and 2. For the digital test signals GPIO4 and 5 can be used.

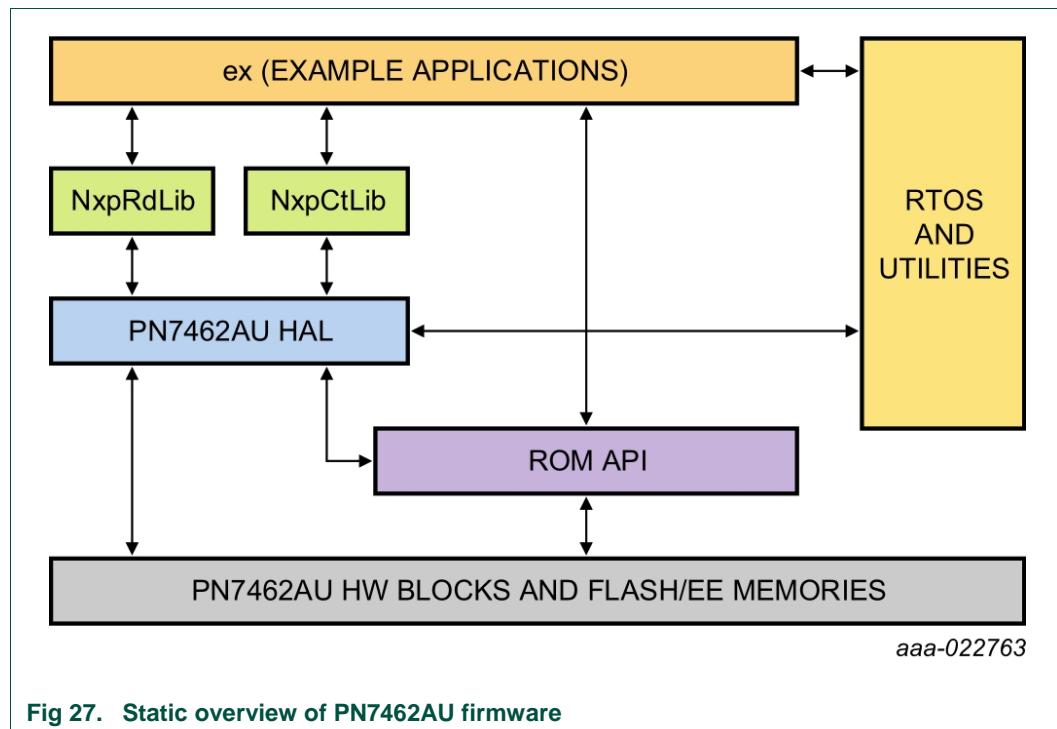
Afterwards, a click on the <Route Test Signal> button activates the chosen signals.

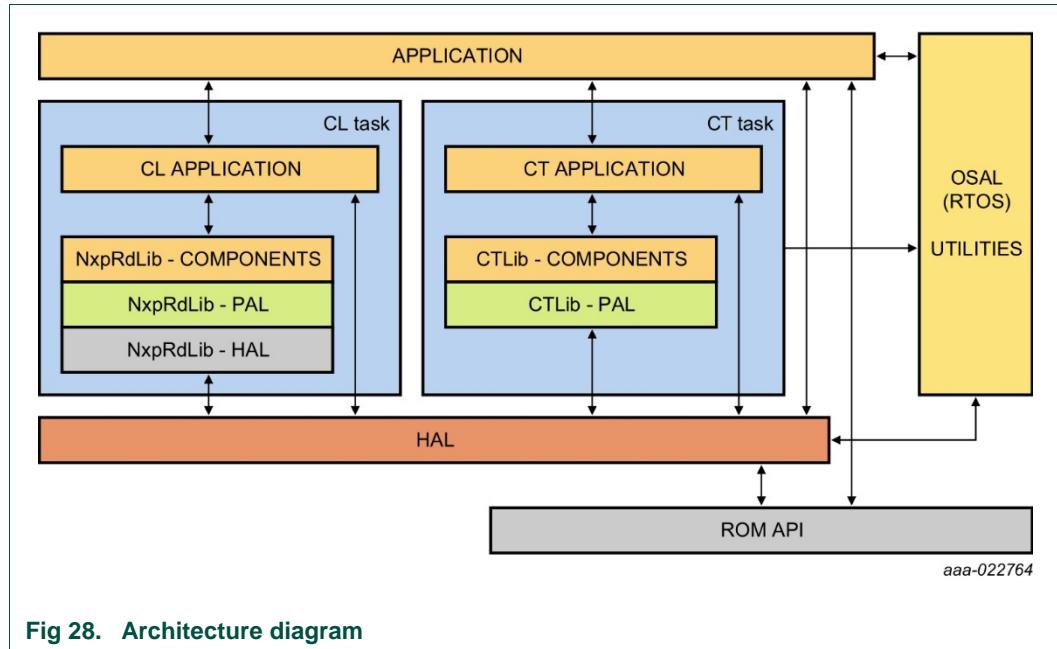
5. Software application stack

The PN7462AU Firmware is a modular software written in C language, which provides an API that enables customers to create their own contact and contactless software stack and applications for the PN7462AU. This API facilitates all operations and commands required in contact and contactless applications such as reading or writing data to cards or tags, exchanging data with other NFC-enabled devices or allowing NFC reader ICs to emulate cards as well.

The PN7462AU software application stack consists of 4 main layers.

- Application & example layer
- Protocol abstraction layer – PAL
- Hardware abstraction layer – HAL
- OSAL (FreeRTOS) and utilities layer



**Fig 28. Architecture diagram**

5.1 Hardware abstraction layer – HAL

Hardware abstraction layer – HAL is responsible for the CPU, communication, memory and utility peripherals. HAL composed of a set of HW functions, HW ISR and OSAL functions.

The HW functions can further be divided to:

1. Atomic functions: functions configuring the HW, but don't result in any event from the HW, EEPROM, Flash, CRC, RNG, PMU/ PCR.
2. Blocking functions: functions configuring the HW and wait till one or more expected events occurs from the HW. CLIF HAL, CT HAL, I2CM/ SPIM HAL
3. Non-blocking functions: functions configuring the HW and expect one or more events, but don't wait till it occurs. The events are notified to the caller of the function. Timer, Host interface.

The HW ISR handles HW events (interrupts) and signals of the blocking functions or notifies non-blocking functions. The HW ISR also handles time critical HW configuration or functions.

5.2 Protocol abstraction layer – PAL

Protocol abstraction layer – PAL implement HW independent communication protocols for contactless and contact interface and it is composed of two libraries.

NxpNfcRdLib library implement contactless protocol and application components. Followed ISO/IEC contactless standards protocols are available:

- **ISO14443-3A**: Contactless proximity card air interface communication at 13.56MHz for the Type A and Jewel contactless cards.

- **ISO14443-3B:** Contactless proximity card air interface communication at 13.56MHz for the Type B contactless cards.
- **ISO14443-4:** Specifies a half-duplex block transmission protocol featuring the special needs of a contactless environment and defines the activation and deactivation sequence of the protocol.
- **ISO14443-4A:** Transmission protocol for Type A contactless cards.
- **MIFARE (R):** Contains support for MIFARE authentication and data exchange.
- **ISO15693:** Contactless protocol for vicinity RFID. It operates on 13.56MHz and uses magnetic coupling between the reader and transponder.
- **ISO18000-3M3:** Contactless protocol for vicinity RFID. It is especially suited for applications where reliable identification and high anti-collision rates are required.
- **FeliCa (JIS: X6319):** Contactless RFID smart card system from Sony.
- **ISO/IEC 18092:** NFC Interface and Protocol standard that enables NFC Data Exchange protocol.

The contact protocol library implement the components for the contactless protocol, such as EMV ATR Parser, T=0 protocol, T=1 protocol. This library also handles the timing compliance violations.

5.3 Application layer – AL

In the application layer customer applications, shall be implemented and can directly use HAL APIs or APIs from the PAL libraries.

The contactless example (or application) is either NFC Forum Polling Loop or EMV Polling Loop that branches to dedicated examples depending on the card detected such as MIFARE Classic, MIFARE UL, MIFARE DF, EMV Paypass transactions (PPSE). There exists a compile time macro phExMain_Cfg.h to decide whether the example is NFC Forum or EMV Polling Loop.

The contact example (or application) is an EMV contact (PPSE application on JCOP card) application that uses the T=1 protocol and the ATR processing of the protocol library.

5.4 OSAL and utilities layer

The OSAL and Utilities layer is used to abstract FreeRTOS messages, to handle events, signals and messages between HW functions and to handle HW ISR.

Utilities layer includes a set of utilities which are grouped and encapsulated together in an independent set of functions. Utilities components provide an interface for protocol libraries to use HAL APIs such as CRC, RNG etc.

Note:

Detailed description how to use OSAL and utilities layer refer to the CHM help file.

5.5 Component view

5.5.1 Contactless component view

In contactless component view (Fig 29) for the “phExMain” example is shown.

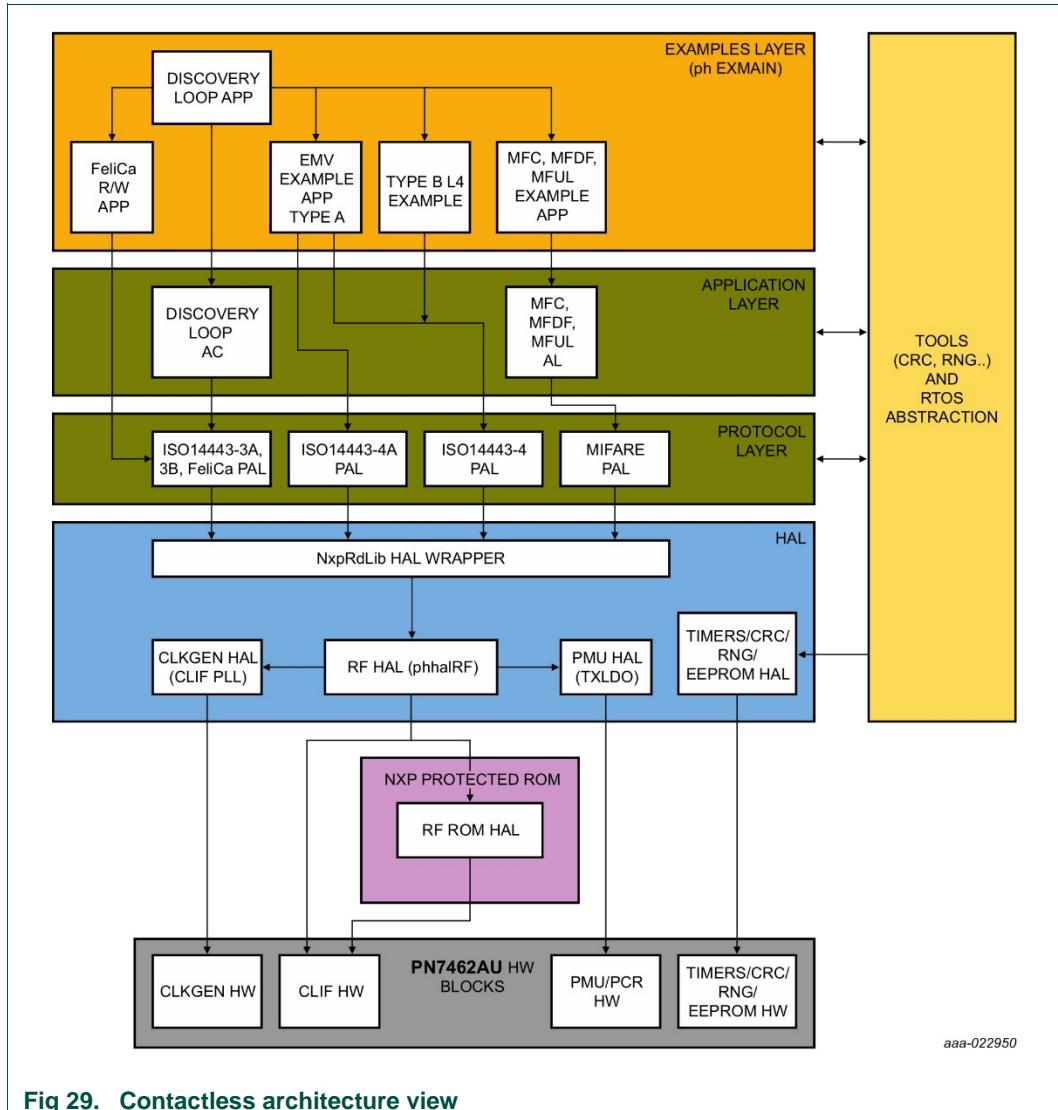


Fig 29. Contactless architecture view

5.5.2 Contact component view

In the Fig 30 contact component view for the “phExMain” example is shown.

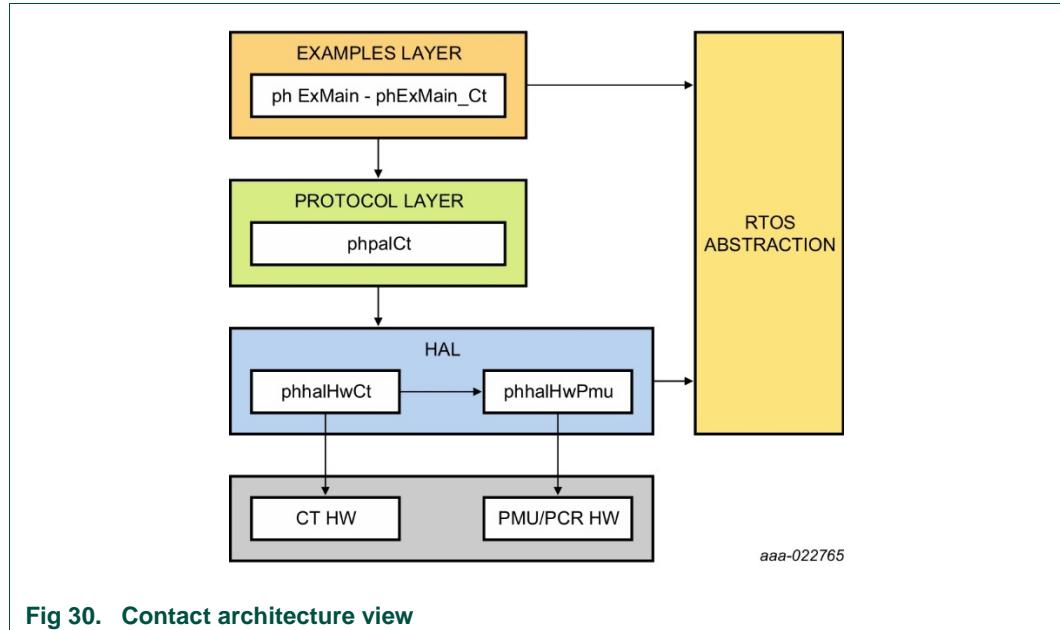


Fig 30. Contact architecture view

5.6 Building a project from bottom to top

In order to use the PN7462AU firmware, a stack of components has to be initialized from bottom to top. Every component in the software stack has to be initialized before it can be used. The referred initialization of each layer generates a data context which feeds the immediate upper layer. Some of the components may need a data context coming from the same layer to be used as an entry point.

The Fig 31 illustrates the mentioned implementation for the initialization procedure of a “phExtMain” application.

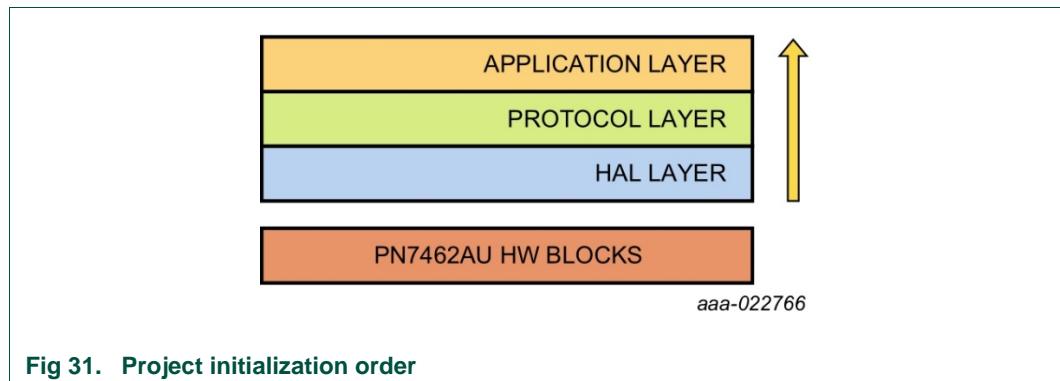


Fig 31. Project initialization order

5.7 RTOS and it's usage

The PN7462AU FW is using FreeRTOS. The port.c file in the OpenRTOS source is modified to support disabling/enabling of scheduler (SysTick timer) and context switch (PendSV) during FW critical sections. The Cortex-M0 port is already available from FreeRTOS.

The FreeRTOS provides flexibility to develop multi-application environment. It provides the creation of multiple tasks. The FreeRTOS will handle multiple tasks with its scheduler. It is also possible to prioritize the tasks according to our requirement.

The FreeRTOS provides the message queues which are used to communicate between the tasks. The tasks can wait for the messages and if not available scheduler suspends these tasks which are waiting, and allow the other tasks to run.

The FreeRTOS provides the events which are used to communicate inside the tasks.

The tasks can go to suspended state waiting for the events as well. Whenever the events occur the scheduler wakes up that particular task and allows it to run.

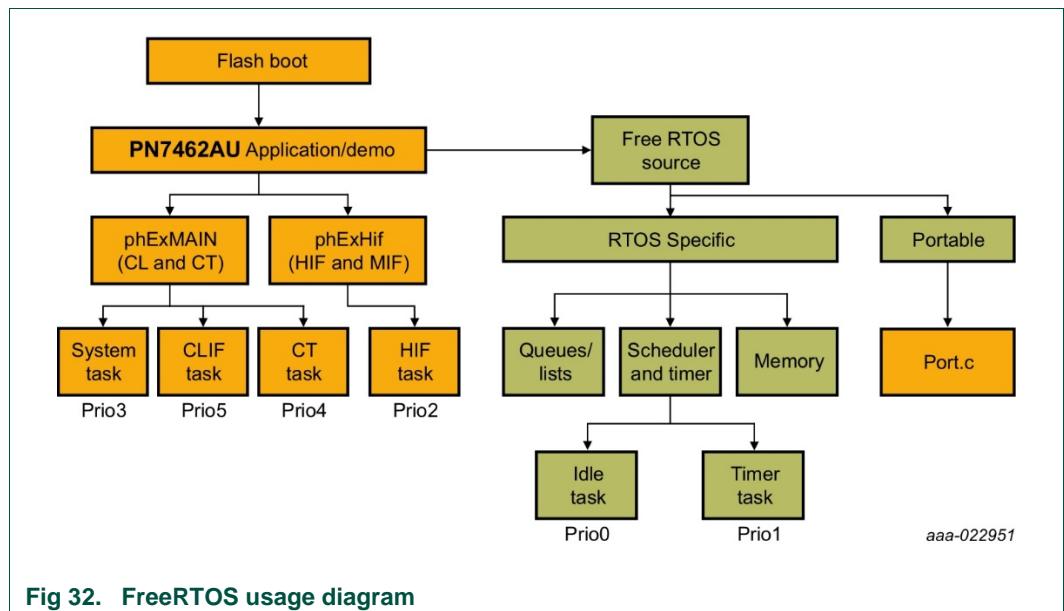
For more information on FreeRTOS please refer the following link
<http://www.freertos.org/>

The Fig 32 FreeRTOS Usage (below) provides the structure of FreeRTOS and its relation to PN7462AU FW Application.

The Flash boot performs the boot reason handling and initialization of common HALs.

See Below are the lists of examples available in current release to demonstrate the HW and FW features of PN7462AU IC.

In general, the FreeRTOS Scheduler has 2 default tasks running which are Idle task and Timer task whose priority is kept lower than the application tasks.



6. Managing the PN7462AU SW projects with MCUXpresso IDE

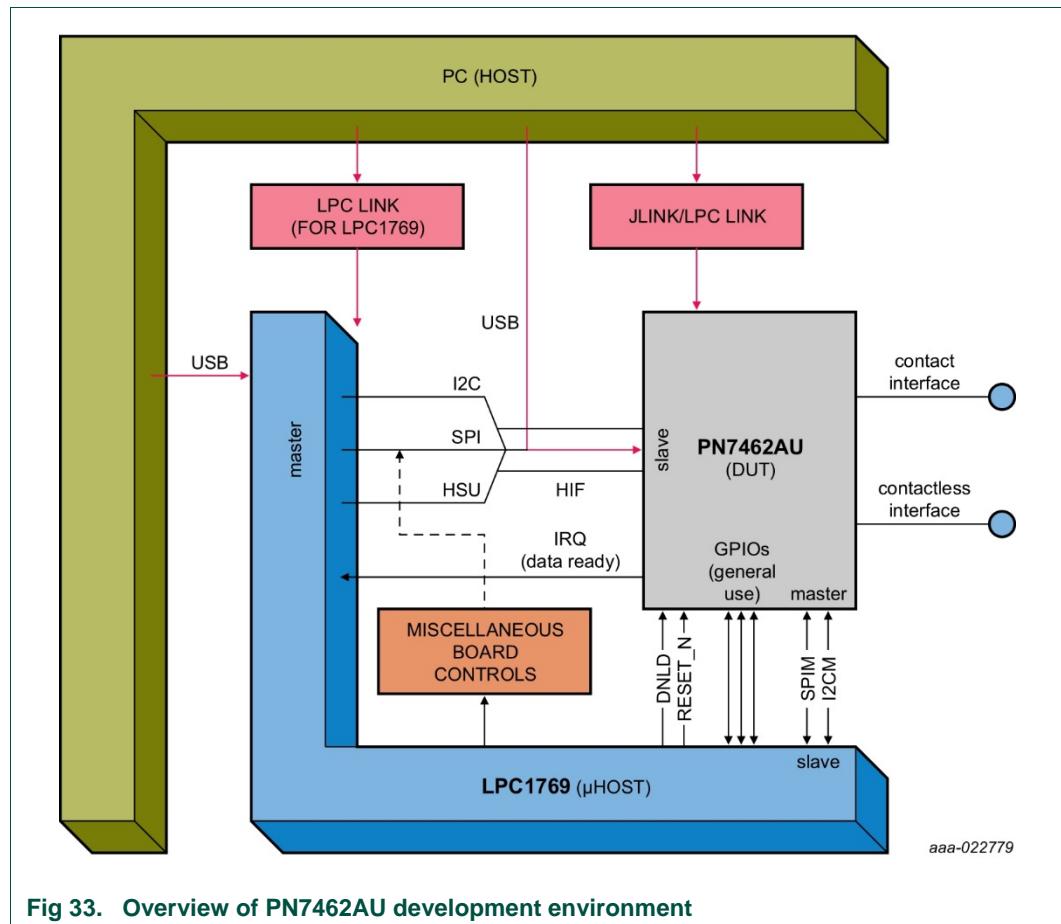
6.1 Development environment

For developing PN7462AU firmware and customer applications all components listed in the Table 4 are required.

Table 4. Development environment

Item	Version	Purpose
PN7462AU Customer board	2.1/2.2	Engineering development board
LPC-Link 2	1.0	Standalone debug adaptor
MCUXpresso IDE	>10.0.2	Development IDE
PN7462AU FW and SW examples	4.06.00	Installer package

Fig 33 gives general overview of the development environment elements and their interconnections:



6.2 Installation of the MCUXpresso IDE

The MCUXpresso IDE enables powerful application development for NXP MCUs based on ARM® Cortex®-M cores, including LPC and Kinetis microcontrollers. The MCUXpresso IDE offers advanced editing, compiling and debugging features with the addition of MCU-specific debugging views, code trace and profiling, multicore debugging, and more. Feature-rich IDE optimized for ease-of-use, based on industry standard Eclipse and GCC providing a powerful application development environment, Supports Freedom, Tower, LPCXpresso and your custom development boards with debug probes from NXP, P&E, and SEGGER. Available in full-featured free (code size unlimited) and affordable professional editions (including MCUXpresso IDE email support and advanced trace features).

This tool can freely be downloaded from the MCUXpresso website [1]. Before one can download the software, it is necessary to create an account. Creating an account is absolutely free.

If a Pro Edition activation code as not been installed, then MCUXpresso IDE will start as a Free Edition. There is no Activation process required to use the MCUXpresso IDE Free Edition. There are also no restrictions in code generation size or binary programming size. However, some advanced debug features will not be available.

The installation starts after double-clicking the installer file.

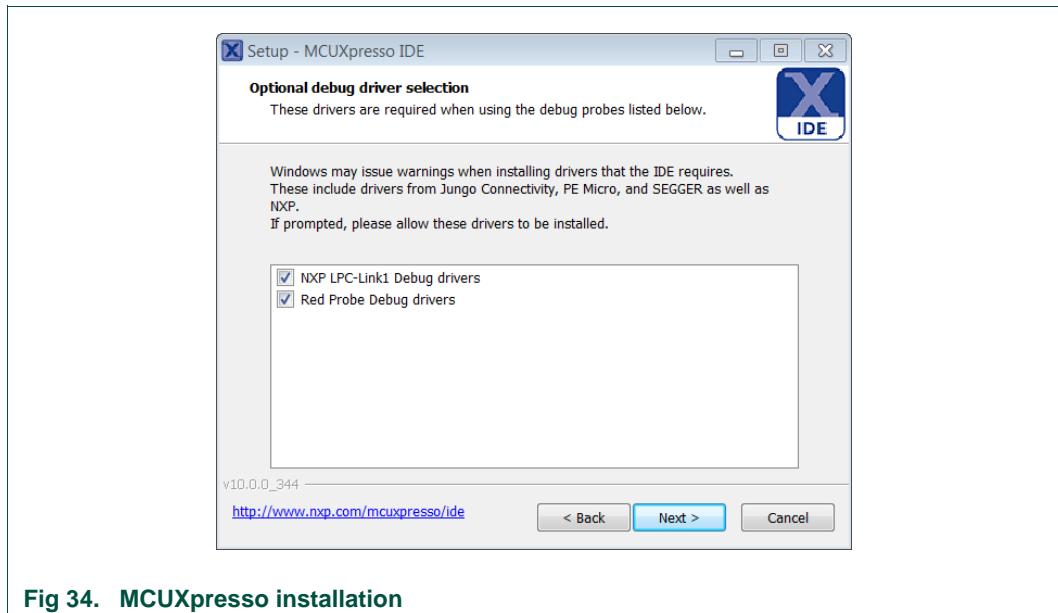


Fig 34. MCUXpresso installation

Make sure, the checkbox for installing the NXP debug drivers is activated.

During the installation, the user will be asked to install additional drivers (SEGGER JLink, P&E). This installation shall be accepted.

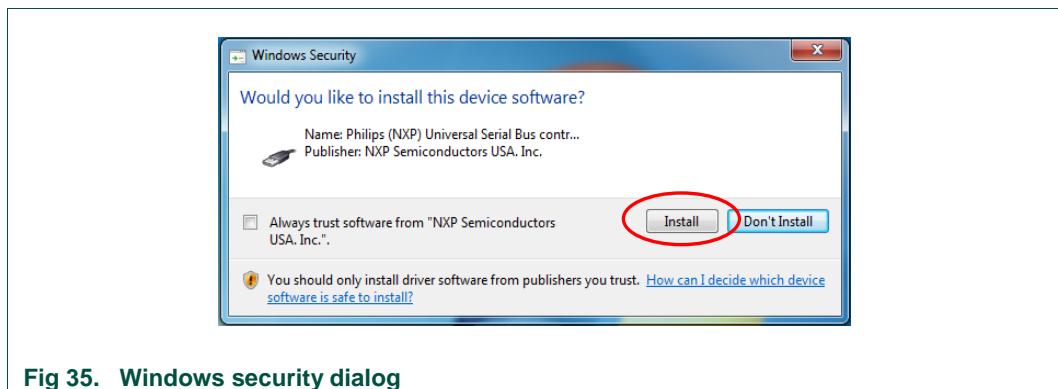


Fig 35. Windows security dialog

After the setup wizard, has finished, the newly installed IDE can be launched.

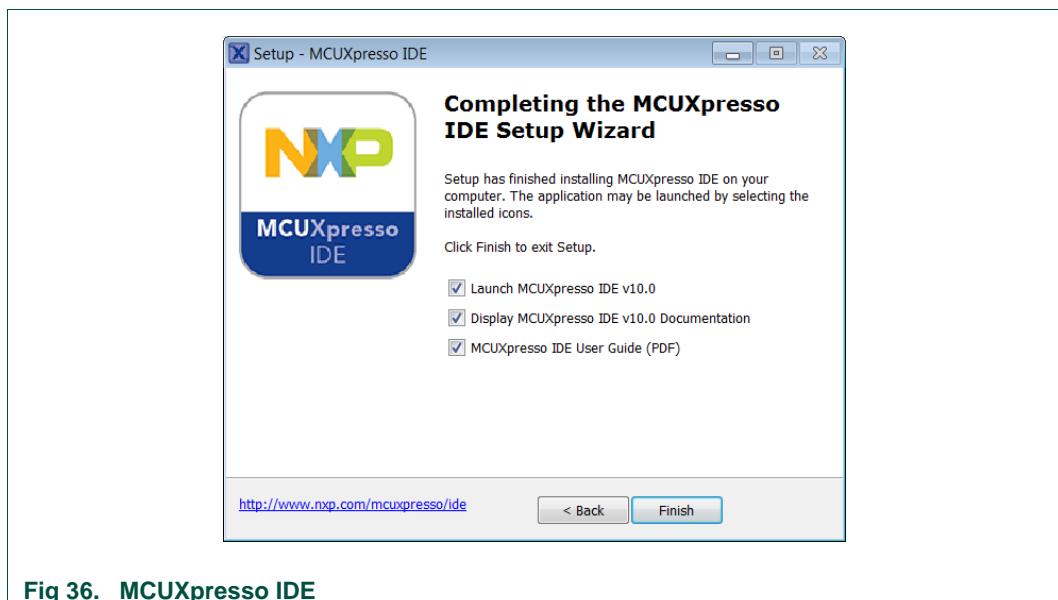


Fig 36. MCUXpresso IDE

Note: With MCUXpresso version prior to 10.0.2 PN7462 plugin is needed.

6.3 Importing provided SW example projects

The use of Quickstart Panel provides fast access to the most commonly used features of the MCUXpresso IDE. Quickstart Panel eases importing, creating, building and debugging projects.

FW and SW examples are provided in archive file and are part of the "PN7462AU Product Support Package" PSP, this package is available on the PN7462AU product page. It is assumed that examples are installed on development PC.

Project import consists of following steps:

- Start the MCUXpresso IDE and select new workspace
- Select the option "Import project(s)" (see picture below)
- Browse to the software package .zip archive

- MCUXpresso unzips the software package
- The software package is ready for use

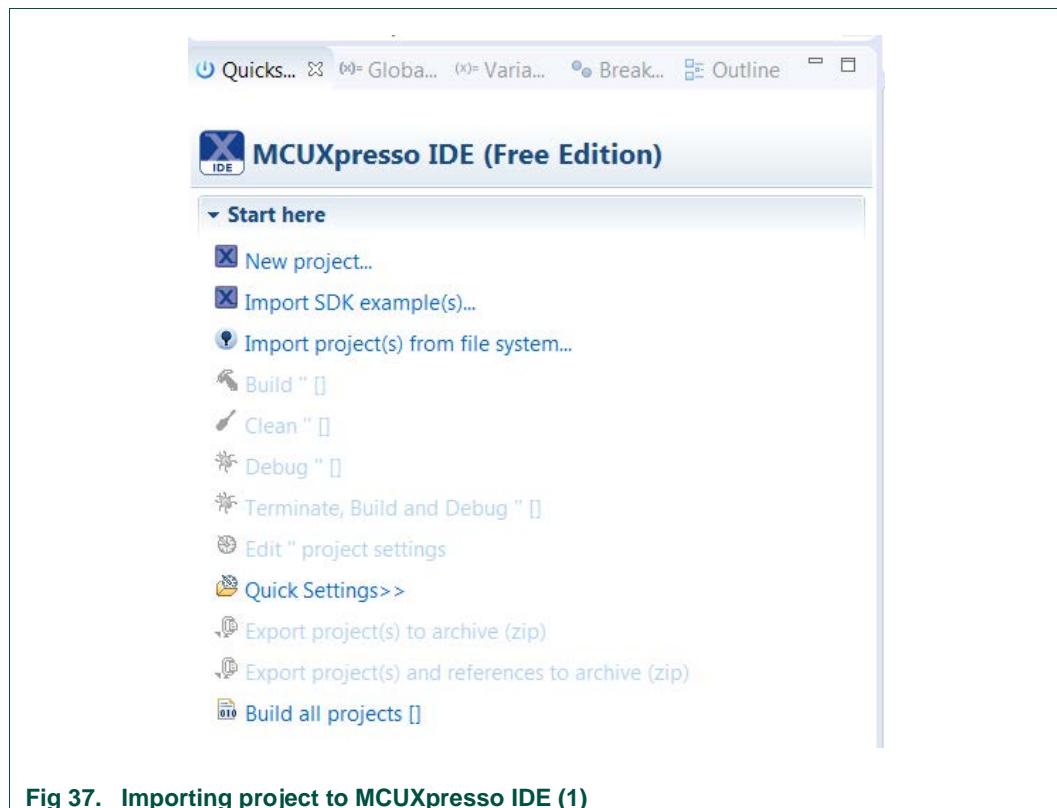


Fig 37. Importing project to MCUXpresso IDE (1)

In the “Quickstart Panel” window, click on Import project(s) from file system...

The dialog for importing projects opens.

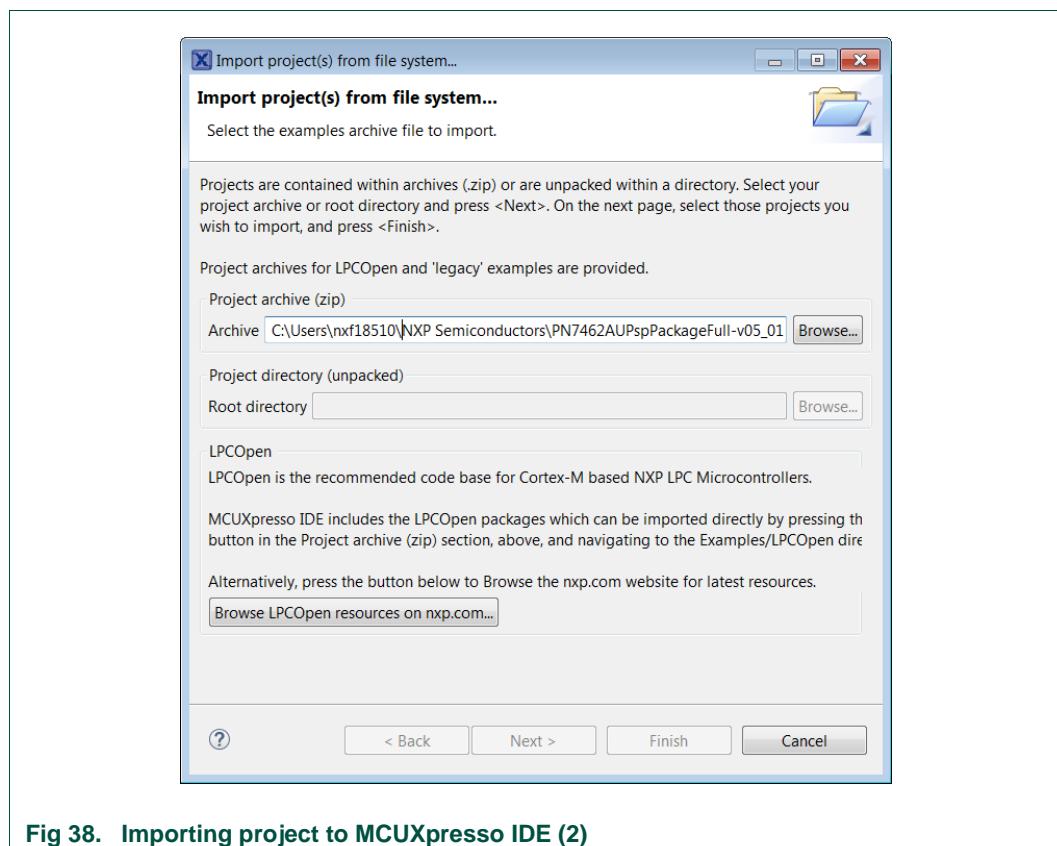


Fig 38. Importing project to MCUXpresso IDE (2)

Browse to the project zip file *PN7462AU-FW_v05.01.00_Full.zip* and click “Next”.

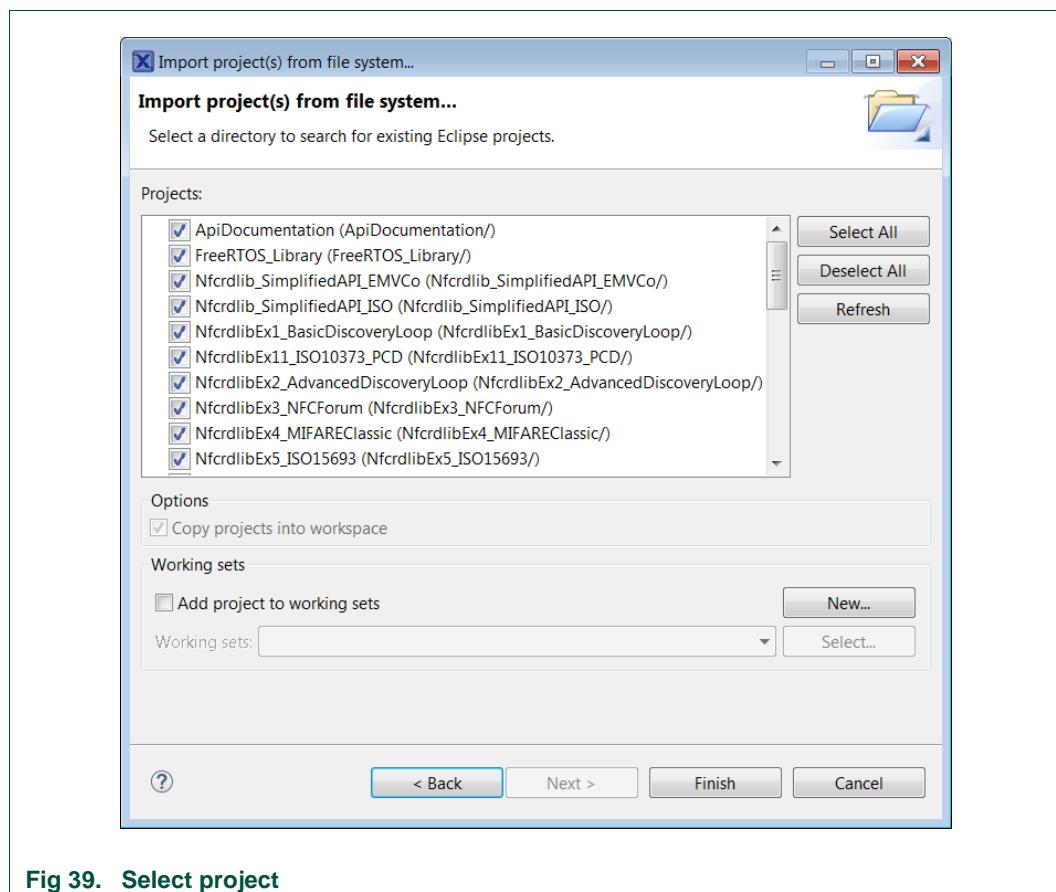


Fig 39. Select project

Select projects to be imported and then click “Finish”. Selected examples will be imported to the workspace.

When the import process is finished, the development and editing the code can start.

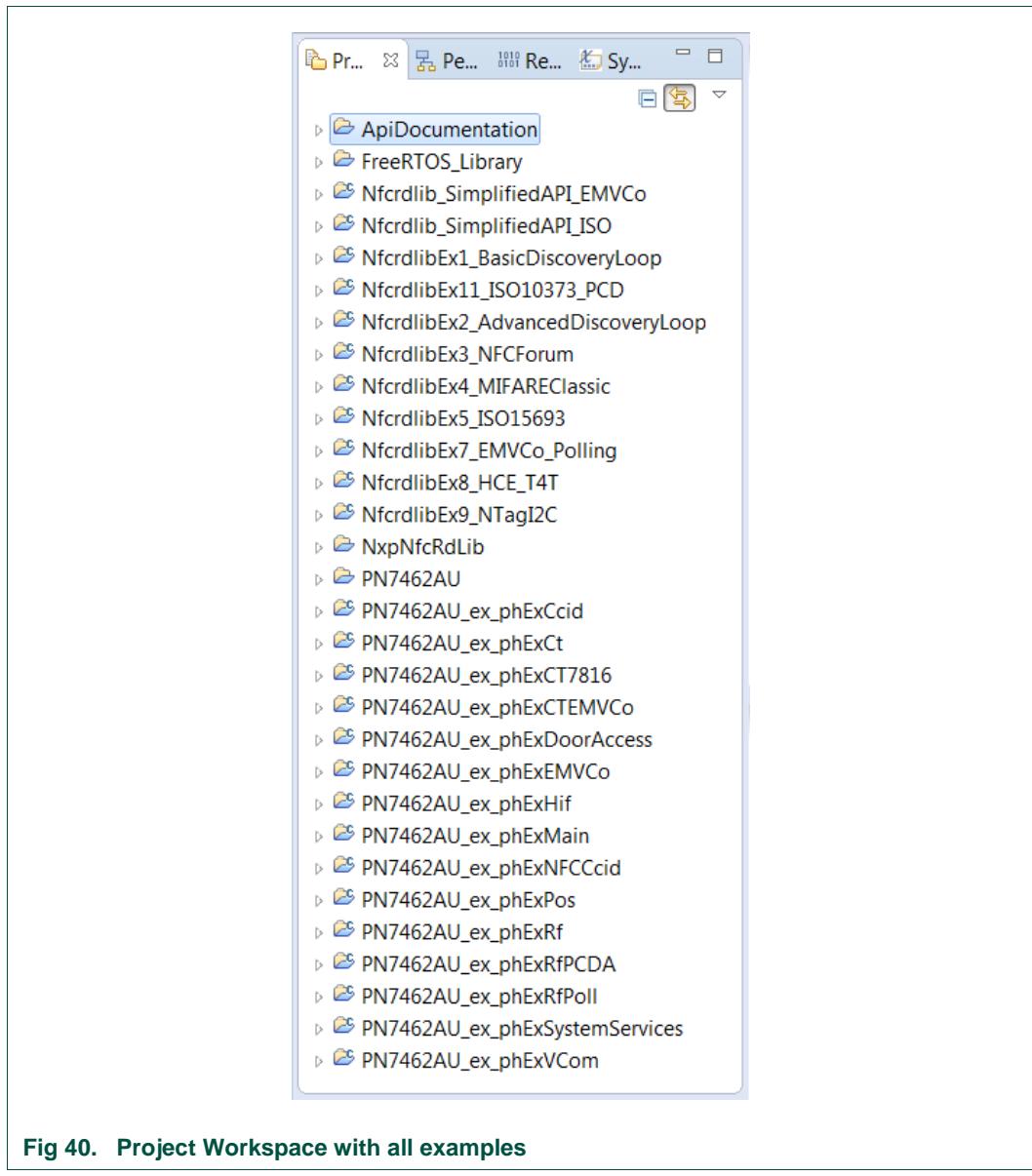
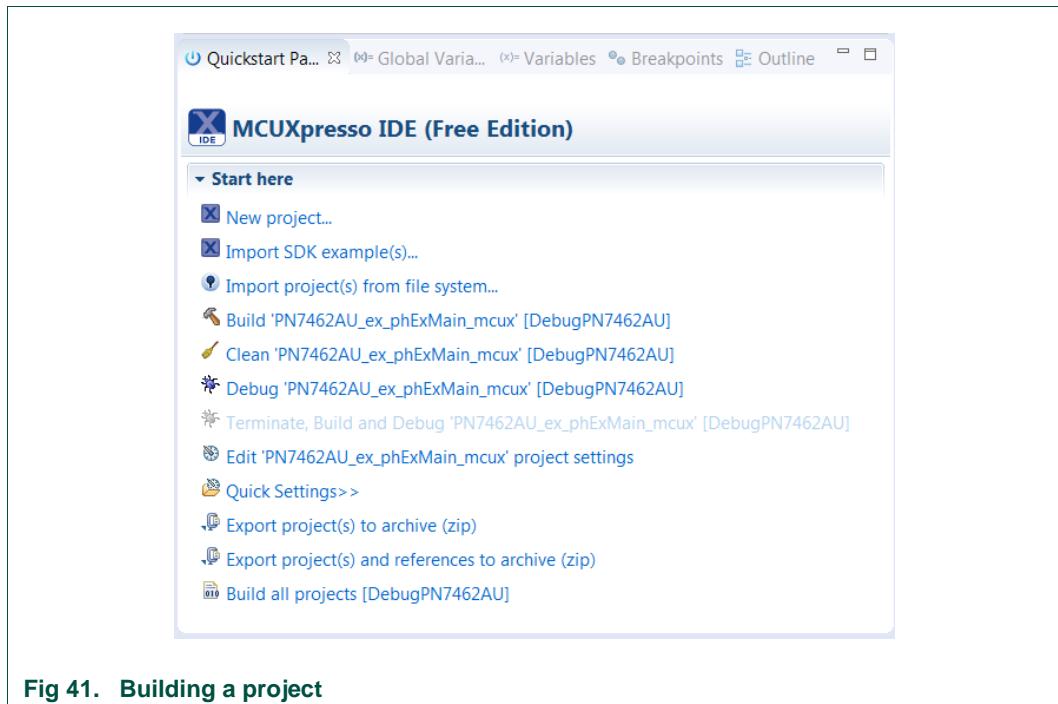


Fig 40. Project Workspace with all examples

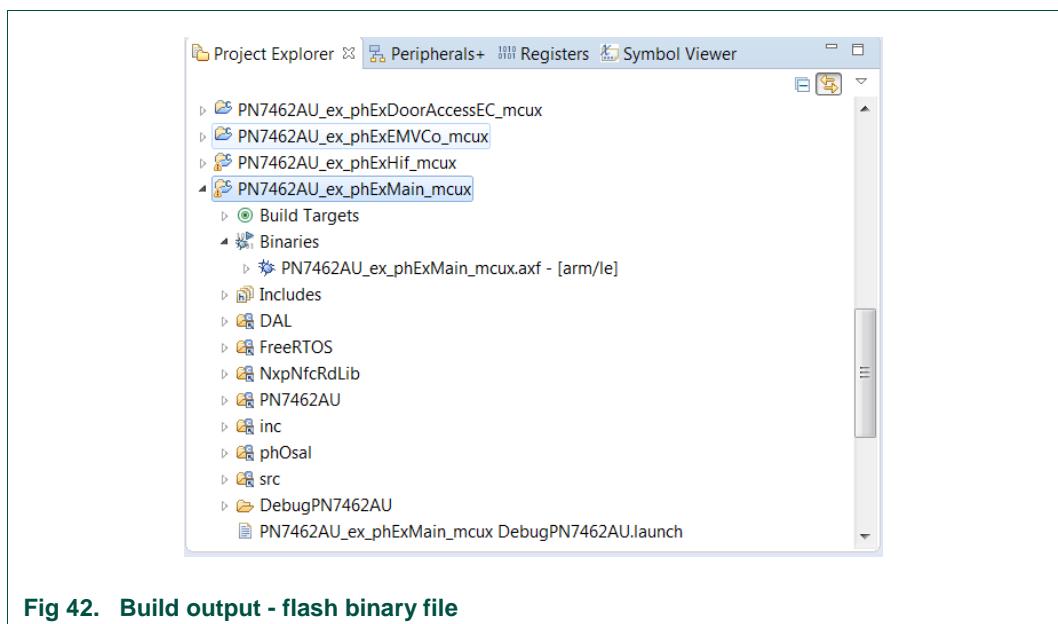
6.4 Building projects

Building projects in a workspace can be started through Quickstart Panel - 'Build all projects' command. Alternatively, a single project can be selected in the "Project Explorer View" and built separately. Note that building a single project may also start a build of any associated library projects.

The project can be built as shown in the Fig 41.

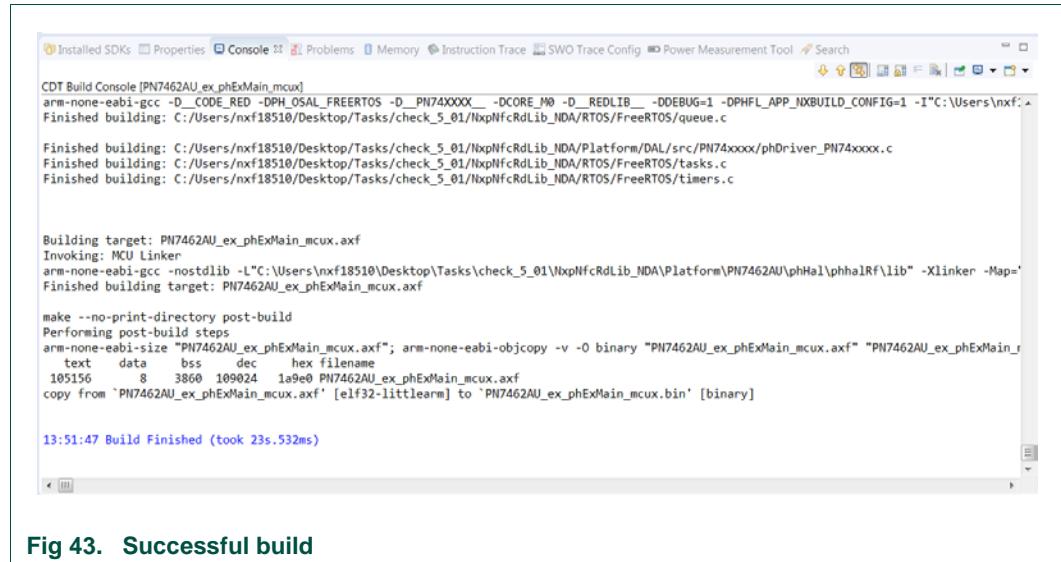


As a part of the build process, the binary file for Flash is created. This binary file can be used to update PN7462AU Flash via USB mass storage interface or by using Flash tool or debug in MCUXpresso IDE. In case that “Binaries” folder is not visible in the project structure, refresh the project (right click on project and select “Refresh”).



The project settings, compiler and link flags can be changed in the project properties dialog. To open the project properties dialog, select appropriate project in the “Project Explorer View” and click “Edit ‘selected-project’ project settings”.

Build result can be monitored on the build console Successful build Fig 43.



```
CDT Build Console [PN7462AU_ex_phExMain_mcux]
arm-none-eabi-gcc -D_CODE_RED -DPH_OSAL_FREERTOS -D_PN74XXXX -DCORE_M0 -D_REDLIB -DDEBUG=1 -DPHFL_APP_NXBUILD_CONFIG=1 -I"C:\Users\nxfs\source\repos\PN7462AU\Platform\DAL\src\PN74xxxx\phDriver_PN74xxxx.c"
Finished building: C:/Users/nxf18510/Desktop/Tasks/check_5_01/NxpNfcRdLib_NDA/RTOS/FreeRTOS/queue.c
Finished building: C:/Users/nxf18510/Desktop/Tasks/check_5_01/NxpNfcRdLib_NDA/RTOS/FreeRTOS/tasks.c
Finished building: C:/Users/nxf18510/Desktop/Tasks/check_5_01/NxpNfcRdLib_NDA/RTOS/FreeRTOS/timers.c

Building target: PN7462AU_ex_phExMain_mcux.axf
Invoking: MCU Linker
arm-none-eabi-gcc -nostdlib -L"C:/Users/nxf18510/Desktop/Tasks/check_5_01\NxpNfcRdLib_NDA\Platform\PN7462AU\phHal\phHalRF.lib" -Xlinker -Map='
Finished building target: PN7462AU_ex_phExMain_mcux.axf

make --no-print-directory post-build
Performing post-build steps
arm-none-eabi-size "PN7462AU_ex_phExMain_mcux.axf"; arm-none-eabi-objcopy -v -O binary "PN7462AU_ex_phExMain_mcux.axf" "PN7462AU_ex_phExMain_mcux.bin"
      text    data     bss   dec
105156       8   3860 109024 1a9e0 PN7462AU_ex_phExMain_mcux.axf
copy from `PN7462AU_ex_phExMain_mcux.axf' [elf32-littlearm] to `PN7462AU_ex_phExMain_mcux.bin' [binary]

13:51:47 Build Finished (took 23s.532ms)
```

Fig 43. Successful build

6.5 Running and debugging the example projects

This description shows how to run the PN7462AU “PN7462AU_ex_phExMain” example application for the PN7462AU customer development board in debug mode. The same basic principles will apply for all other examples. In cases where example will need additional configuration this will be detailed described in the example description.

The PNEV7462B customer board needs to be connected to the host PC running the MCUXpresso software via LPC-Link 2, as shown in Fig 44.

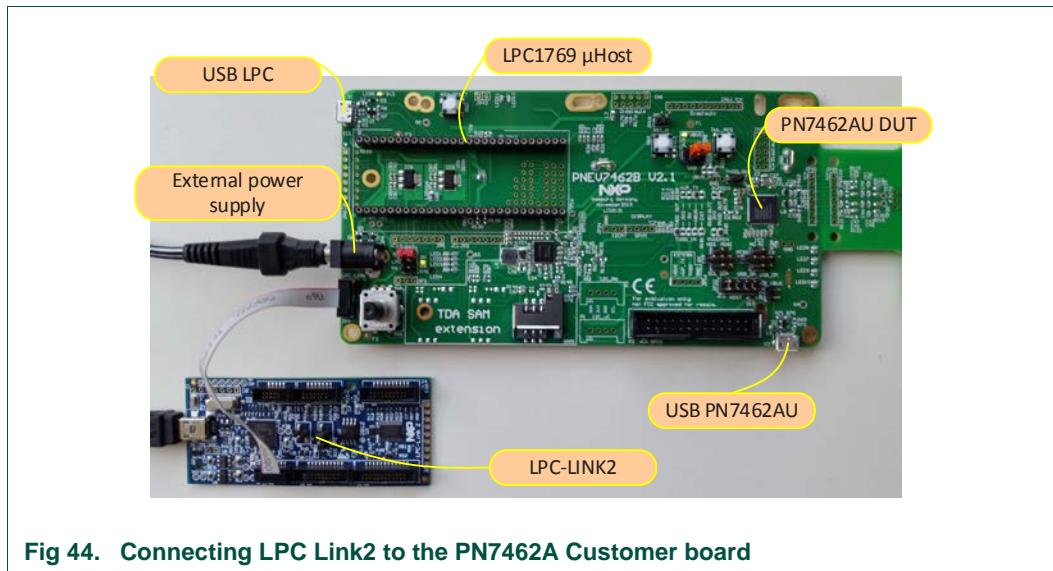


Fig 44. Connecting LPC Link2 to the PN7462A Customer board

When debug is started, the application is automatically downloaded to the target and it's programmed to the FLASH memory; a default breakpoint is set on the first instruction in main (), the application is started (by simulating a processor reset), and code is executed until the default breakpoint is hit.

To start debugging your application on the PN7462AU, simply highlight the project in the Project Explorer and then in the Quick start Panel click Debug, as shown in Fig 45. The MCUXpresso IDE will first build application and then start debugging.

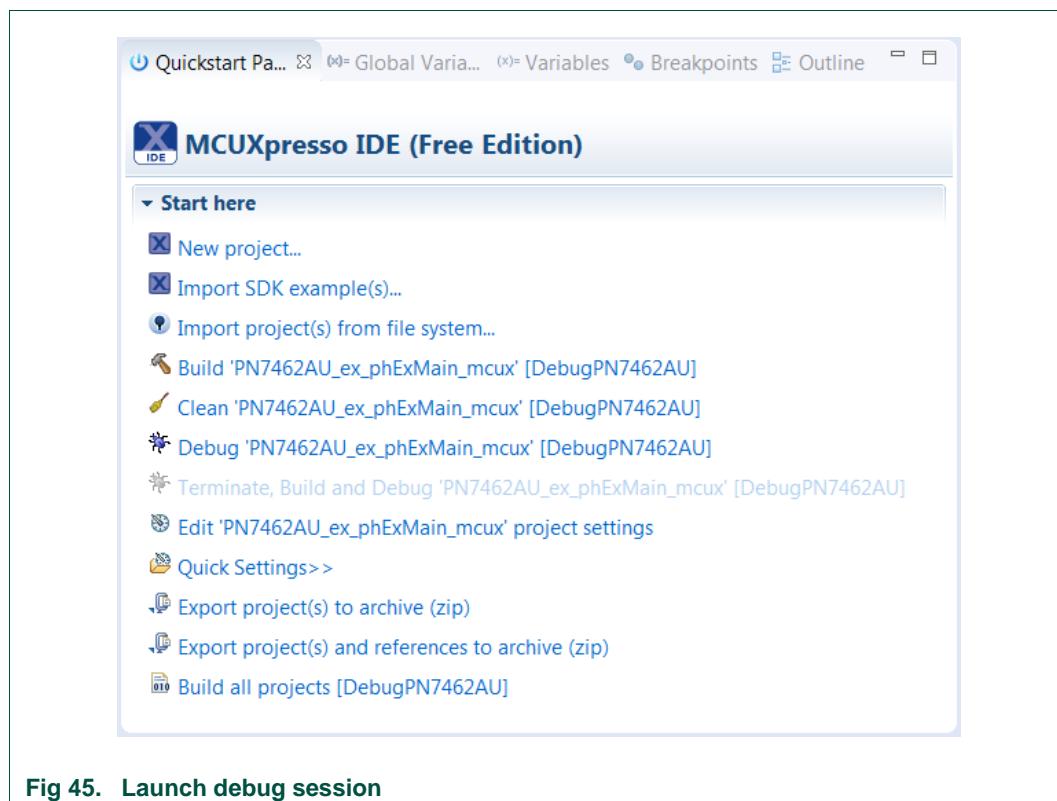


Fig 45. Launch debug session

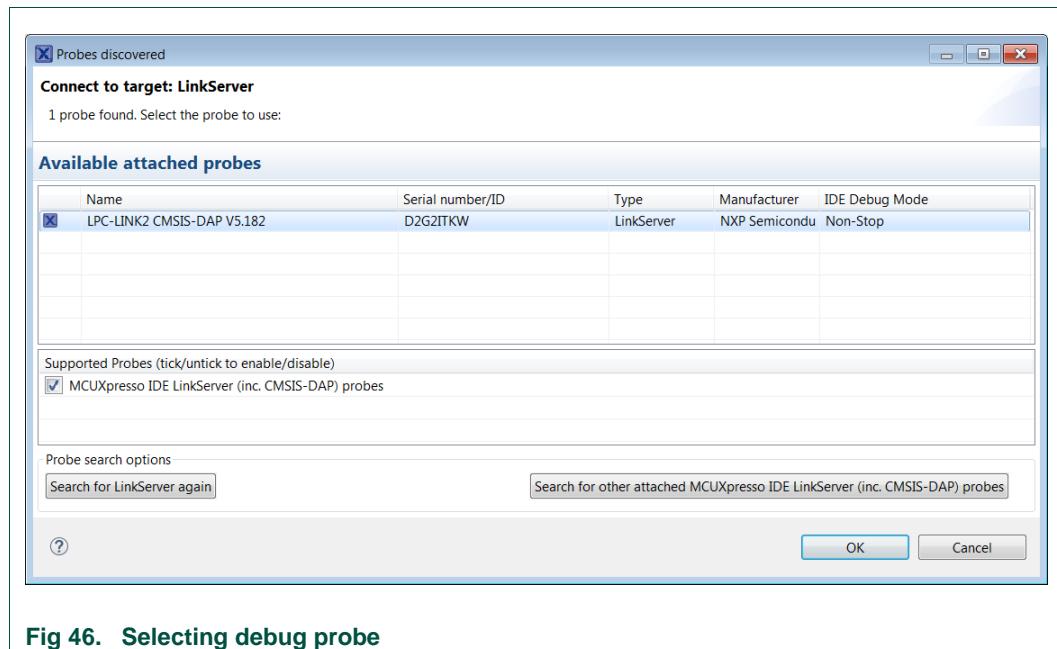


Fig 46. Selecting debug probe

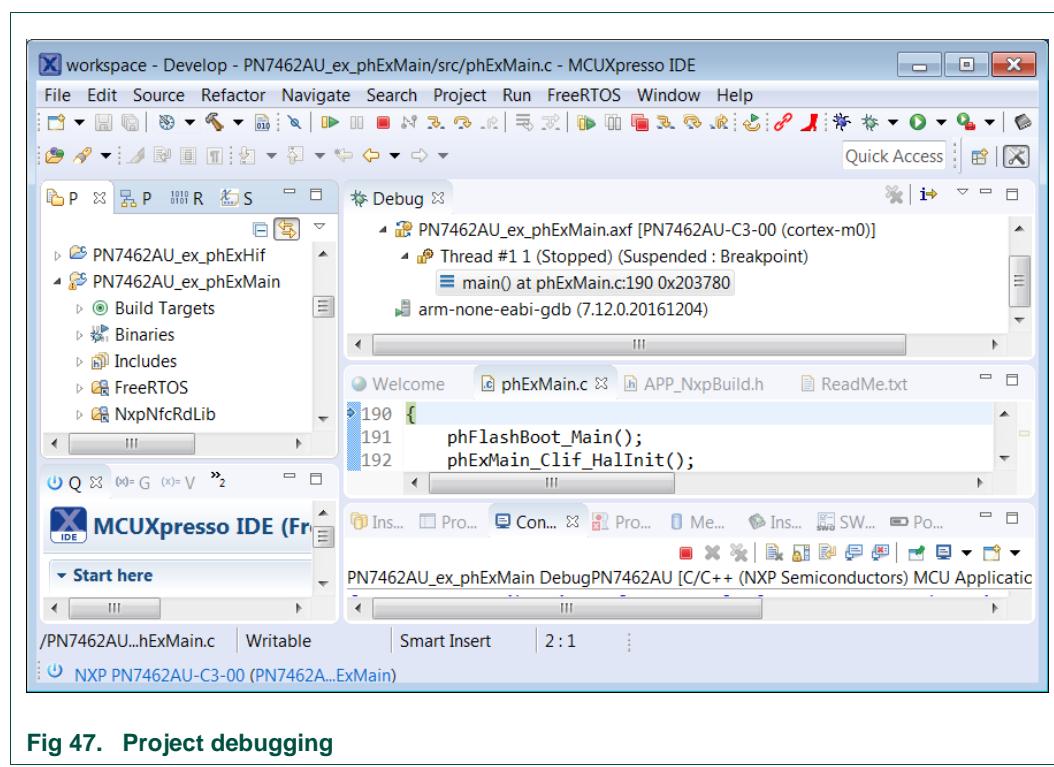
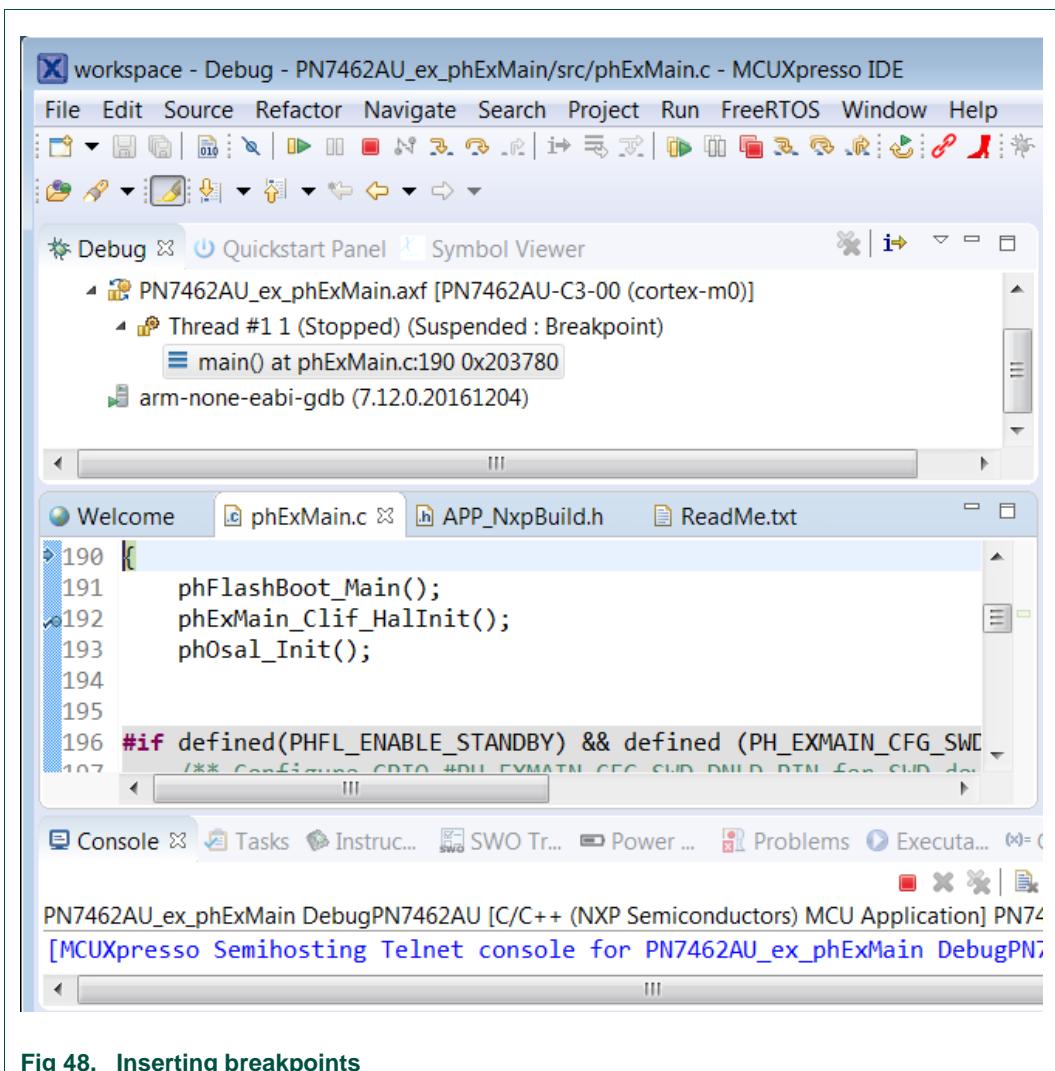


Fig 47. Project debugging

After the software upload, the execution of the application starts immediately.

6.5.1 Break points

PN7462AU supports 4 breakpoints and 2 watch points. In usual way, double click on the left vertical editor strip to set the break points. The execution of the application will be stopped when the break point is reached.



6.5.2 Debug traces

The debug traces can be seen on console as shown in Fig 49.

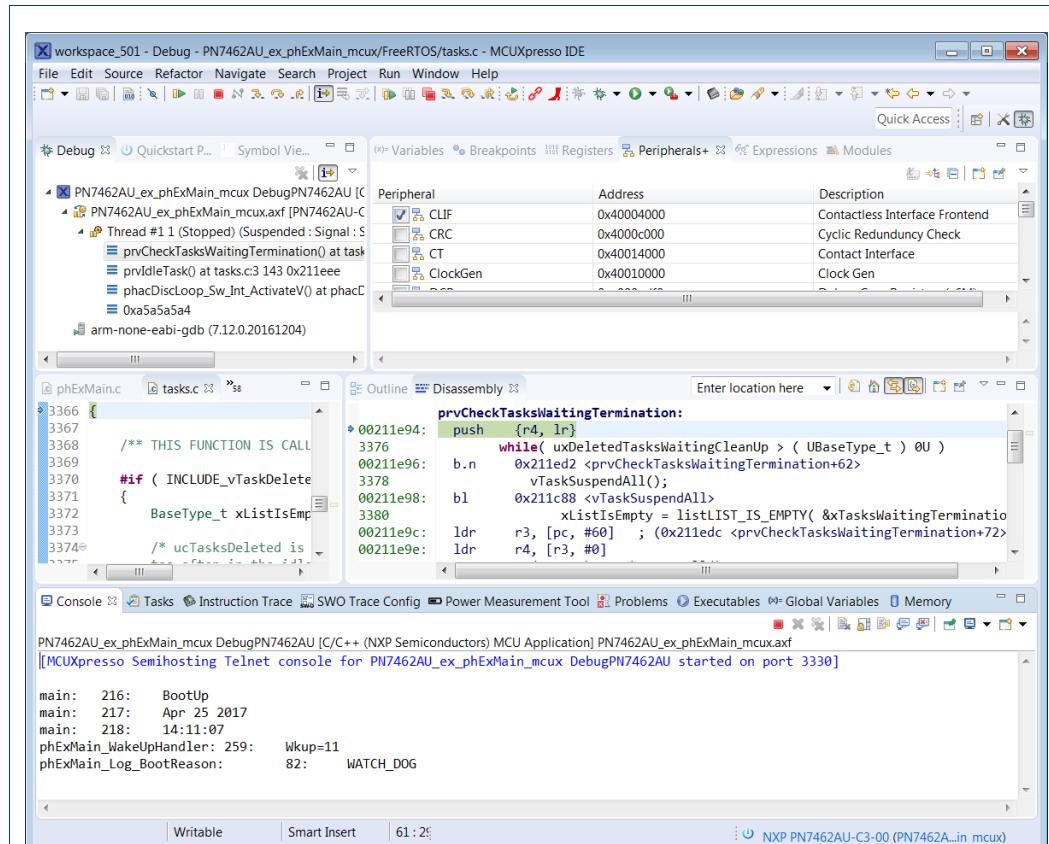


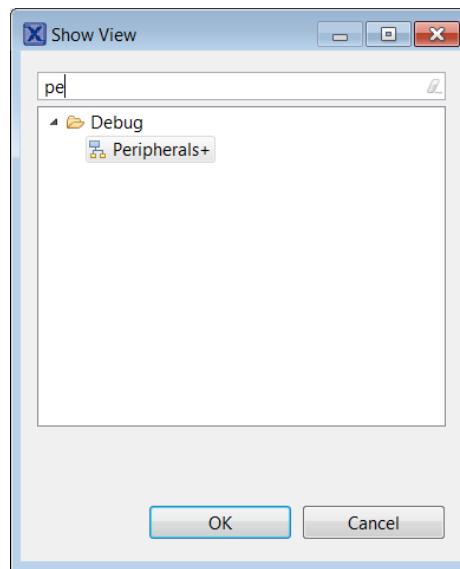
Fig 49. Debug view and debugger traces

6.5.3 Peripheral view

In MCUXpresso IDE we get direct access to all the peripheral registers of the PN7462AU.

As shown below, we can see the fields and description of the EEPROM Controller on the PN7462AU IC.

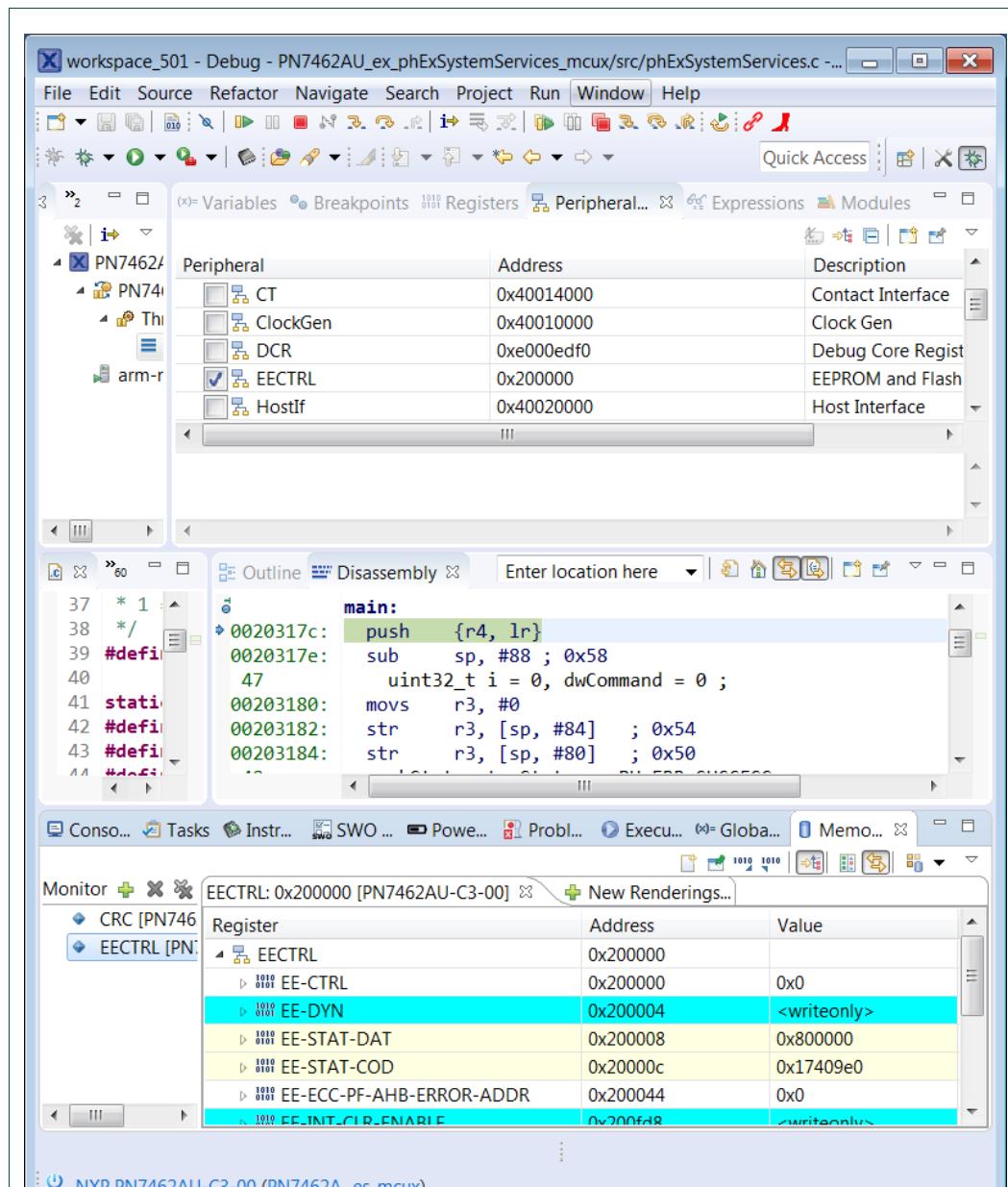
To see the peripheral registers, follow the steps as shown below.



- (1) Go to Window → Show view → Other
- (2) Select "Peripherals+"

Fig 50. Peripheral view

Select the appropriate register or IP to watch or change the register values.



- (1) Select the relevant peripheral
- (2) Register, bit fields and description in the relevant view

Fig 51. PN7462AU EECTRL peripheral view

6.6 Updating Customer Board Firmware (Flash and EEPROM memory)

The customer board firmware is located in the PN7462AU flash memory. PN7462AU flash memory can be updated either Using USB Mass Storage mode (primary downloader) or using SWD interface and LPC-Link 2 debug probe.

6.7 Updating Flash via SWD interface

Ensure that LPC-LINK2 is connected to PN7462AU Fig 52 and follow the steps below.

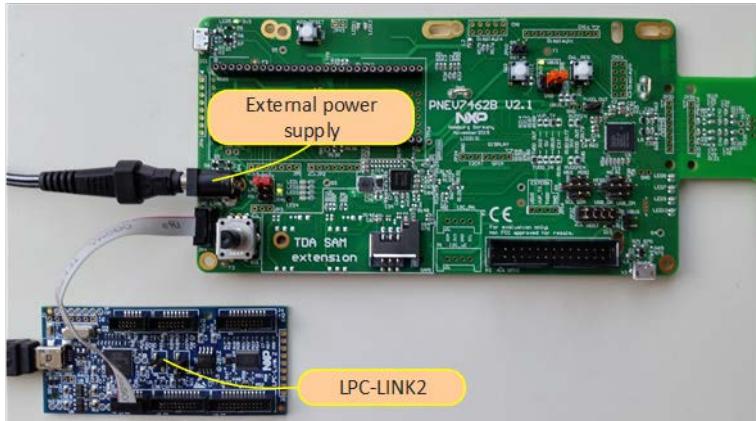


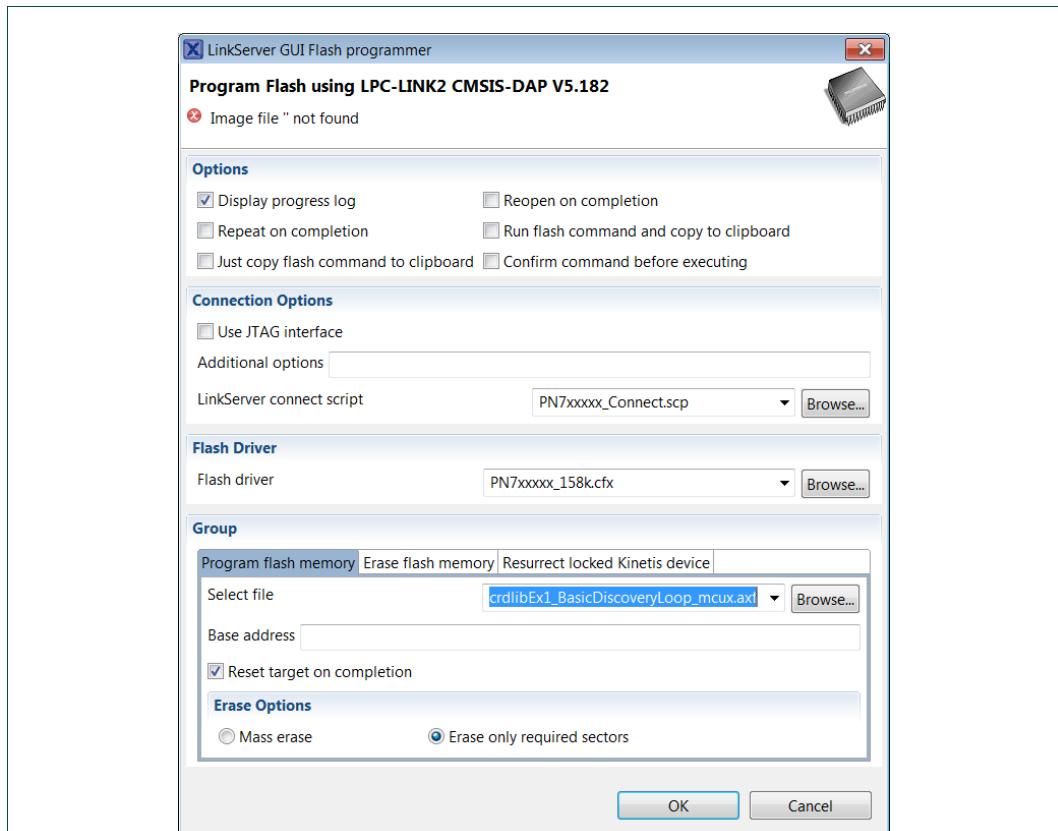
Fig 52. HW setup for the flashing via LPC-Link 2

Click Flash icon on the menu bar to start LinkServer GUI Flash programmer tool:



Fig 53. Flash tool command button in MCUXpresso

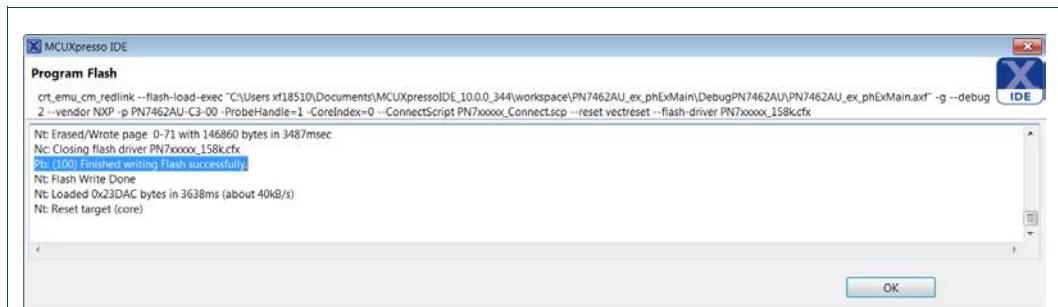
Once Flash tool started, correct LPC connection file and Flash driver file needs to be specified. For PN7462AU-C03-00 correct flash driver is PN7xxxxx_158k.cfx when updating user application. When updating EEPROM settings appropriate driver is PN7xxxxx_EE_3_5k.cfx



- (1) Select conenction script, flash driver and binary file
- (2) Ensure that all the options are set properly and Click OK

Fig 54. Build output - flash binary file

After selecting binary file flash process starts, and report is shown.



- (3) Flash report appears

Fig 55. Program flash report

6.8 Updating Flash and EEPROM via USB MSD interface

PN7462AU can update FLASH and EEPROM content via USB Mass Storage interface (primary download mode). This feature provides mechanism to easily update the application binary (users flash code) and EEPROM configuration.

To mount PN7462AU IC as USB Mass storage drive:

1. Ensure that “HIF selection” is USB, see Fig 56
2. USB Port of PC is connected to the USB port labelled X3 socket on the customer demo board
3. Press “RST_N” switch + Press “DWL_REQ” switch
4. Release “RST_N” and keep holding “DWL_REQ”
5. Release “DWL_REQ” button after about two seconds



Fig 56. PN7462AU as USB mass storage device

Now the customer demo board is detected by the PC as USB MSD (Mass Storage Device).

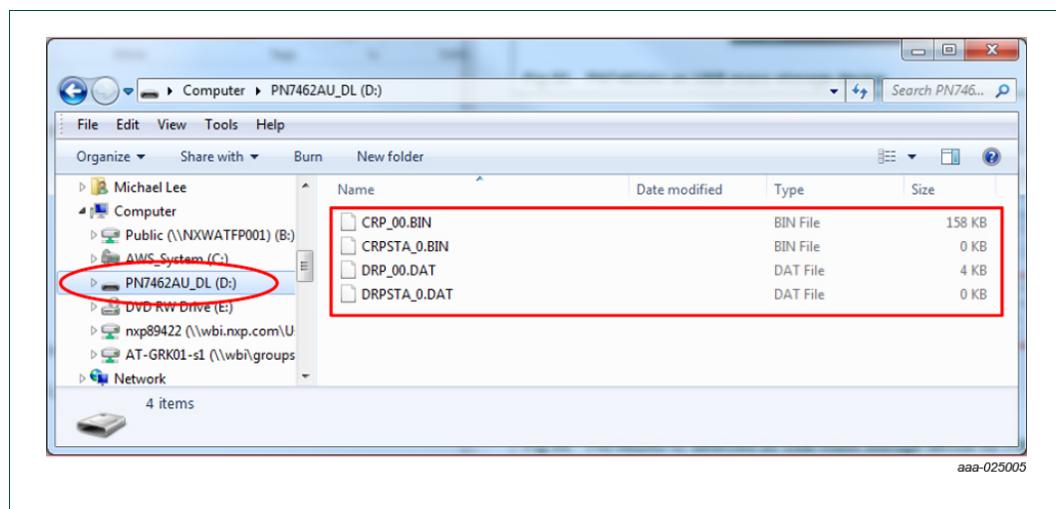


Fig 57. PN7462AU IC detected as USB mass storage device for FW/ EEPROM upgrade

When the PN7462AU is mounted as a USB mass storage device files listed in the table below are visible in the device root.

Table 5. Files found in USB mass storage

File	Description
CRP_<nn>.BIN	PN7462AU's user flash code (see Table 6 for description of <nn>)
CRPSTA_<s>.BIN	Status of previous write operation to user flash (see Table 7 for description of <s>)
DRP_<nn>.DAT	PN7462AU's user EEPROM data (see Table 6 for description of <nn>)
DRPSTA_<s>.DAT	Status of previous write operation to user EEPROM (see Table 7 for description of <s>)

PN7462AU USB mass storage supports various data/ code protection levels.

Table 6. Code and data protection level

<nn>	Description
00	Read and write allowed
01	Cannot read. Write allowed. Only applicable sectors erased before writing
02	Cannot read. All sectors of the applicable memory are erased before writing.
03	Cannot read. Cannot write via USB mass storage.

Table 7. Status of read write operating code

<s>	Description
0	Last write operation was successful
1	Memory region formatted
2 – or anything else	Failed
3	Fresh memory (FLASH/ EEPROM has never been downloaded via USB mass storage)

To effectively update the user flash or EEPROM via USB once the device is in USB Mass storage mode, the following instructions are to be followed:

1. Navigate to the newly mounted PN7462AU drive.
2. Delete CRP_<nn>.bin file in case the flash area needs to be updated or DRP_<nn>.bin file in case the EEPROM area needs to be updated.
3. Copy the Flash binary or the EEPROM binary file to the new Drive.
4. PN7462AU should automatically un-mount and re-mount itself.
5. The update was successful, if the following status files are present on the USB MSD.
CRPSTA_00.bin for the flash memory,
DPRSTA_00.bin for the EEPROM memory.
6. Press the “RST_N” switch and PN7462AU starts executing the new flash code.

7. PN7462AU software examples

7.1 General overview

For a detailed description of examples, please refer to the “UM10913 - PN7462AU Software User Manual”.

7.1.1 Application messages – debug printouts

The most of the examples supports debug messages printouts via the LPC-Link 2 debug probe directly to the MCUXpresso IDE console. The LPC-Link 2 probe needs to be connected to the customer board 10pin Cortex connector - SWD interface (Fig 52). “Debug build” configuration enables printout of application messages. Printout messages are displayed in the Debug Messages Console View. Console view can be opened in menu “Window → Show View → Console” or by clicking the shortcut keys “Alt+Shift+Q C”.

7.1.2 LEDs status specifications

All examples are programmed in way that LEDs on the board shows the current status of the running example. At the polling, all LEDs are turning on in a circular sequence and when any card is detected the Fig 58 represent the meaning of the LED pattern.

		Blue	Green	Yellow	Red
CL	Card detected			■	
	Operation successful		■	■	
	Operation/transaction failed			■	■
	Operation Ongoing		■	■	
Ct	Card detected	■			
	Operation successful	■	■		
	Operation/transaction failed	■			■
	Operation Ongoing	■	■	■	

Fig 58. LEDs status

7.2 PN7462AU_ex_phExMain – (CLIF + CTIF functionality)

The “phExMain” is the main example demonstrating CLIF and CTIF functionalities. CLIF functionality covering NFC Forum operation modes: R/W mode, card mode and P2P mode. The “phExMain” is the root of many sub examples described below. For task and interface managing, the application can be configured to use FreeRTOS or not.

Contactless operation:

1. Reader mode

Supports TypeA, TypeB, Felica, ISO15693, ISO18000p3m3 protocols. Example application can support only one card per technology. Supports up-to read and write for all protocols. Supports proprietary cards MIFARE Classic, MIFARE Ultralight and MIFARE Ultralight C till read and write. Supports authentication and reauthentication for MIFARE Classic and inventory read command for ICODE SLIX. Since Inventory read is a manufacturer specific proprietary command, thus, inventory read will work only for NXP manufactured ICODE cards one of which is ICODE SLIX. Supports Topaz/Jewel Tags - Command supported RID, READ8, WRITE-NE8

2. Peer to peer mode

Supports Active F 212 till PSL request only. Supports Passive A 106 and performs DEP exchange. API Given for active DEP transmit for f212.

3. Card mode

Emulates as Type A Card and support till RATS exchange.

Contact card operations:

ISO7816 Profile – implementation in source file phExMain_Ct.c: Supports SCosta card (ISO7816 profile) presence check, activation, PPS Exchange for higher baud rate, APDU exchange with card according to card's protocol (Either T0 or T1). Supports reading and writing binaries to SCosta card for selected EF.

7.2.1 Demo setup

This section describes in detail the setup and execution environment required for *phExMain* application.

The following devices are required to run the example:

1. PN7462AU customer board v2.1/2.2
2. LPC-Link 2 board
3. Power adapter
4. Contactless cards: Type A, Type B, Type F
5. Contact card ISO7816 compatible

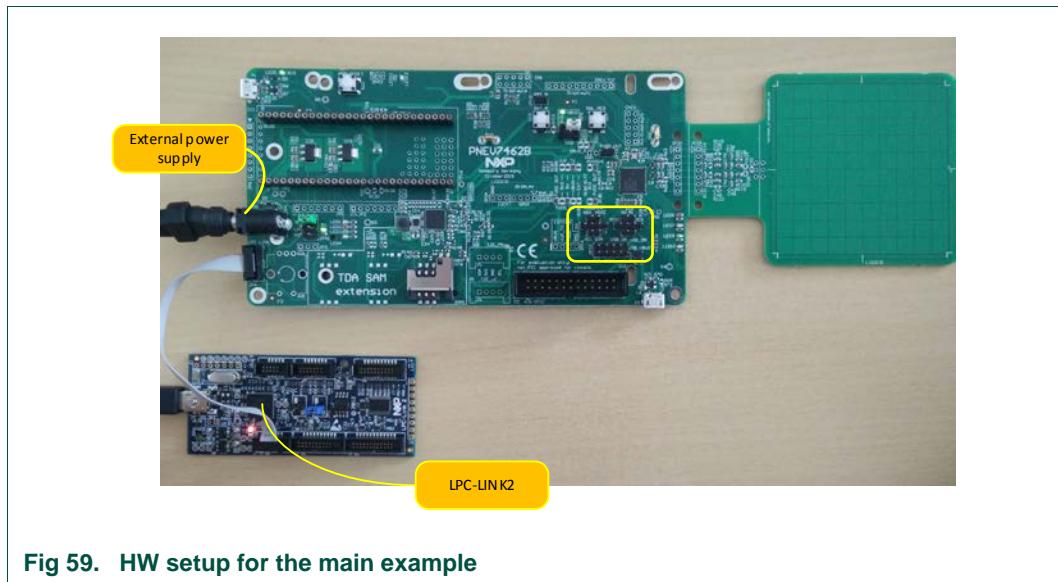


Fig 59. HW setup for the main example

7.2.2 Features

“phExMain” example is covering the following features:

Table 8. “phExMain” Example features

Feature	supported
CLIF Interface	Yes
CT Interface	Yes
NXP NFC Reader Library	Yes
CT Reader Library	Yes
FreeRTOS	Yes
Non RTOS	Yes
Standby mode	Yes
HIF/MIF Interface	No

7.2.3 FreeRTOS usage in this example

Example can be built in two configuration modes, with FreeRTOS and without FreeRTOS support.

By setting precompile directive “#PHFL_HALAPI_WITH_RTOS” or “#PHFL_HALAPI_NO_RTOS” the mode of the configuration is specified.

To build example in one or another mode, comment/uncomment proper directive in the “APP_NxpBuild.h” file.

In case of FreeRTOS mode, 3 tasks are used to control application flow:

- System Task which switches between CLIF functionality and CT functionality and handles system functions such as going to standby

- CLIF Task which executes NFC A, B, F reader application or EMV application and discovery loop
- CT Task which does an activation of a JCOP contact card, selects the T=1 protocol and executes EMV Card application.

In case of non RTOS support one main task is taking control on the application flow.

7.2.4 Operation with standby and without standby

Based on the compile time options, system task is responsible for managing different operation modes. The application can be in:

- Standby mode with wakeup timer and CT presence as wakeup configuration.
- Full power mode with GP Timer1 and CT presence interrupt enabled.

The standby feature can be enabled/disabled at compile time with the precompile directive. To enable standby mode "#PHFL_ENABLED_STANDBY" directive needs to be uncomment and can be found in the "APP_NxpBuild.h" file.

In this configuration, the FW by default puts the IC to standby and enables the wakeup sources such as contact card presence, wakeup timer and RF level detector (only for listen mode). The wakeup timer duration is taken from EE configuration (by default: 300ms). The IC wakes up at every wakeup timer duration and polls for contact card presence and if not present, polls for contactless technologies (or LPCD).

When a contactless or contact card is detected, the FW executes the corresponding application and returns back to standby.

In case "Standby" feature is disabled, the FW uses General Purpose Timer 1 as wakeup timer and CT presence interrupt to either branch to Contactless application or Contact application respectively.

The below 2 diagrams explain the Standby and Non-Standby scenarios. See Section 5.7 for further reference regarding RTOS.

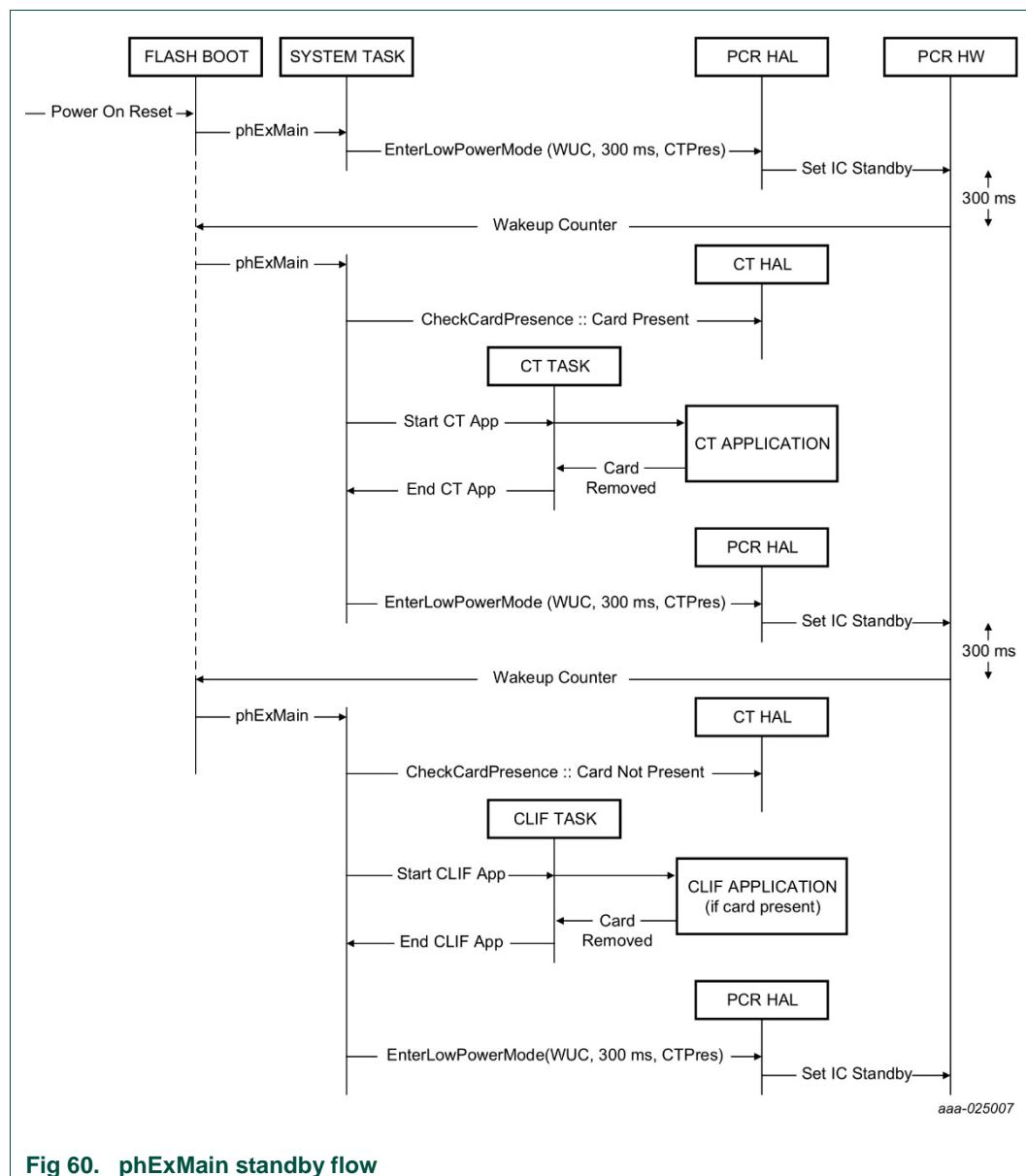
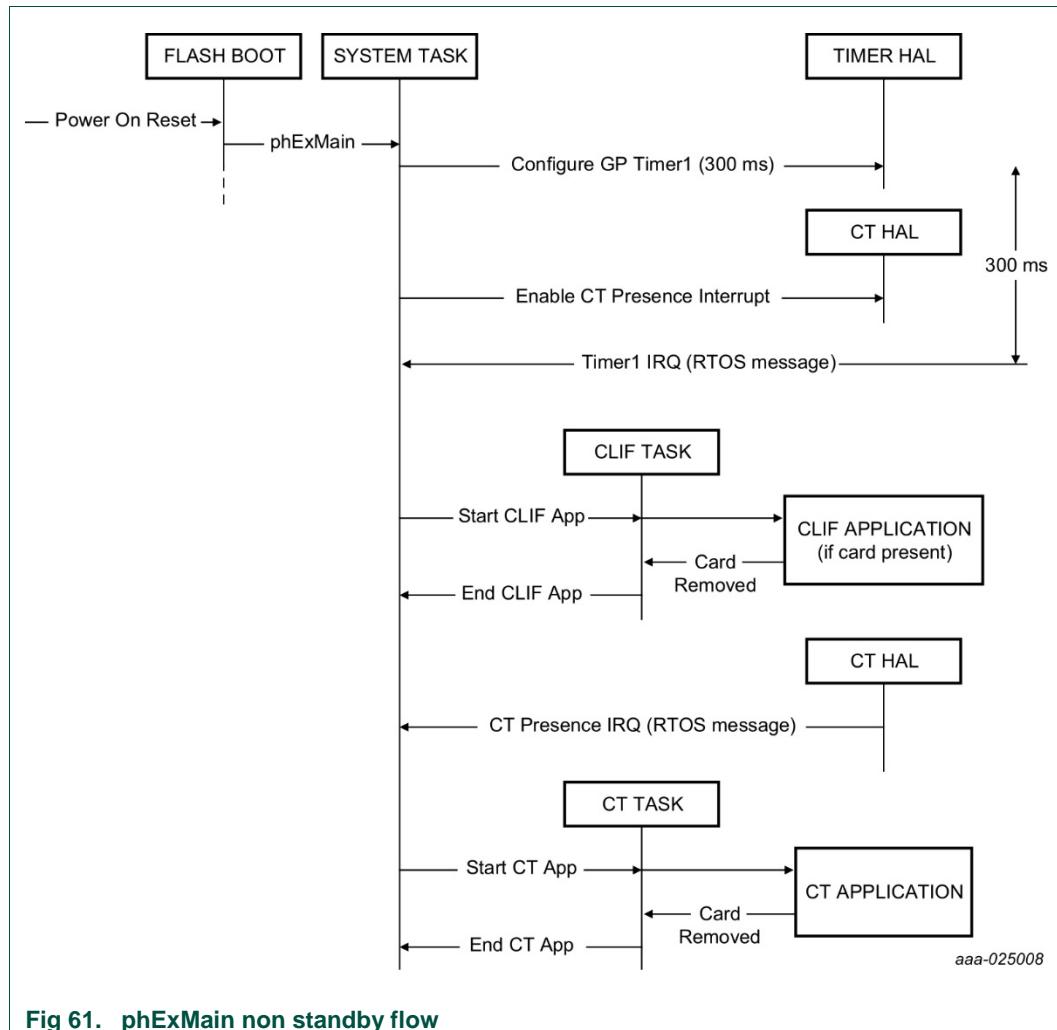


Fig 60. phExMain standby flow



7.2.5 MIFARE Classic

The MIFARE Classic example is implementing basic read/write functionality using a MIFARE Classic card with a predefined default key. If a Type A card is detected with SAK of 0x8 (1K MIFARE Classic card) or 0x18 (4K MIFARE Classic card), then the MIFARE Classic example is executed. The example performs initial authentication of block X and then reads/write to this sector. Further the example performs authentication of another block (say X +1) using the session key established during initial authentication (this is called re-authentication). It then performs read/write to this block X+1. See the function `phExMain_MiFareClassic()` and `phExMain_MifareOperations()`

Supported Functionality:

1. Authentication & Re-Authentication
2. Read/Write

Implementation in the “`phExMain_MiFareClassic.c`” file.

7.2.6 MIFARE Ultralight

The MIFARE Ultralight example is implementing basic read/write functionality using a non-secure MIFARE Ultralight card. If a Type A card is detected with SAK 0x00, then MIFARE Ultralight example is executed.

The example performs read and write to predefined pages of the card.

Supported functionality:

1. Read
 2. Write
- Since the stack also supports Type 2 tag, a check is performed to see if the card is NDEF tag or MIFARE Ultralight tag

Implementation in the “*phExMain_MiFareUltralight.c*” file.

7.2.7 MIFARE DESFire

If the detected SAK is 0x20 (expected card is MIFARE DESFire EV1), then ISO14443-4 Type A reader example is executed. The MIFARE DESFire example implements L4 exchange of “GetVersion” command at 106, 212, 424 and 848 kbps. No other commands are currently exchanged as they require authentication and crypto operations (which are not currently supported in the release).

Supported functionality:

1. Get Version at 106/212/424/848 kbps

Implementation in the “*phExMain_TypeA_L4Exchange.c*” file.

7.2.8 Jewel reader

If the ATQA of a Type A card denotes jewel card, the jewel example is executed.

The jewel example assumes a non-secure jewel card. The example performs read and write to predefined blocks of the card.

Supported functionalities:

1. Read
 2. Write
- Since the stack also supports Type 1 tag, a check is performed to see if the card is an NDEF tag or jewel card.

Implementation in the “*phExMain_Jewel.c*” file.

7.2.9 ISO15693 – ICODE SLIX

The example performs read and write to predefined blocks of the card.

Supported functionality:

1. Read single block
2. Write single block

3. Datarate Tx - 26kbit/s (1out of 4 coding) and Rx 26kbit/s
Implementation in the “*phExMain_ISO15693.c*” file.

7.2.10 ISO18000-3.3 – ICODE ILT

The example performs read and write to predefined blocks of the card.

Supported functionality:

1. Read block
2. Write word
3. TX TARI = 9.44 and RX 424_2 Manchester Period

Implementation in the “*phExMain_ISO18000p3m3.c*” file.

7.2.11 Type B eZLINK/ SLE card

If the detected technology is Type B, then ISO14443-4 Type B reader is executed.

This example is used demonstrate the ISO144434 exchange of APDUs to a Type B card at all baud rates.

Supported functionality:

1. Get Challenge106/212/424/848 kbps
2. No encryption

Implementation in the “*phExMain_TypeB_L4Exchange.c*” file.

7.2.12 Type F (FeliCa tag)

This example is used to read and write FeliCa frames to FeliCa tags at 212/424 kbps.

Since the stack supports Type 3 tags, check is performed to see if the card is a NDEF tag or FeliCa card.

Supported functionality:

1. CHECK
2. UPDATE
3. 212/424 kbps

Implementation in the “*phExMain_FeliCa.c*” file.

7.2.13 ISO14443-4 card mode (till activation)

During listen, the example can be configured to either act as ISO14443-4 card emulator (SAK = 0x20) or NFC-DEP Target (SAK = 0x40). This configuration is done via #define macro in *phExMain_Clif.h*

If the SAK is 0x20, discovery loop detects peer ISO14443A reader, the *phExMain_CardMode* is executed, that responds to RATS from the reader. This example does not demonstrate L4 APDUs exchange (it is done in *phExHCE* and *phExNFCForum*).

7.2.14 Passive and active ISO18092 initiator (till activation)

During active poll mode, if ATR_REQ is received or during passive poll mode, if SAK denotes 0x40, then the example implemented in phExMain_PasIni.c/ phExMain_ActIni.c is executed. These examples simply transmit a DEP_REQ command with arbitrary payload to peer target. The purpose of this example is only to demonstrate integration of ISO18092.

7.2.15 Passive ISO18092 target (till activation)

During listen, the example can be configured to either act as ISO14443-4 card emulator (SAK = 0x20) or NFC-DEP Target (SAK = 0x40). This configuration is done via #define macro in *phExMain_Clif.h*.

If the SAK is 0x40, discovery loop detects peer ISO18092 initiator, the phExMain_PasTgt is executed, that responds to ATR_REQ from the initiator. This example further waits for a NFC-DEP frame from the initiator.

7.2.16 Contact Example

If the IC boots because of CT presence wakeup reason or if the CT presence interrupt is generated, the System task starts the CT task. The CT task performs the Contact application. The contact application activates the card, and determines the card is of EMVCo payment card or nonpayment card. If payment card is detected, the application further communicates with the card to know which type of card (Master card, VISA or AMEX card), and prints the information.

Supported ISO7816 Functionality:

1. ATR Parsing
2. Create MF
3. Create EF
4. Select EF
5. Write Binary
6. Read Binary
7. Delete EF
8. SCOSTA Card
9. TA1 = 97
10. Supports Class A (DCDC always in double mode)

7.2.17 RTOS task management

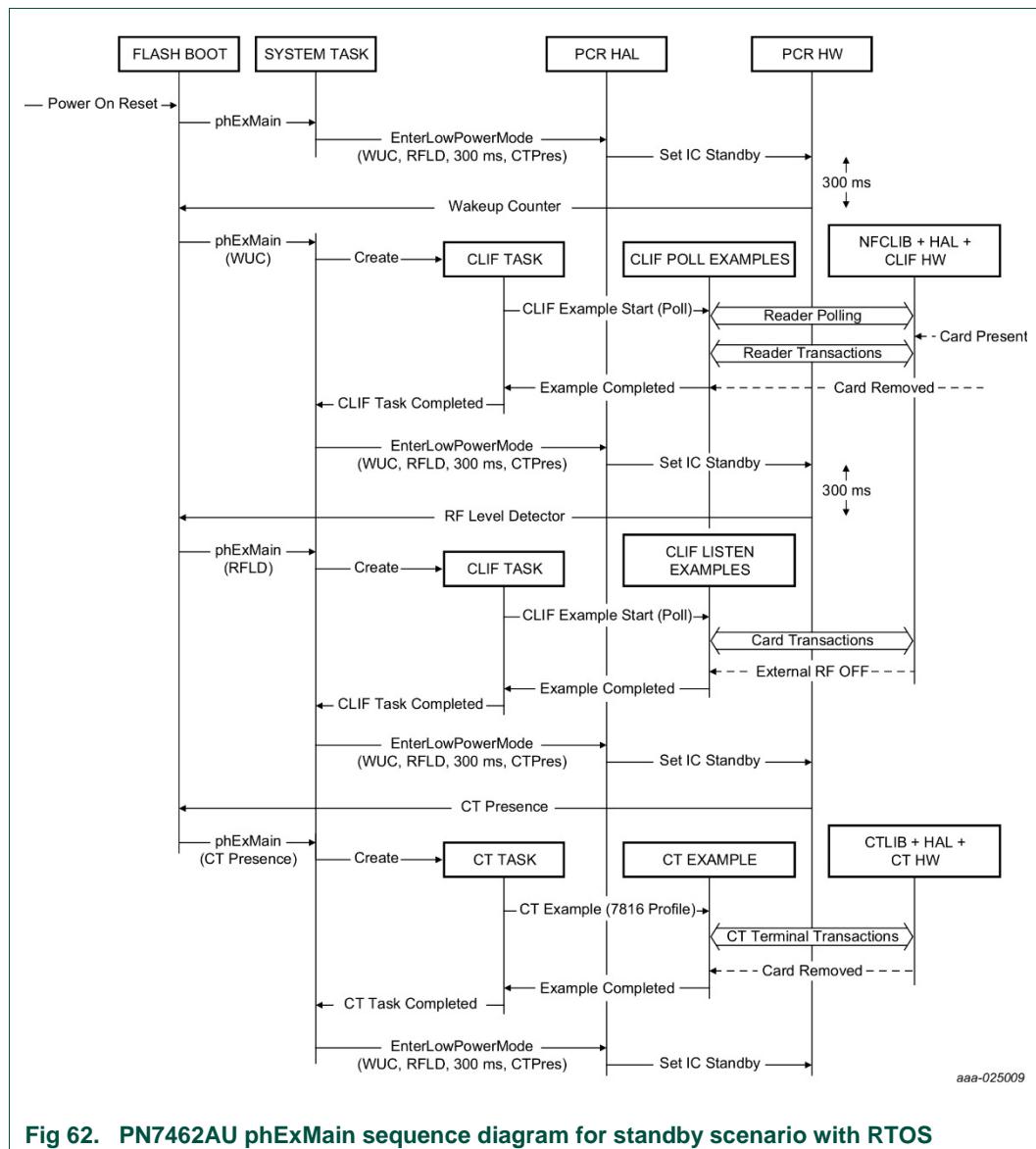
The phExMain example can be executed in both RTOS. In RTOS environment, three tasks are created.

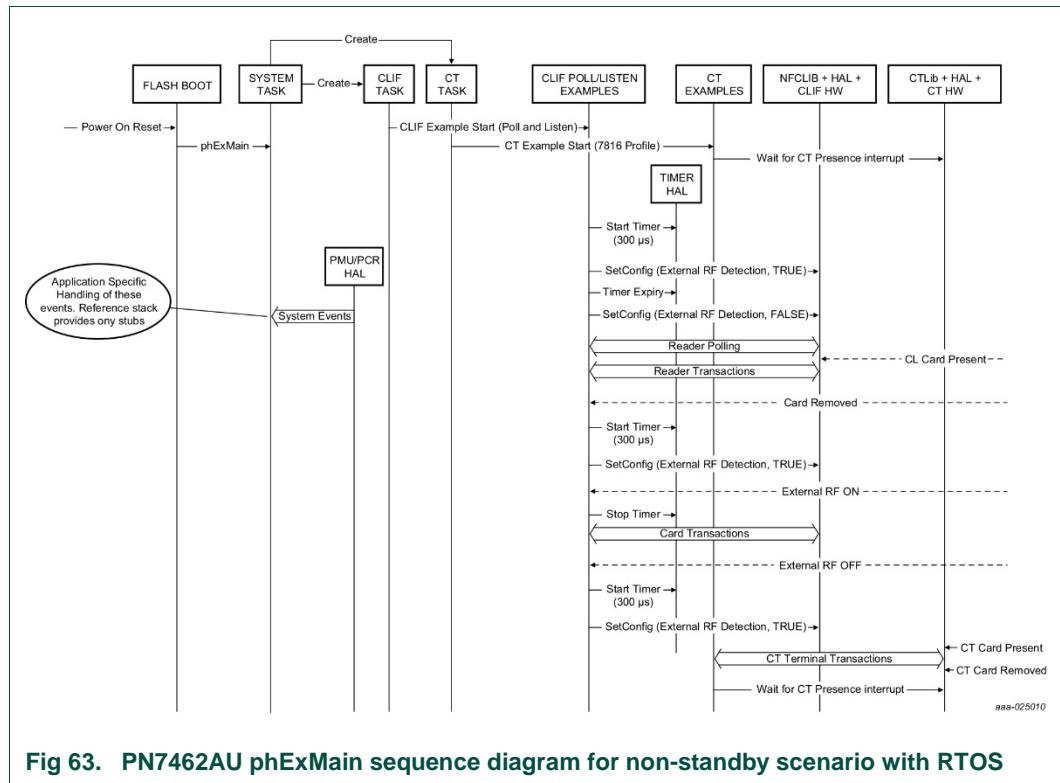
1. System task
 - a. Creates CLIF task
 - b. Creates CT task
 - c. Waits for PMU/PCR exception events

- d. Waits for CLIF Task completion if standby is enabled
 - e. Waits for CT Task completion if standby is enabled
 - f. Enter low power mode (standby)
2. CLIF task
 - a. Starts GP timer for listen duration if standby is **not** enabled and wait for GP timer expiry
 - b. Configure external RF on detection
 - c. If boot reason is WUC counter or GP timer expiry, perform polling mode of discovery loop
 - d. If boot reason is RFLD or external RF is detected, perform listen mode of discovery loop
 - e. Notify system task if polling/listening is completed and standby is enabled
 3. CT task
 - a. Enable CT presence interrupt and wait for CT presence interrupt
 - b. If boot reason is CT presence or CT presence interrupt is detected, perform CT example
 - c. Notify system task if polling/listening is completed and standby is enabled

Fig 62 and Fig 63 illustrate one instance of phExMain execution for both standby and non-standby scenarios.

- Please note that the CLIF and CT tasks are independent and can concurrently operate the CL and CT interfaces. During such concurrent operation, there is a possibility that CT interface may be unstable. It is up to the application design to configure interrupt and task priorities for a stable operation.





7.2.18 No-RTOS management

In case of No-RTOS the entry point from flash boot is *phExMain_NoRTOS*. The functionality remains the same except that the CLIF example and the CT examples are called from a single executive while loop based on timer interrupt or external RF detection or CT presence interrupt.

7.3 PN7462AU_ex_phExEMVCo (CLIF + CTIF functionality)

The “*phExEMVCo*” is an example which implements the polling for the EMVCo contact and contactless cards and implement reference EMV transaction.

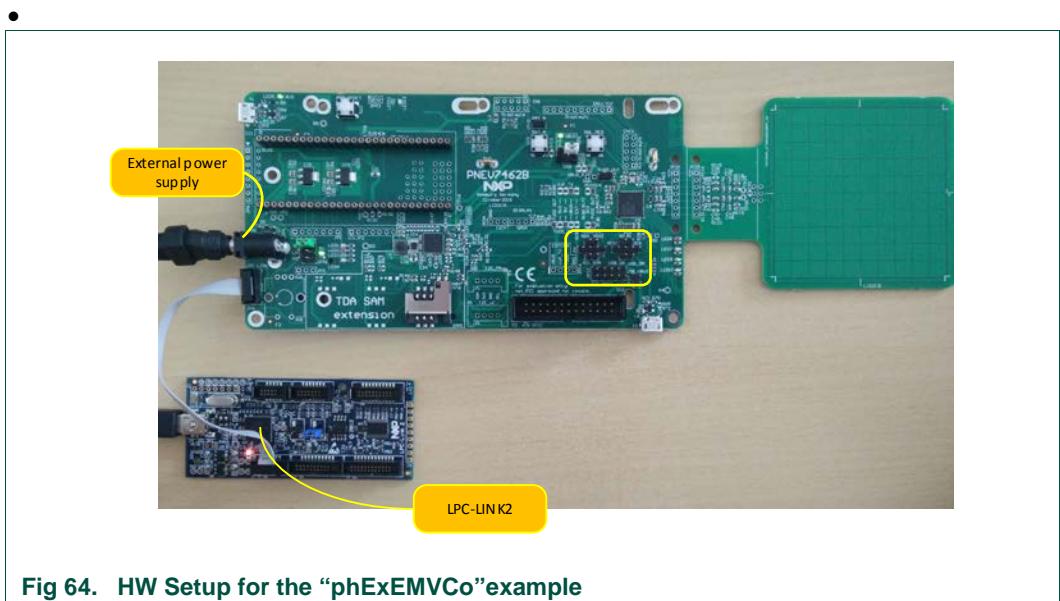
Application is based on the NFC Reader Library, CT Library and be run with or without FreeRTOS.

7.3.1 Demo setup

This section describes in detail the setup and execution environment required for the “*phExEMVCo*” application.

The following things are required for setup:

1. PN7462AU customer board v2.1/2.2
2. LPC-Link 2 board
3. Power adapter
4. Contact and contactless EMVCo card



7.3.2 Features

“*phExEMVCo*” example features:

Table 9. “phExEMVCo” Example features

Feature	supported
CLIF Interface	Yes
CT Interface	Yes
NXP NFC Reader Library	Yes
CT Reader Library	Yes
FreeRTOS	Yes

Feature	supported
Non RTOS	Yes
Standby mode	No
HIF/MIF Interface	No

7.3.3 EMVCo polling loop

In this example EMVCo polling loop is enabled. In this profile, only Type A and B technology polling is enabled and bail out is set such that both A and B techs are polled even if one of them is detected. This is to ensure no two cards of same/different tech are present in the POS for EMV transaction. Low Power Card Detection (LPCD) is disabled in this profile.

7.3.4 EMV transaction

This example implement next EMV Transactions:

- SELECT (PPSE)
- SELECT command
- GET PROCESSING OPTIONS
- READ RECORD
- GENERATE AC

Supported EMV functionality:

- ATR Parsing accordingly to the EMV specifications
- Send Different AIDs to identify card
 - Master Card: Credit or Debit
 - Visa Card: Credit or Debit
 - Master Card: Maestro (debit card)
 - Master Card: Cirrus (interbank network)
 - Master Card: Maestro UK
 - Visa Card: Electron card
 - Visa Card: V PAY card
 - Visa Card: VISA Plus card
 - Amex Card –
- Class A (DCDC always in double mode)

7.3.5 RTOS task management

- For information regarding RTOS task management, refer to Section 7.2.17

7.3.6 No RTOS management

- For information regarding No RTOS management, refer to Section 7.2.18

7.4 PN7462AU_ex_phExRf (CL functionality)

The “*phExRf*” is an example which implements the polling for contactless cards without NFC Reader Library support. Application use only HAL APIs and perform same CLIF functionality as 0 “*phExMain*” example with the only difference that for the transaction static predefined packets are used.

Application does not implement CT and “Standby” functionality and it is not based on the FreeRTOS.

7.4.1 Demo setup

This section describes in detail the setup and execution environment required for “*phExRf*” application.

The following devices are required to run the example:

1. PN7462AU customer board v2.1/2.2
2. LPC-Link2 board
3. Power adapter
4. Contactless cards Type A, Type B, Type F, ISO15693
5. NFC Enabled Phone

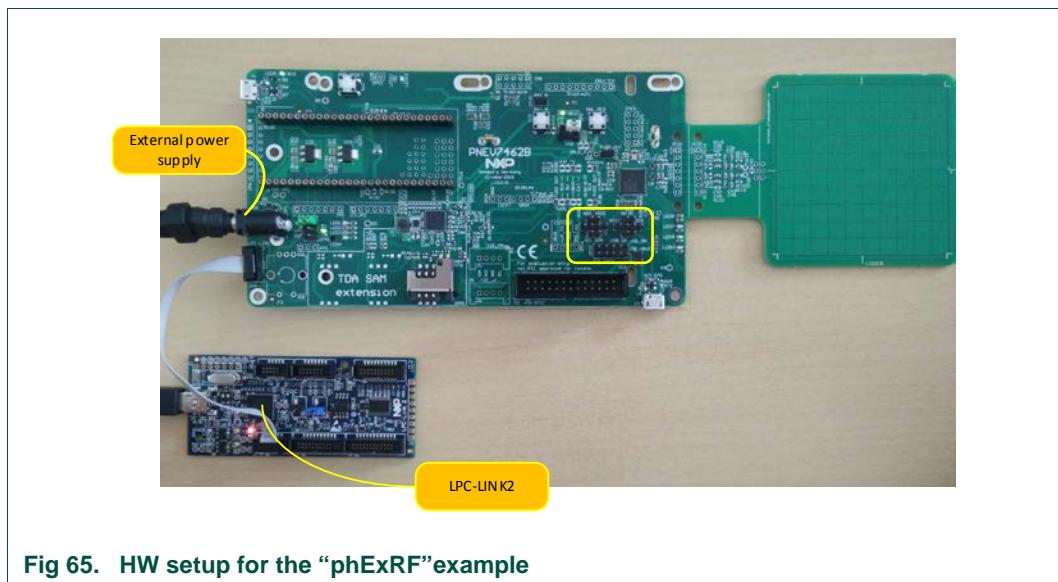


Fig 65. HW setup for the “phExRF”example

7.4.2 Features

“*phExRF*” example is covering next features:

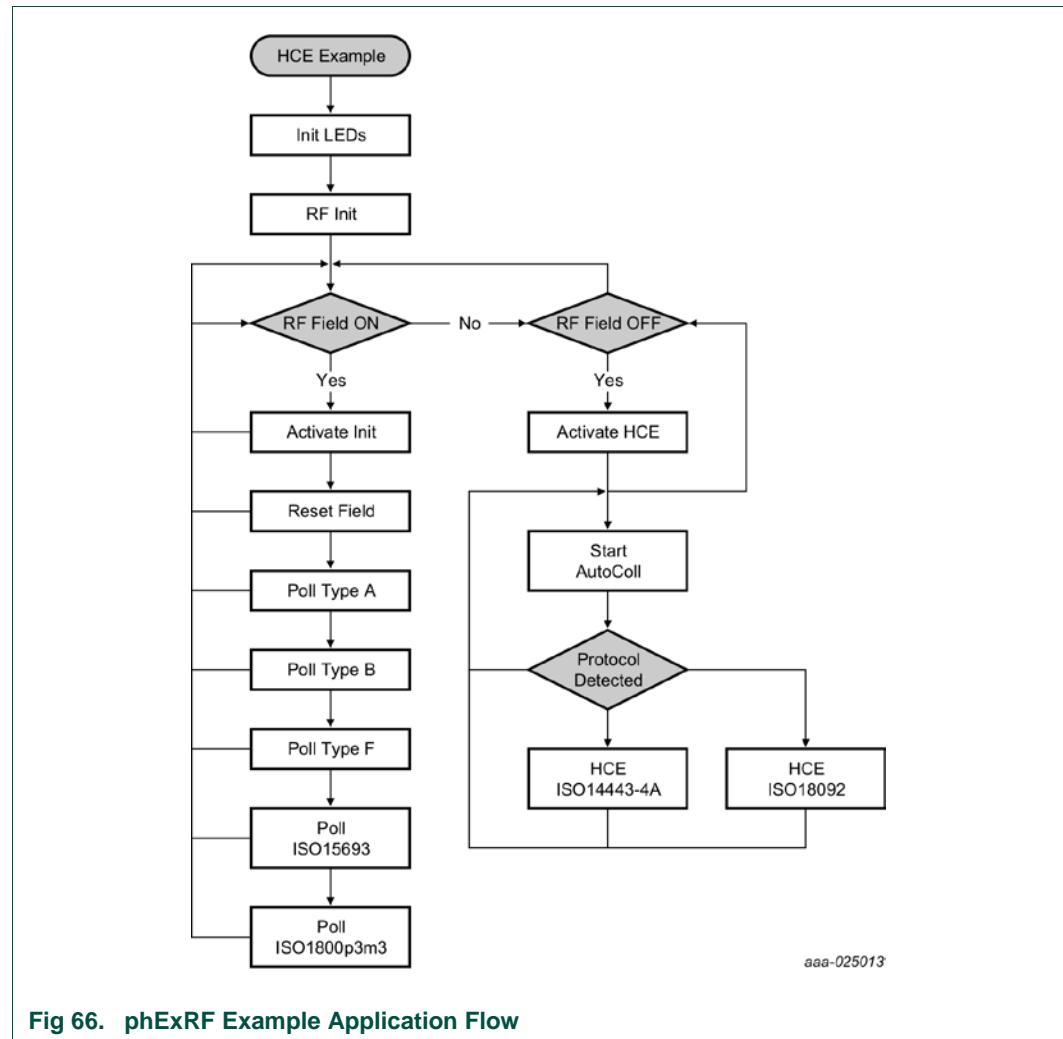
Table 10. “*phExRf*” Example features

Feature	supported
CLIF Interface	Yes
CT Interface	No

Feature	supported
NXP NFC Reader Library	No
CT Reader Library	No
FreeRTOS	No
Non RTOS	Yes
Standby mode	No
HIF/MIF Interface	No

7.4.3 Application Flow

The figure below demonstrates the application flow.



7.5 PN7462AU_ex_phExRfPoll example (CL functionality)

The “*phExRfPoll*” is an example which implements the polling for contactless cards without NFC Reader Library support for the optimization of the RF-signal. Through defines in *phExRfPoll.c* the specific technology to poll for can be selected.

By setting breakpoints RF registers can be modified to change the signal.

7.6 PN7462AU_ex_phExCT (CT functionality)

This example implements simple polling for contact cards. Application use only HAL APIs and perform same CTIF functionality as 0 “*phExMain*” example with the only difference that for the transaction static predefined packets are used and example is not using any library. *phExCt* performs activation of an EMVCo card. SELECT Master card APDU is sent depending on the protocol supported by the card and expects RAPDU 0x90 0x00.

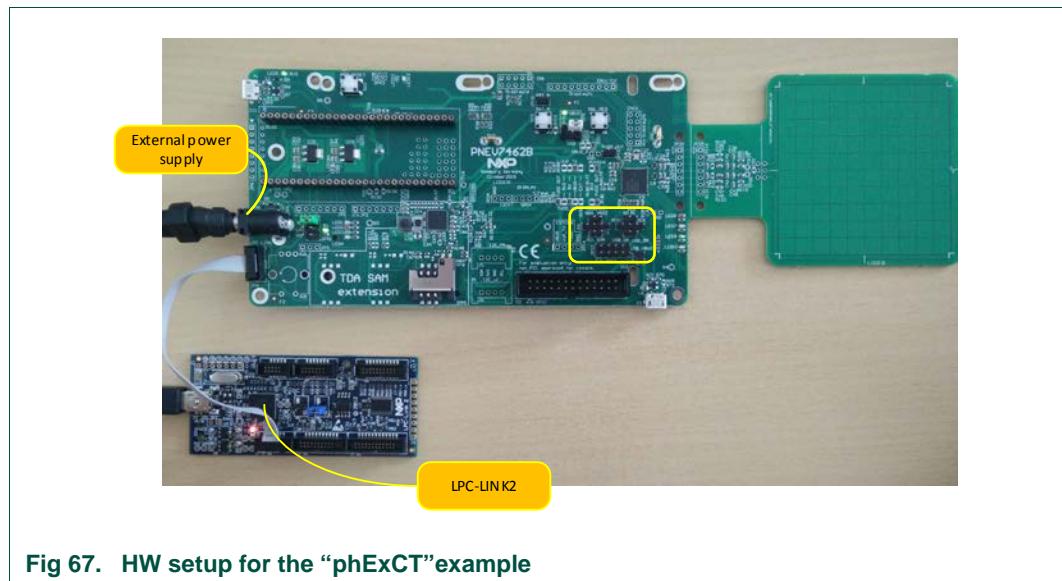
The example is also capable of determining the non-EMVCo card or non-Master card. After the transactions, deactivation is performed. Also, this example demonstrates the non-RTOS integration of application with HALs.

7.6.1 Demo setup

This section describes in detail the setup and execution environment required for “*phExCT*” application.

The following devices are required to run the example:

1. PN7462AU customer board v2.1/2.2
2. LPC-Link 2 board
3. Power adapter
4. Contact card ISO7816 compatible



7.6.2 Features

phExCT example is covering next features:

Table 11. “phExRf” Example features

Feature	supported
CLIF Interface	No
CT Interface	Yes
NXP NFC Reader Library	No
CT Pal Library	No
FreeRTOS	No
Non RTOS	Yes
Standby mode	No
HIF/MIF Interface	No

7.6.3 Application Flow

The figure below demonstrates the application flow.

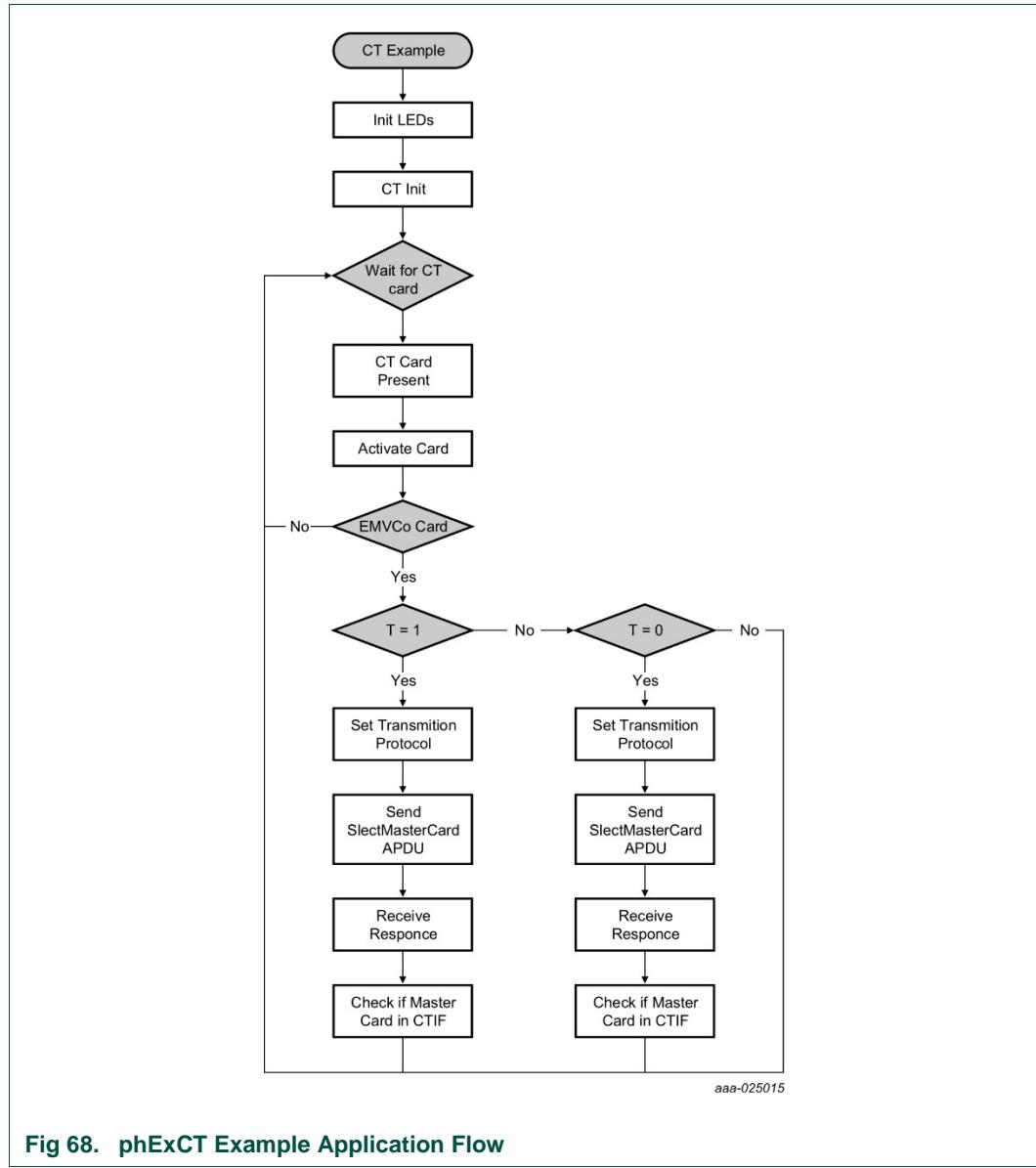


Fig 68. phExCT Example Application Flow

7.6.4 EMVCo activation

The example performs EMVCo activation and EMVCo ATR parsing. It also determines the protocol supported by the card.

7.6.5 SELECT master card

The example sends a SELECT master card APDU and expects a RAPDU 0x90 0x00.

7.7 PN7462AU_ex_phExCTEMVCo (CT functionality)

The “*phExCtEMVCo*” is an example which implements the CT functionality with CT Pal library support. Application use CT PAL library APIs and perform same CT functionality as 0 “*phExEMVCo*” example with the only difference that for the transaction static predefined packets are used. After the transactions, deactivation is performed. The example is also capable of determining the Non-EMVCo card.

Application does not implement CLIF and “Standby” functionality and it is not based on the FreeRTOS.

7.7.1 Demo setup

In this example the same setup is used as in “*phExEMVCo*” example.

7.7.2 Features

“*phExCT*” example is covering next features:

Table 12. “*phExRf*” Example features

Feature	supported
CLIF Interface	No
CT Interface	Yes
NXP NFC Reader Library	No
CT Pal Library	Yes
FreeRTOS	No
Non RTOS	Yes
Standby mode	No
HIF/MIF Interface	No

7.7.3 EMVCo activation

The example performs an EMVCo activation and EMVCo ATR parsing. It also determines the protocol supported by the card and applies the protocol supported.

7.7.4 APDU transactions

The example is capable of sending select commands for nine pre-selected types of EMVCO cards after successful activation.

1. Master Card: Credit or Debit
2. Visa Card: Credit or Debit
3. Master Card: Maestro (debit card)
4. Master Card: Cirrus (inter-bank network)
5. Master Card: Maestro UK
6. Visa Card: Electron card
7. Visa Card: V PAY card
8. Visa Card: VISA Plus card
9. Amex Card

7.8 PN7462AU_ex_phExCT7816 (CT functionality)

The “PN7462AU_ex_phExCt7816” example implements the CT functionality with CT library support. Application use CT library APIs and perform same CT functionality as in “PN7462AU_ex_phExMain” example with the only difference that for the transaction static predefined packets are used. The example is built to work on a SCOSTA card. PN7462AU_ex_phExCT7816 demonstrates the CT Protocol Lib + HAL API’s. After the transactions, deactivation is performed.

Application does not implement CLIF and “Standby” functionality and it is not based on the FreeRTOS.

7.8.1 Demo setup

In this example the same setup is used as in “phExMain” example.

7.8.2 Features

“phExCT7816” example is covering next features:

Table 13. “phExCT7816” Example features

Feature	supported
CLIF Interface	No
CT Interface	Yes
NXP NFC Reader Library	No
CT Pal Library	Yes
FreeRTOS	No
Non RTOS	Yes
Standby mode	No
HIF/MIF Interface	No

7.8.3 ISO7816 activation

The example performs an ISO7816 activation and ISO7816 ATR parsing. Also, it determines the protocol supported by the card and applies the protocol supported.

7.8.4 APDU transactions

The following APDU's are sent after the activation of the card. If the card supports the following APDU's (e.g. SCOSTA), proper responses will come from the card.

1. Create MF
2. Create EF
3. Select EF
4. Write binary
5. Read binary
6. Delete EF

7.9 PN7462AU_ex_phExHif

This example demonstrates host interface loopback functionality for I2C, SPI, HSU and master interface functionality for I2CM, SPIM. Beside that it demonstrates secondary downloader functionality to EEPROM and FLASH memory over SPI Host interface. For Host Interface Frames “FREE Format” is used.

Application is implementing CT functionality with SPI Host interface and it is not based on the FreeRTOS.

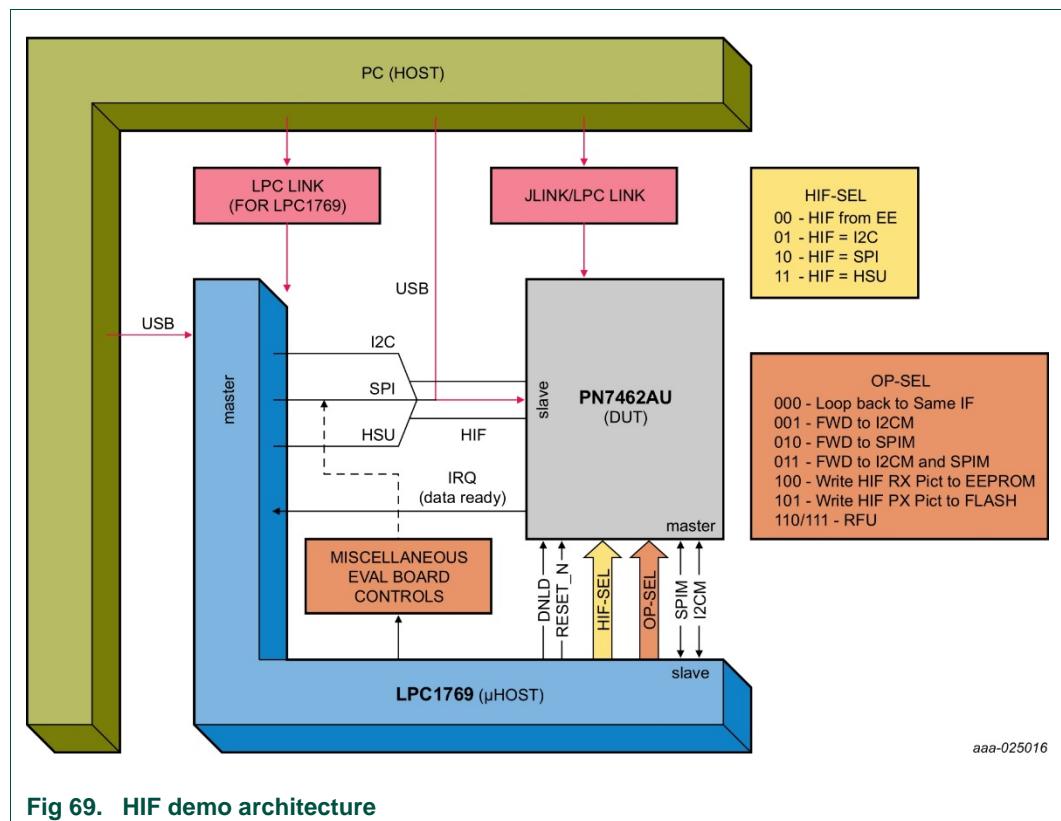
Application consist from two projects. First application is executed on the PN7464AU and second application needs to be executed on the LPC1769 board (LPCXpresso board for LPC1769 with CMSIS DAP probe [5]).

7.9.1 Demo setup

This section describes in detail the setup and execution environment required for the “*phExHif*” application.

The following devices are required for setup:

1. PN7462AU customer board v2.1/2.2
2. LPC1769 board
3. LPC-Link2 board
4. Power adapter



The GPIOs of LPC and PN7462AU are used to determine which functionality of this example has to be executed. It is also used to select the host interface or master interface to be used. For each different functionality, a different MCUXpresso project is required for LPC1769 side while PN7462AU side has only the phExHif MCUXpresso project.

The phExHIF indicates its readiness to LPC1769 through GPIO1 of PN7462AU connected to GPIO0.0 of LPC1769 (APP ready pin).

7.9.2 Features

“phExHif” example is covering next features:

Table 14. “phExHif” Example features

Feature	supported
CLIF Interface	No
CT Interface	Yes
NXP NFC Reader Library	No
CT Pal Library	Yes
FreeRTOS	No
Non RTOS	Yes
Standby mode	No
HIF/MIF Interface	yes

7.9.3 HIF selection

Table 15. Host interface selection

GPIO5_PN7462AU ← GPIO2.0_LPC	GPIO4_PN7462 ← GPIO2.1_LPC	Chosen HIF
0	0	Invalid
0	1	I2C
1	0	SPI
1	1	HSU

PN7462 USB mass storage supports various data/ code protection levels.

7.9.4 Operation selection

The tabulated GPIO configuration selects the operation to be performed by examples shown in Table 16.

Table 16. Operation on the packet received on HIF

GPIO8_PN7462AU ← GPIO2.2_LPC	GPIO7_PN7462AU ← GPIO2.3_LPC	GPIO6_PN7462AU ← GPIO2.4_LPC	Chosen HIF
0	0	0	Loopback on HIF
0	0	1	Forward HIF Rx Packet to I2CM Tx
0	1	0	Forward HIF Rx Packet to SPIM Tx
0	1	1	Forward HIF Rx Packet to SPIM & I2CM Tx Both
1	0	0	Program EEP with HIF Rx Packet
1	0	1	Program FLASH with HIF Rx Packet
1	1	0	Forward HIF Rx Packet to CT
1	1	1	RFU

Application ready PIN is connected with GPIO0.0_LPC on the LPC board.

Important guidelines:

- 1 → Logical HIGH as seen/set by the GPIO.
- 0 → Logical HIGH as seen/set by the GPIO.
- Start PN7462AU Application before launching LPC Application
- Since both the projects are MCUXpresso IDE based, while updating FW image via the LPC Link, ensure that the image is downloaded to the correct platform.

7.9.5 EEPROM configuration dependencies

Values from the following EEPROM structures are used in this example:

- Boot: EEPROM
- Boot: FLASH
- Boot: CT
- Boot: GPIO
- HW: I2CM
- HW: SPIM
- HW: HIF

7.9.6 MCUXpresso projects provided for LPC1769

- LPCEHif_HSU_LoopBack_App
- LPCEHif_HSU_to_I2CM_SPIM_App
- LPCEHif_I2C_Loopback_App
- LPCEHif_I2C_to_SPIM_App
- LPCEHif_SPI_CT_App
- LPCEHif_SPI_LoopBack_App
- LPCEHif_SPI_to_EEPROM_App
- LPCEHif_SPI_to_FLASH_App
- LPCEHif_SPI_to_I2CM_App
- Supporting libraries
 - PN640_lpc17xx_lib, CMSISv2p00_LPC17xx

7.10 PN7462AU_ex_phExPos

POS use-case demo application shows how to use PN7462AU in combination with second application hosted on the µController. In this example LPC1769 µC is used and connection is established through SPI host interface. POS use-case demonstrate the Pay pass transaction on the contact and contactless frontend.

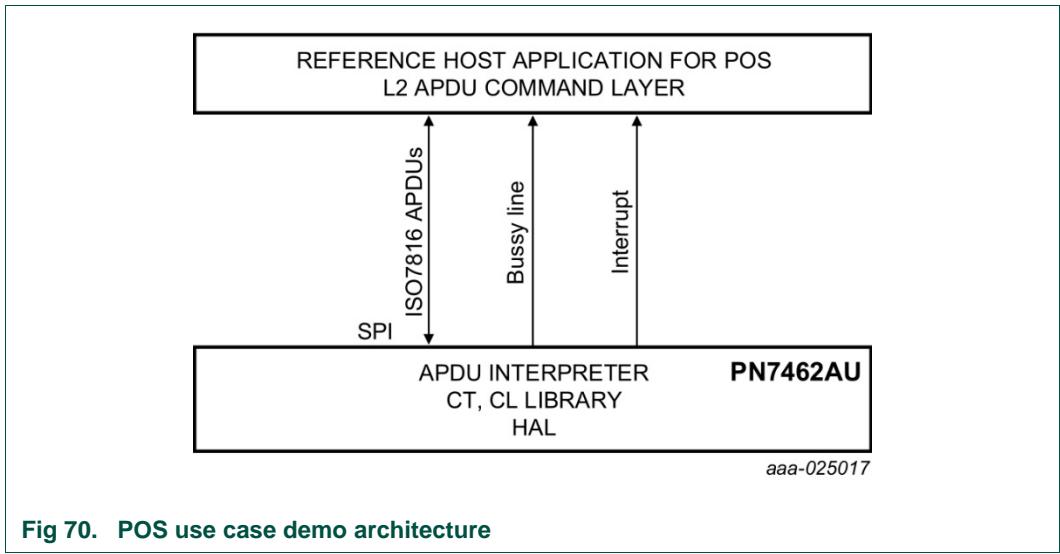


Fig 70. POS use case demo architecture

The POS demo architecture is split into application layer (L2) and low level EMVCo compliant layer L1 which is hosted on the PN7462AU. The application layer L2 commands are simulated in reference microcontroller board (LPC1769) and L1 layer components are placed in PN7462AU.

The application APDU commands (L2) are communicated to PN7462AU through SPI host interface. PN7462AU GPIO pin is used to synchronize command/response between LPC1769 and PN7462AU.

Interrupt pin is used to notify valid ISO 14443-4 card to LPC1769.

Note

Detailed description and how to use example is described in “POS Use Case Demo Setup Manual”.

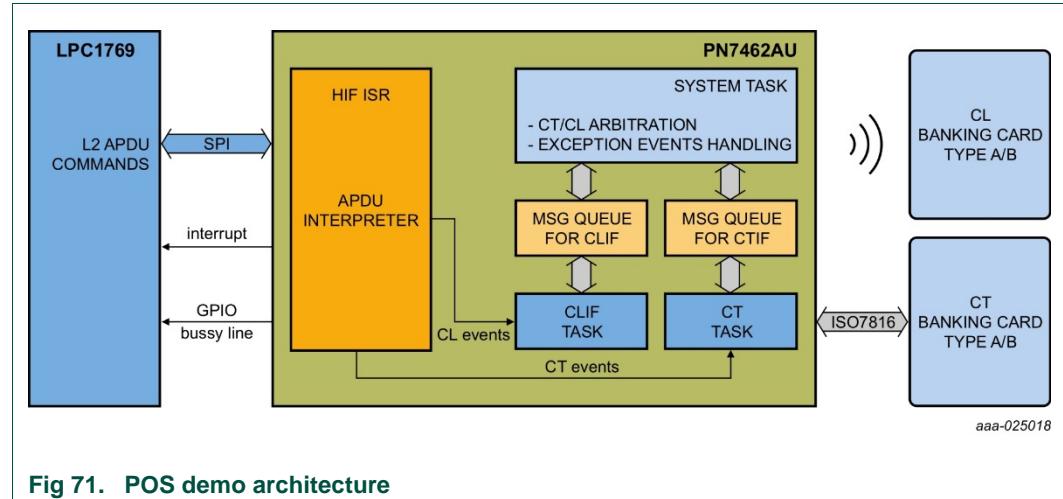
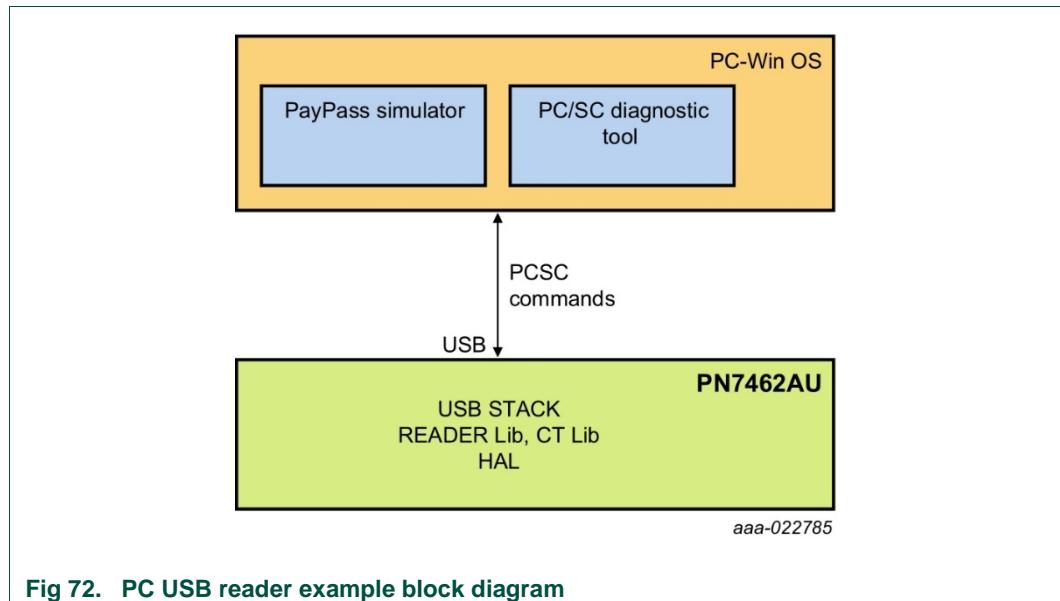


Fig 71. POS demo architecture

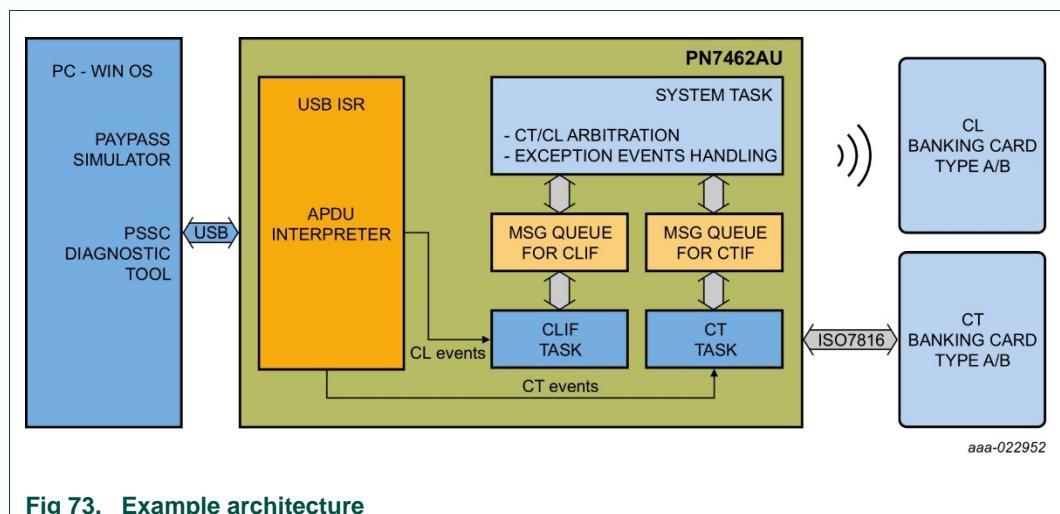
7.11 PN7462AU_ex_phExCcid

The PC USB reader application demonstrate how to use the PN7462AU Customer Demo board as a CCID reader and shows how connected PN7462AU via USB interface to a PC and provide the CCID protocol implementation on the top of the physical link.

The PC USB reader example is hosted on the PN7462AU and can be tested with any PC/SC application running on the PC with Windows OS.

**Fig 72. PC USB reader example block diagram**

The USB stack and CCID class is implemented in the PN7462AU. The default CCID driver present in PC with Windows OS is used for operation.

**Fig 73. Example architecture****Note:**

Detailed description and how to use example is described in “PC Reader Demo Setup Manual”.

7.12 PN7462AU_ex_phSystemServices

This example application demonstrates system services invocation. The PN7462AU provides ROM services that are accessible via flash APIs, also described in /PN7462AU/phROMIntf/phhalSysSer/inc/phhalSysSer.h and with more detailed description in API documentation.

This application requires user interface for performing the operations so it is needed to use debug mode. Some of the featured system service commands could be irreversible or reversible depending on the application mode configured by:

```
#define ENABLE_IR_REVERSIBLE_COMMANDS 0 //1
```

If the macro ENABLE_IR_REVERSIBLE_COMMANDS is defined to 0, example will not run irreversible commands, if defined to 1 example will run irreversible commands but user confirmation is needed.

Table 17. PN7462AU_ex_phSystemServices features

Feature	description
SECROW Lock	The HW SecRow contains the SWD access bits, code write-protection bits and RSTN pin behavior bits. For blocking any further writes to SecRow, the phhalSysSer OTP_SetSecrowLock() is used. It prevents further usage of phhalSysSer OTP_SecrowConfig() function.
Code write protection	It is required to lock flash memory from write at HW level. It is locked possibly at a stage when secure secondary upgrade is not planned for the remaining lifecycle of the product. For such use cases, phhalSysSer OTP_SecrowConfig() is used to lock flash memory from any further write. Any flash programming after locking the flash results in hard fault. Once SECROW functionality is locked, this feature cannot be used anymore.
Block SWD debugging	This command disables PN7462AU SWD debug interface. When the PN7462AU IC is delivered from production to user, the default SWD access level enables the user to view and debug user flash memory, user EEPROM memory, user RAM memory, and peripheral registers. The access level can be irreversibly changed to prevent view/debug access to any memory region or peripheral registers, before deploying the IC to the field. phhalSysSer OTP_SecrowConfig() can be used to lock the SWD against any further access. Once SECROW functionality is locked, this feature cannot be used anymore.
Disable primary download	Command is used to irreversibly disable the ROM primary download feature. On subsequent boots, the ROM boot never enters ROM primary download mode, even if DWL_REQ pin and USB_VBUS pin is high. This feature is typically used after development and flashing of secondary downloader in the flash memory, for subsequent code/data upgrades.
Update Product ID	USB Product ID - PID update
Update Vendor ID	USB vendor ID - VID update
Perform In Application Programming	Application asks for FLASH page number. Page is 128bytes long, for 158kb of the flash memory, the page number is in range 0-1263. The selected flash page is updated from user programmable values.
Set internal PVDD	PVDD is pad voltage reference and supply of the host interface (HSU, USB, I2C, and SPI) and the GPIOs. This command sets PVDD configuration to internal.
Get ROM version	Commands returns current ROM firmware version

Note:

For irreversible commands: Secrow lock, code write protection, block SWD debugging and disable primary download the undo is not possible!

7.13 PN7462AU_ex_phExVCom

This example application features TypeA card detection, RF field control and communication with the PC host over USB CDC interface (VCOM).

7.13.1 Demo setup

Customer demo board is connected to the PC host via USB interface. USB micro socket X3 on the Customer demo board needs to be connected to the PC's USB port. The proper USB host interface configuration on the Customer Demo board is depicted in 3.2.1.1. Application outputs debug traces to and receives commands from the terminal emulation application running on the PC host. Serial port parameters are 9600/8/1/N/1.

7.13.2 Command set

Commands are entered by the terminal emulation program. Each command is one character long.

- a) T command (character T), example application enters Type A detection mode and the terminal output is as follows:

```
Poll command received  
Entering TypeA Polling mode..  
Type A Polling  
Type A Polling  
Card UID=0424566AF13B80  
Card UID=0424566AF13B80  
Card UID=0424566AF13B80  
Type A Polling  
Type A Polling
```

LED8-10 lit in circular pattern.

- b) O command (character O), example application turns RF field permanently ON, the corresponding output on the terminal console is:

```
RF ON command received  
LED9 (Green) and LED10 (Blue) lit.
```

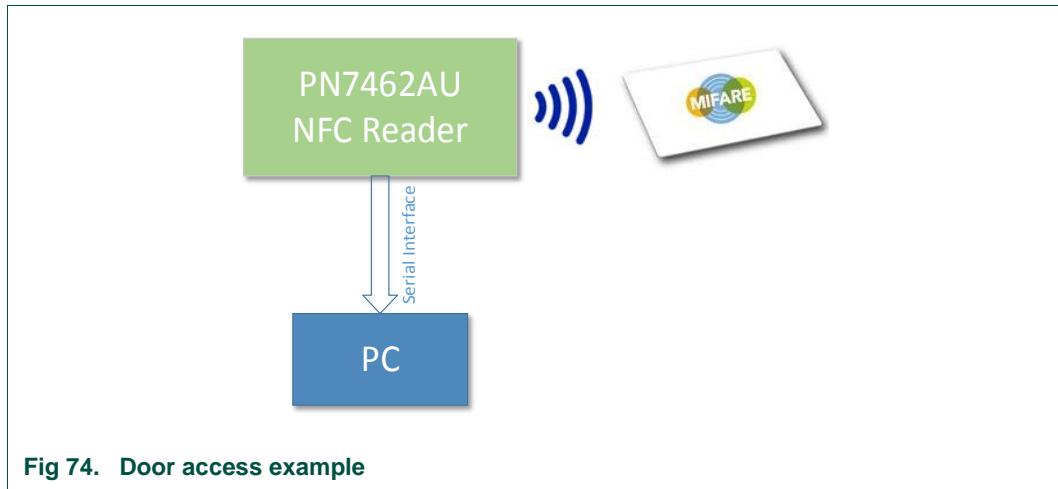
- c) F command (character F), example application turns RF field permanently OFF, output on the terminal console is :

```
RF OFF command received  
LED7 (Red) and LED8 (Yellow) lit.
```

7.14 PN7462AU_ex_phExDoorAccess

The example application demonstrates card detection, card authentication and HSU interface communication with the PC host. The application is running a NFC polling loop and goes to standby mode after each polling loop in case no CL card is detected by the RF field of the reader. The polling loop is implemented for Type A, B, F, ISO15693 and ISO 1800-P3M3. The application prints out the detected type of the card and UID if

available. In case the NFC device is detected, the application sends a NDEF message containing the NXP webpage address.



After each polling loop the application goes to standby mode and remains for 500ms. A timer is used as a wakeup source from standby. This process continues until a card is detected by the RF field of the reader. If a card is detected, the card type with its UID is sent via HSU and will be printed on the PC console.

In case a MIFARE Classic card is detected, application tries to authenticate the card using the default MIFARE key. If the authentication is successful a block of data is read from the card. The type of the card, UID and data are sent via HSU and printed on the PC console.

P2P functionality is integrated. When a NFC enabled phone is detected from the RF field as an active or passive target the LLCP SNEP will be activated and NDEF message will be sent to the mobile device.

If LPCD (Low Power Card Detection) is enabled, the reader checks during the wakeup time the presence of a card and enters the card detected mode when a card is present & repeats the cycle. If no card is present it goes back to standby mode. LPCD is enabled by default.

Note:

Detailed description and how to use example is described in "Door Access User Manual".

7.15 PN7462AU_ex_phExDoorAccessEC

This example is related to the 7.14 but in this version the application is using a MIFARE DESFire EV1 card for the authentication, data exchange is done over contactless interface and software key store or SAM (Secure Access Module) key store is used for storing the authentication key. By default, the software key store is enabled. The user can use the SAM key store by enabling corresponding. SAM is a key storage element and it should be inserted in the CT main.

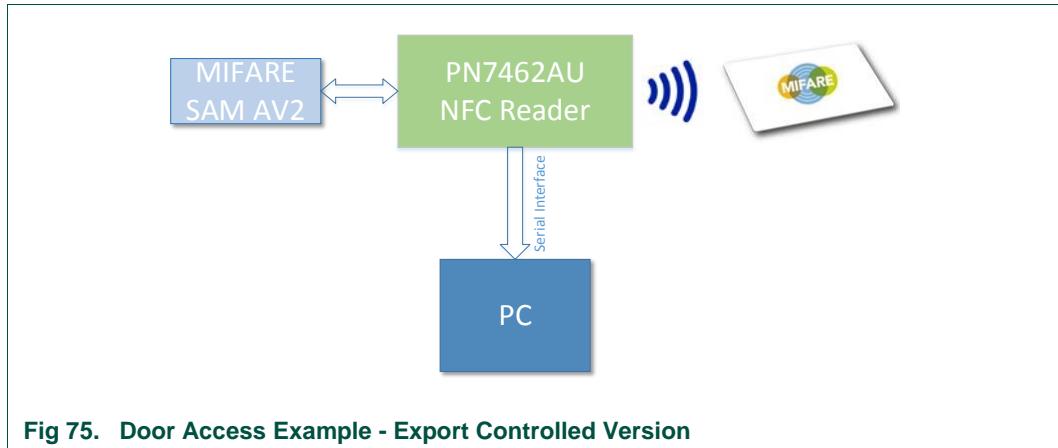


Fig 75. Door Access Example - Export Controlled Version

On power-up, NFC Reader starts polling for (PICC) cards (Type A, B or F, ISO15693, ISO18000-3M3) and if no card is present, the reader goes to standby mode. Timer is used as a wakeup source from standby - timer periodically every 500 ms. This process continues until a card is detected by the RF field of the reader. If a card is detected, the card type with its UID is sent via HSU & this is printed on the PC console

If a MIFARE DESFire EV1 card is detected, the reader tries to select a pre-written custom application on the card. It tries to authenticate the card using the key stored in SAM. If SAM is not present, then software keys can be used for authentication. If authentication is successful a block of data will be read from the card.

Note:

*Detailed description and how to use example is described in “Door Access User Manual”.
This example is available only with PSP package from NXP DocStore.*

7.16 PN7462AU_ex_phExNFCCcid

The NFC CCID is versatile demo application that features:

- Card detection for TypeA, TypeB, Felica, ISO15693, ISO18000p3m3 technologies
- Support for proprietary commands for MIFARE Classic, MIFARE UltraLight and MIFARE UltraLightC for read and write.
- CCID USB device protocol implementation. Supports the Suspend Resume and Wakeup Feature.
- Communication of the CLIF information with the PC using a PCSC application.
- P2P passive initiator mode. Supports LLCP Initiator Mode for sending the NDEF message to the mobile.

Demo setup for this application is the same as described in 7.10

7.17 PN7462AU_ex_phExMfCrypto

The PN7462AU_ex_phExMfCrypto demo application includes both CL and CT library components. Example is based on the Discovery Loop alongside Crypto layers and it is

intended to evaluate MIFARE DESFire card functionalities. Application performs following operations:

1. Application and Data and Value File creation inside the card.
2. AES authentication of the application.
3. Changing of the key.
4. Enciphered Read of Value File and Plain Read of Data File.
5. Enciphered Write of Value File and Plain write of Data File.
6. Supports Different Keys for Read and write.
7. CT part does not include any crypto example for CT but gives scope to include the CT example later

Example application trace in case when the application file is already created:

```
Entering Polling mode..
Type A Card - ISO14443-4A - UID : Len=7
    04 24 81 5A 47 21 80
Master Application of Desfire Card Selected,
Application A515A5 selected proceed for File Operations
APP Created By:
NxpNfcRdLib_v4.030.00.011627_2016
Value :   Len=4
    0D 00 00 00
Operation successful

Please remove the card.
```

Note:

This example is available only with PSP package from NXP DocStore.

7.18 PN7462AU_ex_phExRfPCDA

This example demonstrates simple low level API usage to perform detection, anti-collision, activation, authentication and R/W operation on the Type A cards according to ISO14443 and MIFARE standard.

Application is using low level Rf interface HAL implementation in Flash. There is limitation to only one card at the time. Supported TypeA cards are Type1 TOPAZ, MIFARE Ultralight, MIFARE Classic, MIFARE DESFire cards will pass through activation and anti-collision and. In the case of MIFARE Classic card also authentication with default key is demonstrated. In the case of MIFARE DESFire card L4 activation is demonstrated.

Application trace in case of MIFARE DESFire card is as follows:

```
Polling Start
Found TypeA
    DesFire R/W PASS : =106
    DesFire R/W PASS : =212
    DesFire R/W PASS : =424
```

8. Abbreviations

Table 18. Abbreviations

Acronym	Description
APDU	Application Protocol Data Unit
API	Application Programming Interface
CLIF	Contactless Interface
CRC	Cyclic Redundancy Code
CTIF	Contact Interface
EEPROM	Electrically Erasable Programmable Read Only Memory
FW	Firmware
GPIO	General-Purpose Input Output
HAL	Hardware Abstraction Layer
HSU	High Speed UART
HW	Hardware
LDO	Low Drop Out
MSD	Mass Storage Device
NFC	Near Field Communication
P2P	Peer to Peer
PCB	Printed Circuit Board
PAL	Protocol Abstraction Layer
PMU	Power Management Unit
PSP	Product Support Package
RF	Radio Frequency
ROM	Read Only Memory
RTOS	Real Time Operating System
SAM	Secure Access Module
SDA	Serial Data Signal
SPI	Serial Peripheral Interface
SPIM	SPI Master interface
SRAM	Static Random Access Memory
SW	Software
SWD	Serial Wire Debug
TXLDO	Transmitter Low Drop Out
USB	Universal Serial Bus

9. References

- [1] MCUXpresso webpage
<http://mcuxpresso.nxp.com/>
- [2] PN7462AU Datasheet
- [3] AN11706 PN7462 Antenna design guide
- [4] NFC-COCKPIT: NFC Cockpit configuration tool for NFC ICs
<http://www.nxp.com/products/:NFC-COCKPIT>
- [5] LPCXpresso board for LPC1769 with CMSIS DAP probe
<http://www.nxp.com/products/.OM13085>

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in the section 'Legal information'.