

# 12-bit 10 KSPS Incremental Delta-Sigma ADC in Skywater 130 nm

Raymond Yang and Yaqing Xia

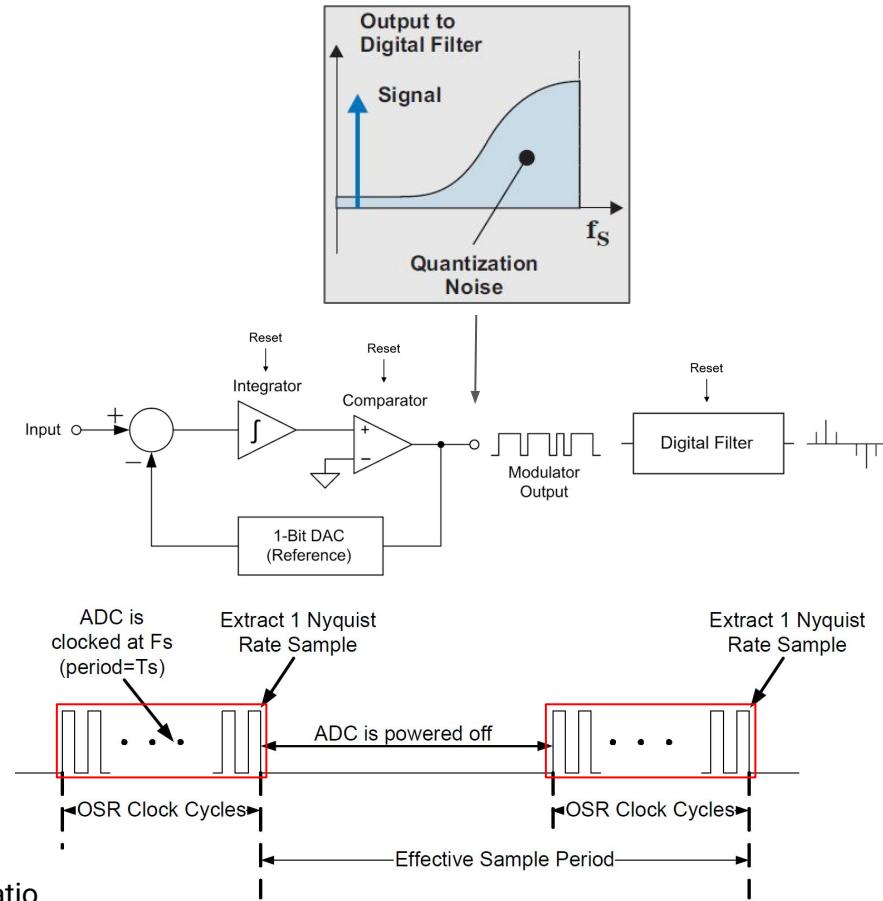
# Outline

- **Overview**
- Analog Modulator Design, Verification, and Layout
- Digital Filter Design, Verification, and Layout
- Summary & Future Plan

# Background

- Delta-Sigma modulator can achieve high in-band SQNR
- Simplified digital filter with IADC
- Instrumentation and sensor interface applications
- Reset of memory elements every conversion cycle — suitable for multiplexed applications with many channels

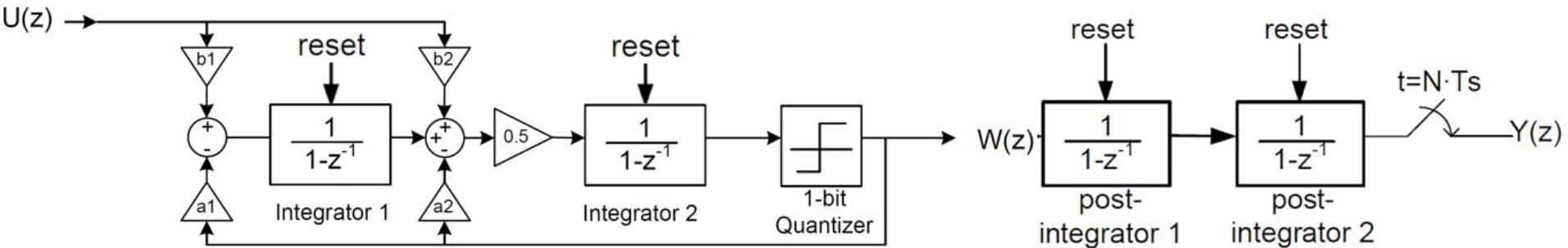
OSR = Oversampling Ratio



Source: Wu, Joseph. Delta-Sigma ADC Basics: Understanding the Delta-Sigma Modulator.  
Baker, Bonnie. How delta-sigma ADCs work. Texas Instruments Analog Applications Journal.  
Liang, Joshua. Master Thesis: A Frequency-Scalable 14-bit ADC for Low Power Sensor Applications.

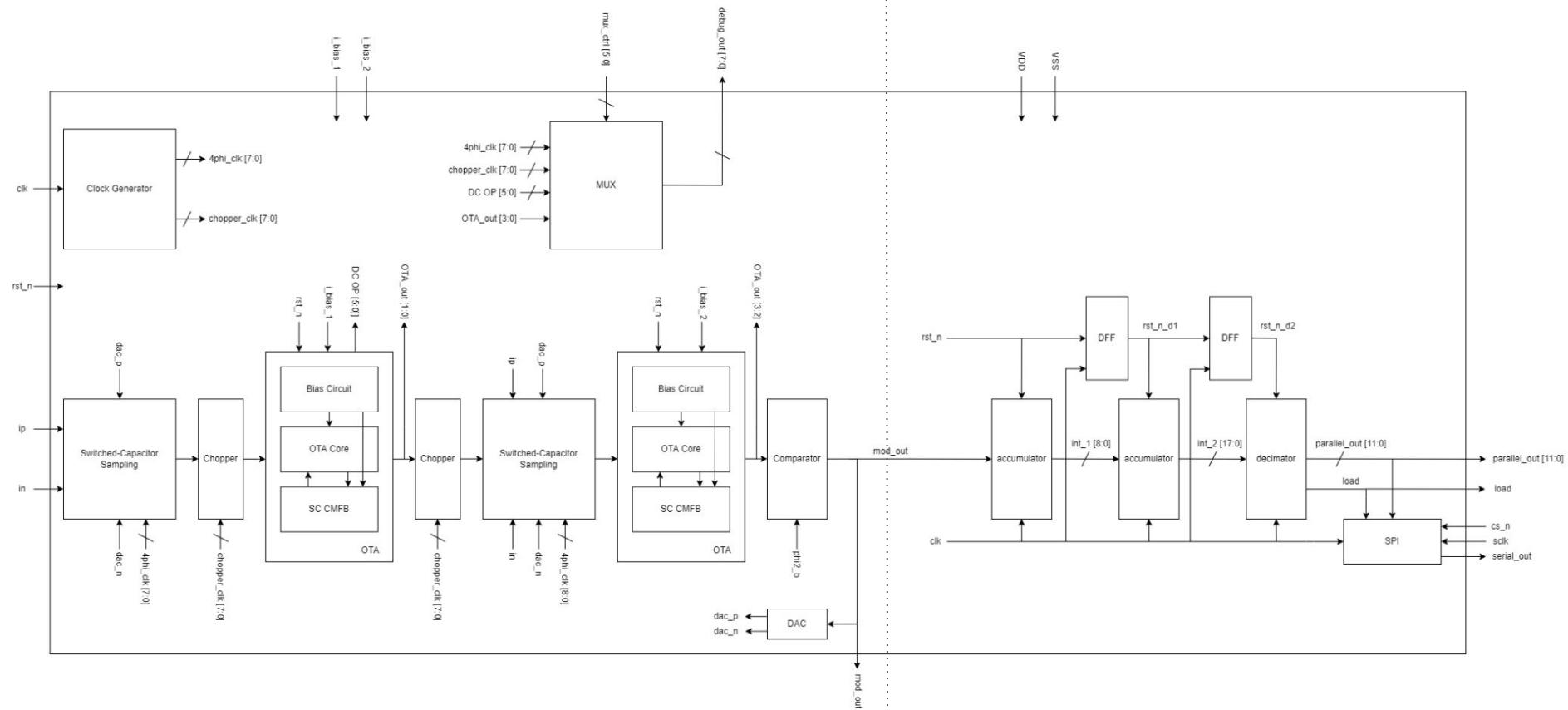
# Incremental ADC Architecture

- Second-order Incremental Modulator with 2 post-integrators
- Cascade of Integrators Feedback (CIFB) architecture to simplify timing and inputs to the quantizer
- Binary modulator output for linearity and simplified DAC circuit



# System-Level Block Diagram

Analog      Digital

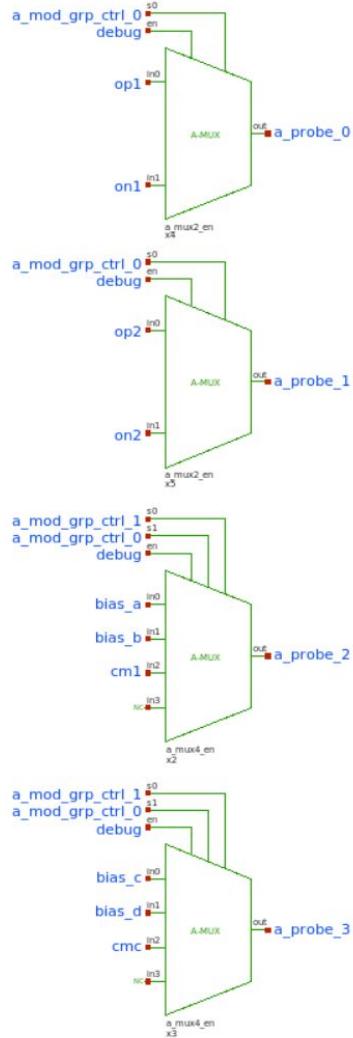
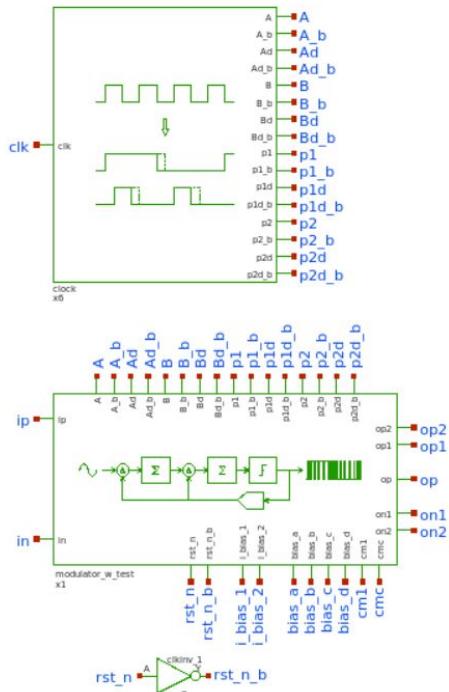
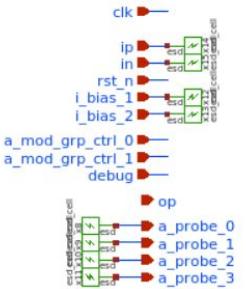


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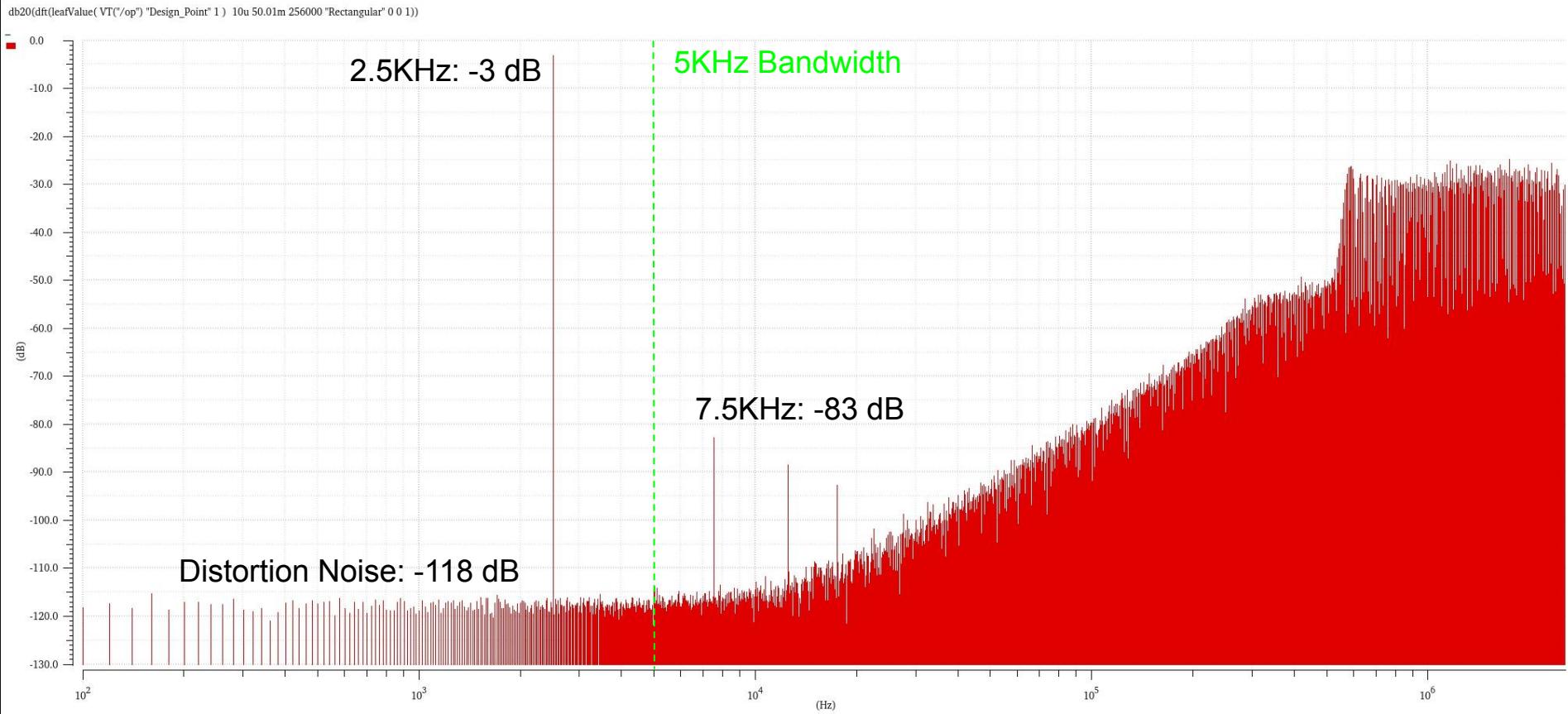
# Top-Level Modulator Schematic

- 4-phase Clock generator
- Second-order incremental modulator
- Analog Mux
- ESD protection on analog I/O pads

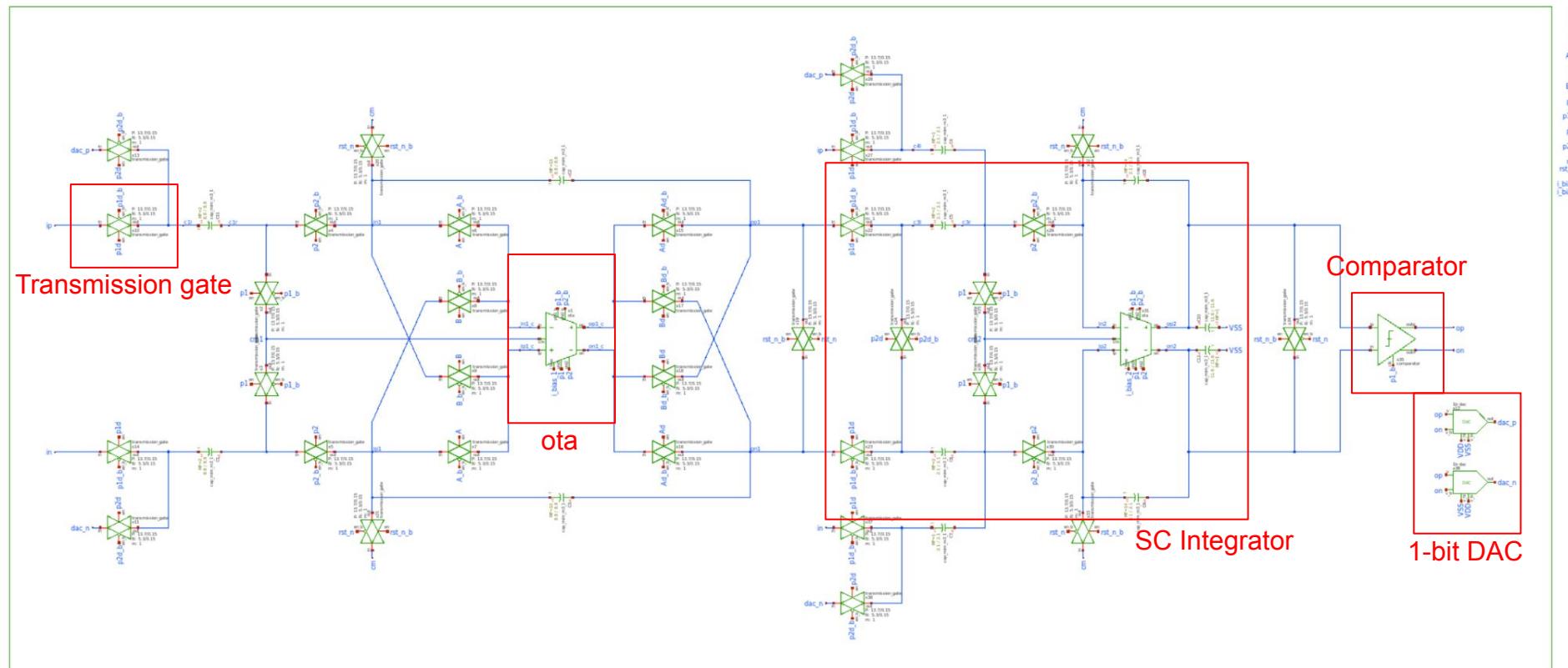


# Analog Top Schematic-Level Simulation

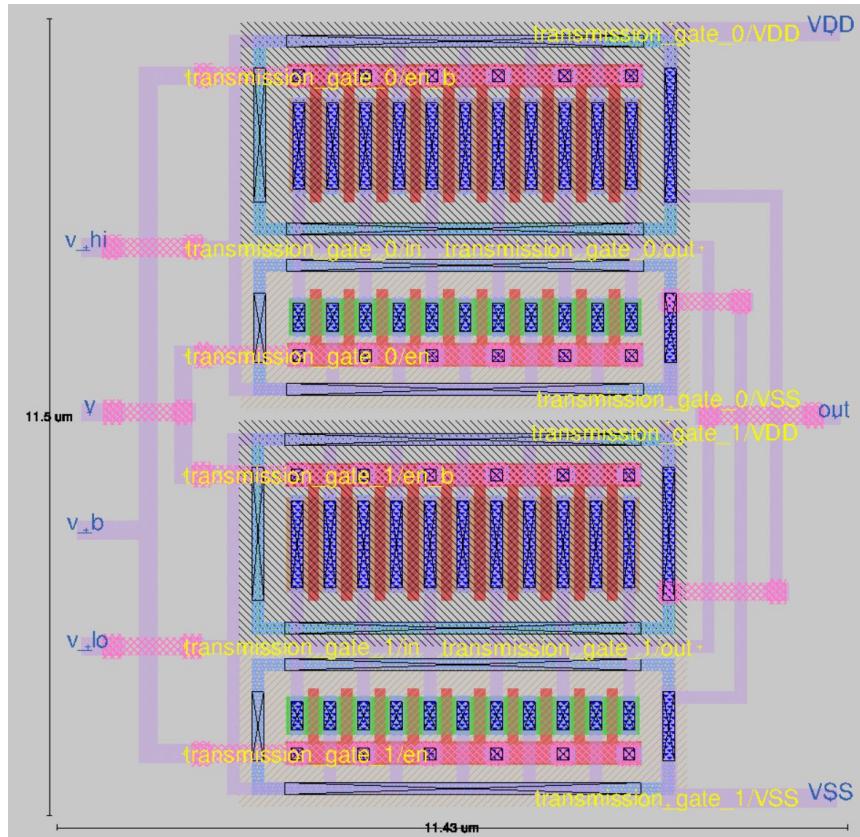
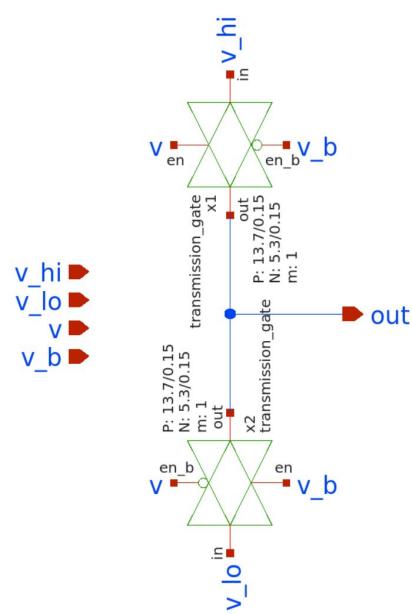
- Ran transient simulation from 10us to 50.01ms and took DFT with rectangular window. (RBW = 20 Hz)



# Modulator Schematic



# 1-bit DAC



- Negative feedback important for noise shaping
- Two transmission gates
- Multi-finger transistors layout to reduce parasitic capacitance and save area
- Layout dimensions about  $11.5\mu\text{m} \times 11.5\mu\text{m} = 132\mu\text{m}^2$

3. NMOS input differential pair (ota: AB)

-ABBAAB-

-BAABBA-

4. NMOS cascode (ota: ABCDEF; bias circuit: GHIJ)

-IIIIIIIIIIII--

-JIIIIIIIIIIII--

--IIIIIIIIIIIIJ-

--IIIIIIIIIIII-

-FFFFFFF--EEEEEE--HHHH--FFFFFFF--EEEEEE--

-HHHHH--EEEEEE--FFFFFFFFF--EEEEEE--HHHHH-

-EEEEEEE--FFFFF--HHHH--EEEEEE--FFFFF--

-AAABBBBBBAAAAAABBBBBBAAAAAABBBBBB-

-BBBAAAAAAABBBBBBAAAAAABBBBBBAAAAAA-

-AAABBBBBBAAAAAA--BBBBBBAAAAAAABBB-

-GDDDDDDGGCCCCC--DDDDDDGGCCCCCG-

-GGGDDCCDDCCDDCC--CCDDCCDDCCDDGG-

-GCCCCCCGGDDDDDD--CCCCCGGDDDDDG-

-BBBAAAAAAABBBBBB--AAAAAABBBBBBAAA-

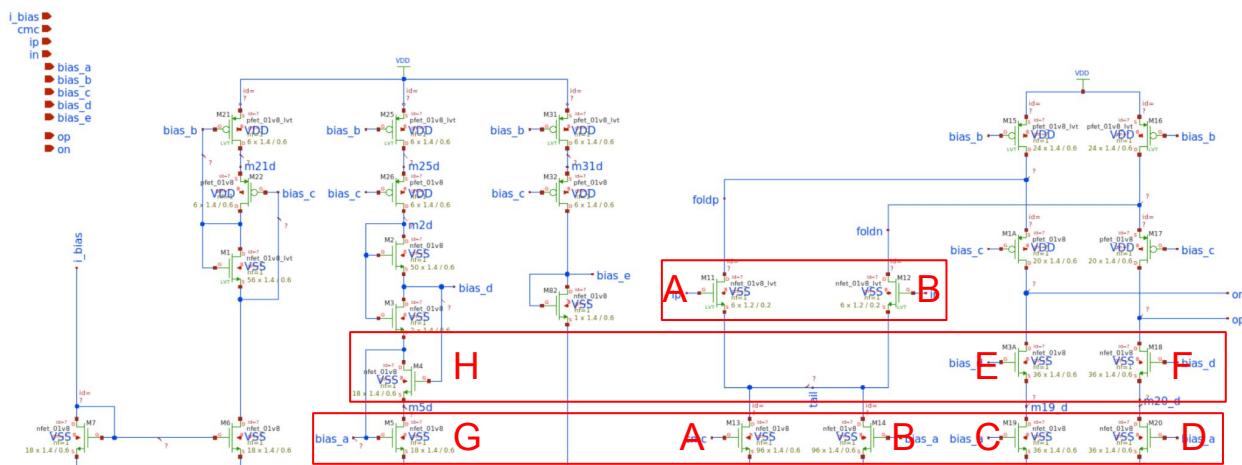
-AAAAAABBBBBBAAAAAABBBBBBAAAAAABBB-

-BBBBBAAAAAABBBBBBAAAAAABBBBBBAAA-

# OTA Layout Pattern

- 2D Common-centroid layout technique used to improve transistor matching and reduce gradient errors caused by process variation

- Dummy devices placed to maintain symmetry and improve matching. Dummy is electrically neutral.

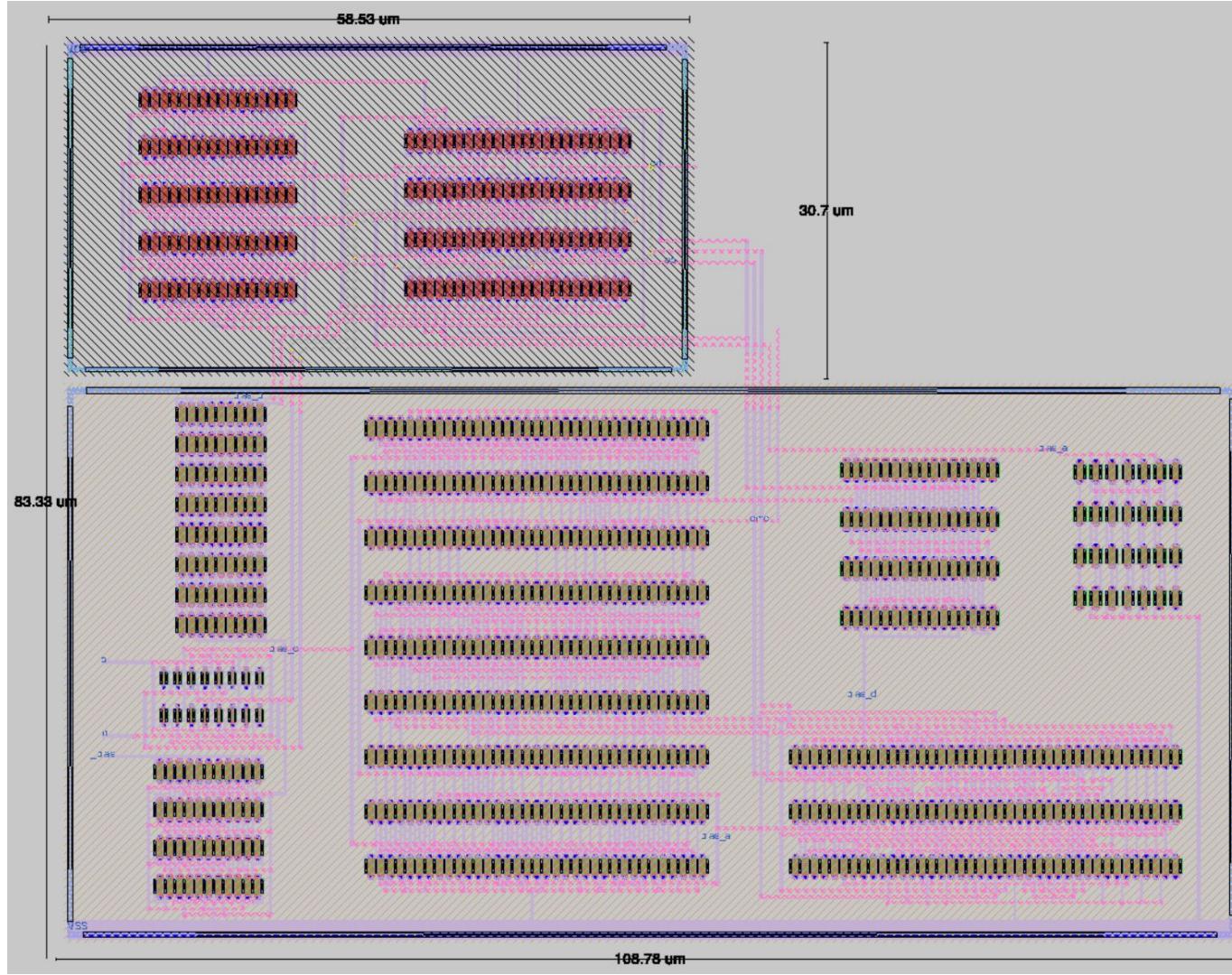


Match by Common-Centroid

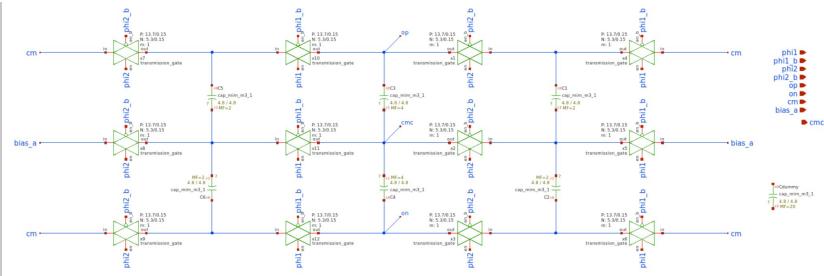
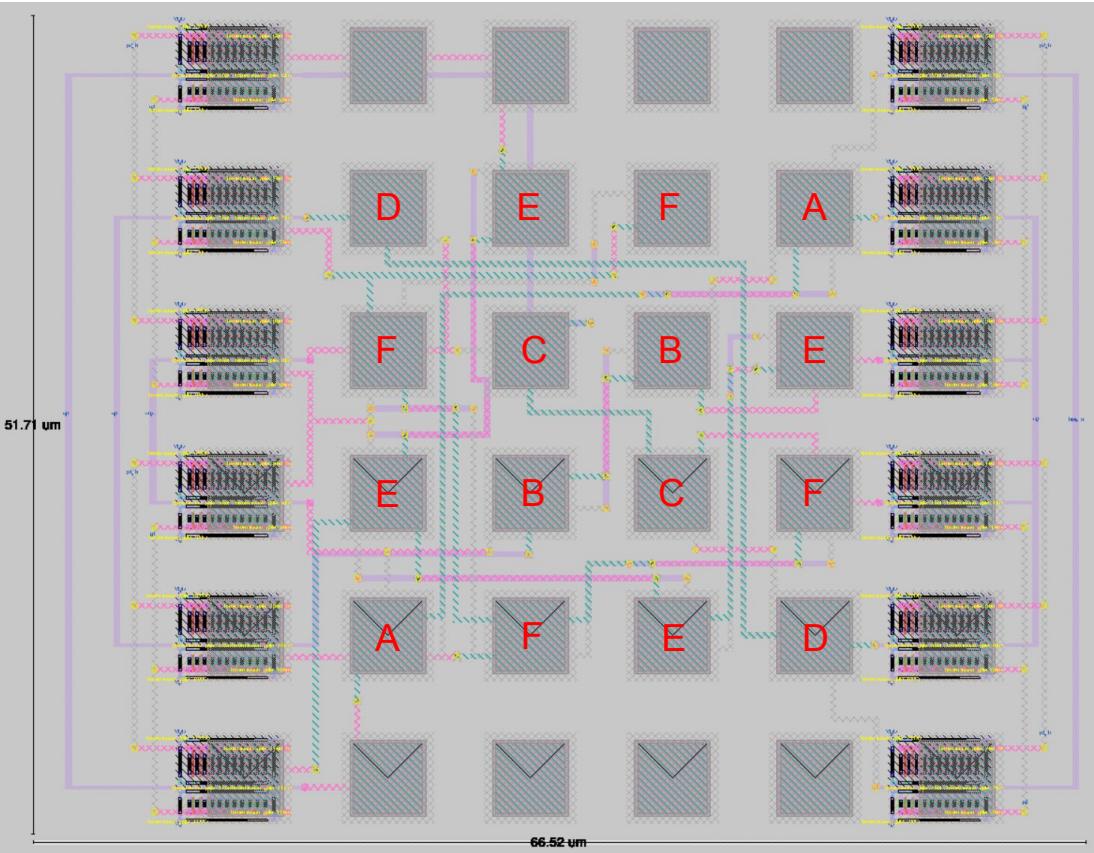
Performance Summary:  
AO = 53.7 dB  
PM = 70 deg  
fu = 344 MHz  
f3db = 750 KHz

# Bias Circuit & OTA

- Fully differential folded-cascode OTA
- Sooch cascode current mirror
- unit transistor size:  
 $W = 1.4\mu m, L = 0.6\mu m$
- Area:  $108\mu m \times 83\mu m$   
 $= 8964 \mu m^2$

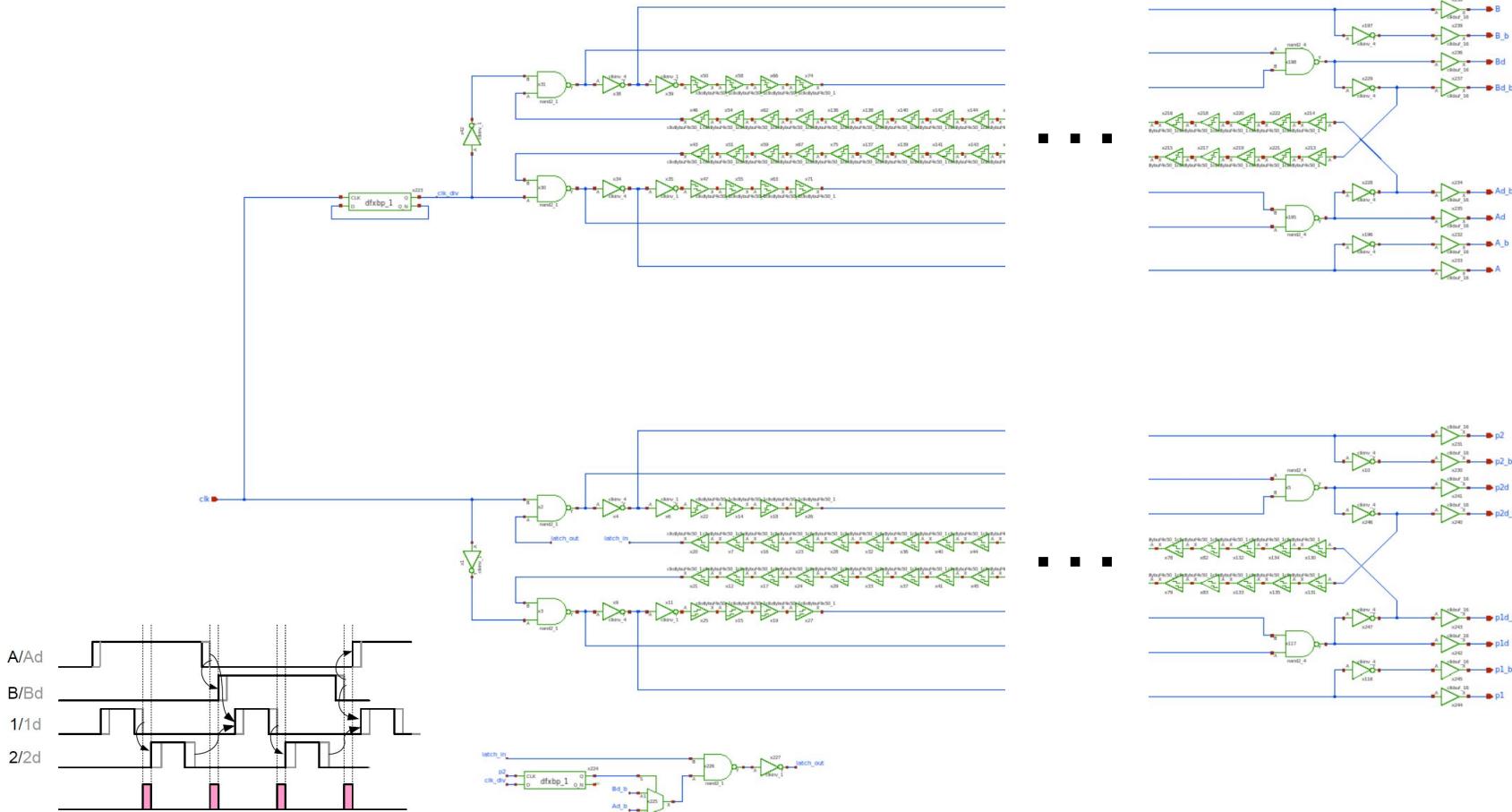


# Switched-Capacitor Common-mode Feedback

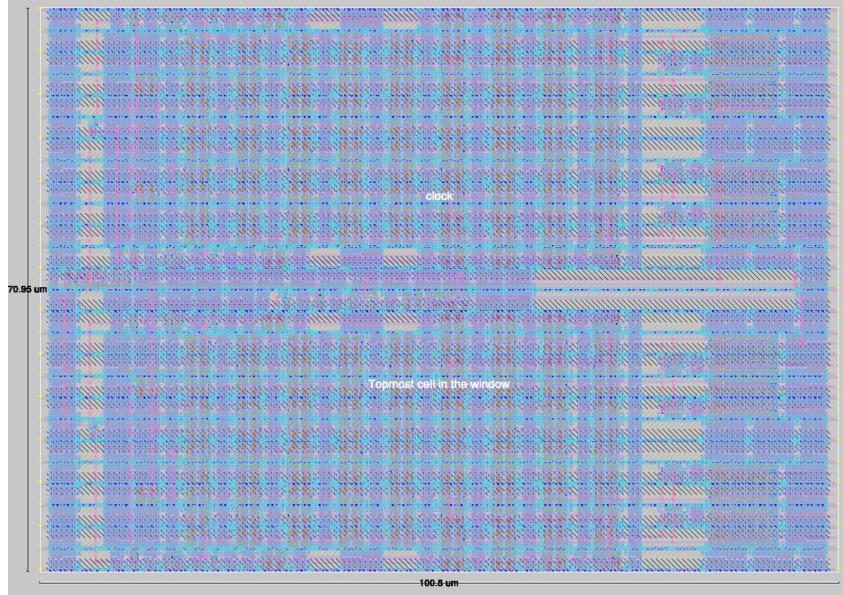


- 2D common centroid
- DEFA
- FCBE
- EBCF
- AFED
- Used unit and dummy caps
- Area =  $52\text{um} \times 67\text{um} = 3484\text{um}^2$

# 4-Phase Clock Generator

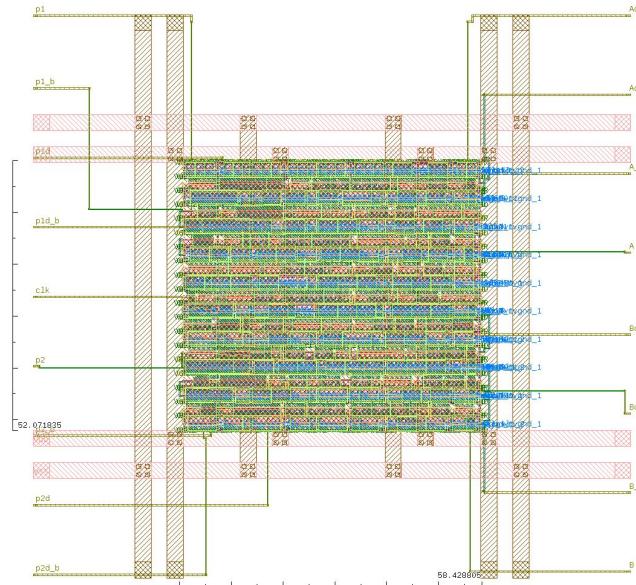


# 4-Phase Clock Generator



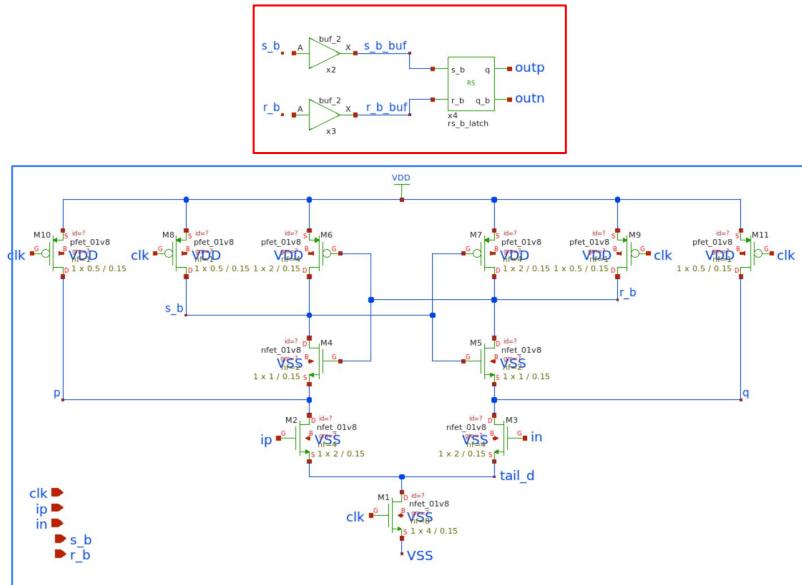
- Manual PnR
- Area:  $100\text{um} \times 71\text{um} = 7100\text{um}^2$
- Placed taps and decaps around each cell

Will run post-layout simulation for both, with manual pnr design as backup

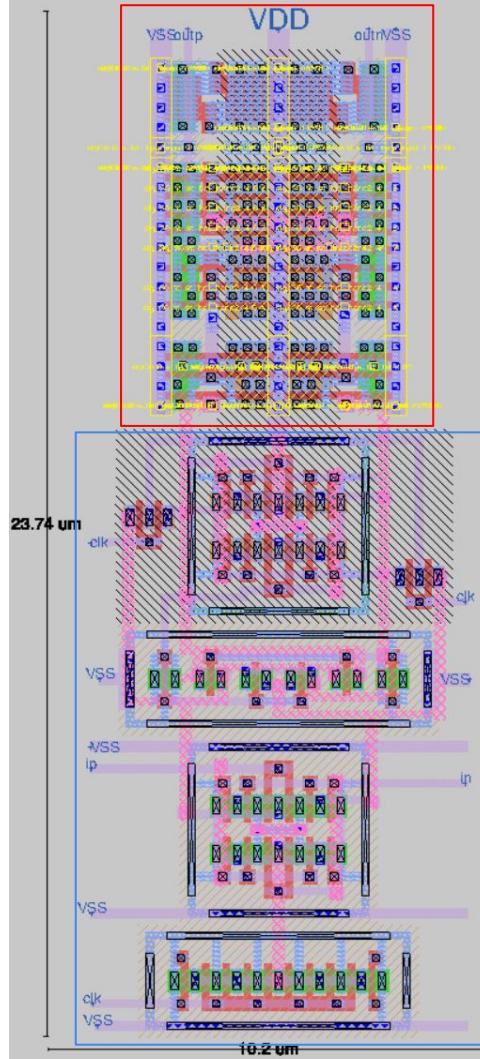


- Innovus PnR using gate-level netlist
- Area:  $53\text{um} \times 59\text{um} = 3127\text{um}^2$

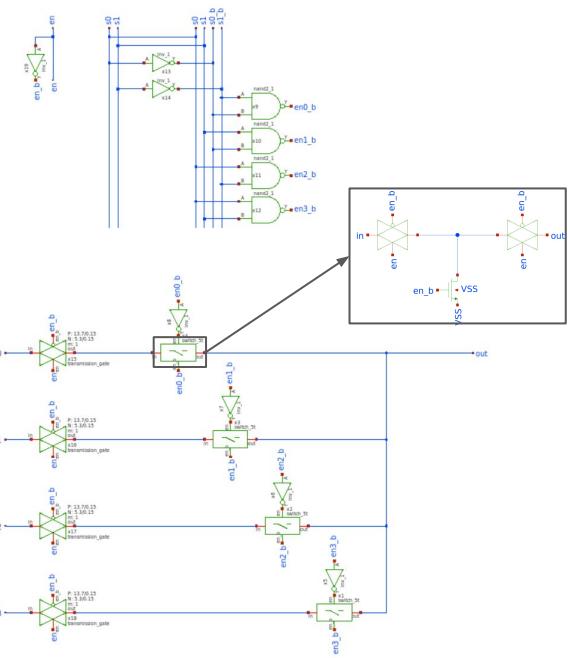
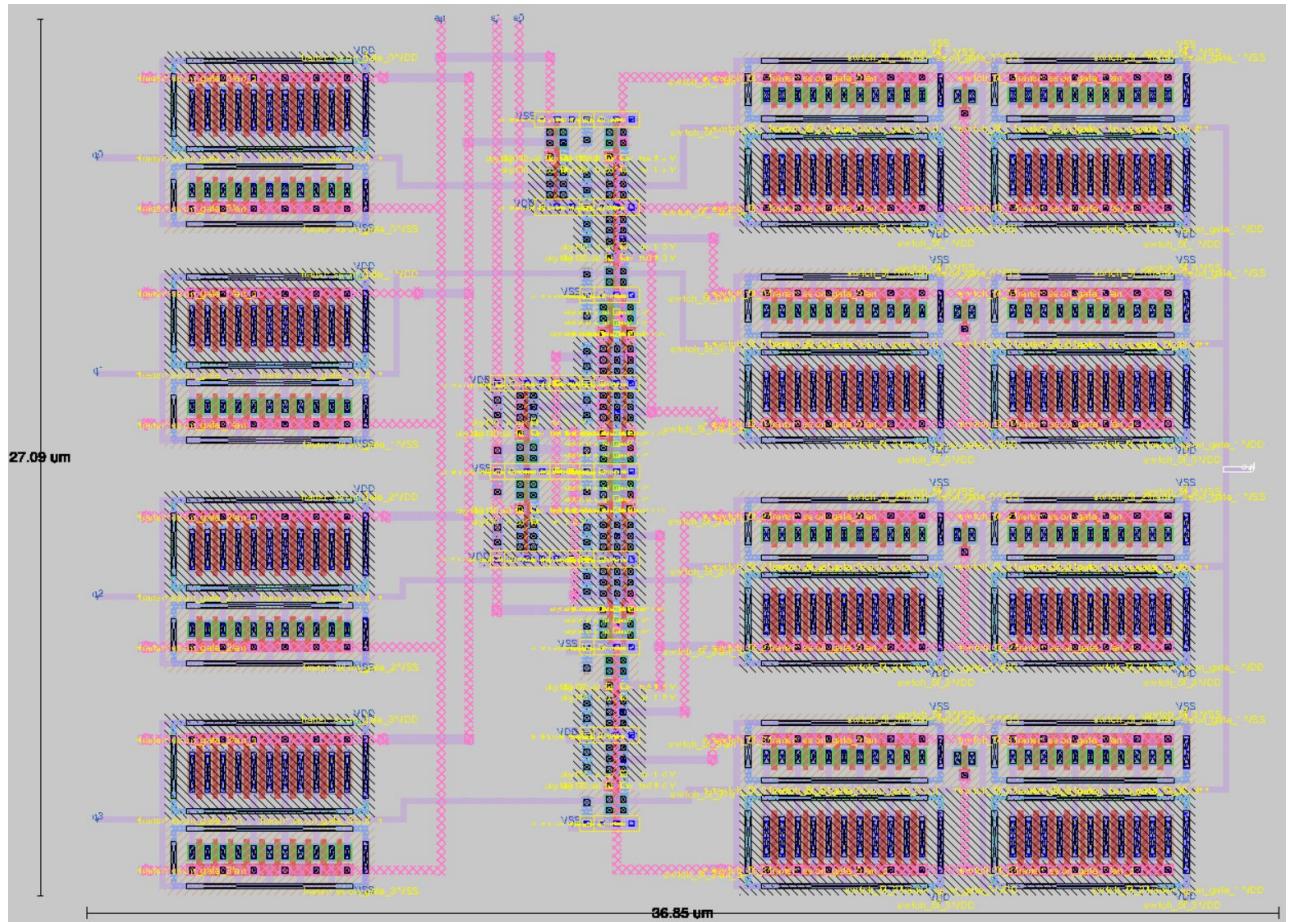
# Comparator



$$\text{Area: } 24\mu\text{m} \times 10\mu\text{m} = 240 \mu\text{m}^2$$



# 4-to-1 Analog MUX with Enable

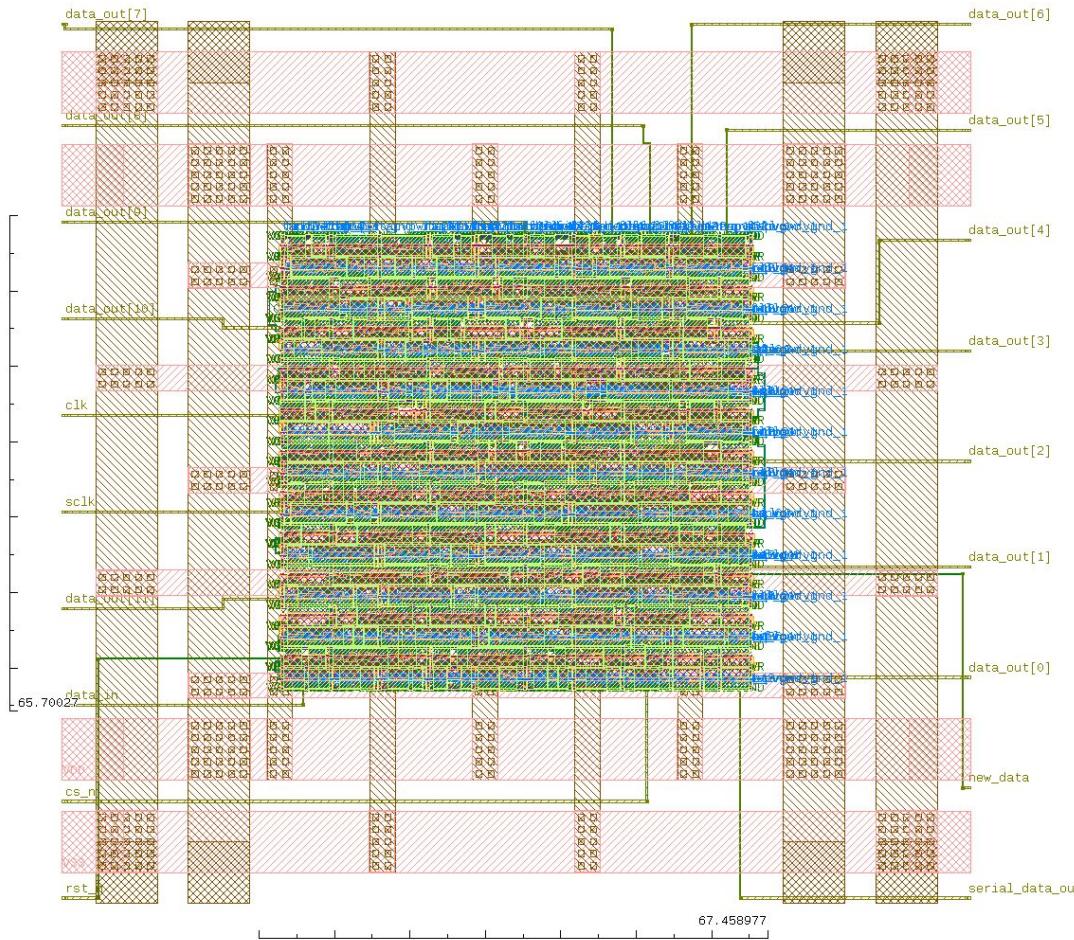


- Several fF of parasitic capacitance when off
- Area =  $27\text{um} \times 37\text{um} = 999\text{um}^2$

# Outline

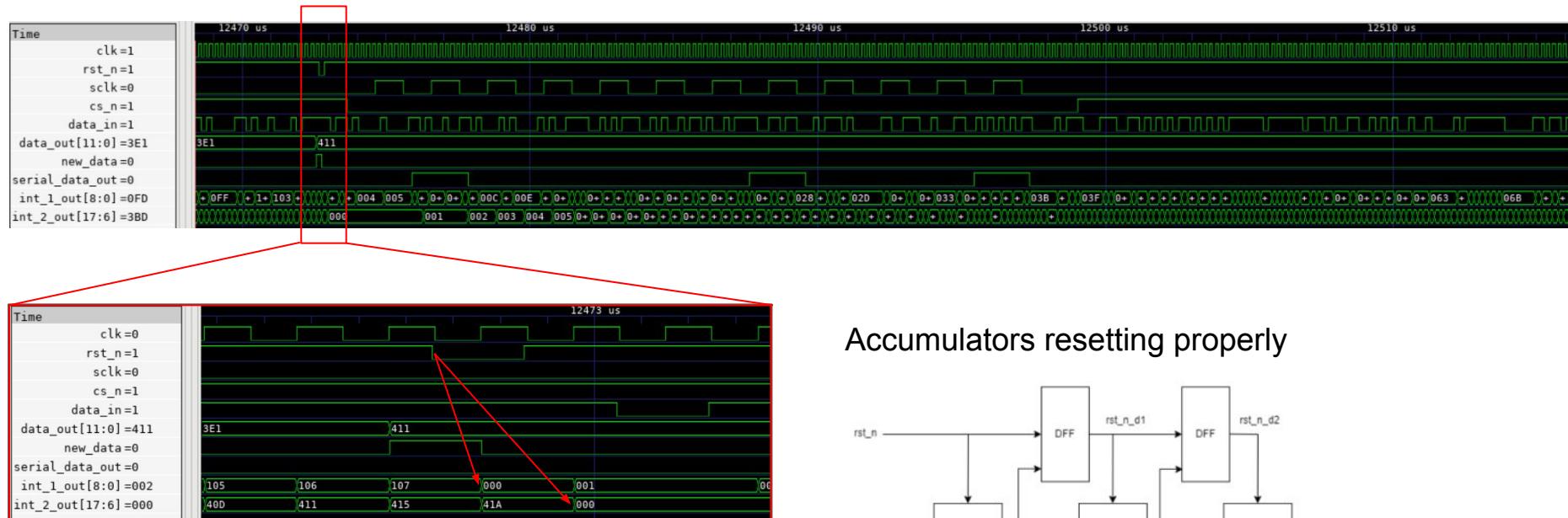
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# Digital Filter

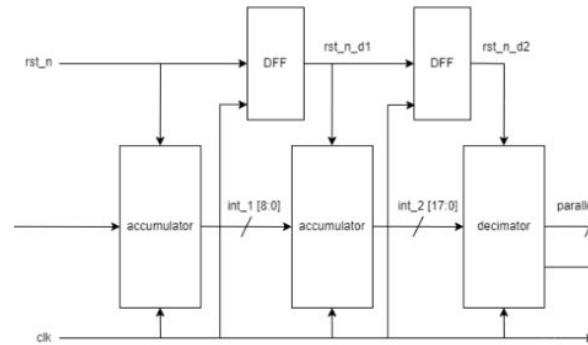


- 194 logic gates
- 65% core density
- Passed all checks, no violations
- 18 uW total power (75% clock network)
- Area = 66um x 68um = 4488um<sup>2</sup>

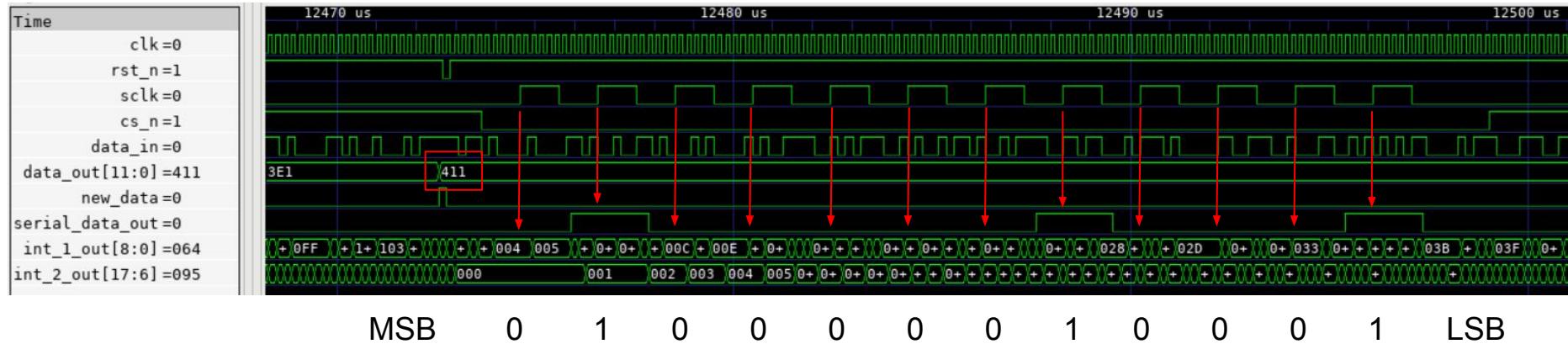
# Digital Filter Gate-Level Simulation



## Accumulators resetting properly



# Digital Filter Gate-Level Simulation



Matches 0x411

SPI works properly and serial data is correct.

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# Summary & Future Plan

## Done

- Analog modulator schematic top-level verification
- Digital filter full flow
- Debugging circuits
- Block level layout with DRC and LVS clean

## To Do

- Top-level layout
- Post layout simulation
- Integration into Caravel