In-Memory Logic Operations with 8T SRAM cells

Rahul Tiwari , Btech in ECE, Techno India Salt Lake, Kolkata

Abstract—**Processing in memory (PIM) aims at improving computational speed by bringing the computational engine to memory and avoid the energy consumption associated with existing von Neumann style of computing. Improve in compute ability by reduction in transistor size is approaching its limit, and with increase in compute intensive tasks involved with edge computing, IoT applications etc. we need to look for alternative techniques like – In/near memory computing. In this paper we will perform logical operations using 8TSRAM cells to overcome the von Neumann bottleneck.**

Keywords— In memory computing, SRAM, Inverter trip point

I. INTRODUCTION

SRAM is a commercially mature technology and is readily available in computing systems of all size and shapes, the SRAM based PIM approach can have a revolutionary impact on the computing industry's landscape.: (1) There have been attempts to perform operations in memory using 6TSRAM, however the use of PIM in 6TSRAM leads to severe reliability issues such as read-disturbance and degradation of read noise margins. Evidently realizing the full potential of SRAM-PIM requires novel and intelligent techniques. (2) Logical operations like NAND, NOR form the basic building block of all computational algorithms.

II. 8TSRAM CELL FOR IN MEMORY LOGIC

Operands A and B are written to the 8TSRAM cells by enabling Write word Line (WWL) and driving bit lines to 0 or 1. For writing 0, Write Bit Line (WBL) is driven to 0 while Write Bit Line compliment (WBLB) is driven to 1 by drive buffer circuits which provide low impedance paths. The Read Bit Lines (RBL) of the two cells which are 'wire NORed' are initially precharged. If Q=1, Qb=0, the RBL discharges otherwise it stays at its initial precharged condition.

NOR operation – The output of a NOR operation is '1' only if both the inputs are '0'. We activate both RWL1 and RWL2 corresponding to operands A and B. The precharged RBL line retains the precharged state if and only if both the bits Q corresponding to operands A and B are '0'. The output of INV2 mimics the NOR operation.

NAND operation- The output of a NAND operation is '0' only if both inputs are '1'. We activate both RWL1 and RWL2 corresponding to operands A and B. If any of the operands are 1, the RBL discharges. However, when both operands are 1, the rate of discharge is much faster than when one of the operands is 1. The duration of RWL1/RWL2 is decreased such that RBL does not discharge completely in case of 01/10. This leads to a difference in voltage levels on the RBL in the two cases (01/10 and 11) (Fig2). The trip point of the INV3 is chosen such that it goes high only for the case '11' Thus output of INV4 mimics the NAND operation.
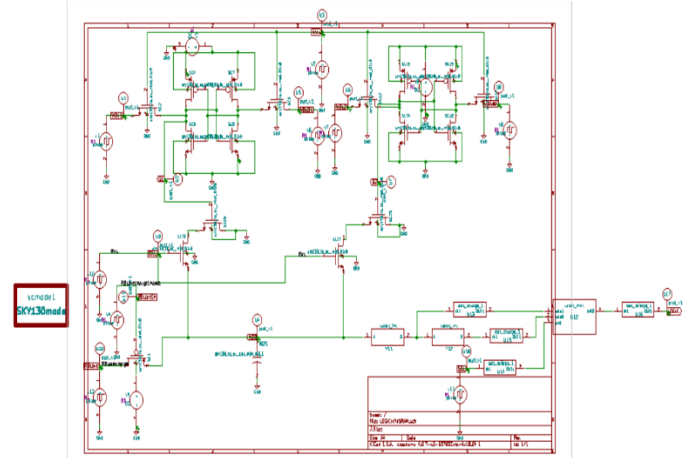

Fig 1. Circuit Schematic of the Design

III. SIMULATION

Fig 2. Simulation result displaying both NOR and OR operation while both 8TSRAM cells have 1 written to them.

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