

Boolean Algebra

- The Boolean Algebra called as mathematics of digital systems.
- It was developed by George Boole.
- It is used for the study and analysis of logic circuits.
- It is different from ordinary algebra and binary number system.

Boolean Algebra

OR Rule

$$x + 0 = x$$

$$x + 1 = 1$$

$$x + x = x$$

$$x + \bar{x} = 1$$

Boolean Algebra

AND Rules

$$x \cdot 0 = 0$$

$$x \cdot 1 = x$$

$$x \cdot x = x$$

$$x \cdot \bar{x} = 0$$

Boolean Algebra

Complementation Rule / NOT Rule

$$\overline{\overline{x}} = x$$

$$\overline{\overline{0}} = \overline{1} = 0$$

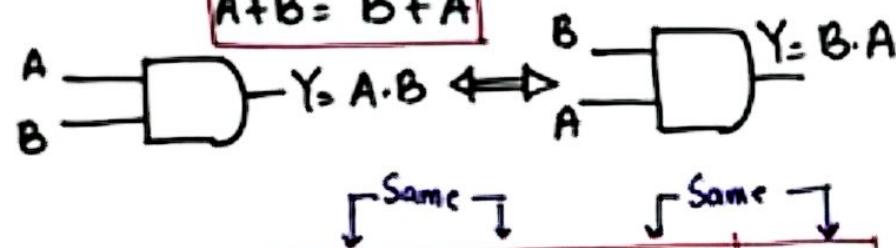
$$\overline{\overline{1}} = \overline{0} = 1$$

Boolean Laws:-

① Commutative Law:

$$\hookrightarrow A \cdot B = B \cdot A \text{ and}$$

$$A + B = B + A$$



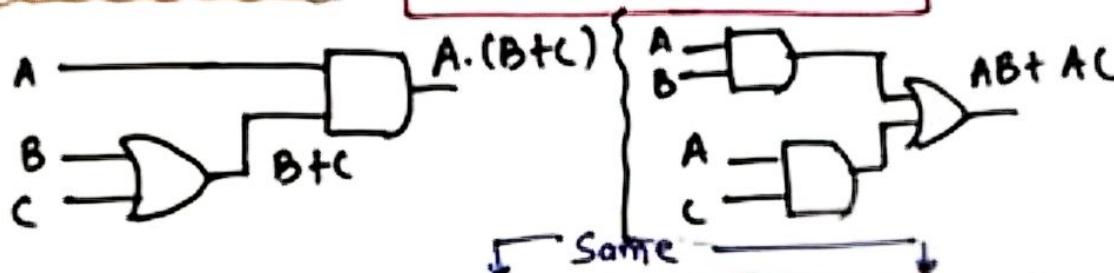
A	B	$A \cdot B$	$B \cdot A$	$A + B$	$B + A$
0	0	0	0	0	0
0	1	0	0	1	1
1	0	0	0	1	1
1	1	1	1	1	1

② Associative Law: O/p is not affected by pos'g of logical op's. $(A \cdot B) \cdot C = A \cdot (B \cdot C)$ = and $(A + B) + C = A + (B + C)$] Assignment = Same

A	B	C	$B \cdot C$	$A \cdot (B \cdot C)$	$A \cdot B$	$(A \cdot B) \cdot C$
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	0	1	0
1	1	1	1	1	1	1

(3) Distributive Law:-

$$A \cdot (B+C) = AB + AC$$



A	B	C	B+C	$A \cdot (B+C)$	AB	AC	$AB + AC$
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

(4) AND Laws:- AND operation is used.

$$\begin{aligned} &\hookrightarrow A \cdot 0 = 0 \quad \begin{matrix} 1 \cdot 0 = 0 \\ 0 \cdot 0 = 0 \end{matrix} \\ &\hookrightarrow A \cdot 1 = A \quad \begin{matrix} 0 \cdot 1 = 0 \\ 1 \cdot 1 = 1 \end{matrix} \\ &\hookrightarrow A \cdot A = A \quad \begin{matrix} 0 \cdot 0 = 0 \\ 1 \cdot 1 = 1 \end{matrix} \\ &\hookrightarrow A \cdot \bar{A} = 0 \quad \begin{matrix} 1 \cdot 1 = 1 \\ 1 \cdot 0 = 0 \\ 0 \cdot 1 = 0 \end{matrix} \end{aligned}$$

(5) OR Laws:- OR operation is used.

$$\begin{aligned} &\hookrightarrow A + 0 = A \quad \begin{matrix} 1 + 0 = 1 \\ 0 + 0 = 0 \end{matrix} \\ &\hookrightarrow A + 1 = 1 \quad \begin{matrix} 0 + 1 = 1 \\ 1 + 1 = 1 \end{matrix} \\ &\hookrightarrow A + A = A \quad \begin{matrix} 1 + 1 = 1 \\ 0 + 0 = 0 \end{matrix} \\ &\hookrightarrow A + \bar{A} = 1 \quad \begin{matrix} 0 + 1 = 1 \\ 1 + 0 = 1 \end{matrix} \end{aligned}$$

(6) Inversion Law: NOT operation .

$$\hookrightarrow \bar{\bar{A}} = A$$

Complement of a "Variable Complement" gives back the Variable.
 $A=0, \bar{A}=1, \bar{\bar{A}}=0 \quad] A=\bar{\bar{A}}$

7) other Important Laws/Rules:-

$$\hookrightarrow A + AB = A$$

$$A(1+B) \quad \left\{ 1+B=1 \right.$$

$$A \cdot (1) \quad \left\{ A \cdot 1 = A \right.$$

(A)

$$A + \bar{A}B = A + B$$

L.H.S. $A + \bar{A}B$

Since, $A = A + AB$

$$= A + AB + \bar{A}B$$

$$= A + B(A + \bar{A}) \quad \left\{ A + \bar{A} = 1 \right.$$

$$= A + B \cdot (1) \quad \left\{ B \cdot 1 = B \right.$$

$$= A + B$$

$$(A+B)(A+C) = A+BC$$

$$\left. \begin{aligned} & \hookrightarrow A \cdot A + A \cdot C + B \cdot A + B \cdot C \\ & \qquad \qquad \qquad \left. \begin{aligned} A \cdot A = 1 \\ B \cdot A = A \cdot B \end{aligned} \right\} \end{aligned} \right\}$$

$$\left. \begin{aligned} & \hookrightarrow A + AC + \underline{AB} + BC \\ & \qquad \qquad \qquad \left. \begin{aligned} A + AB = A \end{aligned} \right\} \end{aligned} \right\}$$

$$\hookrightarrow A + AC + BC$$

$$\left. \begin{aligned} & \hookrightarrow A(1+C) + BC \\ & \qquad \qquad \qquad \left. \begin{aligned} (1+C) = 1 \end{aligned} \right\} \end{aligned} \right\}$$

$$\hookrightarrow A + BC$$

Boolean Algebra Theorems:-

① Duality Principle:- In two valued Boolean Algebra, dual of algebraic expression can be obtained simply by interchanging 'OR' and 'AND' operators and by replacing 1s by 0s and vice-versa.

$$\hookrightarrow \text{OR} \curvearrowright \text{AND}, \text{AND} \curvearrowright \text{OR}, 0 \xrightarrow{1} 1 \xrightarrow{0}$$

$$A \cdot 0 = 0 \rightarrow (A+1) = 1$$

$$(A+B) \cdot (A+C) \rightarrow AB + A \cdot C$$

$$\hookrightarrow A(B+C)$$

Ques:- Find dual of following Boolean Expressions:

(i) $A + AB = A$

$$\hookrightarrow A \cdot (A+B) = A$$

$$A + \bar{A} = 1$$

$$A \cdot \bar{A} = 0$$

(ii) $A + \bar{A}B = A + B$

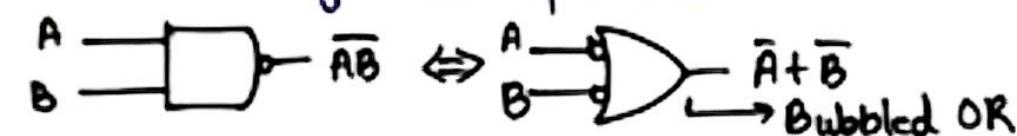
$$\hookrightarrow A \cdot (\bar{A} + B) = A \cdot B$$

(iii) $(A+B)(A+C) = A + BC$

$$\hookrightarrow (AB) + (AC) = A \cdot (B+C)$$

De-Morgan's theorem:-

Theorem 1:- Complement of a product is equal to addition of the complements. $\overline{AB} = \overline{A} + \overline{B}$

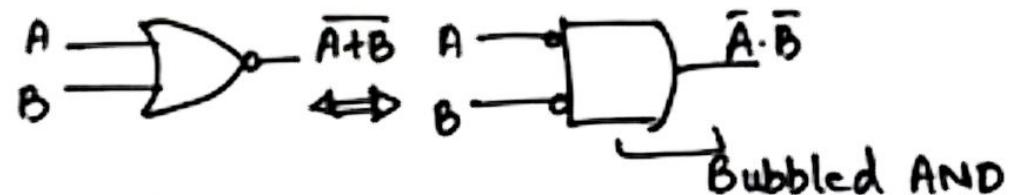


TRUTH TABLE:-

A	B	AB	\overline{AB}	\overline{A}	\overline{B}	$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Hence Verified

Theorem 2: Complement of a sum is equal to the product of complements. $\overline{A+B} = \overline{A} \cdot \overline{B}$



Truth Table:-

A	B	$A+B$	$\overline{A+B}$	\overline{A}	\overline{B}	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Simplify $Z = \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + ABC$

$$Z = BC(\bar{A} + A) + \bar{B}\bar{C}(A + \bar{A}) + A\bar{B}C$$

$$Z = BC + \bar{B}\bar{C} + A\bar{B}C$$

$$Z = BC + \bar{B}(\bar{C} + AC)$$

$$x + \cancel{\bar{x}}y = x + y$$

or

$$\bar{x} + xy = \bar{x} + y$$

$$\text{Simplify } Z = \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + ABC$$

$$Z = BC(\bar{A} + A) + \bar{B}\bar{C}(A + \bar{A}) + A\bar{B}C$$

$$Z = BC + \bar{B}\bar{C} + A\bar{B}C$$

$$Z = BC + \bar{B}(\bar{C} + AC)$$

$$Z = BC + \bar{B}(\bar{C} + A)$$

$$Z = BC + \bar{B}\bar{C} + A\bar{B}$$

$$BC + \bar{B}\bar{C} = 1 \times$$

$$BC + \bar{B}\bar{C} = 1 \checkmark$$

1

Ques1:- Prove following Boolean expressions:

$$(i) A + AB = A$$

$$\textcircled{1} \quad A + AB = A$$

$$(ii) A + \bar{A}B = A + B$$

$$A(1+B) \quad] 1+B=1$$

$$A.(1) \quad] A \cdot 1 = A$$

$$\textcircled{A} = \underline{\underline{R.H.S}}$$

$$(2) L.H.S = A + \bar{A}B$$

$$= A + AB + \bar{A}B \quad] \text{replace } A \text{ with } \underline{\underline{A+AB}}$$

$$= A + B(A + \bar{A}) \quad] (A + \bar{A}) = 1$$

$$= A + B \cdot (1) \quad] B \cdot 1 = B$$

$$= \textcircled{A+B} \quad \underline{\underline{R.H.S}}$$

Ques2:- Prove that

$$(A + \bar{B}) + AB = A + \bar{B}$$

$$(A + AB = A) \quad [\text{we know that}]$$

$$L.H.S = (A + \bar{B})(A + \bar{B})(\bar{A}B)$$

$$= (AA + A\bar{B} + \bar{B}A + \bar{B}\bar{B})(\bar{A}B) \quad] \begin{array}{l} A \cdot A = A \\ \bar{B}\bar{B} = \bar{B} \end{array}$$

$$= (A + A\bar{B} + \bar{B})(\bar{A}B)$$

$$= (A[1 + \bar{B}] + \bar{B})(\bar{A}B) \quad] 1 + \bar{B} = 1$$

$$= (A + \bar{B})(\bar{A}B)$$

$$= A\bar{A}B + \bar{B}\bar{A}B \quad] \begin{array}{l} A \cdot \bar{A} = 0 \rightarrow 0 \cdot B \rightarrow 0 \\ \bar{B} \cdot \bar{B} = 0 \rightarrow 0 \cdot \bar{A} \rightarrow 0 \end{array}$$

$$= 0 + 0$$

$$= \textcircled{0} \quad \underline{\underline{R.H.S}}$$

$$A\bar{B} + A\bar{B} = A\bar{B}$$

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- Let, $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$ where x_1, x_2, x_3, x_4 are Boolean variables, and \oplus is the XOR operator.

Which one of the following must always be TRUE?

- (A) $x_1 x_2 x_3 x_4 = 0$ ①
- (B) $x_1 x_3 + x_2 = 0$
- (C) $x'_1 \oplus x'_3 = x'_2 \oplus x'_4$
- (D) $x_1 + x_2 + x_3 + x_4 = 0$

$$x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$$

$$1 \oplus 1 \oplus 1 \oplus 1 = 0$$

$$x_1 = 1, x_2 = 1, x_3 = 1, x_4 = 1$$

$$x_1 x_3 + x_2 = 1$$

$$x'_1 \oplus x'_3 = 1 \quad x'_2 \oplus x'_4$$

$$0 \oplus 0 = 0 \oplus 0$$

$$0 \neq 0$$

Q.5

The simplification of the Boolean expression $(\overline{\overline{ABC}}) + (\overline{ABC})$ is

- (A) 0
(C) A

- (B) 1
(D) BC

Ans: B

The Boolean expression is $(\overline{\overline{ABC}}) + (\overline{ABC})$ is equivalent to 1

$$\begin{aligned}(\overline{\overline{ABC}}) + (\overline{ABC}) &= \overline{\overline{A}} + \overline{B} + \overline{\overline{C}} + \overline{A} + \overline{\overline{B}} + \overline{\overline{C}} = A + \overline{B} + C + \overline{A} + B + \overline{C} \\&= (A + \overline{A})(B + \overline{B})(C + \overline{C}) = 1 \times 1 \times 1 = 1\end{aligned}$$

Q.1

The NAND gate output will be low if the two inputs are

(A) 00

(B) 01

(C) 10

(D) 11

Ans: D

The NAND gate output will be low if the two inputs are 11

(The Truth Table of NAND gate is shown in Table.1.1)

X(Input)	Y(Input)	F(Output)
0	0	1
0	1	1
1	0	1
1	1	0

Table 1.1 Truth Table for NAND Gate

eup

$$A \cdot (A+B) = A$$

$$R' \cdot R = 0$$

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$$A+BC = (A+B)(A+C)$$

If P, Q, R are Boolean variables, then $(P + Q')(PQ' + PR)(P'R' + Q')$ simplifies

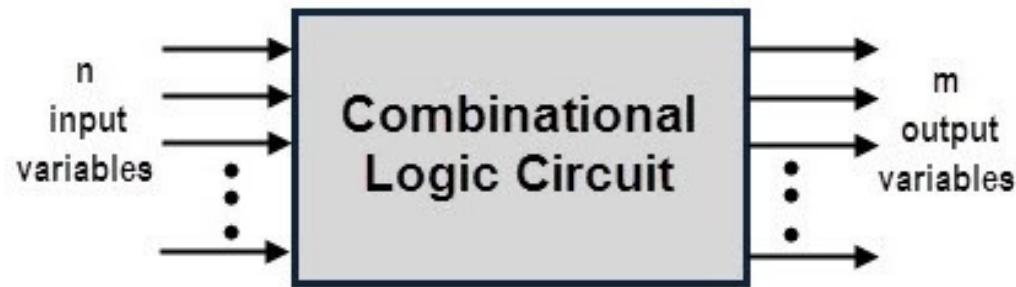
- (A) PQ'
- (B) PR'
- (C) $PQ' + R$
- (D) $PR' + Q$

$$\begin{aligned} & (P + Q') (\underline{PQ'} + \underline{PR})(P'R' + Q') \\ &= (P + Q') P (Q' + R) (Q' + P'R') \\ &= (P + Q') P (Q' + P'R' \cancel{\cdot R}) \\ &= P (P + Q') \cdot Q' \\ &= \underline{P \cdot Q'} \end{aligned}$$

Combinational Circuit

Definition

- Combinational logic circuits are memoryless digital logic circuits whose output at any instant depends only on the combination of its inputs
- It can have any number of in/outputs.

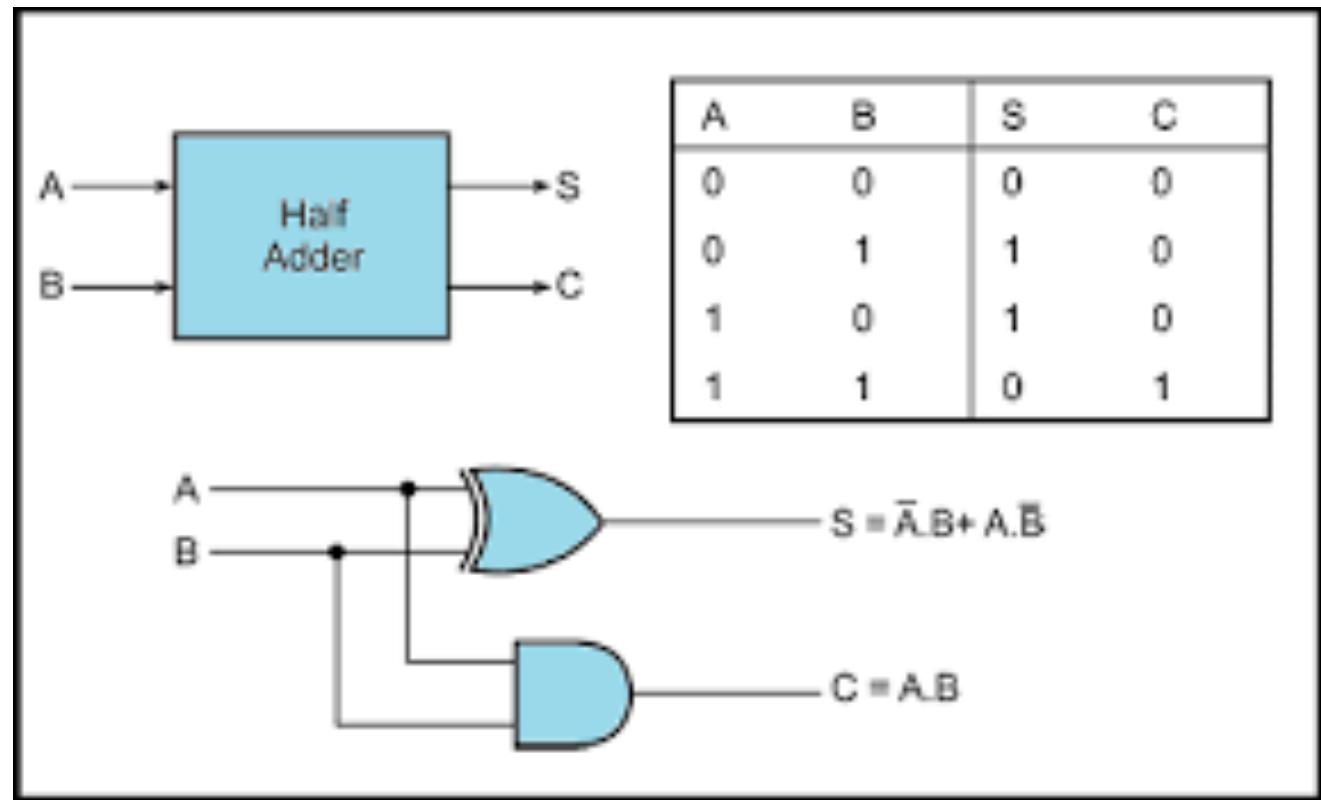


Binary Adder

- Performs addition of binary numbers
- IO: 2 or more bits, OU: sum and carry
- Types:
 - Half adder
 - Full adder

Half Adder

- Adds two inputs and produces sum and carry as output



Half adder

- K Map ad circuit diagram

For Sum :-

\bar{A}	\bar{B}	0	1
\bar{A}	B	0	1
A	\bar{B}	0	1

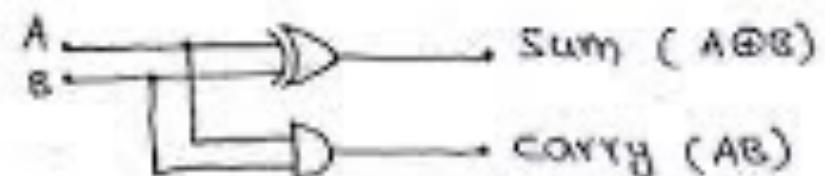
$$\therefore \text{Sum} = \bar{A}B + A\bar{B}$$
$$= A \oplus B$$

For carry :-

\bar{A}	\bar{B}	0	1
\bar{A}	B	0	1
A	\bar{B}	0	1

$$\therefore \text{carry} = AB$$

Logic circuit :-

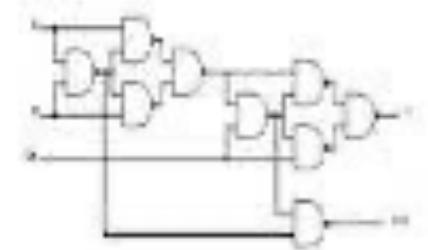


Full Adder

- Full Adder is the adder that adds three inputs and produces two outputs which consist of two EX-OR gates, two AND gates, and one OR gate. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

Full Adder
Truth
Table

Inputs			Outputs	
A	B	C _{in}	C _{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Full Adder

- K map and expression

For Sum

A\B\c	00	01	11	10
0	0	1	1	0
1	1	0	0	1

$$\begin{aligned}\text{Sum} &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + ABC \\ &= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}C + BC) \\ &= \bar{A}(B \oplus C) + A(\overline{B \oplus C}) \quad (\because \bar{x}y + x\bar{y} = x \oplus y) \\ &= A \oplus B \oplus C\end{aligned}$$

For Carry

A\B\c	00	01	11	10
0	0	0	1	0
1	0	1	0	1

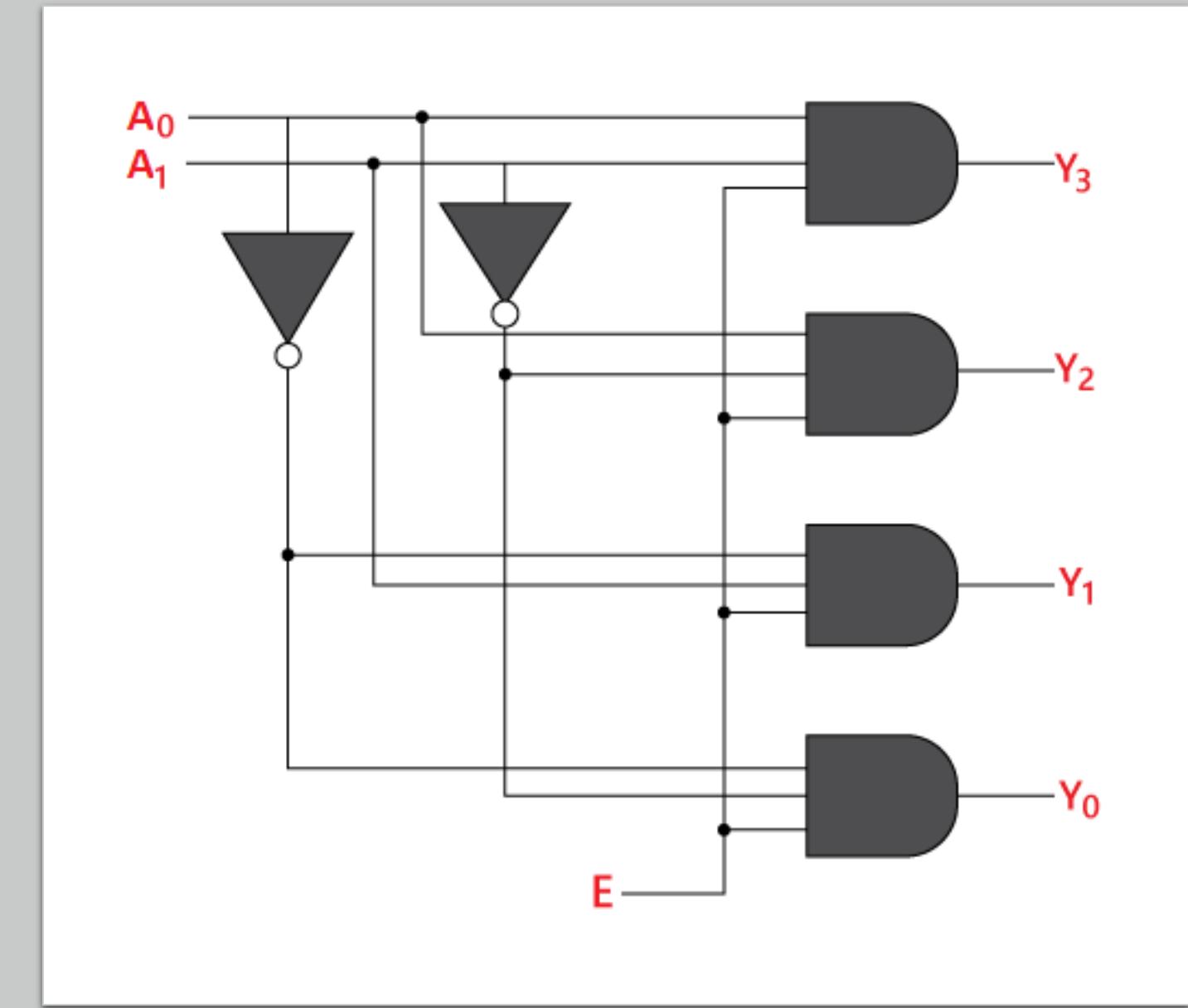
$$\text{Carry} = AB + BC + AC$$

Decoder

- Takes binary input in N lines and returns output in 2^N lines
 - 2 to 4
 - 3 to 8
 - 4 to 16

2 to 4

- In the 2 to 4 line decoder, there is a total of three inputs, i.e., A_0 , and A_1 and E and four outputs, i.e., Y_0 , Y_1 , Y_2 , and Y_3 . For each combination of inputs, when the enable 'E' is set to 1, one of these four outputs will be 1.



2 to 4

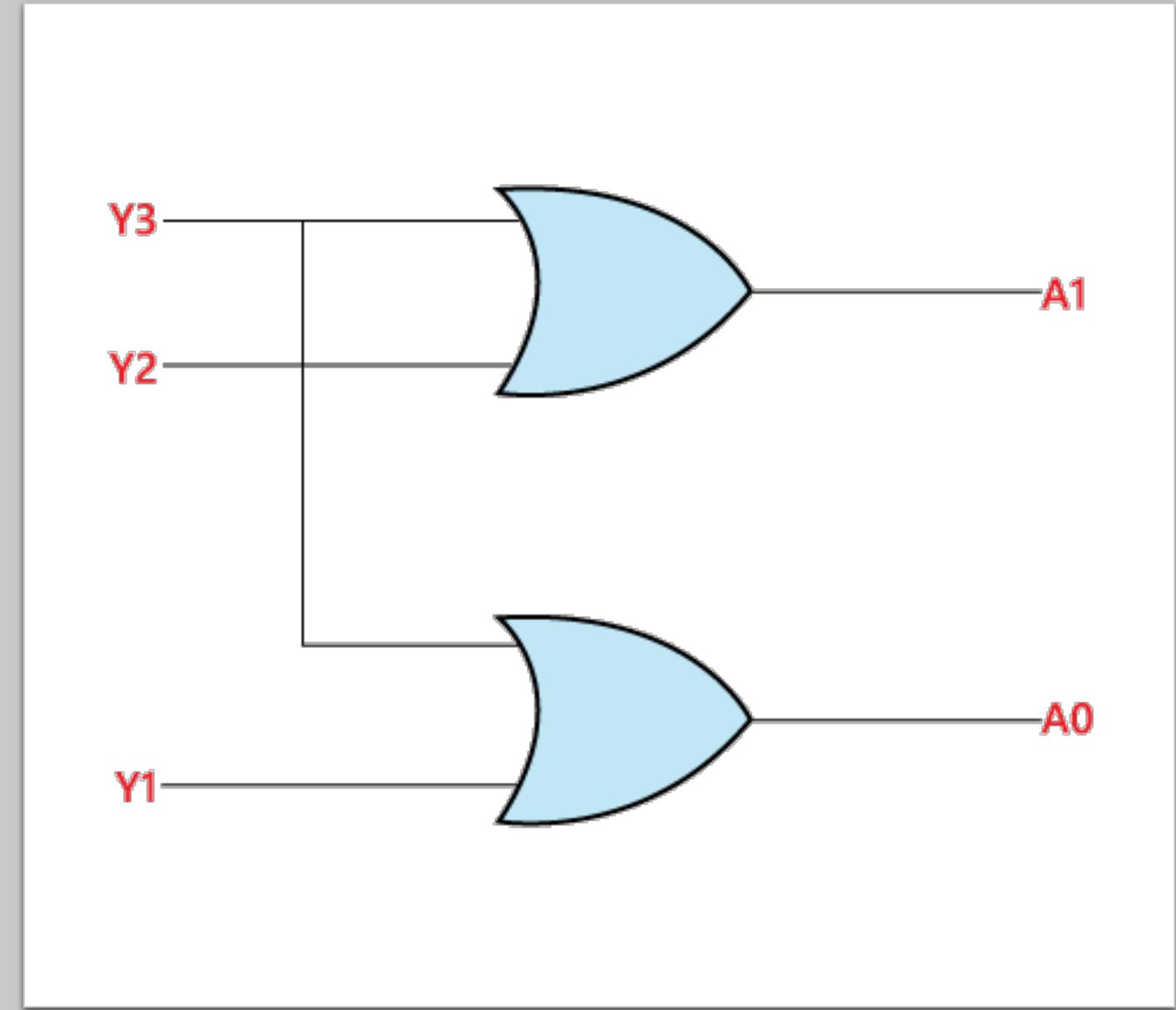
Enable	INPUTS		OUTPUTS			
	A ₁	A ₀	Y ₃	Y ₂	Y ₁	Y ₀
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Encoder

- Change 2^N input to N output
- Exact opposite of decoder
 - 4 to 2
 - 8 to 3

4 to 2 Encoder

- In 4 to 2 line encoder, there are total of four inputs, i.e., Y_0 , Y_1 , Y_2 , and Y_3 , and two outputs, i.e., A_0 and A_1 . In 4-input lines, one input-line is set to true at a time to get the respective binary code in the output side.



4 to 2 encoder

INPUTS				OUTPUTS	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Questions

Which of the following statements are true ?

- I. A circuit that adds two bits, producing a sum bit and a carry bit is called half adder.
- II. A circuit that adds two bits, producing a sum bit and a carry bit is called full adder.
- III. A circuit that adds two bits and a carry bit producing a sum bit and a carry bit is called full adder.
- IV. A device that accepts the value of a Boolean variable as input and produces its complement is called an inverter.

A

I & II

B

II & III

C

I, II, III

D

I, III & IV

Answer

- I, III and IV are correct

Questions

10. 3 bits full adder contains _____

- a) 3 combinational inputs
- b) 4 combinational inputs
- c) 6 combinational inputs
- d) 8 combinational inputs

Answer

- Input bits = 3
- Output bits = 2
- Total combinational inputs = 2 options for each input bit => $2*2*2 = 8$

Questions

A device which converts BCD to seven segment is called____

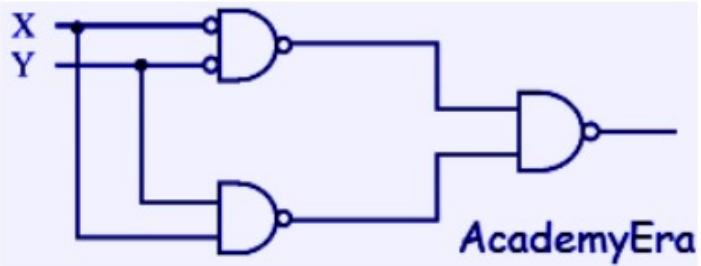
- A Encoder
- B Decoder
- C Decoder
- D Demultiplexer

Answer

- Decoder

Question

The output of the following combinational circuit.



A

$$X \cdot Y$$

B

$$X + Y$$

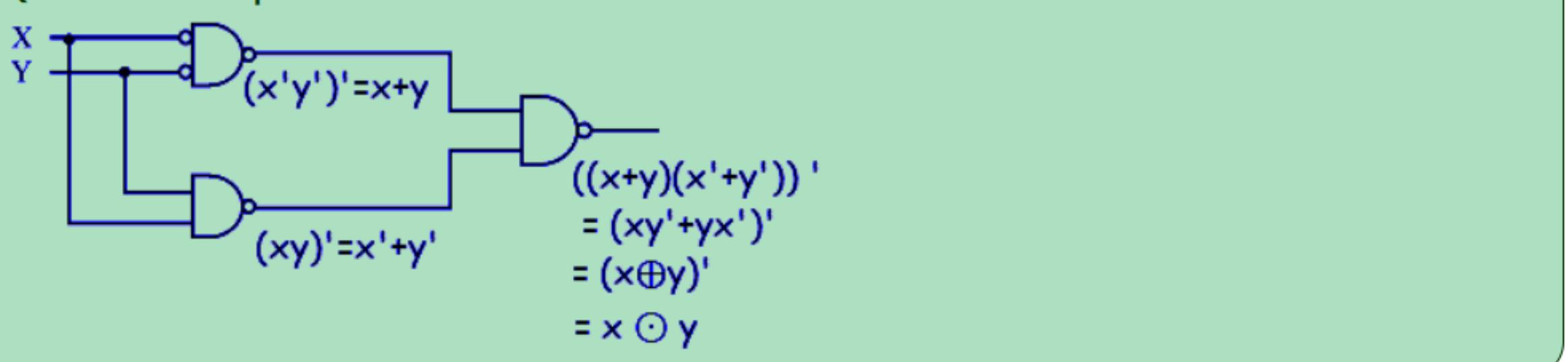
C

$$X \oplus Y$$

D

$$(X \oplus Y)'$$

Answer



Combinational Circuits (continued)

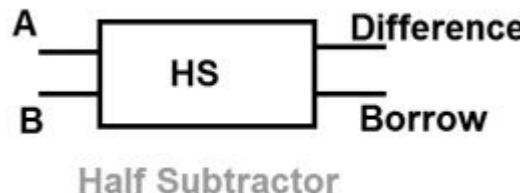
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Binary Subtractors

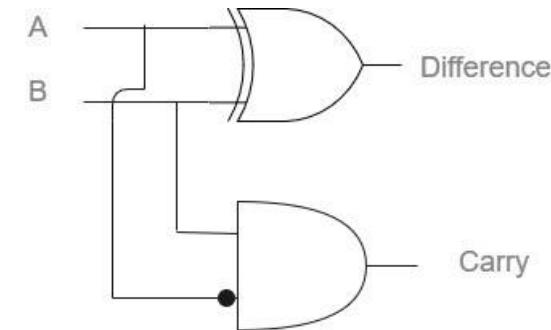
The binary subtractor is another type of combinational arithmetic circuit that produces an output which is the subtraction of two binary numbers

The type of binary subtractors are:

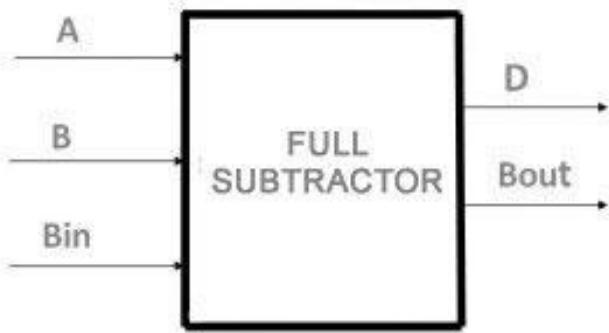
1) HALF SUBTRACTOR



A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



2) FULL SUBTRACTOR



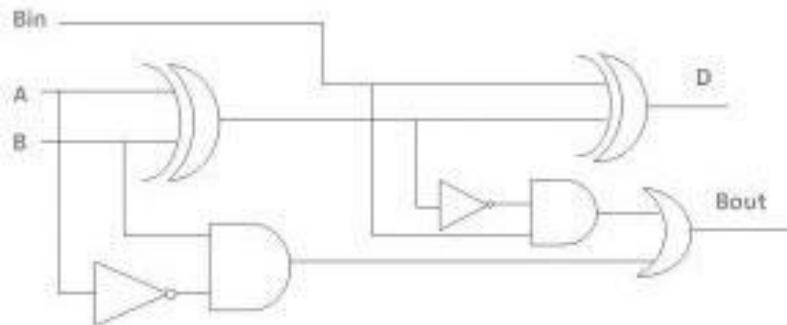
	B Bin	00	01	11	10
A	0	0	1	0	1
1	1	0	0	1	0

$$D = A'B'Bin + AB'Bin' + A'BBin' + BBin$$

	B Bin	00	01	11	10
A	0	0	1	1	1
1	0	0	1	0	0

$$Bout = A'Bin + A'B + BBin$$

INPUT			OUTPUT	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Multiplexer

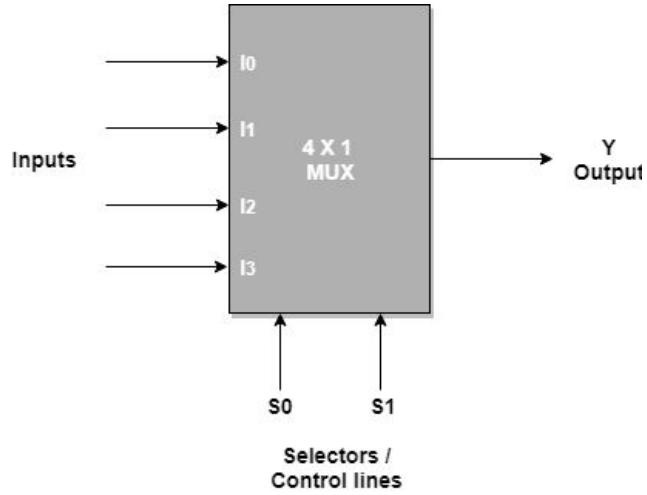
Multiplexer is a special type of combinational circuit. It selects one of the data inputs and routes it to the output with the help of selection lines. The Multiplexer, shortened to ‘MUX’ is also called a data selector.

The standard form of a MUX is $2^n \times 1$ where

2^n = number of input lines

n = no of selection lines

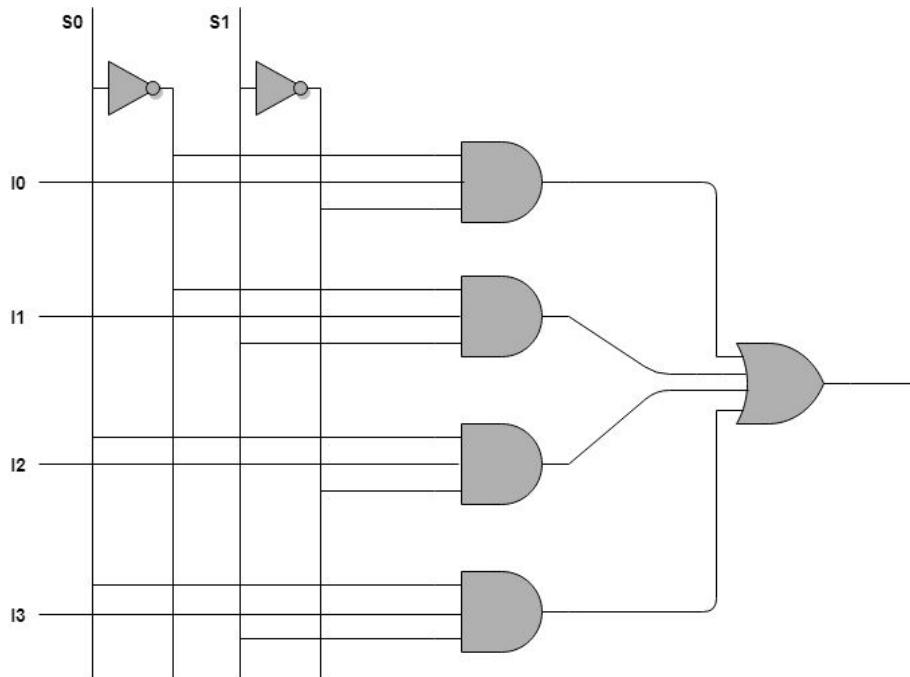
1 = output lines



Multiplexer

Truth Table

S_0	S_1	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



So, final equation,

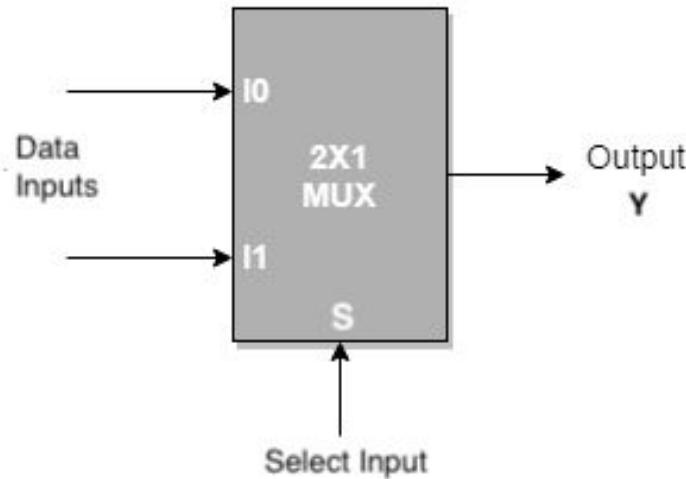
$$Y = S_0'.S_1'.I_0 + S_0'.S_1.I_1 + S_0.S_1'.I_2 + S_0.S_1.I_3$$

Advantages of Multiplexers

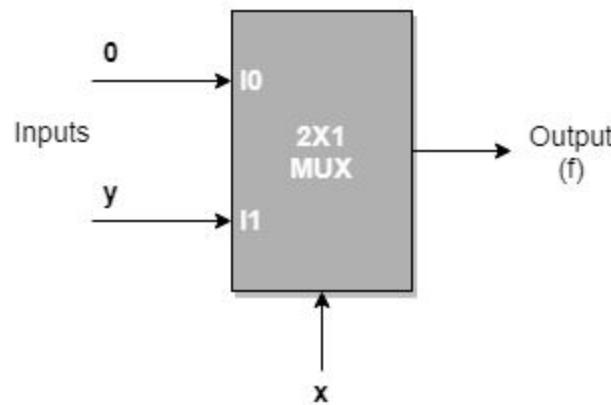
- It reduces the number of wires, and therefore reduces the circuit complexity and cost
- It simplifies the logic design
- It does not need the K-maps and simplification
- With the help of a MUX, we can implement many combinational circuits

2×1 MUX

It has 2 data inputs I_0 and I_1 , 1 select input S and 1 output Y



Implementation of AND gate using 2×1 MUX



Truth Table			
x	y	f	$f \rightarrow y$
0	0	0	$f = 0$
0	1	0	
1	0	0	$f = y$
1	1	1	

Demultiplexer

A demultiplexer performs the reverse operation of a multiplexer i.e. it receives one input and distributes it over several outputs. At a time only one output line is selected by the select lines and the input is transmitted to the selected output line.

The standard form of a DEMUX is 1×2^n where

$1 =$ no. of input lines

$n =$ no. of selection lines

$2^n =$ no. of output lines

GATE Questions

For a binary half-subtractor having two inputs A and B, the correct set of logical expressions for the outputs D($= A - B$) and X($=$ borrow) are

- A. $D = AB + A'B, X = A'B$
- B. $D = A'B + AB', \quad X = AB'$
- C. $D = A'B + AB', \quad X = A'B$
- D. $D = AB + A'B, X = AB'$

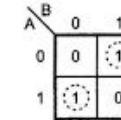
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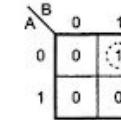
Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

For Difference



$$\text{Difference} = AB + \bar{A}B \\ = A \oplus B$$

For Borrow



$$\text{Borrow} = \bar{A}B$$

ANS: C

GATE Questions

Minimum number of 2×1 multiplexers required to realize the following function, $f = A'B'C + A'B'C'$

Assume that inputs are available only in true form and Boolean constant 1 and 0 are available

- A. 1
- B. 2
- C. 3
- D. 7

GATE Questions

Minimum number of 2×1 multiplexers required to realize the following function, $f = A'B'C + A'B'C'$

Assume that inputs are available only in true form and Boolean constant 1 and 0 are available

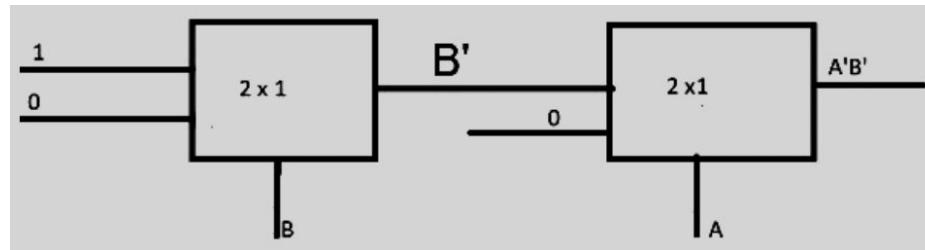
A. 1

B. 2

C. 3

D. 7

$$\begin{aligned} &A'B'C + A'B'C' \\ &A'B'(C + C') \\ &A'B'(1) \\ &A'B' \end{aligned}$$



ANS: B

GATE Questions

If four 4 input multiplexers drive a 4 input multiplexer we get a:

A. 16 input MUX

B. 8 input MUX

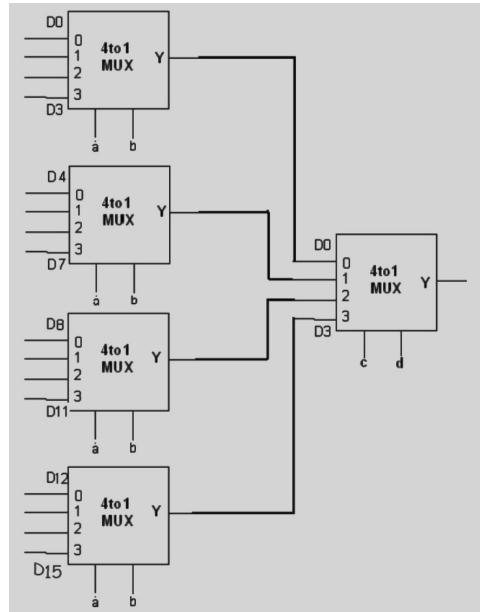
C. 4 input MUX

D. 2 input MUX

GATE Questions

If four 4 input multiplexers drive a 4 input multiplexer we get a:

- A. 16 input MUX
- B. 8 input MUX
- C. 4 input MUX
- D. 2 input MUX



This is a circuit for a 16 to 1 MUX
The select lines are a, b, c and d

ANS: A

SEQUENTIAL CIRCUITS

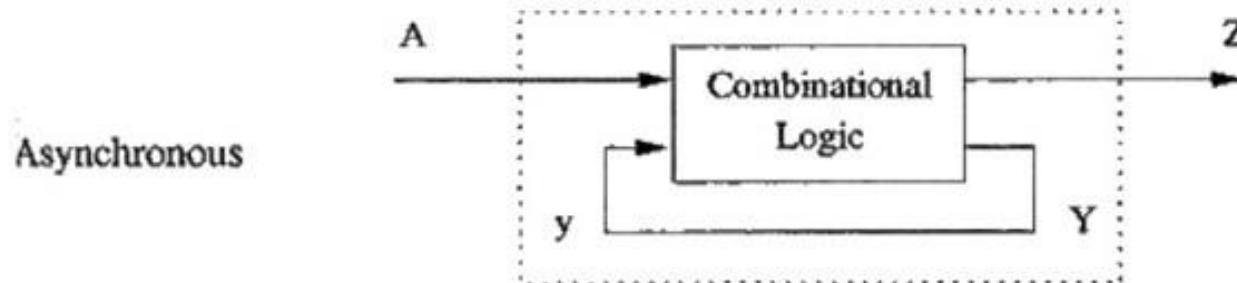
Introduction

- The sequential circuit is a special type of circuit that has a series of inputs and outputs. The outputs of the sequential circuits depend on both the combination of present inputs and previous outputs. The previous output is treated as the present state. So, the sequential circuit contains the combinational circuit and its memory storage elements. A sequential circuit doesn't need to always contain a combinational circuit. So, the sequential circuit can contain only the memory element.

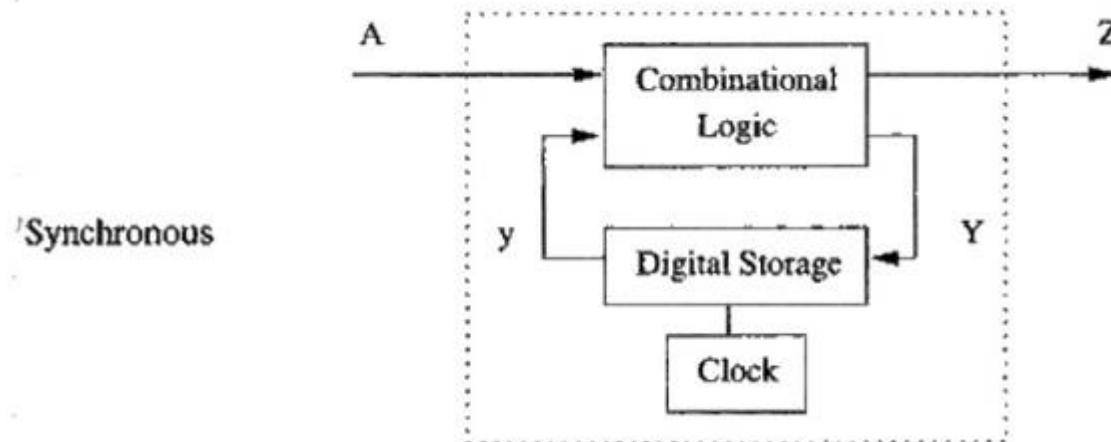
Types of Sequential Circuits

1. Asynchronous circuits

The clock signals are not used by the **Asynchronous sequential circuits**. The asynchronous circuit is operated through the pulses. So, the changes in the input can change the state of the circuit. The asynchronous circuits do not use clock pulses. The internal state is changed when the input variable is changed. The un-coded flip-flops or time-delayed are the memory elements of asynchronous sequential circuits.



2. In synchronous sequential circuits, synchronization of the memory element's state is done by the clock signal. The output is stored in either flip-flops or latches(memory devices).

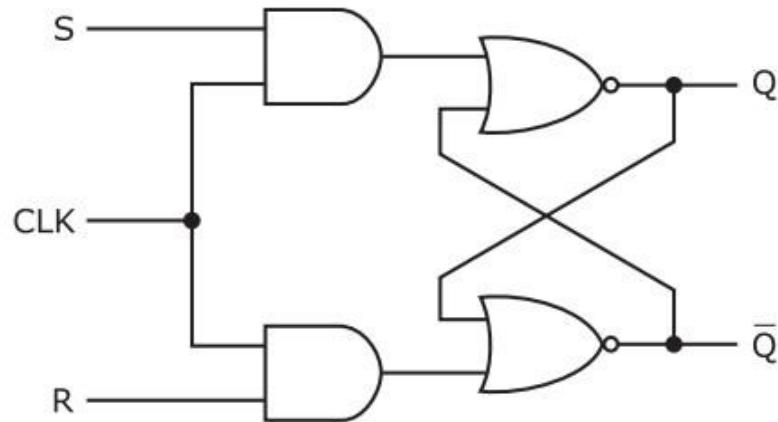


Flip Flops

- It is a one-bit memory cell which stores the 1-bit logical data (logic 0 or logic 1). It is a basic memory element. The most commonly used application of flip flops is in the implementation of a feedback circuit. In the synchronous sequential circuit, Memory elements are clocked flip flops and generally edge triggered. In the asynchronous sequential circuit, Memory elements are unclocked flip flops/time delay elements which are generally level triggered.
- Types of Flip-flops:
 1. S-R Flip-flops
 2. Delay Flip-flops
 3. J-K Flip-flops
 4. T Flip-flops

S-R Flip-flop

Circuit diagram

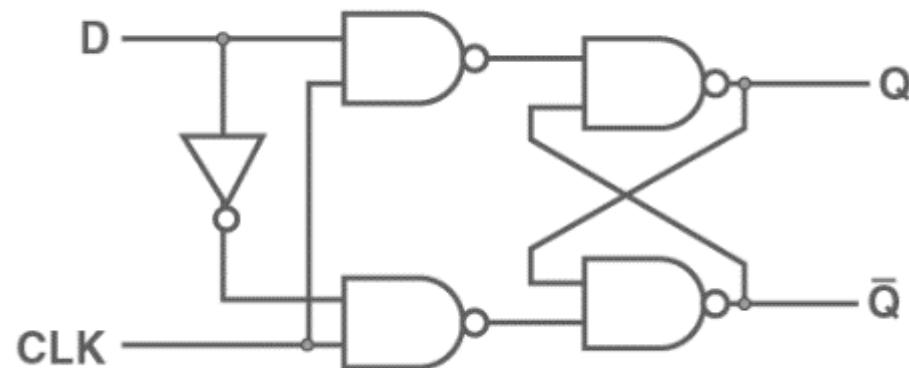


Characteristic Table

S	R	$Q(t+1)$	Operation
0	0	$Q(t)$	No change/Hold
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined/Invalid

D Flip-flop

Circuit diagram

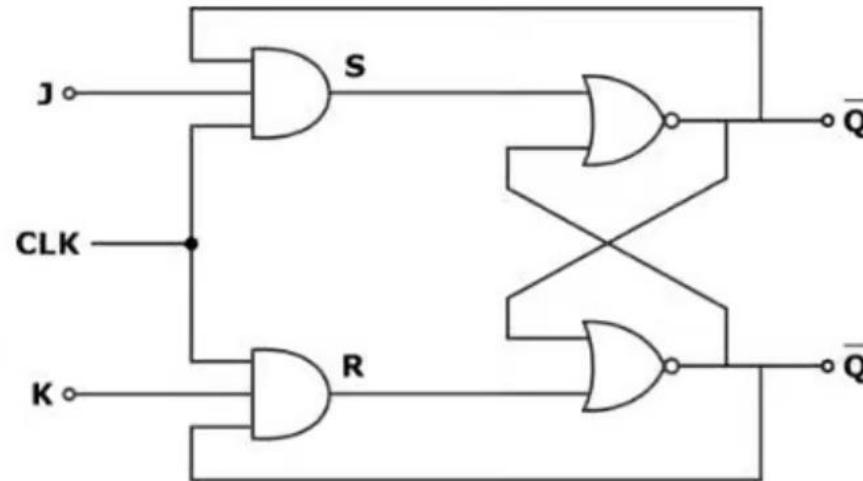


Characteristic Table

D	Q(t+1)	Operation
0	0	Set
1	1	Reset

J-K Flip-flop

Circuit diagram



Characteristic Table

J	K	Q_n	Q_{n+1}	State
0	0	0	0	Q_n (Hold)
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	

Questions

The logic operations of two combinational circuits in Figure-I and Figure-II are

1.

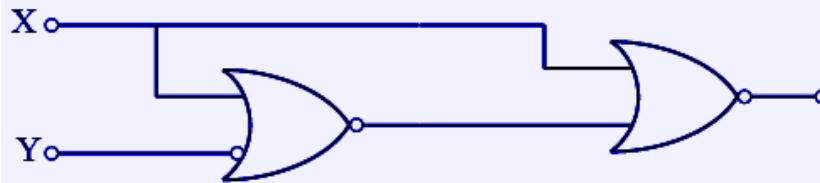


Figure - I

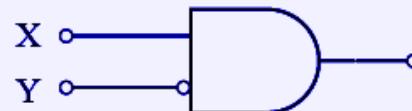
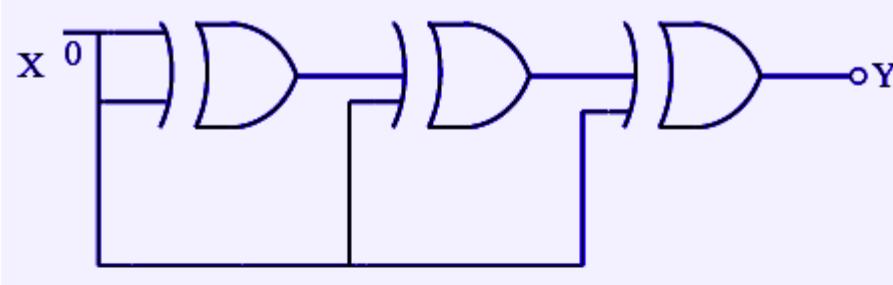


Figure - II

- A** Entirely different
- B** Identical
- C** Complementary
- D** Dual

2.

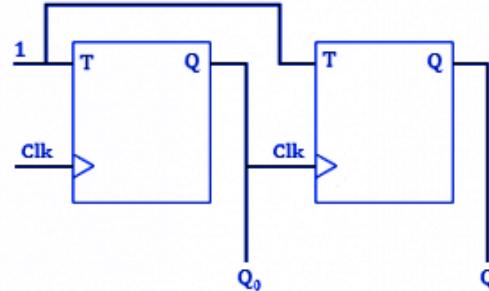
The output Y of the given circuit



- A 1
- B 0
- C X
- D X'

3.

Consider the following sequential circuit



What are the values of Q_0 and Q_1 after 4 clock cycles if the initial values are ?

- A 11
- B 01
- C 10
- D 00

4. How many flip-flop are needed to divide the input frequency by 64?

- A
- B
- C
- D

4
5
6
8

5. If a clock with time period "T" is used with n stage shift register, then output of final stage will be delayed by

- A
- B
- C
- D

NT sec
 $(n-1)T$ sec
 N/T sec
 $(2n-1)T$ sec