

CS2106 AY23/24 Finals CheatSheet

Chapter 6: Synchronization

//Normal code
Enter CS
Critical Section
Exit CS
//Normal code



4 Properties of Critical Section Implementation

Mutex	If process P_i is executing in critical section, all other processes are prevented from entering the critical section.
Progress	If no process is in a critical section, one of the waiting processes should be granted access.
Bound-ed Wait	<ul style="list-style-type: none"> After process P_i request to enter critical section, there exists an upper bound of number of times other processes can enter the critical section before P_i. <ul style="list-style-type: none"> No process hogs the CS (there is a time limit) Decision of next process (i.e. CS scheduling) should be fair. Each process should have guaranteed access to the CS
Indpt	Process not executing in CS should never block other process.

Wrong Implementations of Synchronization result in:

Deadlock	<ul style="list-style-type: none"> All process blocked, no progress. (Circular wait) Caused by accessing limited resources in an interleaving way.
Livelock	<ul style="list-style-type: none"> Happens when deadlock avoidance mechanism malfunctions. Processes are NOT Blocked. They just constantly change state to avoid deadlock. (Instead of running, jump on the spot)
Starvation	<ul style="list-style-type: none"> Some Processes may be blocked forever with bad scheduling algo
Race Condition	Processes compete to get to access shared resources (concurrency), resulting in unpredictable/inconsistent outputs.
Assembly Level Implementation of Synchronization	<ul style="list-style-type: none"> Implemented via Test and Set (Lock mechanism) Works, but with busy waiting → Avoids simultaneous access to shared mem. <ul style="list-style-type: none"> Wastes resources, as CPU time is used for waiting for the process's turn. Variants: Compare & Exchange, Store Conditional, Atomic Swap, Load Link. Peterson's Algorithm (Has both Turn and Want[] variables)

High Level Implementation of Synchronization

- Ensure that the 4 properties of synchronization are met.
- Why Disabling/Enabling Interrupts may not be a good idea for synchronization?
 - Buggy CS may stall whole system. Interrupts disables → Cannot Ctrl+C to end code, since keyboard interrupts are disabled.
 - Security issue. Interrupts → Kernel level method, need privileged access.
 - Busy waiting → Waste clock cycles.
 - Interrupt is isolated within a single core. This synchronization method will not work for a multicore system. (Mutex not resolved)
- Turn based system is NOT GOOD. (Turn = 0 or 1).
 - Other programs will be starved if the program in CS does not finish executing, since the turn is only updated once the program finishes executing in CS.
 - If P_0 has yet to enter CS → turn not updated → P_1 gets starved.
 - The process not executing in CS should not block other processes.
 - If P_0 is not in CS SHOULD NOT block P_1 (Need to update turn pre-empted)

Global Check Array (Not good)

- This is similar to turn based system, except that the turn/“want” parameter gets updated when another program is pre-empted.
- However, this can result in deadlocks (violates Progress)
 - If pre-emption happens right after P_0 sets want[0] = 1, and P_1 set want[1] = 1 → P_0 cannot escape the while (want[0]) loop.
 - When P_0 gets pre-empted, it also gets stuck in while (want[1]) loop.

Semaphores (machine-independent)

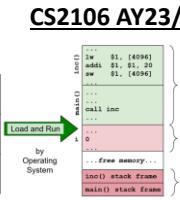
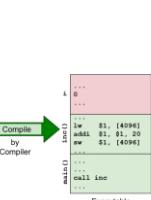
- Wait(s);
Critical Section
Signal(s);
- Uses Wait() and Signal() operations.
 - If $s \geq 0$, blocks; Decrement s
 - Signal(s) → Increments s ; wakes up sleeping process; NOT a blocking call.
 - Properties of Semaphores:
 - Since ≥ 0
 - $s_{current} = s_{initial} + \#Signal(s) - \#Wait(s)$
 - Wait() & Signal() MUST BE USED CORRECTLY.
 - Interleaving processes with wait(s) will cause deadlocks, since the signals() are unreachable.

- When user-level threads share a single kernel-level thread, they can run concurrently, but not parallel.
 - The instructions of user-level threads may be interleaved, giving the appearance that all threads are progressing together over time.
 - However, this does not mean they are running at the exact same moment.
- True parallel execution, where threads run simultaneously, requires a computer with multiple processors or cores.
 - Given that the scheduler only see kernel-level threads, it can allocate only one CPU core per kernel-level thread.
 - Consequently, user-level threads sharing a single kernel-level thread cannot run in parallel.

Chapter 7: Memory Abstraction

- A single byte (byte addressable) or ** char = 1 byte
- A single word (word addressable) ** 1 word = 4 bytes (Word is usually 2ⁿ bytes)

- Word alignment → the memory address is a multiple of the word size
- Buffer is flushed when 1. Buffer full, 2. fflush() called. 3. (n) printed
- FD table is in the kernel side and is never copy-on-write.
- The threads in a single process will share the same fdtable, so no need to copy.



- Physical frames, page table, TLB are not stored in memory.
- PCB & page table will be stored in RAM.
- The PCB stores info crucial for process management, in RAM.

Chapter 8: Disjoint Memory (Paging Scheme + Segmentation Scheme)

- Storing data in contiguous blocks is inefficient as it results in many holes.
- Disjoint chunks are more memory efficient. OS splits the process into disjoint chunks, and puts them into the chunks in memory.
 - Disjoint chunks can either be fixed or variable sizes.
- The frame size is decided by hardware. (Memory Management Unit, MMU in the CPU)
- Mem addresses are abstracted into logical mem, and this mapping is done by the MMU

Paging Scheme

- To support multitasking:
 - Allow multiple processes in the physical mem simul. So that we can switch btwn processes.

Free up mem by (phy mem full):

- Removing terminated process (Reclaim used space for other processes)
- Swapping blocked process to secondary storage (Increases efficiency)

- Paging: split the logical address into fixed size pages
- A page table is used to translate between Logical Page and Physical Page.

$$\text{Number of Frames} = \frac{\text{Page Size}}{\text{Page Size}}$$

$$\text{Physical Address} = \text{Frame Number} \times \text{sizeof(Physical Frame)} + \text{Offset}$$

$$\text{Logical Address} = \text{Page Number} \times \text{sizeof(Logical Page)} + \text{Offset}$$

4. Logical Frame SIZE = Physical Page Size.



In Paging scheme, External Fragmentation is NOT POSSIBLE

- Internal Fragmentation is still possible if the process size != page size → Holes
 - There will only 1 page in a process that has holes. (Last page will have internal frag)
 - E.g. 3kb total, but page size = 2kb → split 2kb, 1kb → Hole = 1kb (Int Frag)
- Page table is PER PROCESS, not global. It is kept tracked via the Process Control Block.
- Keeps track of the pointer to base address of the page table.

Translation Look-Aside Buffer (TLB)

- “Cache” for Page Table entries. **PTB → Page Table Base Register
- TLB is a REGISTER → VERY FAST, but expensive, small storage. (TLB part of hardware ctx)
 - For every context switch, update PTB & update address in register.
- TLB maintains the page and frame number, and stores most used/recently accessed pages/frames in the TLB. → faster access time compared to 2 * mem reference.

With TLB

- 1 * Memory Access + 1 TLB look up:
 - Check if TLB has a hit (Fast, using registers), if yes, return frame number + offset, if not, look up in the Page Table.
 - Access the actual memory item in Physical Memory.

Average Mem Access Time: Latency: hit → 1 MA, 1TLB miss → 2 MA, 1TLB hit + 1 TLB miss = P(hit) x latency(hit) + P(miss) x latency(miss)

No TLB

Requires 2 memory access for every memory reference:

- 1. Access the page table entry to get the frame number.
- 2. Access the actual memory item in Physical Memory.

TLB reduces #page table access. TLB contains permission bits.

Paging Scheme Protection

- | Access Right Bits | • Each Page Table Entry has { writable, readable, executable } bits |
|---|--|
| • Every mem access is checked against the access right bits in hardware | |
| Best Fit | • Protect from unwanted behaviour via wrx. |
| Worst Fit | Find the LARGEST hole |
| | Choose D |
| | • With worst-fit, we won't end up with many small holes. Bigger holes → more efficient in assigning holes to new processes (in the future) |
- Each Page Table Entry has { writable, readable, executable } bits
 - Every mem access is checked against the access right bits in hardware
 - Protect from unwanted behaviour via wrx.

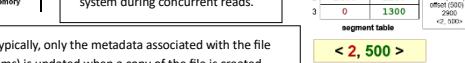
- | Valid Bits | • Indicates whether the page is valid to access by the process |
|------------|--|
| | • OS will set the valid bits as mem is being allocated to the process |
| | • Every memory access is checked against this bit in hardware: <ul style="list-style-type: none"> - Out-of-range access will be caught by OS in this manner |

Paging Scheme Page Sharing

- With the use of Copy on Write (COW), we save memory and space.
- COW → Copy the page table instead of the frames → More efficient.
- COW → Only when a file is modified, then a new page is created, + update page table

Segmentation Scheme

While multiple processes reading the same file won't directly result in interleaved output due to file pointers and access control, there might be some internal interleaving within the operating system during concurrent reads.



When COW is applied to file systems, typically, only the metadata associated with the file (such as the inode in Unix-like file systems) is updated when a copy of the file is created.

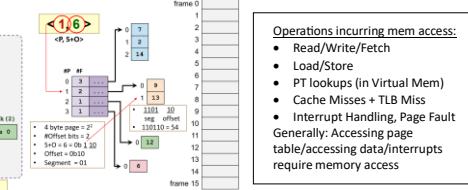
Segment Table

- Keeps track of Base Address + Limit Size. <Base, Limit>
- Access beyond limit → Segmentation fault. (Valid if offset < limit)
- Seg ID is used to lookup <Base, Limit> of the segment in the segment table
- Memory referenced by: Segment Name + Offset. <Seg ID, Offset> → e.g. <2, 500>

- Segments are disjoint pieces in memory, created to better fit a process. Segments are not further divided into subsegments.
- Segmentation does not suffer from external fragmentation
- A large mem space can be more efficiently represented by few segments, than by many pages.
 - The size of the segment table DOES NOT depend on the size of the corresponding segments, while the page table size increase with the #pages.

Segmentation with Paging

- Each segment is now composed of several pages instead of a contiguous mem region
- Essentially, each segment has a page table.
- Segment can grow/shrink by allocating/freeing new page then add to its page table.



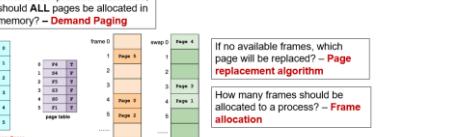
- Operations incuring mem access:
 - Read/Write/Fetch
 - Load/Store
 - PT lookups (in Virtual Mem)
 - Cache Misses + TLB Miss
 - Interrupt Handling, Page Fault

How to access secondary storage?

- Check page table:
 - Is page X memory resident?
 - Yes: Access physical memory location. Done.
 - No: raise an exception!
- Page Fault: OS takes control
- Locate page X in secondary storage
- Load page X into a physical memory
- Update page table
- Go to step 1 to re-execute the same instruction
 - This time with the page in memory

- Secondary Storage access time >>> Physical mem access time (milli >>> nano)
- If mem access results in page faults (i.e. not mem resident) [THRASHING]
 - Slows down system, as we need to retrieve non-resident and paste it in memory.
- To prevent Thrashing, we can take advantage of the principles of locality.

- | Temporal | • Mem address used is likely to be used again (e.g. loops) |
|---------------|---|
| | • After a page is loaded into phy mem, it may be needed again soon |
| Spatial | • Mem address close to that address is likely to be used soon (seq). |
| | • A page containing many consecutive locations is likely to be accessed soon → Later access to nearby locations will not cause seg fault. |
| Demand Paging | • Processes start with NO MEMORY in resident page. |
| | • Only allocate a page when there is a page fault. |
| | + Reduces startup cost, small memory footprint. |
| | - Cascading effect → Many page faults back-to-back (initially) |



- When a new process is launched, should ALL pages be allocated in memory? – Demand Paging
 - If no available frames, which page will be replaced? – Page replacement algorithm
 - How many frames should be allocated to a process? – Frame allocation
 - What if page table is huge? – Page table structure
 - Page Table Structure: **PT is PER PROCESS
- | Direct | • size = # of frames (EXP) |
|------------------|---|
| <P, PID>
-> F | • Keep all entries in a single table. (2 ⁿ pages in logical mem space) |
| 2-Level / | <ul style="list-style-type: none"> • size = (# process) * (avg # pages / process) • Page the page table. (Split whole table into regions) |

Data blocks must fill the direct blocks first, then indirect block, and after that doubly indirect blocks and so on.

Multi Level P->F	<ul style="list-style-type: none"> - Split 2^l table into smaller 2^(P_l) tables - #Pages = VA space / Page size PT size = #Pages * Size PTE • Additional Info needed to keep track (Page Directory Needed) <p>+ Page table structure can grow beyond the size of a frame. - Requires 2 * serialized memory access just to get frame number. ➤ Use TLB to remedy this issue, but will longer page-table walks.</p>
	<ul style="list-style-type: none"> • Radix-tree structure. A table in each level in the hierarchy is put in a frame. All tables are setup by OS in SW, but traversed by HW virtual address (bits 48 - 63 currently unused) <p>Part of the HW context of each process An invalid entry in any level means that the entire subtree does not exist</p>

Hierar-chical	<ul style="list-style-type: none"> • Frame Allocation. A table in each level in the hierarchy is put in a frame. All tables are setup by OS in SW, but traversed by HW virtual address (bits 48 - 63 currently unused) <p>Part of the HW context of each process An invalid entry in any level means that the entire subtree does not exist</p>
	<ul style="list-style-type: none"> • Size = Size of Physical Memory • Keep a single mapping of physical frame to <pid, page#> - page# is not unique; pid + page# can uniquely identify a mem pg - #Frames = Size of Mem/Page Size - Inverted Page Table Size = #Frames * Size of PTE (e.g 2 bytes) <p>In inverted page table, the entries are ordered by frame number - To lookup page X, need to search the whole table - Reduce memory needed, but longer lookup time; Easier to cache</p>

Invert-ed	<p>Page Replacement Algorithms</p> <p>p → probability of a fault</p> $T_{Mem\ access} = (1-p) \times T_{Mem\ p} + p \times T_{page\ fault}$
	<ul style="list-style-type: none"> • Theoretical Baseline to compare the other algorithms. • Replace the page that will not be needed again for the longest period of time → Guarantees minimum number of page faults. • However this is not feasible, as we cant predict the future.

Optimum (OPT)	<ul style="list-style-type: none"> • Memory pages are evicted based on their loading time • Evict the oldest memory page • OS maintains a queue of resident page numbers, and removes the 1st page in the queue upon replacement request + Update queue. <p>Problems of FIFO</p> <ul style="list-style-type: none"> • FIFO does not exploit temporal locality (BAD PERFORMANCE) • By right: If #phy frames ↑, #page faults should ↓. • FIFO: ↑ frames → ↑ page faults (Belady's Anomaly) - Any stack based algo will NOT suffer from Belady's Anomaly 			
	<ul style="list-style-type: none"> • Make use of temporal locality <ul style="list-style-type: none"> - Recency: Replace page that hasn't been used in longest time. ➤ the least recent page one - Expect a page to be reused in a short time window ➤ Page not used for some time → most likely will not be used again. • Approximates OPT via predicting future by mirroring the past. • Additional hardware is needed for Least Recently Used Algo. <table border="1"> <thead> <tr> <th>1: Use Counter</th> <th>2: Use "Stack"</th> </tr> </thead> <tbody> <tr> <td> <ul style="list-style-type: none"> • Tracks "Time of Usage" • Replace smallest TOU pg. • Overflow (32 bit), while time ↑ forever. </td> <td> <ul style="list-style-type: none"> • Stack for page numbers. • Pop stack, use page then push to top of stack. • Bottom of stack replaced. </td> </tr> </tbody> </table>	1: Use Counter	2: Use "Stack"	<ul style="list-style-type: none"> • Tracks "Time of Usage" • Replace smallest TOU pg. • Overflow (32 bit), while time ↑ forever.
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FIFO	<ul style="list-style-type: none"> • Memory pages are evicted based on their loading time • Evict the oldest memory page • OS maintains a queue of resident page numbers, and removes the 1st page in the queue upon replacement request + Update queue. <p>Chapter 10: File Systems</p> <p>** Provides abstraction for Hard Disk</p> <ul style="list-style-type: none"> • A file is basically data + some operation. (It is an abstract data type) • A file contains: Data (Info) + Metadata (Additional Info associated with the file) <table border="1"> <thead> <tr> <th>Name</th><th>A human readable reference to the file</th></tr> </thead> <tbody> <tr> <td>Identifier</td><td>A unique ID for the file used internally by File Systems</td></tr> <tr> <td>Type</td><td>Indicates different types of files. E.g Executable, Text File, etc... <ul style="list-style-type: none"> • ASCII Files → Can be displayed/printed as it is (e.g txt file) • Binary Files → Needs special processing to read (e.g png file) </td></tr> <tr> <td>Size</td><td>Current size of file (in bytes, words or blocks)</td></tr> <tr> <td>Protection</td><td>Access permissions, can be classified as RWX rights. 000 to 777 XXX XXX XXXX → OWNER GROUP OTHERS (7 = 111; RWX) Access: Read, Write, Execute, Append, Delete, List</td></tr> <tr> <td>Time,Data&OI</td><td>Creation, Last Modified Time, Owner ID etc... OI → Owner Info</td></tr> <tr> <td>TOC</td><td>Info for the File System to determine how to access the file.</td></tr> </tbody> </table>	Name	A human readable reference to the file	Identifier	A unique ID for the file used internally by File Systems	Type	Indicates different types of files. E.g Executable, Text File, etc... <ul style="list-style-type: none"> • ASCII Files → Can be displayed/printed as it is (e.g txt file) • Binary Files → Needs special processing to read (e.g png file) 	Size	Current size of file (in bytes, words or blocks)	Protection	Access permissions, can be classified as RWX rights. 000 to 777 XXX XXX XXXX → OWNER GROUP OTHERS (7 = 111; RWX) Access: Read, Write, Execute, Append, Delete, List	Time,Data&OI	Creation, Last Modified Time, Owner ID etc... OI → Owner Info	TOC	Info for the File System to determine how to access the file.
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<ul style="list-style-type: none"> • Operations on Metadata: <ul style="list-style-type: none"> - Rename → Change file's name - Change Attributes → File access permission, dates, ownership etc. - Read Attributes → Get file creation time <p>General Criteria for a good File System:</p> <ul style="list-style-type: none"> • Self-Contained (Plug&play, no extra configuration needed to read data e.g Thumbdrive) • Persistent (Data should be independent of PC's state + Transferrable across PCs) • Efficient (Provides good management of free/used space + Min overhead) <p>File Data Structure</p> <ul style="list-style-type: none"> • Array of bytes; each byte has a unique offset from the start of file • Fixed Length Records; Offset of the Nth record = size of Record * (N - 1) **Int Frag • Variable Length Records; flexible but harder to locate a record. <p>File Data Access Methods</p> <table border="1"> <thead> <tr> <th>Sequential</th> <th> <ul style="list-style-type: none"> • Data read in order, starting from beginning • Cannot skip, but can rewind (e.g Cassette Tape) </th> </tr> </thead> </table>	Sequential	<ul style="list-style-type: none"> • Data read in order, starting from beginning • Cannot skip, but can rewind (e.g Cassette Tape) 													
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LRU	<ul style="list-style-type: none"> • BEST Algorithm (Closest to OPT) • Maintains a Victim page, a pointer to victim page & reference ptr. • A modified FIFO can give a second chance to pages that are accessed • Each PTE now maintains a reference bit: <ul style="list-style-type: none"> - 1 = Accessed since the last reset, 0 = Not accessed <p>Algorithm:</p> <ul style="list-style-type: none"> • The oldest FIFO page is selected (victim page) • If reference bit == 0 → Page is replaced. Done. • If reference bit == 1 → Page is skipped (given a 2nd chance) <ul style="list-style-type: none"> - Reference bit cleared to 0 - Effectively resets the arrival time → page taken as newly loaded - Next FIFO page (victim) is selected, go to Step 2 • Degenerate into FIFO algorithm when all pages have ref bit == 1
	<p>Disk Access Time = Seek Time + Rotational Latency + Transfer Time</p> <p>Total Seek Time = Total head Movement * Seek Time</p> <p>When a page is evicted:</p> <p>Clean page: not modified → no need to write back</p> <p>Dirty page: modified → need to write back</p>

