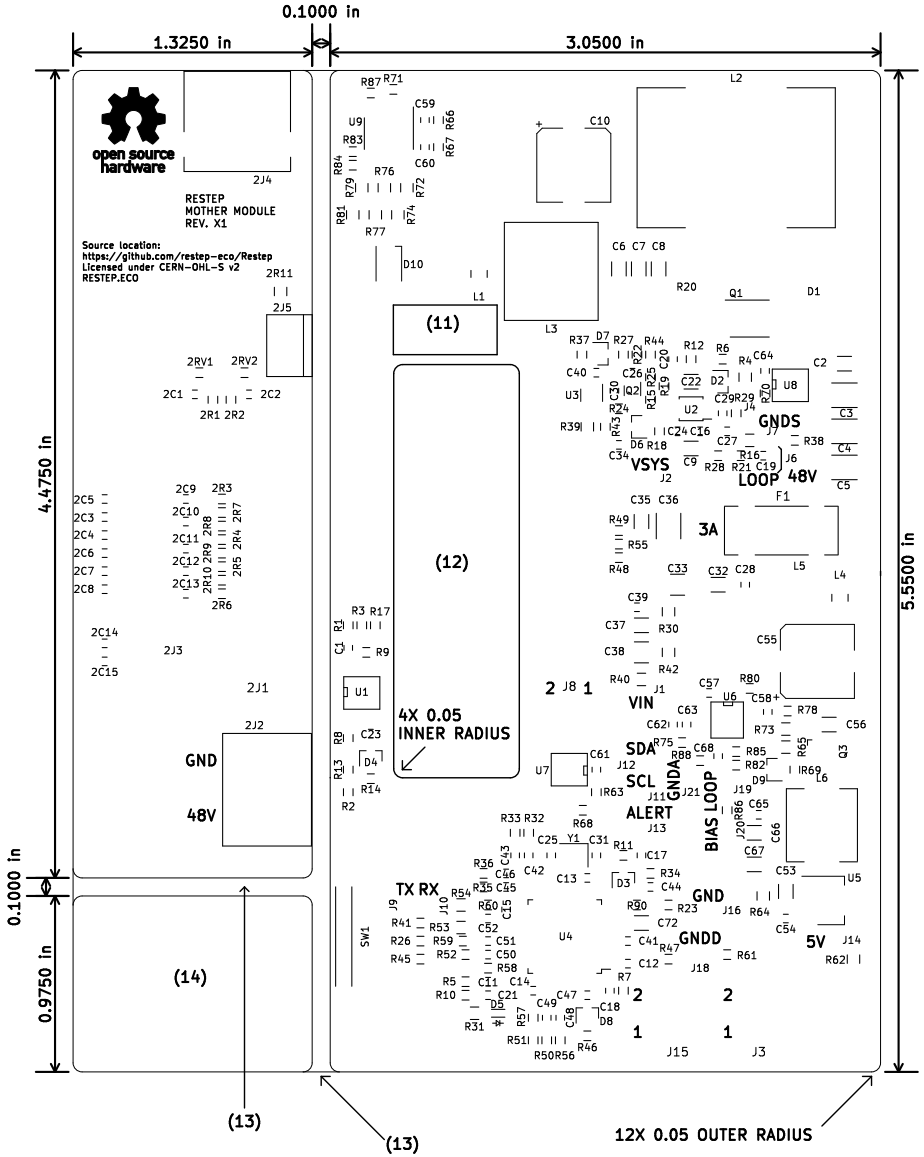

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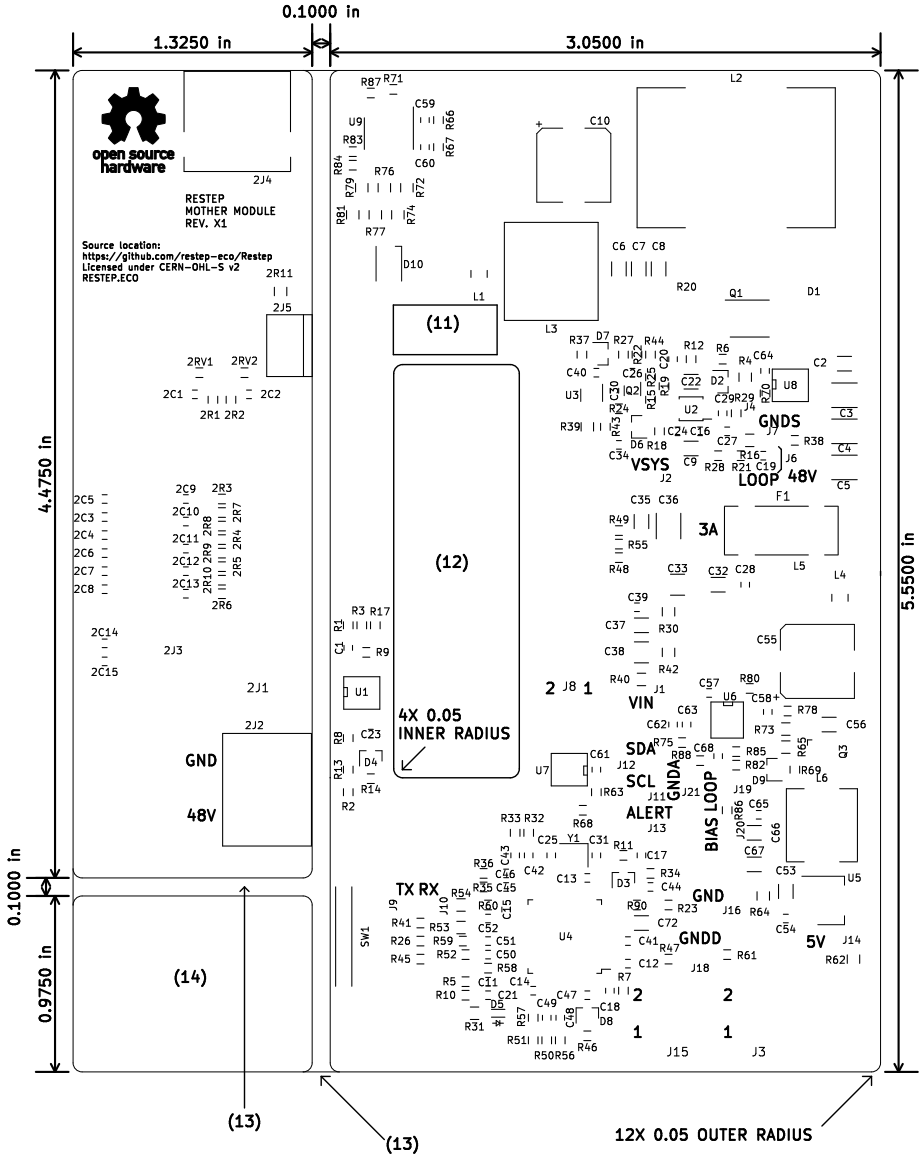
14. UNUSED AREA. DISCARD AFTER SEPARATING.
13. V-SCORE ON CENTER BETWEEN BOARD OUTLINES.
    AFTER ASSEMBLY SNAP BOARDS APART AND SMOOTH ANY ROUGH EDGE.
12. NON-PLATED CUT OUT AREA. THIEVING MAY BE ADDED TO COPPER LAYERS IN THIS AREA AS NEEDED TO IMPROVE MANUFACTURABILITY. ALL BOARD EDGES SHALL NOT HAVE EXPOSED COPPER.
11. SILKSCREEN DATE CODE, LOT CODE, AND LOGO APPROX. WHERE SHOWN.
10. ALL VIA HOLES 0.016 SHALL BE TENTED.
9. PLATED HOLES SHALL HAVE PLATING THICKNESS GREATER THAN 0.0012.
8. FINISH: ALL EXPOSED CONDUCTIVE SURFACES TO BE SILVER AFTER APPLICATION OF SOLDER MASK.
7. APPLY SOLDER MASK TO TOP SIDE ONLY.
6. DIELECTRIC MATERIAL IS FR-4 Tg > 130
5. COPPER WEIGHT IS 2 OZ.
4. NUMBER OF LAYERS IS 4
3. PCB THICKNESS IS 0.062
2. BOARD DESIGNED IAW IPC-2221, CLASS 2
1. DIMENSIONS IN INCHES

DESIGN BY CHRIS ARNTZEN
RESTEP

Sheet:
File: MotherX4.kicad_pcb

Title: MOTHER MODULE PCB

Size: A4	Date: 8/11/18	**Rev: X1**
KiCad E.D.A. kicad 4.0.7		Id: 1/1



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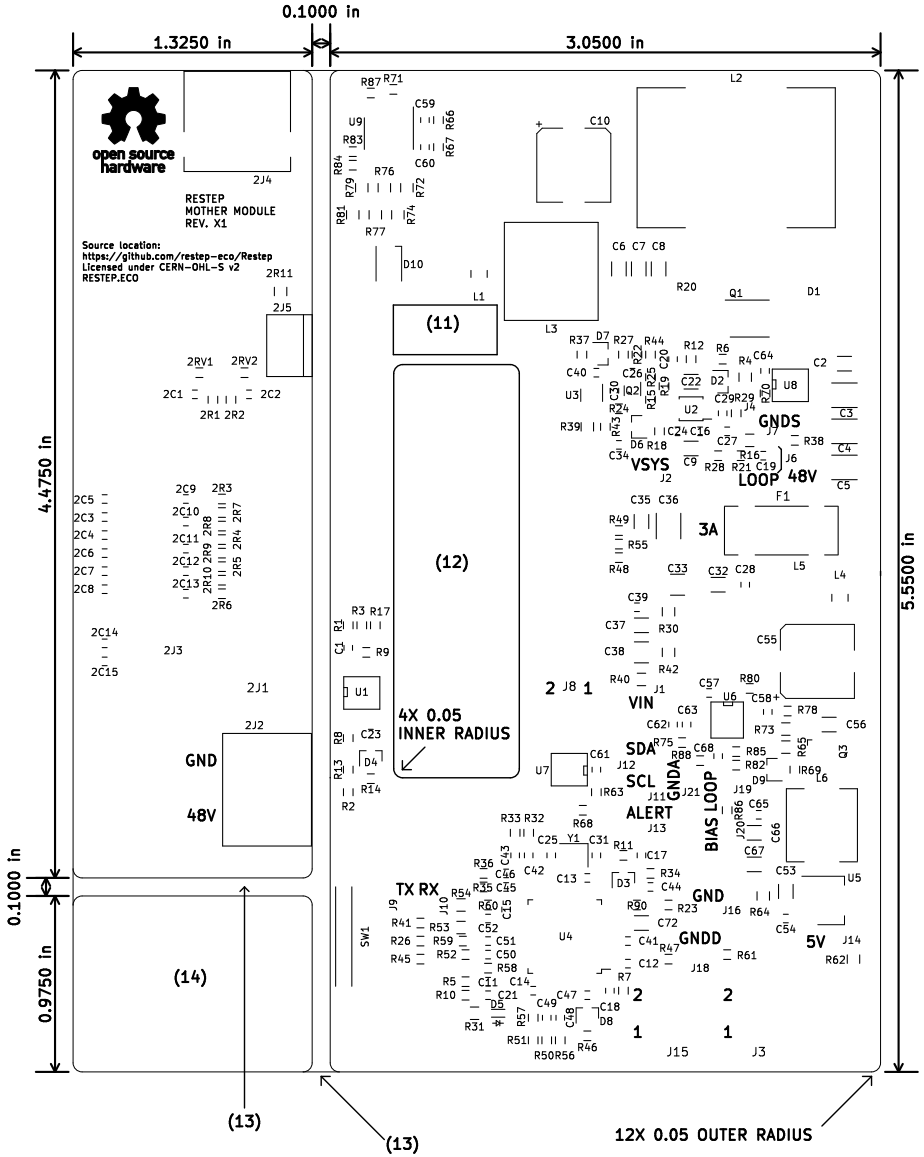

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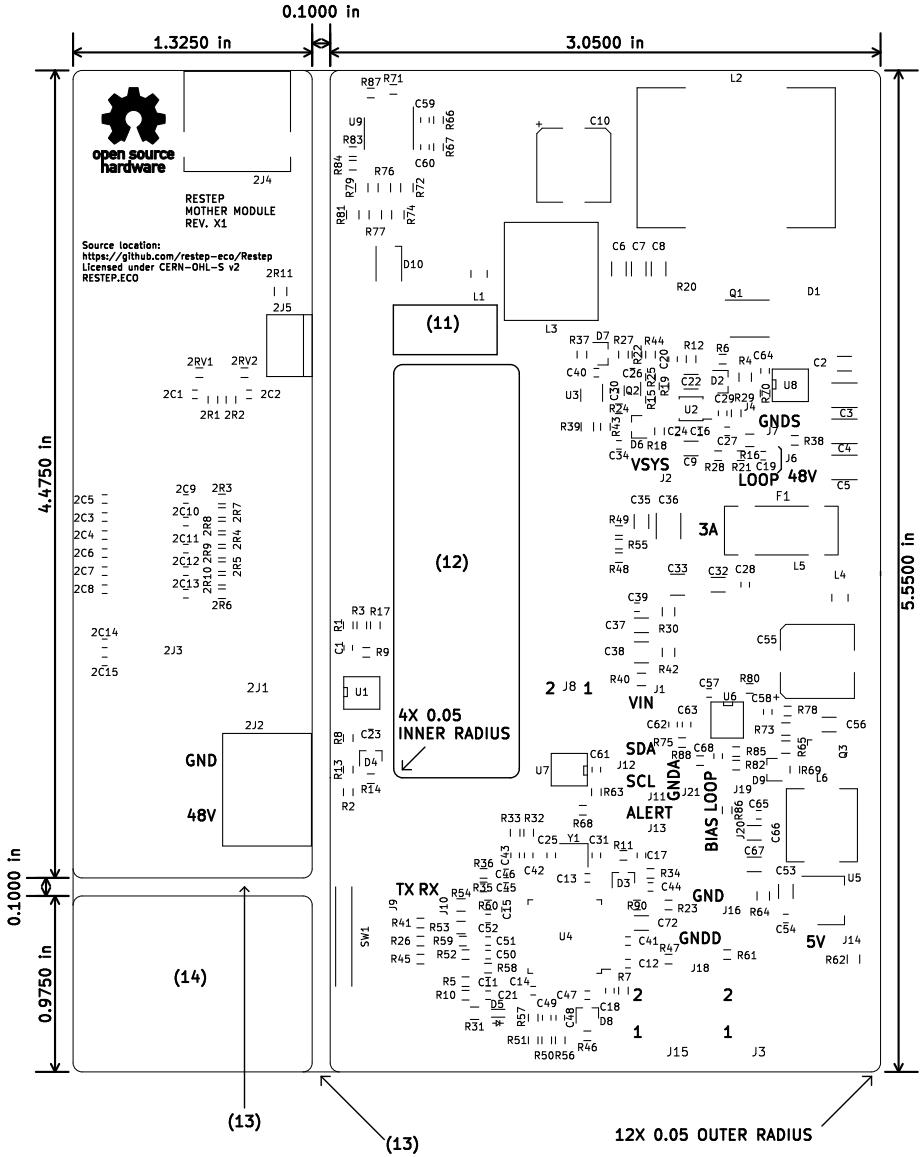

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