A Library of Circuits

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Chapter 1

Basic Operational Amplifier Circuits

Operational amplifiers are extremely useful and versatile circuits. This chapter presents basic application circuits which use operational amplifiers for amplification, buffering, summing, integrating, etc.

Basic analysis of op amp circuits uses the following properties of an ideal op amp:

1. Input impedance is very high / infinite for the inverting and non-inverting inputs, implying zero / negligible input bias current for both inputs.

2. Output impedance is (nearly) 0.

3. Very high / infinite open loop gain, implying that *with negative feedback* an op amp's inputs must be at (nearly) the same voltage in order to produce a finite output.

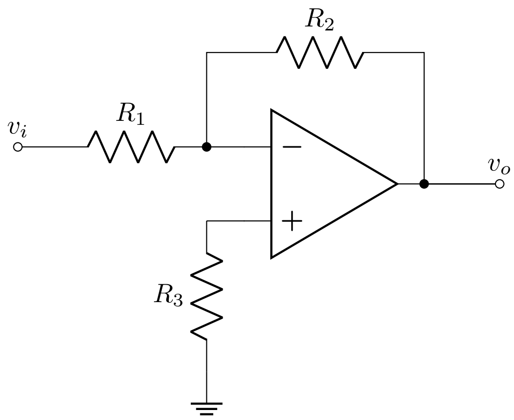
While these ideal properties can simplify the analysis of op amp circuits, it is important not to completely neglect an op amp's non-idealities. For example, an op amp's inputs much each have a Direct Current (DC) path for the small but nonzero input bias currents to flow to ground – without such a path an input bias current will bias the op amp's input to an undesired voltage.

Relaxing these assumptions will result in a more complicated but realistic analysis (especially when substituting with values from a real op amp whose specifications are available), which may allow the design to be substantially improved. For example, it is more realistic to assume that an op amp's input bias currents are nonzero but equal in magnitude and direction. This assumption leads to the principle that the equivalent impedances to ground at each input should be equal so that the input bias currents produce equal (small) bias voltages at each input, thus minimizing the offset voltage caused by imbalanced bias voltages.

Many of the following circuits' gain is determined by a ratio of resistors, which makes the circuits very insensitive to temperature if the resistors are manufactured by the same process. All circuit elements are temperature dependent, but since the gain is determined by a ratio of resistors the change in resistance of one resistor due to temperature should be very similar to the change in resistance of the other and the gain undergoes no net change. The op amp itself will exhibit temperature dependencies that affect the operation of the circuit, but modern op amps are designed to have very low temperature drifts so the op amp usually will not cause the circuit to become overly temperature sensitive.

The bandwidth of many op amp amplifiers depends on the gain since most op amps use voltage feedback (rather than current feedback), and such op amps have a constant gain-bandwidth product – increase the gain and the bandwidth decreases, decrease the gain and the bandwidth increases. The gain-bandwidth product depends on the particular op amp used to implement a circuit, so the bandwidth cannot be calculated for a generic op amp. Multiple op amp inverting (or non-inverting) amplifiers with lower individual gains can be cascaded to achieve a high bandwidth along with high overall gain if the specified gain and bandwidth of an application circuit exceeds an individual op amp's gain-bandwidth product.

1.1 Inverting amplifier



The op amp's non-inverting input has ideally no input bias current so no current flows through R_3 or C_1 and the non-inverting input is at ground potential. Due to the op amp's high open loop gain, the inverting input is also ideally at ground potential (this is a "virtual ground" condition) so Kirchhoff's Current Law (KCL) relates v_i and v_o through the inverting input node. There is ideally no input bias current into the op amp's inverting input so the current through R_1 (which is v_i/R_1) is equal to the current through R_2. The R_2 terminal connected to the inverting input is at ground potential so the voltage across R_2 is equal to v_o. The transfer function is therefore

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1} \tag{1.1}$$

Since the non-inverting input is at ground potential the input resistance is simply

$$R_i = R_1 \tag{1.2}$$

Unfortunately, this is considerably lower than the op amp's input impedance. R_i can be improved by maximizing R_1 (and therefore also R_2) while not making the resistors so high than the op amp's input bias currents produce a significant bias voltages.

R_3 is typically a short circuit, but may be set to

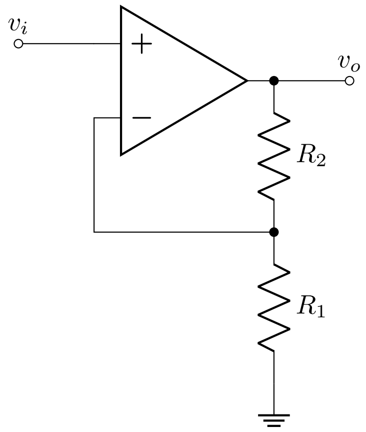
$$R_3 = R_1 \parallel R_2 \tag{1.3}$$

in order to balance the bias voltages produced by the op amp's input bias currents.

An optional capacitor may be placed in parallel with non-zero R_3 to reduce high frequency noise added by R_3. R_3 is only needed to produce a DC offset and has no effect on the signal's transfer function, but it produces white thermal noise that can be attenuated by the low pass filter (LPF) formed by R_3 and the capacitor in parallel.

A capacitor C may be inserted between v_i and R_1 if the amplifier must be Alternating Current (AC)-coupled. The op amp's inverting input is at virtual ground so the time constant is $\tau = R_1C$ and $f_c = 1/(2\pi R_1 C)$.

1.2 Non-inverting amplifier



The resistors form what is essentially a voltage divider network, with v_o as the voltage divider "input" and the op amp's inverting input as the voltage divider "output". The inputs of an op amp with negative feedback are ideally at the same voltage, so the voltage divider "output" is v_i. Such a voltage divider has the relation

$$v_i = \frac{R_1}{R_1 + R_2} v_o$$

Rearranging gives the transfer function:

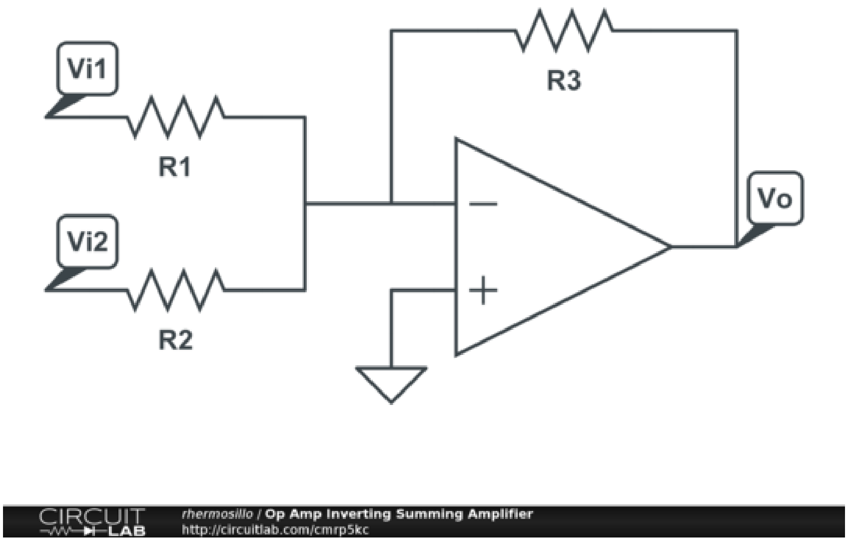
$$\frac{v_o}{v_i} = 1 + \frac{R_2}{R_1} \tag{1.4}$$

The transfer function shows that this circuit is a voltage buffer if $R_1 = R_2$, which is as simple as replacing the resistors with wires. The input impedance of this amplifier is the same as the op amp's input impedance, which is much higher than can be achieved with the inverting amplifier's R_i. The very high input impedance and very low output impedance of op amps ensures the non-inverting amplifier/buffer is a good voltage source.

One option if this amplifier must be AC-coupled is to add a passive RC filter in series with the input, which produces the first-order active high pass filter (HPF) shown on page 17. It is not enough to simply add a series capacitor – a resistor to GND is necessary to provide a DC path for the op amp's input bias current and to set the filter cutoff frequency. Set the resistor $R = R_1 \parallel R_2$ to minimize the error caused by the op amp's input bias currents, then set the capacitor C to achieve the desired cutoff frequency $f_c = 1/(2\pi RC)$. Unfortunately, this option reduces the amplifier's input resistance to $R_i = R$ in the passband.

Another option, if the signal is AC but DC does not need to be blocked, is to insert a capacitor C between R_1 and GND. The capacitor is an open circuit for DC, which makes the denominator in (1.4) very large and the DC gain approximately 1; in the passband the capacitor is a short circuit so the gain is unaffected. The capacitor sees an equivalent resistance to GND of $R_1 + R_2$ so the cutoff frequency is $f_c = 1/(2\pi(R_1 + R_2)C)$.

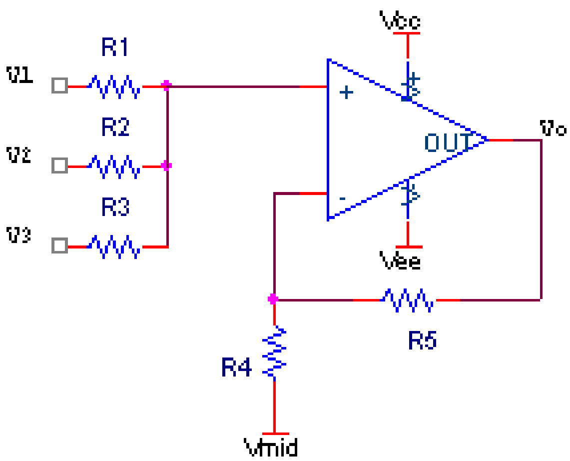
1.3 Inverting summing amplifier



This circuit multiplies each input voltage by a factor determined by a resistor ratio, sums these amplified voltages, and inverts the result. It is essentially an op amp inverting amplifier with multiple inputs. It is often used as an audio mixer, where multiple voltage signals must be combined into one (for example, voltage signals from multiple microphones which must be combined into one signal for recording). The transfer function can be found by superposition of the inputs and, for the two input case, is

$$v_o = -\left(\frac{R_3}{R_1}v_{i1} + \frac{R_3}{R_2}v_{i2}\right) \tag{1.5}$$

1.4 Non-inverting summing amplifier



The non-inverting summing amplifier is similar to the op amp non-inverting amplifier, except that it has multiple inputs. To analyze it, note that the inverting input voltage v_- is

$$v_- = \frac{R_4}{R_4 + R_5}v_o \tag{1.6}$$

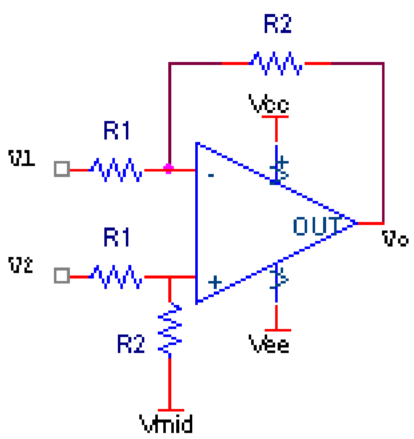
(assume for simplicity that $V_{\mathrm{REF}} = 0\,\mathrm{V}$) since R_4 and R_5 form a voltage divider. This is also the voltage at the non-inverting input and KCL can be used on the currents through the input resistors. This gives the transfer function:

$$v_o = \frac{R_4 + R_5}{R_4\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)}\left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right) \tag{1.7}$$

Determining the correct resistor values to use in order to achieve the desired gain for each input (and finding the standard resistor values that will do it) is slightly trickier than the inverting summing amplifier's case. For audio circuits the inverting summing amplifier is easier to work with since a voltage signal that has been inverted cannot be distinguished by the human ear from the same signal that has not – only amplitude and frequency matter in this case, not phase. Other applications may also allow for an inversion, but if not the non-inverting summing amplifier works well.

1.5 Difference Amplifiers

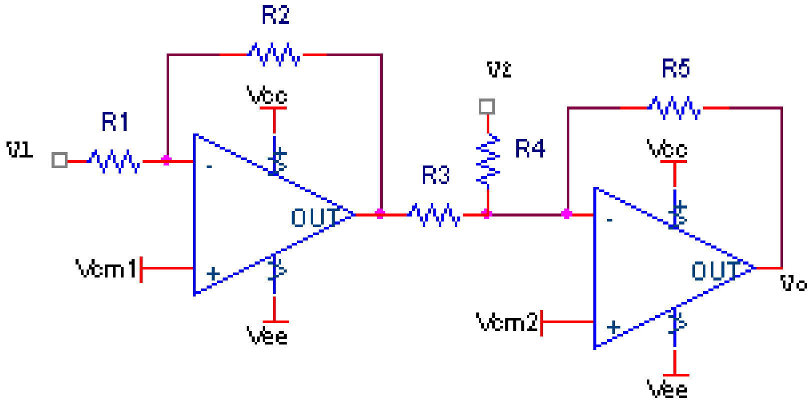
1.5.1 Basic difference amplifier



In this configuration each of the two inputs is connected to one of the op amp's inputs through a resistor (R_1). Two additional resistors are used: a feedback resistor from the output to the inverting input of the op amp, and another resistor of equal value from the non-inverting input of the op amp to the common mode voltage (usually $V_{CC}/2$ for a single supply system and GND for a dual supply system). Using the fact that an ideal op amp's inputs are at equal voltages and KCL on both the inverting and non-inverting inputs, the transfer function is

$$v_o = \frac{R_2}{R_1}(v_2 - v_1) \tag{1.8}$$

1.5.2 High common-mode range difference amplifier



This improved difference amplifier allows for a higher common-mode range because the resistors in series with the signal inputs v_1 and v_2 (R_1 and R_4, respectively) limit the currents into the op amps' inputs, increasing the voltage range within the op amp's drive capability. (Mancini, *Op Amps for Everyone*, p. 418)

The transfer function can be derived easily using superposition and the above transfer functions for inverting and non-inverting op amp amplifiers to determine v_o in terms of all four inputs (v_1, v_2, V_{CM1}, and V_{CM2}). For v_1,

$$v_o = \frac{R_2}{R_1}\frac{R_5}{R_3}v_1, v_2 = V_{\mathrm{CM1}} = V_{\mathrm{CM2}} = 0 \tag{1.9}$$

(the output of the first op amp is $-(R_2/R_1)v_1$, which is then amplified by $-R_5/R_3$). For v_2,

$$v_o = -\frac{R_5}{R_4}v_2, v_1 = V_{\mathrm{CM1}} = V_{\mathrm{CM2}} = 0 \tag{1.10}$$

For V_{CM1},

$$v_o = -\left(1 + \frac{R_2}{R_1}\right)\frac{R_5}{R_3}V_{\mathrm{CM1}}, v_1 = v_2 = V_{\mathrm{CM2}} = 0 \tag{1.11}$$

For V_{CM2},

$$v_o = \left(1 + \frac{R_5}{R_3 \parallel R_4}\right)V_{\mathrm{CM2}} = \left(1 + \frac{(R_3 + R_4)R_5}{R_3 R_4}\right)V_{\mathrm{CM2}}, v_1 = v_2 = V_{\mathrm{CM2}} = 0 \tag{1.12}$$

Putting it all together,

$$v_o = \frac{R_2}{R_1}\frac{R_5}{R_3}v_1 - \frac{R_5}{R_4}v_2 - \left(1 + \frac{R_2}{R_1}\right)\frac{R_5}{R_3}V_{\mathrm{CM1}} + \left(1 + \frac{(R_3 + R_4)R_5}{R_3 R_4}\right)V_{\mathrm{CM2}} \tag{1.13}$$

If all the resistors are equal, the transfer function simplifies to

$$v_o = v_1 - v_2 - 2V_{\mathrm{CM1}} + 3V_{\mathrm{CM2}} \tag{1.14}$$

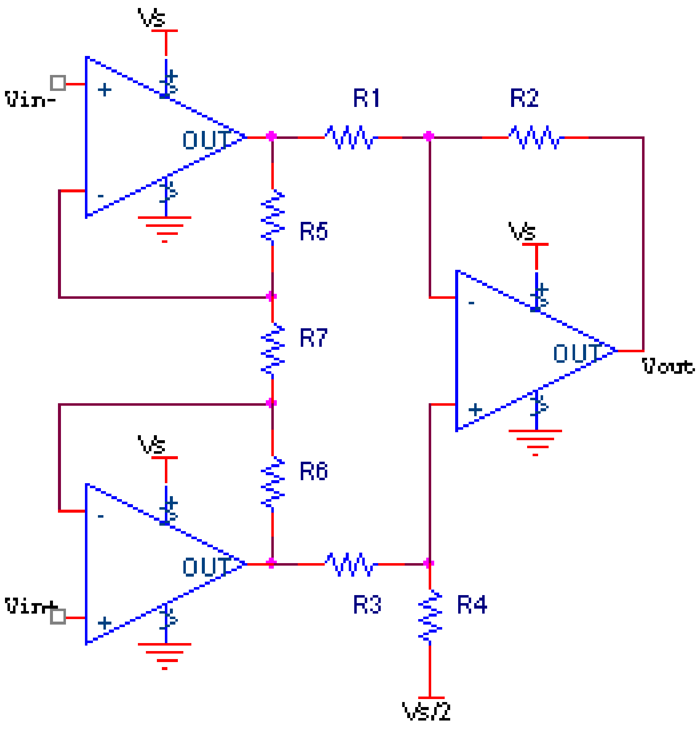
Chapter 2

Instrumentation Amplifiers

Instrumentation amplifiers are differential amplifiers just like operational amplifiers – in fact, instrumentation amplifiers are constructed out of several operational amplifiers. Instrumentation amplifiers, or in amps, have an extremely high input impedance. This high input impedance is often achieved with a three op amp topology, using two of the op amps as input buffers or non-inverting amplifiers. The in amp's input impedance is much higher than the op amp difference amplifier previously discussed, so the in amp is able to measure a differential voltage with much better accuracy. In amps are often used to calibrate electronic instruments (hence the name *instrumentation* amplifier) or to directly measure the small voltage signals from sensors (such as pressure transducers), voltage references, test equipment, etc.

While in amps can be constructed out of discrete op amps and resistors, the input op amps and all the resistors must be highly matched in order to minimize undesirable characteristics such as input offset voltage, common mode gain, etc. As a result, in amps are usually constructed in integrated circuit form.

2.1 Three op amp topology instrumentation amplifier



This is the standard, symmetric topology using three op amps. To maintain symmetry (which, in this case, ensures each input voltage is amplified by the same amount), we must have

$$R_5 = R_6 \tag{2.1}$$

$$R_1 = R_3 \tag{2.2}$$

$$R_2 = R_4 \tag{2.3}$$

The input differential voltage is

$$v_{diff} = v_{in+} - v_{in-} \tag{2.4}$$

and it is the voltage across R_7 since the voltages at the inverting inputs of the input op amps are equal to the input voltages. The current through R_7 is thus

$$i_{R7} = \frac{v_{diff}}{R_7} \tag{2.5}$$

The differential voltage between the two input op amps' outputs (call it v_{o1}) is

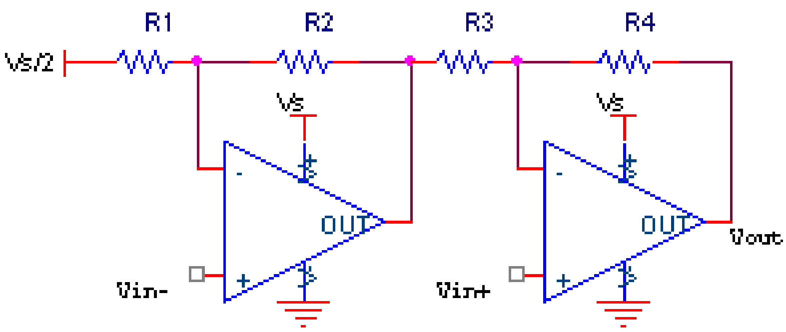
$$v_{o1} = i_{R7}(R_5 + R_6 + R_7) = i_{R7}(2R_5 + R_7) = v_{diff}(1 + 2\frac{R_5}{R_7}) \tag{2.6}$$

The output op amp is configured as a difference amplifier with v_{o1} as the input so the overall gain A_v is

$$A_v = \frac{R_2}{R_1}(1 + 2\frac{R_5}{R_7}) \tag{2.7}$$

R_5 and R_6 can be shorted and R_7 removed (replaced with an open circuit) to reduce the number of resistors – this configures the input op amps as buffers. The disadvantage, of course, is that the output op amp must be configured with a higher gain in order to achieve the same overall gain, which will reduce the in amp's bandwidth.

2.2 Two op amp topology instrumentation amplifier



This in amp topology is less common but uses only two op amps, which can be useful to minimize the number of op amps used in the application circuit or to minimize power consumption. As with the three op amp topology, resistors must be matched:

$$R_1 = R_4 \tag{2.8}$$

$$R_2 = R_3 \tag{2.9}$$

The transfer function is

$$A_v = 1 + \frac{R_1}{R_2} \tag{2.10}$$

Unfortunately, this topology requires the v_{in-} op amp to be used with less than unity gain (so it may be unstable) and the v_{in-} signal has a higher propagation delay than the v_{in+} signal. Depending on the application circuit and the op amps available, the three op amp topology may have to be used instead.

Chapter 3

Filters

This chapter presents a variety of filters using either passive or active components. First and second order filters are presented so that an nth-order filter can be constructed by cascading these first and/or second order filters.

Some of these filters can be designed either as Butterworth or Chebyshev filters. Butterworth filters are characterized by their maximally flat magnitude in the pass band for all-pole filters (so that, for all-pole filters, they are the best approximation to an ideal filter in the pass band). Unfortunately, the magnitude of a Butterworth filter poorly approximates an ideal filter near the cutoff frequency in that the magnitude does not drop particularly sharply from the pass band to the stop band. Higher order Butterworth filters transition more sharply and thus better approximate an ideal filter, but they are still inferior at the cutoff frequency to filters like the Chebyshev filter. Chebyshev filters' magnitude response best approximates an ideal filter for all-pole filters in that the magnitude drops very sharply from the pass band to the stop band, but their frequency response has ripples in the pass band (i.e. the magnitude oscillates in the pass band, particularly near the cutoff frequency). Higher order Chebyshev filters transition even more sharply than lower order Chebyshev filters. Thus, Butterworth and Chebyshev filters solve different problems – the former approximates an ideal filter best in the pass band while the latter is a better approximation near the cutoff frequency. (Johnson and Jayakumar, *Operational Amplifier Circuits: Design and Application*, pp. 107, 111)

Filter transfer functions are given as a function of the complex frequency-domain variable $s = \sigma + \jmath\omega$, where the angular frequency ω in rad/s is related to the frequency f in Hz as

$$f = \frac{\omega}{2\pi} \tag{3.1}$$

The filter transfer function, typically denoted $H(s)$, can be expressed as a rational function of polynomials with real coefficients:

$$H(s) = H_0 \frac{\sum\limits_{i=0}^{m} a_i s^i}{\sum\limits_{i=0}^{n} b_i s^i} \tag{3.2}$$

where H_0 is the passband gain (Zumbahlen, *Basic Linear Design*, p. 8.5). The degree of the denominator determines the order of the filter, and a higher order is required to achieve a sharper cutoff from passband to stopband.

A passive filter (which uses no active components) is limited to $|H_0| \leq 1$. Additionally, passive filter sections often require (active) buffer(s) at their input and/or output to isolate them from a high source impedance and/or low load impedance, respectively. Furthermore, higher order filters are often constructed by cascading multiple lower order filters – and buffers will likely need to be inserted between lower order filters if they are passive. The result is that all but the simplest filters require active component(s). Analyses of passive filters in this chapter assume low source and high load impedances.

Filters' transfer functions are characterized by the cutoff frequency f_c, angular cutoff frequency ω_c, and/or the time constant τ in s. f_c and ω_c are related by (3.1), and τ to the cutoff frequencies by

$$\tau = \frac{1}{\omega_\mathrm{c}} = \frac{1}{2\pi f_\mathrm{c}} \tag{3.3}$$

Second and higher order filters are also characterized by the dimensionless "quality factor" Q or alternatively as the damping ratio

$$\alpha = \frac{1}{Q} \tag{3.4}$$

The damping ratio may alternatively be expressed as

$$\zeta = 2\alpha = \frac{2}{Q} \tag{3.5}$$

A filter with high Q is underdamped, exhibiting peaking in the frequency response and oscillation that eventually converges to a steady-state value in the step response (ibid., p. 8.7).

Below are general forms for filters of various types and orders (for second-order equations see ibid., p. 8.13):

$$\text{1st-order LPF: } H(s) = H_0 \frac{\omega_\mathrm{c}}{\omega_\mathrm{c} + s} = H_0 \frac{1}{1 + \tau s} \tag{3.6}$$

$$\text{1st-order HPF: } H(s) = H_0 \frac{s}{\omega_\mathrm{c} + s} = H_0 \frac{\tau s}{1 + \tau s} \tag{3.7}$$

$$\text{2nd-order LPF: } H(s) = H_0 \frac{\omega_\mathrm{c}^2}{s^2 + \frac{\omega_\mathrm{c}}{Q} s + \omega_\mathrm{c}^2} \tag{3.8}$$

$$\text{2nd-order HPF: } H(s) = H_0 \frac{s^2}{s^2 + \frac{\omega_\mathrm{c}}{Q} s + \omega_\mathrm{c}^2} \tag{3.9}$$

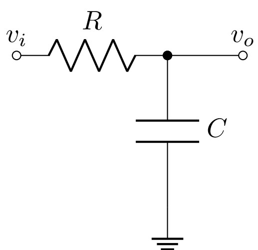
$$\text{2nd-order BPF: } H(s) = H_0 \frac{\frac{\omega_\mathrm{c}}{Q} s}{s^2 + \frac{\omega_\mathrm{c}}{Q} s + \omega_\mathrm{c}^2} \tag{3.10}$$

$$\text{2nd-order BRF: } H(s) = H_0 \frac{s^2 + \omega_\mathrm{z}^2}{s^2 + \frac{\omega_\mathrm{c}}{Q} s + \omega_\mathrm{c}^2} \tag{3.11}$$

Since s is proportional to frequency, we can determine a filter's low frequency response by evaluating its $H(s)$ as $s \to 0$ and its high frequency response by evaluating its $H(s)$ as $s \to \infty$.

3.1 First-order low and high pass filters

3.1.1 First-order RC passive low pass filter



Viewing the resistor and capacitor as an impedance divider:

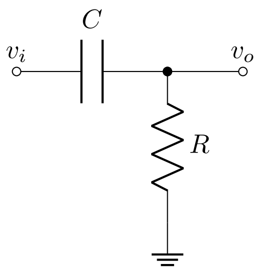
$$v_o = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} v_i$$

Rearranging, this is

$$\frac{v_o}{v_i}(s) = H(s) = \frac{1}{1 + sRC} \tag{3.12}$$

By inspection its cutoff frequency is $\omega_c = 1/(RC)$.

3.1.2 First-order RC passive high pass filter



Compared to the LPF, the resistor and capacitor have been switched so the impedance divider is

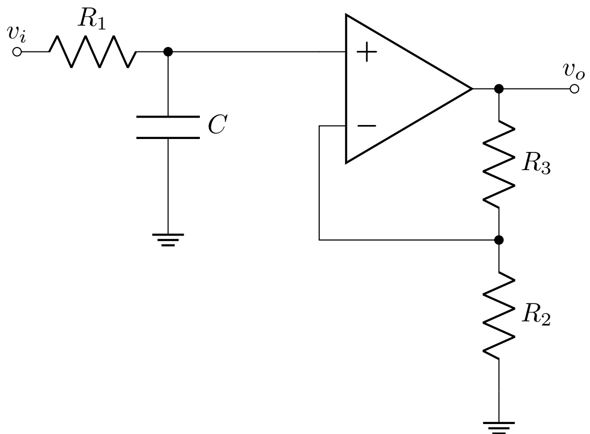
$$v_o = \frac{R}{R + \frac{1}{sC}} v_i$$

Rearranged, this is

$$\frac{v_o}{v_i}(s) = H(s) = \frac{sRC}{1 + sRC} \tag{3.13}$$

By inspection its cutoff frequency is $\omega_c = 1/(RC)$.

3.1.3 First-order non-inverting active low pass filter



This circuit is simply a cascade of the RC passive LPF and the non-inverting amplifier. The transfer function is thus

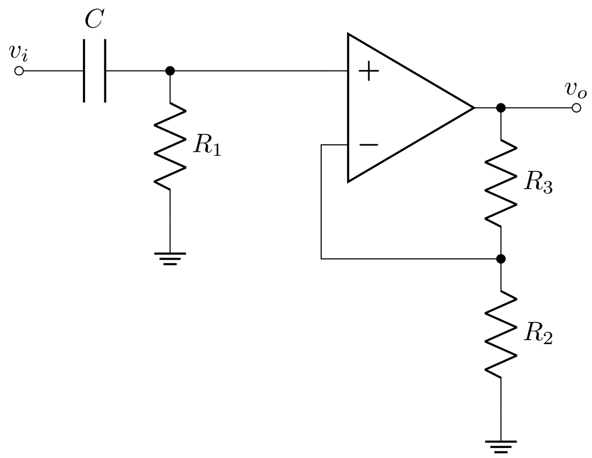
$$\frac{v_o}{v_i}(s) = H(s) = \left(1 + \frac{R_3}{R_2}\right)\left(\frac{1}{1 + sR_1C}\right) \tag{3.14}$$

As usual, the resistors should be chosen such that $R_1 = R_2 \parallel R_3$ to minimize the error due to the op amp's input bias currents.

In this circuit R_1 and C perform the same filtering function as the passive RC filter so the op amp isn't strictly necessary – however, the op amp provides gain for the filter and can provide isolation of the RC filter from other circuit elements which might affect its performance. If gain is not needed, the op amp can be configured as a voltage buffer by removing R_2 and replacing R_3 with a short.

If R_2 and R_3 are used, the three resistors should be chosen such that the filter formed by R_1 and C has the desired cutoff frequency and $R_1 = R_2 \parallel R_3$ (the latter relationship minimizes the error due to the op amp's input bias currents).

3.1.4 First-order non-inverting active high pass filter



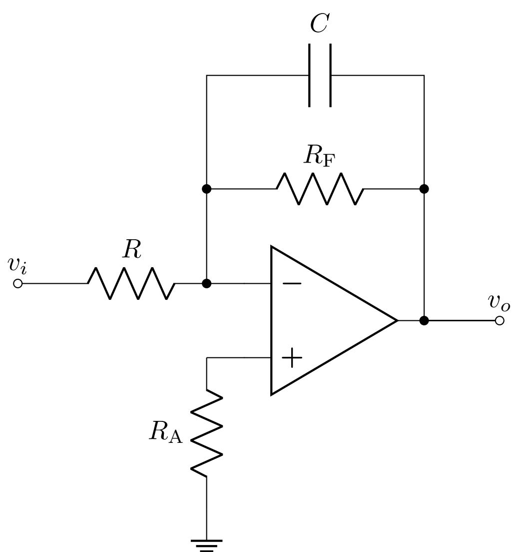
This circuit is simply a cascade of the RC passive HPF and the non-inverting amplifier. The transfer function is thus

$$\frac{v_o}{v_i}(s) = H(s) = \left(1 + \frac{R_3}{R_2}\right)\left(\frac{sR_1C}{1 + sR_1C}\right) \tag{3.15}$$

As usual, the resistors should be chosen such that $R_1 = R_2 \parallel R_3$ to minimize the error due to the op amp's input bias currents.

In this circuit R_1 and C perform the same filtering function as the passive RC filter so the op amp isn't strictly necessary – however, the op amp provides gain for the filter and can provide isolation of the RC filter from other circuit elements which might affect its performance. If gain is not needed, the op amp can be configured as a voltage buffer by removing R_2 and replacing R_3 with a short.

3.1.5 First-order inverting active low pass filter



This circuit is the same as the inverting amplifier from section 1.1, but with a capacitor in parallel with the feedback resistor so that the feedback impedance is

$$Z_{\mathrm{F}} = R_{\mathrm{F}} \parallel C = \frac{R_{\mathrm{F}}/(sC)}{R_{\mathrm{F}} + 1/(sC)} = \frac{R_{\mathrm{F}}}{1 + sR_{\mathrm{F}}C}$$

Substituting this impedance into (1.1) we obtain

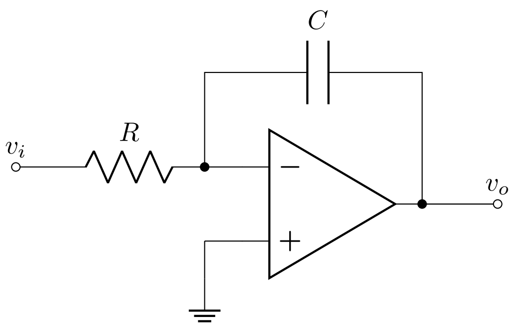
$$\frac{v_o}{v_i}(s) = H(s) = -\frac{R_{\mathrm{F}}}{R}\left(\frac{1}{1 + sR_{\mathrm{F}}C}\right) \tag{3.16}$$

To minimize the error due to the op amp's input bias current, set $R_{\mathrm{A}} = R \parallel R_{\mathrm{F}}$; if this error is negligible R_{A} can be replaced with a short circuit.

3.2 Integrator and Differentiator

3.2.1 Inverting Integrator

An ideal but impractical integrator circuit is:



The inverting input's voltage is at GND and the non-inverting input is at a virtual ground. The voltage across R is thus equal to $v_i(t)$ and the current through it is

$$i_i(t) = v_i(t)/R$$

By KCL on the inverting input node and the fact that the input bias current into the op amp's inverting input is negliglible, $i_i(t)$ is also the current through the capacitor. The voltage across C is $-v_o(t)$ so

$$i_i(t) = -C\frac{\mathrm{d}v_o(t)}{\mathrm{d}t}$$

Equating the two expressions for $i_i(t)$ and solving for $v_o(t)$:

$$v_o(t) = \frac{-1}{RC}\int v_i(t)\,\mathrm{d}t + V_O \tag{3.17}$$

where V_O is the initial output voltage.

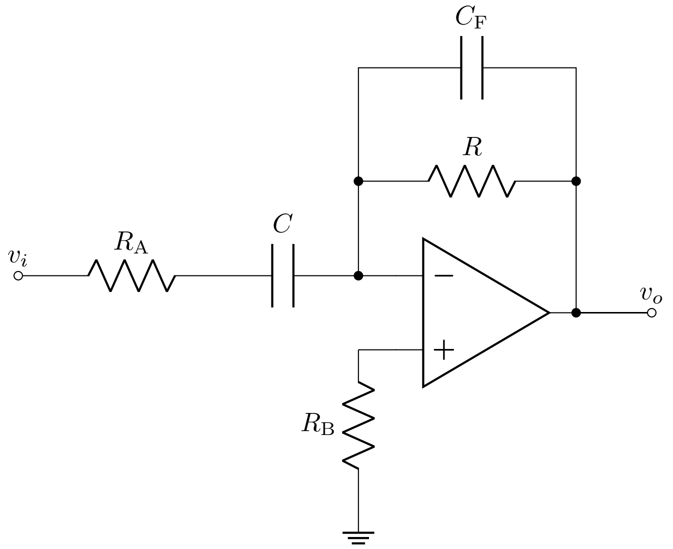
The transfer function in the frequency domain can be derived using KCL at the inverting input node and the capacitor's impedance $1/(sC)$:

$$\frac{v_o}{v_i}(s) = H(s) = -\frac{1}{sRC} \tag{3.18}$$

Unfortunately, C is an open circuit at DC so the ideal integrator provides no DC feedback for the op amp. To avoid operating the op amp with an open loop, it is necessary to add a finite resistor R_{F} in parallel with C. Such **a practical integrator is the same as the inverting active LPF** given in subsection 3.1.5. Its transfer function given in (3.16) simplifies to (3.18) as $R_\mathrm{F} \to \infty$ since $sR_\mathrm{F}C \gg 1 \implies 1 + sR_\mathrm{F}C \approx sR_\mathrm{F}C$, so the R_F terms in the numerator and denominator cancel.

The practical integrator acts as an inverting amplifier for frequencies below $\omega_\mathrm{c} = 1/(R_\mathrm{F}C)$ and as an integrator for frequencies above ω_c. The difference between a a LPF and integrator is that the frequencies of interest are below ω_c for the former and above ω_c for the latter. Also, the integrator should minimize ω_c and maximize the "passband" gain for more ideal behavior; setting R_F as high as possible while staying within the capabilities of the op amp achieves both of these objectives. Relevant specifications of the op amp for determining R_F include its gain-bandwidth product, input offset voltage (which is amplified at the output by the DC gain of the circuit), and input bias current (which flows through R_F and introduces an error voltage).

3.2.2 Inverting Differentiator



Since differentiation is the opposite of integration, the operating principle of the differentiator circuit is to build an integrator but swap the placement of R and C. The ideal differentiator is also similar to the inverting op amp amplifier except that the resistor in series between the input and the op amp's inverting input is replaced with a capacitor. The circuit shown above is a practical differentiator which includes some necessary components for a real implementation, but an ideal differentiator has $R_\mathrm{A} = C_\mathrm{F} = 0$ (i.e., the resistor is a short circuit and the feedback capacitor is an open circuit). For the ideal differentiator, the inverting input's voltage is equal to GND (the op amp's input bias current produces a negligible voltage across R_B) and the non-inverting input is at a virtual ground. The capacitor voltage is thus equal to $v_i(t)$ and by definition the current through it is $i_i(t)$, so

$$i_i(t) = C\frac{\mathrm{d}v_i(t)}{\mathrm{d}t}$$

KCL on the inverting input node means that $i_i(t) = -v_o(t)/R$ also, which relates the input to the output:

$$C\frac{\mathrm{d}v_i(t)}{\mathrm{d}t} = -\frac{v_o(t)}{R}$$

Solving for $v_o(t)$, we find that it is proportional to the derivative of $v_i(t)$:

$$v_o(t) = -RC\frac{\mathrm{d}v_i(t)}{\mathrm{d}t} \tag{3.19}$$

Another way to represent the transfer function is in the frequency domain. KCL on the inverting input node using the capacitor's impedance $1/(sC)$ relates the input to the output as

$$\frac{v_o(s)}{R} = -\frac{v_i(s)}{1/(sC)} = -v_i(s)sC$$

Rearranging gives the transfer function as

$$\frac{v_o}{v_i}(s) = -sRC \tag{3.20}$$

Unfortunately, the ideal differentiator tends to be unstable and is sensitive to high frequency noise. Both of these problems are due to the fact that the gain increases as frequency increases – the circuit's gain is theoretically infinite at very high frequencies (though a real op amp's finite gain and bandwidth will limit the high frequency gain). To address these problems a practical differentiator introduces R_{A} and C_{F}. Substituting the practical differentiator's impedances into (1.1) we have:

$$\frac{v_o}{v_i}(s) = -\frac{R \parallel 1/(sC_{\mathrm{F}})}{R_{\mathrm{A}} + 1/(sC)}$$

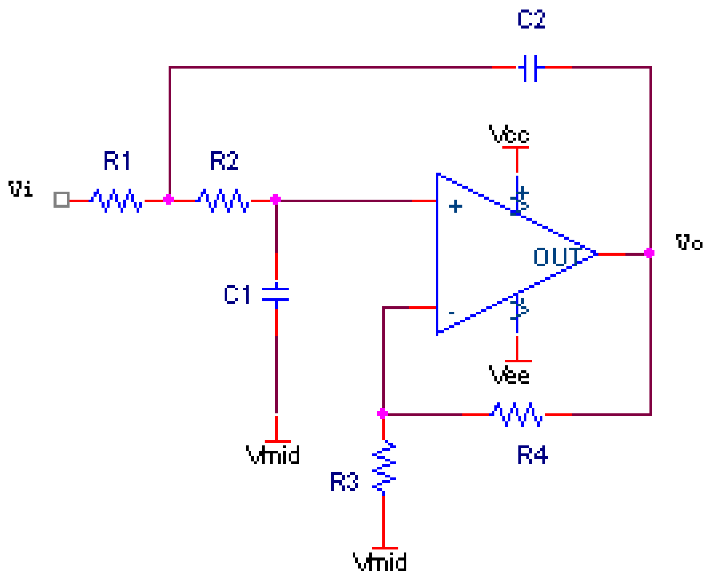
From this equation it is clear that at high frequencies ($s \to \infty$, where C is a short circuit), R_{A} in series with C prevents the denominator from approaching 0. After some algebra we obtain:

$$\frac{v_o}{v_i}(s) = \frac{-sRC}{(1 + sR_{\mathrm{A}}C)(1 + sRC_{\mathrm{F}})} \tag{3.21}$$

This equation shows that the practical differentiator has a zero at $s = 0$ (like the ideal differentiator) but also poles at $s = 1/(R_{\mathrm{A}}C)$ and $s = 1/(RC_{\mathrm{F}})$, resulting in corner frequencies of $f_{\mathrm{A}} = 1/(2\pi R_{\mathrm{A}}C)$ and $f_{\mathrm{B}} = 1/(2\pi RC_{\mathrm{F}})$. The practical differentiator is a second-order BPF since its transfer function has the form of (3.10), though the differentiator is intended to be used for frequencies below the passband. f_{A} and f_{B} are chosen so that the lower corner frequency is at the maximum signal frequency to be differentiated, and the higher corner frequency is at a low enough frequency to keep the op amp stable.

3.3 Second-order low and high pass filters

3.3.1 Second-order VCVS active low pass filter



This second order VCVS low pass filter is similar in topology to the the above first order low pass filter except that it includes an extra resistor and capacitor. The full derivation of the input/output relationship requires a somewhat lengthy manipulation of equations, but it requires only three facts: (1) the voltage at the input terminals, which is $\frac{R_3}{R_3+R_4}v_o$ (again assuming that $v_{\mathrm{MID}} = 0\,\mathrm{V}$), (2) the nodal equation at the non-inverting input, and (3) the nodal equation at the node common to R_1, R_2, and C_2. This circuit is a second order filter so the transfer function is of the form

$$\frac{v_o}{v_i}(s) = H(s) = \frac{Kb\omega_c^2}{s^2 + a\omega_c s + b\omega_c^2} \tag{3.22}$$

In this case

$$b\omega_c^2 = \frac{1}{R_1 R_2 C_1 C_2} \tag{3.23}$$

$$a\omega_c = \frac{1}{C_2}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{R_4}{R_2 R_3 C_1} \tag{3.24}$$

$$K = 1 + \frac{R_4}{R_3} \tag{3.25}$$

To minimize the error due to the op amp's input bias currents we need

$$R_3 \parallel R_4 = R_1 + R_2 \tag{3.26}$$

With these restrictions and a desired gain K and ω_c we have the following equations for deciding the resistor and capacitor values (Johnson and Jayakumar, *Operational Amplifier Circuits: Design and Application*, pp. 118–119):

$$C_1 \leq \frac{(a^2 + 4b(K-1))C_2}{4b} \tag{3.27}$$

$$R_1 = \frac{2}{(aC_2 + \sqrt{(a^2 + 4b(K-1))C_2^2 - 4bC_1C_2})\omega_c} \tag{3.28}$$

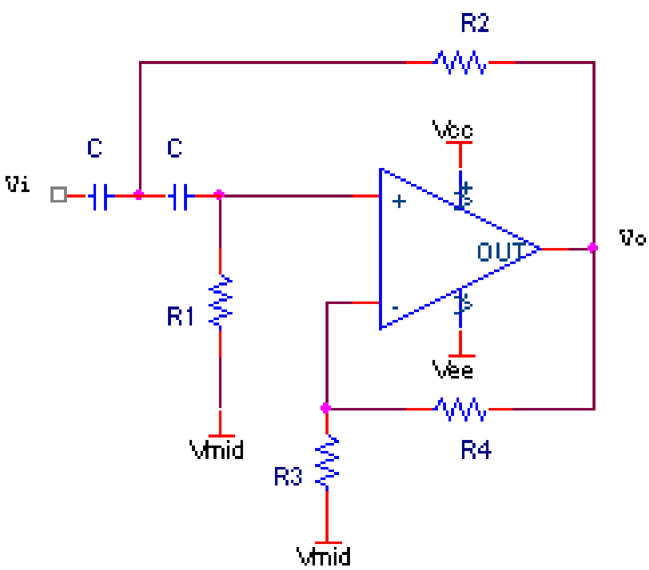
$$R_2 = \frac{1}{bC_1C_2R_1\omega_c^2} \tag{3.29}$$

$$R_3 = \frac{K(R_1 + R_2)}{K-1}, K > 1 \tag{3.30}$$

$$R_4 = K(R_1 + R_2) \tag{3.31}$$

The parameters a and b depend on the type of filter desired – Butterworth or Chebyshev. Check Butterworth and Chebyshev coefficient tables for these parameter values.

3.3.2 Second-order VCVS high pass filter



The VCVS second-order high pass filter is the same as the VCVS second-order low pass filter but with the resistors replaced with capacitors and the capacitors replaced by resistors (except for the resister divider). Using the general transfer function for a second-order high pass filter

$$\frac{v_o}{v_i}(s) = H(s) = \frac{Ks^2}{s^2 + \frac{a}{b}\omega_c s + \frac{\omega_c^2}{b}} \tag{3.32}$$

the resistors determine the transfer function as follows (Johnson and Jayakumar, *Operational Amplifier Circuits: Design and Application*, pp. 130–131):

$$R_1 = \frac{4b}{(a + \sqrt{a^2 + 8b(K-1)})\omega_c C} \tag{3.33}$$

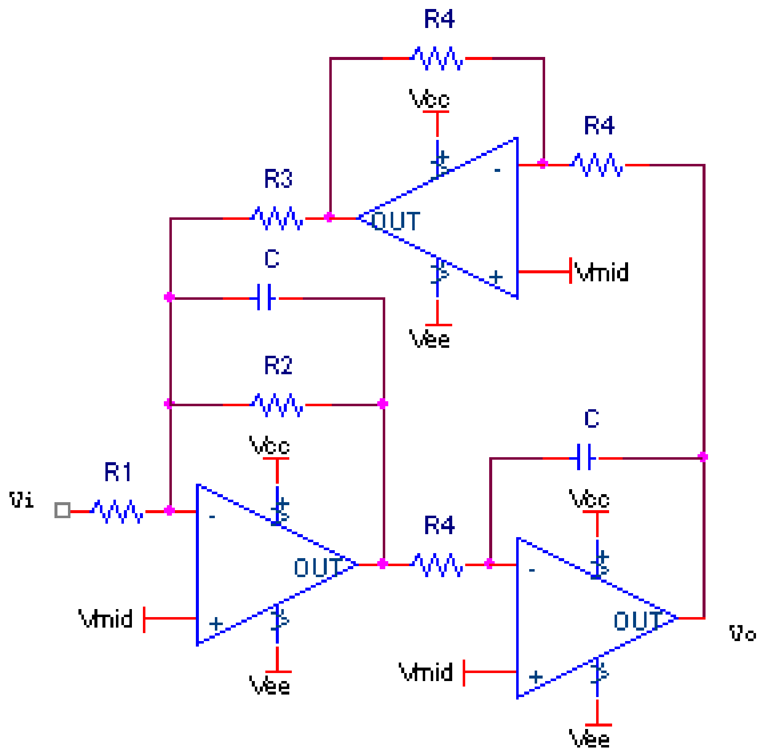
$$R_2 = \frac{b}{\omega_c^2 C^2 R_1} \tag{3.34}$$

$$R_3 = \frac{KR_1}{K-1}, K > 1 \tag{3.35}$$

$$R_4 = KR_1 \tag{3.36}$$

If no gain is needed (i.e. $K = 1$) R_3 can be removed and R_4 replaced with a short.

3.3.3 Second-order biquad low pass filter



The biquad filter requires two more op amps than the above VCVS filters. Two of the op amps are used as integrators and the third is an inverter. The two integrators (which, of course, are low pass filters) form a second order low pass filter. The transfer function can be determined by nodal analysis and noting the functions of each of the three op amps, but the full analysis is skipped. Instead, the resistors and capacitors are simply given in terms of the general second-order low pass filter transfer function

$$\frac{v_o}{v_i}(s) = H(s) = \frac{Kb\omega_c^2}{s^2 + a\omega_c s + b\omega_c^2} \tag{3.37}$$

The resistors relate to the general transfer function as follows:

$$R_4 = \frac{1}{\omega_c C} \tag{3.38}$$

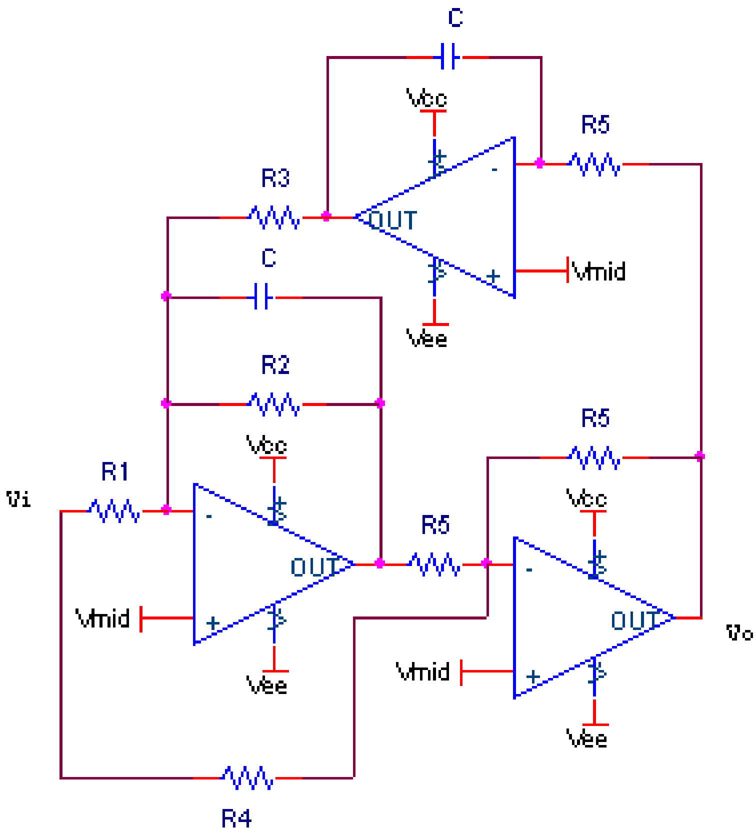
$$R_1 = \frac{R_4}{Kb} \tag{3.39}$$

$$R_2 = \frac{R_4}{a} \tag{3.40}$$

$$R_3 = \frac{R_4}{b} \tag{3.41}$$

Why use the biquad circuit with its three op amps when a second order filter can be built with only one op amp? Notice that the above equations for the biquad circuit's resistor and capacitor choices that the biquad is easier to tune than the VCVS filters. In particular, the desired ω_c determines the values of C and R_4, and with R_4 chosen parameter a is determined solely by R_2, parameter b can be determined by R_3, and with R_3 determined R_1 can be used to set the filter's gain K. The VCVS filters require two different capacitor values and the resistors affect one or more values of a, b, and K in nontrivial ways. The biquad circuit's offer of simpler tuning may be worth the two additional op amps. (ibid., pp. 120–122)

3.3.4 Second-order biquad high pass filter



This circuit is a biquad filter that implements the general second-order high pass filter transfer function

$$\frac{v_o}{v_i}(s) = H(s) = \frac{Ks^2}{s^2 + \frac{a}{b}\omega_c s + \frac{\omega_c^2}{b}} \tag{3.42}$$

with an inverting gain (i.e. $K < 0$). The resistors relate to the transfer function as follows (ibid., p. 131):

$$R_1 = \frac{b}{aK\omega_c C} \tag{3.43}$$

$$R_2 = KR_1 \tag{3.44}$$

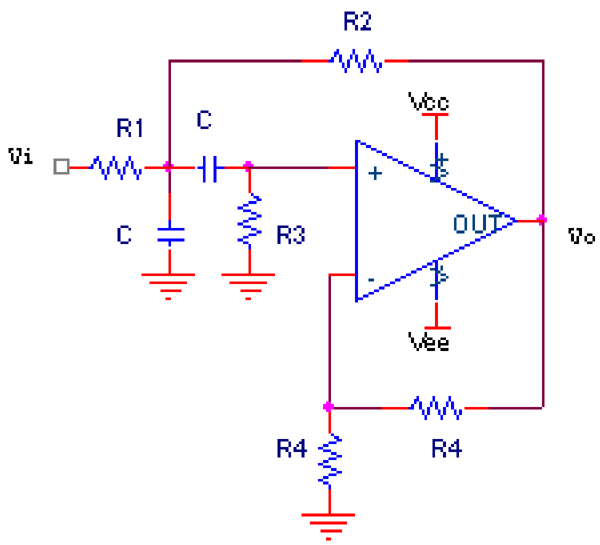
$$R_3 = \frac{b}{\omega_c C} \tag{3.45}$$

$$R_4 = \frac{1}{K\omega_c C} \tag{3.46}$$

$$R_5 = \frac{1}{\omega_c C} \tag{3.47}$$

3.4 Band pass filters

3.4.1 VCVS band pass filter



The general equation for the transfer function of this filter is

$$\frac{v_o}{v_i}(s) = H(s) = \frac{\alpha\omega_c s}{s^2 + \beta\omega_c s + \gamma\omega_c^2} \tag{3.48}$$

Since this is a band pass filter $v_o/v_i \approx 0$ as $s \to 0$ and $s \to \infty$ but the gain is nonzero in the midband. The resistors are related to the transfer function as follows (Johnson and Jayakumar, *Operational Amplifier Circuits: Design and Application*, pp. 138–139):

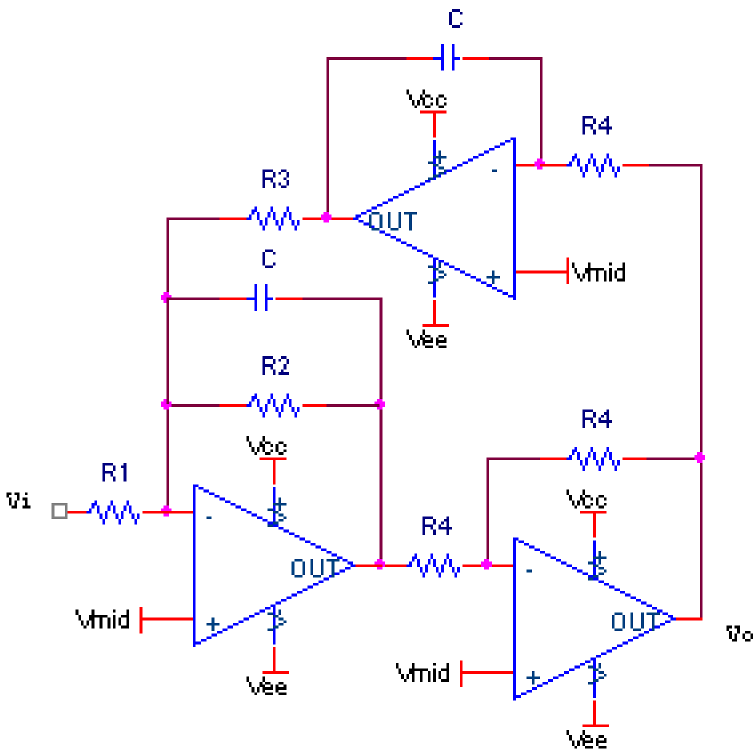
$$R_1 = \frac{2}{\alpha\omega_c C} \tag{3.49}$$

$$R_2 = \frac{2}{(-\beta + \sqrt{(\alpha-\beta)^2 + 8\gamma})\omega_c C} \tag{3.50}$$

$$R_3 = \frac{1}{\gamma\omega_c^2 C^2}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{3.51}$$

$$R_4 = 2R_3 \tag{3.52}$$

3.4.2 Biquad band pass filter



The biquad band pass filter has the same transfer function as the VCVS band pass filter:

$$\frac{v_o}{v_i}(s) = H(s) = \frac{\alpha\omega_c s}{s^2 + \beta\omega_c s + \gamma\omega_c^2} \tag{3.53}$$

with the four resistors related to the transfer function as

$$R_1 = \frac{1}{\alpha\omega_c C} \tag{3.54}$$

$$R_2 = \frac{1}{\beta\omega_c C} \tag{3.55}$$

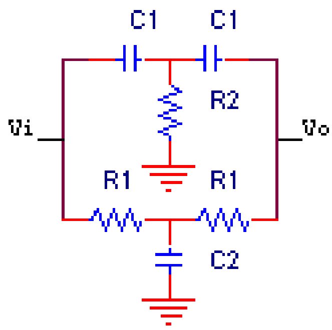
$$R_3 = \frac{1}{\gamma\omega_c C} \tag{3.56}$$

$$R_4 = \frac{1}{\omega_c C} \tag{3.57}$$

Again, the VCVS band pass filter is simpler than the biquad but the latter is easier to tune than the former. (ibid., p. 140)

3.5 Band reject filters

3.5.1 Passive Twin-T band reject filter



The intuitive way to understand that this circuit is a band reject filter is to realize that these are two T circuits in parallel – one T circuit is composed of the two R_1 resistors and C_2 capacitor, and the other T circuit is composed of the two C_1 capacitors and R_2 resistor. Consider each T individually: the T circuit with the two resistors is a low pass filter since C_2 shorts the middle node to ground for high frequency signals and passes low frequency signals, and the T circuit with the two capacitors blocks low frequency signals but shorts v_i to v_o for high frequency signals. Low frequencies can pass through the low pass T circuit and high frequencies can pass through the high pass T circuit, but there is a middle frequency that can pass through neither. Thus, this Twin-T circuit is a band reject filter.

There are several methods for deriving the notch frequency, but the derivation is lengthy and not presented here. The result of the derivation (see Bond, *Problems and Solutions in Mathematics, Physics and Applied Sciences - Design Notes: Twin 'T' RC Notch Filter*) is

$$R_1C_1 = 4R_2C_2 \tag{3.58}$$

and

$$\omega^2 = \frac{1}{2R_1R_2C_2^2} \tag{3.59}$$

Usually the components are chosen such that $R_2 = R_1/2$ and $C_2 = 2C_1$. In that case, the notch frequency is

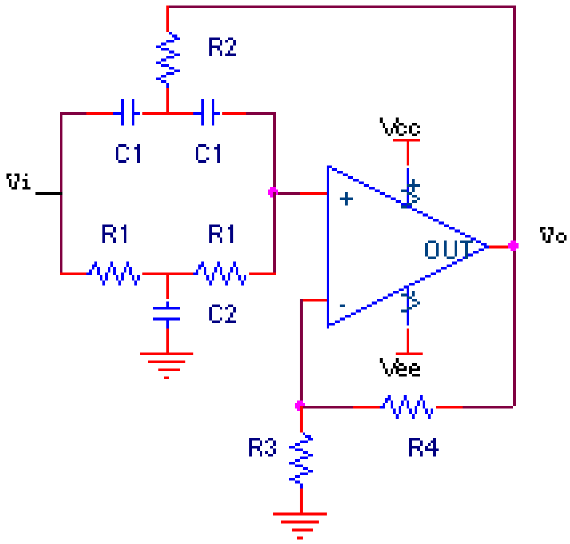
$$f = \frac{\omega}{2\pi} = \frac{1}{2\pi R_1C_1} \tag{3.60}$$

The limitation of this circuit is its quality factor $Q = 1/\Delta\Omega$, where $\Delta\Omega$ is the difference between the $-3\,\text{dB}$ frequencies just above and below the notch frequency f. For the passive Twin-T band reject filter,

$$Q = \frac{1}{4} \tag{3.61}$$

An active Twin-T band reject filter (which uses the Twin-T topology in the feedback path of an operational amplifier) improves Q. (Mancini, *Op Amps for Everyone*, p. 321)

3.5.2 Active Twin-T band reject filter



The active Twin-T band reject filter adds an operational amplifer to the passive Twin-T filter. The operational amplifier provides an increased gain and Q since it is an active element. R_4 provides negative feedback and R_3 sets the gain in the pass band (the filter circuitry has a gain of appoximately 1 in the pass band, so the circuit is essentially a non-inverting op amp amplifier). The pass band gain K is thus simply

$$K = 1 + \frac{R_4}{R_3} \tag{3.62}$$

The filter circuitry itself is configured the same as that of the passive Twin-T filter, with the passive version's output node connected to the operational amplifier's non-inverting input and R_2 connected to the active filter's output. Since the filter circuitry is the same, so is the notch frequency f. Assuming the typical case of $R_2 = R_1/2$ and $C_2 = 2C_1$,

$$f = \frac{1}{2\pi R_1 C_1} \tag{3.63}$$

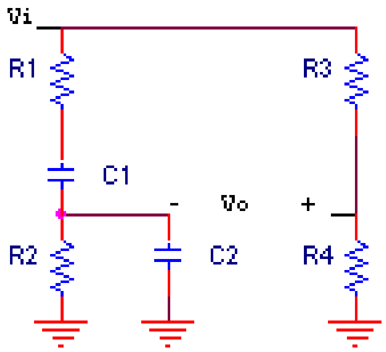
It can be shown (ibid., p. 322) that the active Twin-T filter's Q is

$$Q = \frac{1}{2(2-k)} = \frac{R_3}{2(R_3 - R_4)} \tag{3.64}$$

With K and Q given in terms of the circuit components, the overall transfer function can be written in terms of the circuit components as well:

$$\frac{v_o}{v_i}(s) = H(s) = \frac{K(s^2+1)}{s^2 + \frac{s}{Q} + 1} = \frac{\frac{R_3+R_4}{R_3}(s^2+1)}{s^2 + \frac{2(R_3-R_4)}{R_3}s + 1} \tag{3.65}$$

3.5.3 Passive Wien-Robinson band reject filter



The Wien-Robinson band reject filter takes a single-ended input and produces a differential output. It can be analyzed intuitively by realizing that it is composed of a voltage divider (R_3 and R_4) in parallel with a band pass filter. R_1, R_2, C_1, and C_2 form a band pass filter because C_1 blocks low frequencies (no current passes through C_1 to create a voltage across R_2 and C_2) and C_2 shorts the band pass filter's output (the negative terminal of v_o) to ground, but midrange frequencies are passed to the output. The overall circuit acts as a band reject filter because at low and high frequencies the negative terminal of v_o is grounded so that

$$v_o = \frac{R_3}{R_2 + R_3} v_i$$

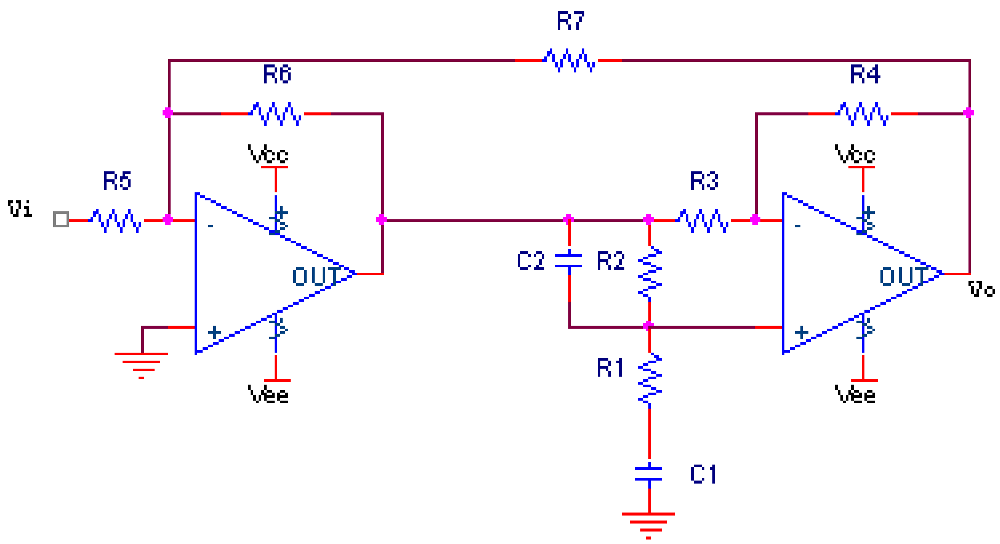
At middle frequencies v_i is passed to the negative terminal of v_o so that the terminals of v_o are equal and $v_o = 0$.

This circuit suffers from a low Q (Mancini, *Op Amps for Everyone*, p. 323), just as the passive Twin-T band reject filter (the two have similar values of Q). It too can be improved with the use of operational amplifiers.

Typically the component values are chosen such that $R_1 = R_2$ and $C_1 = C_2$. In that case the notch frequency (ibid., p. 324) is

$$f = \frac{1}{2\pi R_1 C_1} \tag{3.66}$$

3.5.4 Active Wien-Robinson band reject filter



The active Wien-Robinson band reject filter uses two operational amplifiers to improve the passive Wien-Robinson filter's Q and gain. The resistors and capacitors which compose the passive Wien-Robinson filter are labeled the same in the above schematic of the active version as in the passive version from before. The inputs of the operational amplifier which drives the overall output are driven by the filter's differential output. The other operational amplifier is configured simply as an inverting amplifier. The transfer function (ibid., p. 323) can be written as

$$\frac{v_o}{v_i}(s) = H(s) = \frac{\frac{R_6 R_7}{R_5(R_6+R_7)}(s^2+1)}{s^2 + \frac{3R_7}{R_6+R_7}s + 1} \tag{3.67}$$

If $R_1 = R_2$ and $C_1 = C_2$ as is typical, then

$$f = \frac{1}{2\pi R_1 C_1} \tag{3.68}$$

since the filtering circuitry is unchanged from the passive version. Q can be determined by inspection since it is the coefficient of the first order s term,

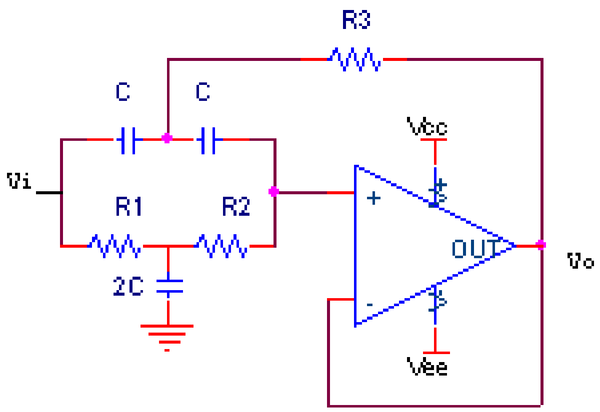
$$Q = \frac{3R_7}{R_6 + R_7} \tag{3.69}$$

and the active filter's passband gain K can also be determined by inspection:

$$K = \frac{R_6 R_7}{R_5(R_6 + R_7)} \tag{3.70}$$

The active Wien-Robinson band reject filter differs from its active Twin-T counterpart in that the passband gain k can be chosen without affecting the quality factor Q.

3.5.5 VCVS band reject filter



This band reject filter's transfer function can be written in the form

$$\frac{v_o}{v_i}(s) = \frac{s^2 + \omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2} \tag{3.71}$$

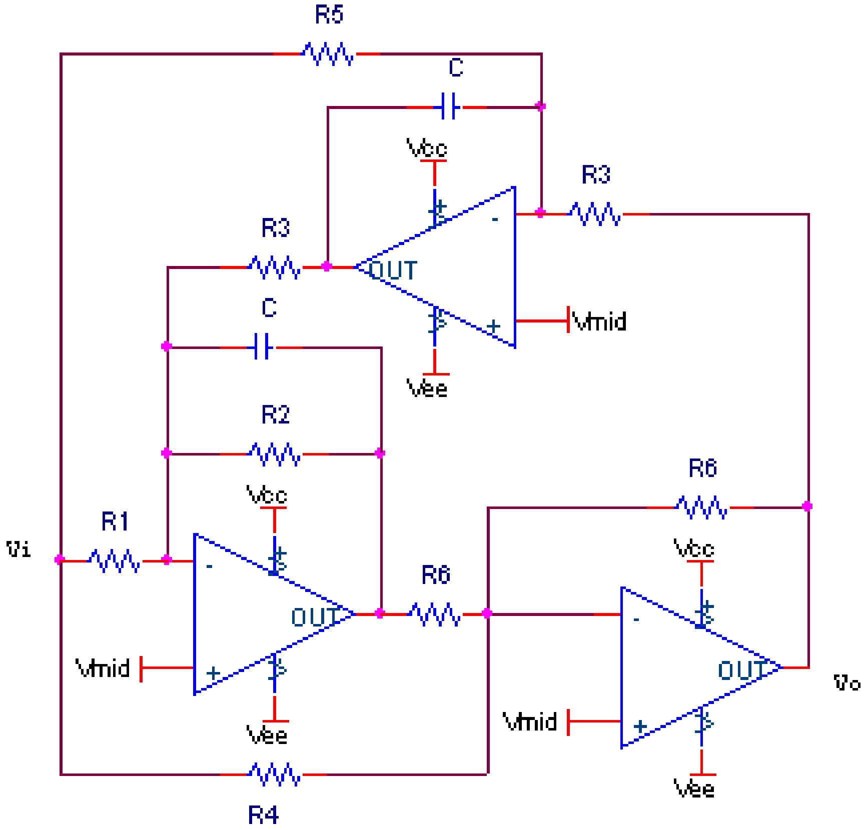
The op amp is configured as a voltage follower and, since it is the only active device in the circuit, the overall gain of this filter can never exceed unity even in the pass band. To achieve the desired transfer function the resistors must be chosen as follows (Johnson and Jayakumar, *Operational Amplifier Circuits: Design and Application*, pp. 145–146):

$$R_1 = \frac{1}{2Q\omega_c C} \tag{3.72}$$

$$R_2 = \frac{2Q}{\omega_c C} \tag{3.73}$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \tag{3.74}$$

3.5.6 Biquad band reject filter



A band reject filter's transfer function can also be written in the form

$$\frac{v_o}{v_i}(s) = H(s) = \frac{\alpha(s^2 + \omega_c^2)}{s^2 + \beta\omega_c s + \gamma\omega_c^2} \tag{3.75}$$

Unlike the VCVS band reject filter above, this biquad filter can provide an inverting gain greater than unity (the α term), and it can also achieve a much higher Q. The resistors relate to the transfer function as (Johnson and Jayakumar, *Operational Amplifier Circuits: Design and Application*, pp. 146–148)

$$R_1 = \frac{1}{\alpha\beta\omega_c C} \tag{3.76}$$

$$R_2 = \alpha R_1 \tag{3.77}$$

$$R_3 = \frac{1}{\sqrt{\gamma}\omega_c C} \tag{3.78}$$

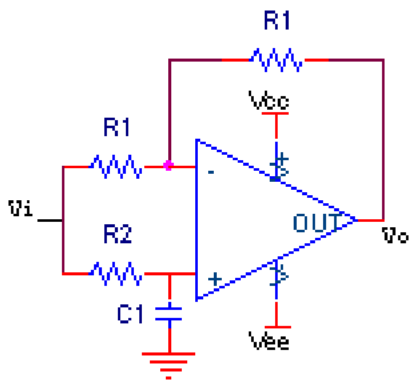
$$R_4 = \frac{1}{\alpha\omega_c C} \tag{3.79}$$

$$R_5 = \frac{\sqrt{\gamma}}{\alpha\omega_c C} \tag{3.80}$$

$$R_6 = \frac{1}{\omega_c C} \tag{3.81}$$

3.6 All pass filters

3.6.1 First-order all pass filter



This circuit (Mancini, *Op Amps for Everyone*, p. 328) has a gain of 1 at low frequencies and -1 at high frequencies. At low frequencies, neither the capacitor nor the non-inverting input of the operational amplifier draw any current, so there is no voltage drop across R_2 and the non-inverting input has a voltage equal to v_i. The inverting input also has a voltage equal to v_i since the operational amplifier's inputs must be at (approximately) equal voltage, so there is no voltage drop across the R_1 connected to v_i. Since there is no voltage drop across (or current through) the R_1 connected to v_i, there is no current through (or voltage drop across) the R_1 connected to v_o. Thus, $v_o = v_i$ at low frequencies. At high frequencies, the non-inverting input of the operational amplifier is shorted to ground since the capacitor has a very low impedance. R_2 does nothing to the circuit since it is only connected to v_i and GND and the circuit looks like an inverting op amp amplifier, which of course has a gain of -1 when the gain and feedback resistors (R_1, in this case) are equal.

It is not intuitively obvious, however, that the circuit has a gain of magnitude 1 in the middle of the frequency spectrum, so we need to derive the transfer function. Let the voltage at the operational amplifier's inputs be v_x. R_2 and C_1 act as a voltage divider for v_i at the operational amplifier's inverting input, so

$$v_x = \frac{\frac{1}{sC_1}}{R_2 + \frac{1}{sC_1}} v_i = \frac{v_i}{1 + sR_2C_1} \tag{3.82}$$

The operational amplifier's non-inverting input is also at voltage v_x (ideally), so use KCL at the non-inverting input node:

$$\frac{v_o - v_x}{R_1} = \frac{v_x - v_i}{R_1} \tag{3.83}$$

Substituting for v_x, we have

$$\frac{v_o}{R_1} - \frac{v_i}{R_1(1 + sR_2C_1)} = \frac{v_i}{R_1(1 + sR_2C_1)} - \frac{v_i}{R_1} \tag{3.84}$$

Rearranging, we have

$$v_o = v_i \left(\frac{2}{1 + sR_2C_1} - 1 \right) \tag{3.85}$$

Rearranging further, the transfer function is thus

$$\frac{v_o}{v_i}(s) = \frac{1 - sR_2C_1}{1 + sR_2C_1} \tag{3.86}$$

The transfer function reveals a zero at $s = 1/(R_2C_1)$ and a pole at $s = -1/(R_2C_1)$ (technically, the operational amplifier introduces its own poles to the system so that the gain does actually go to zero at very high frequencies, but we are assuming that the frequencies of operation are well below the operational amplifier's poles). In any case, the gain has constant magnitude $|H(s)| = |H(\jmath\omega)|$ across the (operational) frequency spectrum since

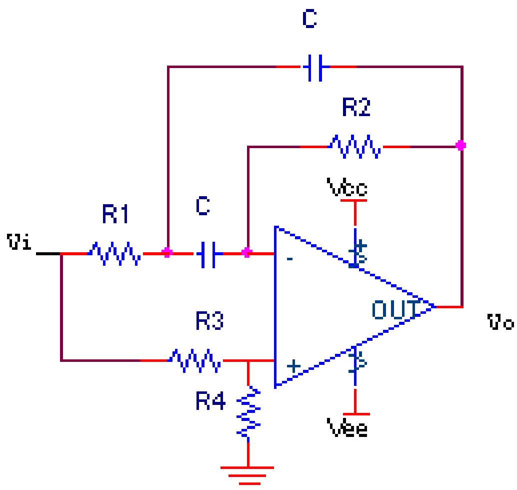
$$|H(\jmath\omega)| = \frac{\sqrt{1 + (-\omega R_2C_1)^2}}{\sqrt{1 + (\omega R_2C_1)^2}} = 1 \tag{3.87}$$

so the circuit is an all pass filter. The point of an all pass filter is that it can change a system's phase response across the frequency spectrum – the phase changes from 0 to $-\pi$ radians from low to high frequency. More specifically, the phase $\angle H(s) = \angle H(\jmath\omega)$ is

$$\angle H(\jmath\omega) = \tan^{-1}(-\omega R_2C_1) - \tan^{-1}(\omega R_2C_1) = -2\tan^{-1}(\omega R_2C_1) \tag{3.88}$$

Although the values of R_2 and C_1 do not affect the magnitude of the circuit's gain across the frequency spectrum, they must be chosen appropriately to shape the circuit's phase response over frequency as desired. R_1 can be any reasonable value, of course, since the R_1 resistors do not directly affect the transfer function.

3.6.2 Second-order all pass filter



A second order all pass filter has the transfer function

$$\frac{v_o}{v_i}(s) = H(s) = \frac{K(s^2 - a\omega_c s + b\omega_c^2)}{s^2 + a\omega_c s + b\omega_c^2} \tag{3.89}$$

since this transfer function has two poles and

$$|H(\jmath\omega)| = K\frac{\sqrt{(b\omega_c^2 - \omega^2) + (-a\omega_c\omega)^2}}{\sqrt{(b\omega_c^2 - \omega^2) + (a\omega_c\omega)^2}} = K \tag{3.90}$$

The phase is

$$\angle H(\jmath\omega) = \tan^{-1}\left(-\frac{b\omega_c^2 - \omega^2}{a\omega_c\omega}\right) - \tan^{-1}\left(\frac{b\omega_c^2 - \omega^2}{a\omega_c\omega}\right) = -2\tan^{-1}\left(\frac{b\omega_c^2 - \omega^2}{a\omega_c\omega}\right) \tag{3.91}$$

This circuit implements the second order all pass filter transfer function, with the resistors chosen such that

$$a\omega_o = \frac{2}{R_2 C} \tag{3.92}$$

$$b\omega_o^2 = \frac{1}{R_1 R_2 C^2} \tag{3.93}$$

$$K = \frac{R_4}{R_3 + R_4} \tag{3.94}$$

$$4R_1 R_4 = R_2 R_3 \tag{3.95}$$

For minimum DC offset, choose (Johnson and Jayakumar, *Operational Amplifier Circuits: Design and Application*, pp. 151–153):

$$R_2 = \frac{R_3 R_4}{R_3 + R_4} \tag{3.96}$$

Chapter 4

Compensators

Compensators modify the loop transfer function $L(s)$ of a feedback system to stabilize the system or improve its performance. Compensators add one or more poles and/or zeros to $L(s)$ to change the feedback system's steady-state error, noise rejection, crossover frequency ω_c, phase margin ϕ_M, gain margin, etc. There are three types of compensators: lag, lead, and lead-lag compensators.

Lag compensators have a low frequency pole and a higher frequency zero so they have a transfer function of the form

$$G_c(s) = K\frac{\tau_1 s + 1}{\tau_2 s + 1}, \tau_1 < \tau_2$$

Lag compensators are typically used either to decrease $|L(s)|$ at high frequencies while maintaining a high $|L(s)|$ at low frequencies, or to increase $|L(s)|$ at low frequencies without also increasing $|L(s)|$ at high frequencies. The latter is more common, and decreases the system's steady state error and improves its disturbance rejection but maintains ω_c, ϕ_M, and (high frequency) noise rejection. (Lundberg, *Feedback Systems for Analog Circuit Design*, p. 269)

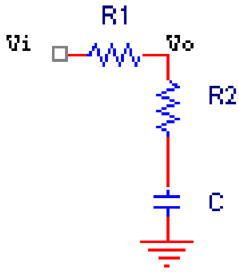
Lead compensators have a low frequency zero and high frequency pole so a lead compensator's transfer function is of the form

$$G_c(s) = K\frac{\alpha\tau_1 s + 1}{\tau_2 s + 1}, \tau_1 > \tau_2$$

The phase increases (i.e. moves away from $-\pi$) between the zero and pole's frequency, so ϕ_M can be increased if the zero and pole are placed such that ω_c is greater than the zero's frequency but less than the pole's frequency. The maximum increase in phase between the compensator's zero and pole is given by $\phi = \arcsin\frac{\alpha-1}{\alpha+1}$. A typical value of $\alpha = 10$ yields $\phi = 55^\circ$. α should not be too high, however, because the higher the value of α the greater the increase in high frequency gain (which reduces high frequency noise rejection). The easiest way to design a lead compensator is to place the zero at ω_c – if α is high enough (i.e. the pole is at a high enough frequency) the phase margin ϕ_M can be increased by approximately 45° and ω_c is not changed significantly. To maximize the increase in ϕ_M, however, the zero and pole should be placed such that their geometric mean is equal to ω_c. (ibid., pp. 277–278)

The benefits of both a lead and lag compensator can be acheived with a lead-lag compensator, which can be as simple as cascading a lag compensator and lead compensator. The lag compensator can improve the low frequency characteristics of the plant while the lead compensator improves the plant's transfer function near ω_c.

4.1 Passive lag compensator



This lag compensator is constructed out of passive components. It cannot achieve a gain greater than 1 (i.e. $K > 1$), of course, but in cases where such a gain is not necessary this compensator can reduce the feedback system's power consumption versus an active lag compensator. It is easy to see how this is a lag compensator: at low frequencies the capacitor is an open circuit so the impedance to ground is much higher than R_1 and $\frac{v_o}{v_i}(s) = 1$, and at high frequencies the capacitor is a short so R_1 and R_2 form a simple voltage divider which gives $\frac{v_o}{v_i}(s) = \frac{R_2}{R_1+R_2}$. To be more precise, this is a voltage divider consisting of impedances R_1 and $R_2 + \frac{1}{sC}$. The transfer function (ibid., p. 270) is therefore

$$\frac{v_o}{v_i}(s) = \frac{R_2 + \frac{1}{sC}}{R_1 + R_2 + \frac{1}{sC}} = \frac{sR_2C + 1}{1 + s(R_1 + R_2)C} \tag{4.1}$$

An alternative passive lag compensator places the capacitor in parallel with R_2 rather than in series with it:

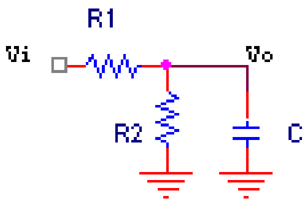


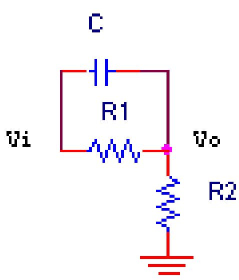
Figure 4.1: Alternative passive lag compensator

This too is a voltage divider, but this time the impedances are R_1 and $R_2 \parallel C$. The transfer function is $\frac{v_o}{v_i}(s) = \frac{R_2\|C}{R_1+R_2\|C} = \frac{R_2}{R_1+R_2+sR_1R_2C}$, which is best expressed as

$$\frac{v_o}{v_i}(s) = \frac{R_2}{R_1 + R_2} \frac{1}{1 + s(R_1 \parallel R_2)C} \tag{4.2}$$

to make the DC gain and the location of the pole obvious.

4.2 Passive lead compensator

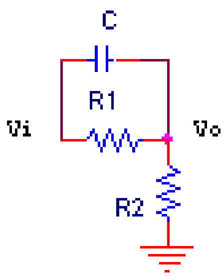


This lead compensator is very similar to the above passive lag compensator. In this case, at low frequencies the capacitor is an open circuit so R_1 and R_2 simply form a voltage divider to give $\frac{v_o}{v_i}(s) = \frac{R_2}{R_1+R_2}$, and at high frequencies the capacitor shorts R_1 so that $\frac{v_o}{v_i}(s) = 1$. The full analysis isn't much more difficult: this is an voltage divider consisting of impedances $R_1 || \frac{1}{sC} = \frac{R_1}{1+sR_1C}$ and R_2. The transfer function is thus

$$\frac{v_o}{v_i}(s) = \frac{R_2}{\frac{R_1}{sR_1C+1} + R_2} = \frac{R_2(sR_1C + 1)}{(R_1 + R_2)(s\frac{R_1R_2}{R_1+R_2}C + 1)} \tag{4.3}$$

The latter expression puts the transfer function in the $K\frac{\alpha\tau_1 s+1}{\tau_2 s+1}$ form to make the gain and time constants clear. (Lundberg, *Feedback Systems for Analog Circuit Design*, p. 278)

4.3 Passive lead-lag compensator



This lead-lag compensator provides the benefits of both a lead compensator and a lag compensator and does it entirely with passive components. Its transfer function is fairly easy to derive since this circuit is a voltage divider using the impedances $R_1 \parallel \frac{1}{sC}$ and R_2. Since

$$R_1 \parallel C = \frac{R_1}{1 + sR_1C} \tag{4.4}$$

we have

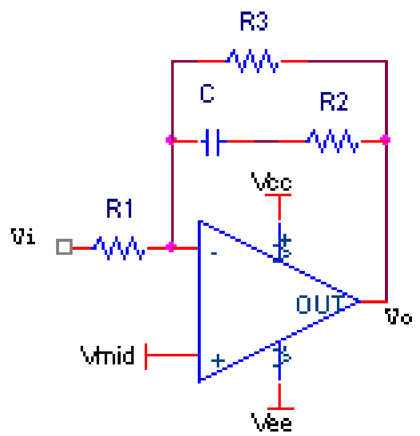
$$\frac{v_o}{v_i}(s) = \frac{R_2}{R_2 + \frac{R_1}{1+sR_1C}} = \frac{R_2(1 + sR_1C)}{R_1 + R_2 + sR_1R_2C} \tag{4.5}$$

By factoring out $R_1 + R_2$ we get

$$\frac{v_o}{v_i}(s) = \frac{R_2}{R_1 + R_2}\frac{1 + sR_1C}{1 + s(R_1 \parallel R_2)C} \tag{4.6}$$

The location of the zero is determined first by choosing appropriate values of R_1 and C, and R_2 determines the location of the pole.

4.4 Active lag compensator



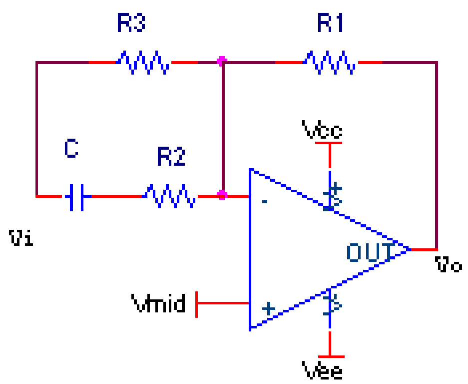
This is a basic lag compensator constructed with an operational amplifier so that a choice of $K > 1$ is possible. It is the same as an inverting amplifier except that a capacitor and resistor in series are placed in parallel with the feedback resistor. The same analysis can be used as the one for the inverting amplifer except that the feedback impedance is $R_3||(R_2 + \frac{1}{sC})$. The transfer function is

$$\frac{v_o}{v_i}(s) = -\frac{R_3}{R_1}\frac{1 + sR_2C}{1 + s(R_2 + R_3)C} \tag{4.7}$$

This compensator can also be used as a proportional-plus-integral (sometimes abbreviated P+I or PI) compensator by removing R_3 (ibid., p. 270):

$$\frac{v_o}{v_i}(s) = -\frac{1 + sR_2C}{sR_1C} \tag{4.8}$$

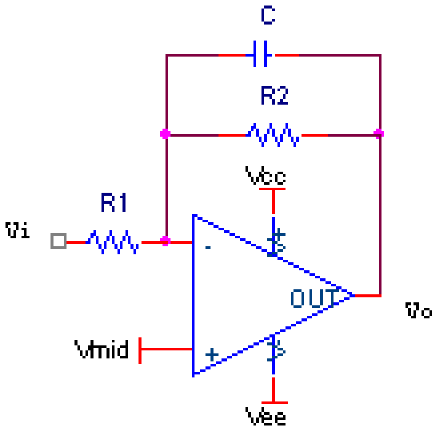
4.5 Active lead compensator



This is a fairly simple lead compensator which uses an operational amplifier to provide $K > 1$. It is the same as an inverting amplifier except that a capacitor and resistor in series are placed in parallel with the input resistor. The same analysis can be used as the one for the inverting amplifer except that the impedance from v_i to the op amp's inverting input is $R_3 \parallel (R_2 + \frac{1}{Cs})$. The transfer function (ibid., p. 278) is thus

$$\frac{v_o}{v_i}(s) = -\frac{R_1}{R_3}\frac{1 + s(R_2 + R_3)C}{1 + sR_2C} \tag{4.9}$$

4.6 Type I active compensator



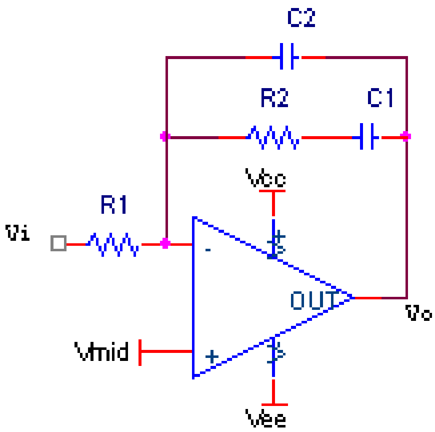
This compensator is essentially a low pass filter since it has a single pole and no zeroes. It can be used to lower the plant's gain at higher frequencies exactly as a low pass filter and thus improve high frequency noise rejection, or it can be used a dominant pole compensator if the DC gain $\frac{R_2}{R_1}$ is chosen sufficiently high and the compensator's pole is chosen to be a sufficiently low frequency. The transfer function is the same as that of an op amp in an inverting amplifier configuration, except that the feedback impedance is

$$R_2||C = \frac{R_2}{1 + sR_2C} \tag{4.10}$$

Thus it is

$$\frac{v_o}{v_i}(s) = -\frac{R_2}{R_1}\frac{1}{1 + sR_2C} \tag{4.11}$$

4.7 Type II active compensator



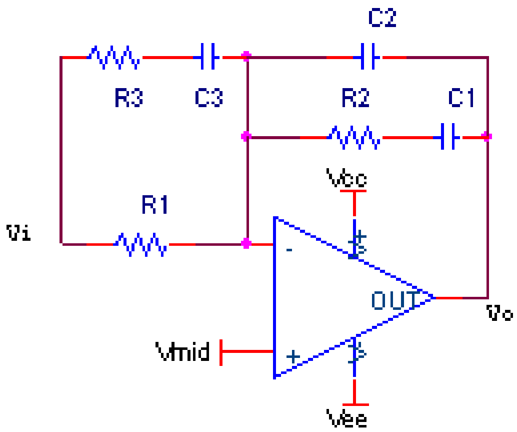
This compensator is a bit more complex: it has a zero, a pole at the origin, and a second pole. The pole at the origin is caused by the two capacitors in the feedback path; since both are open circuits at DC there is no feedback path at DC and the DC gain is the op amp's open loop gain. To derive the transfer function use the fact that the op amp is configured as an inverting amplifier but with a feedback impedance of

$$\left(R_2 + \frac{1}{sC_1}\right)||\frac{1}{sC_2} = \frac{1 + sR_2C_1}{s(sR_2C_1C_2 + C_1 + C_2)} \tag{4.12}$$

Dividing this impedance by $-\frac{1}{R_1}$ and rearranging, we see the transfer function is

$$\frac{v_o}{v_i}(s) = -\frac{1 + sR_2C_1}{sR_1(C_1 + C_2)(1 + sR_2\frac{C_1C_2}{C_1+C_2})} \tag{4.13}$$

4.8 Type III active compensator



This compensator is even more complex because it adds a resistor and capacitor to the input network and in doing so adds another zero and pole for a total of two zeroes, a pole at the origin, and two additional poles. So many zeroes and poles make this a very flexible compensator that can significantly improve a plant's transfer function, but at the cost of complexity. Fortunately, we have already done most of the work in deriving the transfer function since this compensator's feedback network is the same as that of the type II compensator above. The input network is now

$$R_1 || \left(R_3 + \frac{1}{sC_3}\right) = \frac{R_1(1 + sR_3C_3)}{1 + s(R_1 + R_3)C_3} \tag{4.14}$$

and so the transfer function is

$$\frac{v_o}{v_i}(s) = -\frac{(1 + sR_2C_1)(1 + s(R_1 + R_3)C_3)}{sR_1(C_1 + C_2)(1 + sR_3C_3)(1 + sR_2\frac{C_1C_2}{C_1+C_2})} \tag{4.15}$$

Chapter 5

Transistor-Level Amplifiers and Buffers

This chapter presents some very basic amplifiers and buffers built out of transistors. These circuits are very common in transistor level circuit designs, and many are used as components of operational amplifiers. Without these basic circuits none of the circuits in the previous chapters would be possible since they are the basis of operational amplifiers.

The two most common types of transistors are Bipolar Junction Transistors (BJTs) and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). There are two different types of bipolar transistors – *npn* and *pnp*. Similarly, MOSFETs are either NMOS or PMOS. BJTs and MOSFETs can be constructed in various ways to exhibit different characteristics – some bipolar transistors have larger emitter areas or are designed to have a higher β_F, for example, and some MOSFETs are designed to handle high power or to have a low $R_{\mathrm{DS(on)}}$. The transistors in the circuits that follow, however, are all general purpose; the only variation is between *npn* and *pnp* for bipolar transistors and NMOS and PMOS for MOSFETs.

Many of the circuits that follow can be implemented with either bipolar transistors or MOSFETs. The analysis of both implementations are usually very similar so in some cases only the bipolar version is shown and analyzed. The impedance into the gate of a MOSFET can be approximated as infinite but the same is not true for the base of a bipolar transistor, so the bipolar implementation is occasionally more complicated; analysis of only the bipolar implementation is thus slightly more general and informative than analysis of only the MOS implementation.

Although the analysis of bipolar implementations cannot approximate the impedance into the base as infinite, one can approximate impedances into the base and emitter of a bipolar transistor using the principle of *β_F impedance reflection*. *Impedance reflection* allows one to approximate the impedance into the base of a bipolar transistor as the impedance at the base (e.g. r_π) plus the impedance at the emitter multiplied by $\beta_F + 1$ (or $\beta_0 + 1$, for small signals). Thus, a resistor R_E connected from the emitter to signal ground results in a total impedance looking into the base of $r_\pi + (\beta_F + 1)R_E$. Similarly, the impedance looking into the emitter is the impedance at the emitter plus the impedance at the base divided by $\beta_F + 1$.

For most of these circuits the transistor's base (or gate) must be biased to a certain DC voltage depending on the desired I_C (or I_D). Biasing a MOSFET with a resistor divider is trivial since the bias voltage V_G generated by the resistor divider is not affected by a current into or out of the MOSFET's gate (there is ideally no such current since there is an ideally infinite impedance into the gate). A bipolar transistor, on the other hand, has a small but non-negligible base current I_B which can have an effect on V_B if the bias resistors are chosen incorrectly. To ensure the resistor divider generates the desired V_B, a good rule of thumb is to choose resistors such that the current through the bias resistors is at least ten times I_B – this ensures the current through the bias resistors is not so small that I_B affects V_B while not dissipating too much power. Some of the circuits that follow show resistor dividers, which are assumed to be chosen to meet these constraints. There are, of course, other methods to properly bias the transistor(s).

There are several other rules of thumb regarding transistors. One is that a change in voltage applied to the gate/base of a transistor will, in general, result in the source/emitter swinging in the same direction as the gate/base and the drain/collector swinging in the opposite direction; this can be used to determine whether a signal is inverted or not through a path of transistors. Another rule of thumb is that impedances looking into a source/emitter are low and impedances looking into a drain/collector and gate/base are high, and dominant time constants are typically located in nodes with high impedances.

Bipolar equations

$$I_C = I_S\left(e^{\frac{V_{BE}}{V_{TH}}} - 1\right) \tag{5.1}$$

$$I_C = \beta_F I_B \tag{5.2}$$

$$I_E = I_B + I_C = \frac{\beta_F + 1}{\beta_F} I_C \tag{5.3}$$

MOS equations

In the active region with strong inversion:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_t\right)^2\left(1 + \frac{V_{DS}}{V_A}\right), V_{GS} \geq V_t, V_{GD} < V_t \tag{5.4}$$

$$\chi = \frac{g_{mb}}{g_m} \tag{5.5}$$

In the active region with weak inversion:

$$I_D = \frac{W}{L} I_t e^{\frac{V_{GS}-V_t}{nV_t}}\left(1 - e^{-\frac{V_{DS}}{V_t}}\right) \tag{5.6}$$

where

$$I_t = qXD_n n_{po} e^{\frac{k_2}{V_T}} \tag{5.7}$$

and

$$\frac{1}{n} = \frac{1}{1+\chi} \tag{5.8}$$

Small Signal Models

The complete hybrid-π small-signal model (Gray et al., *Analysis and Design of Analog Integrated Circuits*, p. 33) for both *npn* and *pnp* bipolar transistors is shown in Figure 5.1. The complete MOS small-signal model (ibid., p. 55) is shown in Figure 5.2 and is also valid for both NMOS and PMOS transistors.

It is usually not necessary to use the complete hybrid-π or MOS small signal model, and attempting to use the complete models usually makes the small-signal analysis overly complicated. For hand calculations with the hybrid-π small-signal model one can usually treat C_π, r_μ, C_μ, and C_{cs} as open circuits, and r_{es} and r_c as a short circuit. For hand calculations with the MOS small-signal model one can usually treat all the capacitors as open circuits. Additionally, one can usually ignore the $g_{mb}v_{bs}$ dependent current source since the MOSFET's backgate is usually connected to the source. Unless specifically stated otherwise, the following analyses assume the backgate is connected to the source so $g_{mb}v_{bs} = 0$.

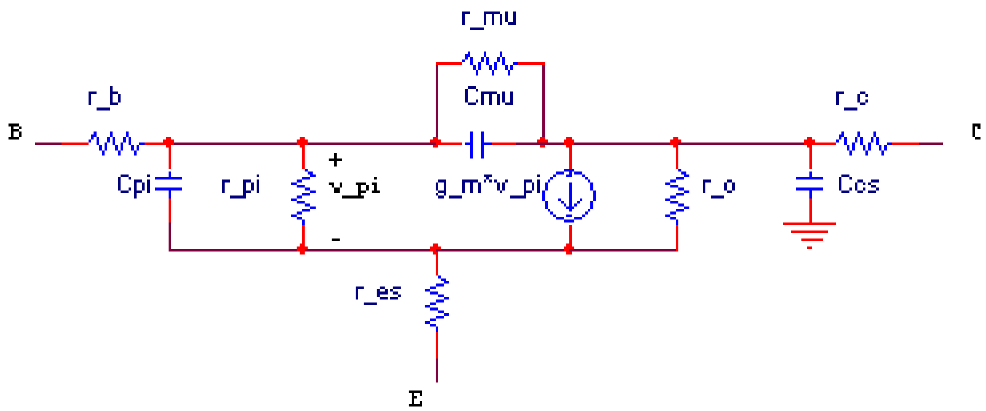


Figure 5.1: Complete bipolar hybrid-pi model

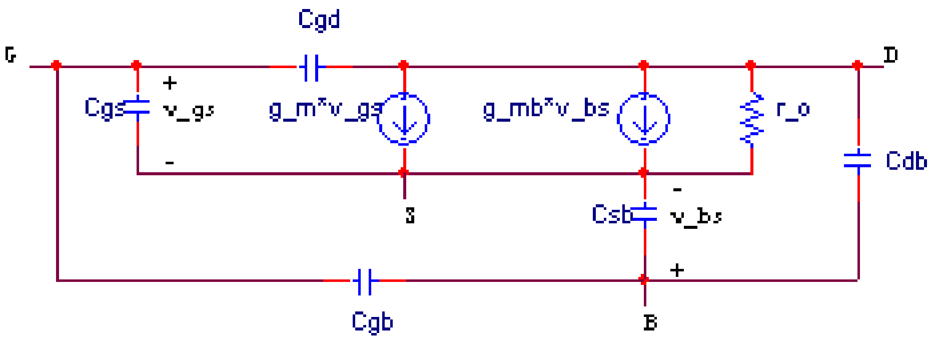
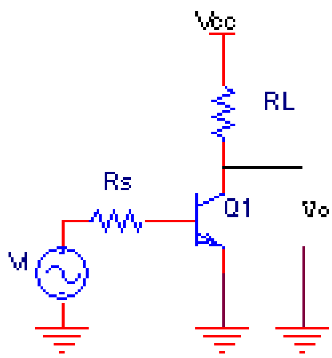


Figure 5.2: Complete MOS small-signal model

5.1 Common emitter/source



The common emitter (or common source) is so named because in this configuration the emitter/source of the transistor is shorted to a common signal source (in this case, GND). The output is taken from the transistor's collector (or drain). Sometimes the common emitter/source is used with a resistor connected from the emitter/source to the common signal source; such a resistor is called an *emitter degeneration* resistor or *source degeneration* resistor. Emitter/source degeneration employs negative feedback in the form of an impedance to provide temperature stability to the circuit at DC – a common emitter without emitter degeneration has $v_{BE} = v_B = v_I$ (where v_B is the voltage at the transistor's base) and $i_C = I_S e^{\frac{v_I}{V_{th}}}$ so $v_O = V_{CC} - R_L I_S e^{\frac{v_I}{V_{th}}}$. Lack of emitter degeneration therefore gives high gain (since the v_I term is part of an exponential) at the expense of temperature stability (since the temperature-dependent V_{th} term is also in the exponential). Such a tradeoff is a familiar concept in control theory. For an AC signal, however, emitter/source degeneration can be used to provide DC stability without sacrificing gain by using an appropriately sized emitter/source capacitor C_E (or C_S)

in parallel with the emitter/source degeneration resistor R_E (or R_S) that has (ideally) zero impedance at all frequencies of the input signal. The DC stability provided by the emitter degeneration resistor ensures that the transistor is biased correctly so that it behaves linearly for the small signal input while the emitter/source capacitor maintains high gain for input AC signals.

If the common emitter/source is used for processing AC signals but not DC, it is usually necessary to use a DC blocking capacitor in series with the output of the preceding stage and the transistor's base. Figure 5.3 shows the common emitter with a DC blocking capacitor, a voltage divider to bias the transistor's base, an emitter degeneration resistor, and an emitter bypass capacitor.

5.1.1 Bipolar

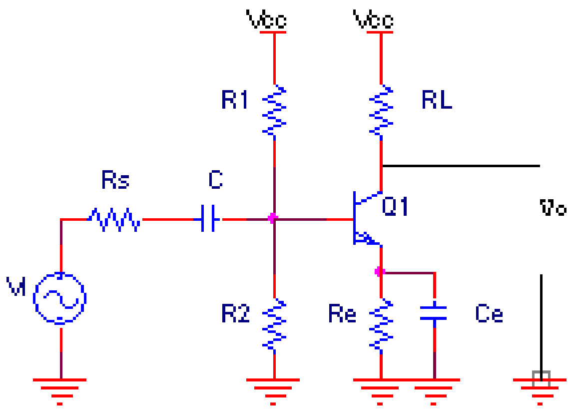


Figure 5.3: Common emitter implementation for AC signals

To analyze the small signal behavior of the common emitter one can use a slightly simplified version of the hybrid-π small signal model. Also, assume the DC blocking capacitor is a short circuit for the frequencies of interest and, to derive as general a transfer function as possible, assume an emitter degeneration resistor is used without an emitter bypass capacitor. For simplicity assume that R_1 and R_2 are large enough that they can be ignored and define $R'_S = R_S + r_b$. Figure 5.4 shows the small signal model of this common emitter circuit.

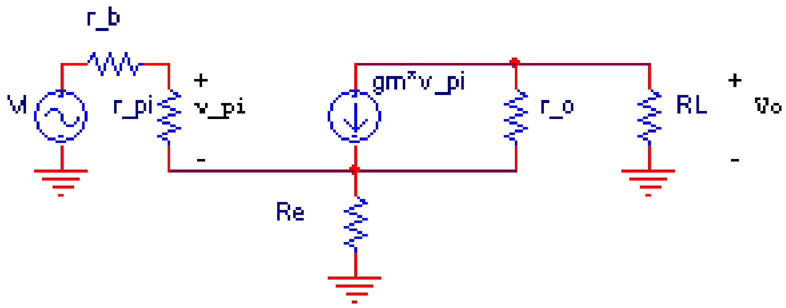


Figure 5.4: Common emitter small signal model

It is easy enough to derive the transfer function of the common emitter without emitter degeneration since with $R_E = 0$ the emitter is shorted to ground and the input section (v_i, r_b, and r_π) is isolated from the output section ($g_m v_\pi$, r_o, and R_L). However, for the general case (i.e. with emitter degeneration) it is easier to view the common emitter as an equivalent two port small-signal model as shown in Figure 5.5 and derive the input resistance R_i, output resistance R_o, and transconductance G_m (note that G_m is not to be confused with the transistor's transconductance g_m – it is $G_m = \frac{i_o}{v_i}$ with the output shorted).

To derive R_i, R_o, and G_m start with Ohm's Law and KCL at the emitter and collector. By Ohm's Law,

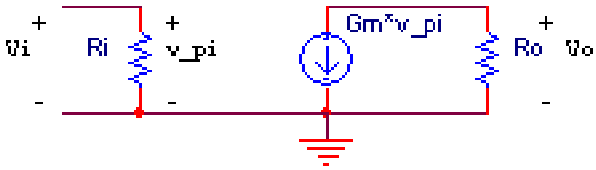


Figure 5.5: Two port equivalent small-signal model

$$i_b = \frac{v_i - v_e}{r_\pi} \tag{5.9}$$

(where v_e is the voltage at the emitter and i_b is the small-signal base current and also the circuit's small-signal input current). KCL at the emitter yields

$$\frac{v_e}{R_E} + \frac{v_e + i_o R_L}{r_o} = (\beta_0 + 1) i_b \tag{5.10}$$

(recall that $g_m v_\pi = \beta_0 i_b$). KCL at the collector yields

$$i_o + \frac{v_e + i_o R_L}{r_o} = i_o \left(1 + \frac{R_L}{r_o}\right) + \frac{v_e}{r_o} = \beta_0 i_b \tag{5.11}$$

Solving for i_o in (5.10), substituting it into (5.11), and rearranging, we find

$$v_e = i_b \left(\frac{1 + (\beta_0 + 1)\frac{r_o}{R_L}}{\frac{1}{R_L} + \frac{1}{R_E} + \frac{r_o}{R_L R_E}} \right) \tag{5.12}$$

Substituting (5.12) into (5.9) (which can be rewritten as $R_i = v_i/i_b = r_\pi + v_e/i_b$), we find (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 197–199)

$$R_i = r_\pi + (\beta_0 + 1) \left(\frac{r_o + \frac{R_L}{\beta_0 + 1}}{r_o + R_L + R_E} \right) R_E \tag{5.13}$$

Often $r_o >> R_L$ and $r_o >> R_E$ so (5.13) can be approximated as

$$R_i \approx r_\pi + (\beta_0 + 1) R_E \tag{5.14}$$

Note that this approximation is consistent with the principle of β_F *impedance reflection*.

For the circuit's transconductance G_m set $R_L = 0$ (since the output is shorted by definition of G_m). From the emitter KCL equation $\frac{v_e}{R_E} + \frac{v_e}{r_o} = (\beta_0 + 1) i_b = (\beta_0 + 1)\frac{v_i - v_e}{r_\pi}$ so

$$v_e = \frac{\frac{\beta_0 + 1}{r_\pi}}{\frac{1}{R_E} + \frac{1}{r_o} + \frac{1}{r_\pi}} v_i \tag{5.15}$$

From the collector KCL equation we know

$$i_o + \frac{v_e}{r_o} = \beta_0 i_b = \beta_0 \frac{v_i - v_e}{r_\pi} \tag{5.16}$$

so we can substitute (5.15), which is in terms of v_i, to find (ibid., p. 199)

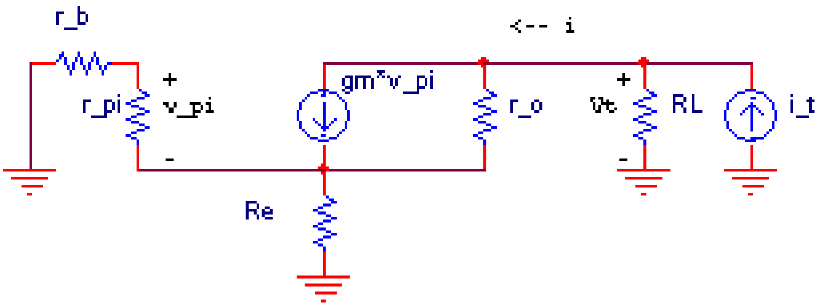


Figure 5.6: Common emitter small-signal equivalent model for computing output resistance

$$G_m = g_m \frac{1 - \frac{R_E}{\beta_0 r_o}}{1 + g_m R_E \left(1 + \frac{1}{\beta_0} + \frac{1}{g_m r_o}\right)} \tag{5.17}$$

Often $r_o \gg R_E$, $\beta_0 \gg 1$, and $g_m r_o \gg 1$ so

$$G_m \approx \frac{g_m}{1 + g_m R_E} \tag{5.18}$$

Without emitter degeneration ($R_E = 0$) both equations reduce to $G_m = g_m$, which is expected since the common emitter's hybrid-π small-signal model looks like the two port small-signal model when the emitter is shorted to ground.

It is clear from the two port model (Figure 5.5) that $v_o = -G_m r_o v_i$ so using (5.17) we know

$$\frac{v_o}{v_i} = g_m \frac{1 - \frac{R_E}{\beta_0 r_o}}{1 + g_m R_E \left(1 + \frac{1}{\beta_0} + \frac{1}{g_m r_o}\right)} r_o \tag{5.19}$$

To find the small-signal output resistance R_o of the common emitter, use the equivalent circuit shown in Figure 5.6. Using a test current source i_t and the voltage v_t across it, R_o is, by definition,

$$R_o = \frac{v_t}{i_t} \tag{5.20}$$

By defining i as the portion of the i_t current into the $g_m v_\pi$ current source and r_o, this becomes

$$R_o = \frac{v_t}{i} || R_L \tag{5.21}$$

The current i splits between the $g_m v_\pi$ current source and r_o but recombines at the emitter node so

$$v_\pi = -i \frac{r_\pi R_E}{r_\pi + R_E} \tag{5.22}$$

assuming r_b is small enough to be ignored (if not, simply add it to r_π). Also, the current i_1 through r_o is

$$i_1 = i - g_m v_\pi = i + i g_m \frac{r_\pi R_E}{r_\pi + R_E} \tag{5.23}$$

where the latter equation is true by substituting $-i(r_\pi || R_E)$ for v_π using (5.22). Using (5.22) and (5.23), the voltage v_t is thus

$$v_t = i_1 r_o - v_\pi = i\frac{r_\pi R_E}{r_\pi + R_E} + i r_o\left(1 + g_m\frac{r_\pi R_E}{r_\pi + R_E}\right) \tag{5.24}$$

Dividing both sides of (5.24) by i and putting the result in parallel with R_L gives (Gray et al., *Analysis and Design of Analog Integrated Circuits*, p. 200)

$$R_o = \left(\frac{r_\pi R_E}{r_\pi + R_E} + r_o\left(1 + g_m\frac{r_\pi R_E}{r_\pi + R_E}\right)\right) \parallel R_L \tag{5.25}$$

The first term is much smaller than the second so

$$R_o \approx r_o\left(1 + g_m\frac{r_\pi R_E}{r_\pi + R_E}\right) \parallel R_L = r_o\left(1 + \frac{g_m R_E}{1 + \frac{g_m R_E}{\beta_0}}\right) \parallel R_L \tag{5.26}$$

Depending on whether β_0 is significantly larger or smaller than $g_m R_E$, R_o can be further simplified as follows:

$$R_o \approx (r_o(1 + g_m R_E)) \parallel R_L,\ \beta_0 \gg g_m R_E \tag{5.27}$$

$$R_o \approx (r_o(1 + \beta_0)) \parallel R_L,\ g_m R_E \gg \beta_0 \tag{5.28}$$

5.1.2 MOS

The small signal model of the common source is identical to the common emitter hybrid-π model shown in Figure 5.4, except that $r_\pi \to \infty$ and the $g_m v_\pi$ current source is replaced with two current sources ($g_m v_{gs}$ and $g_{mb} v_{bs}$) in parallel (assuming the body terminal is connected to GND or V_{SS}, whichever is the lowest supply voltage). First we find $G_m = \frac{i_o}{v_i}$ using KCL at the source and at the drain (with $R_L = 0$):

$$\frac{v_s}{R_S} + \frac{v_s}{r_o} = g_m v_{gs} + g_{mb} v_{bs} = g_m(v_i - v_s) - g_{mb} v_s \tag{5.29}$$

$$i_o + \frac{v_s}{r_o} = g_m v_{gs} + g_{mb} v_{bs} = g_m(v_i - v_s) - g_{mb} v_s \tag{5.30}$$

Solving (5.29) for v_s yields

$$v_s = \frac{g_m v_i}{g_m + g_{mb} + \frac{1}{R_S} + \frac{1}{r_o}} \tag{5.31}$$

Substituting (5.31) into (5.30) and rearranging yields (ibid., p. 201)

$$G_m = \frac{g_m}{1 + (g_m + g_{mb})R_S + \frac{R_S}{r_o}} \tag{5.32}$$

In the case where $r_o \gg R_S$, the equation for G_m simplifies to

$$G_m \approx \frac{g_m}{1 + (g_m + g_{mb})R_S} \tag{5.33}$$

The common source's output resistance R_o can be computed the same way as the common emitter's R_o: we apply a test current i_t into the output and measure the voltage v_t across the current source (as before, temporarily ignore R_L and add it back in parallel) to find $R_o = \frac{v_t}{i_t}$. The test current i_t is also the current through R_S since none of it is diverted through a finite r_π so

$$v_s = i_t R_S \tag{5.34}$$

If i_1 is the current through r_o, Kirchhoff's Voltage Law (KVL) shows that

$$v_t = i_1 r_o + v_s = (i_t - g_m v_{gs} - g_{mb} v_{bs}) r_o + v_s = (i_t + g_m v_s + g_{mb} v_s) r_o + v_s \tag{5.35}$$

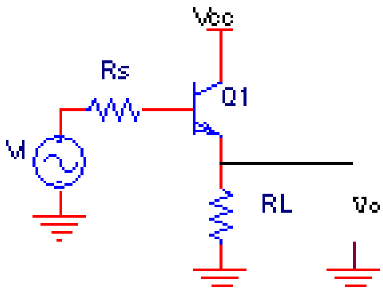
Substituting (5.34) into (5.35), rearranging, and then putting the result in parallel with R_L yields

$$R_o = (R_S + (1 + (g_m + g_{mb}) R_S) r_o + R_S) \parallel R_L \tag{5.36}$$

The common source's input resistance R_i is trivially

$$R_i = \infty \tag{5.37}$$

5.2 Common collector/drain (emitter/source follower)



In this circuit the collector or drain is shorted to the supply voltage so it is called a common collector (or common drain). It is also known as the emitter follower (or source follower) since v_o is the voltage across the emitter (or source) resistor and follows the base voltage (which is also the input voltage v_i). The circuit has a voltage gain of approximately unity so it is a voltage follower (buffer).

As will be seen in the full analysis, emitter/source followers have a high R_i. This makes them useful loads for voltage amplifiers (such as common emitters/sources) so that most of the preceding amplifier's output voltage falls across the emitter/source follower's input. The full analysis will also show that emitter/source followers have a low R_o, which makes them useful sources for circuits that require an input voltage since an ideal voltage source has zero R_o. Emitter/source followers are also used to push out poles that would otherwise appear in a circuit by reducing the resistance seen by a node where a capacitance appears (a high resistance seen by a capacitor can result in a long RC time constant, degrading the circuit's response at higher frequencies). Emitter/source followers are thus highly useful circuits even when processing voltage signals.

5.2.1 Bipolar

For the emitter follower it is easy to see from (5.1) that the voltage gain is approximately unity even without a full analysis. Assuming a constant temperature so V_{TH} does not vary, v_{BE} does not vary significantly even for relatively large variations in I_C due to the exponential relationship between v_{BE} and I_C. Since v_{BE} does not vary then $v_E = v_O$ must follow $v_B = v_I$.

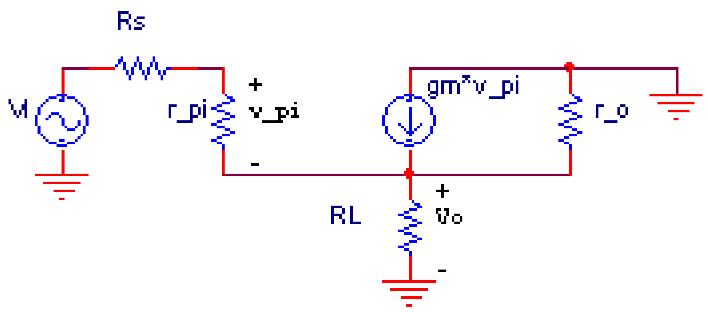


Figure 5.7: Emitter follower small signal model

Although the preceding first order analysis proves that the voltage gain is approximately unity, it is often necessary to know the exact transfer function. To find it, use KCL at the emitter:

$$i_i + \beta_0 i_i - \frac{v_o}{R_L} - \frac{v_o}{r_o} = 0 \tag{5.38}$$

where i_i is the current into the base of the transistor. Since i_i flows through R_S (which may include the transistor's base resistance r_b, if such accuracy is needed) and r_π, and the voltage across these two resistors is $v_{be} = v_i - v_o$,

$$i_i = \frac{v_i - v_o}{R_S + r_\pi} \tag{5.39}$$

Substituting into (5.38) and rearranging terms, the transfer function is

$$\frac{v_o}{v_i} = \frac{1}{1 + \frac{R_S + r_\pi}{(\beta_0+1)(R_L||r_o)}} \tag{5.40}$$

If $(\beta_0 + 1)(R_L||r_o) >> R_S + r_\pi$ then the voltage gain is approximately unity. Another common approximation of the transfer function is

$$\frac{v_o}{v_i} \approx \frac{g_m R_L}{1 + g_m R_L} \tag{5.41}$$

which is true when $\beta >> 1$, $r_\pi >> R_S$, and $r_o >> R_L$.

The input resistance R_i of the emitter follower can be determined by removing the input voltage source (including its resistance R_S) and measuring the equivalent resistance looking into the input terminals. Similarly, the output resistance R_o can be determined by removing the load resistor R_L and measuring the equivalent resistance looking into the output terminals. However, both R_i and R_o can be determined by inspection using *impedance reflection*:

$$R_i = r_\pi + (\beta_0 + 1)(R_L||r_o) \tag{5.42}$$

$$R_o = \frac{R_S + r_\pi}{\beta_0 + 1}||r_o \tag{5.43}$$

The latter simplifies to

$$R_o \approx \frac{1}{g_m} + \frac{R_S}{\beta_0 + 1} \tag{5.44}$$

if $\beta >> 1$ and $r_o >> \frac{R_S + r_\pi}{\beta_0 + 1}$.

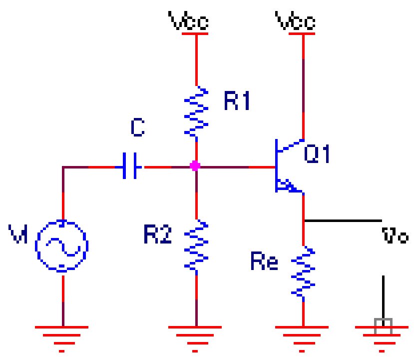


Figure 5.8: Emitter follower implementation for AC signals

An emitter follower implementation for AC signals is shown above in Figure 5.8. It includes bias resistors R_1 and R_2 which of course affect R_i – add $R_1||R_2$ in parallel with (5.42).

5.2.2 MOS

The source follower also has a voltage gain of approximately unity, a fact which can be seen from the square-law dependence of I_D on V_{GS} in the active region as shown by (5.4) – V_{GS} does not vary significantly even for relatively large variations in I_D. V_{GS} does vary with I_D more than the bipolar transistor's V_{BE} varies with its I_C, however, so a source follower's voltage gain is generally less than unity and more so than the emitter follower's voltage gain. The full small signal analysis will demonstrate this.

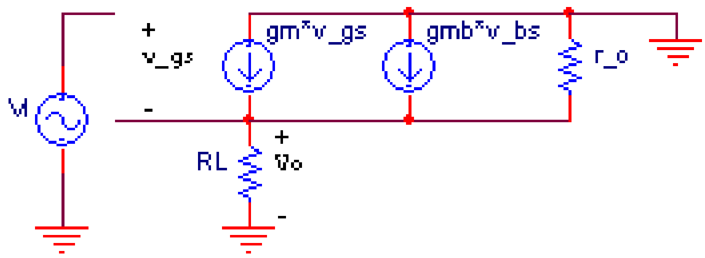


Figure 5.9: Source follower small signal model

With the MOSFET's body terminal connected to the lowest supply voltage (GND) in the small signal model shown in Figure 5.9, we can determine the transfer function exactly by realizing that

$$v_{bs} = -v_s = -v_o \tag{5.45}$$

and finding KCL at the output (the source):

$$g_m v_{gs} - g_{mb} v_o = \frac{v_o}{R_L} + \frac{v_o}{r_o} \tag{5.46}$$

Also, KVL around the input loop shows that

$$v_i = v_o + v_{gs} \tag{5.47}$$

Solving (5.46) for v_{gs} and substituting the result into (5.47) gives

$$\frac{v_o}{v_i} = \frac{g_m}{g_m + g_{mb} + \frac{1}{R_L} + \frac{1}{r_o}} = \frac{g_m r_o}{(g_m + g_{mb})r_o + 1 + \frac{r_o}{R_L}} \tag{5.48}$$

In the case where $R_L \to \infty$, (5.48) simplifies to

$$\frac{v_o}{v_i} \approx \frac{g_m r_o}{1 + (g_m + g_{mb}) r_o} \tag{5.49}$$

If both $R_L \to \infty$ and $r_o \to \infty$ then

$$\frac{v_o}{v_i} \approx \frac{g_m}{g_m + g_{mb}} = \frac{1}{1 + \chi} \tag{5.50}$$

where χ is defined in (5.5) and is typically well below unity (in the range of 0.2).

The voltage gain can be improved by tying the MOSFET's body to its source so that $v_{bs} = 0$ and the g_{mb} term disappears:

$$\frac{v_o}{v_i} = \frac{g_m r_o}{1 + g_m r_o + \frac{r_o}{R_L}} \tag{5.51}$$

$$\frac{v_o}{v_i} \approx \frac{g_m r_o}{1 + g_m r_o} \tag{5.52}$$

The input resistance R_i of the source follower is the resistance looking into the gate of the MOSFET, which is trivially

$$R_i = \infty \tag{5.53}$$

The output resistance R_o is the resistance looking into the output with $v_i = 0$. Since $v_i = 0$ it is obvious that

$$v_{gs} = -v_o \tag{5.54}$$

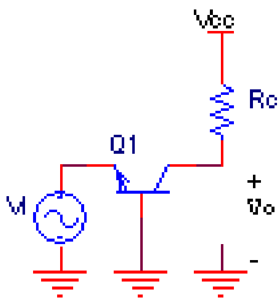
Also, KCL at the output yields

$$i_o = \frac{v_o}{r_o} + \frac{v_o}{R_L} + (g_m + g_{mb}) v_o \tag{5.55}$$

Rearranging (5.55) gives an equation for R_o:

$$R_o = \frac{1}{g_m + g_{mb} + \frac{1}{r_o} + \frac{1}{R_L}} \tag{5.56}$$

5.3 Common base/gate



The transistor in a common base/gate circuit is biased such that the base/gate is directly connected to AC ground, the input is applied to the emitter/source, and the output is taken from the collector/drain. Although the input and output signals are voltages, it is useful to think of the common base/gate as a current source (since $I_C \approx I_E$ and $I_D \approx I_S$) with a high R_o (the resistance looking into the collector/drain is r_o, which is usually very high). These characteristics of the common base/gate make it useful in certain situation, such as a cascode circuit (see below).

5.3.1 Bipolar

The transfer function and input and output resistances of the previous circuits were derived using the hybrid-π small signal model, but the dependent $g_m v_\pi$ current source is directly connected from output to input and thus makes the analysis of the hybrid-π small signal model for the common base difficult. One way to simplify the analysis of the common base circuit is to transform the hybrid-π model into an equivalent *T model*. The first step in this tranformation is to split the $g_m v_\pi$ current source into two current sources of value $g_m v_\pi$, with one connected from the collector to the base and the other connected from the base to the emitter. Splitting the $g_m v_\pi$ current source like this is possible since the currents entering and exiting the base are equal (i.e. KCL at the base is unchanged) and the two current sources supply the same current from collector to emitter. Next, note that the $g_m v_\pi$ dependent current source from the collector to the base is controlled by the voltage across it – so its equivalent resistance r_{cb} is

$$r_{cb} = \frac{v_\pi}{g_m v_\pi} = \frac{1}{g_m} \tag{5.57}$$

and we can replace the dependent current source with a resistor that is in parallel with r_π. The parallel combination of these two resistors is the equivalent resistance r_e, which is

$$r_e = \frac{\frac{r_\pi}{g_m}}{\frac{1}{g_m} + r_\pi} = \frac{1}{\frac{1}{r_\pi} + g_m} = \frac{1}{g_m\left(1 + \frac{1}{\beta_0}\right)} \tag{5.58}$$

At low frequencies the capacitors and resistors r_o and r_μ can be neglected, in which case the small signal model looks like a "T". The transformation from the hybrid-π model to the *T model* with and without the higher frequency elements is shown in Figures 5.10 - 5.12. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 183–184)

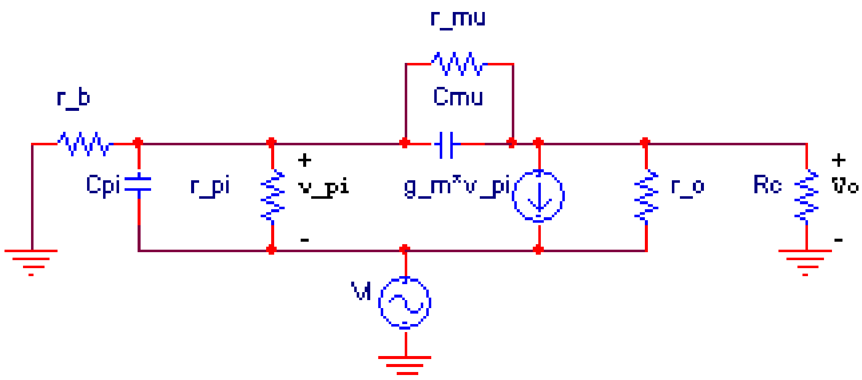


Figure 5.10: Hybrid-π small signal model for common base analysis

With this simplified model it is trivial to see that

$$R_o = R_C \tag{5.59}$$

It is also easy to see that the short-circuit transconductance is

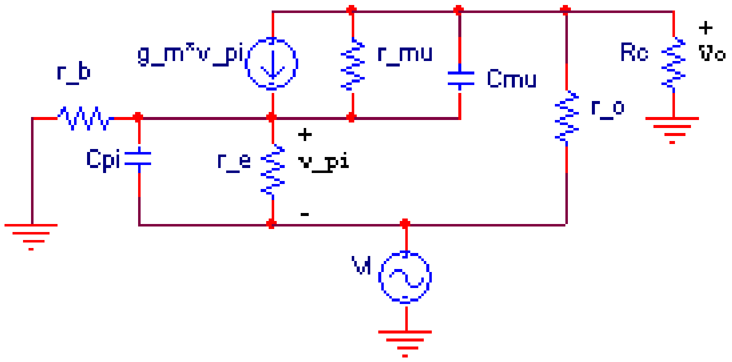


Figure 5.11: Small signal *T model* for common base analysis

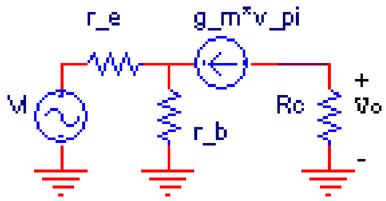


Figure 5.12: Small signal *T model* for common base at low frequencies

$$G_m = \frac{i_o}{v_i}|_{v_o=0} = \frac{g_m v_\pi}{v_i} \tag{5.60}$$

since v_π is the voltage across r_e. We need to know the relationship between v_π and v_i, however, in order to derive a useful expression for G_m and R_i. This relationship can be found by KVL around the input loop

$$v_i = v_b + v_e \tag{5.61}$$

and KCL at the node between r_e and r_b (the transistor's base):

$$g_m v_\pi + \frac{v_b}{r_b} = \frac{v_e}{r_e} \tag{5.62}$$

Substituting for v_b in (5.62) we find that

$$\frac{v_i}{v_\pi} = 1 + \frac{g_m}{\beta_0} r_b = 1 + \frac{r_b}{r_\pi} \tag{5.63}$$

Now a simple substitution from (5.63) into (5.60) gives (ibid., p. 185)

$$G_m = \frac{g_m}{1 + \frac{r_b}{r_\pi}} \tag{5.64}$$

Since the relationship between v_i and v_π is known and

$$R_i = \frac{v_i}{i_i} = \frac{v_i}{v_\pi} r_e \tag{5.65}$$

by inspection, we know

$$R_i = r_e \left(1 + \frac{r_b}{r_\pi}\right) \tag{5.66}$$

We can now calculate the voltage and current gain of the common base:

$$\frac{v_o}{v_i} = G_m R_o = \frac{g_m R_C}{1 + \frac{r_b}{r_\pi}} \tag{5.67}$$

$$\frac{i_o}{i_i} = G_m R_i = g_m r_e \tag{5.68}$$

5.3.2 MOS

As with the common base, the analysis of the common gate may be simplified by transforming the transistor's small signal model into an equivalent *T model*. From the small signal model, the $g_m v_{gs}$ and $g_{mb} v_{bs}$ current sources can be combined if the MOSFET body is connected to ground (which we will assume). The combined current source $(g_m + g_{mb})v_{gs}$ can then be split into two current sources of equal magnitude and opposite direction to ground since KCL at the source and drain are unaffected and no net current enters or leaves ground. Next, the current source $(g_m + g_{mb})v_{gs}$ between the gate and source is controlled by the voltage across it so it is equivalently a resistor of value $1/(g_m + g_{mb})$. Figures 5.13 - 5.16 show this transformation. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, p. 186)

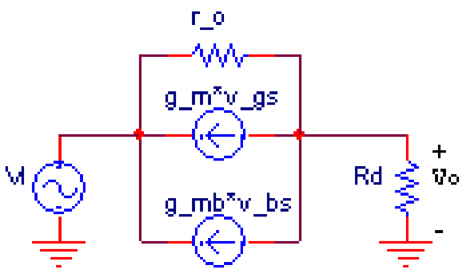


Figure 5.13: Small signal model for the common gate circuit

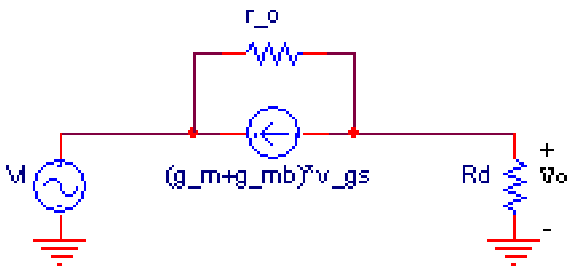


Figure 5.14: Common gate small signal model with current sources combined

Assuming $r_o \to \infty$ we can determine the circuit's parameters by inspection:

$$G_m = g_m + g_{mb} \tag{5.69}$$

$$R_i = \frac{1}{g_m + g_{mb}} \tag{5.70}$$

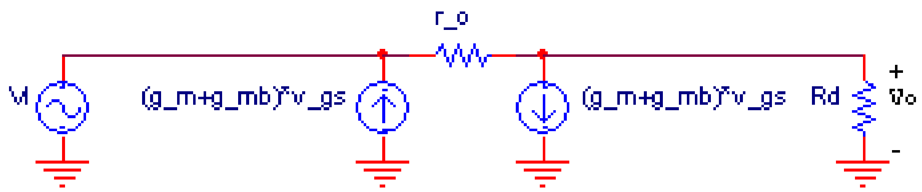


Figure 5.15: Common gate small signal model with current source split

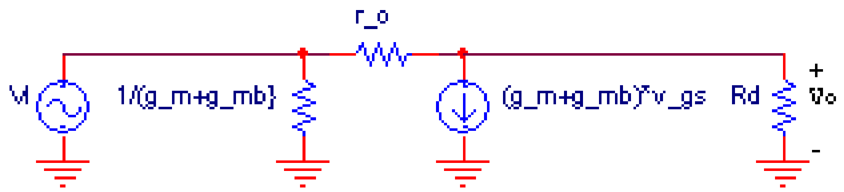


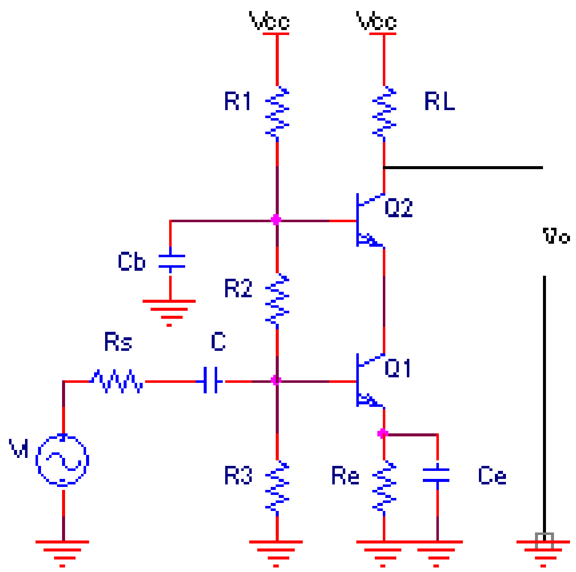
Figure 5.16: Common gate *T model*

$$R_o = R_D \tag{5.71}$$

$$\frac{v_o}{v_i} = G_m R_o = (g_m + g_{mb}) R_D \tag{5.72}$$

$$\frac{i_o}{i_i} = G_m R_i = 1 \tag{5.73}$$

5.4 Cascode



The cascode is a two transistor circuit that is actually a first stage common emitter/source driving a second stage common base/gate. To analyze the small signal voltage gain, we will approximate

$$i_{c1} = i_{e2} = \left(1 + \frac{1}{\beta}\right) i_{c2} \tag{5.74}$$

as

$$i_{c1} \approx i_{c2} \tag{5.75}$$

This approximation is valid if $\beta_0 >> 1$. Under this approximation

$$g_{m1} = g_{m2} \tag{5.76}$$

and

$$r_{\pi 1} = r_{\pi 2} \tag{5.77}$$

We define these as g_m and r_π, respectively. From the circuit configuration

$$v_o = -i_{c2}(R_L||r_o) \approx -i_{c1}(R_L||r_o) \tag{5.78}$$

and from the small signal model

$$i_{c1} = g_m v_{\pi 1} = g_m \frac{r_\pi}{r_\pi + R'_S} v_i \tag{5.79}$$

Substituting gives

$$v_o = -g_m \frac{r_\pi}{r_\pi + R'_S}(R_L||r_o)v_i \tag{5.80}$$

Rearranging and noting that $\beta_0 = g_m r_\pi$ we find

$$\frac{v_o}{v_i} = -\frac{\beta_0(R_L||r_o)}{r_\pi + R'_S} \tag{5.81}$$

This is the same voltage gain as the common emitter! Compared to the common emitter the cascode requires an extra transistor and additional bias circuitry, suffers from reduced signal swing (since v_o is limited by two v_{BE} drops rather than one), and offers the same voltage gain. Why would one ever use a cascode rather than just a common emitter? The key improvement of the cascode over the common emitter is its bandwidth. The resistance seen by Q_1's C_μ for both the cascode and common emitter is

$$R'_S||r_\pi + (1 + g_m(R'_S||r_\pi))R_{LOAD} \tag{5.82}$$

where R_{LOAD} is the load resistance on the common emitter stage. By definition $R_{LOAD} = R_L$ for the common emitter, but $R_{LOAD} \approx \frac{1}{g_m}$ for the cascode (C_B shorts Q_2's base to AC ground so that the bias resistors do not affect R_{LOAD}). R_L is usually much higher than $\frac{1}{g_m}$ (and it must be in order to acheive a high voltage gain) so this open circuit time constant is much smaller for the cascode than the common emitter, yet the cascode offers the same gain as the common emitter. The cascode is thus an extremely useful circuit for high gain while maintaining a high bandwidth, at the expense of signal swing.

Since the first stage of the cascode is a common emitter, the input resistance R_i is the same as (5.13):

$$R_i = r_\pi + (\beta_0 + 1)\left(\frac{r_o + \frac{R_L}{\beta_0 + 1}}{r_o + R_L + R_E}\right) R_E \tag{5.83}$$

and the output resistance R_o is the same as (5.59):

$$R_o = R_L \tag{5.84}$$

5.5 Differential pair

The differential pair is a very common circuit in IC design. It is rarely implemented using discrete components since it requires very good matching of components for good performance. It is composed of two transistors whose emitters (in the bipolar case) or sources (in the MOS case) are tied together (some bipolar differential pairs connect the transistors' emitters through emitter degeneration resistors). Bipolar differential pairs are often called emitter-coupled pairs and MOS differential pairs are often called source-coupled pairs. The differential pair's topology can be used with a single-ended input (one of the transistors' bases or gates is biased to a particular voltage) and differential or single-ended output, or a differential input and differential or single-ended output. The output voltage(s) are one or both of the transistors' collectors/drains. If the differential pair is configured so that both the input and output are single-ended, the circuit is equivalent to a first stage emitter/source follower and second stage common base/gate: the input is applied to the base (or gate) of one transistor (the other transistor's base or gate is tied to a bias voltage) and the output is taken from the collector (or drain) of the second transistor. The differential input and output case is the most common, however, and such a circuit is a common input stage for an operational amplifier design. Differential pairs configured with a differential input and output also have the benefit that they can be connected to each other in a cascade without using coupling capacitors between differential pair stages. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, p. 215)

The differential pair is only linear for a narrow range of input voltages, but this limitation is usually unimportant since the differential pair is typically used as the input stage for high gain amplifiers (such as operational amplifiers), which prevents the input voltages from swinging outside the narrow linear range since the output voltage cannot swing above or below the supply voltages. If the range of input voltages for which the differential pair is linear is too narrow for a particular application, the range can be increased by using emitter degeneration resistors. The increase in the linear input voltage range, however, results in a decrease in the voltage gain of the differential pair. (ibid., pp. 216–218)

Before analyzing the differential pair variants, a brief note on notation for common-mode and differential signals: if we define the voltage at one input as v_{i1} and the voltage at the other input as v_{i2}, then the differential input is

$$v_{id} = v_{i1} - v_{i2} \tag{5.85}$$

and the common-mode voltage is

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} \tag{5.86}$$

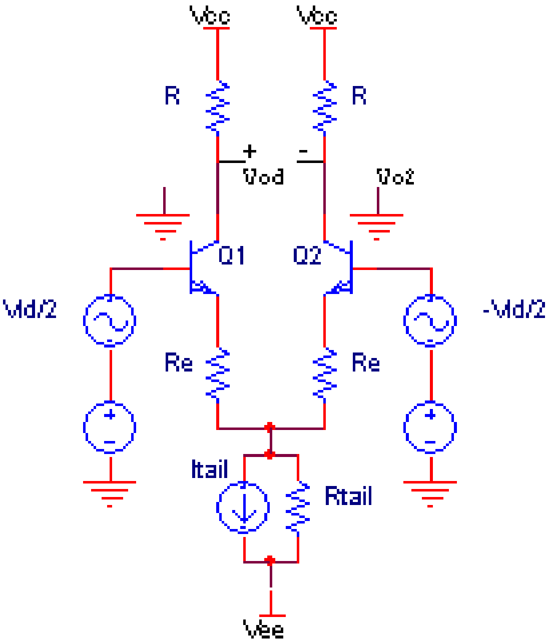
The above equations can be inverted to define the input voltages v_{i1} and v_{i2} in terms of the differential voltage v_{id} and common-mode voltage v_{ic} (ibid., p. 222):

$$v_{i1} = v_{ic} + \frac{v_{id}}{2} \tag{5.87}$$

$$v_{i2} = v_{ic} - \frac{v_{id}}{2} \tag{5.88}$$

By defining the input voltages as linear combinations of the differential and common-mode voltages, we can use superposition to analyze the differential pair's response to differential signals and its response to common-mode signals separately (as long as the input voltages are within the differential pair's linear range, since superposition is only valid for linear circuits). The output voltages can also be expressed in terms of the differential and common-mode output voltages in the same way.

5.5.1 Differential pair with resistive load



The above differential pair is shown with a resistive load and with the optional emitter degeneration resistors R_{E1} and R_{E2}. The MOS version of the differential pair (the source-coupled pair) is the same but without the degeneration resistors and, of course, MOSFETs instead of Q_1 and Q_2. The current source I_{TAIL} and its output resistance R_{TAIL} represent a Norton equivalent current source (usually composed of transistors, such as a current mirror), but the current source can simply consist of a resistor R_{TAIL}, in which $I_{TAIL} = 0$. The bases (or gates) of the transistors are also biased to some voltage which is not necessarily equal to GND (certainly not if $V_{EE} = GND$), but the bias voltages are usually equal so that $V_{B1} = V_{B2}$ (or $V_{G1} = V_{G2}$ in the MOS version).

To determine the small signal differential behavior of this circuit set $I_{TAIL} = 0$ and use the bipolar hybrid-π small signal model for the transistors (the MOS version of the circuit has a similar analysis, except with $r_\pi \to \infty$). The voltage at the base of Q_1 is $\frac{v_{id}}{2}$ and the voltage at the base of Q_2 is $-\frac{v_{id}}{2}$, and the voltage at the collector of Q_1 is $\frac{v_{od}}{2}$ and the voltage at the collector of Q_2 is $-\frac{v_{od}}{2}$. Both transistors act as voltage followers to the node that connects the two sides of the circuit (either the node that connects the emitter resistors or, if the emitter resistors are omitted, the node that connects the emitters). Since this node is driven by equal and opposite input voltages its voltage is constant, and since its voltage is constant R_{TAIL} can be shorted (which grounds the connecting node) without affecting the operation of the circuit. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, p. 226) Since the connecting node is grounded, the two sides of the differential pair are independent and are configured as common emitters! The two independent sides are sometimes called *differential half circuits*. Using the above analysis of common emitters, we thus have a differential voltage gain of

$$\frac{v_{od}}{v_{id}} = -\frac{\beta_F (R \parallel r_o)}{R'_S + r_\pi} \tag{5.89}$$

where r_o and r_π are from the hybrid-π small signal model and and R'_S is defined as above. As before, we can often simplify the transfer function to

$$\frac{v_{od}}{v_{id}} \approx -g_m R \tag{5.90}$$

The MOS version has a transfer function of

$$\frac{v_{od}}{v_{id}} = -g_m R \tag{5.91}$$

since $r_\pi \to \infty$.

A differential pair ideally has zero voltage gain for common-mode inputs. To determine the actual small signal common-mode voltage gain use a similar approach as the differential voltage gain: split the two sides of the circuit into two *common-mode half circuits*. To split the circuit replace R_{TAIL} with two resistors in parallel with resistance $2R_{TAIL}$. This does not modify the circuit since two identical resistors in parallel have an equivalent resistance of half the individual resistors. The two sides are now combined only by a wire which connects the two $2R_{TAIL}$ resistors, but this wire carries no small signal current since both transistors are driven by identical input voltages (v_{ic}). (ibid., p. 228) Consequently, the wire can be severed without affecting the circuit behavior and we have two *common-mode half circuits* which are commom emitters with emitter degeneration resistances of $R_E + 2R_{TAIL}$. From (5.19) the common-mode voltage gain is thus

$$\frac{v_{oc}}{v_{ic}} = -\frac{g_m R}{1 + g_m(R_E + 2R_{TAIL})} \tag{5.92}$$

R_E is usually much smaller than $2R_{TAIL}$ so the common-mode voltage gain is approximately

$$\frac{v_{oc}}{v_{ic}} \approx -\frac{g_m R}{1 + 2g_m R_{TAIL}} \tag{5.93}$$

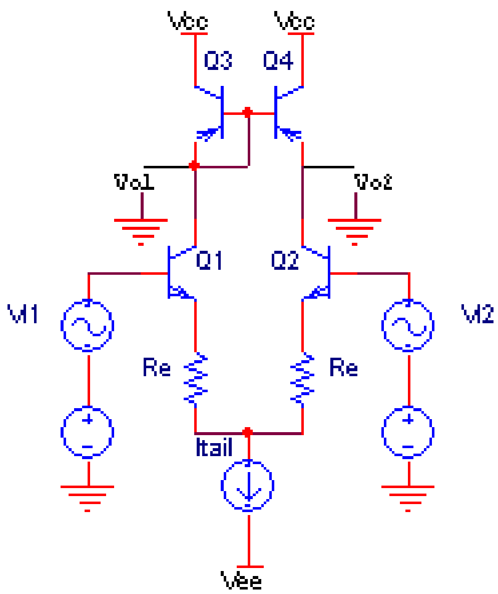
Using the approximate differential voltage gain (5.90) divided by the the approximate common-mode voltage gain (5.93) gives a good approximation of the common-mode rejection ratio CMRR, which is

$$\text{CMRR} \approx 1 + 2g_m R_{TAIL} \tag{5.94}$$

The CMRR is strongly dependent on the value of R_{TAIL} so the use of a good current source (which has an ideally infinite Norton equivalent resistance) yields a high CMRR.

The differential pair shown uses *npn* transistors, but Q_1 and Q_2 can also be *pnp* transistors. If *pnp* transistors are used the only difference is that I_{TAIL} is sourced from V_{CC} rather than sinking into V_{EE}. The same is true of the MOS version of the differential pair – PMOS transistors can be used instead of NMOS with the same change in I_{TAIL}.

5.5.2 Differential pair with active load (GHLM, p. 278, 288)



The gain of the differential pair can be increased by using an active load. Q_3 and Q_4 form a current mirror (since Q_3 is diode connected) so that I_{TAIL} is split evenly and $I_{C1} = I_{C2}$. Unfortunately, the circuit is no longer symmetrical since only Q_3 is diode connected and as a result the *differential half circuit* approach used above cannot be employed.

Chapter 6

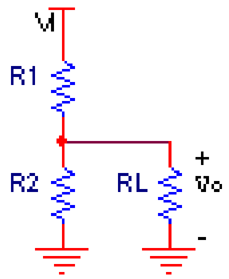
Voltage Sources and References

Voltage sources are circuits designed to maintain a constant voltage and supply a load current to other circuitry. Voltage references also maintain a constant voltage for other circuitry (for example, to bias a one input of a comparator so that the comparator's output is high when its input is at a higher voltage than the voltage reference and low otherwise). Unlike voltage sources, however, voltage references are usually not required to supply a significant load current. Ideally, the voltage output v_O of voltage references and sources does not vary with the load current and v_O has no AC component (it is a pure DC voltage). In practice, higher load currents often cause v_O to decrease slightly because the voltage reference/source has a nonzero output resistance R_o. If the input voltage is v_I and the load current i_L, then the output voltage is

$$v_O = v_I - i_L R_o \tag{6.1}$$

It is crucial, therefore, for a voltage source to have a low R_o. Voltage references should also have a low R_o, but they do not need to supply larger load currents so $v_O \approx v_I$ even if R_o is significant. Also in practice, AC noise is present in the output. One way to minimize AC noise is to add a low pass filter after the voltage source/reference to help remove the high frequency noise. However, the low pass filter will affect R_o.

6.1 Resistor divider



The resistor divider is the simplest voltage source or reference possible. Its transfer function (unloaded) can be determined by inspection:

$$v_O = \frac{R_2 v_I}{R_1 + R_2} \tag{6.2}$$

When loaded by a resistance R_L, the transfer function is the same but with R_2 replaced by $R_2 \parallel R_L$. Specifically,

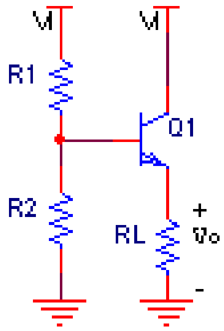
$$v_O = \frac{R_2 R_L v_I}{R_1(R_2 + R_L) + R_2 R_L} \tag{6.3}$$

The output resistance R_o is also easy to determine – with $v_I = 0$ the two resistors are in parallel looking into the output:

$$R_o = \frac{R_1 R_2}{R_1 + R_2} \tag{6.4}$$

R_o is usually quite high since R_1 and R_2 must be large enough that the current drawn by the circuit is not unnecessarily high. Consequently, the simple resistor divider is a poor voltage source and is often only used as a voltage reference.

6.2 Resistor divider with emitter/source follower



One way to improve R_o of the resistor divider is to connect an emitter/source follower to the output. An emitter/source follower has a high input resistance so that the load current seen by the resistor divider is low, but it also has a low output resistance. The drawback is that v_O is lower by approximately v_{BE} or v_{GS} due to the transistor. More specifically, v_O is dependent on the load current i_L since

$$v_O = i_L R_L \tag{6.5}$$

For an emitter follower, the relationship between i_L and v_{BE} is given by (5.1). Since

$$i_L = i_E = \frac{\beta_F + 1}{\beta_F} i_C \tag{6.6}$$

we can use (5.1) to find v_{BE} in terms of i_L:

$$v_{BE} = V_{th} \ln\left(\frac{\beta_F i_L}{(\beta_F + 1) I_S}\right) \tag{6.7}$$

The transfer function is therefore

$$v_O = \frac{R_2 v_I}{R_1 + R_2} - V_{th} \ln\left(\frac{\beta_F i_L}{(\beta_F + 1) I_S}\right) \tag{6.8}$$

The output resistance R_o is simply that of an emitter follower, given by (5.43). In terms of the above circuit it is

$$R_o = \frac{(R_1 || R_2) + r_\pi}{\beta_F + 1} || r_o \tag{6.9}$$

If a source follower is used instead then the relationship between i_L and v_{GS} is given by (5.4). For the MOS transistor

$$i_L = i_D \tag{6.10}$$

so we can solve for v_{GS} in (5.4) to find v_{GS} in terms of i_L:

$$v_{GS} = V_t + \sqrt{\frac{L}{W}\frac{2I_D}{\mu_n C_{ox}}\left(1 + \frac{V_{DS}}{V_A}\right)} \tag{6.11}$$

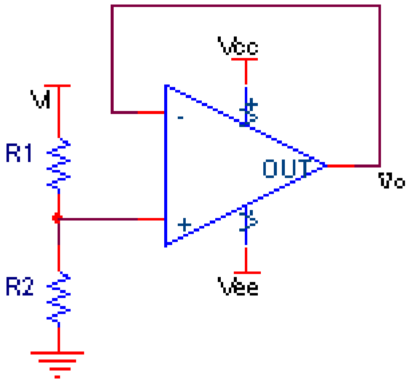
The transfer function is therefore

$$v_O = \frac{R_2 v_I}{R_1 + R_2} - \left(V_t + \sqrt{\frac{L}{W}\frac{2I_D}{\mu_n C_{ox}}\left(1 + \frac{V_{DS}}{V_A}\right)}\right) \tag{6.12}$$

and the output resistance R_o is the same as (5.56):

$$R_o = \frac{1}{g_m + g_{mb} + \frac{1}{r_o} + \frac{1}{R_L}} \tag{6.13}$$

6.3 Resistor divider with operational amplifier buffer

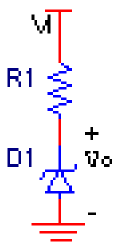


The best way to improve the output resistance of R_o of the resistor divider is to use an operational amplifier buffer on the output (although the use of a full operational amplifier may be unnecessary or undesirable). Unlike the emitter/source follower, the output voltage is not lowered by a v_{BE} (or v_{GS}) drop and is simply

$$v_O = \frac{R_2 v_I}{R_1 + R_2} \tag{6.14}$$

The output resistance R_o is simply the operational amplifier's R_o.

6.4 Zener diode regulator



The Zener diode regulator relies on a Zener diode's reverse-bias breakdown voltage – the reverse-bias voltage V_Z at which a Zener diode begins to conduct current. The Zener diode has a low impedance at V_Z so the reverse-bias voltage remains mostly constant even over a wide range of reverse current through the diode. The series resistor R_1 limits the current through the diode. As long as $V_I > V_Z$ and the current through the diode is nonzero

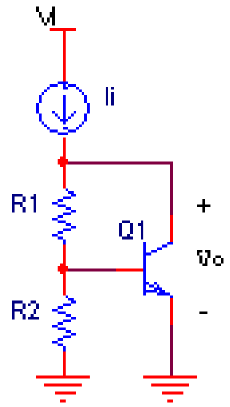
$$v_O = V_Z \tag{6.15}$$

The output resistance R_o is approximately the (low) resistance of the Zener diode in reverse breakdown, R_Z, since generally $R_1 \gg R_Z$ and

$$R_o = R_1 \parallel R_Z \approx R_Z \tag{6.16}$$

As with the resistor divider, the simple Zener diode regulator can be improved by adding an emitter/source follower or operational amplifier buffer to the output. In this case, the emitter/source follower or operational amplifier buffer help ensure that the reverse-bias voltage across the diode remains greater than the diode's reverse-bias breakdown voltage.

6.5 V_{BE} multiplier



The V_{BE} multiplier requires a bipolar transistor with a high β_F. If $\beta_F \gg 1$ then I_B (the base current into the transistor) is negligible. With that assumption the current I through R_1 is equal to the current through R_2. Since the current through the resistors is nearly equal

$$V_O = I(R_1 + R_2) \tag{6.17}$$

The voltage across R_2 is equal to V_{BE} so

$$I = \frac{V_{BE}}{R_2} \tag{6.18}$$

and thus

$$V_O = V_{BE}\left(1 + \frac{R_1}{R_2}\right) \tag{6.19}$$

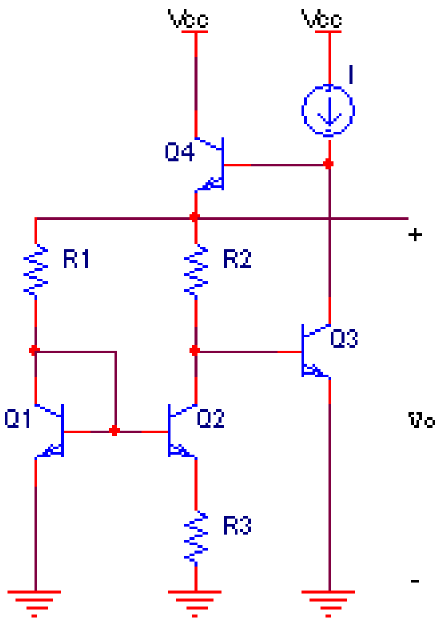
To choose the appropriate I_I, make sure Q_1 is in the forward active region (so that $\beta_F \gg 1$):

$$V_{BE1} > 0 \tag{6.20}$$

and

$$V_{CE1} > V_{CE(\mathrm{sat})} \tag{6.21}$$

6.6 Widlar bandgap reference



The Widlar bandgap reference circuit has two stable operating points but only one desirable operating point, so a start-up circuit (not shown above) is required to ensure that the circuit reaches the desirable operating point. Assuming the circuit is in the desired stable operating point,

$$V_O = V_{BE3} + V_{R2} \tag{6.22}$$

where V_{R2} is the voltage across R_2. The current through R_2 is approximately equal to R_3 if Q_2's $\beta_F \gg 1$, in which case

$$V_{R2} = I_{C2}R_2 = \frac{R_2}{R_3}V_{R3} \tag{6.23}$$

and the voltage across R_3 is

$$V_{R3} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\frac{I_{S2}}{I_{S1}}\right) \tag{6.24}$$

The ratio of I_{C1} to I_{C2} is determined by the ratio of R_2 to R_1, so

$$V_{R3} = V_T \ln\left(\frac{R_2}{R_1}\frac{I_{S2}}{I_{S1}}\right) \tag{6.25}$$

Substituting (6.25) into (6.23),

$$V_{R2} = \frac{R_2}{R_3}V_T \ln\left(\frac{R_2}{R_1}\frac{I_{S2}}{I_{S1}}\right) \tag{6.26}$$

Substituting (6.26) into (6.22),

$$V_O = V_{BE3} + \frac{R_2}{R_3} \ln\left(\frac{R_2}{R_1}\frac{I_{S2}}{I_{S1}}\right) V_T \tag{6.27}$$

The base-emitter voltage is inversely proportional to temperature and the voltage across R_2 is proportional to absolute temperature (PTAT) due to the temperature dependence of V_T, so an appropriate choice of the multiplicative factor to V_T cancels the temperature coefficent for V_O at the desired temperature. The multiplicative factor is determined by three ratios: R_2 to R_3, R_2 to R_1, and I_{S2} to I_{S1}. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 322–323)

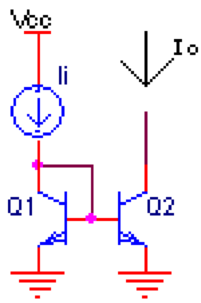
Chapter 7

Current Mirrors and Current Sources

Current mirrors are circuits that are used primarily in integrated circuits to bias other circuit elements or act as active loads (such as in the actively loaded differential pair). They can also be used to sense a current signal in a circuit and mirror (or multiply) it elsewhere to be acted upon or measured by other circuitry. Current mirrors are commonly constructed out of bipolar transistors or MOSFETs. They do not find much use outside of integrated circuits because they require transistor matching and sizing (which is easily accomplished when transistors are manufactured in the same Integrated Circuit (IC) process) and because they usually require less die area than a resistor to provide a particular bias current.

Current mirrors have several important parameters, including current gain, output resistance R_o (ideally infinite), systematic gain error ϵ (deviation from the ideal current gain), and minimum input and output voltages.

7.1 Simple current mirror (Bipolar and MOS)



This is the most basic form of current mirror. The two transistors have the same V_{BE} drop (or V_{GS} in the MOS case) since their bases/gates are tied together and their emitters/sources are both connected to a supply voltage or ground. Q_1/M_1 is diode connected, which means that the base/gate is shorted to the collector/drain.

7.1.1 Bipolar

For the bipolar case,

$$V_{BE1} = V_T \ln \frac{I_{C1}}{I_{S1}} = V_{BE2} = V_T \ln \frac{I_{C2}}{I_{S2}} \tag{7.1}$$

(where I_{S1} and I_{S2} are the transistors' saturation currents and $V_T = \frac{kT}{q}$ is the thermal voltage). Canceling terms on both sides, we see that

$$I_O = I_{C2} = \frac{I_{S2}}{I_{S1}} I_{C1} \tag{7.2}$$

Assuming Q_1 and Q_2 have the same β_F, we also know that

$$I_I = I_{C1} + \frac{I_{C1}}{\beta_F} + \frac{I_{C2}}{\beta_F} \tag{7.3}$$

Solving for I_{C1} and substituting we find

$$I_O = \left(\frac{1}{1 + \frac{1 + (I_{S2}/I_{S1})}{\beta_F}} \right) \left(\frac{I_{S2}}{I_{S1}} \right) I_I \tag{7.4}$$

If $I_{S1} = I_{S2}$ the above equation simplifies to

$$I_O = \left(\frac{1}{1 + \frac{2}{\beta_F}} \right) I_I \tag{7.5}$$

If β_F is large the above equations simplify to

$$I_O \approx \frac{I_{S2}}{I_{S1}} I_I \tag{7.6}$$

A bipolar transistor's saturation current I_S is proportional to its emitter area so the current gain of the current mirror can be any rational number – unity, or less than or greater than unity. The current mirror gets its name from the fact that I_{C1} is mirrored to I_{C2} when the current gain is unity. One way to set the emitter area ratio when the current gain is not unity is to connect M unit bipolar transistors in parallel as Q_2 and N unit bipolar transistors in parallel as Q_1 for an emitter area ratio of M/N.

The above approximation is the ideal current gain of the current mirror. Clearly the approximation is not realized (at least in the bipolar case) due to finite β_F. However, the above analysis neglected the dependence of the transistors' collector currents on the collector-emitter voltage. Taking into account this dependence as well, the transfer function is

$$I_O = \frac{1 + \frac{V_{CE2} - V_{CE1}}{V_A}}{1 + \frac{1 + I_{S2}/I_{S1}}{\beta_F}} \frac{I_{S2}}{I_{S1}} I_I \tag{7.7}$$

where V_A is the Early voltage. The systematic gain error is therefore

$$\epsilon = \frac{1 + \frac{V_{CE2} - V_{CE1}}{V_A}}{1 + \frac{1 + I_{S2}/I_{S1}}{\beta_F}} - 1 \tag{7.8}$$

and is thus caused by both finite β_F and finite output resistance $r_o = \frac{V_A}{I_C}$.

The input voltage V_I is simply

$$V_I = V_{CE1} = V_{BE1} \tag{7.9}$$

since Q_1 is diode connected, and the minimum output voltage is

$$V_{O(\text{min})} = V_{CE2(\text{sat})} \tag{7.10}$$

since Q_2 must remain in the forward active region.

Another important characteristic of a current mirror is its output resistance. Ideally, its output resistance is infinite since the current mirror is a current source. Of course, no real current mirror has an infinite resistance – in reality the output resistance is dependent on the output current. For the bipolar case the output resistance (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 255–256) R_o is

$$R_o = r_{o2} = \frac{V_A}{I_{C2}} = \frac{V_A}{I_O} \tag{7.11}$$

7.1.2 MOS

The MOS current mirror has the same topology as the bipolar current mirror, and its analysis is similar. The MOSFETs must be biased so that $V_{GS} > V_t$ (where V_t is the threshold voltage). Using the characteristic equation of a MOSFET in the active region and noting that $V_{GS1} = V_{GS2}$ we see that

$$V_{GS1} = V_t + \sqrt{\frac{2I_{D1}}{k'(W/L)_1}} = V_{GS2} = V_t + \sqrt{\frac{2I_{D2}}{k'(W/L)_2}} \tag{7.12}$$

Canceling terms on both sides we see that

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{D1} = \frac{(W/L)_2}{(W/L)_1} I_I \tag{7.13}$$

As with the bipolar case, the current gain can be set to any rational number by sizing the MOSFETs appropriately. (ibid., p. 258)

Similar to the bipolar case, the above analysis neglects the slight dependence of a MOSFET's I_D to its V_{DS}. If we take this dependency into account, the transfer function is

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_I \left(1 + \frac{V_{DS2} - V_{DS1}}{V_A}\right) \tag{7.14}$$

where $V_A = 1/\lambda$, the MOS equivalent of the Early voltage. The systematic gain error is therefore

$$\epsilon = \frac{V_{DS2} - V_{DS1}}{V_A} \tag{7.15}$$

The input voltage V_I is simply

$$V_I = V_{DS1} = V_{GS1} \tag{7.16}$$

since M_1 is diode connected, the minimum output voltage $V_{O(min)}$ is

$$V_{O(min)} = V_{ov2} = \sqrt{\frac{2I_O}{(W/L)_2 k}} \tag{7.17}$$

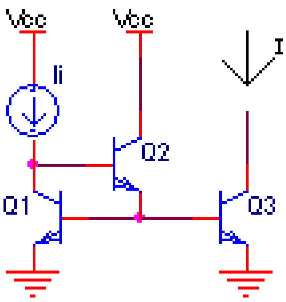
where V_{ov} is the overdrive voltage above V_t (i.e. $V_{GS} = V_t + V_{ov}$). The output resistance R_o is (ibid., pp. 256, 259)

$$R_o = r_{o2} = \frac{1}{\lambda I_{D2}} = \frac{1}{\lambda I_O} \tag{7.18}$$

For all current mirrors, the current source I_I can be implemented by a number of devices. The simplest is a resistor. In that case, use the desired I_{C1} and I_{C2} (or I_{D1} and I_{D2} in the MOS case) to determine $V_{BE1} = V_{CE1}$ (or $V_{GS1} = V_{DS1}$) from the transistor's characteristic equation, and then use KVL to find $R = \frac{V_{CC}-V_{CE1}}{I_{C1}}$ (or $R = \frac{V_{DD}-V_{DS1}}{I_{D1}}$).

One very useful aspect of current mirrors is that Q_1 (or M_1) can be used to generate as many output currents as needed; for each output current simply add another transistor whose base (or gate) is tied to the base (or gate) of Q_1 (or M_1) and whose emitter (or source) is tied to the emitter (or source) of Q_1 (or M_1). The additional output currents flow into the collectors (or drains) of these additional transistors and, by choosing the emitter areas or W/L ratios appropriately, the additional output currents can all have different values.

7.2 Simple current mirror with β_F helper



For the bipolar simple current mirror we assumed β_F was large enough that we could approximate $I_O = \frac{I_{S2}}{I_{S1}} I_I$ (the MOS current mirror has an approximately infinite β_F so it is not applicable here). To make the current mirror better approximate this ideal relationship (especially if β_F is relatively small) an additional transistor is added. In this case, KCL at Q_1's collector yields

$$I_I = I_{C1} + I_{B2} \tag{7.19}$$

To find I_{B2} note that

$$I_{E2} = \frac{I_{C1}}{\beta_F} + \frac{I_{C3}}{\beta_F} \tag{7.20}$$

and

$$I_{B2} = \frac{I_{E2}}{\beta_F + 1} \tag{7.21}$$

so substituting (7.20) into (7.21) we have

$$I_{B2} = \frac{I_{C1} + I_{C3}}{\beta_F(\beta_F + 1)} \tag{7.22}$$

Also,

$$I_{C1} = \frac{I_{S1}}{I_{S3}} I_{C3} = \frac{I_{S1}}{I_{S3}} I_O \tag{7.23}$$

as before. Substituting (7.22) and (7.23) into (7.19) we see

$$I_I = \frac{I_{S1}}{I_{S3}} I_O + \frac{I_{C1} + I_{C3}}{\beta_F(\beta_F + 1)} = \frac{I_{S1}}{I_{S3}} I_O + \frac{\frac{I_{S1}}{I_{S3}} I_O + I_O}{\beta_F(\beta_F + 1)} \tag{7.24}$$

Solving for I_O we see that

$$I_O = \left(\frac{1}{1 + \frac{1 + (I_{S3}/I_{S1})}{\beta_F(\beta_F + 1)}} \right) \frac{I_{S3}}{I_{S1}} I_I \tag{7.25}$$

which is the same as the simple current mirror except for the extra $\beta_F + 1$ term which multiplies with β_F.

The approximation that

$$I_O \approx \frac{I_{S3}}{I_{S1}} I_I \tag{7.26}$$

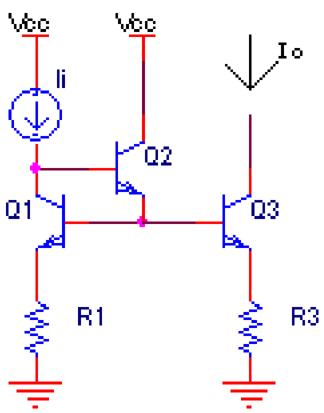
is even better with the β_F helper. Since a MOSFET has $\beta_F \approx \infty$ the base current error can be completely eliminated if a MOSFET is used as the β_F helper transistor.

The β_F helper does not significantly alter the output resistance R_o or the minimum output voltage $V_{O(min)}$, but the input voltage is created by the V_{BE} drop of the β_F helper (or V_{GS} if the β_F helper is a MOSFET). Assuming a bipolar β_F helper, the input voltage is thus

$$V_I = V_{BE1} + V_{BE2} \tag{7.27}$$

The current mirror with β_F helper is also better when multiple outputs are needed. For every extra output another transistor's base must be connected to the base of Q_1, which increases the gain error due to the finite β_F. The β_F helper reduces this gain error for each output by $\beta_F + 1$. The cost of the β_F helper is that V_{CE1} has an extra V_{BE} drop (now $V_{CE1} = V_{BE1} + V_{BE2}$), which can be a limitation if V_{CC} is low. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 261–262)

7.3 Simple current mirror with β_F helper and degeneration



7.3.1 Bipolar

Emitter degeneration improves a current mirror by providing better matching between the input current I_I and output current I_{C3}, and by increasing the mirror's output resistance R_o from $R_o = r_{o3}$ to

$$R_o \approx r_{o3}(1 + g_m R_3) \tag{7.28}$$

The increased R_o not only makes the current mirror behave more like an ideal current source (which has an infinite R_o), but it decreases the systematic gain error ϵ since a finite R_o contributes to ϵ. A simple current mirror with a β_F helper and emitter degeneration thus has a systematic gain error of

$$\epsilon = \frac{1 + \frac{V_{CE2} - V_{CE1}}{V_A(1 + \frac{I_{C3}R_3}{V_T})}}{1 + \frac{1 + I_{S2}/I_{S1}}{\beta_F(\beta_F + 1)}} - 1 \tag{7.29}$$

The drawback of emitter degeneration is, of course, the increase in the minimum input and output voltages by approximately $I_I R_1$ and $I_O R_3$, respectively. The transfer function is easily expressed in implicit form by using KVL and noting that $I_I = I_{C1}$ and $I_O = I_{C3}$:

$$I_I R_1 + V_T \ln \frac{I_I}{I_{S1}} = I_O R_3 + V_T \ln \frac{I_O}{I_{S3}} \tag{7.30}$$

so

$$I_O = \frac{1}{R_3}\left(I_I R_1 + V_T \ln \frac{I_I I_{S3}}{I_O I_{S1}}\right) \tag{7.31}$$

Given a desired input/output current ratio $\frac{I_O}{I_I}$, I_O can be set by choosing the appropriate resistor ratio $\frac{R_1}{R_3}$ and/or sizing the transistors appropriately (which changes $\frac{I_{S3}}{I_{S1}}$).

The emitter degeneration resistors are limited by the supply voltage V_{CC} since the input voltage V_I is

$$V_I = I_{E1}R_1 + V_{BE1} + V_{BE2} = \left(\frac{1}{\beta_F} + 1\right) I_{C1}R_1 + V_{BE1} + V_{BE2} \tag{7.32}$$

and the minimum output voltage $V_{O(min)}$ is

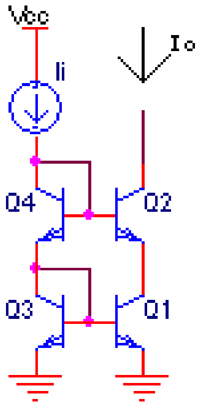
$$V_{O(\text{min})} = I_{E3}R_3 + V_{CE3(\text{sat})} = \left(\frac{1}{\beta_F} + 1\right) I_{C3}R_3 + V_{CE3(\text{sat})} \tag{7.33}$$

and both must be less than V_{CC}.

7.3.2 MOS

Source degeneration is not as commonly used as emitter degeneration because matching of MOS current mirrors can be improved by increasing the MOS transistors' gate areas, and R_O can be increased by increasing the transitors' channel length. Nonetheless, the analysis for the bipolar current mirror with β_F helper and emitter degeneration can be applied to a MOS variant easily. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 262–263)

7.4 Cascode current mirror (Bipolar and MOS)



7.4.1 Bipolar

A cascode current mirror significantly increases R_o. Transistors Q_1 and Q_3 in the above schematic form a simple current mirror (which may also include emitter degeneration). Q_2 is in a common base configuration and transfers I_{C1} to $I_O = I_{C2}$, and Q_4 is connected as a diode to properly bias Q_2 and ensure it is in the forward active region. R_o is greatly increased over the simple current mirror (even with emitter degeneration) because the "emitter resistance" is the resistance looking into the collector of Q_1. Small-signal analysis reveals that

$$R_o \approx \frac{\beta_F r_{o2}}{2} \tag{7.34}$$

(R_o is reduced by half due to the simple current mirror formed by Q_1 and Q_3, which diverts half of $I_O = I_{C2}$ through $r_{\pi 2}$). (ibid., p. 264) The drawback of the cascode current mirror versus a simple current mirror is that the input voltage is increased to

$$V_I = V_{BE3} + V_{BE4} \tag{7.35}$$

and the minimum output voltage is increased to

$$V_{O(\mathrm{min})} = V_{BE1} + V_{CE(\mathrm{sat})} \tag{7.36}$$

so that both Q_1 and Q_2 are in the forward active region.

To derive the cascode current mirror's transfer function we note that

$$I_{E4} = I_{C3} + \frac{2I_{C3}}{\beta_F} \tag{7.37}$$

$$I_I = I_{E4} + \frac{I_{C2}}{\beta_F} \tag{7.38}$$

$$I_O = I_{C2} = \frac{\beta_F}{\beta_F + 1} I_{C3} \tag{7.39}$$

Substituting (7.37) into (7.38) we find

$$I_I = I_{C3} + \frac{2I_{C3}}{\beta_F} + \frac{I_{C3}}{\beta_F + 1} \tag{7.40}$$

Rearranging (7.40) to solve for I_{C3} and substituting the result into (7.39), we see that

$$I_O = \frac{\beta_F}{\beta_F + 1} \frac{I_I}{1 + \frac{2}{\beta_F} + \frac{1}{\beta_F+1}} = I_I \left(1 - \frac{4\beta_F + 2}{\beta_F^2 + 4\beta_F + 2}\right) \tag{7.41}$$

The systematic gain error is clear from the above transfer function:

$$\epsilon = -\frac{4\beta_F + 2}{\beta_F^2 + 4\beta_F + 2} \approx -\frac{4}{\beta_F + 4} \tag{7.42}$$

and is generally greater than ϵ for a simple current mirror.

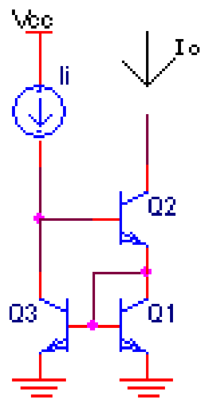
7.4.2 MOS

The MOS version of the cascode current mirror does not have the same finite β_F problems as the bipolar version. Consequently, a MOS cascode current mirror can be made to have as high an output resistance as needed by increasing the number of stacked cascode MOSFETs (provided the increase in the minimum input and output voltages required by the additional cascodes is acceptable). The output resistance for a single MOS cascode current mirror is

$$R_o = r_{o2}(1 + (g_{m2} + g_{mb2})r_{o1}) + r_{o1} \tag{7.43}$$

and each cascode increases R_o by approximately a factor of $1 + g_m r_o$ (although in practice R_o is limited by parasitic leakage paths as the number of cascodes increases). (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 263–268)

7.5 Wilson current mirror



7.5.1 Bipolar

The Wilson current mirror is a slight variation on the cascode current mirror. Q_4 is removed and Q_1 is the only diode connected transistor, which ensures that

$$V_{CE3} = V_{BE1} + V_{BE2} \approx 2V_{BE} \tag{7.44}$$

Bipolar Wilson current mirrors are designed to minimize the systematic gain error ϵ in cascode current mirrors caused by finite β_F by using negative feedback through Q_1 to activate Q_3, which increases R_o and reduces the base current error.

To find the transfer function, first use KCL at Q_1's collector to find

$$I_{E2} = I_{C1} + I_{B1} + I_{B3} = I_{C1}\left(1 + \frac{1}{\beta_F}\right) + \frac{I_{C3}}{\beta_F} \tag{7.45}$$

Approximating $I_{C1} = I_{C3}$, we see that

$$I_{E2} = I_{C1}\left(1 + \frac{2}{\beta_F}\right) \tag{7.46}$$

It follows that

$$I_O = I_{C2} = I_{E2}\frac{\beta_F}{1+\beta_F} = I_{C1}\left(1 + \frac{2}{\beta_F}\right)\left(\frac{\beta_F}{1+\beta_F}\right) \tag{7.47}$$

Finally, substituting

$$I_{C1} = I_I - \frac{I_{C2}}{\beta_F} \tag{7.48}$$

into (7.47) yields

$$I_O = \frac{I_I}{1 + \frac{2}{\beta_F(\beta_F+2)}} \tag{7.49}$$

The systematic gain error ϵ due to finite β_F is much less than that of the cascode current mirror since there is a β_F^2 term. Note that for simplicity of analysis we have neglected the dependence of I_C on V_{CE}.

Calculation of the output resistance R_o is a bit complicated, so we only give an outline of the derivation here: apply a test current i_t into the output node of the current mirror's small signal model and determine the resulting test voltage v_t, which gives $R_o = \frac{v_t}{i_t}$. The small signal model can be simplified by noting that the small signal resistance from the diode connected Q_1's base to ground is $1/g_{m1} \parallel r_{\pi 1} \parallel r_{\pi 3} \parallel r_{o1} \approx 1/g_{m1}$. Also, Q_3 is a voltage controlled current source of magnitude $g_{m3}v_{\pi 3} = g_{m3}v_{\pi 1} \approx g_{m3}i_1/g_{m1} \approx i_1$ (where i_1 is the small signal current through the $1/g_{m1}$ resistance from Q_1's base to ground). With the model simplified as such, it is easy to see that

$$v_t = \frac{i_i}{g_{m1}} + (i_t - g_{m2}v_{\pi 2})r_{o2} \tag{7.50}$$

KCL at Q_3's collector and Q_2's emitter gives i_1 in terms of i_t, g_{m1}, r_{o3}, and $r_{\pi 2}$, and $v_{\pi 2}$ in terms of i_t, $r_{\pi 2}$, g_{m1}, r_{o3}, and $r_{\pi 2}$. The equations for i_1 and $v_{\pi 2}$ can then be substituted into (7.50), and rearranging gives (ibid., pp. 274–277)

$$R_O = \frac{1}{g_{m1}\left(1 + \frac{1+\frac{1}{g_{m1}r_{o3}}}{1+\frac{r_{\pi 2}}{r_{o3}}}\right)} + r_{o2} + \frac{g_{m2}r_{\pi 2}r_{o2}\left(1 + \frac{1}{g_{m1}r_{o3}}\right)}{2 + \frac{r_{\pi 2}}{r_{o3}} + \frac{1}{g_{m1}r_{o3}}} \tag{7.51}$$

For $r_{o3} \to \infty$, we can simplify the above equation considerably:

$$R_O \approx \frac{1}{2g_{m1}} + r_{o2} + \frac{g_{m2}r_{\pi 2}r_{o2}}{2} \approx \frac{\beta_F r_{o2}}{2} \tag{7.52}$$

Fortunately, the input and minimum output voltages can be determined by inspection: they are

$$V_I = V_{BE1} + V_{BE2} \approx 2V_{BE} \tag{7.53}$$

$$V_{O(\text{min})} = V_{BE1} + V_{CE(\text{sat})} \tag{7.54}$$

7.5.2 MOS

The MOS variant is analogous to the bipolar case, except that $\beta_F \to \infty$ and $r_\pi \to \infty$. The above analysis for the bipolar case thus suggests that

$$I_O = I_I \tag{7.55}$$

$$R_o = \frac{1}{g_{m1}} + r_{o2} + g_{m2} r_{o2} \left(1 + \frac{1}{g_{m1} r_{o3}}\right) r_{o3} \approx (1 + g_{m2} r_{o3}) r_{o2} \tag{7.56}$$

Since we neglected the dependence of I_C on V_{CE} for the analysis of the bipolar Wilson current mirror, we have also neglected the the dependence of I_D on V_{DS} for the MOS case. The systematic gain error ϵ thus is not zero as the above transfer function would suggest. Due to the mismatch between V_{DS1} and V_{DS3}, the systematic gain error is actually

$$\epsilon = \frac{V_{DS1} - V_{DS3}}{V_A} \tag{7.57}$$

The input voltage is simply

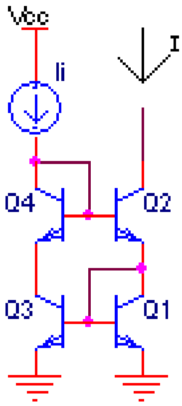
$$V_I = V_{GS1} + V_{GS2} \tag{7.58}$$

and the minimum output voltage is

$$V_{O(\text{min})} = V_{GS1} + V_{GS2} = V_t + 2V_{ov} \tag{7.59}$$

where V_{ov} is the overdrive voltage about V_t.

7.6 Improved Wilson current mirror



The improved Wilson current mirror adds a fourth transistor whose base (or gate) is connected to Q_2 (or M_2) and is placed in series with Q_3 (or M_3). This fourth transistor forces the collector (or drain) voltage of Q_1 (or M_1) to equal the collector (or drain) voltage of Q_3 (or M_3) so that $V_{CE1} = V_{CE3}$ (bipolar) and $V_{DS1} = V_{DS3}$ (MOS). This eliminates the systematic gain error due to the voltage mismatches in the simple Wilson current mirror, thus reducing ϵ in the bipolar case and eliminating it in the MOS case. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 277–278)

7.6.1 Bipolar

The characteristic equations of the bipolar improved Wilson current mirror are

$$I_O = \frac{I_I}{1 + \frac{2}{\beta_F(\beta_F+2)}} \tag{7.60}$$

$$V_I = V_{BE1} + V_{BE2} \approx 2V_{BE} \tag{7.61}$$

$$V_{O(min)} = V_{BE1} + V_{CE(sat)} \tag{7.62}$$

$$\epsilon = \frac{1}{1 + \frac{2}{\beta_F(\beta_F+2)}} \tag{7.63}$$

$$R_o = \frac{1}{g_{m1}\left(1 + \frac{1+\frac{1}{g_{m1}r_{o3}}}{1+\frac{r_{\pi2}}{r_{o3}}}\right)} + r_{o2} + \frac{g_{m2}r_{\pi2}r_{o2}\left(1 + \frac{1}{g_{m1}r_{o3}}\right)}{2 + \frac{r_{\pi2}}{r_{o3}} + \frac{1}{g_{m1}r_{o3}}} \tag{7.64}$$

The output resistance R_o can be approximated as

$$R_o \approx \frac{1}{2g_{m1}} + r_{o2} + \frac{g_{m2}r_{\pi2}r_{o2}}{2} \approx \frac{\beta_F r_{o2}}{2} \tag{7.65}$$

The only difference is in ϵ, which no longer has a component caused by a mismatch between V_{CE1} and V_{CE3}.

7.6.2 MOS

The characteristic equations of the MOS improved Wilson current mirror are

$$I_O = I_I \tag{7.66}$$

$$R_O = \frac{1}{g_{m1}} + r_{o2} + g_{m2}r_{o2}\left(1 + \frac{1}{g_{m1}r_{o3}}\right) r_{o3} \approx (1 + g_{m2}r_{o3})r_{o2} \tag{7.67}$$

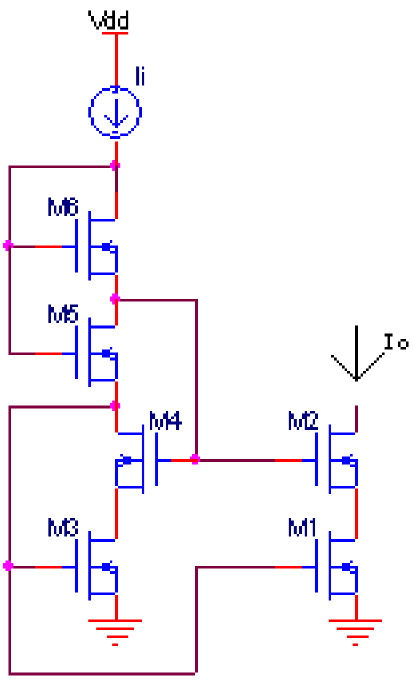
$$V_I = V_{GS1} + V_{GS2} \tag{7.68}$$

$$V_{O(min)} = V_{GS1} + V_{GS2} = V_t + 2V_{ov} \tag{7.69}$$

$$\epsilon = 0 \tag{7.70}$$

The only difference is again in ϵ, which in the MOS case is reduced to zero since there is no systematic gain error due to finite β_F, and the systematic gain error due to the mismatch betweeen V_{DS1} and V_{DS3} has been reduced to zero due to the fact that we now have $V_{DS1} = V_{DS3}$.

7.7 Sooch cascode current mirror (MOS)



The Sooch cascode current mirror is designed to allow a higher output voltage swing by increasing $V_{O(min)}$ at the expense (increase) of $V_{I(min)}$. Referring back to the single MOS cascode current mirror shown above,

$$V_{DS1} = V_{GS3} + V_{GS4} - V_{GS2} = V_t + V_{ov} \tag{7.71}$$

where V_{ov} is the overdrive voltage above the MOSFETs' V_t (i.e. $V_{GS} = V_t + V_{ov}$). Since M_1 only requires

$$V_{DS1} \geq V_{ov} \tag{7.72}$$

to remain in the active region, the cascode current mirror biases V_{DS1} unnecessarily large. The Sooch cascode current mirror level shifts V_{G2} down by V_t so that

$$V_{DS1} = V_{ov} \tag{7.73}$$

and thus

$$V_{O(\mathrm{min})} = 2V_{ov} \tag{7.74}$$

The necessary level shift is achieved by adding M_5 and M_6 and rewiring M_4 as shown in the above schematic. First, consider M_5 and M_6 alone: M_6 is diode connected so it is biased in the active region as long as

$$I_{D6} = I_I > 0 \tag{7.75}$$

$$V_{GS6} > V_t \tag{7.76}$$

A channel exists at the drain of M_5 since

$$V_{GS6} = V_{DG5} \tag{7.77}$$

and a channel exists at the source of M_6. M_5 is thus biased in the triode region by M_6. We want

$$V_{G2} = V_{GS3} + V_{DS5} = V_t + 2V_{ov} \tag{7.78}$$

so that

$$V_{DS1} = V_{G2} - V_{GS2} = (V_t + 2V_{ov}) - (V_t + V_{ov}) = V_{ov} \tag{7.79}$$

We know

$$V_{GS3} = V_{S5} = V_t + V_{ov} \tag{7.80}$$

so we need

$$V_{DS5} = V_{ov} \tag{7.81}$$

We also need

$$V_{GS6} = V_t + V_{ov} \tag{7.82}$$

so that I_{D6} is equal to the other drain currents. Since M_5 is in the triode region and M_6 is in the active region, we know that

$$I_I = I_{D5} = I_{D6} = \frac{k'}{2}\left(\frac{W}{L}\right)_6 (V_{GS6} - V_6)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_5 (2(V_{GS5} - V_t)V_{DS5} - V_{DS5}^2) \tag{7.83}$$

Substituting

$$V_{GS5} = V_{GS6} + V_{DS5} = V_t + 2V_{ov} \tag{7.84}$$

into (7.83), we have

$$\frac{k'}{2}\left(\frac{W}{L}\right)_6 V_{ov}^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_5 (4V_{ov}^2 - V_{ov}^2) \tag{7.85}$$

so we need

$$(\frac{W}{L})_5 = \frac{1}{3}(\frac{W}{L})_6 \tag{7.86}$$

M_4 is obviously used to ensure that

$$V_{DS1} = V_{DS3} \tag{7.87}$$

to minimize the systematic gain error ϵ. With M_4 connected as shown, we have

$$V_{DS3} = V_{G2} - V_{GS4} \tag{7.88}$$

We designed

$$V_{G2} = V_t + 2V_{ov} \tag{7.89}$$

(ignoring channel length modulation) so that

$$V_O = 2V_{ov} \tag{7.90}$$

and we know that

$$V_{GS4} = V_t + V_{ov} \tag{7.91}$$

(ignoring the body effect and assuming that M_4 is in the active region), so we can substitute these equations to find that

$$V_{DS3} = V_{ov} \tag{7.92}$$

V_{DS3} is thus equal to V_{DS1}. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 270–273) A MOS current mirror does not suffer from finite β_F so the matched $V_{DS1} = V_{DS3}$ means that

$$\epsilon = 0 \tag{7.93}$$

The Sooch cascode current mirror has the same output resistance R_o as the simple cascode current mirror since the output transistors are unchanged:

$$R_o = r_{o2}(1 + (g_{m2} + g_{mb2})r_{o1}) + r_{o1} \tag{7.94}$$

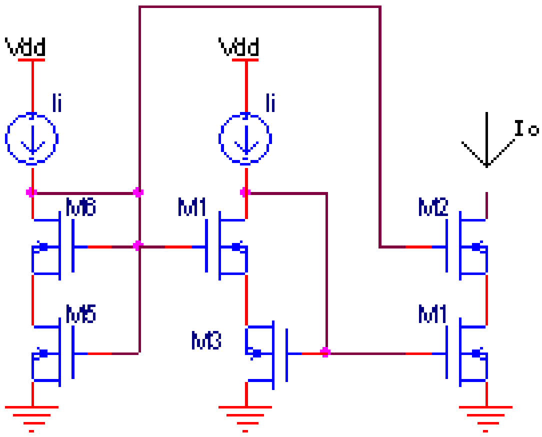
The Sooch cascode current mirror has good $V_{O(min)}$ and ϵ, but the low $V_{O(min)}$ comes at the cost of

$$V_{I(min)} = V_{GS3} + V_{GS5} \tag{7.95}$$

From the above analysis, this gives

$$V_{I(min)} = 2V_t + 3V_{ov} \tag{7.96}$$

7.8 High-swing current mirror with two input branches



The above Sooch cascode current mirror provides a high output voltage swing using only one input branch at the cost of significantly increasing $V_{I(min)}$. This circuit also provides a high output voltage swing but uses a second input branch to lower $V_{I(min)}$. The second input branch increases the current mirror's power consumption since the second branch draws additional current from V_{DD}; in contrast, the added transistors in the Sooch cascode current mirror share the same current as the two transistors of simple cascode current mirror's input branch so they do not increase power consumption. If V_{DD} is too low or needs to be minimized, however, the increase of $V_{I(min)}$ may prohibit the use of the Sooch cascode current mirror in favor of this circuit.

M_5 and M_6 are configured the same for this circuit and the Sooch cascode current mirror, so from the above analysis we need

$$\left(\frac{W}{L}\right)_5 = \frac{1}{3}\left(\frac{W}{L}\right)_6 \tag{7.97}$$

The minimum input voltage for this circuit is the greater of the two minimum input voltages for each of the input branches. The left input branch has

$$V_{I(\min)} = V_{DS5} + V_{GS6} = V_t + 2V_{ov} \tag{7.98}$$

and the right input branch has

$$V_{I(\min)} = V_{GS3} = V_t + V_{ov} \tag{7.99}$$

Thus, the overall minimum input voltage is (ibid., p. 273)

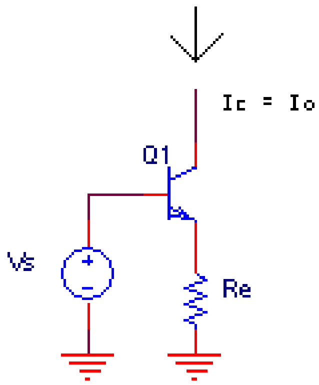
$$V_{I(\min)} = V_t + 2V_{ov} \tag{7.100}$$

As with the Sooch cascode current mirror, the output transistors are unmodified from the simple cascode current mirror so

$$R_o = r_{o2}(1 + (g_{m2} + g_{mb2})r_{o1}) + r_{o1} \tag{7.101}$$

$$V_{O(\min)} = 2V_{ov} \tag{7.102}$$

7.9 Collector current source



This is a very basic current source which uses a voltage source V_S and emitter resistor R_E to bias a bipolar transistor to the desired collector current I_C, which is the output of the current source. The voltage source and R_E determine

$$V_{BE} = V_S - I_E R_E = V_S - \frac{\beta_F + 1}{\beta_F} I_C R_E \tag{7.103}$$

where the latter equation results from the relationship between I_C and I_E defined in (5.3). Thus, the output current can be expressed in terms of V_{BE} as

$$I_C = \frac{\beta_F}{\beta_F + 1} \frac{V_S - V_{BE}}{R_E} \tag{7.104}$$

Solving for V_{BE} in (5.1) we find

$$V_{BE} = V_{th} \ln\left(\frac{I_C}{I_S} + 1\right) \tag{7.105}$$

so that we can express I_C in a transcendental equation

$$I_C = \frac{\beta_F}{\beta_F + 1} \frac{V_S - V_{th} \ln\left(\frac{I_C}{I_S} + 1\right)}{R_E} \tag{7.106}$$

The bipolar transistor is configured the same way as the common emitter, so the output resistance R_O can be borrowed from (5.25):

$$R_o = \left(\frac{r_\pi R_E}{r_\pi + R_E} + r_o\left(1 + g_m \frac{r_\pi R_E}{r_\pi + R_E}\right)\right) \tag{7.107}$$

The MOS version of the collector current source is the drain current source. With a source resistor R_S the output current $I_D = I_O$ depends on V_{GS} as

$$I_D = \frac{V_S - V_{GS}}{R_S} \tag{7.108}$$

By rearranging (5.4) to solve for V_{GS} and substituting into (7.108) we can express I_O as a transcendental equation:

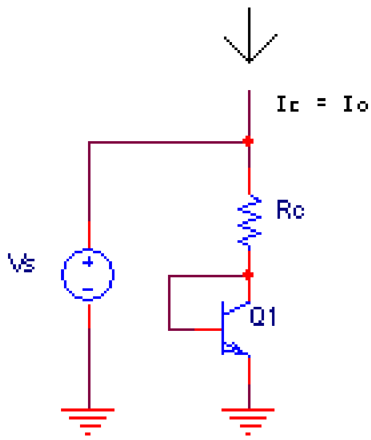
$$I_D = \frac{V_S - V_t - \sqrt{\frac{L}{W}\frac{2I_D}{\mu_n C_{ox}}}}{R_S} \tag{7.109}$$

The MOSFET is configured as a common source so the output resistance R_o is

$$R_o = R_S + (1 + (g_m + g_{mb})R_S)r_o + R_S \tag{7.110}$$

which is borrowed from (5.36).

7.10 Diode connected collector/drain current source



The diode connected collector current source is similar to the simple collector current source. KVL around the circuit's loop shows that

$$I_C R_C = V_S - V_{CE} = V_S - V_{BE} \tag{7.111}$$

Dividing both sides by R_C to solve for $I_C = I_O$ gives

$$I_O = \frac{V_S - V_{BE}}{R_C} \tag{7.112}$$

This is nearly identical to (7.104), so we can borrow the above analysis to express I_O as a transcendental equation:

$$I_C = \frac{V_S - V_{th}\ln\left(\frac{I_C}{I_S} + 1\right)}{R_C} \tag{7.113}$$

The MOS version is the diode connected drain current source. With a drain resistor R_D the output current $I_O = I_D$ is

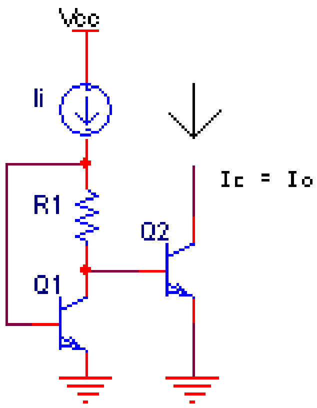
$$I_O = \frac{V_S - V_{GS}}{R_D} \tag{7.114}$$

Again, we can borrow the above analysis to write I_O as a transcendental equation:

$$\frac{V_S - V_t - \sqrt{\frac{L}{W}\frac{2I_D}{\mu_n C_{ox}}}}{R_D} \tag{7.115}$$

A notable characteristic of this current source is that the output voltage is simply V_S.

7.11 Peaking current source



The Peaking current source is useful for generating very small currents (e.g., in the nA range) without using large values of resistance. It is available in bipolar and CMOS technologies with identical topologies but with a slightly different analysis between the bipolar and CMOS versions.

7.11.1 Bipolar

Applying KVL and neglecting the small I_{B1} current,

$$V_{BE2} = V_{BE1} - I_I R_1 \tag{7.116}$$

Still neglecting the small base currents,

$$I_{C1} = I_I \tag{7.117}$$

and, trivially,

$$I_{C2} = I_O \tag{7.118}$$

Using (5.1) and solving it for V_{BE}, we can substitute for V_{BE1} and V_{BE2} in (7.116) and substitute I_I for I_{C1} and I_O for $= I_{C2}$ to find

$$I_I R_1 = V_T \ln\left(\frac{I_I}{I_{S1}}\right) - V_T \ln\left(\frac{I_O}{I_{S2}}\right) \tag{7.119}$$

If Q_1 and Q_2 are identical so that $I_{S1} = I_{S2}$ we can rewrite (7.119) and solve for I_O in terms of I_I:

$$I_O = I_I e^{-\frac{I_I R_1}{V_T}} \tag{7.120}$$

For a circuit design problem in which I_I and I_O are determined and the appropriate value of R_1 must be found, it is useful to know R_1 in terms of I_I and I_O. Rewriting (7.119) and again assuming Q_1 and Q_2 are identical,

$$R_1 = \frac{V_T}{I_I} \ln\left(\frac{I_I}{I_O}\right) \tag{7.121}$$

To demonstrate the usefulness of the Peaking current source for generating small currents without requiring large resistors, suppose $I_I = 10\,\mu\text{A}$ and $I_O = 100\,\text{nA}$. Also suppose $V_T = 26\,\text{mV}$ (the approximate thermal voltage at room temperature). In that case application of (7.121) shows that the required resistor would be $R_1 \approx 12\,\text{k}\Omega$. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 303–304)

7.11.2 MOS

The analysis of the MOS Peaking current source is similar. KVL shows that

$$V_{GS2} = V_{GS1} - I_I R_1 \tag{7.122}$$

The sources of M_1 and M_2 are connected together so the threshold voltages V_t cancel and (7.122) simplifies to

$$V_{ov2} = V_{ov1} - I_I R_1 \tag{7.123}$$

where the overdrive voltage V_{ov} is defined as $V_{ov} = V_{GS} - V_t$. Assuming M_1 and M_2 operate in the active region and strong inversion, we can use (5.4) and (7.123) to find

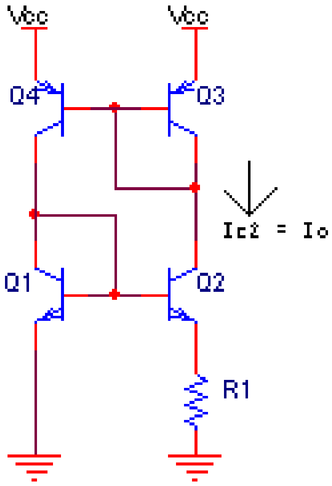
$$I_O = \frac{k'}{2}\left(\frac{W}{L}\right)_2 V_{ov2}^2 = \frac{k'}{2}\left(\frac{W}{L}\right)_2 (V_{ov1} - I_I R_1)^2 \tag{7.124}$$

However, the input current I_I is often small enough that M_1 must operate in weak inversion and, since $V_{ov2} < V_{ov1}$ from (7.123), M_2 must also operate in weak inversion (where I_D is an exponential function of V_{GS}). Assuming $V_{DS1} > 3V_T$ and $V_{DS2} > 3V_T$ and the transistors are identical, we can apply (5.6) to both transistors and substitute into (7.124) to find

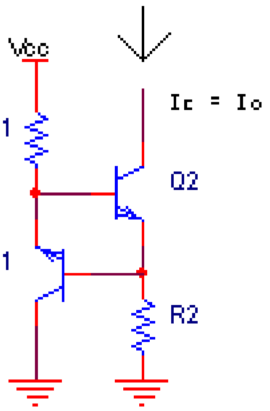
$$I_O \approx \frac{W}{L} I_t e^{\frac{V_{GS2} - V_t}{n V_T}} \approx I_I e^{\frac{I_I R_1}{n V_T}} \tag{7.125}$$

The transfer functions of the bipolar and MOS versions of the Peaking current source are thus nearly the same, with the exception of the multiplicative factor n to the thermal voltage V_T, where n is defined in (5.8). For MOS transistors, $1.3 \leq n \leq 1.5$ and effectively $n = 1$ for bipolar transistors. (ibid., pp. 304–305)

7.12 ΔV_{BE} current source (DC Analysis 1)



7.13 Base-emitter referenced current source



The base-emitter referenced current source is designed to decrease the sensitivity of the output current I_O on the supply voltage V_{CC} by designing I_O to depend on a transistor's V_{BE}. Assuming both transistors are biased in the forward active region, the base currents are small and can be neglected so that we can use (5.1) solved for V_{BE} to find

$$V_{BE1} = V_T \ln\left(\frac{I_I}{I_{S1}}\right) \tag{7.126}$$

since

$$I_C = I_I - I_{B2} \approx I_I \tag{7.127}$$

The voltage across R_2 is simply V_{BE1} and the current through it is I_{E2} so

$$I_{E2} = \frac{V_{BE1}}{R_2} = \frac{V_T}{R_2}\ln\left(\frac{I_I}{I_{S1}}\right) \tag{7.128}$$

Again assuming the base currents are negligible

$$I_O = I_{C2} = I_{E2} - I_{B2} \approx I_{E2} \tag{7.129}$$

so that

$$I_O = \frac{V_T}{R_2} ln(\frac{I_I}{I_{S1}}) \tag{7.130}$$

Since the point of the base-emitter reference current source is to decrease the sensitivity of I_O to V_{CC}, $S_{V_{CC}}^{I_O}$, it is useful to quantify it. By definition (Gray et al., *Analysis and Design of Analog Integrated Circuits*, p. 306),

$$S_{V_{CC}}^{I_O} = \frac{V_{CC}}{I_O} \frac{\partial I_O}{\partial V_{CC}} \tag{7.131}$$

so differentiating (7.130) with respect to V_{CC} and substituting the result into (7.131) shows that

$$S_{V_{CC}}^{I_O} = \frac{V_T}{I_O R_2} S_{V_{CC}}^{I_I} = \frac{V_T}{V_{BE1}} S_{V_{CC}}^{I_I} \tag{7.132}$$

If $V_{CC} \gg V_{BE1} + V_{BE2}$ then V_{CC} is the approximate voltage across R_1 and

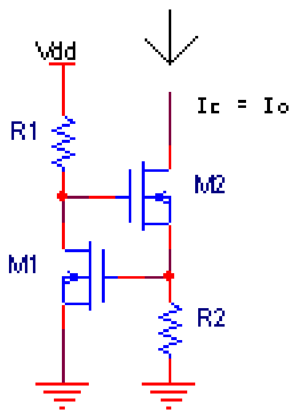
$$I_I \approx \frac{V_{CC}}{R_1} \tag{7.133}$$

so that $S_{V_{CC}}^{I_I}$ is approximately unity and thus

$$S_{V_{CC}}^{I_O} \approx \frac{V_T}{V_{BE1}} \tag{7.134}$$

For typical values of V_T and V_{BE1}, $S_{V_{CC}}^{I_O}$ is less than ten percent.

7.14 Threshold referenced current source



The threshold referenced current source is the MOS equivalent to the base-emitter referenced current source. The output current I_O is the current through R_2, which has a voltage V_{GS1} across it. Using (5.4) solved for V_{GS} we see that

$$I_O = \frac{V_{GS1}}{R_2} = \frac{V_t + \sqrt{\frac{2I_I}{k'(W/L)_1}}}{R_2} \tag{7.135}$$

Differentiating (7.135) with respect to the supply voltage V_{DD} gives the sensitivity I_O to V_{DD}:

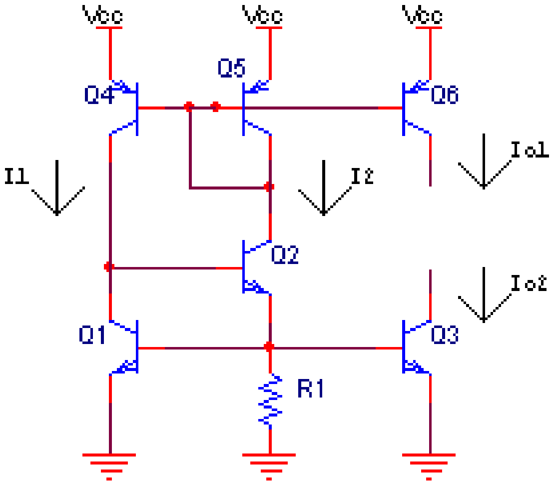
$$S_{V_{DD}}^{I_O} = \frac{V_{ov1}}{2I_O R_2} S_{V_{DD}}^{I_I} \tag{7.136}$$

V_{ov1} is the overdrive voltage above V_t. If $V_{DD} \gg V_{GS1} + V_{GS2}$ then the voltage across R_1 is approximately V_{DD} and $S_{V_{DD}}^{I_I}$ is approximately unity. Thus,

$$S_{V_{DD}}^{I_O} = \frac{V_{ov1}}{2I_O R_2} \tag{7.137}$$

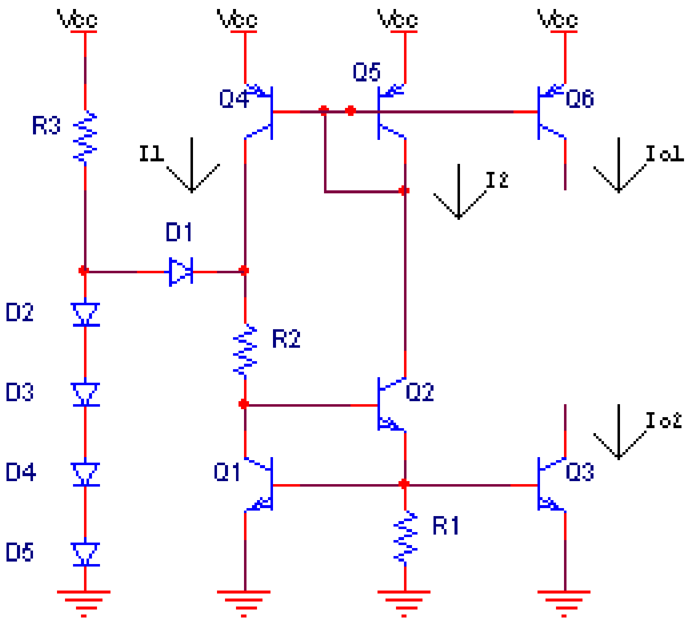
For typical values of V_{ov1} and V_{GS1}, $S_{V_{DD}}^{I_O}$ is less than ten percent.

7.15 Self-biasing V_{BE} reference



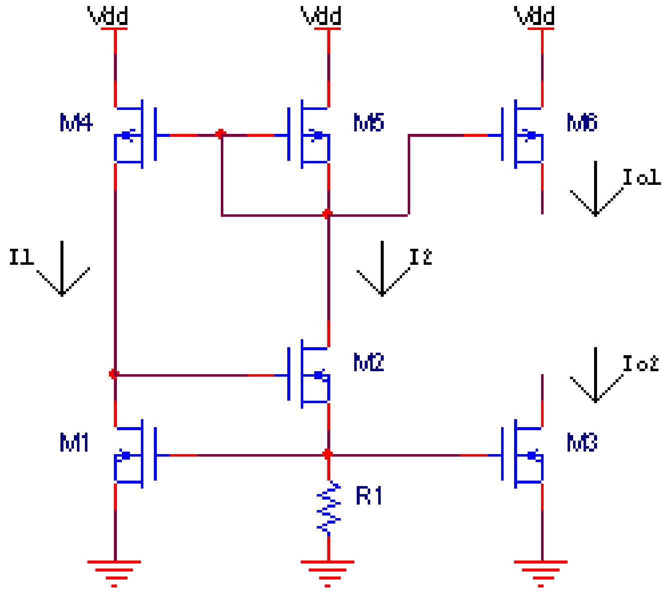
(Gray et al., *Analysis and Design of Analog Integrated Circuits*, p. 311)

7.15.1 Self-biasing V_{BE} reference with startup circuit



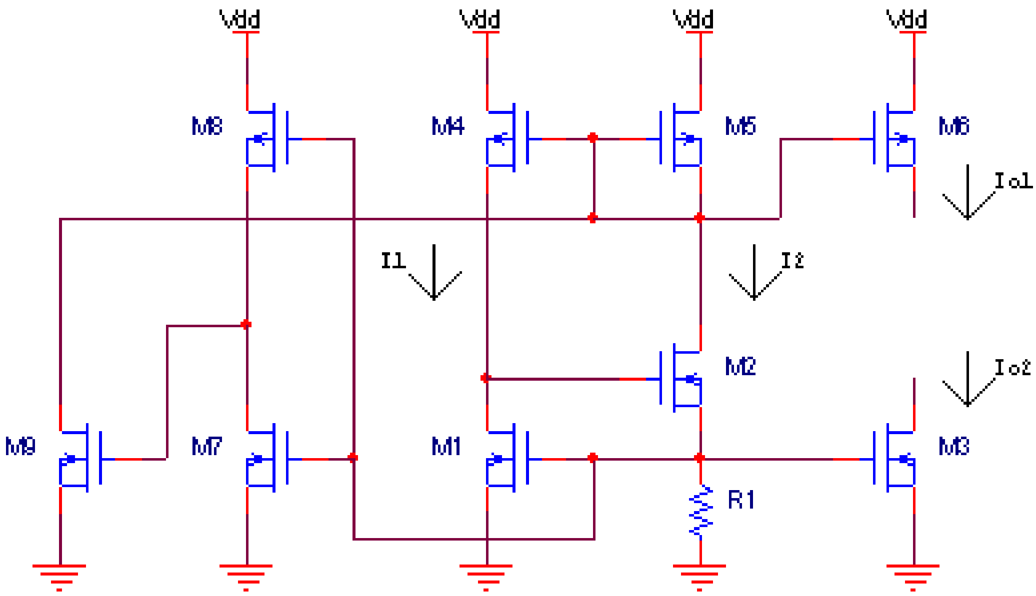
(ibid., p. 312)

7.16 Self-biasing V_t reference



(ibid., p. 311)

7.16.1 Self-biasing V_t reference with startup circuit



(ibid., p. 312)

Chapter 8

Output Stage and Power Amplifiers

Output stage and power amplifiers must be capable of processing some of the highest voltages and currents of a circuit design. A common use for output stage amplifiers is to amplify the power of a voltage signal representing a sound. In this application, pre-amplifiers operate on very small input signals (such as from a microphone), summing amplifiers mix the input signals, and the output stage amplifier processes the mixed input signals and drive a speaker.

To reduce power consumption and the circuit's supply voltage without lowering the maximum output voltage swing, these amplifiers usually require an output voltage swing that is nearly rail-to-rail, is rail-to-rail, or in some cases is greater than rail-to-rail. This requirement, along with the relatively high voltages and currents processed by these circuits, often results in loss of linearity as the output stage transistors operate on signals that are too large for typical small signal assumptions to remain valid. Many output stage and power amplifiers must thus also be designed to minimize these nonlinearities caused by large signals since nonlinearities cause harmonic distortions and other undesirable behaviors. In the case of audio signals, nonlinearities produce audible and very undesirable distortions which significantly reduce the quality of the audio signal.

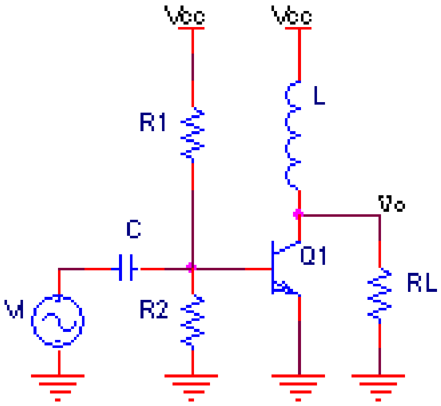
Another consideration for output stage and power amplifiers is that output stage/power transistors must be designed differently from the transistors that process smaller signals (such as the transistors in pre-amplifiers) in order to ensure that the signals processed by the output stage or power amplifier remain in all the transistors' safe operating area (SOA). Unfortunately, increasing the SOA for output stage/power transistors reduces their performance in other areas – such as the unity gain frequency (f_T) or, in the case of bipolar transistors, current gain (β).

With all these design challenges, output stage and power amplifiers are divided into classes based on the percent of time the output stage/power transistors are conducting (the amplifier's power efficiency). These classifications include class A, B, AB, C, D, E, F, G, and H amplifiers. The transistors in a class A amplifier conduct for the entire cycle of a sine wave input signal and so are the least power efficient. A simple example of a class A amplifier is the common emitter. Transistors in class B amplifiers conduct for half the cycle of a sine wave, and transistors in a class AB amplifier are biased at a low quiescent current and conduct for slightly more than half a cycle. (Neamen, *Microelectronics: Circuit Analysis and Design*, pp. 574–575)

Although output stage amplifiers and power amplifiers often share similar designs, there is an important distinction: power amplifiers are designed to maximize the power $P_L = V_L I_L$ delivered to a load while output stage amplifiers are designed to maximize voltage swing and minimize output impedance. The applications for each type of amplifier differs slightly, too; power amplifiers are used to drive speakers or an antenna – to transmit a Radio Frequency (RF) signal, for example – while an output stage amplifier is used for applications such as the output stage of op amps.

8.1 Class A Amplifiers

8.1.1 Inductively coupled class A amplifier



This is a common emitter circuit with an inductor in place of the collector resistor. The inductor should be chosen such that

$$\omega L \gg R_L \tag{8.1}$$

for all signal frequencies ω. If this is true then the inductor is a short circuit to DC and all frequencies below those of interest, and an open circuit to the frequencies of interest. Since there is no emitter resistor

$$I_C = \frac{V_{CE}}{R_L} = \frac{V_{CC}}{R_L} \tag{8.2}$$

The latter equation holds true since L is a short at DC. I_C is the maximum signal current because

$$i_c = \frac{-v_{ce}}{R_L} \leq \frac{-V_{CC}}{R_L} \tag{8.3}$$

since the impedance of L increases with frequency (and thus v_{CE} is maximized at DC). The maximum possible average signal power delivered to R_L is

$$\overline{P_L} = \frac{1}{2} I_C^2 R_L = \frac{1}{2} \frac{V_{CC}^2}{R_L} \tag{8.4}$$

Ignoring the power dissipated by the bias resistors R_1 and R_2, the average power dissipated by the amplifier is

$$\overline{P_D} = I_C V_{CC} = \frac{V_{CC}}{R_L} \tag{8.5}$$

The (theoretical) maximum possible power conversion efficiency is thus (ibid., pp. 588–589)

$$\eta = \frac{\overline{P_L}}{\overline{P_D}} = \frac{\frac{1}{2}\frac{V_{CC}^2}{R_L}}{\frac{V_{CC}^2}{R_L}} = \frac{1}{2} \tag{8.6}$$

If the inductor is instead a resistor and the transistor biased so that $V_{CE} = \frac{V_{CC}}{2}$ (to maximize the possible signal swing in both positive and negative directions), then for a sinusoidal signal

$$i_C = I_C + i_i \sin \omega t \tag{8.7}$$

and

$$v_C = \frac{V_{CC}}{2} - v_i \sin \omega t \tag{8.8}$$

where i_i and v_i are the input current and voltage, respectively. Thus, the maximum

$$i_{C(\max)} = I_C \tag{8.9}$$

and

$$v_{C(\max)} = \frac{V_{CC}}{2} \tag{8.10}$$

so

$$\overline{P_L} = \frac{1}{2} I_C \frac{V_{CC}}{2} = \frac{I_C V_{CC}}{4} \tag{8.11}$$

As before

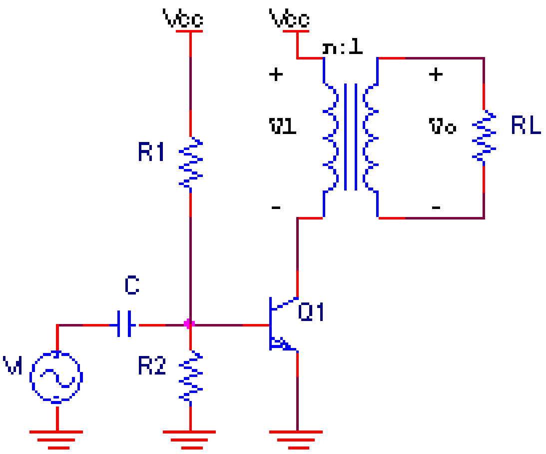
$$\overline{P_D} = I_C V_{CC} \tag{8.12}$$

so the maximum possible power conversion efficiency is only (Neamen, *Microelectronics: Circuit Analysis and Design*, pp. 575–576)

$$\eta = \frac{\overline{P_L}}{\overline{P_D}} = \frac{\frac{1}{4} I_C V_{CC}}{I_C V_{CC}} = \frac{1}{4} \tag{8.13}$$

The inductively coupled class A amplifier is thus considerably more power efficient than a simple common emitter.

8.1.2 Transformer-coupled class A amplifier



The inductively coupled class A amplifier design depends in part on the load resistance R_L, so it may be difficult to acheive a power conversion efficiency near the theoretical maximum of 50 %. The load resistance seen by the amplifier can be optimized by using a transformer with a specific turns ratio. For a turns ratio of $n:1$ the current i_L through the load resistance R_L is related to the collector current i_C by

$$i_L = n i_C \tag{8.14}$$

Similarly, the voltage v_O across the load is related to the voltage from V_{CC} to the voltage at the transistor's collector (v_1 in the schematic) by

$$v_O = nv_1 \tag{8.15}$$

By definition

$$R_L = \frac{v_O}{i_L} \tag{8.16}$$

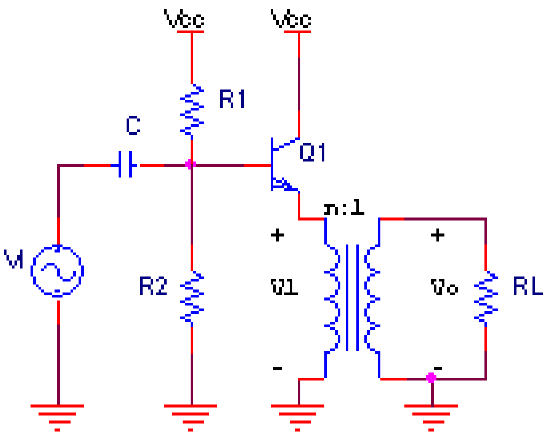
so the transformed load resistance (that is, the resistance seen by the transistor) is

$$R_L' = n^2 R_L \tag{8.17}$$

By choosing an appropriate R_L' using the transformer's turns ratio the same analysis can be applied to the transformer-coupled amplifier as the inductively coupled amplifier to achieve a (theoretical) maximum power conversion efficiency (ibid., pp. 589–590)

$$\eta = \frac{1}{2} \tag{8.18}$$

8.1.3 Transformer-coupled emitter follower amplifier



The transformer-coupled emitter follower does not provide a voltage gain like most amplifiers do, but its low output impedance makes it a useful final stage for many amplifiers. As with the preceding circuit, the transformer alters the load resistance seen by the transistor to

$$R_L' = n^2 R_L \tag{8.19}$$

Since the emitter follower has a voltage gain

$$\frac{v_o}{v_i} \approx 1 \tag{8.20}$$

and the maximum output voltage is

$$v_O = \frac{v_1}{n} = \frac{V_{CC}}{n} \tag{8.21}$$

(since the emitter voltage can go no higher than V_{CC} and $v_O = \frac{v_1}{n}$) the average power delivered to the load is simply

$$\overline{P_L} = \frac{1}{2}\frac{V_{CC}^2/2}{n^2 R_L} \tag{8.22}$$

The average power dissipated is

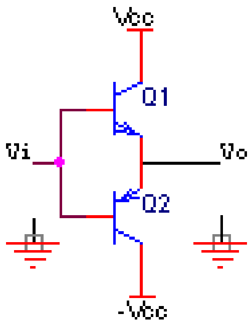
$$\overline{P_D} = \frac{V_{CC}^2/2}{n^2 R_L} \tag{8.23}$$

so (Neamen, *Microelectronics: Circuit Analysis and Design*, p. 591)

$$\eta = \frac{\overline{P_L}}{\overline{P_D}} = \frac{1}{2} \tag{8.24}$$

8.2 Class B Amplifiers

8.2.1 Class B bipolar push-pull output stage



This class B amplifier is a *complementary* output stage because it uses both *npn* and *pnp* transistors. Class B output stages such as these are typically implemented in integrated circuits only since the two transistors must be well matched for optimal behavior. Class A output stages dissipate significant power even when there is no input signal (since the single transistor in the class A output stage as always on), but class B output stages have very low power dissipation with no input signal because each of the two transistors is only on for about half the signal cycle and neither is on when there is no input signal.

There are three distinct regions of the transfer characteristic for this class B output stage. The first is for $|v_i| < v_{BE(on)}$ (assuming the transistors are matched so that they have the same $v_{BE(on)}$). In this case neither transistor is on so

$$v_o = 0,\ |v_i| < v_{BE(\text{on})} \tag{8.25}$$

The second region is for $v_{BE(\text{on})} < |v_i| < V_{CC} + v_{BE(\text{on})} - v_{CE(\text{sat})}$ (where $v_{CE(\text{sat})}$ is the value of v_{CE} above which the transistor enters the saturation region). If v_i satisfies this condition and is positive then Q_1 is active and Q_2 is off; if v_i is negative then Q_2 is active and Q_1 is off. The active transistor acts as an emitter follower since its collector is at AC ground and the output is taken from its emitter. Thus,

$$v_o = v_i,\ v_{BE(\text{on})} < |v_i| < V_{CC} + v_{BE(\text{on})} - v_{CE(\text{sat})} \tag{8.26}$$

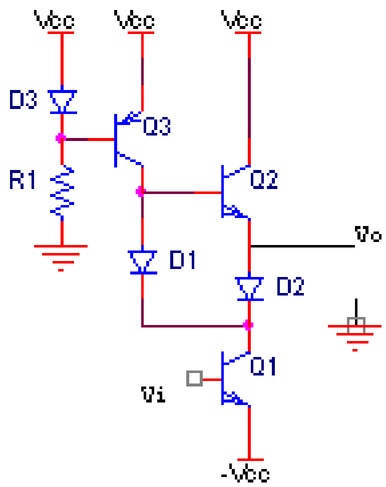
in this region. The third region is caused by the saturation of the active transistor. In this region the output does not change with the input:

$$v_o = V_{CC} - v_{CE1(\text{sat})},\ v_i > V_{CC} + v_{BE1(on)} - v_{CE1(sat)} \tag{8.27}$$

$$v_o = -V_{CC} + v_{CE2(\text{sat})},\ v_i = -V_{CC} + v_{BE2} - v_{CE2(\text{sat})} \tag{8.28}$$

The class B output stage unfortunately suffers from two types of distortion: clipping and crossover distortion. Clipping obviously occurs when the input signal has too high an amplitude for the output stage. To avoid clipping, the supply voltage of the circuit must be increased or the input signal must have a low enough amplitude that the transistors do not enter the saturation region. Unfortunately, the input signal cannot have too low an amplitude, either: crossover distortion is the result of the fact that $v_o = 0$ for $|v_i| < v_{BE(on)}$. With neither transistor active in this region (sometimes called the deadband), the output does not follow the input. The only way to minimize the effect of crossover distortion is to ampilify the input signal sufficiently so that the deadband is only a small percentage of the input signal's amplitude, or to use a class AB output stage. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 362–364)

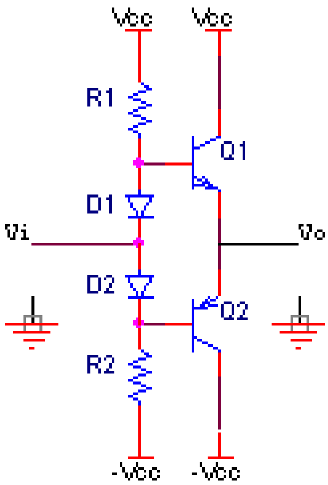
8.2.2 Class B *npn* bipolar output stage (GHLM p. 376)



This class B output stage, like the previous class AB output stage with Darlington pairs, takes into account the fact that *pnp* transistors perform poorly compared to *npn* transistors because IC process technologies usually optimize the *npn* transistors at the expense of the *pnp* transistors. This circuit is designed for higher power applications (several watts of output power or more) because the *pnp* transistors are incapable of carrying higher currents.

8.3 Class AB Amplifiers

8.3.1 Class AB bipolar output stage



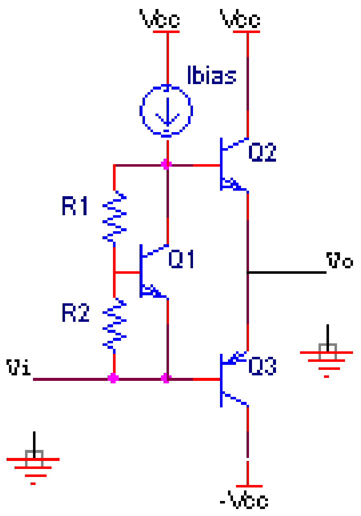
This class AB output stage eliminates the deadband (and the resulting crossover distortion) by adding two diodes and two resistors to the class B push-pull output stage. The resistors bias the two diodes on, which forces a voltage drop across each diode (nearly all of the current through the resistors flows through the diodes since I_B is a factor of β_F smaller than the bias current). The voltage drop across each diode creates a nonzero V_{BE} so that $|v_i|$ no longer needs to overcome the transistors' $v_{BE(\text{on})}$ – one of the transistors becomes active as soon as $v_i \neq 0$. (Gray et al., *Analysis and Design of Analog Integrated Circuits*, p. 365) Other than correcting for the deadband region, the operation of the class AB output stage is nearly the same as that of the class B output stage:

$$v_o = v_i,\ |v_i| < V_{CC} + v_{BE(\text{on})} - v_{CE(\text{sat})} \tag{8.29}$$

$$v_o = V_{CC} - v_{CE1(\text{sat})},\ v_i > V_{CC} + v_{BE1(\text{on})} - v_{CE1(\text{sat})} \tag{8.30}$$

$$v_o = -V_{CC} + v_{CE2(\text{sat})},\ v_i = -V_{CC} + v_{BE2} - v_{CE2(\text{sat})} \tag{8.31}$$

8.3.2 Class AB output stage with V_{BE} multiplier



An alternate class AB output stage replaces the two diodes with a V_{BE} multiplier. From (6.19)

$$V_{CE1} = V_{BE1}\left(1 + \frac{R_1}{R_2}\right) \tag{8.32}$$

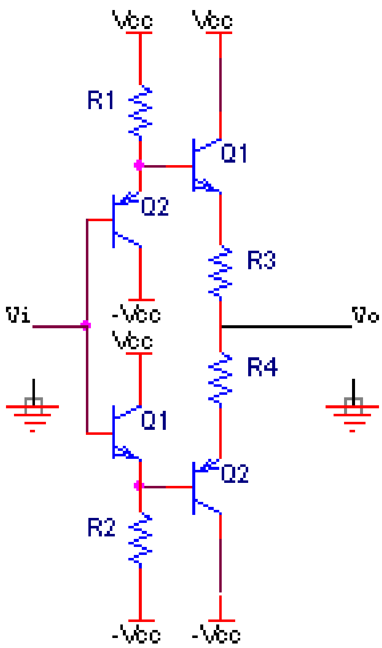
and

$$I_{\text{BIAS}} = I_R + I_{C1} \tag{8.33}$$

where I_R is the current through the resistors R_1 and R_2. I_{BIAS} can be any current source implementation, such as a current mirror.

This biasing scheme is considerably more flexible than the two diode scheme since any bias voltage can be set using only the ratio of R_1 and R_2 and an appropriate I_{BIAS}.

8.3.3 Class AB output stage with input buffer transistors



In this circuit the components between the output transistors' bases is again replaced (and R_3 and R_4 have been added for temperature stability). Q_1 and Q_2 are simply emitter followers and R_1 and R_2 determine the bias current. If $V_I = V_O = 0$ and assuming $V_{EB1} \approx V_{BE2} \approx 0.6V$ (typical values in the forward active region), the voltage across R_1 and R_2 is $V_{CC} - V_{EB1}$ and $V_{CC} - V_{BE2}$, respectively. The desired bias currents, neglecting the small I_{B3} and I_{B4}, are therefore

$$I_{E1} \approx \frac{V_{CC} - V_{EB1}}{R_1} \tag{8.34}$$

$$I_{E2} \approx \frac{V_{CC} - V_{BE2}}{R_2} \tag{8.35}$$

Since all the transistors are configured as emitter followers, the voltage gain of this output stage, like the preceding circuits, is approximately unity. The current gain, however, is substantial. To find the approximate current gain, note that

$$i_i = i_{b2} - i_{b1} \tag{8.36}$$

and (neglecting the voltage drops across R_3 and R_4)

$$i_{b1} \approx \frac{V_{CC} - (v_i + v_{eb})}{(1+\beta)R_1} \tag{8.37}$$

and

$$i_{b2} \approx \frac{(v_i - v_{be}) - V_{CC}}{(1+\beta)R_2} \tag{8.38}$$

so that

$$i_i \approx \frac{2v_i}{(1+\beta)R},\ R = R_3 = R_4 \tag{8.39}$$

Invoking the fact that

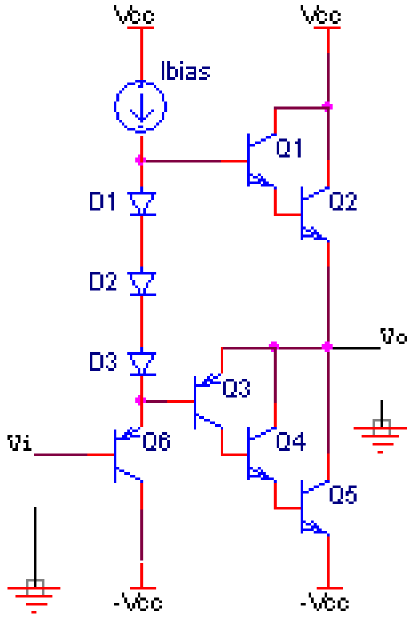
$$i_o = \frac{v_o}{R_L} \approx \frac{v_i}{R_L} \tag{8.40}$$

the current gain is

$$\frac{i_o}{i_i} \approx \frac{(1+\beta)R}{2R_L} \tag{8.41}$$

β_F is usually large, so the current gain (and thus the power gain) is usually significant. (Neamen, *Microelectronics: Circuit Analysis and Design*, pp. 598–599)

8.3.4 Class AB output stage with Darlington pairs



This class AB output stage takes into account the fact that, in IC process technologies, *pnp* transistors typically have a much lower β_F than *npn* transistors. Assuming individual *npn* and *pnp* transistors have current gains of β_n and β_p, respectively, the composite transistor formed by Q_1 and Q_2 has an effective current gain of approximately $\beta_n\beta_n$ and the composite transistor formed by Q_3, Q_4, and Q_5 has an effective current gain of approximately $\beta_p\beta_n\beta_n$. Since $\beta_n >> \beta_p$ the effective current gains of the composite transistors are approximately equal. (ibid., pp. 601–602)

Q_6 is configured as an emitter follower, and the three diodes reduce the deadband by matching the three V_{BE} drops from Q_1, Q_2, and Q_3. Since all the transistors are configured as emitter followers, the transfer function is approximately the same as that of the simple class AB output stage.

Chapter 9

Charge Pumps

Charge pumps are used for power conversion, similar to buck and boost converters. The difference between converters and charge pumps is that the latter store energy using capacitors while the former store energy in inductors. This means charge pumps are generally much smaller (inductors usually dominate the size of converters) and can be integrated. Converters have good performance over a wide range of input voltages while charge pumps are limited to a much narrower range. Consequently, converters are usually used for discrete circuits while charge pumps are typically integrated. On the other hand, they are typically simpler than converters and so they may be more suitable for simpler discete designs.

Like a boost converter, a charge pump can be used to generate a voltage that is higher than its input voltage (often the supply voltage). It can also be used to generate a negative voltage. Since power must be conserved, of course, the output current is always less than the input current. Charge pumps are typically used in ICs to generate voltages above the positive supply voltage or below the negative supply voltage (or GND). Charge pumps are also useful for generating programming voltages for non-volatile memories (such as EEPROM).

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