
STM32
CubeMX

1. Description

1.1. Project

Project Name	stm32_h7_adc_test
Board Name	custom
Generated with:	STM32CubeMX 6.0.0
Date	02/10/2021

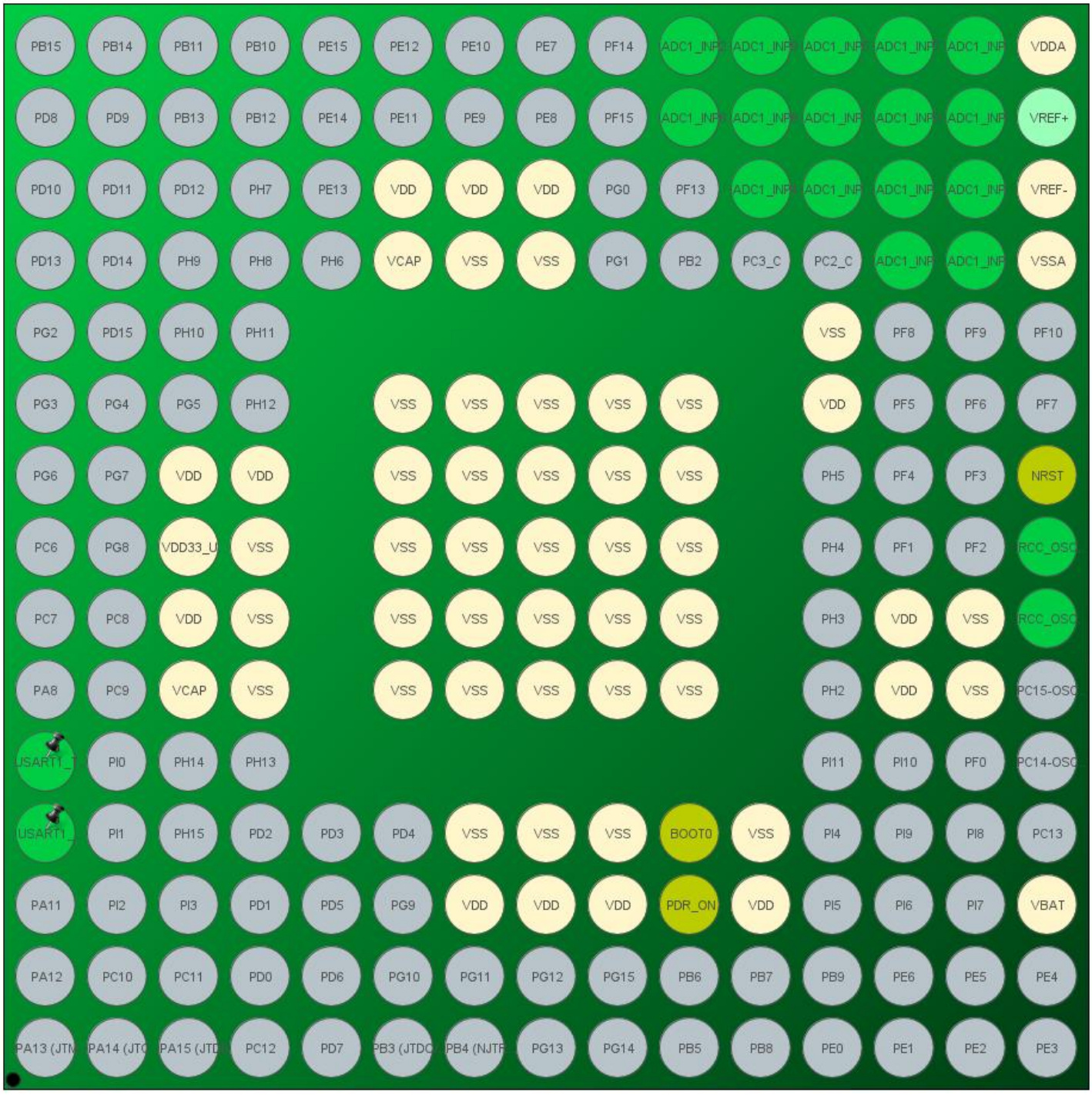
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743IIKx
MCU Package	UFBGA176
MCU Pin number	201

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



UFBGA176 +25 (Bottom view - Rotated +180°)

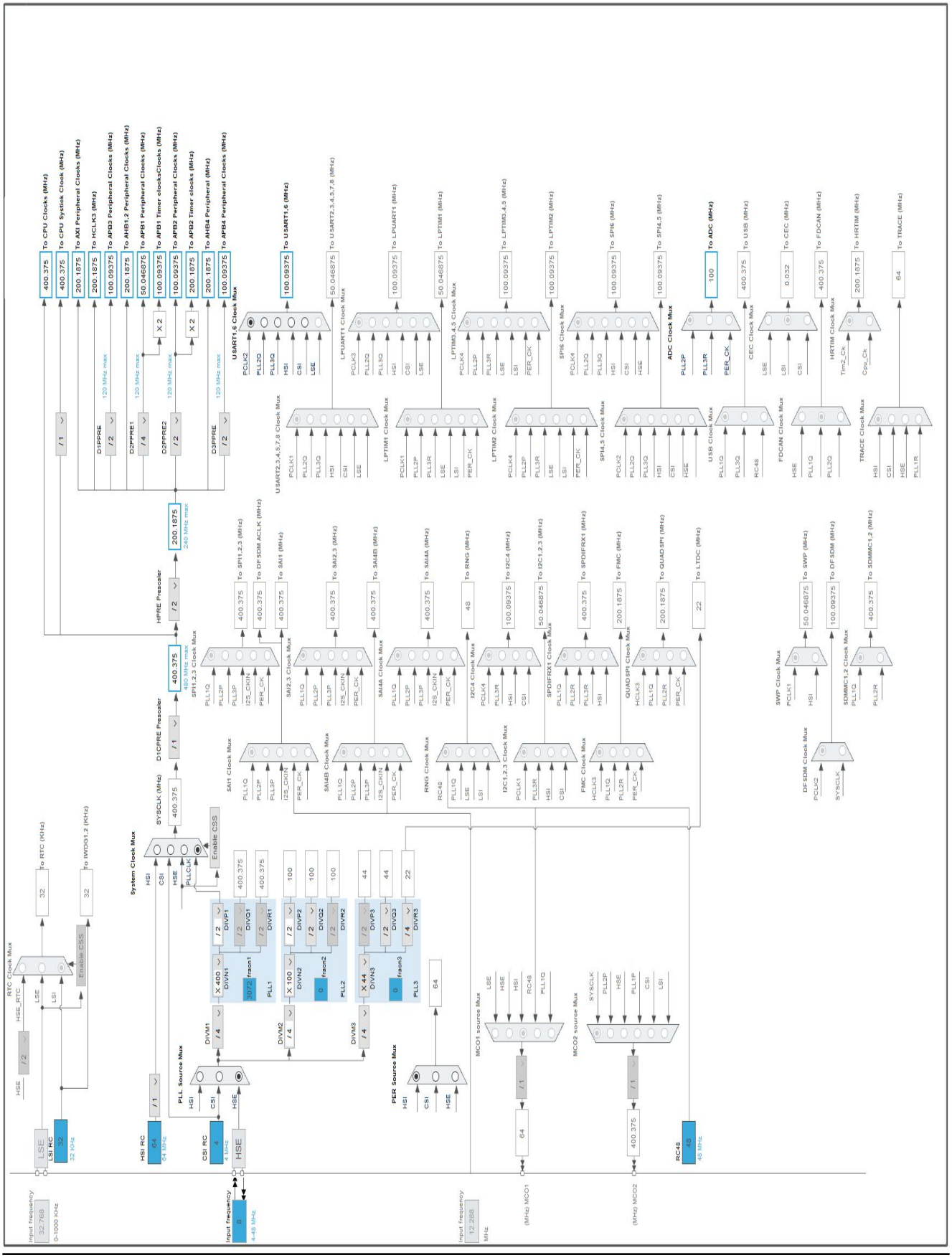
3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
C1	VBAT	Power		
C5	VDD	Power		
C6	PDR_ON	Reset		
C7	VDD	Power		
C8	VDD	Power		
C9	VDD	Power		
D5	VSS	Power		
D6	BOOT0	Boot		
D7	VSS	Power		
D8	VSS	Power		
D9	VSS	Power		
D15	PA10	I/O	USART1_RX	
E15	PA9	I/O	USART1_TX	
F2	VSS	Power		
F3	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VCAP	Power		
G1	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
G2	VSS	Power		
G3	VDD	Power		
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G12	VSS	Power		
G13	VDD	Power		
H1	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H9	VSS	Power		
H10	VSS	Power		
H12	VSS	Power		
H13	VDD33_USB	Power		
J1	NRST	Reset		
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J12	VDD	Power		
J13	VDD	Power		
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
L4	VSS	Power		
M1	VSSA	Power		
M2	PC0	I/O	ADC1_INP10	
M3	PC1	I/O	ADC1_INP11	
M8	VSS	Power		
M9	VSS	Power		
M10	VCAP	Power		
N1	VREF-	Power		
N2	PA1	I/O	ADC1_INP17	
N3	PA0	I/O	ADC1_INP16	
N4	PA4	I/O	ADC1_INP18	
N5	PC4	I/O	ADC1_INP4	
N8	VDD	Power		
N9	VDD	Power		
N10	VDD	Power		
P2	PA2	I/O	ADC1_INP14	
P3	PA6	I/O	ADC1_INP3	
P4	PA5	I/O	ADC1_INP19	
P5	PC5	I/O	ADC1_INP8	
P6	PF12	I/O	ADC1_INP6	
R1	VDDA	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R2	PA3	I/O	ADC1_INP15	
R3	PA7	I/O	ADC1_INP7	
R4	PB1	I/O	ADC1_INP5	
R5	PB0	I/O	ADC1_INP9	
R6	PF11	I/O	ADC1_INP2	

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm32_h7_adc_test
Project Folder	E:\Users\yc253\STM32CubeIDE\workspace_1.4.0\stm32_h7_adc_test
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.8.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_USART1_UART_Init	USART1
5	MX_ADC1_Init	ADC1
0	MX_CORTEX_M7_Init	CORTEX_M7

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743IIKx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

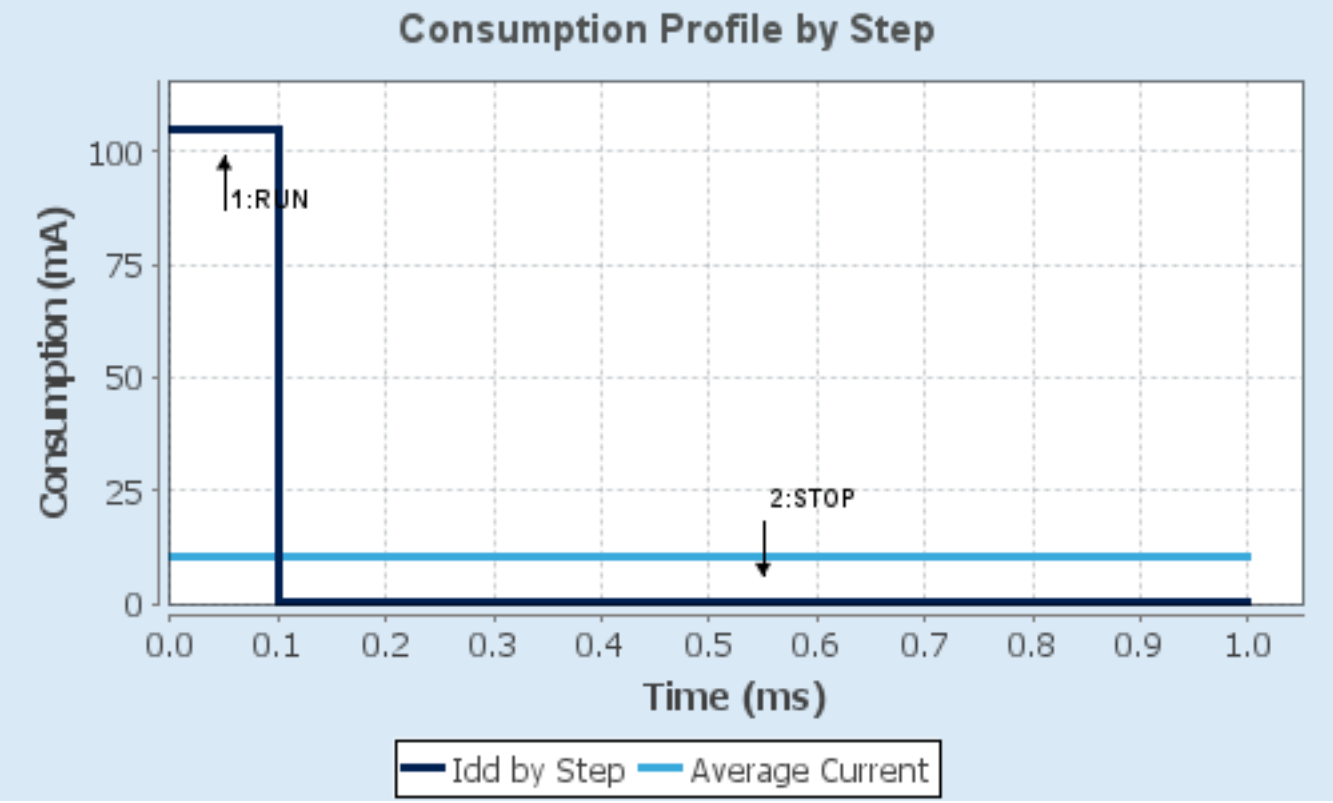
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS1: Scale1-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DSTANDBY	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	FLASH_A	NA
CPU Frequency	400 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON Cache-ON	Flash-LP
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	105 mA	170 µA
Duration	0.1 ms	0.9 ms
DMIPS	856.0	0.0
Ta Max	113.03	124.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	10.65 mA
Battery Life	2 days, 10 hours	Average DMIPS	856.00006 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

mode: IN6

mode: IN7

mode: IN8

mode: IN9

IN10: IN10 Single-ended

mode: IN11

mode: IN14

mode: IN15

IN16: IN16 Single-ended

mode: IN17

IN18: Single-ended

mode: IN19

7.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	**ADC 10-bit resolution ***
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**16 ***

External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 2
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 3 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**3 ***
Channel	**Channel 4 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**4 ***
Channel	**Channel 5 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**5 ***
Channel	**Channel 6 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**6 ***
Channel	**Channel 7 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**7 ***
Channel	**Channel 8 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**8 ***
Channel	**Channel 9 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**9 ***
Channel	**Channel 10 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset

Rank	**10 ***
Channel	**Channel 11 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**11 ***
Channel	**Channel 14 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**12 ***
Channel	**Channel 15 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**13 ***
Channel	**Channel 16 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**14 ***
Channel	**Channel 17 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**15 ***
Channel	**Channel 18 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset
Rank	**16 ***
Channel	**Channel 19 ***
Sampling Time	**810.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. GPIO

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY
RCC Parameters:	
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32
System Parameters:	
VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Power Parameters:	
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0
PLL range Parameters:	
PLL1 clock Input range	Between 2 and 4 MHz
PLL2 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

7.4. SYS

Timebase Source: SysTick

7.5. USART1

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:	
Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1
Advanced Parameters:	

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_INP10	Analog mode	No pull-up and no pull-down	n/a	
	PC1	ADC1_INP11	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_INP17	Analog mode	No pull-up and no pull-down	n/a	
	PA0	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_INP14	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_INP19	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_INP8	Analog mode	No pull-up and no pull-down	n/a	
	PF12	ADC1_INP6	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_INP15	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_INP7	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	
	PF11	ADC1_INP2	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Stream0	Peripheral To Memory	Low

ADC1: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
USART1 global interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		

8.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
DMA1 stream0 global interrupt	true	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

9.1.2. Without filters

9.2. Power Domain view

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00387108.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00314099.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00368411.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337873.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00356635.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00609692.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00600614.pdf
Application note	http://www.st.com/resource/en/application_note/DM00628458.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf