VTC Inc.
Value the Customer™

VM71110

4, 6, 8 OR 10-CHANNEL, 5-VOLT, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

August, 1994

FEATURES

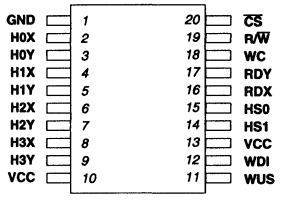
- High Performance
  - Read Gain = 200 300 V/V
  - Input Noise = 0.5nV/√Hz Typical
  - Head Inductance Range = 0.4 – 5 µH
  - Write Current Range 1 - 40 mA
  - Input Capacitance = 13 pF Typical
- Very Low Power Dissipation = 3 mW Typical in Sleep Mode
- Power Up/Down Data Protect Circuitry
- Reduced Write-to-Read Recovery Time
- Single Power Supply = 5 V ± 10%
- Fault Detect Capability
- Designed for 2-Terminal Thin-Film or MIG Heads

DESCRIPTION

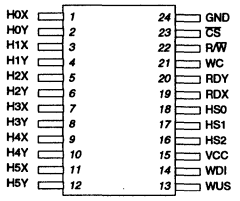
The VM71110 is a high-performance, very low-power read/write preamplifier designed for use with external 2-terminal, thin-film or MIG recording heads. This circuit operates on a single 5-volt power supply.

The VM71110 provides write current switching in the write mode and provides a low noise data path in the read mode for up to ten read/write recording heads. When deactivated, the device enters a ***sleep mode*** which reduces power dissipation to 3 mW. Data protection circuitry is provided to ensure that the write current source is totally disabled during power supply power up/power down conditions. Write-to-read recovery time is minimized by eliminating common mode output voltage swings when switching between modes.

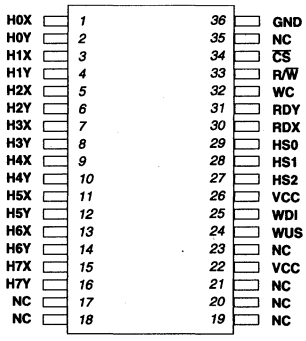
CONNECTION DIAGRAM



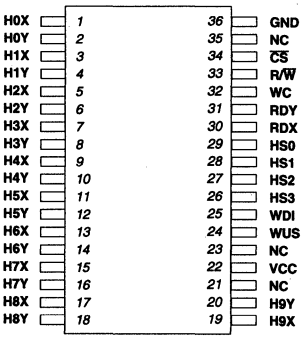
VM7114
4-Channel
20-lead SOIC, SSOP, VSOP



VM7116
6-Channel
24-lead SSOP

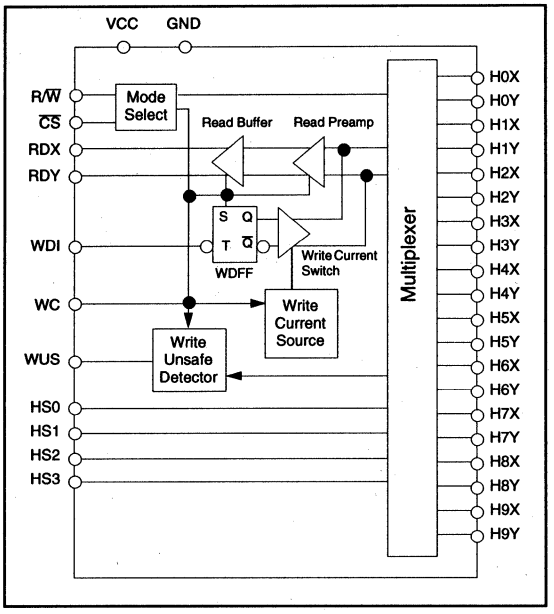


VM7118
8-Channel
36-lead SOIC



VM71110
10-Channel
36-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{CC} ..... -0.3V to +7V

Write Current I_W 60mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} ..... -0.3V to +6V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature ..... 150°C

Storage Temperature T_{stg} ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 20-lead SOIC ..... 90°C/W
- 20-lead SSOP ..... 110°C/W
- 20-lead VSOP ..... 120°C/W
- 24-lead SSOP ..... 100°C/W
- 36-lead SOIC ..... 80°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- V_{CC} .....+5V ± 10%

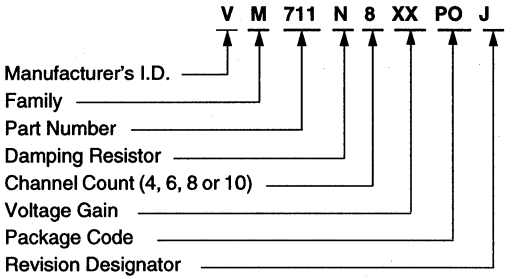
Write Current (I_W) ..... 1 to 40mA

Head Inductance (L_H) ..... 0.4 to 10µH

Junction Temperature (T_J) ..... 25°C to 125°C

ORDERING INFORMATION

The VM71110 is available with a wide variety of possible options that allow the device to closely fit different applications. In order to simplify the task of defining the various possible options, ordering information is included here. Please note, not all possible combinations of options may actually have been built. Please consult the factory with any questions.



DAMPING RESISTOR
- Blank = Schottky Diode Connected Damping Resistor
- N = No Internal Damping Resistor

VOLTAGE GAIN
- 20 = 200 Voltage Gain

PACKAGE CODES
- PO = Small Outline Integrated Circuit (SOIC)
- SS = Shrink Small Outline Package (SSOP)
- VS = Very Small Outline Package (VSOP)

CIRCUIT OPERATION

The VM71110 addresses up to ten 2-terminal, thin-film recording heads, providing switched write current in the write mode, or data amplification in the read mode. Head selection and mode control is determined by the head select line, HS1 and mode control lines, $\overline{CS}$, R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups, provided on the $\overline{CS}$ and R/$\overline{W}$ lines, will force the device into a non-write condition if either control line opens up. The part's operation over a wide range of inductive loads makes it suitable for 2-terminal MIG heads.

Write Mode

In write mode, the VM71110 acts as a write current switch with the write unsafe (WUS) detection circuitry activated. Write current is toggled between the X and Y side of the selected head on each high to low transition on the write data flip-flop (WDFF) so that upon switching to the write mode, the write current flows into the "X" side of the head.

The write current magnitude is determined by an external resistor (RWC) connected between the WC pin and ground. An internally generated reference voltage is present at the WC pin. The magnitude of the Write Current (0-PK, ± 8%) is:

$$I_W = K_W/R_{WC} + 0.2mA$$
$$= 50/R_{WC} + 0.2mA$$

Power supply fault protection ensures data security on the disk by disabling the write current source during a power supply voltage fault or by supply power up/down conditions. Additionally,

the write unsafe (WUS) detection circuitry will flag any of the conditions listed below, as a high level on the WUS line. Two negative transitions on the WDI pin, after the fault is corrected, is required to clear the WUS line.

- No write current
- WDI frequency too low
- Read or sleep mode

Read Mode

In read mode, the VM71110 acts as a low noise differential amplifier for signals coming off the disk. The write current generator and write unsafe circuitry is deactivated. The RDX, RDY pins are emitter follower outputs and are in phase with "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode output voltage is constant, minimizing the transient between read and write mode, thereby, substantially reducing the recovery time in the pulse detector circuit connected to these outputs.

Sleep Mode

When $\overline{CS}$ is high, all circuitry is shut down so that power dissipation is reduced to 3 mW in the ***sleep mode***. Switching the $\overline{CS}$ line low *wakes up* the chip and the device will enter the read or write mode, depending on the status of the R/$\overline{W}$ line.

Input Structure:

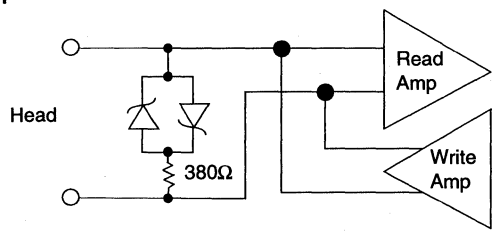


Table 1: Head Select

HS3	*HS2*	*HS1*	*HS0*	*HEAD*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
0	0	0	0	8
0	0	0	1	9

Table 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	*MODE*
0	0	Write/Awake
0	1	Read/Awake
1	X	Sleep

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS3	I*	Head Select: selects one of up to ten heads
H0X - H9X H0Y - H9Y	I/O	X,Y Head Terminals
WDI	I*	Write Data Input: TTL input signal, negative transition toggles direction of head current
$\overline{CS}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{W}$	I*	Read/Write Select: high level selects read mode, low-level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply**
GND		Ground

* May be wire-OR'ed for multi-chip usage.
** Although both VCC connections are recommended, only one connection is required as both are connected internally.

DC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Power Supply Current	I_{CC}	Read Mode		$40 + 0.05I_W$	$51 + 0.05I_W$	mA
		Write Mode		$31 + 1.05I_W$	$45 + 1.05I_W$	
		Idle Mode		0.6	3	
Power Dissipation	PD	Read Mode, $I_W = 20mA$		205	286	mW
		Write Mode, $I_W = 20mA$		320	402	
		Idle Mode		3	5.5	
Input High Voltage	V_{IH}		2		$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	$V_{IH} = 2.7V$			80	µA
Input Low Current	I_{IL}	$V_{IL} = 0.4V$	-160		-0.6	µA
WUS Output Low Voltage	V_{OL}	$I_{OL} = 4.0mA$		0.35	0.5	V
WUS Output High Current	I_{OH}	$V_{OH} = 5.0V$		13	100	µA
VCC Value for Write Current Turn Off		$I_H < 0.2mA$	3.7	4.0	4.3	V

Note 1: Typical values are given at $V_{CC} = 5V$ and $T_A = 25°C$.

READ CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, C_L (RDX, RDY) < 20pF, R_L (RDX, RDY) = 1kΩ.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, 1MHz	167	200	233	V/V
Bandwidth	BW	-1dB |Zs| < 5Ω, V_{IN} = 1mVp-p, gain = 150	30	40		MHz
		-3dB |Zs| < 5Ω, V_{IN} = 1mVp-p, gain = 150	65	75		
Input Noise Voltage	e_{in}	BW = 17MHz, L_H = 0, R_H = 0		0.55	0.7	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		13	16	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz	280	1000		Ω
Dynamic Range	DR	AC input where A_V is 90% of gain at 0.2mVrms input	2	9		mVrms
Common Mode Rejection Ratio	CMRR	V_{IN} = 100mVp-p @ 5MHz	50	63		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @ 5MHz on V_{CC}	45	66		dB
Channel Separation	CS	Unselected channel driven with 20mVp-p @ 5MHz	45	60		dB
Output Offset Voltage	V_{OS}		-300	50	+300	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode		V_{CC} - 2.7		VDC
Read to Write Common Mode Output Voltage Difference	ΔV_{OCM}		-350	-60	350	mV
Single-Ended Output Resistance	R_{SEO}			16	35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	±1.5			mA

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

WRITE CHARACTERISTICS Recommended operating conditions apply unless otherwise specified, L_H = 1µH, R_H = 30Ω, I_W = 20mA, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP (Note 1)*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
I_{WC} to Head Current Gain	A_I			20		mA/mA
Write Current Constant	K_W	$K_W = (V_{WC})(A_I)$	46	50	54	V
Write Current Range	I_W	$12.56 < R_{WC} < 62.5k\Omega$	5		40	mA
Write Current Tolerance	ΔI_W	I_W = 10 - 40mA	-8	-1	+8	%
Differential Head Voltage Swing	V_{DH}		4.5	5.4		Vp-p
WDI Transition Frequency for Safe Condition	f_{DATA}	WUS = low	1			MHz
Differential Output Capacitance	C_{OUT}				15	pF
Differential Output Resistance	R_{OUT}		2200			Ω
Unselected Head Current	I_{UH}			0.15	0.5	mA(pk)
RDX, RDY Common Mode Output Voltage	V_{CM}			V_{CC} - 2.7		V

Note 1: Typical values are given at V_{CC} = 5V and T_A = 25°C.

SWITCHING CHARACTERISTICS Recommended operating conditions apply unless otherwise specified; I_W = 20mA, f_{DATA} = 5MHz, L_H = 1µH, R_H = 30Ω, C_L (RDX, RDY) ≤ 20pF (see Figure 1).

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP* *(Note 1)*	*MAX*	*UNITS*
R/$\overline{W}$ Read to Write Delay	t_{RW}	R/$\overline{W}$ to 90% I_W		0.06	0.3	µs
R/$\overline{W}$ Write to Read Delay	t_{WR}	R/$\overline{W}$ to 90% of 100mV, 10 MHz read signal envelope		0.55	1	µs
$\overline{CS}$ Unselect to Select Delay	t_{IR}	$\overline{CS}$ to 90% I_W or 90% of 100mV, 10MHz read signal envelope		0.30	0.6	µs
$\overline{CS}$ Select to Unselect Delay	t_{RI}	$\overline{CS}$ to 10% of I_W		0.05	0.6	µs
HS0 - HS3 any Head Delay	t_{HS}	HS0 - HS3 to 90% of 100mV, 10MHz read signal envelope		0.03	0.6	µs
WUS Safe to Unsafe Delay	t_{D1}		0.6	2.3	3.6	µs
WUS Unsafe to Safe Delay	t_{D2}			0.4	1	µs
Head Current Propagation	t_{D3}	L_H = 0, R_H = 0, from 50% points		12	30	ns
Head Current Asymmetry	A_{SYM}	50% duty cycle on WDI, 1ns rise/fall time; L_H = 0, R_H = 0		0.03	0.5	ns
Head Current Rise/Fall Time	t_r/t_f	10% to 90% points, L_H = 0, R_H = 0		1.9	5	ns
		10% to 90% points, L_H = 1µH, R_H = 30Ω		12	16	

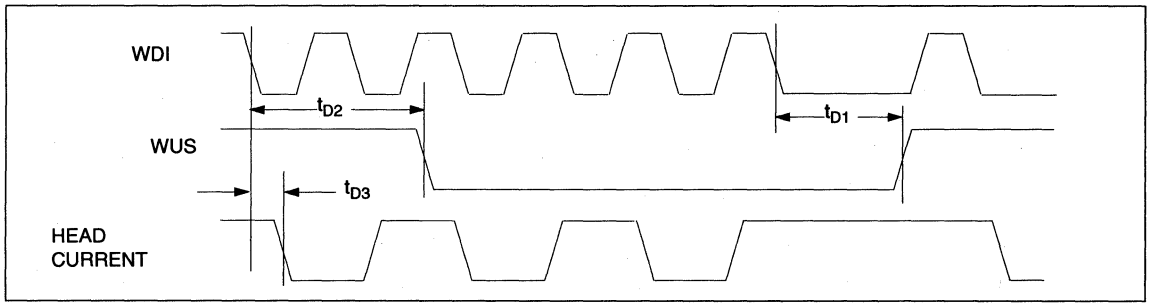


Figure 1: Write Mode Timing Diagram