



Five Frequently Asked Questions about System Level Transient Voltage Protection

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As semiconductor manufacturers introduce new wireline transmission devices built on smaller CMOS geometries, more circuit protection challenges are emerging. This article will explore some frequently asked questions regarding the basics of ESD and transient voltage suppression for board level circuit protection on dataline communication circuits.

1. “Do I really need a circuit protection device to protect my system from ESD?”

Years ago, you could probably get away without external protection devices, but today's systems are different. Systems have I/O interfaces, of course, and I/O interfaces are driven by advanced submicron semiconductor integrated circuits (ICs). So, the challenge is to protect the ICs connected to your system I/O interfaces from transient overstress. And, indeed, this is becoming a complex challenge as communications ICs get faster and more efficient, but also highly sensitive to electrical overstress (EOS). In the past, many engineers could rely on good layout technique and employing a range of “tricks” for EMC/ESD immunity (guard rails, ferrites, etc) to “harden” systems against ESD threats. This approach is rapidly becoming the exception, as the ICs employed into current generation and next generation systems are more vulnerable to ESD than at any other time within our industry. Nowadays, most tier 1 and tier 2 electronic equipment manufacturers recognize the tradeoffs, understand the value of time to market, and opt for using good low-clamping off-chip protection to safeguard their systems from electrical overstress. Sure, protecting system ports adds some cost to the BOM, but if you have ever experienced the agony and panic of debugging a system in the compliance phase while the market window is shrinking quickly, you'll likely conclude that the cost of insurance is more economical in the long run.

2. “The transceiver I have in my design is rated for 2kV ESD. Shouldn't this be sufficient?”

Probably not. In order to insure safe handling through the semiconductor manufacturing process, IC manufacturers typically design ESD protection structures at the I/O cells of their transceivers. This “on-chip” protection is to insure that manufacturing operators handling the die during assembly and test procedures do not render damage to a statistically high number of IC devices. Unfortunately, the 2kV your transceiver IC provides at the chip I/O cells is not a good metric for evaluating *system* level transient immunity, nor should it be relied upon for system level immunity. Several different ESD immunity standards are used in the electronics industry, each one describing appropriate immunity levels for the intended ESD environment. For chip level (*device level*) ESD, the standard generally used is the JESD22-A114E standard. This JEDEC human body model (HBM) standard is what your transceiver manufacturer designed according to in the development of their chip. This standard is intended to insure a minimum level of on-chip protection needed for safely handling ICs on the manufacturing floor.

In contrast, at the system level you should consider an altogether different standard, IEC61000-4-2. IEC61000-4-2 describes and models the ESD threat level encountered at the system environment, with fully packaged ICs operating in a complete electronic system. As you might expect, to model more 'real world' system ESD threats, the IEC standard is a more severe ESD immunity test. IEC calls for 4 contact test voltages for different threat levels: $\pm 2\text{kV}$, $\pm 4\text{kV}$, $\pm 6\text{kV}$, and $\pm 8\text{kV}$ with peak discharge currents as high as 30A

The JEDEC and IEC standards call for different peak pulse current levels as illustrated in the table below. While a 2kV ESD pulse according to JEDEC is probably sufficient ESD immunity threshold for a highly controlled manufacturing floor and insuring that an acceptable level of ICs migrate through the process unharmed, it represents an insufficient level of protection for the system environment and should not be used as a design guide to protect against system level ESD strikes.

IEC Level (contact discharge)	ESD Voltage (kV)	JEDEC JESD22-A114E Ipp (A)	IEC 61000-4-2 Ipp (A)
1	2	1.33	7.5
2	4	2.67	15.0
3	6	4.00	22.5
4	8	5.33	30.0

Table 1 – ESD Peak Pulse Current : JESD22-A114E vs. IEC61000-4-2

3. “If I want to design with ESD protection devices, what type of device should I be looking for?”

There are many devices on the market for transient voltage protection. There are many different technologies as well: polymer devices, multi-layered varistors (MLVs), transient voltage suppression diodes (TVS), gas discharge tubes (GDTs), zener diodes, and others. Each device technology presents advantages and tradeoffs. For mitigating electrical stress on low-voltage dataline communication circuits, Transient Voltage Suppression (TVS) diodes offer the most optimized balance between low clamping voltage and low capacitance. TVS diodes will respond to the transient faster than other protection technologies. As today's circuits are more delicate to EOS than previous chip design generations, a fast response time is critical.

It is important that we define clamping voltage. Clamping voltage is the voltage that will be seen by the IC after the protection circuit has engaged the transient and clamped the voltage. You can think of this as

how well a protection device can “knock down” a transient voltage spike on a dataline. The TVS device operates as a shunt element on the dataline. When a transient spike presents on the line, the TVS diode junction breaks down in a sub-nanosecond response time to shunt the transient current away from the protected IC and clamp the transient voltage. In Figure 1, you can see a conceptual example of ESD voltage, in this case, being clamped to a low voltage threshold. What becomes apparent from the diagram, is that lower clamping voltage can be related to a higher level of protection.

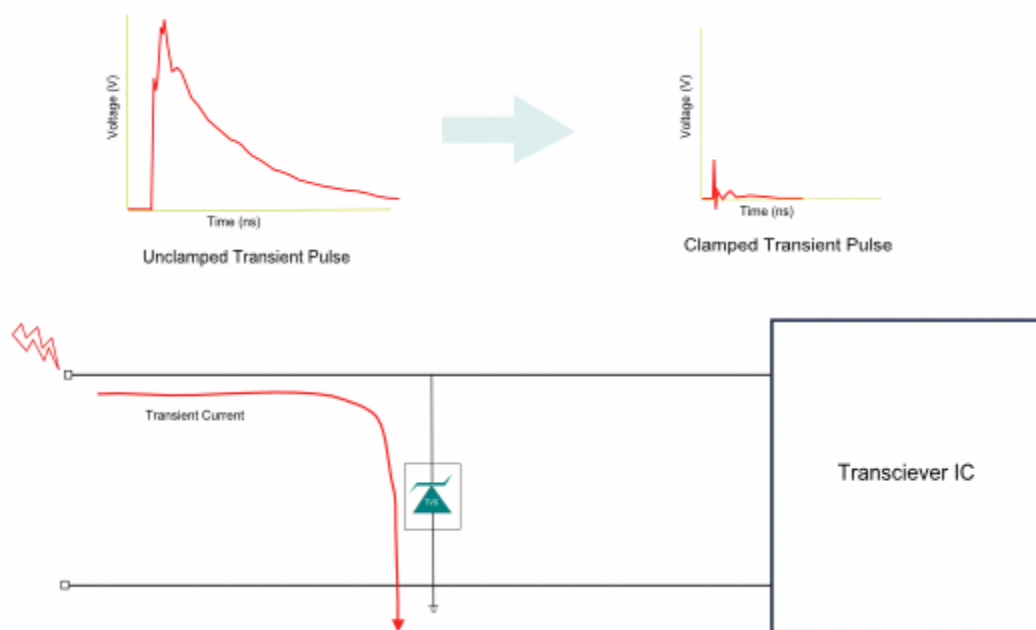


Figure 1 – TVS Diode Conceptual Operation

A closely related parameter in transient voltage suppression elements is working voltage. The working voltage, sometimes called the reverse standoff voltage (V_{rwm}), is the nominal voltage below which the TVS device presents a high impedance state and appears nearly “transparent” to the dataline. When the voltage on a dataline exceeds the working voltage, as is the case during a transient, the protection begins to clamp the voltage spike. This is not to be confused with the clamping voltage, but it is the inflection point between a high-impedance state and a low impedance shunt element. All shunt protection devices are non-linear I-V curve devices as illustrated Figure 2. A lower working voltage correlates to a protection device’s ability to engage to the transient more quickly. This is essential in protection circuitry as there is a general correlation between lower working voltage and a resulting lower clamping voltage.

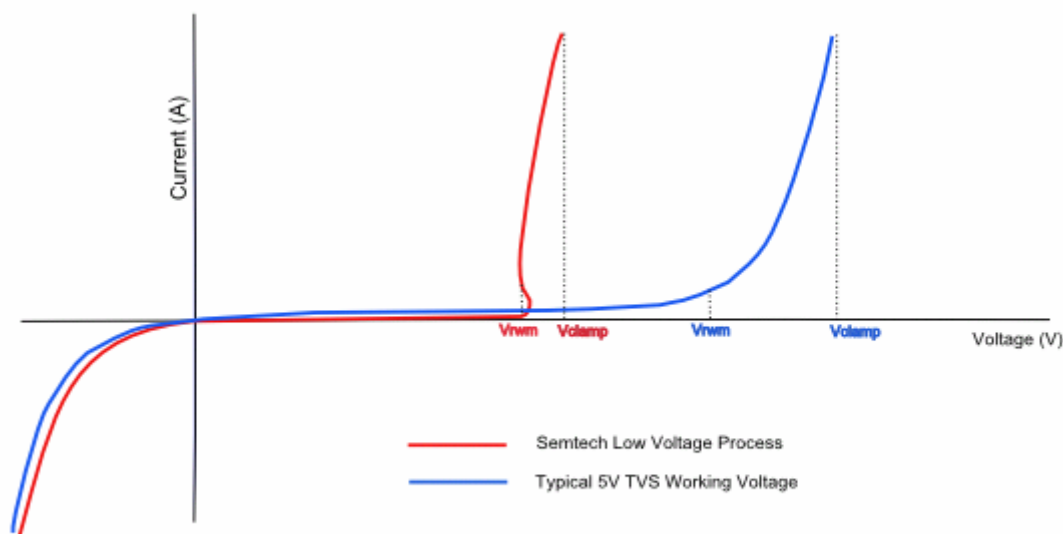


Figure 2 – IV Curve for Transient Circuit Protection Diodes

In addition to contributing to a lower clamping voltage, low working voltage circuit protection is also critical for another reason, mainly the consideration of the on-chip ESD protection structures. Consider the circuit shown in Figure 3. This diagram shows a dataline connected to a representative I/O pad at the input of a transceiver IC. It is important that the external protection TVS device engage the transient before the “on-chip” protection element triggers. If the “on-chip” ESD structure at the chip I/O responds more quickly to the transient than the external protection component, the transceiver IC sees the initial brunt of the transient stress. And, of course, the whole idea of our protection device is to divert that energy, or as much as possible, away from the transceiver IC. Choosing devices with a lower working voltage is one way to safeguard from such a scenario. There are next generation TVS devices that are achieving remarkably low working voltages, even as low as 2.5V.

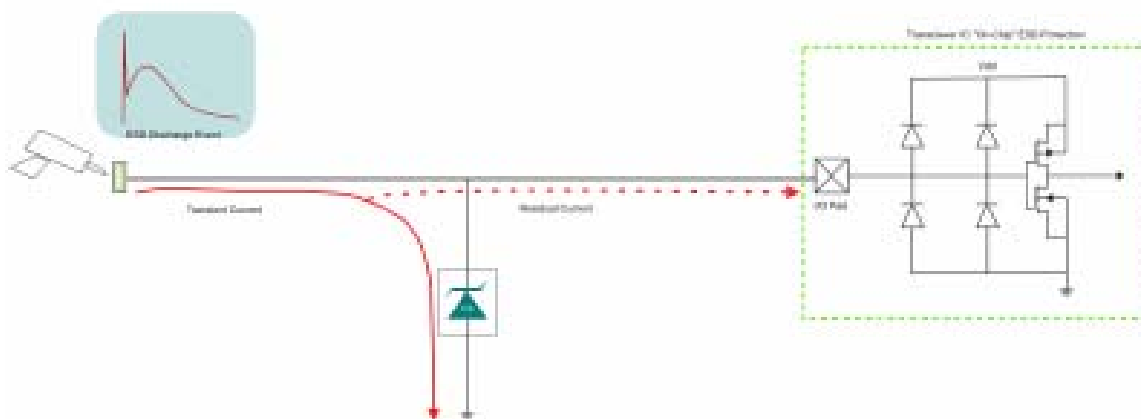


Figure 3 – TVS Diode on Dataline with representative “on-chip” ESD structure

4. “What clamping voltage is needed to insure that my system is adequately protected?”

It's unfortunate, but transceiver IC datasheets (the devices you want to protect) generally do not provide transient voltage immunity ratings. A new engineer, fresh on the job, might be tempted to look at the absolute maximum voltage rating provided on the datasheet as a reference for the maximum voltage that the IC can withstand, but this DC spec has no relationship to the voltage or current level that can be sustained for a *transient* pulse. Likewise, it is a mistake to try to correlate the 2kV HBM JEDEC rating of your transceiver IC to a *system* immunity level. There are simply too many variables at the system level.

So the question of “how much energy can my system interface survive?” is a very good one, but not an easy one to answer. There is no perfect way to make this determination other than *to test your system* to the worst case transients expected for your operating environment. One thing is certain: the lower your protection circuit can clamp the transient voltage, the better the protection and the more protection margin you will have built into your system. Lowering the clamping voltage will minimize the energy that the IC must bear during the transient. With transceiver IC geometries shrinking, it's not uncommon for a few volts of reduced clamping voltage at the peak pulse current (Ipp) to protect an IC from latch-up, system upset, degradation, or, worse, catastrophic transceiver damage. But, to understand the limits for your system interface, there's no substitute for testing your system.

5. “How should I think about placing the TVS component for optimal board layout?”

A good layout is very critical for transient protection performance. When you are dealing with a fast rise time transient, like ESD, taming the initial transient spike is highly dependent upon the quality of the PCB layout. Even a very good protection circuit may not overcome a poor layout. Here are some things to consider when you go to layout with your external protection solution.

- Place TVS components near the interface connector, when possible. This will help suppress the energy at the entry point of your PCB and will reduce the secondary effects possible from radiated emissions from the ESD event.
- Minimize parasitic inductance by running shorter trace length from the TVS device to the protected I/O line. Considering that the rise time of a simulated ESD event is 1ns, a 30A pulse (IEC 61000-4-2) on a 1nH series inductance trace can raise the clamping voltage of the device by 30V.
- When possible, make ground connections from the TVS device directly to the ground plane. If vias are required, multiple vias to the ground plane are suitable.
- On high-speed digital signals, the capacitance of the TVS device becomes an important consideration. To preserve signal integrity, select devices that will present minimal capacitive loading without sacrificing clamping performance.

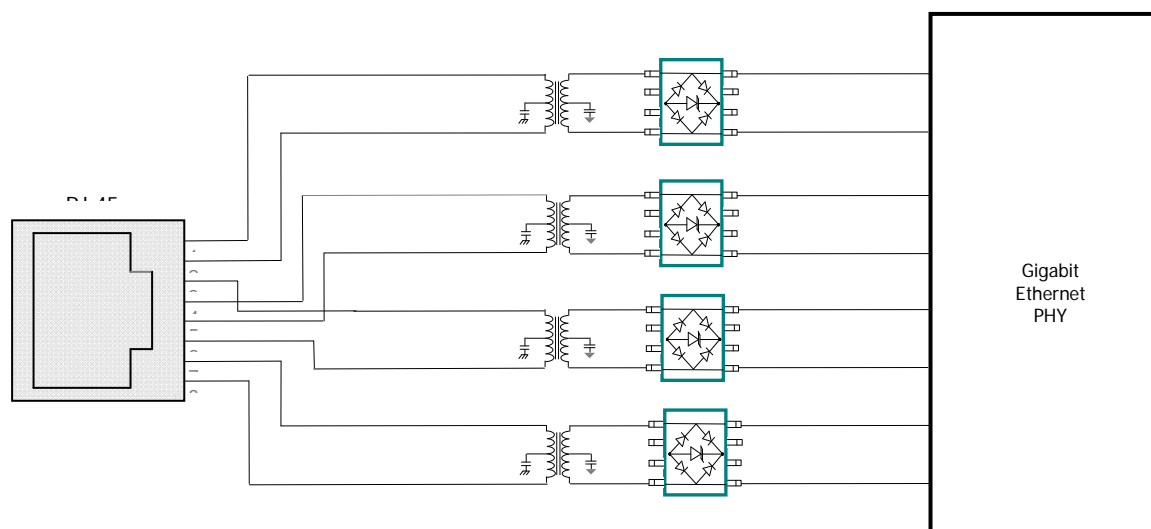


Figure 4 – RClamp2502L Flow-through layout for Gigabit Ethernet Protection

- When available, use flow-through packages on high speed interfaces. These packages allow for placing the protection component directly over the PCB differential pair. This eliminates stubs and unnecessary bends in the traces, which helps preserve signal quality. Figure 4 shows an example of how flow-through packages can be implemented.



Today's systems are more vulnerable to transient threats than ever before. By giving attention to a clean layout and careful selection of low-clamping voltage TVS components, you can insure that your system is adequately safeguarded against electrical transient threats.

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