Tips about PCB design: Part 3 - Static and dynamic PCB effects

Walt Kester - December 07, 2010

In static printed circuit board designs, leakage resistance is the dominant effect. Contamination of the PCB surface by flux residues, deposited salts, and other debris can create leakage paths between circuit nodes. Even on well-cleaned boards, it is not unusual to find 10 nA or more of leakage to nearby nodes from 15 V supply rails.

Nanoamperes of leakage current into the wrong nodes often cause volts of error at a circuit's output; for example, 10 nA into a 10 MΩ resistance causes a 0.1 V error. Unfortunately, the standard op amp pinout places the VS supply pin next to the input, which is often hoped to be at high impedance.

To help identify nodes sensitive to the effects of leakage currents, ask the simple question: If a spurious current of a few nanoamperes or more were injected into this node, would it matter?

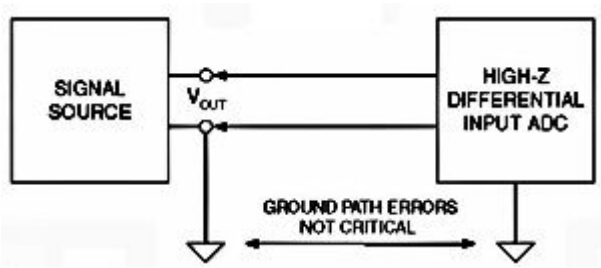

Figure C.26: A high-impedance differential input ADC also allows high transmission accuracy between source and load.

If the circuit is already built, it is possible to localize moisture sensitivity to a suspect node with a classic test. While observing circuit operation, blow on potential trouble spots through a simple soda straw. The straw focuses the breath's moisture, which, with the board's salt content in susceptible portions of the design, disrupts circuit operation upon contact.

There are several means of eliminating simple surface leakage problems. Thorough washing of circuit boards to remove residues helps considerably. A simple procedure includes vigorously brushing the boards with isopropyl alcohol, followed by thorough washing with deionized water and an 85ºC bakeout for a few hours.

Be careful when selecting board-washing solvents, though. When cleaned with certain solvents, some water-soluble fluxes create salt deposits, exacerbating the leakage problem.

Unfortunately, if a circuit displays sensitivity to leakage, even the most rigorous cleaning can offer only a temporary solution. Problems soon return upon handling or exposure to foul atmospheres and

high humidity. Some additional means must be sought to stabilize circuit behavior, such as conformal surface coating.

Fortunately, there is an answer to this problem, namely guarding, which offers a fairly reliable and permanent solution to the problem of surface leakage. Well-designed guards can eliminate leakage problems, even for circuits exposed to harsh industrial environments. Two schematics illustrate the basic guarding principle, as applied to typical inverting and noninverting op amp circuits.

Figure C.27 below illustrates an inverting mode guard application. In this case, the op amp reference input is grounded, so the guard is a grounded ring surrounding all leads to the inverting input, as noted by the dotted line.

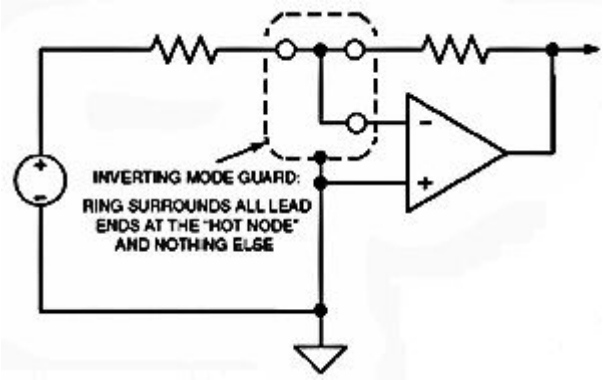

Figure C.27: Inverting mode guard encloses all op amp inverting input connections within a grounded guard ring.

Basic guarding principles are simple: Completely surround sensitive nodes with conductors that can readily sink stray currents, and maintain the guard conductors at the exact potential of the sensitive node (as otherwise the guard will serve as a leakage source rather than a leakage sink).

For example, to keep leakage into a node below 1 pA (assuming 1000 MΩleakage resistance) the guard and guarded node must be within 1 mV. Generally, the low offset of a modern op amp is sufficient to meet this criterion.

There are important caveats to be noted with implementing a true high-quality guard. For traditional through-hole PCB connections, to be most effective the guard pattern should appear on both sides of the circuit board. It should also be connected along its length by several vias.

Finally, when either justified or required by the system design parameters, do make an effort to include guards in the PCB design process from the outset—there is little likelihood that a proper guard can be added as an afterthought.

Figure C.28 below illustrates the case for a noninverting guard. In this instance the op amp reference input is directly driven by the source, which complicates matters considerably. Again, the guard ring completely surrounds all of the input nodal connections. In this instance however, the guard is driven from the low impedance feedback divider connected to the inverting input.

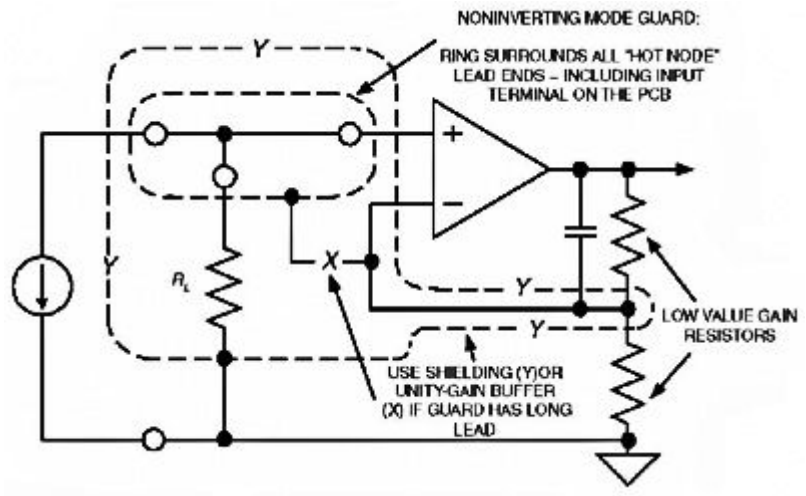

Figure C.28: Noninverting mode guard encloses all op amp noninverting input connections within a low impedance, driven guard ring.

Usually the guard-to-divider junction will be a direct connection, but in some cases a unity gain buffer might be used at X to drive a cable shield or to maintain the lowest possible impedance at the guard ring.

In lieu of the buffer, another useful step is to use an additional, directly grounded screen ring, Y, which surrounds the inner guard and the feedback nodes as shown. This step costs nothing except some added layout time and will greatly help buffer leakage effects into the higher-impedance inner guard ring.

Of course what hasn't been addressed to this point is just how the op amp itself is connected into these guarded islands without compromising performance. The traditional method using a TO-99 metal can package device was to employ double-sided PCB guard rings, with both op amp inputs terminated within the guarded ring.

Many high-impedance sensors use the above described method. The next section illustrates how more modern IC packages can be mounted to PCB patterns and take advantage of guarding and low leakage operation.

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MINIDIP & SOIC Op Amp PCB Guard Layouts

Modern assembly practices have favored smaller plastic packages such as 8-pin MINIDIP and SOIC types. Some suggested partial layouts for guard circuits using these packages is shown in the next two figures.

While guard traces may also be possible with even more tiny op amp footprints, such as SOT-23, SC70, etc., the required trace separations become even more confining, challenging the layout designer as well as the manufacturing processes.

For the ADI "N" style MINIDIP package, **Figure C.29 below** illustrates how guarding can be accomplished for inverting (left) and noninverting (right) operating modes. This setup would also be applicable to other op amp devices where relatively high voltages occur at pin 1 or 4.

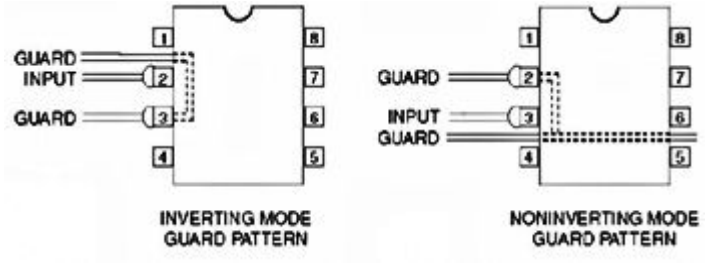

Figure C.29: PCB guard patterns for inverting and noninverting mode op amps using 8-pin MINIDIP (N) package.

Using a standard 8-pin DIP outline for a single op amp, it can be noted that this package's 0.1" pin spacing allows a PC trace (here, the guard trace) to pass between adjacent pins. This is the key to implementing effective DIP package guarding, as it can adequately prevent a leakage path from the VS supply at pin 4 or from similar high potentials at pin 1.

For the left-side inverting mode, note that the grounded guard traces connected to pin 3 surround the op amp inverting input (pin 2), and run parallel to the input trace. This guard would be continued out to and around the source and feedback connections of Figure C.27 (or other similar circuit), including an input pad in the case of a cable.

In the right-side noninverting mode, the guard voltage is the feedback divider voltage to pin 2. This corresponds to the inverting input node of the amplifier, from Figure C.28.

Note that in both of the cases of Figure C.29, the guard physical connections shown are only partial—an actual layout would include all sensitive nodes within the circuit. In both the inverting and the noninverting modes using the MINIDIP or other through-hole style package, the PCB guard traces should be located on both sides of the board, with top and bottom traces connected with several vias.

Things become slightly more complicated when using guarding techniques with the SOIC sur-fac--mount ("R") package, as the 0.05" pin spacing doesn't easily allow routing of PCB traces between the pins. But there is still an effective guarding answer, at least for the inverting case. **Figure C.30 below** shows guards for the ADI "R" style SOIC package.

Note that for many single op amp devices in this SOIC "R" package, pins 1, 5, and 8 are "No Connect" pins. For such instances, this means that these locations can be employed in the layout to route guard traces.

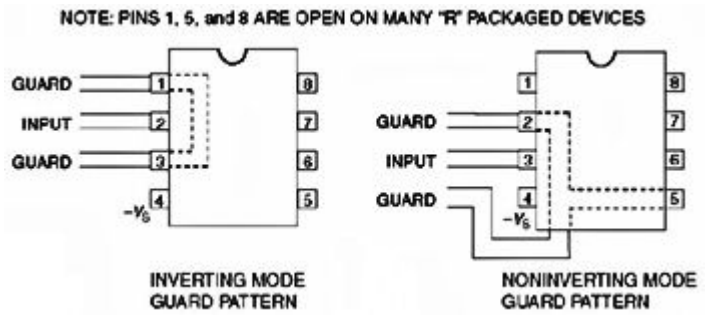

Figure C.30. PCB guard patterns for inverting and noninverting mode op amps using 8-pin SOIC (R) package.

In the case of the inverting mode (left), the guarding is still completely effective, with the dummy pin 1 and pin 3 serving as the grounded guard trace. This is a fully effective guard without compromise.

Also, with SOIC op amps, much of the circuitry around the device will not use through-hole components. So, the guard ring may only be necessary on the op amp PCB side.

In the case of the follower stage (right), the guard trace must be routed around the negative supply at pin 4, and thus pin 4 to pin 3 leakage isn't fully guarded. For this reason, a precision high-impedance follower stage using an SOIC package op amp isn't generally recommended, as guarding isn't as effective for dual supply connected devices.

However, an exception to this caveat does apply to the use of a single-supply op amp as a non-inverting stage. For example, if the AD8551 is used, pin 4 becomes ground, and some degree of intrinsic guarding is then established by default.

Dynamic PCB Effects

Although static PCB effects can come and go with changes in humidity or board contamination, problems that most noticeably affect the dynamic performance of a circuit usually remain relatively constant. Short of a new design, washing or any other simple fixes can't fi x them. As such, they can permanently and adversely affect a design's specifications and performance.

The problems of stray capacitance, linked to lead and component placement, are reasonably well known to most circuit designers. Since lead placement can be permanently dealt with by correct layout, any remaining difficulty is solved by training assembly personnel to orient components or bend leads optimally.

Dielectric absorption (DA), on the other hand, represents a more troublesome and still poorly understood circuit-board phenomenon. Like DA in discrete capacitors, DA in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes. Its effect is inverse with spacing and linear with length.

As shown in **Figure C.31 below**, the RC model for this effective capacitance ranges from 0.1 pF to 2.0 pF, with the resistance ranging from 50 MΩ to 500 MΩ. Values of 0.5 pF and 100 MΩare most common. Consequently, circuit-board DA interacts most strongly with high-impedance circuits.

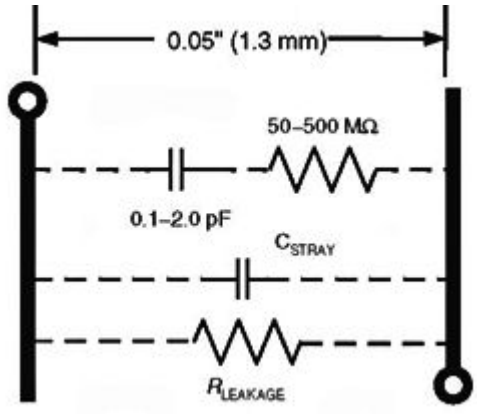

Figure C.31: Dielectric ambsorption (DA) plagues dynamic response of PCB-based circuits.

PCB DA most noticeably influences dynamic circuit response, for example, settling time. Unlike circuit leakage, the effects aren't usually linked to humidity or other environmental conditions, but rather, are a function of the board's dielectric properties.

The chemistry involved in producing plated-through holes seems to exacerbate the problem. If circuits don't meet expected transient response specs, consider PCB DA as a possible cause.

Fortunately, there are solutions. As in the case of capacitor DA, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes from parasitic coupling often eliminate the problem. (Note that these guards should be duplicated on both sides of the board, in cases of through-hole components.) As noted previously, low-loss PCB dielectrics are also available at higher costs.

PCB "hook," similar if not identical to DA, is characterized by variation in effective circuit-board capacitance with frequency. In general, it affects high-impedance circuit transient response where board capacitance is an appreciable portion of the total in the circuit. Circuits operating at frequencies below 10 kHz are the most susceptible. As in circuit-board DA, the board's chemical makeup very much influences its effects.

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Stray Capacitance

When two conductors aren't short-circuited together or totally screened from each other by a conducting (Faraday) screen, there is a capacitance between them. So, on any PCB, there will be a large number of capacitors associated with any circuit (which may or may not be considered in models of the circuit).

Where high-frequency performance matters (and even DC and VLF circuits may use devices with high Ft and therefore be vulnerable to high-frequency instability), it is very important to consider the effects of this stray capacitance.

Any basic textbook will provide formulas for the capacitance of parallel wires and other geometric configurations). The example we need consider in this discussion is the parallel plate capacitor, often formed by conductors on opposite sides of a PCB. The basic diagram describing this capacitance is shown in **Figure C.32 below**.

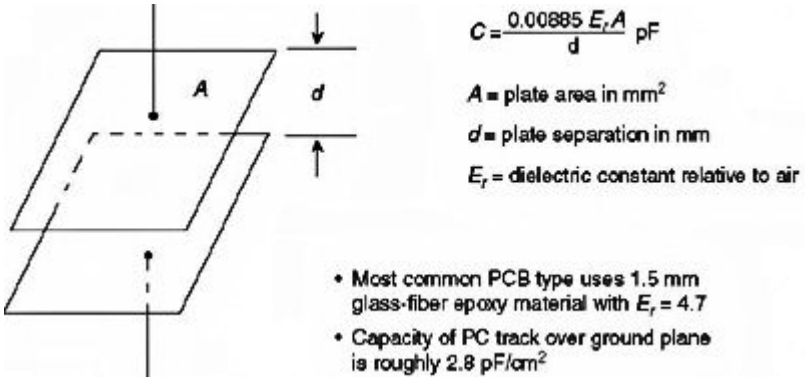

Figure C.32: Capacitance of two parallel plates.

Neglecting edge effects, the capacitance of two parallel plates of area A mm2 and separation d mm in a medium of dielectric constant Er relative to air is 0.00885 Er A/d pF.

From this formula, we can calculate that for general-purpose PCB material (Er 4.7, d 1.5 mm), the capacitance between conductors on opposite sides of the board is just under 3 pF/cm.2 In general, such capacitance will be parasitic, and circuits must be designed so that it does not affect their performance.

While it is possible to use PCB capacitance in place of small discrete capacitors, the dielectric properties of common PCB substrate materials cause such capacitors to behave poorly. They have a

rather high temperature coefficient and poor Q at high frequencies, which makes them unsuitable for many applications. Boards made with lower loss dielectrics such as Teflon are expensive exceptions to this rule.

Capacitive Noise and Faraday Shields

There is a capacitance between any two conductors separated by a dielectric (air or vacuum are dielectrics). If there is a change of voltage on one, there will be a movement of charge on the other. A basic model for this is shown in **Figure C.33 below.**

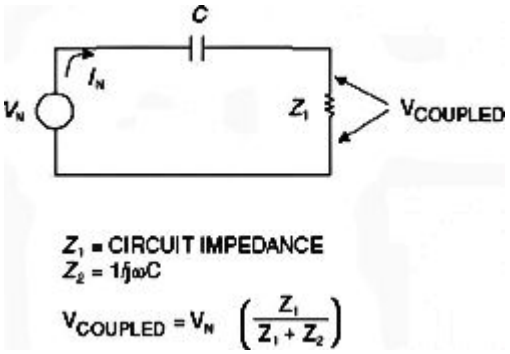

Figure C.33: Capacitive coupling equivalent circuit model.

It is evident that the noise voltage VCOUPLED appearing across Z1 may be reduced by several means, all of which reduce noise current in Z1. They are reduction of the signal voltage VN, reduction of the frequency involved, reduction of the capacitance, or reduction of Z1 itself.

Unfortunately, however, often none of these circuit parameters can be freely changed, and an alternate method is needed to minimize the interference. The best solution toward reducing the noise coupling effect of C is to insert a grounded conductor, also known as a Faraday shield, between the noise source and the affected circuit. This has the desirable effect of reducing Z1 noise current, thus reducing VCOUPLED.

A Faraday shield model is shown by **Figure C.34 below**. In the left picture, the function of the shield is noted by the way it effectively divides the coupling capacitance, C. In the right picture, the net effect on the coupled voltage across Z1 is shown. Although the noise current IN still fl ows in the shield, most of it is now diverted away from Z1. As a result, the coupled noise voltage VCOUPLED across Z1 is reduced.

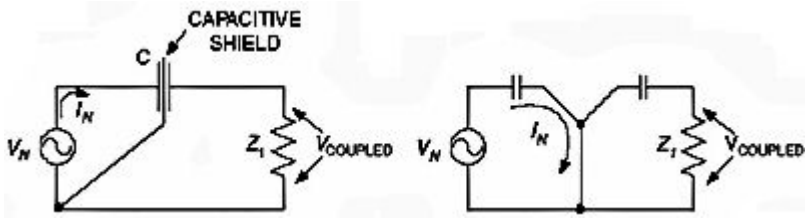

Figure C.34: An operational model of a Faraday shield.

A Faraday shield is easily implemented and almost always successful. Thus capacitively coupled noise is rarely an intractable problem. However, to be fully effective, a Faraday shield must completely block the electric field between the noise source and the shielded circuit. It must also be connected so that the displacement current returns to its source, without fl owing in any part of the circuit where it can introduce conducted noise.

The Floating Shield Problem

It is quite important to note here that a conductor that is intended to function as a Faraday shield must never be left fl oating, because this almost always increases capacity and exacerbates the noise problem.

An example of this “floating shield” problem is seen in side-brazed ceramic IC packages. These DIP packages have a small square conducting Kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package, or it may be left unconnected.

Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. Alas, many analog circuits don’t have a ground pin at a package corner, and the lid is left floating—acting as an antenna for noise. Such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic DIP package, where the chip is completely unshielded.

Whenever practical, it is good practice for the user to ground the lid of any side-brazed ceramic IC where the lid is not grounded by the manufacturer, thus implementing an effective Faraday shield.

This can be done with a wire soldered to the lid (this will not damage the device, as the chip is thermally and electrically isolated from the lid). If soldering to the lid is unacceptable, a grounded phosphor-bronze clip or conductive paint from the lid to the ground pin may be used to make the ground connection,.

A **safety note** is appropriate at this point: Never attempt to ground such a lid without first verifying that it is unconnected. Occasionally device types are found with the lid connected to a power supply rather than to ground.

A case where a Faraday shield is impractical is between IC chip bondwires. This can have important consequences, as the stray capacitance between chip bondwires and associated lead-frames is typically 0.2 pF, with observed values generally between 0.05 pF and 0.6 pF.

Buffering ADCs Against Logic Noise

If we have a high-resolution data converter (ADC or DAC) connected to a high-speed data bus that carries logic noise with a 2 V/ns–5 V/ns edge rate, this noise is easily connected to the converter analog port via stray capacitance across the device. Whenever the data bus is active, intolerable amounts of noise are capacitively coupled into the analog port, thus seriously degrading performance.

This particular effect is illustrated by the diagram of **Figure C.35 below**, where multiple package capacitors couple noisy edge signals from the data bus into the analog input of an ADC.

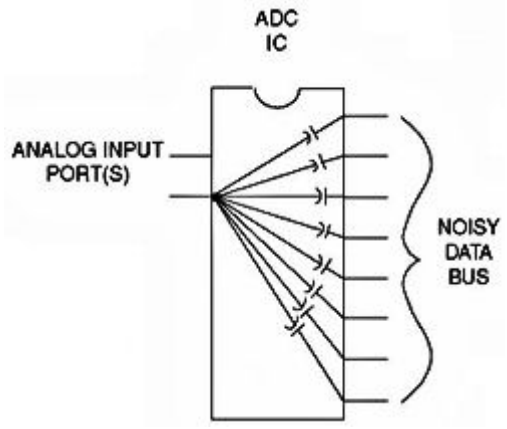

Figure C.35: A high-speed ADC IC sitting on a fast data bus couples digital noise into the analog port, thus limiting performance.

As of this writing, present technology offers no cure for this problem, within the affected IC device itself. The problem also limits performance possible from other broadband monolithic mixed signal ICs with single-chip analog and digital circuits.

Fortunately, this coupled noise problem can simply be avoided by not connecting the data bus directly to the converter. Instead, use a CMOS latched buffer as a converter-to-bus interface, as shown by **Figure C.36 below.**

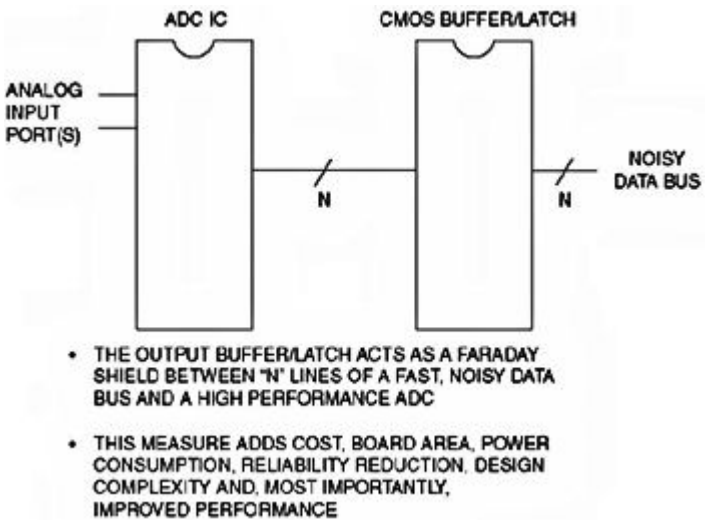

Figure C.36: A high-speed ADC IC using a CMOS buffer/latch at the output shows enhanced immunity of digital data bus noise.

Now the CMOS buffer IC acts as a Faraday shield and dramatically reduces noise coupling from the digital bus. This solution costs money, occupies board area, reduces reliability (very slightly), consumes power, and it complicates the design—but it does improve the signal-to-noise ratio of the converter. The designer must decide whether it is worthwhile for individual cases, but in general it is highly recommended. Bus switches can also be utilized to isolate data lines from buses.

To read Part 1, go to "**Dealing with harmful PCB effects**."
To read Part 2, go to "**Single card grounding for multicard systems**."

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