DATA SHEET

NVIDIA Jetson TX1 System-on-Module

Description

The NVIDIA® Jetson TX1 System-on-Module (SoM) combines the NVIDIA Maxwell GPU architecture with an ARM® Cortex® - A57 MPCore (Quad-Core) CPU cluster to deliver the performance and power efficiency required by next generation products targeting GPU computing, computer graphics and artificial intelligence (AI).

Designed for power and space constrained applications, the Jetson TX1 integrates:

- Parallel computing, computer vision and machine learning capabilities.
- Advanced 3D graphics, video and image processing.
- 32-bit and 64-bit operating capability.

This combination of exceptional performance and power efficiency, integrated capabilities, rich I/O, and small-size enable new classes of products while reducing complexity in system integration. The Jetson TX1 is ideal for many applications, including:

- Augmented Reality (AR)
- Drones
- Gaming Devices
- Intelligent Video Analytics (IVA)
- Portable Medical Devices
- Robotics
- Smart Factory
- Virtual Reality (VR)

Ordering Information

Part Number	Description
900-82180-0001-000	Jetson TX1 System-on-Module (SoM)
900-82180-A301-000	Jetson TX1 System-on-Module (SoM) for India ‡
900-82180-A401-000	Jetson TX1 System-on-Module (SoM) for Israel ‡

‡ Region-specific SKU – supports full functionality

Description		Jetson TX1 Module
Maxwell GPU		
256-core GPU | End-to-end lossless compression | Tile Caching | OpenGL® 4.5 | OpenGL ES 3.1 | Vulkan™ 1.0 | CUDA® | GPGPU | Android™ Extension Pack (AEP)		
OpenGL ES Shader Performance (up to)	GFLOPS (fp16)	1024◊
CPU Subsystem		
ARM® Cortex® -A57 MPCore (Quad-Core) Processor with NEON Technology. Operating Frequency per Core (up to)		1.73GHz‡
L1 Cache: 48KB L1 instruction cache (I-cache) per core; 32KB L1 data cache (D-cache) per core | L2 Unified Cache: 2MB		
HD Video & JPEG		
Decode		
H.265: Main10		2160p 60fps | 1080p 240fps
H.265: Main		2160p 60fps | 1080p 240fps
H.264: Baseline, Main, High, Stereo SEI (half-res)		2160p 60fps | 1080p 240fps
H.264: MVC Stereo (per view)		2160p 30fps | 1080p 120fps
WEBM VP9		2160p 60fps | 1080p 240fps
WEBM VP8		2160p 60fps | 1080p 240fps
VC-1: Simple, Main, Advanced		1080p 120fps | 1080i 240fps
MPEG-2: Main		2160p 60fps | 1080p 240fps | 1080i 240fps
Encode		
H.265 (I and P frames)		2160p 30fps | 1080p 120fps
H.264: Baseline, Main, High		2160p 30fps | 1080p 120fps
H.264: MVC Stereo (per view)		1440p 30fps | 1080p 60fps
WEBM VP8		2160p 30fps | 1080p 120fps
JPEG (Decode & Encode)		600 MP/sec
Audio Subsystem		
Dedicated programmable audio processor | ARM Cortex A9 with NEON operating at up to 844MHz | Digital Audio Mixer: 10-in/5-out (up to 8 channels per stream) | 3 x I2S Stereo I/O | PDM Receiver: 3 x (Stereo) or 6 x (Mono)		
Display Controller Subsystem		
Two independent display controllers with support for DSI with VESA link compression (VESA DSC), HDMI, and eDP		
Captive Panel		
MIPI-DSI (1.5Gbps/lane)	Uncompressed: 24bpp	Support for Single x4 or Dual x4 links
	VESA DSC Compression: 12bpp	
eDP 1.4 (HBR2 5.4Gbps)	24bpp	Single link (1x4) 4096x2160 at 60Hz
External Display		
HDMI 2.0 (6Gbps)	24bpp	4096x2160 at 60Hz
Imaging System		
Dedicated RAW to YUV processing engines process up to 1200Mpix/s | supports up to 128MP sensor		
MIPI CSI 2.0 up to 1.5Gbps (per lane)		Support for x4 and x2 configurations (up to 3 x4-lane or 6 x2-lane cameras)
Clocks		
System clock: 38.4 MHz | Sleep clock: 32.768 KHz | Dynamic clock scaling and clock source selection		
Boot Sources		
Internal eMMC and USB (recovery mode)		

Description	Jetson TX1 Module
Security	
Secure memory with video protection region for protection of intermediate results | Configurable secure DRAM regions for code and data protection | Hardware acceleration for AES 128/192/256 encryption and decryption to be used for secure boot and multimedia Digital Rights Management (DRM) | Hardware acceleration for AES CMAC, SHA-1 and SHA-256 algorithms | 2048-bit RSA HW for PKC boot| HW Random number generator (RNG) SP800-90 | TrustZone technology support for DRAM, peripherals | Dedicated HDCP HW	
Memory	
Dual Channel | Secure External Memory Access Using TrustZone Technology | System MMU	
Memory Type	4ch x 16-bit LPDDR4
Maximum Memory Bus Frequency (up to)††	1600MHz
Memory Capacity	4GB
Storage	
eMMC 5.1 Flash Storage	
Bus Width	8-bit
Maximum Bus Frequency	200MHz (HS400)
Storage Capacity	16GB
Connectivity	
WiFi	
Radio type	IEEE 802.11ac 2x2
Maximum data rate	867Mbps
Bluetooth	
Version level	4.0
Maximum transfer rate	24Mbps
LAN	
10/100/1000 BASE-T Ethernet	
Peripheral Interfaces*	
XHCI host controller with integrated PHY: 2 x USB 3.0, 3 x USB 2.0 | USB 3.0 device controller with integrated PHY | EHCI controller with embedded hub for USB 2.0 | 5-lane PCIe: one x1 and one x4 controllers | SATA (1 port) | 2 x SD/MMC controllers (supporting eMMC 5.1, SD 4.0, SDHOST 4.0 and SDIO 3.0) | 3 x UART | 3 x SPI | 4 x I^2C | 4 x I2S: support I^2S, RJM, LJM, PCM, TDM (multi-slot mode) | GPIOs	
Operating Requirements	
Temperature Range	-25C – 80C**
Module Power	6.5 – 15 W**
Applications	
Embedded (Intelligent Video Analytics, Drones, Robotics, etc.), Automotive Research, Clamshells, Gaming, Internet TV, and more	

◊ See Table 3 for Guaranteed GPU operation across supported temperature range.

‡ See Table 4 for Guaranteed CPU operating frequency across supported temperature range.

†† Dependent on board layout. Refer to Interface Design Guide for layout guidelines.

* Refer to the Interface Design Guide and Technical Reference Manual to determine which peripheral interface options can be simultaneously exposed.

** Refer to the Product Design Guide and Thermal Design Guide for evaluating product power and thermal solution requirements

Revision History

Version	Date	Description
v0.9	AUG, 2015	Initial Release
v0.91	FEB, 2016	Updated CPU operating frequency. Added Use Case Models. Updated Package Drawing and Dimensions: updated weight to include TTP base and top plate weight, changed MAX TTP height from 6.0 ± 0.25 to 6.25, corrected connector pin dimensions.
v1.0	SEP, 2016	Updated Electrical Characteristics section

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1.0 Module Overview

The Jetson TX1 incorporates the following components and interfaces:

- NVIDIA Tegra X1 SoC
  - NVIDIA Maxwell GPU
  - Quad-core ARM Cortex-A57 CPU
- LPDDR4 memory
- eMMC 5.1 storage
- 802.11ac 2x2 WiFi
- Gigabit Ethernet
- PMIC
- Thermal Transfer Plate (TTP) (primary thermal interface)
- 400-pin board-to-board connector (exposes both high-speed and low-speed industry standard I/O)
- WiFi/BT antenna connectors

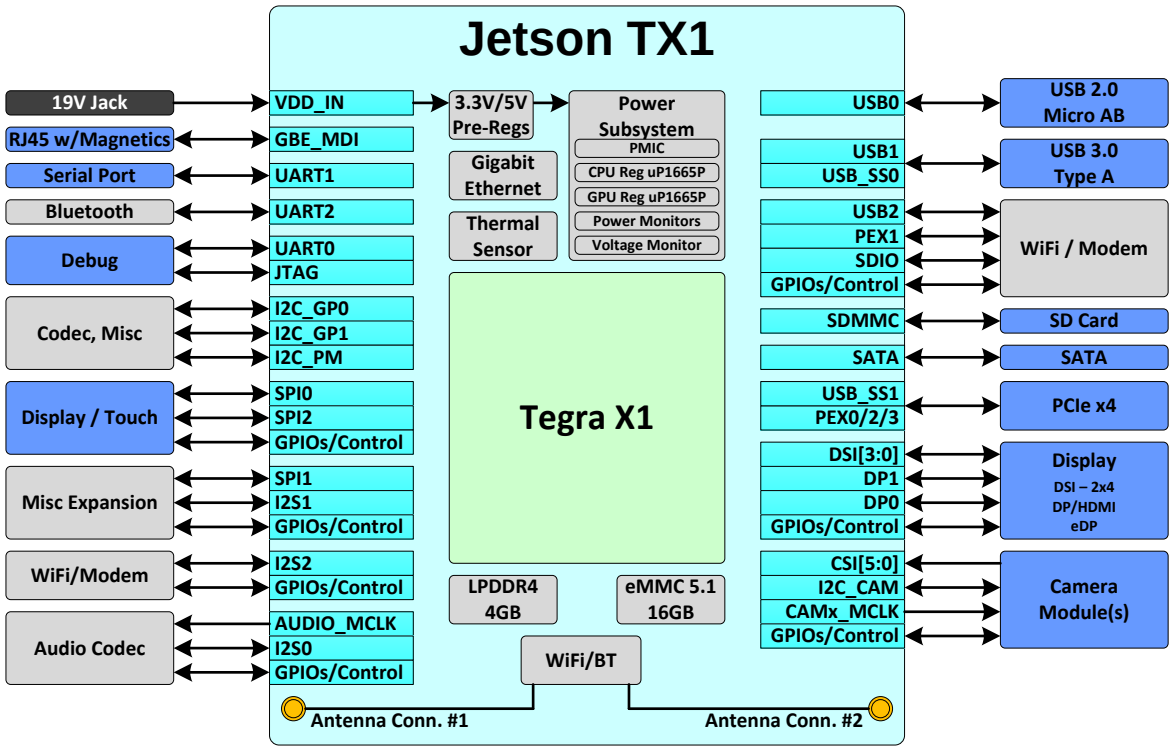
Table 1 Manufacturers and Part Numbers for 3rd Party Components Integrated on the Jetson TX1 Module

Component	Manufacturer	Part Number
WiFi 802.11ac Client/BT	Broadcom Corp.	BCM4354
Ethernet Controller 10/100/1000 Mbps	Realtek Semiconductor Corp.	RTL8153
Power Management IC (PMIC)	Maxim Integrated	MAX77620
400 pin Board-to-board connector	Samtec	REF-186137-03◇

◇ Mating connector for OEM carrier board is REF-186138-02.

Refer to the manufacturer's documentation for specific component details and specifications. All features supported by a 3rd party component may not be enabled on the Jetson TX1 module.

Figure 1 Jetson TX1 Block Diagram – General Application



1.1 Tegra X1 SoC

The NVIDIA Tegra® X1 SoC couples the latest NVIDIA Maxwell™ GPU architecture with an ARM®v8 CPU cluster to deliver high performance and power efficiency. The Maxwell GPU implements a number of architectural enhancements designed to extract maximum performance per watt consumed. Designed for use in power-limited environments, Tegra X1 processors enable industry-leading visual computing capabilities, 32-bit and 64-bit operating capability, and integrate advanced multi-function audio, video and image processing pipelines that exceed performance targets for next generation small form factor (SFF) devices.

1.2 Memory

On-board 4GB of LPDDR4, over a 4 channel x 16-bit interface. The maximum frequency is 1600MHz. The theoretical peak memory bandwidth is 25.6 GB/s.

1.3 Storage

On-board 16GB of eMMC 5.1 flash storage. The theoretical peak bandwidth is 400 MB/s

1.4 Connectivity

WiFi/Bluetooth integrated on the Jetson TX1 module supports:

- WiFi Ready
  - 802.11ac compliant (backwards compatible with legacy 802.11b/g/a/n devices)
  - 867Mbps PHY maximum data rate
  - 2x2 MIMO

- Bluetooth Ready
  - Bluetooth 4.0 ready (can connect to Bluetooth 4.0 enabled devices)
  - HIDP
  - RFKILL

Table 2 lists the WiFi frequency ranges, modes, and channels supported on the Jetson TX1 module. Table also includes the equivalent isotropically radiated power (EIRP) for each mode.

Table 2 Jetson TX1 WiFi Power and Channel Specification

Frequency(MHz)	Mode	EIRP(mW)	Total Supported Channels	Channel List
2412~2472	802.11b	48.5	11	1,2,3,4,5,6,7,8,9,10,11
2412~2472	802.11g	30.5	11	1,2,3,4,5,6,7,8,9,10,11
2412~2472	802.11n HT20	38.5	11	1,2,3,4,5,6,7,8,9,10,11
5180~5320	802.11a	96.5	8	36,40,44,48,52,56,60,64
5180~5320	802.11n HT20	52.0	8	36,40,44,48,52,56,60,64
5190~5310	802.11n HT40	92.0	4	38,46,54,62
5180~5320	802.11ac VHT20	52.0	8	36,40,44,48,52,56,60,64
5190~5310	802.11ac VHT40	92.0	4	38,46,54,62
5190~5310	802.11ac VHT80	123.0	2	42,58

1.5 Networking

The Ethernet controller on the Jetson TX1 supports:

- 10/100/1000 Mbps Gigabit Ethernet
- IEEE 802.3u Media Access Controller (MAC)
- Embedded memory

1.6 Power

Power is provided by a single DC input, and supplied to the devices on board through a power management IC (PMIC) and dedicated voltage regulators. More details can be found in Section 2.0

1.7 Thermal Transfer Plate

Jetson TX1 is provided with a thermal transfer plate (TTP) to simplify integration with a system-level thermal solution. The TTP mechanically isolates the Jetson TX1 board and components from external mechanical forces, standardizes the thermal and mechanical interface, and allows for a modular system design.

Refer to the ***Jetson TX1 Thermal Design Guide*** for system-level thermal and mechanical requirements.

1.8 Board-to-board Connector

The primary interface to Jetson TX1 is via a 400-pin board-to-board connector. This connector exposes both high-speed and low-speed industry standard I/O. Refer to Section 4.0 of this document for the individual pin descriptions and mapping.

See the ***NVIDIA Jetson TX1 OEM Product Design Guide*** for details on integrating the TX1 module and mating connector into product designs.

1.9 WiFi/BT Antenna Connector

Male I-PEX antenna connectors for WiFi and BT are located on the module. These support antennas with the following characteristics:

- 2x Female I-PEX connector
- Dual-band (x2), dipole
- 2.4 GHz and 5 GHz frequency bands
- 50 Ω impedance

2.0 Power and System Management

The Jetson TX1 module was designed with ease of system integration in mind. It operates from a single power source (VDD_IN) with all internal module voltages and IO voltages generated from this input. An optional back up battery can be attached to the VDD_RTC module input (this will maintain the on system RTC, when VDD_IN is not present).

The Jetson TX1 module is required to be powered on and off in a known sequence. Sequencing is determined through a set of control signals; the signal CARRIER_PWR_ON is provided so that the carrier board is powered on using this signal after the Jetson TX1 is fully powered.

2.1 Use Case Models

The Jetson TX1 module can be used in a wide variety of applications requiring varying performance metrics. To accommodate these varying conditions, Tegra SoC frequencies and voltages are actively managed by Tegra Power and Thermal Management Software and influenced by workload. The following use case models were used to detail CPU and GPU performance; models were selected to demonstrate a varied range of operating time. Note that the operating frequencies for CPU and GPU may have different maximum limits in each model.

Use Case Models (UCM):

- UCM #1
  - Operating time per day up to maximum specification: 20% (remaining time is spent in a SLEEP or OFF state)
- UCM #2
  - Operating time per day up to maximum specification: 100%

Table 3 Guaranteed GPU Operations (UCM#1, UCM#2)

Use Case Model	Guaranteed GPU Operations: GFLOPS (FP16)		
	T_J <= 70C	T_J<= 90C	T_J <= 105C
UCM: 1	1024	1024	942
UCM: 2	1024	1024	942

T_J = SoC Junction Temperature

Table 4 Guaranteed CPU Operating Frequency (UCM #1, UCM #2)

Use Case Model	Guaranteed CPU Operating Frequency		
	T_J <= 70C	T_J <= 90C	T_J <= 105C
UCM: 1	1.73GHz	1.63GHz	1.55GHz
UCM: 2	1.68GHz	1.55GHz	1.47GHz

T_J = SoC Junction Temperature

2.2 Power Rails

2.2.1 VDD_IN

VDD_IN must be supplied by the carrier board that the Jetson TX1 is designed to connect to. It must meet the required electrical specifications detailed in Section 5.

2.2.2 VDD_RTC

A back up battery can be connected to this input. It is used to maintain the JETSON TX1 RTC when VDD_IN is not present. This pin is connected directly to the onboard PMIC. When a backup cell is connected to the PMIC, the RTC will retain its contents and also can be configured to charge the backup cell.

The following backup cells may be attached to this pin:

- Super Capacitor (gold cap, double layer electrolytic)
- Standard capacitors (tantalum)
- Rechargeable Lithium Manganese cells

The backup cells must provide a voltage in the range 2.5V to 3.5V. These will be charged with a constant current (CC) , constant voltage (CV) charger that can be configured between 2.5V and 3.5V CV output and 50uA to 800uA CC.

2.2.3 IO Rail Voltages

All of the signals on the Jetson TX1 interfaces are referenced to on-module voltage rails. No IO voltage is required to be supplied to the module. See the ***Jetson TX1 OEM Product Design Guide*** for details of connecting to each of the interfaces.

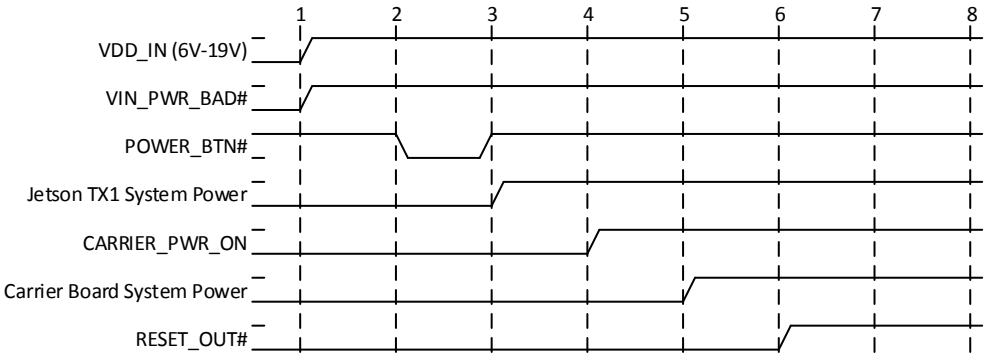
2.3 Power Sequencing

The following sections provide an overview of the power sequencing steps between the carrier board and Jetson TX1 module. Refer to the ***Jetson TX1 OEM Product Design Guide*** for system level details on the application of power, power sequencing and monitoring. The Jetson TX1 module and the product carrier board must be power sequenced properly to avoid potential damage to components on either the module or the carrier board system.

2.3.1 Power Up

During power up, the carrier board must wait until the signal CARRIER_PWR_ON is asserted from the Jetson TX1 before enabling its power. Jetson TX1 will de-assert the RESET_OUT# signal to enable the complete system to boot.

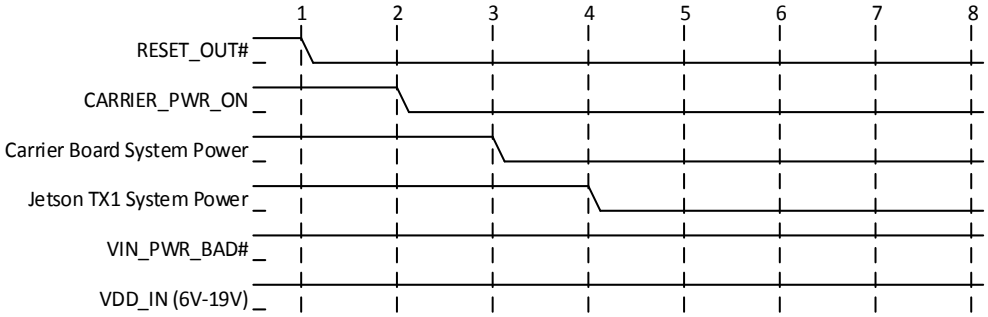
Figure 2 Power Up Sequence



2.3.2 Power Down

On receiving a Shutdown request the Jetson TX1 will assert the RESET_OUT# signal, allowing the carrier board to put any components into a known state. The CARRIER_PWR_ON signal will then be de-asserted to indicate to the carrier board to power down. The carrier board must disable its power at this point; the Jetson TX1 module will then disable its power and shut down.

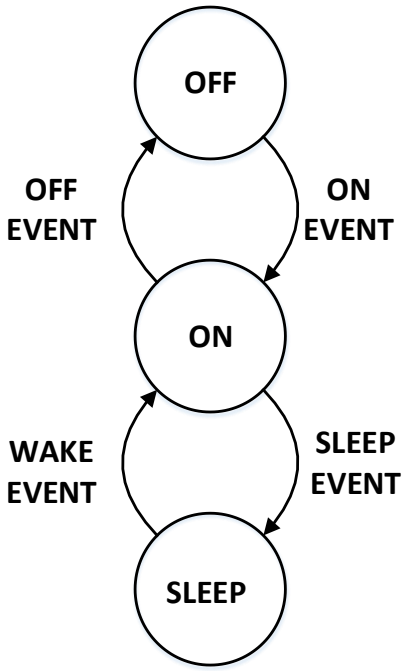
Figure 3 Power Down Sequence



2.4 Power States

The Jetson TX1 module operates in 3 main power modes: OFF, ON and SLEEP. The module transitions between these states are based on various events from hardware or software. Figure 4 shows the transitions between these states.

Figure 4 Power State Diagram



2.4.1 ON State

The ON power state is entered from either OFF or SLEEP states. In this state the Jetson TX1 module is fully functional and will operate normally. An ON event has to occur for a transition between OFF and ON states. The only ON EVENT currently used is a low to high transition on the POWER_BTN# pin. This must occur with VDD_IN connected to a power rail, and VIN_PWR_BAD# is asserted (at a logic1). The VIN_PWR_BAD# control is the carrier board indication to the Jetson TX1 module that the VDD_VIN power is good. The Carrier board should assert this high only when VIN has reached its required voltage level and is stable. This prevents the Jetson TX1 module from powering up until the VIN power is stable.

NOTE: The Jetson TX1 module does include an Auto-Power-On option; a system input (i.e., CHARGER_PRSNT#) that could enable the module to power on if asserted. For more information on available signals and broader system usage, see the ***Jetson TX1 OEM Product Design Guide.***

When in the ON power state, Jetson TX1 has various design features to minimize the power when possible. These include such items as:

- Advanced Power Management IC (PMIC)
- On system Power Gating
- Advanced on chip Clock Gating
- Dynamic Voltage and Frequency Scaling (DVFS)
- Always on logic used to wake the system based on either a timer event or an external trigger (e.g., key press).
- Low power DRAM (LPDDR4)

2.4.2 OFF State

The OFF state is the default state when the system is not powered. It can only be entered from the ON state, through an OFF event. OFF Events are listed in the table below.

Table 5 OFF State Events

Event	Details	Preconditions
Power Button (10 second Press)	Keeping POWER_BTN# low for 7 seconds will power down the Jetson TX1	In ON State
SW Shutdown	SW will initiate	ON state, SW operational
Thermal Shutdown	If the internal temperature of Jetson TX1 reaches an unsafe temperature, the HW is designed to initiate a shutdown	Any power state
Voltage Brown out	A voltage monitor circuit is implemented on the Jetson TX1 module to indicate if the main DC input rail, VDD_IN, “droops” below an acceptable level. If VDD_IN drops below 5V, the HW initiates throttling the Tegra clocks to reduce power consumption.	Any power state

2.4.3 SLEEP State

The Sleep state can only be entered from the ON state. This state allows the Jetson TX1 to quickly resume to an operational state without performing a full boot sequence. In this state Jetson TX1 operates in low power with enough circuitry powered to allow the device to resume and re-enter the ON state. During this state the output signals from Jetson TX1 are maintained at their logic level prior to entering the state (i.e. they do not change to a 0V level).

The SLEEP state can only be entered directly by SW. For example, operating within an OS, with no operations active for a certain time can trigger the OS to initiate a transition to the SLEEP state.

To Exit the SLEEP state a WAKE event must occur. WAKE events can occur from within the Jetson TX1 or from external devices through various pins on the JETSON TX1 connector. A full list is given in the table below.

Table 6 SLEEP State Events

Event	Details
RTC WAKE up	Timers within Jetson TX1 can be programmed, on SLEEP entry. When these expire they will create a WAKE event to exit the SLEEP state.
Thermal Condition	If the JETSON TX1 internal temperature exceeds programmed hot and cold limits the system will be forced to wake up, so it can report and take appropriate action (shut down for example)
Low VDD_IN	If VDD_IN voltage drops below 6V then the system can be woken up to initiate a graceful shutdown.
USB VBUS detection	If VBUS is applied to the system (USB cable attached) then the device can be configured to Wake and enumerate
SD Card detect	The Card detect pin may be configured to enable the system to wake.
On Jetson TX1 WIFI Wake	Wifi can be configured to Wake up the system
On Jetson TX1 Bluetooth Wake	Bluetooth events can also trigger a system Wake
Jetson TX1 connector Interface WAKE signal	There are 16 signals on the Jetson TX1 connector. These are listed in the table below.

Table 7 Programmable Interface Wake Event

Event	Jetson TX1 Pin Assigned	Wake #
Audio Interrupt	GPIO20_AUD_INT	4
External BT Wake Request to AP	GPIO13_BT_WAKE_AP	10
External WiFi Wake Request to AP	GPIO10_WIFI_WAKE_AP	11
Modem to AP Ready	GPIO17_MDM2AP_READY	14
Modem Coldboot Alert	GPIO18_MDM_COLDBOOT	15
HDMI CEC	HDMI_CEC	19
GPIO Exapander 0 Interrupt	GPIO_EXP0_INT	21
Power Button On	POWER_BTN#	24
Charging Interrupt	CHARGING#	26
Sleep Request from Carrier Board	SLEEP#	27
Ambient/Proximity Interrupt	GPIO8_ALS_PROX_INT	32
HDMI Hot Plug Detect	DP1_HPD	53
Battery Low Warning	BATLOW#	57
Primary Modem Wake Request to AP	GPIO16_MDM_WAKE_AP	61
Touch Controller Interrupt	GPIO6_TOUCH_INT	62
Motion Sensor Interrupt	GPIO9_MOTION_INT	63

2.5 Thermal Management

Jetson TX1 is designed to operate under various workloads, and environmental conditions. It has been designed so that an active or passive heat sinking solution can be attached. The module contains various methods through hardware and software to limit the internal temperature to within operating limits. More details can be found in the Thermal design guide.

2.6 Clocks

The Jetson TX1 module requires no external clocks for operation, all system clocks are generated within the module. This includes a low power 32.768KHz clock for real-time operation.

The following clocks are provided by the Jetson TX1 module for use with the peripheral interfaces: AUDIO_MCLK, TOUCH_CLK, SPI0_CLK, SPI1_CLK, SPI2_CLK, CAM0_MCLK, CAM1_MCLK.

2.7 WiFi Power States

Jetson TX1 integrates a 5G WiFi 802.11ac Client. The following power states are available

2.7.1 STA Mode

- PM0

  No power save, always on.

- PM1

  Legacy 802.11 powersave. STA must indicate to the AP that it is entering into powersave by setting the PM bit in a data packet. Upon acknowledgement from the AP it can go into powersave. STA must wake up periodically (at period=DTIM) to check AID in the TIM map. If AID is set, STA will use a PS-Poll packet to fetch buffered packets (one PS-Poll per buffered packet). This is an inefficient mechanism as the traffic will tend to be bursty.

- PM2

  Vendor implementation. In PM2 mode, whenever there is a traffic (either Tx or Rx), the DUT will come out of powersave and remain there until packet exchanges have ceased for a minimum idle period (typically 200ms). When there is traffic, PM2 will operate nearly as well as PM0 mode, with almost no PS related latency. When there is no traffic, PM2 will be similar to PM1 powersave.

2.7.2 P2P Group-owner Powersave States

- Opportunistic power save (OPS)

  OPS allows the P2P Group Owner to save power when all associated clients are in a sleep state. P2P Power Management protocol defines an availability period “CTWindow” (Client Traffic Window), during which a P2P Group Owner is present. P2P Clients are allowed to transmit during CTWindow period. If at the end of the CTWindow all associated P2P Clients are in a sleep state, the P2P Group Owner is permitted to sleep until the next Beacon time. However, if any P2P Client remains in active mode at the end of the CTWindow the P2P Group Owner must remain awake until the next Beacon time.

- Notice-of-Absence

  NoA is similar to the Opportunistic Power Save protocol. For NoA, GO defines absence periods with a signaling element included in Beacon frames and Probe Responses containing

2.8 Bluetooth Power States

The integrated a Bluetooth controller includes the following power states:

- Active

  This is the default state. No power savings.

- LP

  This is the power saving state. The BT chip will go into low power mode, and will wake on traffic.

To change the mode: Assert/deassert the ext_wake GPIO to put the chip in Active or LP mode.

The BT controller also includes a wake-on-BT function. When it receives data, the chip will assert Host_wake GPIO. The AP, depending on its state, can treat it as a wake interrupt or info GPIO.

2.9 Ethernet

The Ethernet device used on the Jetson TX1 module contains many power saving features. Refer to the device datasheet for more details.

3.0 Interface and Signal Descriptions

3.1 SD/eMMC Controller

Standard	Notes
SD Specifications Part A2 SD Host Controller Standard Specification Version 4.00	
SD Specifications Part 1 Physical Layer Specification Version 4.00	
SD Specifications Part E1 SDIO Specification Version 4.00	Support for SD 4.0 Specification without UHS-II
Embedded Multimedia Card (e•MMC), Electrical Standard 5.1	

The SecureDigital (SD)/Embedded MultiMediaCard (eMMC) controller is capable of interfacing to SD/eSD, SDIO cards, and eMMC devices. It has a direct memory interface and is capable of initiating data transfers between memory and external card. The SD/eMMC controller supports 2 different bus protocols: SD and eMMC bus protocol for eMMC. It has an APB Slave interface to access configuration registers. To access the iRAM for Micro Boot, the SD/eMMC controller relies on the AHB redirection arbiter in the Memory Controller.

Features:

- Supports of 8-bit data interface for eMMC/eSD cards
- Supports 4-bit data interface for SD cards
- Allows card to interrupt host in 1-bit, 4-bit, 8-bit SD modes.
- Supports Read wait Control, Suspend/Resume operation for SDIO cards
- Supports FIFO overrun and underrun condition by stopping SD clock
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TB.

Jetson TX1 provides two instances of this controller: The SDCARD interface is intended for supporting an SD Card socket & the SDIO interface is available to support various compatible peripherals, such as a secondary Wi-Fi/BT controller. The SD/SDIO controllers support Default and High Speed modes as well as the High and Low voltage ranges.

Table 8 SD/MMC Controller I/O Capabilities

Controller	Bus Width	Supported Voltages (V)	I/O bus clock (MHz)	Maximum Bandwidth (MBps)	Notes
SDCARD	4	1.8	208	104	
SDIO	4	1.8	208	104	

Table 9 SD/SDIO Signal Descriptions

Signal Name	Type	Description
SDCARD_CLK, SDIO_CLK	Output	SD/SDIO/MMC Clock
SDCARD_CMD, SDIO_CMD	Bidirectional	SD/SDIO/MMC Command
SDCARD_DAT[3:0], SDIO_DAT[3:0]	Bidirectional	SD/SDIO/MMC Data bus
SDCARD_WP	Input	SD Write Protect
SDCARD_CD#	Input	SD Card Detect

3.2 Serial ATA (SATA) Controller

Standard	Notes
Serial ATA Revision 3.1	Including all errata, ENC, and TP, except DHU (direct head unload)
Serial ATA Advanced Host Controller Interface (AHCI) Specification, Rev 1.3.1	

The SATA controller enables a control path from Jetson TX1 to an external SATA device. A SSD / HDD / ODD drive can be connected. Controller can support the maximum throughput of a Gen 2 drive.

Features:

- Port multiplier support
  - Command based switching (CBS)
- Supported Cables and connectors
  - Standard internal connector
  - Internal micro connector
  - Internal slimline connector
  - mSATA connector
  - BGA SSD interface
  - Not supported: External connector (eSATA), USM, Internal LIF-SATA

See the ***Jetson TX1 OEM Product Design Guide*** for supported USB 3.0/PCIe/SATA configurations and connection examples.

Table 10 SATA Signal Descriptions

Signal Name	Type	Description
SATA_RX+/–	Input	Receive data, differential analog input
SATA_TX+/–	Output	Transmit data, differential analog output

3.3 Display Interfaces

The Jetson TX1 Display Controller Complex integrates two MIPI-DSI interfaces and two Serial Output Resources (SOR) to collect pixels from the output of the display pipeline, format/encode them to desired format, and then streams to various output devices. The SOR consists of several individual resources which can be used to interface with different display devices such as HDMI, DP or eDP.

3.3.1 MIPI Display Serial Interface (DSI)

The Display Serial Interface (DSI) is a serial bit-stream replacement for the parallel MIPI DPI and DBI display interface standards. DSI reduces package pin-count and I/O power consumption. DSI support enables both display controllers to connect to an external display(s) with a MIPI DSI receiver. The DSI transfers pixel data from the internal display controller to an external third-party LCD module.

Features:

- PHY Layer
  - Start / End of Transmission. Other out-of-band signaling
  - Per DSI interface: 1 Clock Lane; up to 4 Data Lanes
  - Supports link configuration – 1x4, 2x4

- Supports dual link operation in 2x4 configurations for asymmetrical/symmetrical split in both left-right side or odd-even group split schemes.
- DSC link compression
- Maximum link rate 1.5Gbps as per MIPI D-PHY 1.1v version
- Maximum 10MHz LP receive rate

- Lane Management Layer with Distributor
- Protocol Layer with Packet Constructor
- Supports MIPI DSI 1.0.1v version mandatory features
- Command Mode (One-shot) with Host and/or display controller as master
- Clocks
  - Bit Clock : Serial data stream bit-rate clock
  - Byte Clock : Lane Management Layer Byte-rate clock
  - Application Clock: Protocol Layer Byte-rate clock.
- Error Detection / Correction
  - ECC generation for packet Headers
  - Checksum generation for Long Packets
- Error recovery
- High Speed Transmit timer
- Low Power Receive timer
- Turnaround Acknowledge Timeout

Table 11 DSI Signal Descriptions

Name	Type	Description
DSI_0_CLK_N, DSI_0_CLK_P DSI_2_CLK_N, DSI_2_CLK_P	Output	Differential output clock for up to two 1x4 DSI interfaces
DSI_0_D[1:0]_N, DSI_0_D[1:0]_P DSI_1_D[1:0]_N, DSI_1_D[1:0]_P DSI_2_D[1:0]_N, DSI_2_D[1:0]_P DSI_3_D[1:0]_N, DSI_3_D[1:0]_P	Bidirectional	Differential data lanes for DSI interfaces. DSI_0_D[1:0] & DSI_1_D[1:0] are associated with DSI_0_CLK. DSI_2_D[1:0] & DSI_3_D[1:0] are associated with DSI_2_CLK

3.3.2 High-Definition Multimedia Interface (HDMI) and DisplayPort (DP) Interfaces

Standard	Notes
High-Definition Multimedia Interface (HDMI) Specification, version 2.0	> 340MHz pixel clock Scrambling support Clock/4 support (1/40 bit-rate clock)
High-bandwidth Digital Content Protection (HDCP) System Specification, version 2.2	
High-bandwidth Digital Content Protection (HDCP) System Specification, version 1.3	

The HDMI and DP interfaces share the same set of interface pins. A new transport mode was introduced in HDMI 2.0 to enable link clock frequencies greater than 340MHz and up to 600MHz.

Features:

- On-chip HDCP key storage, no external Secure ROM required
- Support for both HDCP 1.3 and HDCP 2.2

- HDMI
  - HDMI 2.0 mode (3.4Gbps < data rate <= 6Gbps)
  - HDMI 1.4 mode (data rate<=3.4Gbps)
  - Multi-channel audio from HDA controller, up to 8 channels 192kHz 24-bit.
  - Vendor Specific Info-frame (VSI) packet transmission
  - 24-bit RGB pixel formats
  - Transition Minimized Differential Signaling (TMDS) functional up to 340MHz pixel clock rate

Table 12 HDMI Signal Descriptions

Signal Name	Type	Description
DP1_TX3+ DP1_TX3–	Output	HDMI Differential Clock. AC coupling & pull-downs (with disble) required on Carrier board.
DP1_TX[2:0]+ DP1_TX[2:0]–	Output	HDMI/DP Differential Data. AC coupling & pull-downs (with disble) required on Carrier board. DP1_TX0 = HDMI TXD2 DP1_TX1 = HDMI TXD1 DP1_TX2 = HDMI TXD0
DP1_HPD	Input	Interrupt. Used for Hot Plug detection. Level shifter required as this pad is not 5V tolerant
HDMI_CEC	Bidirectional	Consumer Electronics Control (CEC) one-wire serial bus. NVIDIA provides low level CEC APIs (read/write). These are not supported in earlier Android releases. For additional CEC support, 3rd party libraries need to be made available.
DP1_AUX_CH+ (DDC_SCL)	Output	DDC Serial Clock. Level shifter required; pad is not 5V tolerant.
DP1_AUX_CH– (DDC_SDA)	Bidirectional	DDC Serial Data. Level shifter required; pad is not 5V tolerant.

Table 13 DP Signal Descriptions

Signal Name	Type	Description
DP1_TX[3:0]+ DP1_TX[3:0]–	Output	DP Differential Lanes. AC coupling required on Carrier board.
DP1_HPD	Input	Interrupt. Used for Hot Plug detection.
DP1_AUX_CH+ DP1_AUX_CH–	Bidirectional	DP auxiliary channel. AC coupling required on Carrier board.

3.3.3 Embedded DisplayPort (eDP) Interface

Standard	Notes
Embedded DisplayPort 1.4	Supported eDP 1.4 features: ▪ Additional link rates ▪ Enhanced framing ▪ Power sequencing ▪ Reduced aux timing ▪ Reduced main voltage swing

eDP is a mixed-signal interface consisting of 4 differential serial output lanes and 1 PLL. This PLL is used to generate a high frequency bit-clock from an input pixel clock enabling the ability to handle 10-bit parallel data per lane at the pixel rate for the desired mode. Embedded DisplayPort (eDP) modes (1.6GHz for RBR, 2.16GHz, 2.43GHz, 2.7GHz for HBR, 3.42GHz, 4.32GHz and 5.4GHz for HBR2).

NOTE: eDP has been tested according to DP1.2b PHY CTS even though eDPv1.4 supports lower swing voltages and additional intermediate bit rates. This means the following nominal voltage levels (400mV, 600mV, 800mV, 1200mV) and data rates (RBR, HBR, HBR2) are tested. This interface can be tuned to drive lower voltage swings below 400mV and can be programmed to other intermediate bit rates as per the requirements of the panel and the system designer.

The eDP block collects pixels from the output of the display pipeline, formats/encodes them to the eDP format, and then streams them to various output devices. It drives local panels only (does not support an external DP port), includes a small test pattern generator and CRC generator.

Table 14 eDP Signal Descriptions

Signal Name	Type	Description
DP0_TX[3:0]+ DP0_TX[3:0]–	Output	eDP Differential lanes
DP0_HPD	Input	eDP hot-plug detect
DP0_AUX_CH+ DP0_AUX_CH–	Bidirectional	eDP Auxiliary channel

3.4 Audio Interfaces

The I2S controller transports streaming audio data between system memory and an audio codec. The I2S controller supports I^2S format, Left-justified Mode format, Right-justified Mode format, and DSP mode format, as defined in the Philips inter-IC-sound (I^2S) bus specification.

The I2S and PCM (master and slave modes) interfaces support clock rates up to 24.5760MHz.

The I2S controller supports point-to-point serial interfaces for the I^2S digital audio streams. I^2S-compatible products, such as compact disc players, digital audio tape devices, digital sound processors, and those with digital TV sound may be directly connected to the I^2S controller. The controller also supports the PCM and telephony mode of data-transfer. Pulse-Code-Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. The Telephony mode is used to transmit and receive data to and from an external mono CODEC in a slot-based scheme of time-division multiplexing (TDM). The I2S controller supports bidirectional audio streams and can operate in half-duplex or full-duplex mode.

Features:

- Basic I2S modes to be supported (I2S, RJM, LJM and DSP) in both Master and Slave modes.
- PCM mode with short (one-bit-clock wide) and long-fsync (two bit-clocks wide) in both master and slave modes.
- NW-mode with independent slot-selection for both Tx and Rx
- TDM mode with flexibility in number of slots and slot(s) selection.

- Capability to drive-out a High-z outside the prescribed slot for transmission
- Flow control for the external input/output stream.

Table 15 I2S Signal Descriptions

Signal Name	Type	Description
I2S[3:0]_LRCK	Bidirectional	Frame Sync/Word Select. Supports I2S/PCM audio. Interface can be master or slave
I2S[3:0]_CLK	Bidirectional	Serial Clock/Bit Clock. Supports I2S/PCM audio. Interface can be master or slave
I2S[3:0]_SDIN	Input	Data In. Supports I2S/PCM audio. Interface can be master or slave.
I2S[3:0]_SDOUT	Bidirectional	Data Out. Supports I2S/PCM audio. Interface can be master or slave.

3.5 USB Interfaces

Standard	Notes
Universal Serial Bus Specification Revision 3.0	Refer to specification for related interface timing details.
Universal Serial Bus Specification Revision 2.0	USB Battery Charging Specification, version 1.0; including Data Contact Detect protocol Modes: Host and Device Speeds: Low, Full, and High Refer to specification for related interface timing details.
Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0	Refer to specification for related interface timing details.

See the ***Jetson TX1 OEM Product Design Guide*** for supported USB 3.0/PCIe/SATA configurations and connection examples.

Table 16 USB Signals

Signal (Pin Name if different)	Type	Description
USB[2:0]_D–	Analog	USB Data Negative (USB 2.0 interfaces)
USB[2:0]_D+	Analog	USB Data Positive (USB 2.0 interfaces)
USB_SS1_RX–	Input	USB 3.0 #1: Receive Data Negative input
USB_SS1_RX+	Input	USB 3.0 #11: Receive Data Positive input
USB_SS1_TX–	Output	USB 3.0 #1: Transmit Data Negative output
USB_SS1_TX+	Output	USB 3.0 #1: Transmit Data Positive output
USB_SS2_RX– (PEX1_RX– or PEX3_RX–)	Input	USB 3.0 #2 options: Receive Data Negative input
USB_SS2_RX+ (PEX1_RX+ or PEX3_RX+)	Input	USB 3.0 #2 options: Receive Data Positive input
USB_SS2_TX– (PEX1_TX– or PEX3_TX–)	Output	USB 3.0 #2 options: Transmit Data Negative output
USB_SS2_TX+ (PEX1_TX+ or PEX3_TX+)	Output	USB 3.0 #2 options: Transmit Data Positive output
USB_SS3_RX– (SATA_RX–)	Input	USB 3.0 #3 option: Receive Data Negative input
USB_SS3_RX+ (SATA_RX+)	Input	USB 3.0 #3 option: Receive Data Positive input
USB_SS3_TX– (SATA_TX–)	Output	USB 3.0 #3 option: Transmit Data Negative output
USB_SS3_TX+ (SATA_TX+)	Output	USB 3.0 #3 option: Transmit Data Positive output

Note: USB_SS0 interface is not available at the connector; it is used for the Gigabit Ethernet controller on Jetson TX1.

3.6 PCI Express (PCIe) Interface

Standard	Notes
PCI Express Base Specification Revision 2.0	Jetson TX1 meets the timing requirements for the Gen2 (5.0 GT/s) data rates. Refer to specification for complete interface timing details. Although NVIDIA validates that the Jetson TX1 design complies with the PCIe specification, PCIe software support may be limited.

Jetson TX1 integrates a x5 lane PCIe bridge to enable a control path from Jetson TX1 to external PCIe devices. Two PCIe Gen2 controllers (one x4, one x1) support connections to one or two endpoints.

NOTE: Upstream Type 1 Vendor Defined Messages (VDM) should be sent by the Endpoint Port (EP) if the Root Port (RP) also belongs to same vendor/partner; otherwise the VDM will be silently discarded.

See the ***Jetson TX1 OEM Product Design Guide*** for supported USB 3.0/PCIe/SATA configurations and connection examples.

Table 17 PCIe Signal Descriptions

Signal Function (Pin Name)	Type	Description
PEX_WAKE#	Input	PCI Express Wake This signal is used as the PCI Express defined WAKE# signal. When asserted by a PCI Express device, it is a request that system power be restored. No interrupt or other consequences result from the assertion of this signal.
PCIe Controller #0		
PEX0_REFCLK+/–	Output	Differential Reference Clocks. PEX0_REFCLK is associated with PCIe Controller #0.
PEX2_RX+/– (Lane 3) PEX_RFU_RX+/– (Lane 2) USB_SS1_RX+/– (Lane 1) PEX0_RX+/– (Lane 0)	Input	Differential Receive Data Lanes, associated with PCIe Controller #0.
PEX2_TX+/– (Lane 3) PEX_RFU_TX+/– (Lane 2) USB_SS1_TX+/– (Lane 1) PEX0_TX+/– (Lane 0)	Output	Differential Transmit Data Lanes, associated with PCIe Controller #0.
PEX0_CLKREQ#	Bidirectional	PCI Express Reference Clock Request This signal is used by a PCI Express device to indicate it needs the PEX_REFCLKP and PEX_REFCLKN to actively drive reference clock. PEX0_CLKREQ# is associated with PCIe Controller #0.
PEX0_RST#	Output	PCI Express Reset This signal provides a reset signal to all the PCI Express links. It must be asserted 100 ms after the power to the PCI Express slots has stabilized. PEX0_RST# is associated with PCIe Controller #0.
PCIe Controller #1		
PEX1_REFCLK+/–	Output	Differential Reference Clocks. PEX1_REFCLK is associated with PCIe Controller #1.
PEX1_RX+/–	Input	Differential Receive Data Lane, associated with PCIe Controller #1.
PEX1_TX+/–	Output	Differential Transmit Data Lane, associated with PCIe Controller #1.
PEX1_CLKREQ#	Bidirectional	PCI Express Reference Clock Request This signal is used by a PCI Express device to indicate it needs the PEX_REFCLKP and PEX_REFCLKN to actively drive reference clock. PEX0_CLKREQ# is associated with PCIe Controller #1.
PEX1_RST#	Output	PCI Express Reset This signal provides a reset signal to all the PCI Express links. It must be asserted 100 ms after the power to the PCI Express slots has stabilized. PEX0_RST# is associated with PCIe Controller #1.

3.7 Serial Peripheral Interface

The SPI controllers operate up to 65 Mbps in master mode and 45 Mbps in slave mode. It allows a duplex, synchronous, serial communication between the controller and external peripheral devices. It consists of 4 signals, SS_N (Chip select), SCK (clock), MOSI (Master data out and Slave data in) and MISO (Slave data out and master data in). The data is transferred on MOSI or MISO based on the data transfer direction on every SCK edge. The receiver always receives the data on the other edge of SCK.

Features:

- Independent RX FIFO and TX FIFO.
- Software controlled bit-length supports packet sizes of 1 to 32 bits.
- Packed mode support for bit-length of 7 (8-bit packet size) and 15 (16-bit packet size).
- SS_N can be selected to be controlled by software, or it can be generated automatically by the hardware on packet boundaries.
- Receive compare mode (controller listens for a specified pattern on the incoming data before receiving the data in the FIFO).
- Simultaneous receive and transmit supported
- Supports Master mode. Slave mode has not been validated

Table 18 SPI Signal Descriptions

Signal Name	Type	Description
SPI[2:1]_CS[1:0]# SPI0_CS0_N	Bidirectional	Chip Select options for SPI[2:1]: Depending on pin multiplexing, there may be one or more chip select options for each SPI interface. Multiple available chip selects can be used to differentiate between two or more SPI slave devices
SPI[2:0]_MISO	Bidirectional	Master In / Slave Out.
SPI[2:0]_MOSI	Bidirectional	Master Out / Slave In.
SPI[2:0]_CLK	Bidirectional	Serial Clock: Clock phase and polarity is programmable.

Figure 5 SPI Master Timing Diagram

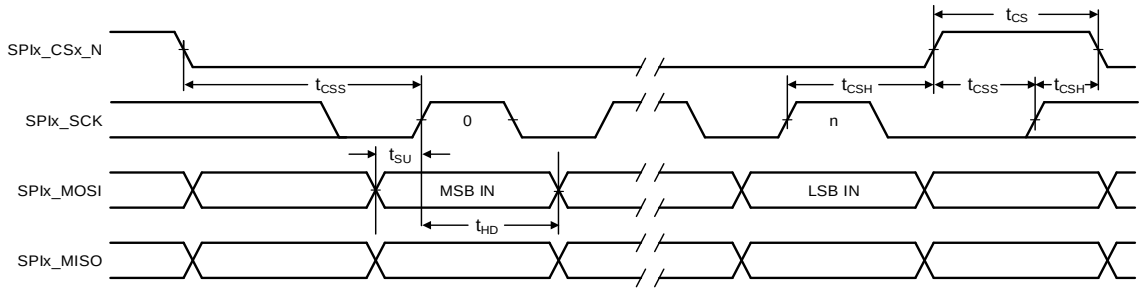


Table 19 SPI Master Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
Fsck	SPIx_SCK clock frequency			65	MHz
Psck	SPIx_SCK period	1/Fsck			ns
t_{CH}	SPIx_SCK high time	50%Psck -10%		50%Psck +10%	ns
t_{CL}	SPIx_SCK low time	50%Psck -10%		50%Psck +10%	ns
t_{CRT}	SPIx_SCK rise time (slew rate)	0.1			V/ns
t_{CFT}	SPIx_SCK fall time (slew rate)	0.1			V/ns
t_{SU}	SPIx_MOSI setup to SPIx_SCK rising edge	2			ns
t_{HD}	SPIx_MOSI hold from SPIx_SCK rising edge	3			ns
t_{CSS}	SPIx_CSx_N setup time	2			ns
t_{CSH}	SPIx_CSx_N hold time	3			ns
t_{CS}	SPIx_CSx_N high time	10			ns

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

Figure 6 SPI Slave Timing Diagram

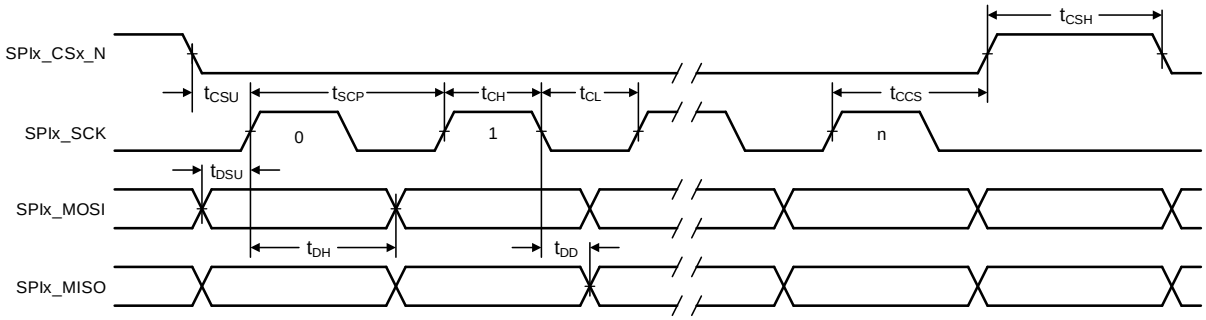


Table 20 SPI Slave Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCP}	SPIx_SCK period	$2*(t_{SDD}+ t_{MSU}$[1]$)$			ns
t_{SCH}	SPIx_SCK high time	$t_{SDD} + t_{MSU}$[1]			ns
t_{SCL}	SPIx_SCK low time	$t_{SDD} + t_{MSU}$[1]			ns
t_{SCSU}	SPIx_CSx_n setup time	1			t_{SCP}
t_{SCSH}	SPIx_CSx_n high time	1			t_{SCP}
t_{SCCS}	SPIx_SCK rising edge to SPIx_CSx_n rising edge	1		1	t_{SCP}
t_{SDSU}	SPIx_MOSI setup to SPIx_SCK rising edge	1		1	ns
t_{SDH}	SPIx_MOSI hold from SPIx_SCK rising edge	2		11	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT1[2])	3.5		16	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT2[2])	3		13	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT3[2])	4		17	ns

1. t_{MSU} is the setup time required by the external master
2. ALT1/2/3 refers to the position of the SPI pins in the Signal Pinout Multiplexing tables in Section 3.1, *Signal List and Multiplexing Functions*.

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

3.8 Inter-Chip Communication (I2C) Controller

Standard	Notes
NXP inter-IC-bus (I^2C) specification	

The I2C controller implements an I^2C-bus specification compliant I2C master and a slave controller. The I2C controller supports multiple masters and slaves in: Standard-mode (up to 100Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1Mbit/s) and High-speed mode (up to 3.4Mbit/s) of operations. A general purpose I2C controller allows system expansion for I2C-based devices, such as AM/FM radio, remote LCD display, serial ADC/DAC, and serial EPROMs, as defined in the NXP inter-IC-bus (I^2C) specification. The I2C bus supports serial device communications to multiple devices. The I2C controller handles bus mastership with arbitration, clock source negotiation, speed negotiation for standard and fast devices, and 7-bit and 10-bit slave address support according to the I2C protocol and supports master and slave mode of operation.

Table 21 I2C Usage

Interface (Balls) name	Target Application	On-Jetson TX1 Termination
I2C_GP0_CLK/DAT	Various	1KΩ on Jetson TX1 to 1.8V
I2C_GP1_CLK/DAT	Power Monitors	1KΩ on Jetson TX1 to 3.3V
I2C_PM_CLK/DAT	Camera	1KΩ on Jetson TX1 to 1.8V
I2C_CAM_CLK/DAT	Camera & Camera related functions	1KΩ on Jetson TX1 to 1.8V
DP1_AUX_CH+/- (see note)	Display: HDMI/DP (DDC)	None
DP0_AUX_CH+/- (see note)	Display: eDP	None

Note: See Display section for additional information for DP[1:0]_AUX_CH+/-

Table 22 I2C Signal Descriptions

Signal Name	Type	Description
I2C_GP[1:0]_CLK I2C_PM_CLK I2C_CAM_CLK	Bidirectional	Serial Clock for I2C interfaces.
I2C_GP[1:0]_DAT I2C_PM_DAT I2C_CAM_DAT	Bidirectional	Serial Data for I2C interfaces.

3.9 UART Controller

UART controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be checked by the receiver for any transmission bit errors.

NOTE: The UART receiver input has low baud rate tolerance in 1-stop bit mode. External devices must use 2 stop bits. In 1-stop bit mode, the Tegra UART receiver can lose sync between Tegra receiver and the external transmitter resulting in data errors/corruption. In 2-stop bit mode, the extra stop bit allows the Tegra UART receiver logic to align properly with the UART transmitter.

Features:

- Synchronization for the serial data stream with start and stop bits to transmit data and form a data character
- Supports both 16450- and 16550-compatible modes. Default mode is 16450
- Device clock up to 200MHz, baud rate of 12.5Mbits/second

- Data integrity by attaching parity bit to the data character
- Support for word lengths from five to eight bits, an optional parity bit and one or two stop bits
- Support for modem control inputs
- DMA capability for both TX and RX
- 8-bit x 36 deep TX FIFO
- 11-bit x 36 deep RX FIFO. 3 bits of 11 bits per entry will log the RX errors in FIFO mode (break, framing and parity errors as bits 10,9,8 of FIFO entry)
- Auto sense baud detection
- Timeout interrupts to indicate if the incoming stream stopped
- Priority interrupts mechanism
- Flow control support on RTS and CTS
- Internal loopback
- SIR encoding/decoding (3/16 or 4/16 baud pulse widths to transmit bit zero)

Table 23 UART Signal Descriptions

Function	Type	Description
UART[2:0]_TX	Output	UART Transmit
UART[2:0]_RX	Input	UART Receive
UART[2:0]_CTS#	Input	UART Clear-to-send
UART[2:0]_RTS#	Output	UART Request-to-send

3.10 Video Input Interfaces

3.10.1 MIPI Camera Serial Interface (CSI)

Standard	Notes
MIPI CSI 2.0 Receiver specification	
MIPI D-PHY® v1.2 Physical Layer specification	

The Jetson TX1 module incorporates three MIPI CSI x4 blocks supporting a variety of device types and camera configurations. The Camera Serial Interface (CSI) is based on MIPI CSI 2.0 standard specification and implements the CSI receiver which receives data from an external camera module with a CSI transmitter.

Features:

- Supported camera configurations:
  - 1 x4: single camera with a 4 lane sensor using any one of three MIPI x4 blocks.
  - 2 x4: stereo pair with 4 lanes for each camera using any pair of three MIPI x4 blocks.
  - 2 x2: dual camera mode, breaking up any MIPI x4 block to two x2 sub blocks; can support up to 6 camera streams simultaneously.
- Supported input data formats:
  - RGB: RGB888, RGB666, RGB565, RGB555, RGB444
  - YUV: YUV422-8b, YUV420-8b (legacy), YUV420-8b, YUV444-8b
  - RAW: RAW6, RAW7, RAW8, RAW10, RAW12, RAW14

- DPCM: user defined
- User defined: JPEG8
- Embedded: Embedded control information

- Supports single-shot mode
- Physical Interface (MIPI D-PHY) Modes of Operation
  - High Speed Mode – High speed differential signaling up to 1.5Gbps; burst transmission for low power
  - Low Power Control – Single-ended 1.2V CMOS level. Low speed signaling for handshaking.
  - Low Power Escape –Low speed signaling for data, used for escape command entry only. 20Mbps

If the two streams come from a single source, then the streams are separated using a filter indexed on different virtual channel numbers or data types. In case of separation using data types, the normal data type is separated from the embedded data type. Since there are only two pixel parsers, virtual channel and embedded data capability cannot be used at the same time.

Table 24 CSI Signal Descriptions

Signal Name	Type	Description
CSI_[5:0]_CLK_N CSI_[5:0]_CLK_P	Input	Differential CSI clock
CSI_[5:0]_D[1:0]_N CSI_[5:0]_D[1:0]_P	Input	Differential CSI data lanes. Each data pair can be associated with a different camera, or CSI_[1:0]_D[1:0], CSI_[3:2]_D[1:0], CSI_[5:4]_D[1:0] can be used to interface with quad-lane cameras.

3.10.2 Camera / VI (Video Input)

The Video Input (VI) block receives data from the CSI receiver and prepares it for presentation to system memory or the dedicated image signal processor (ISP) execution resources. The VI block provides formatting for RGB, YCbCr, and raw Bayer data in support of a number of camera user models. These models include single and multi-camera systems, which may have up to six active streams. The input streams are obtained from MIPI compliant CMOS sensor camera modules.

Table 25 Camera Clock & Control Signal Descriptions

Signal Name	Type	Description
I2C_CAM_CLK	Bidirectional	See I2C section
I2C_CAM_DAT	Bidirectional	See I2C section
CAM[1:0]_MCLK	Output	Video Input Master clocks for primary & secondary cameras
GPIO1_CAM1_PWR# GPIO0_CAM0_PWR#	Bidirectional	Camera Power Control signals: Connect to powerdown pins on camera(s). Available for use as general purpose I/Os.
GPIO5_CAM_FLASH_EN	Output	Camera Flash Enable: Connect to enable of flash circuit. Available for use as general purpose I/O.
GPIO3_CAM1_RST# GPIO2_CAM0_RST#	Output	Camera Resets: Used for camera module resets. If AutoFocus Enable is required, GPIO3_CAM1_RST# to AF_EN pin on camera module & use GPIO2_CAM0_RST# as common reset line. Available for use as general purpose I/Os.

3.11 Miscellaneous Interfaces

3.11.1 Debug

Jetson TX1 has an optional JTAG interface that can be used for SCAN testing or for communicating with either integrated CPU.

Table 26 Debug Signal Descriptions

Signal Name	Type	Description
JTAG_RTCK	Output	Return Test Clock
JTAG_TCK	Input	Test Clock
JTAG_TDI	Input	Test Data In
JTAG_TDO	Output	Test Data Out
JTAG_TMS	Input	Test Mode Select
JTAG_TRST#	Input	Test Reset

3.11.2 Pulse Width/Frequency Modulation (PWFM)

The Pulse Width Frequency Modulator (PWFM) is a frequency divider with a varying pulse width. The PWFM runs off a device clock programmed in the Clock and Reset controller, and can be any frequency up to the device clock maximum speed of 48MHz. The PWFM gets divided by 256 before being subdivided based on a programmable value. Two PWM signals are available on Jetson TX1 pins. One is intended for LCD contrast and brightness control and another for fan speed control.

Table 27 PWFM Signal Descriptions

Signal Name	Type	Description
LCD0_BKLT_PWM FAN_PWM	Output	LCD Backlight (PM3_PWM0) and FAN (PM3_PWM3) Pulse Width Frequency Modulation Signals. These output a frequency divided down from the device clock source and output a pulse of programmed width.

4.0 Pin Definitions

Jetson TX1 has pins that are multi-purpose digital I/O pads (MPIO). Each MPIO can be configured to act as a GPIO or it can be assigned for use by a particular I/O controller. Though each MPIO has up to 5 functions (GPIO function and up to 4 SFIO functions), a given MPIO can only act as a single function at a given point in time. The functions for each pin on Jetson TX1 is fixed to a single SFIO function or as a GPIO. The different MPIO pins share a similar structure, but there are several varieties of such pads. The varieties are designed to minimize the number of on-board components (such as level shifters or pull-up resistors) required in Jetson TX1 designs.

Jetson TX1 employs the following MPIO pads:

- ST (standard) pads are the most common pads on the chip. They are used for typical General Purpose I/O.
- DD (dual-driver) pads are similar to the ST pads. A DD pad can tolerate its I/O pin being pulled up to 3.3V (regardless of supply voltage) as long as the pad's output-driver is set to open-drain mode. There are special power-sequencing considerations when using this functionality.

  NOTE: The output of DD pads cannot be pulled High during deep-power-down (DPD).

- CZ (controlled output impedance) pads are optimized for use in applications requiring tightly controlled output impedance. They are similar to ST pads except for changes in the drive strength circuitry and in the weak pull-ups/-downs. CZ pads are included on the VDDIO_SDMMC1 and VDDIO_SDDMC3 power rails. Each of those rails also includes a pair of CZ_COMP pads. Circuitry within Jetson TX1 continually matches the output impedance of the CZ pads to the on-board pull-up/-down resistors attached to the CZ_COMP pads.
- LV_CZ (low voltage controlled impedance) pads are similar to CZ pads but are optimized for use with a 1.2V supply voltage (and signaling level). They support a 1.8V supply voltage (and signaling level) as a secondary mode. Jetson TX1 uses LV_CZ pads for SPI interfaces operating at 1.8V.
- DP_AUX pad is used as an Auxiliary control channel for the Display Port which needs differential signaling. Because the same I/O block is used for the Display Port and HDMI to ensure the control path to the display interface is minimized, the DP_AUX pads can operate in open-drain mode so that HDMI's control path (i.e., DDC interface which needs I2C) can also be used in the same pad.

Table 28 MPIO Pad Types

Pad Details	Pad Type				
	ST	**CZ**	**DD**	**LV_CZ**	**ST_EMMC**
IO rail voltage	1.8V	1.8V/3.3V	1.8V	1.8V	1.8V
Input Buffer	Schmitt & CMOS	Schmitt & CMOS	Schmitt & CMOS	Schmitt & CMOS	Schmitt & CMOS
Output Buffer	Push-pull	Push-pull	Push-pull & Open Drain	Push-pull	Push-pull
IO Voltage tolerance	1.8V	VDDIO	Open Drain: 3.3V Otherwise:VDDIO	1.8V	1.8V
Nominal Pull strength	100kΩ	18kΩ (PU)	100kΩ	15kΩ	15kΩ
"Slew Rate" control	No	2-bits up/down	No	2-bits up/down	3 bits up/down
Drive strength control	5-bits up/down	7-bits up/down	5-bits up/down	5-bits up/down	5 bits up/down
Per Pad Control					
PUPD	✓	✓	✓	✓	✓
Tristate_control	✓	✓	✓	✓	✓
DPD_PARKING_CONTROL	✓	✓	✓	✓	✓
E_INPUT	✓	✓	✓	✓	✓

Pad Details	Pad Type				
	ST	CZ	DD	LV_CZ	ST_EMMC
E_LPDR	✓		✓		
E_OD	✓		✓		
E_IO_HV			✓		
E_HSM		✓			
SCHMT	✓	✓	✓	✓	✓
DRV_TYPE[1:0]		✓		✓	

Each MPIO pad consists of:

- An output driver with tristate capability, drive strength controls and push-pull mode, open-drain mode, or both
- An input receiver with either schmitt mode, CMOS mode, or both
- A weak pull-up and a weak pull-down

MPIO pads are partitioned into multiple “pad control groups” with controls being configured for the group. During normal operation, these per-pad controls are driven by the pinmux controller registers. During deep sleep, the PMC bypasses and then resets the pinmux controller registers. Software reprograms these registers as necessary after returning from deep sleep.

Refer to the ***Tegra X1 (SoC) Technical Reference Manual*** for more information on modifying pad controls.

4.1 Power-on Reset Behavior

Each MPIO pad has a deterministic power-on reset (PoR) state. The particular reset state for each pad is chosen to minimize the need of on-board components like pull-up resistors in a Jetson TX1-based system. For example, the on-chip weak pull-ups are enabled during PoR for pads which are usually used to drive active-low chip selects.

The following list is a simplified description of the Jetson TX1 boot process focusing on those aspects which relate to the MPIO pins.

1. System-level hardware executes the power-up sequence. This sequence ends when system-level hardware releases SYS_RESET_N.
2. The boot ROM begins executing and programs the on-chip I/O controllers to access the secondary boot device.
3. The boot ROM fetches the Boot Configuration Table (BCT) and boot loader from the secondary boot device.
4. If the BCT and boot loader are fetched successfully, the boot ROM transfers control to the boot loader.
5. Otherwise, the boot ROM enters USB recovery mode.

4.2 Deep Sleep Behavior

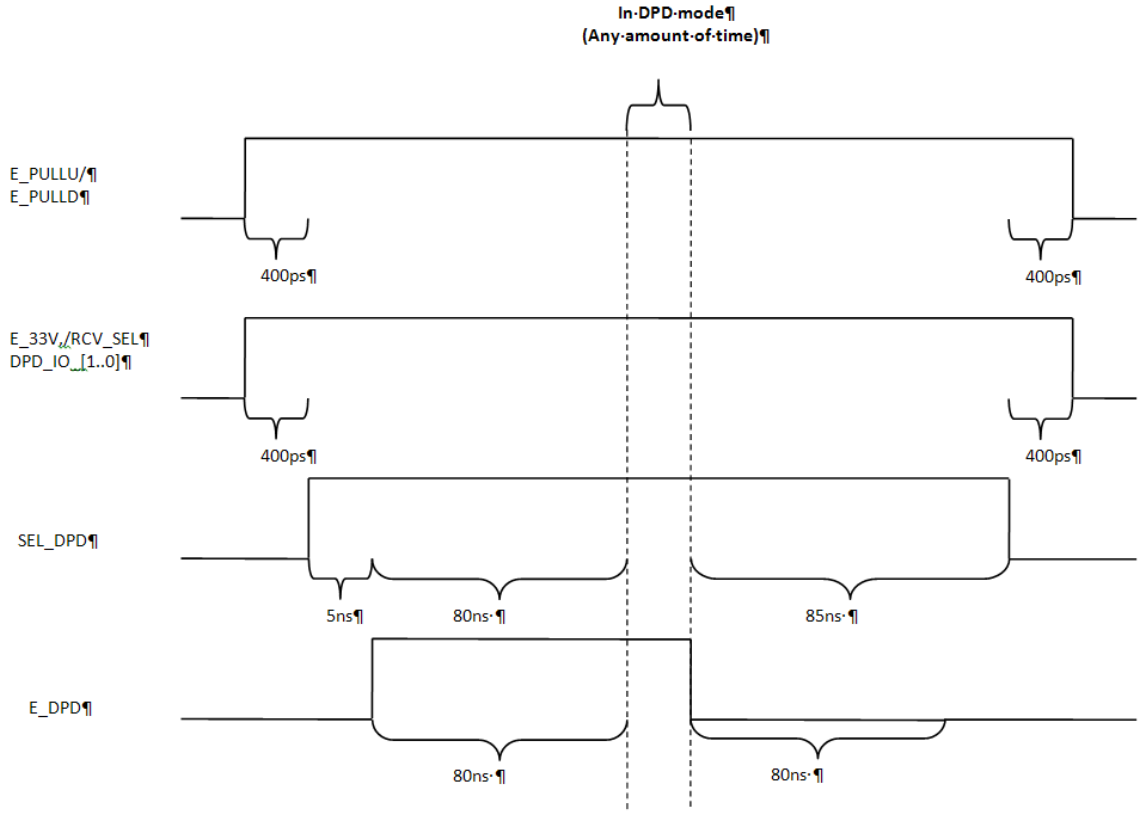
Deep Sleep is an ultra-low-power standby state in which the Jetson TX1 maintains much of its I/O state while most of the chip is powered off. The following lists offer a simplified description of the deep sleep entry and exit concentrating on those aspects which relate to the MPIO pads. During deep sleep most of the pads are put in a state called Deep Power Down (DPD). The sequence for entering to DPD is same across pads. Specific variations are there in some pads in terms of type of features that are available in DPD.

NOTE: The output of DD pads cannot be pulled High during deep-power-down (DPD).
OD pads do NOT retain their output during DPD. OD pads should NOT be configured as GPIOs in a platform where they are expected to hold a value during DPD.

ALL MPIO pads **do NOT** have identical behavior during deep sleep. They differ with regard to:

- Input buffer behavior during deep sleep
  - Forcibly disabled OR
  - Enabled for use as a “GPIO wake event” OR
  - Enabled for some other purpose (e.g., a “clock request” pin)
- Output buffer behavior during deep sleep
  - Maintain a static programmable (0, 1, or tristate) constant value OR
  - Capable of changing state (i.e., dynamic while the chip is still in deep sleep)
- Weak pull-up/pull-down behavior during deep sleep
  - Forcibly disabled OR
  - Can be configured
- Pads that do not enter deep sleep
  - Some of the pads whose outputs are dynamic during deep sleep are of special type and they do not enter deep sleep (e.g., pads that are associated with PMC logic do not enter deep sleep, pads that are associated with JTAG do not enter into deep sleep any time.

Figure 7 DPD Wait Times



4.3 GPIO Controller

The Jetson TX1 has multiple dedicated GPIOs. Each GPIO can be individually configurable as Output/Input/Interrupt sources with level/edge controls.

4.4 Pin Assignments

	A	B	C	D	E	F	G	H	
1	VDD_IN	VDD_IN	VDD_IN	RSVD	FORCE_RECOV#	AUDIO_MCLK	I2S0_SDIN	I2S0_LRCLK	1
2	VDD_IN	VDD_IN	VDD_IN	RSVD	SLEEP#	GPIO19_AUD_RST	I2S0_CLK	I2S0_SDOUT	2
3	GND	GND	GND	RSVD	SPI0_CLK	SPI0_CS0#	GND	GPIO20_AUD_INT	3
4	GND	GND	GND	RSVD	SPI0_MISO	SPI0_MOSI	RSVD	RSVD	4
5	RSVD	RSVD	RSVD	RSVD	I2S3_SDIN	I2S3_LRCLK	I2S2_CLK	I2S2_LRCLK	5
6	I2C_PM_CLK	I2C_PM_DAT	I2C_CAM_CLK	I2C_CAM_DAT	I2S3_CLK	I2S3_SDOUT	I2S2_SDIN	I2S2_SDOUT	6
7	CHARGING#	CARRIER_STBY#	BATLOW#	GPIO5_CAM_FLASH_EN	RSVD	GPIO1_CAM1_PWR#	GPIO4_CAM_STROBE	GPIO3_CAM1_RST#	7
8	GPIO14_AP_WAKE_MDM	VIN_PWR_BAD#	RSVD	RSVD	RSVD	CAM1_MCLK	GPIO0_CAM0_PWR#	GPIO2_CAM0_RST#	8
9	GPIO15_AP2MDM_READY	GPIO17_MDM2AP_READY	RSVD	UART1_TX	UART1_RTS#	CAM0_MCLK	UART3_CTS#	UART3_RX	9
10	GPIO16_MDM_WAKE_AP	GPIO18_MDM_COLDBOOT	RSVD	UART1_RX	UART1_CTS#	GND	UART3_RTS#	UART3_TX	10
11	RSVD	JTAG_TCK	RSVD	RSVD	RSVD	RSVD	UART0_RTS#	UART0_CTS#	11
12	JTAG_TMS	JTAG_TDI	RSVD	RSVD	RSVD	RSVD	UART0_RX	UART0_TX	12
13	JTAG_TDO	JTAG_GP0	RSVD	I2S1_LRCLK	SPI1_CS1#	SPI1_MOSI	SPI1_CLK	GPIO8_ALS_PROX_INT	13
14	JTAG_RTCK	GND	I2S1_SDIN	I2S1_SDOUT	SPI1_CS0#	SPI1_MISO	GPIO9_MOTION_INT	SPI2_CLK	14
15	UART2_CTS#	UART2_RX	I2S1_CLK	I2C_GP0_DAT	I2C_GP0_CLK	GND	SPI2_MOSI	SPI2_MISO	15
16	UART2_RTS#	UART2_TX	FAN_PWM	RSVD	RSVD	SPI2_CS1#	SPI2_CS0#	SDCARD_PWR_EN	16
17	USB0_EN_OC#	FAN_TACH	RSVD	RSVD	RSVD	SDCARD_CD#	GND	SDCARD_D1	17
18	USB1_EN_OC#	RSVD	RSVD	RSVD	RSVD	SDCARD_D3	SDCARD_CLK	SDCARD_D0	18
19	RSVD	GPIO11_AP_WAKE_BT	RSVD	RSVD	GND	SDCARD_D2	SDCARD_CMD	GND	19
20	I2C_GP1_DAT	GPIO10_WIFI_WAKE_AP	RSVD	GND	CSI5_D1-	SDCARD_WP	GND	CSI4_D1-	20
21	I2C_GP1_CLK	GPIO12_BT_EN	GND	CSI5_CLK-	CSI5_D1+	GND	CSI4_CLK-	CSI4_D1+	21
22	GPIO_EXP1_INT	GPIO13_BT_WAKE_AP	CSI5_D0-	CSI5_CLK+	GND	CSI4_D0-	CSI4_CLK+	GND	22
23	GPIO_EXP0_INT	GPIO7_TOUCH_RST	CSI5_D0+	GND	CSI3_D1-	CSI4_D0+	GND	CSI2_D1-	23
24	RSVD	TOUCH_CLK	GND	CSI3_CLK-	CSI3_D1+	GND	CSI2_CLK-	CSI2_D1+	24
25	LCD_TE	GPIO6_TOUCH_INT	CSI3_D0-	CSI3_CLK+	GND	CSI2_D0-	CSI2_CLK+	GND	25
26	RSVD	LCD_VDD_EN	CSI3_D0+	GND	CSI1_D1-	CSI2_D0+	GND	CSI0_D1-	26
27	RSVD	LCD0_BKLT_PWM	GND	CSI1_CLK-	CSI1_D1+	GND	CSI0_CLK-	CSI0_D1+	27
28	GND	LCD_BKLT_EN	CSI1_D0-	CSI1_CLK+	GND	CSI0_D0-	CSI0_CLK+	GND	28
29	SDIO_RST#	SDIO_CMD	CSI1_D0+	GND	DSI3_D1+	CSI0_D0+	GND	DSI2_D1+	29
30	SDIO_D3	SDIO_CLK	GND	RSVD	DSI3_D1-	GND	DSI2_CLK+	DSI2_D1-	30
31	SDIO_D2	GND	DSI3_D0+	RSVD	GND	DSI2_D0+	DSI2_CLK-	GND	31
32	SDIO_D1	SDIO_D0	DSI3_D0-	GND	DSI1_D1+	DSI2_D0-	GND	DSI0_D1+	32
33	DP1_HPD	HDMI_CEC	GND	RSVD	DSI1_D1-	GND	DSI0_CLK+	DSI0_D1-	33
34	DP1_AUX_CH-	DP0_AUX_CH-	DSI1_D0+	RSVD	GND	DSI0_D0+	DSI0_CLK-	GND	34
35	DP1_AUX_CH+	DP0_AUX_CH+	DSI1_D0-	GND	DP1_TX3-	DSI0_D0-	GND	DP0_TX3-	35
36	USB0_OTG_ID	DP0_HPD	GND	DP1_TX2-	DP1_TX3+	GND	DP0_TX2-	DP0_TX3+	36
37	GND	USB0_VBUS_DET	DP1_TX1-	DP1_TX2+	GND	DP0_TX1-	DP0_TX2+	GND	37
38	USB1_D+	GND	DP1_TX1+	GND	DP1_TX0-	DP0_TX1+	GND	DP0_TX0-	38
39	USB1_D-	USB0_D+	GND	PEX_RFU_TX+	DP1_TX0+	GND	PEX_RFU_RX+	DP0_TX0+	39
40	GND	USB0_D-	PEX2_TX+	PEX_RFU_TX-	GND	PEX2_RX+	PEX_RFU_RX-	GND	40
41	RSVD	GND	PEX2_TX-	GND	PEX1_TX+	PEX2_RX-	GND	PEX1_RX+	41
42	RSVD	USB2_D+	GND	USB_SS1_TX+	PEX1_TX-	GND	USB_SS1_RX+	PEX1_RX-	42
43	GND	USB2_D-	USB_SS0_TX+	USB_SS1_TX-	GND	USB_SS0_RX+	USB_SS1_RX-	GND	43
44	PEX0_REFCLK+	GND	USB_SS0_TX-	GND	PEX0_TX+	USB_SS0_RX-	GND	PEX0_RX+	44
45	PEX0_REFCLK-	PEX1_REFCLK+	GND	SATA_TX+	PEX0_TX-	GND	SATA_RX+	PEX0_RX-	45
46	RESET_OUT#	PEX1_REFCLK-	RSVD	SATA_TX-	GND	GBE_LINK1000#	SATA_RX-	GND	46
47	RESET_IN#	GND	PEX1_CLKREQ#	RSVD	GBE_LINK_ACT#	GBE_MDI1+	GND	GBE_MDI3+	47
48	CARRIER_PWR_ON	RSVD	PEX0_CLKREQ#	PEX_WAKE#	GBE_MDI0+	GBE_MDI1-	GBE_MDI2+	GBE_MDI3-	48
49	CHARGER_PRSNT#	RSVD	PEX0_RST#	RSVD	GBE_MDI0-	GND	GBE_MDI2-	GND	49
50	VDD_RTC	POWER_BTN#	RSVD	RSVD	PEX1_RST#	GBE_LINK100#	GND	RSVD	50
	A	B	C	D	E	F	G	H	

4.5 Pin Descriptions

In the following table, pins are categorized by functional block.

Table 29 Pin List

Pin #	Jetson TX1 Pin Name	Usage/Description	Direction	Pin Type	Pin Type Code
Display					
B34	DP0_AUX_CH-	Display Port 0 Auxiliary Channel-	Bidir	AC-Coupled on Carrier Board	DP_AUX
B35	DP0_AUX_CH+	Display Port 0 Auxiliary Channel+	Bidir	AC-Coupled on Carrier Board	DP_AUX
B36	DP0_HPD	Display Port 0 Hot Plug Detect	Input	CMOS – 1.8V	ST
H38	DP0_TX0-	Display Port 0 Data Lane 0-	Output	AC-Coupled on Carrier Board	DP
H39	DP0_TX0+	Display Port 0 Data Lane 0+	Output	AC-Coupled on Carrier Board	DP
F37	DP0_TX1-	Display Port 0 Data Lane 1-	Output	AC-Coupled on Carrier Board	DP
F38	DP0_TX1+	Display Port 0 Data Lane 1+	Output	AC-Coupled on Carrier Board	DP
G36	DP0_TX2-	Display Port 0 Data Lane 2-	Output	AC-Coupled on Carrier Board	DP
G37	DP0_TX2+	Display Port 0 Data Lane 2+	Output	AC-Coupled on Carrier Board	DP
H35	DP0_TX3-	Display Port 0 Data Lane 3-	Output	AC-Coupled on Carrier Board	DP
H36	DP0_TX3+	Display Port 0 Data Lane 3+	Output	AC-Coupled on Carrier Board	DP
A34	DP1_AUX_CH-	Display Port 1 Aux- or HDMI DDC SDA	Bidir	AC-Coupled on Carrier Board	DP_AUX
A35	DP1_AUX_CH+	Display Port 1 Aux+ or HDMI DDC SCL	Bidir	AC-Coupled on Carrier Board	DP_AUX
A33	DP1_HPD	Display Port 1 Hot Plug Detect	Input	CMOS – 1.8V	ST
E38	DP1_TX0-	DisplayPort 1 Lane 0- / HDMI Lane 2-	Output	AC-Coupled on Carrier Board	DP
E39	DP1_TX0+	DisplayPort 1 Lane 0+ / HDMI Lane 2+	Output	AC-Coupled on Carrier Board	DP
C37	DP1_TX1-	DisplayPort 1 Lane 1- / HDMI Lane 1-	Output	AC-Coupled on Carrier Board	DP
C38	DP1_TX1+	DisplayPort 1 Lane 1+ / HDMI Lane 1+	Output	AC-Coupled on Carrier Board	DP
D36	DP1_TX2-	DisplayPort 1 Lane 2- / HDMI Lane 0-	Output	AC-Coupled on Carrier Board	DP
D37	DP1_TX2+	DisplayPort 1 Lane 2+ / HDMI Lane 0+	Output	AC-Coupled on Carrier Board	DP
E35	DP1_TX3-	DisplayPort 1 Lane 3- / HDMI Clk Lane-	Output	AC-Coupled on Carrier Board	DP
E36	DP1_TX3+	DisplayPort 1 Lane 3+ / HDMI Clk Lane+	Output	AC-Coupled on Carrier Board	DP
G34	DSI0_CLK-	Display, DSI 0 Clock-	Output	MIPI D-PHY	DPHY
G33	DSI0_CLK+	Display, DSI 0 Clock+	Output	MIPI D-PHY	DPHY
F35	DSI0_D0-	Display, DSI 0 Data 0-	Output	MIPI D-PHY	DPHY
F34	DSI0_D0+	Display, DSI 0 Data 0+	Output	MIPI D-PHY	DPHY
H33	DSI0_D1-	Display, DSI 0 Data 1-	Output	MIPI D-PHY	DPHY
H32	DSI0_D1+	Display, DSI 0 Data 1+	Output	MIPI D-PHY	DPHY
C35	DSI1_D0-	Display, DSI 1 Data 2-	Output	MIPI D-PHY	DPHY
C34	DSI1_D0+	Display, DSI 1 Data 2+	Output	MIPI D-PHY	DPHY
E33	DSI1_D1-	Display, DSI 1 Data 3-	Output	MIPI D-PHY	DPHY
E32	DSI1_D1+	Display, DSI 1 Data 3+	Output	MIPI D-PHY	DPHY
G31	DSI2_CLK-	Display DSI 2 Clock-	Output	MIPI D-PHY	DPHY
G30	DSI2_CLK+	Display DSI 2 Clock+	Output	MIPI D-PHY	DPHY
F32	DSI2_D0-	Display, DSI 2 Data 0-	Output	MIPI D-PHY	DPHY
F31	DSI2_D0+	Display, DSI 2 Data 0+	Output	MIPI D-PHY	DPHY
H30	DSI2_D1-	Display, DSI 2 Data 1-	Output	MIPI D-PHY	DPHY
H29	DSI2_D1+	Display, DSI 2 Data 1+	Output	MIPI D-PHY	DPHY
C32	DSI3_D0-	Display, DSI 3 Data 2-	Output	MIPI D-PHY	DPHY
C31	DSI3_D0+	Display, DSI 3 Data 2+	Output	MIPI D-PHY	DPHY
E30	DSI3_D1-	Display, DSI 3 Data 3-	Output	MIPI D-PHY	DPHY

Pin #	Jetson TX1 Pin Name	Usage/Description	Direction	Pin Type	Pin Type Code
E29	DSI3_D1+	Display, DSI 3 Data 3+	Output	MIPI D-PHY	DPHY
B19	GPIO11/AP_WAKE_BT	LCD Enable	Output	CMOS – 1.8V	ST
B33	HDMI_CEC	HDMI CEC	Bidir	Open Drain, 1.8V	DD
B28	LCD_BKLT_EN	Display Backlight Enable	Output	CMOS – 1.8V	ST
A25	LCD_TE	Display Tearing Effect	Input	CMOS – 1.8V	ST
B26	LCD_VDD_EN	Display Reset	Output	CMOS – 1.8V	ST
B27	LCD0_BKLT_PWM	Display Backlight PWM	Output	CMOS – 1.8V	ST
Camera					
F9	CAM0_MCLK	Camera 0 Reference Clock	Output	CMOS – 1.8V	ST
F8	CAM1_MCLK	Camera 1 Reference Clock	Output	CMOS – 1.8V	ST
G27	CSI0_CLK-	Camera, CSI 0 Clock-	Input	MIPI D-PHY	DPHY
G28	CSI0_CLK+	Camera, CSI 0 Clock+	Input	MIPI D-PHY	DPHY
F28	CSI0_D0-	Camera, CSI 0 Data 0-	Input	MIPI D-PHY	DPHY
F29	CSI0_D0+	Camera, CSI 0 Data 0+	Input	MIPI D-PHY	DPHY
H26	CSI0_D1-	Camera, CSI 0 Data 1-	Input	MIPI D-PHY	DPHY
H27	CSI0_D1+	Camera, CSI 0 Data 1+	Input	MIPI D-PHY	DPHY
D27	CSI1_CLK-	Camera, CSI 1 Clock-	Input	MIPI D-PHY	DPHY
D28	CSI1_CLK+	Camera, CSI 1 Clock+	Input	MIPI D-PHY	DPHY
C28	CSI1_D0-	Camera, CSI 1 Data 0-	Input	MIPI D-PHY	DPHY
C29	CSI1_D0+	Camera, CSI 1 Data 0+	Input	MIPI D-PHY	DPHY
E26	CSI1_D1-	Camera, CSI 1 Data 1-	Input	MIPI D-PHY	DPHY
E27	CSI1_D1+	Camera, CSI 1 Data 1+	Input	MIPI D-PHY	DPHY
G24	CSI2_CLK-	Camera, CSI 2 Clock-	Input	MIPI D-PHY	DPHY
G25	CSI2_CLK+	Camera, CSI 2 Clock+	Input	MIPI D-PHY	DPHY
F25	CSI2_D0-	Camera, CSI 2 Data 0-	Input	MIPI D-PHY	DPHY
F26	CSI2_D0+	Camera, CSI 2 Data 0+	Input	MIPI D-PHY	DPHY
H23	CSI2_D1-	Camera, CSI 2 Data 1-	Input	MIPI D-PHY	DPHY
H24	CSI2_D1+	Camera, CSI 2 Data 1+	Input	MIPI D-PHY	DPHY
D24	CSI3_CLK-	Camera, CSI 3 Clock-	Input	MIPI D-PHY	DPHY
D25	CSI3_CLK+	Camera, CSI 3 Clock+	Input	MIPI D-PHY	DPHY
C25	CSI3_D0-	Camera, CSI 3 Data 0-	Input	MIPI D-PHY	DPHY
C26	CSI3_D0+	Camera, CSI 3 Data 0+	Input	MIPI D-PHY	DPHY
E23	CSI3_D1-	Camera, CSI 3 Data 1-	Input	MIPI D-PHY	DPHY
E24	CSI3_D1+	Camera, CSI 3 Data 1+	Input	MIPI D-PHY	DPHY
G21	CSI4_CLK-	Camera, CSI 4 Clock-	Input	MIPI D-PHY	DPHY
G22	CSI4_CLK+	Camera CSI 4 Clock+	Input	MIPI D-PHY	DPHY
F22	CSI4_D0-	Camera, CSI 4 Clock-	Input	MIPI D-PHY	DPHY
F23	CSI4_D0+	Camera, CSI 4 Clock+	Input	MIPI D-PHY	DPHY
H20	CSI4_D1-	Camera, CSI 4 Data 1-	Input	MIPI D-PHY	DPHY
H21	CSI4_D1+	Camera, CSI 4 Data 1+	Input	MIPI D-PHY	DPHY
D21	CSI5_CLK-	Camera, CSI 5 Clock-	Input	MIPI D-PHY	DPHY
D22	CSI5_CLK+	Camera, CSI 5 Clock+	Input	MIPI D-PHY	DPHY
C22	CSI5_D0-	Camera, CSI 5 Data 0-	Input	MIPI D-PHY	DPHY
C23	CSI5_D0+	Camera, CSI 5 Data 0+	Input	MIPI D-PHY	DPHY
E20	CSI5_D1-	Camera, CSI 5 Data 1-	Input	MIPI D-PHY	DPHY
E21	CSI5_D1+	Camera, CSI 5 Data 1+	Input	MIPI D-PHY	DPHY
G8	GPIO0/CAM0_PWR#	Camera 1 Powerdown	Output	CMOS – 1.8V	ST

Pin #	Jetson TX1 Pin Name	Usage/Description	Direction	Pin Type	Pin Type Code
F7	GPIO1/CAM1_PWR#	Camera 1 Powerdown	Output	CMOS – 1.8V	ST
H8	GPIO2/CAM0_RST#	Camera Reset	Output	CMOS – 1.8V	ST
H7	GPIO3/CAM1_RST#	Camera Autofocus Enable	Output	CMOS – 1.8V	ST
G7	GPIO4/CAM_STROBE	Camera 1 Strobe	Output	CMOS – 1.8V	ST
D7	GPIO5/CAM_FLASH_EN	Camera Flash Enable	Output	CMOS – 1.8V	ST
C6	I2C_CAM_CLK	Camera I2C Clock	Bidir	Open Drain – 1.8V	DD
D6	I2C_CAM_DAT	Camera I2C Data	Bidir	Open Drain – 1.8V	DD
Audio					
F1	AUDIO_MCLK	Audio Codec Master Clock	Output	CMOS – 1.8V	ST
F2	GPIO19/AUD_RST	Audio Codec Reset	Output	CMOS – 1.8V	ST
H3	GPIO20/AUD_INT	Audio Codec Interrupt	Input	CMOS – 1.8V	ST
G2	I2S0_CLK	Digital Audio Port 1 Clock	Bidir	CMOS – 1.8V	CZ
H1	I2S0_LRCLK	I2S Audio Port 0 Field Select	Bidir	CMOS – 1.8V	CZ
G1	I2S0_SDIN	Digital Audio Port 1 Data In	Input	CMOS – 1.8V	CZ
H2	I2S0_SDOUT	I2S Audio Port 0 Data Out	Bidir	CMOS – 1.8V	CZ
C15	I2S1_CLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V	CZ
D13	I2S1_LRCLK	I2S Audio Port 1 Field Select	Bidir	CMOS – 1.8V	CZ
C14	I2S1_SDIN	I2S Audio Port 1 Data In	Input	CMOS – 1.8V	CZ
D14	I2S1_SDOUT	I2S Audio Port 1 Data Out	Bidir	CMOS – 1.8V	CZ
G5	I2S2_CLK	Digital Audio Port 3 Clock	Bidir	CMOS – 1.8V	ST
H5	I2S2_LRCLK	I2S Audio Port 2 Field Select	Bidir	CMOS – 1.8V	ST
G6	I2S2_SDIN	Digital Audio Port 3 Data In	Input	CMOS – 1.8V	ST
H6	I2S2_SDOUT	I2S Audio Port 2 Data Out	Bidir	CMOS – 1.8V	ST
E6	I2S3_CLK	I2S Audio Port 3 Clock	Bidir	CMOS – 1.8V	ST
F5	I2S3_LRCLK	I2S Audio Port 3 Field Select	Bidir	CMOS – 1.8V	ST
E5	I2S3_SDIN	I2S Audio Port 3 Data In	Input	CMOS – 1.8V	ST
F6	I2S3_SDOUT	I2S Audio Port 3 Data Out	Bidir	CMOS – 1.8V	ST
G13	SPI1_CLK	SPI 1 Clock	Bidir	CMOS – 1.8V	LV-CZ
E14	SPI1_CS0#	SPI 1 Chip Select 0	Bidir	CMOS – 1.8V	LV-CZ
E13	SPI1_CS1#	SPI 1 Chip Select 1	Bidir	CMOS – 1.8V	LV-CZ
F14	SPI1_MISO	SPI 1 MISO	Bidir	CMOS – 1.8V	LV-CZ
F13	SPI1_MOSI	SPI 1 MOSI	Bidir	CMOS – 1.8V	LV-CZ
WiFi/BT					
B20	GPIO10/WIFI_WAKE_AP	WiFi 2 Wake AP (Jetson TX1)	Input	CMOS – 1.8V	ST
B21	GPIO12/BT_EN	BT 2 Enable	Output	CMOS – 1.8V	ST
B22	GPIO13/BT_WAKE_AP	BT 2 Wake AP (Jetson TX1)	Input	CMOS – 1.8V	ST
E50	PEX1_RST#	PCIe 1 Reset	Output	Open Drain 3.3V, Pull-up on Jetson TX1	DD
A15	UART2_CTS#	UART 2 Clear to Send	Input	CMOS – 1.8V	ST
A16	UART2_RTS#	UART 2 Request to Send	Output	CMOS – 1.8V	ST
B15	UART2_RX	UART 2 Receive	Input	CMOS – 1.8V	ST
B16	UART2_TX	UART 2 Transmit	Output	CMOS – 1.8V	ST
B43	USB2_D-	USB 2.0, Port 2 Data+	Bidir	USB PHY	USB
B42	USB2_D+	USB 2.0, Port 2 Data+	Bidir	USB PHY	USB
LAN					
E47	GBE_LINK_ACT#	GbE RJ45 connector Link ACT LED0	Output	CMOS – 3.3V tolerant	LAN_3V3
F50	GBE_LINK100#	GbE RJ45 connector Link 100 LED1	Output	CMOS – 3.3V tolerant	LAN_3V3
F46	GBE_LINK1000#	GbE RJ45 connector Link 1000 LED2	Output	CMOS – 3.3V tolerant	LAN_3V3

Pin #	Jetson TX1 Pin Name	Usage/Description	Direction	Pin Type	Pin Type Code
E49	GBE_MDI0-	GbE Transformer Data 0-	Bidir	MDI	MDI
E48	GBE_MDI0+	GbE Transformer Data 0+	Bidir	MDI	MDI
F48	GBE_MDI1-	GbE Transformer Data 1-	Bidir	MDI	MDI
F47	GBE_MDI1+	GbE Transformer Data 1+	Bidir	MDI	MDI
G49	GBE_MDI2-	GbE Transformer Data 2-	Bidir	MDI	MDI
G48	GBE_MDI2+	GbE Transformer Data 2+	Bidir	MDI	MDI
H48	GBE_MDI3-	GbE Transformer Data 3-	Bidir	MDI	MDI
H47	GBE_MDI3+	GbE Transformer Data 3+	Bidir	MDI	MDI
Modem					
A8	GPIO14/AP_WAKE_MODEM	AP (Jetson TX1) Wake Modem	Output	CMOS – 1.8V	CZ
A9	GPIO15/AP2MDM_READY	AP (Jetson TX1) to Modem Ready	Input	CMOS – 1.8V	ST
A10	GPIO16/MODEM_WAKE_AP	Modem Wake AP	Input	CMOS – 1.8V	ST
B9	GPIO17/MDM2AP_READY	Modem to AP (Jetson TX1) Ready	Input	CMOS – 1.8V	CZ
B10	GPIO18/MODEM_COLDBOOT	Modem Coldboot	Input	CMOS – 1.8V	CZ
SDIO					
B30	SDIO_CLK	SDIO Clock	Output	CMOS – 1.8V	CZ
B29	SDIO_CMD	SDIO Command	Bidir	CMOS – 1.8V	CZ
B32	SDIO_D0	SDIO Data 0	Bidir	CMOS – 1.8V	CZ
A32	SDIO_D1	SDIO Data 1	Bidir	CMOS – 1.8V	CZ
A31	SDIO_D2	SDIO Data 2	Bidir	CMOS – 1.8V	CZ
A30	SDIO_D3	SDIO Data 3	Bidir	CMOS – 1.8V	CZ
A29	SDIO_RST#	SDIO Reset	Output	CMOS – 1.8V	ST
SD Card					
F17	SDCARD_CD#	SD Card Card Detect	Input	CMOS – 1.8V	ST
G18	SDCARD_CLK	SD Card Clock	Output	CMOS – 3.3/1.8V	CZ
G19	SDCARD_CMD	SD Card Command	Bidir	CMOS – 3.3/1.8V	CZ
H18	SDCARD_D0	SD Card Data 0	Bidir	CMOS – 3.3V/1.8V	CZ
H17	SDCARD_D1	SD Card Data 1	Bidir	CMOS – 3.3V/1.8V	CZ
F19	SDCARD_D2	SD Card Data 2	Bidir	CMOS – 3.3/1.8V	CZ
F18	SDCARD_D3	SD Card Data 3	Bidir	CMOS – 3.3/1.8V	CZ
H16	SDCARD_PWR_EN	SD Card power switch Enable	Output	CMOS – 1.8V	ST
F20	SDCARD_WP	SD Card Write Protect	Input	CMOS – 1.8V	ST
USB 2.0					
B40	USB0_D-	Micro USB Data-	Bidir	USB PHY	USB
B39	USB0_D+	Micro USB Data+	Bidir	USB PHY	USB
A17	USB0_EN_OC#	Micro USB VBUS Enable 0	Bidir	Open Drain – 3.3V	DD
A18	USB1_EN_OC#	USB 3.0 Type A, USB Enable 1	Bidir	Open Drain – 3.3V	DD
A36	USB0_OTG_ID	USB0 ID / VBUS EN	Input	Analog	USB
B37	USB0_VBUS_DET	USB0 VBUS	Input	USB VBUS, 5V	USB
A39	USB1_D-	USB 2.0, Port 1 Data+	Bidir	USB PHY	USB
PCIe/USB 3.0/SATA					
A44	PEX0_REFCLK+	PCIe Reference Clock 0+	Output	PCIe PHY	
A45	PEX0_REFCLK-	PCIe Reference Clock 0-	Output	PCIe PHY	
B45	PEX1_REFCLK+	PCIe Reference Clock 1+	Output	PCIe PHY	
B46	PEX1_REFCLK-	PCIe Reference Clock 1-	Output	PCIe PHY	
C40	PEX2_TX+	PCIe Lane 2 Transmit+	Output	PCIe PHY, AC-Coupled on Carrier Board	
C41	PEX2_TX-	PCIe Lane 2 Transmit -	Output	PCIe PHY, AC-Coupled on Carrier Board	

Pin #	Jetson TX1 Pin Name	Usage/Description	Direction	Pin Type	Pin Type Code
C47	PEX1_CLKREQ#	PCIE 1 Clock Request	Bidir	Open Drain 3.3V, Pull-up on Jetson TX1	
C48	PEX0_CLKREQ#	PCIE 0 Clock Request	Bidir	Open Drain 3.3V, Pull-up on Jetson TX1	
C49	PEX0_RST#	PCIe Reset 0	Output	Open Drain 3.3V, Pull-up on Jetson TX1	
D39	PEX_RFU_TX+	PCIe Lane RFU Transmit+	Output	PCIe PHY, AC-Coupled on Carrier Board	
D40	PEX_RFU_TX-	PCIe Lane RFU Transmit-	Output	PCIe PHY, AC-Coupled on Carrier Board	
D48	PEX_WAKE*	PCIe Wake	Input	Open Drain 3.3V, Pull-up on Jetson TX1	
E41	PEX1_TX+	PCIe Lane 1 Transmit+	Output	PCIe PHY, AC-Coupled on Carrier Board	
E42	PEX1_TX-	PCIe Lane 1 Transmit -	Output	PCIe PHY, AC-Coupled on Carrier Board	
E44	PEX0_TX+	PCIe Lane 0 Transmit+	Output	PCIe PHY, AC-Coupled on Carrier Board	
E45	PEX0_TX-	PCIe Lane 0 Transmit-	Output	PCIe PHY, AC-Coupled on Carrier Board	
F40	PEX2_RX+	PCIe Lane 2 Receive+	Input	PCIe PHY, AC-Coupled on Carrier Board	
F41	PEX2_RX-	PCIe Lane 2 Receive-	Input	PCIe PHY, AC-Coupled on Carrier Board	
G39	PEX_RFU_RX+	PCIe Lane RFU Receive+	Input	PCIe PHY, AC-Coupled on Carrier Board	
G40	PEX_RFU_RX-	PCIe Lane RFU Receive+	Input	PCIe PHY, AC-Coupled on Carrier Board	
H41	PEX1_RX+	PCIe Lane 1 Receive+	Input	PCIe PHY, AC-Coupled on Carrier Board	
H42	PEX1_RX-	PCIe Lane 1 Receive-	Input	PCIe PHY, AC-Coupled on Carrier Board	
H44	PEX0_RX+	PCIe Lane 0 Receive+	Input	PCIe PHY, AC-Coupled on Carrier Board	
H45	PEX0_RX-	PCIe Lane 0 Receive+	Input	PCIe PHY, AC-Coupled on Carrier Board	
D42	USB_SS1_TX+	USB 3.0 #1 or PCIe Lane 3 Transmit+	Output	USB SS PHY, AC-Coupled on Carrier Board	
D43	USB_SS1_TX-	USB 3.0 #1 or PCIe Lane 3 Transmit-	Output	USB SS PHY, AC-Coupled on Carrier Board	
G42	USB_SS1_RX+	USB 3.0 #1 or PCIe Lane 3 Receive+	Input	USB SS PHY, AC-Coupled (off Jetson TX1)	
G43	USB_SS1_RX-	USB 3.0 #1 or PCIe Lane 3 Receive-	Input	USB SS PHY, AC-Coupled (off Jetson TX1)	
D45	SATA_TX+	SATA Transmit+	Output	SATA PHY, AC-Coupled on Carrier Board	
D46	SATA_TX-	SATA Transmit-	Output	SATA PHY, AC-Coupled on Carrier Board	
G45	SATA_RX+	SATA Receive+	Input	SATA PHY, AC-Coupled on Carrier Board	
G46	SATA_RX-	SATA Receive-	Input	SATA PHY, AC-Coupled on Carrier Board	
C43	USB_SS0_TX+	USB 3.0 #0 Transmit+ (PCIe Lane 5)	Output	USB SS PHY, AC-Coupled on Carrier Board	
C44	USB_SS0_TX-	USB 3.0 #0 Transmit- (PCIe Lane 5)	Output	USB SS PHY, AC-Coupled on Carrier Board	
F43	USB_SS0_RX+	USB 3.0 #0 Receive + (PCIe Lane 5)	Input	USB SS PHY, AC-Coupled (off Jetson TX1)	
F44	USB_SS0_RX-	USB 3.0 #0 Receive - (PCIe Lane 5)	Input	USB SS PHY, AC-Coupled (off Jetson TX1)	
Touch/SPI					
B25	GPIO6/TOUCH_INT	Touch Interrupt	Input	CMOS – 1.8V	ST
B23	GPIO7/TOUCH_RST	Touch Reset	Output	CMOS – 1.8V	ST
E3	SPI0_CLK	SPI 0 Clock	Bidir	CMOS – 1.8V	LV-CZ
F3	SPI0_CS0#	SPI 0 Chip Select 0	Bidir	CMOS – 1.8V	LV-CZ
E4	SPI0_MISO	SPI 0 MISO	Bidir	CMOS – 1.8V	LV-CZ
F4	SPI0_MOSI	SPI 0 MOSI	Bidir	CMOS – 1.8V	LV-CZ
H14	SPI2_CLK	SPI 2 Clock	Bidir	CMOS – 1.8V	CZ
G16	SPI2_CS0#	SPI 2 Chip Select 0	Bidir	CMOS – 1.8V	CZ
F16	SPI2_CS1#	SPI 2 Chip Select 1	Bidir	CMOS – 1.8V	CZ
H15	SPI2_MISO	SPI 2 MISO	Bidir	CMOS – 1.8V	CZ
G15	SPI2_MOSI	SPI 2 MOSI	Bidir	CMOS – 1.8V	CZ
B24	TOUCH_CLK	Touch Clock	Output	CMOS – 1.8V	ST
Serial Port					
E10	UART1_CTS#	UART 1 Receive	Input	CMOS – 1.8V	ST
E9	UART1_RTS#	UART 1 Transmit	Output	CMOS – 1.8V	ST
D10	UART1_RX	UART 1 Receive	Input	CMOS – 1.8V	ST

Pin #	Jetson TX1 Pin Name	Usage/Description	Direction	Pin Type	Pin Type Code
D9	UART1_TX	UART 1 Transmit	Output	CMOS – 1.8V	ST
I2C					
E15	I2C_GP0_CLK	General I2C Bus #0 Clock	Bidir	Open Drain – 1.8V	DD
D15	I2C_GP0_DAT	General I2C Bus #1 Data	Bidir	Open Drain – 1.8V	DD
A21	I2C_GP1_CLK	General I2C Bus #1 Clock	Bidir	Open Drain – 3.3V	DD
A20	I2C_GP1_DAT	General I2C Bus #1 Data	Bidir	Open Drain – 3.3V	DD
A6	I2C_PM_CLK	PM I2C Bus Clock	Bidir	Open Drain – 1.8V	DD
B6	I2C_PM_DAT	PM I2C Bus Data	Bidir	Open Drain – 1.8V	DD
Fan					
C16	FAN_PWM	Fan PWM	Output	CMOS – 1.8V	ST
B17	FAN_TACH	Fan Tach	Input	CMOS – 1.8V	CZ
Sensor					
H13	GPIO8/ALS_PROX_INT	Proximity sensor Interrupt	Input	CMOS – 1.8V	ST
G14	GPIO9/MOTION_INT	ICM20628 Gyro/Accel	Input	CMOS – 1.8V	ST
System					
C7	BATLOW#	GPIO – Low Battery	Input	CMOS – 1.8V	ST
A48	CARRIER_PWR_ON	Carrier Power On	Output	CMOS – 1.8V	–
B7	CARRIER_STBY#	SOC Power Request	Output	CMOS – 1.8V	ST
A49	CHARGER_PRSNT#	PMIC AC OK	Input	Open Drain, 1.8V	PMIC
A7	CHARGING#	Charger Interrupt	Input	CMOS – 1.8V	ST
E1	FORCE_RECOV#	Force Recovery strap pin	Input	CMOS – 1.8V	ST
B50	POWER_BTN#	Power on	Input	Open Drain, 1.8V	ST
A47	RESET_IN#	System Reset Input	Input	Open Drain, 1.8V	JT_RST
A46	RESET_OUT#	System Reset Output from PMIC	Output	CMOS – 1.8V	PMIC
E2	SLEEP*	Sleep input	Input	Open Drain, 1.8V	ST
B8	VIN_PWR_BAD#	Input Power Bad	Input	CMOS – VDD_IN	–
C7	BATLOW#	GPIO – Low Battery	Input	CMOS – 1.8V	ST
GPIO					
A23	GPIO_EXP0_INT	GPIO expander 0 Interrupt	Input	CMOS – 1.8V	CZ
A22	GPIO_EXP1_INT	GPIO Expander 1 Interrupt	Input	CMOS – 1.8V	ST
Debug					
B13	JTAG_GP0	JTAG Test Reset	Input	CMOS – 1.8V	JT_RST
A14	JTAG_RTCLK	JTAG Return Clock	Output	CMOS – 1.8V	JT_RST
B11	JTAG_TCLK	JTAG Test Clock	Input	CMOS – 1.8V	JT_RST
B12	JTAG_TDI	JTAG Test Data In	Input	CMOS – 1.8V	JT_RST
A13	JTAG_TDO	JTAG Test Data Out	Output	CMOS – 1.8V	ST
A12	JTAG_TMS	JTAG Test Mode Select	Input	CMOS – 1.8V	JT_RST
H11	UART0_CTS#	UART 0 Clear to Send	Input	CMOS – 1.8V	ST
G11	UART0_RTS#	UART 1 Return to Send	–	CMOS – 1.8V	ST
G12	UART0_RX	UART 1 Receive	Input	CMOS – 1.8V	ST
H12	UART0_TX	UART 0 Transmit	Output	CMOS – 1.8V	ST

Table 30 Power Pin List

VDD_IN	Pins
Main VDD Input (5.5-19.6V)	A1, A2, B1, B2, C1, C2
VDD_RTC	**Pins**
PMIC Real Time Clock power	A50

Table 31 Ground Pin List

GND	Pins
Ground	A3, A4, A28, A37, A40, A43, B3, B4, B14, B31, B38, B41, B44, C3, C4, C21, C24, C27, C30, C33, C36, C39, C42, C45, D20, D23, D26, D29, D32, D35, D38, D41, D44, E19, E22, E25, E28, E31, E34, E37, E40, E43, E46, F10, F15, F21, F24, F27, F30, F33, F36, F39, F42, F45, F49, G3, G17, G20, G23, G26, G29, G32, G35, G38, G41, G44, G47, G50, H19, H22, H25, H28, H31, H34, H37, H40, H43, H46, H49, B47

Table 32 Reserved Pin List

Reserved	Pins
Reserved	A5, A11, A19, A24, A26, A27, A41, A42, B5, B18, B48, B49, C5, C8, C9, C10, C11, C12, C13, C17, C18, C19, C20, C46, C50, D1, D2, D3, D4, D5, D8, D11, D12, D16, D17, D18, D19, D30, D31, D33, D34, D47, D49, D50, E7, E8, E11, E12, E16, E17, E18, F11, F12, G4, G9, G10, H4, H9, H10, H50

5.0 Physical / Electrical Characteristics

5.1 Absolute Maximum Ratings

The absolute maximum ratings describe stress conditions. These parameters do not set minimum and maximum operating conditions that will be tolerated over extended periods of time. If the device is exposed to these parameters for extended periods of time, no guarantee is made and device reliability may be affected. It is not recommended to operate the Jetson TX1 module under these conditions, recommended operating conditions are provided in the following section.

WARNING: Exceeding the listed conditions may damage and/or affect long-term reliability of the part.
The Jetson TX1 module should never be subjected to conditions exceeding absolute maximum ratings.

Table 33 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
VDD_{MAX}	VDD_IN	-0.5	30	V	
	VDD_RTC	-0.3	6.0	V	
IDD_{MAX}	VDD_IN Imax		3	A	
V_{M_PIN}	Voltage applied to any powered I/O pin	-0.5	VDD + 0.5	V	
	DD pads configured as open drain	-0.5	3.63	V	pad's output-driver must be set to open-drain mode
T_{TTP}	Operating Temperature: Sensed from Thermal Transfer Plate	-25	80	°C	
T_{STG}	Storage Temperature	-40	80	°C	

The parameters listed in following table are specific to a temperature range and operating voltage. Operating the Jetson TX1 module beyond these parameters is not recommended. Exceeding these conditions for extended periods may adversely affect device reliability.

Table 34 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD_{DC}	VDD_IN	5.5		19.6	V	
	VDD_RTC	1.65		5.5	V	

5.2 Digital Logic

Voltages less than the minimum stated value can be interpreted as an undefined state or logic level low which may result in unreliable operation. Voltages exceeding the maximum value can damage and/or adversely affect device reliability.

Table 35. CMOS Pad Type DC Characteristics

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	0.5 + VDD	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	---	V

Table 36 Open Drain Pad Type DC Characteristics

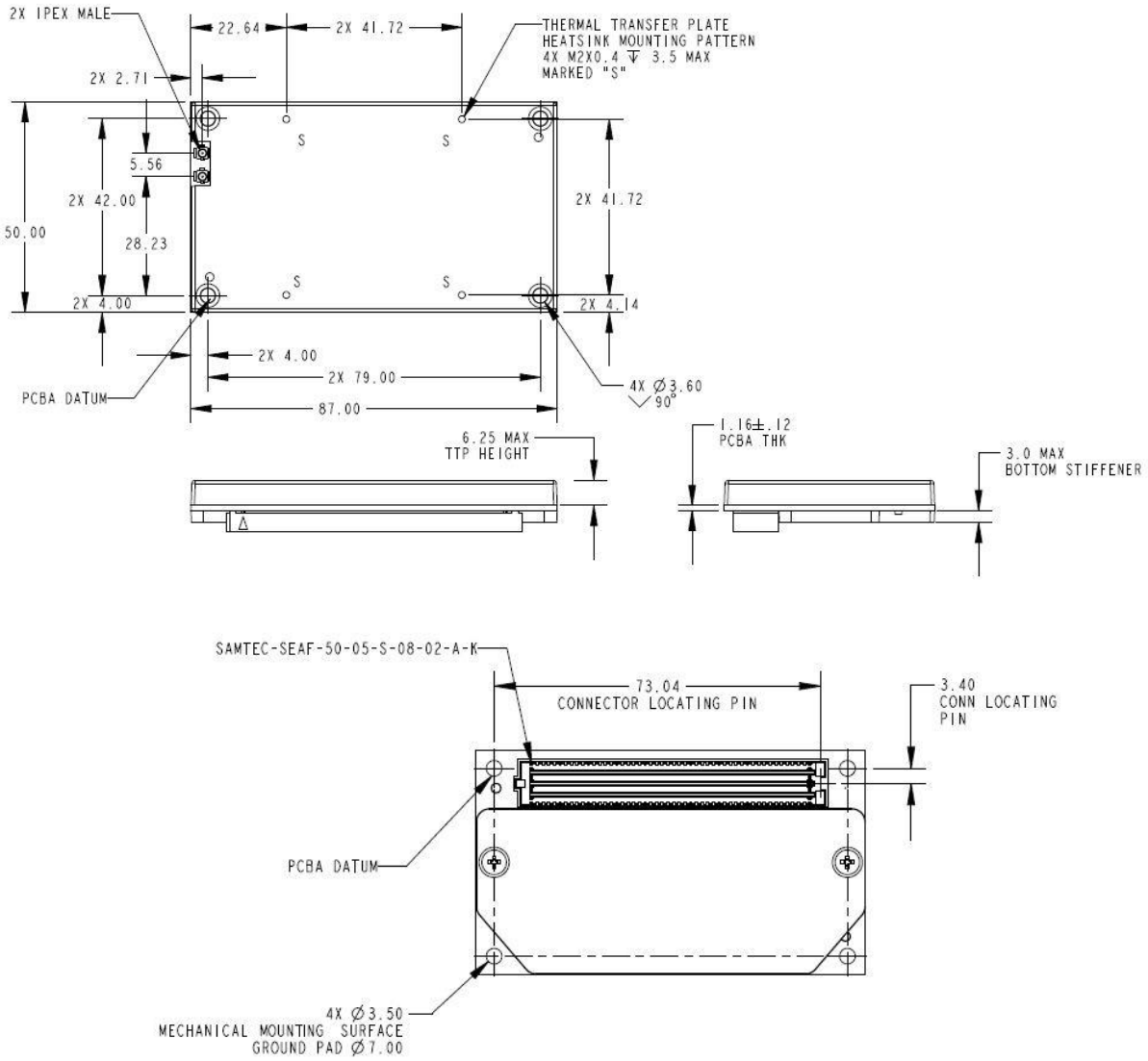
Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	3.63	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	---	V

5.3 Thermal

Jetson TX1 was designed to be modular from both a functionality standpoint as well as a thermal standpoint. While it integrates several individual components the primary Jetson TX1 thermal interface is via a single Thermal Transfer Plate (TTP) that covers the top side. The TTP simplifies thermal design and integration with the system-level thermal solution. See the ***Jetson TX1 Thermal Design Guide*** for complete details on the thermal evaluation and design process using Jetson TX1.

5.4 Package Drawing and Dimensions

Figure 8 Jetson TX1 Package Outline with Dimensions



NOTES

1. All dimensions are in millimeters unless otherwise specified.
2. Tolerances are: .X ± .25, .XX ± .13, Angles ± 1°
3. Calculated Mass: 75 ±2% Grams
4. Thermal transfer plate and bottom stiffener finish: Clear Chemfilm per MIL-C-5541-E Class 3

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