# Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects

**Walt Kester** - December 06, 2010

(***In this three part series, Walt Kester provides a compendium of tips and hints that will help embedded systems developers speed the design of the printed circuit boards upon which their designs are based***.)

Printed circuit boards (PCBs) are by far the most common method of assembling modern electronic circuits. Composed of a sandwich of insulating layer (or layers) and one or more copper conductor patterns, they can introduce various forms of errors into a circuit, particularly if the circuit is operating at either high precision or high speed. PCBs, then, act as "unseen" components wherever they are used in precision circuit designs.

Since embedded designers don't always consider the PCB electrical characteristics as additional components of their circuit, overall performance can easily end up worse than predicted. This general topic, manifested in many forms, is the focus of this series of articles.

PCB effects that are harmful to precision circuit performance include leakage resistances; spurious voltage drops in trace foils, vias, and ground planes; the influence of stray capacitance, dielectric absorption (DA), and the related "hook." In addition, the tendency of PCBs to absorb atmospheric moisture, hygroscopicity, means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, PCB effects can be divided into two broad categories: those that most noticeably affect the static or dc operation of the circuit and those that most noticeably affect dynamic or AC circuit operation.

Another very broad area of PCB design is the topic of grounding. Grounding is a problem area in itself for all analog designs, and it can be said that implementing a PCB-based circuit doesn't change that fact. Fortunately, certain principles of quality grounding, namely the use of ground planes, are intrinsic to the PCB environment. This factor is one of the more significant advantages to PCB-based analog designs, and an appreciable amount of this appendix is focused on this issue.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or simply excessive IR drops in ground conductors. Proper conductor routing and sizing as well as differential signal handling and ground isolation techniques enable control of such parasitic voltages.

One final area of grounding to be discussed is grounding appropriate for a mixed-signal, analog/digital environment. This topic is the subject of many application calls, and it is certainly true that interfacing with ADCs (or DACs) is a major part of the system design, and thus it shouldn't be

overlooked. Indeed, the single issue of quality grounding can drive the entire layout philosophy of a high-performance mixed-signal PCB design—as well it should.

**Resistance of Conductors**

Every engineer is familiar with resistors, although perhaps fewer are aware of their idiosyncrasies. But too few engineers consider that all the wires and PCB traces with which their systems and circuits are assembled are also resistors. In higher-precision systems, even these trace resistances and simple wire interconnections can have degrading effects. Copper is not a superconductor—and too many engineers appear to think it is! **Figure C.1 below** illustrates a method of calculating the sheet resistance R of a copper square, given the length Z, the width X, and the thickness Y.

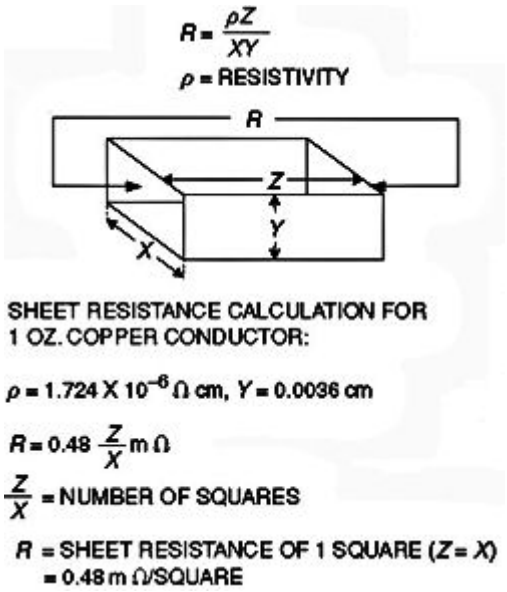


***Figure C.1: Calculation of sheet resistance and linear resistance for standard copper PCB conductors.***

At 25ºC the resistivity of pure copper is 1.724 10–6 Ωcm. The thickness of standard 1-ounce PCB copper foil is 0.036 mm (0.0014). Using the relations shown, the resistance of such a standard copper element is therefore 0.48 Ω/square.

One can readily calculate the resistance of a linear trace by effectively "stacking" a series of such squares end to end, to make up the line's length. The line length is Z and the width is X, so the line resistance R is simply a product of Z/X and the resistance of a single square, as noted in the figure.

For a given copper weight and trace width, a resistance/length calculation can be made. For example, the 0.25 mm (10 mil) wide traces frequently used in PCB designs equates to a resistance/length of about 19 mΩ/cm (48 mΩ/inch), which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4%/ºC around room temperature. This is a factor that shouldn't be ignored, in particular within low-impedance precision circuits, where the TC can shift the net impedance over temperature.

As shown in **Figure C.2 below**, PCB trace resistance can be a serious error when conditions aren't favorable. Consider a 16-bit ADC with a 5 kΩ input resistance, driven through 5 cm of 0.25 mm wide 1 oz PCB track between it and its signal source. The track resistance of nearly 0.1 Ω forms a divider with the 5 kΩ load, creating an error. The resulting voltage drop is a gain error of 0.1/5000 (0.0019%), well over 1 LSB (0.0015% for 16 bits).

So, when dealing with precision circuits, the point is made that even simple design items such as PCB trace resistance cannot be dealt with casually. There are various solutions to address this issue, such as wider traces (which may take up excessive space), the use of heavier copper (which may be too expensive), or simply choosing a high-impedance converter. But the most important thing is to think it all through, avoiding any tendency to overlook items that appear innocuous on the surface.

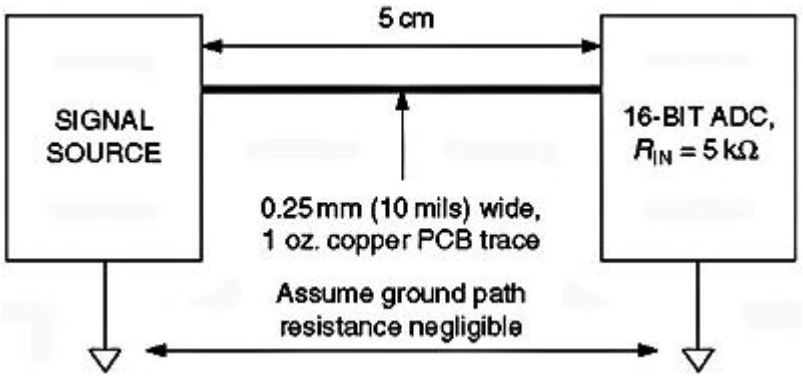


***Figure C.2: Ohm's Law predicts _1 LSB of error due to drop in PCB conductor***.

**Voltage Drop in Signal Leads: Kelvin" Feedback**

The gain error resulting from resistive voltage drop in PCB signal leads is important only with high precision and/or at high resolutions (the Figure C.2 example) or where large signal currents flow. Where load impedance is constant and resistive, adjusting overall system gain can compensate for the error. In other circumstances, it may often be removed by the use of "Kelvin" or "voltage sensing" feedback, as shown in **Figure C.3 below**.


**Figure C.3: Use of a sense connection moves accuracy to the load point.**

In this modification to the case of Figure C.2, a long resistive PCB trace is still used to drive the input of a high-resolution ADC, with low input impedance. In this case, however, the voltage drop in the signal lead does not give rise to an error, because feedback is taken directly from the input pin of the ADC and returned to the driving source. This scheme allows full accuracy to be achieved in the signal presented to the ADC, despite any voltage drop across the signal trace.

The use of separate force (F) and sense (S) connections at the load removes any errors resulting from voltage drops in the force lead, but of course may only be used in systems where there is negative feedback. It is also impossible to use such an arrangement to drive two or more loads with equal accuracy, since feedback may only be taken from one point. Also, in this much-simplified system, errors in the common lead source/load path are ignored, the assumption being that ground path voltages are negligible. In many systems this may not necessarily be the case, and additional steps may be needed, as will be detailed later in this series.

**Signal Return Currents**

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particularly, that the return current must always be considered in analyzing a circuit, as is illustrated in **Figure C.4 below**. In dealing with grounding issues, common human tendencies provide some insight into the way the correct thinking about the circuit can be helpful in analysis. Most engineers readily consider the ground return current, I, when they are considering a fully differential circuit.

However, in considering the more usual circuit case, where a single-ended signal is referred to "ground," it is common to assume that all the points on the circuit diagram where ground symbols are found are at the same potential. Unfortunately, this happy circumstance "just ain't necessarily so."

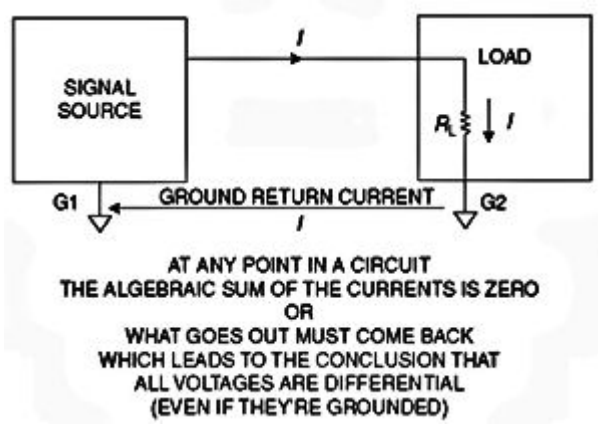


***Figure C.4: Kirchoff's Law helps in analyzing voltage drops around a complete source/load coupled circuit.***

This overly optimistic approach is illustrated in **Figure C.5 below**, where, if it really should exist, "infinite ground conductivity" would lead to zero ground voltage difference between source ground G1 and load ground G2. Unfortunately this approach isn't a wise practice, and when we're dealing with high precision circuits, it can lead to disasters.

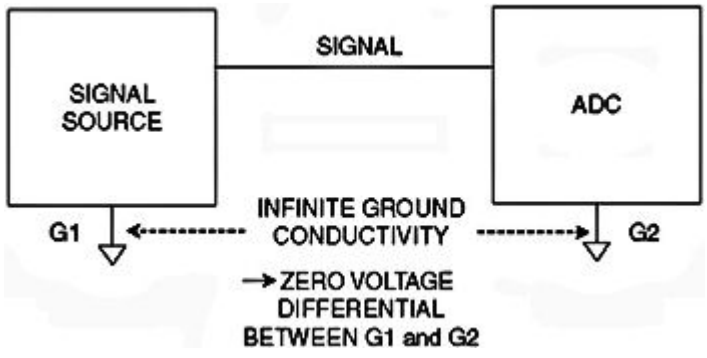


***Figure C.5: Unlike this optimistic diagram, it is unrealistic to assume infi nite conductivity between source/load grounds in a real-world system.***

A more realistic approach to ground conductor integrity includes analysis of the impedance(s) involved and careful attention to minimizing spurious noise voltages. A more realistic model of a ground system is shown in **Figure C.6 below**. The signal return current flows in the complex

impedance existing between ground points G1 and G2 as shown, giving rise to a voltage drop ΔV in this path.

But it is important to note that additional external currents, such as IEXT, may also flow in this same path. It is critical to understand that such currents may generate  uncorrelated noise voltages between G1 and G2 (dependent upon the current magnitude and relative ground impedance). Some portion of these undesired voltages may end up being seen at the signal's load end, and they can have the potential to corrupt the signal being transmitted.

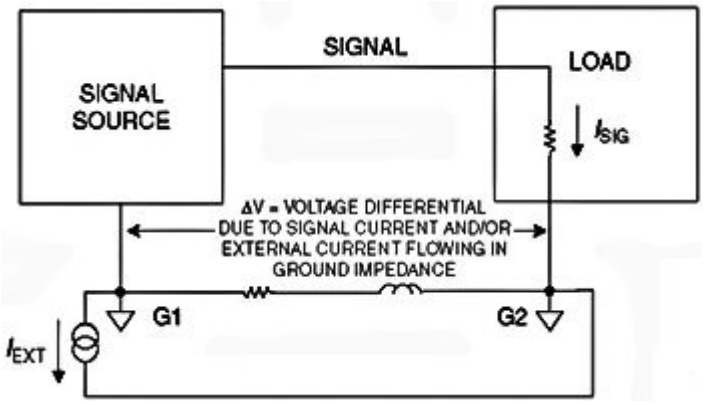


***Figure C.6: A more realistic source-to-load grounding system view includes consideration of the impedance between G1 and G2, plus the effect of any nonsignal-related currents.***

**Grounding in Mixed Analog/Digital Systems**

Today's signal processing systems generally require mixed-signal devices such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) as well as fast digital signal processors (DSPs). Requirements for processing analog signals having wide dynamic ranges increases the importance of high-performance ADCs and DACs. Maintaining wide dynamic range with low noise in hostile digital environments is dependent upon using good high-speed circuit design techniques, including proper signal routing, decoupling, and grounding.

In the past, "high-precision, low-speed" circuits have generally been viewed differently than so-called "high-speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criteria. However, the following two examples show that in practice, most of today's signal processing ICs are really "high speed" and must therefore be treated as such in order to maintain high performance. This is certainly true of DSPs as well as ADCs and DACs.

All sampling ADCs (ADCs with an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high-speed clocks with fast rise and fall times (generally a few nanoseconds) and must be treated as high-speed devices, even though throughput rates may appear low. For example, a medium-speed 12-bit successive approximation (SAR) ADC may operate on a 10 MHz internal clock, although the sampling rate is only 500 kSPS.

Sigma-delta (Σ-Δ) ADCs also require high-speed clocks because of their high oversampling ratios. Even high-resolution, so-called "low-frequency" Σ-Δindustrial measurement ADCs (having throughputs of 10 Hz to 7.5 kHz) operate on 5 MHz or higher clocks and offer resolution to 24 bits (for example, the Analog Devices AD77xx series).

To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. In addition, some

mixed-signal ICs have relatively low digital currents, whereas others have high digital currents. In many cases, these two types must be treated differently with respect to optimum grounding.

Digital and analog design engineers tend to view mixed-signal devices from different perspectives, and the purpose of this section is to develop a general grounding philosophy that will work for most mixed signal devices, without having to know the specific details of their internal circuits.

**Ground and Power Planes**

The importance of maintaining a low-impedance, large-area ground plane is critical to all analog circuits today. The ground plane not only acts as a low-impedance return path for decoupling high-frequency currents (caused by fast digital logic) but also minimizes EMI/RFI emissions.

Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced. Ground planes also allow the transmission of high-speed digital or analog signals using transmission line techniques (microstrip or stripline) where controlled impedances are required.

The use of "buss wire" is totally unacceptable as a "ground" because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20 nH/ inch inductance. A transient current having a slew rate of 10 mA/ns created by a logic signal would develop an unwanted voltage drop of 200 mV at this frequency flowing through 1 inch of this wire:

$$\Delta v = L\frac{\Delta i}{\Delta t} = 20\,\text{nH} \times \frac{10\,\text{mA}}{\text{ns}} = 200\,\text{mV}. \qquad \text{(C.1)}$$

For a signal having a 2 V peak-to-peak range, this translates into an error of about 200 mV, or 10% (approximate 3.5-bit accuracy). Even in all-digital circuits, this error would result in considerable degradation of logic noise margins.

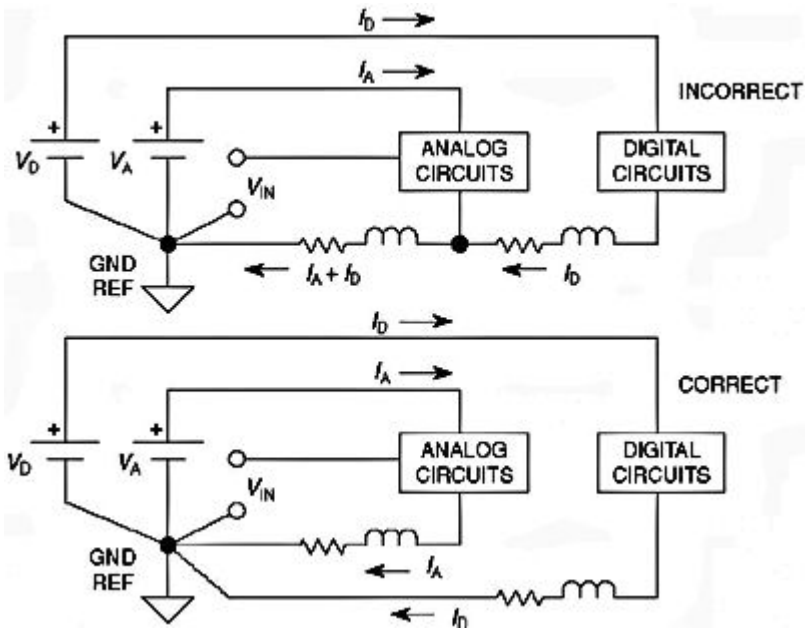


***Figure C.7: Digital currents fl owing in analog return path create error voltages***

**Figure C.7 above** shows an illustration of a situation where the digital return current modulates the analog return current (top). The ground return wire inductance and resistance are shared between the analog and digital circuits, and this is what causes the interaction and resulting error. A possible solution is to make the digital return current path flow directly to the GND REF, as shown

in the bottom of the figure above.

This is the fundamental concept of a “star,” or single-point ground system. Implementing the true single-point ground in a system which contains multiple high-frequency return paths is difficult because the physical length of the individual return current wires will introduce parasitic resistance and inductance, which can make obtaining a low-impedance, high-frequency ground difficult.

In practice, the current returns must consist of large area ground planes for low impedance to high-frequency currents. Without a low-impedance ground plane, it is therefore almost impossible to avoid these shared impedances, especially at high frequencies.

All integrated circuit ground pins should be soldered directly to the low-impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high-speed devices.

The extra inductance and capacitance of even “lowprofile” sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual “pin sockets” or “cage jacks” may be acceptable.

Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-33080--3 and 5-330808-6). They have spring-loaded gold contacts that make good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade their performance.

Power supply pins should be decoupled directly to the ground plane using low-inductance ceramic surface-mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1 mm. The ceramic capacitors should be located as close as possible to the IC power pins. Ferrite beads may be also required for additional decoupling.

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**Double-Sided vs Multilayer PCBs**

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved, and at least 75% should remain.

After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground “islands,” because IC ground pins located in a ground “island” have no current return path to the ground plane.

Also, the ground plane should be checked for “skinny” connections between adjacent large areas which may signifi cantly reduce the effectiveness of the ground plane. Needless to say, autorouting board layout techniques will generally lead to a layout disaster on a mixed-signal board, so manual intervention is highly recommended.

Systems that are densely packed with surface-mount ICs will have a large number of interconnections; therefore multilayer boards are mandatory. This allows at least one complete layer to be dedicated to ground. A simple four-layer board would have internal ground and power plane layers, with the outer two layers used for interconnections between the surface mount components.

Placing the power and ground planes adjacent to each other provides additional interplane

capacitance which helps high-frequency decoupling of the power supply. In most systems, four layers are not enough, and additional layers are required for routing signals as well as power**.** **Figure C.8 below** summarizes the key issues relating to ground planes.

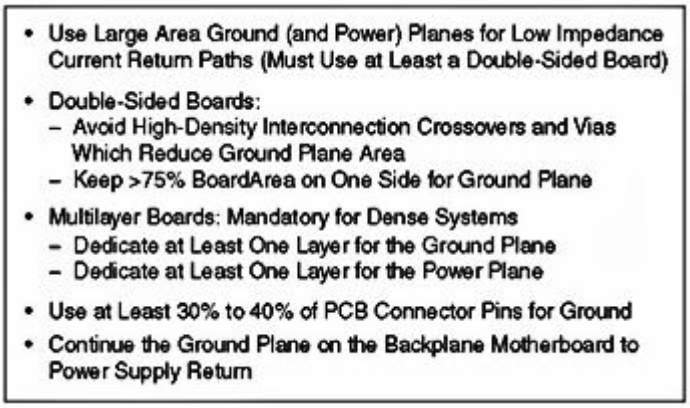


***Figure C.8: Ground planes are mandatory!***

**Multicard Mixed-Signal Systems**

The best way of minimizing ground impedance in a multicard system is to use a “motherboard” PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the backplane. The PCB connector should have at least 30–40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities:

The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. This is commonly referred to as a “multipoint” grounding system and is shown in Figure C.9 below. The ground plane can be connected to a single system “star ground” point (generally at the power supply).

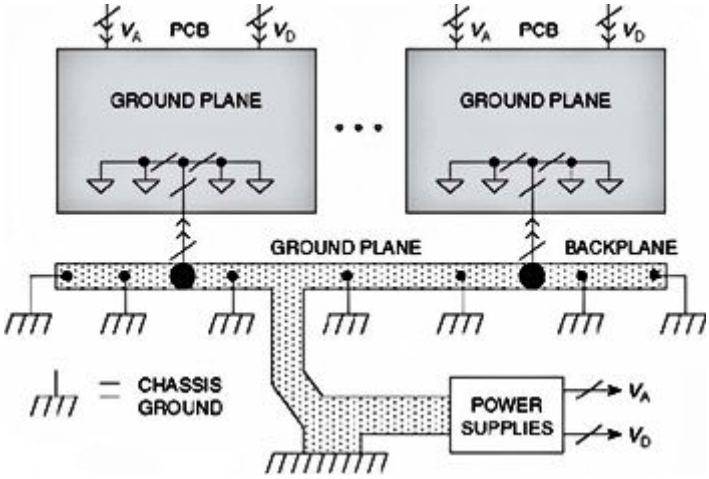


***Figure C.9: Multipoint ground concept.***

The first approach is most often used in all-digital systems but can be used in mixed-signal systems, provided that the ground currents due to digital circuits are sufficiently low and diffused over a large area. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis.

However, it is critical that good electrical contact be made where the grounds are connected to the

sheet-metal chassis. This requires self-tapping sheet-metal screws or “biting” washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

The second approach (“star ground”) is often used in high-speed, mixed-signal systems having separate analog and digital ground systems and warrants further discussion.

**Separating Analog and Digital Grounds**

In mixed-signal systems with large amounts of digital circuitry, it is highly desirable to physically separate sensitive analog components from noisy digital components. It may also be beneficial to use separate ground planes for the analog and the digital circuitry.

These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or “ground screens,” which are made up of a series of wired interconnections between the connector ground pins.

The arrangement shown in **Figure C.10 below** illustrates that the two planes are kept separate all the way back to a common system “star” ground, generally located at the power supplies.

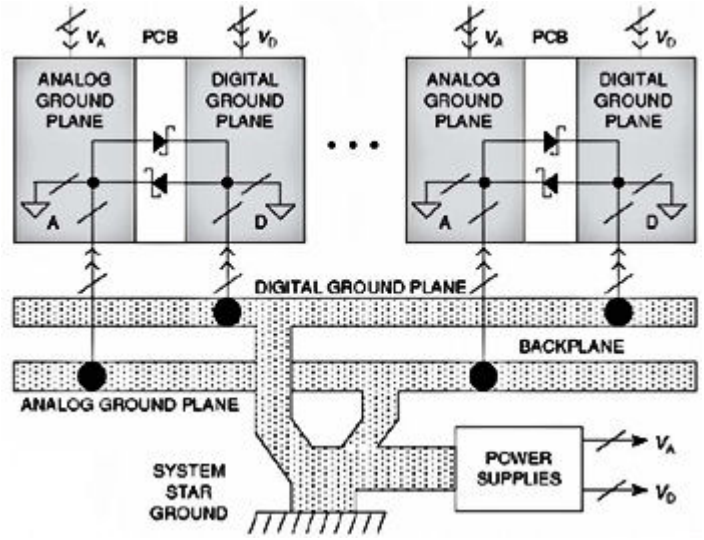


***Figure C.10: Separating analog and digital ground planes.***

The connections between the ground planes, the power supplies, and the “star” should be made up of multiple bus bars or wide copper braids for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged.

This voltage should be kept less than 300 mV to prevent damage to ICs that have connections to both the analog and digital ground planes. Schottky diodes are preferable because of their low capacitance and low forward voltage drop. The low capacitance prevents AC coupling between the analog and digital ground planes.

Schottky diodes begin to conduct at about 300 mV, and several parallel diodes in parallel may be required if high currents are expected. In some cases, ferrite beads can be used instead of Schottky diodes, but they introduce DC ground loops, which can be troublesome in precision systems.

It is mandatory that the impedance of the ground planes be kept as low as possible, all the way back

to the system star ground. DC or AC voltages of more than 300 mV between the two ground planes not only can damage ICs, but they can cause false triggering of logic gates and possible latchup.

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**Grounding and Decoupling Mixed-Signal ICs**

Sensitive analog components such as amplifiers and voltage references are always referenced and de-coupled to the analog ground plane. The ADCs and DACs (and other mixed-signal ICs) with low digital currents should generally be treated as analog components and also grounded and decoupled to the analog ground plane.

At first glance, this advice might seem somewhat contradictory, since a converter has an analog and digital interface and usually has pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in **Figure C.11 below** will help explain this seeming dilemma.

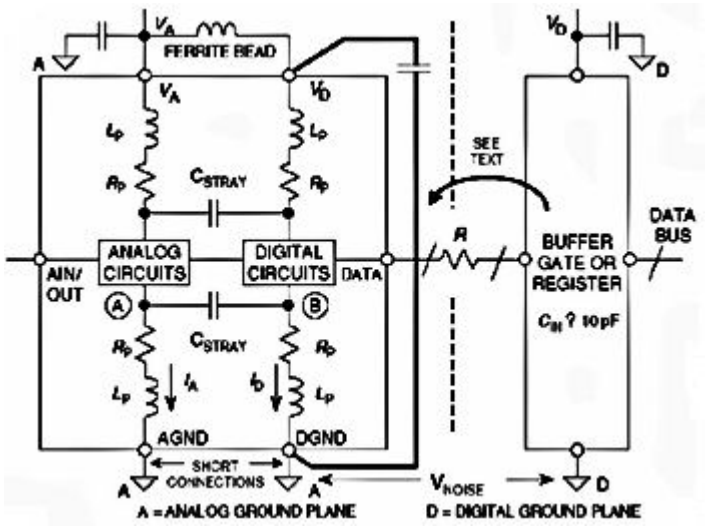


***Figure C.11: Proper grounding of mixed-signal ICs with low internal digital currents.***

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure C.11 shows a simple model of a converter. There is nothing the IC designer can do about the wire-bond inductance and resistance associated with connecting the bond pads on the chip to the package pins except to realize it's there.

The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, CSTRAY. In addition, there is approximately 0.2 pF unavoidable stray capacitance between every pin of the IC package. It's the IC designer's job to make the chip work in spite of this. However, to prevent further coupling, the AGND and DGND pins should be joined together externally to the analog ground plane with minimum lead lengths.

Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. Note that connecting DGND to the digital ground plane applies VNOISE across the AGND and DGND pins and invites disaster. (*The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.*)

It is true that this arrangement may inject a small amount of digital noise onto the analog ground plane. These currents should be quite small and can be minimized by ensuring that the converter output does not drive a large fanout (they normally can't, by design).

Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing and minimize digital switching currents, thereby reducing any potential coupling into the analog port of the converter.

The logic supply pin (VD) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead, as shown in Figure C.11. The internal transient digital currents of the converter will flow in the small loop from VD through the decoupling capacitor and to DGND (this path is shown with a heavy line on the diagram). The transient digital currents will therefore not appear on the external analog ground plane, but are confined to the loop.

The VD pin decoupling capacitor should be mounted as close to the converter as possible to minimize parasitic inductance. These decoupling capacitors should be low inductance ceramic types, typically between 0.01 µF and 0.1 µF.

**Treat the ADC Digital Outputs with Care**

It is always a good idea (as shown in Figure C.11) to place a buffer register adjacent to the converter to isolate the converter's digital lines from noise on the data bus. The register also serves to minimize loading on the digital outputs of the converter and acts as a Faraday shield between the digital outputs and the data bus.

Even though many converters have three-state outputs/inputs, this isolation register still represents good design practice. In some cases it may be desirable to add an additional buffer register on the analog ground plane next to the converter output to provide greater isolation.

The series resistors (labeled R in Figure C.11) between the ADC output and the buffer register input help to minimize the digital transient currents which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register input capacitance acts as a low-pass filter to slow down the fast edges.

A typical CMOS gate combined with PCB trace and a through-hole will create a load of approximately 10 pF. A logic output slew rate of 1 V/ns will produce 10 mA of dynamic current if there is no isolation resistor:

$$\Delta I = C\frac{\Delta v}{\Delta t} = 10\,\text{pF} \times 1\frac{\text{v}}{\text{ns}} = 10\,\text{mA}. \qquad \text{(C.2)}$$

A 500 Ω series resistors will minimize this output current and result in a rise and fall time of approximately 11ns when driving the 10 pF input capacitance of the register:

$$t_r = 2.2 \times \tau = 2.2 \times R \times C = 2.2 \times 500\,\Omega \times 10\,\text{pF} = 11\,\text{ns}. \qquad \text{(C.3)}$$

TTL registers should be avoided because they can appreciably add to the dynamic switching currents due to their higher input capacitance. The buffer register and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface.

Since digital noise immunity is on the order of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, steps should be taken to reduce the digital ground plane impedance, thereby maintaining the digital noise margins at an acceptable level. Under no circumstances should the voltage between the two ground planes exceed 300 mV, or the ICs may be damaged.

Separate power supplies for analog and digital circuits are also highly desirable, even if the voltages are the same. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (VD), it should either be powered from a separate analog supply or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane, as shown in **Figure C.12 below**.

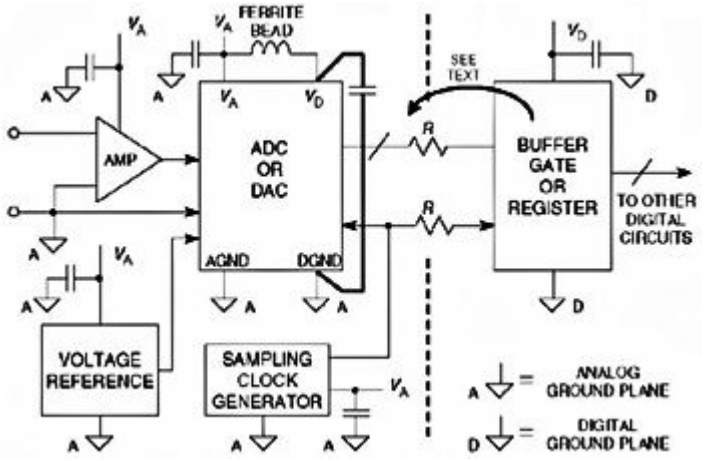


***Figure C.12: Grounding and decoupling points.***

In some cases it might not be possible to connect VD to the analog supply. Some of the newer, high-speed ICs may have their analog circuits powered by 5 V, but the digital interface is powered by 3 V to interface to 3 V logic. In this case, the 3 V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with the power trace that connects the pin to the 3 V digital logic supply.

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system SNR, as will be discussed shortly.

**Sampling Clock Considerations**

In a high-performance sampled data system, a low phase-noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock because sampling clock jitter modulates the analog input/output signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC. The effect of sampling clock jitter on ADC signal-to-noise ratio (SNR) is given approximately by the equation:

$$SNR = 20 \log_{10} \left[ \frac{1}{2\pi f t_j} \right] \qquad (C.4)$$

where SNR is the SNR of a perfect ADC of infinite resolution where the only source of noise is that

caused by the rms sampling clock jitter, tj. Note that f in the equation is the analog input frequency. Just working through a simple example, if tj 50 ps rms, f 100 kHz, then SNR 90 dB, equivalent to about 15-bit dynamic range.

It should be noted that tj in the above example is the root-sum-square (rss) value of the external clock jitter and the internal ADC clock jitter (called aperture jitter). However, in most high-performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to ensure that the sampling clock is as noise-free as possible and has the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low jitter (less than 5 ps rms) CMOS compatible outputs.

Ideally, the sampling clock crystal oscillator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher-frequency multipurpose system clock which is generated on the digital ground plane.

It must then pass from its origin on the digital ground plane to the ADC on the analog ground plane. Ground noise between the two planes adds directly to the clock signal and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics.

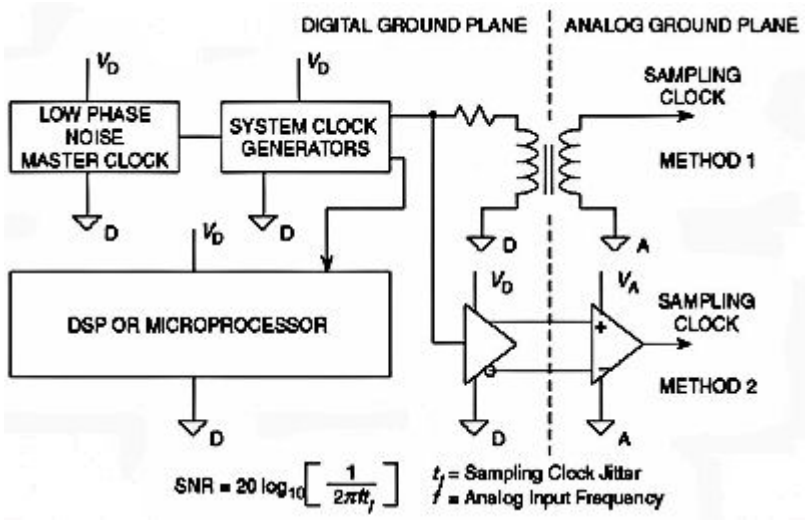


***Figure C.13: Sampling clock distribution from digital to analog ground planes***.

This can be somewhat remedied by transmitting the sampling clock signal as a differential signal using either a small RF transformer as shown in **Figure C.13 above** or a high-speed differential driver and receiver IC. If an active differential driver and receiver are used, they should be ECL to minimize phase jitter. In a single 5 V supply system, ECL logic can be connected between ground and 5 V (PECL), and the outputs AC coupled into the ADC sampling clock input. In either case, the original master system clock must be generated from a low-phase noise crystal oscillator, and not the clock output of a DSP, microprocessor, or microcontroller.

To read **Part 2**, go to: **"Single-card grounding for multicard systems"**
To read **Part 3,** go to: **"Static and dynamic PCB effects"**

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