

P2597-B04

Tegra X1 Jetson CV-B

HDMI, USB, PCIe, SATA, Gbe

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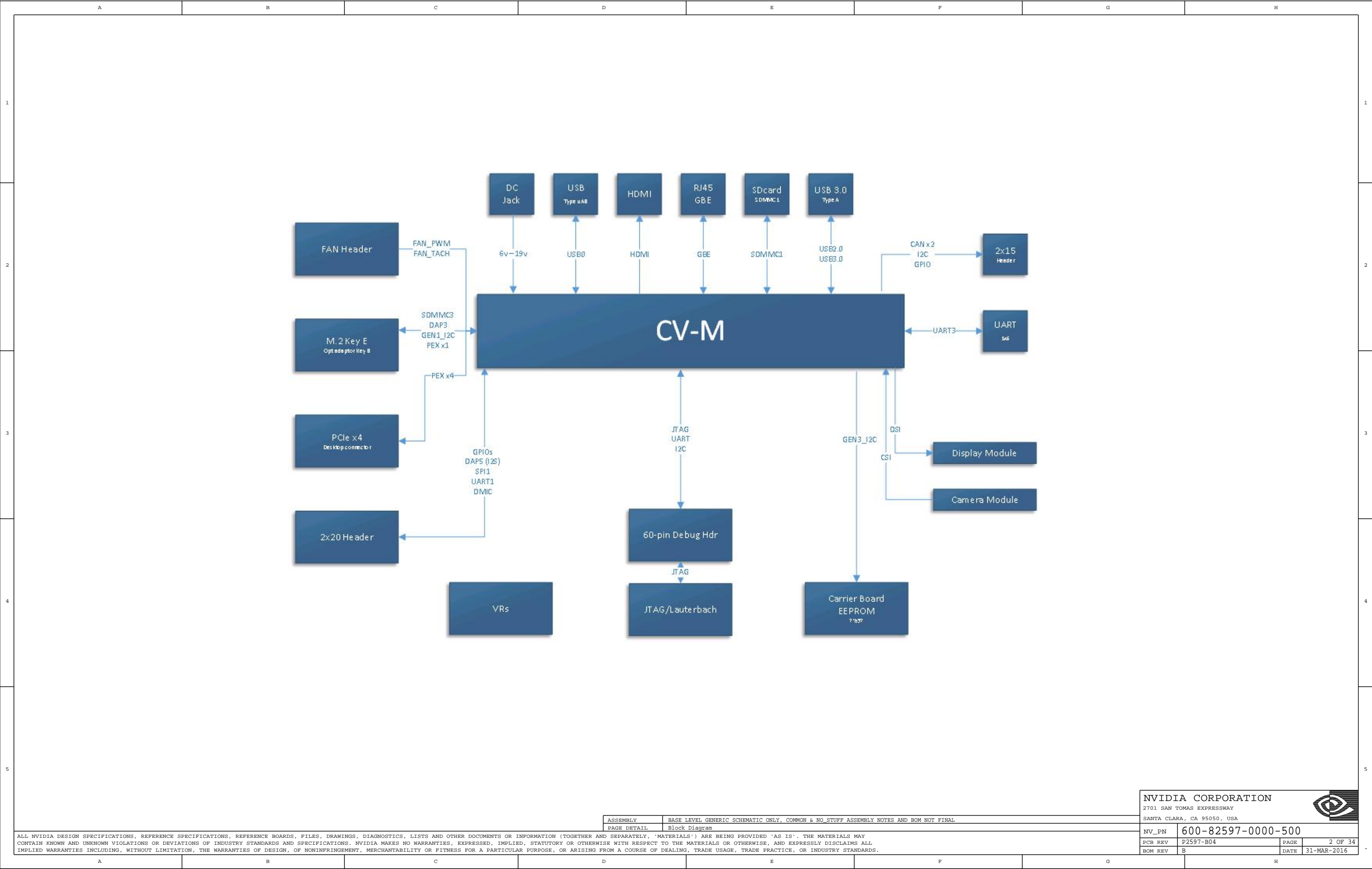
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P2597 I2C Port Assignments

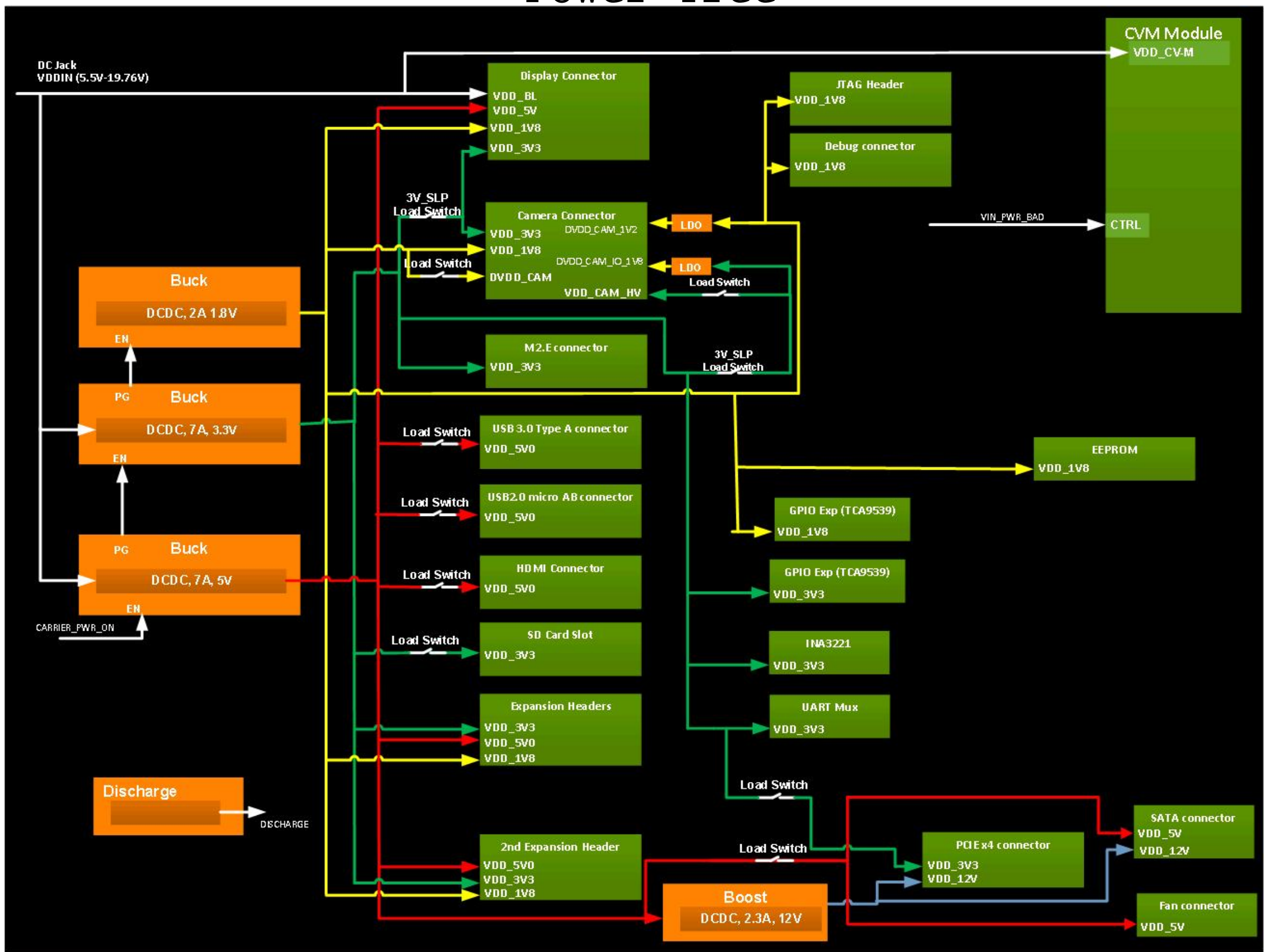
Slave Device	BUS:Device address
INA3221 (Power measurement)	I2C Gen 2 : 7'h42
INA3221 (Power measurement)	I2C Gen 2 : 7'h43
TCA9539 (GPIO Expander)	I2C Gen 2 : 7'h74
TCA9539 (GPIO Expander)	I2C Gen 2 : 7'h77
BOARDID EEPROM	I2C Gen 3 : 7'57h

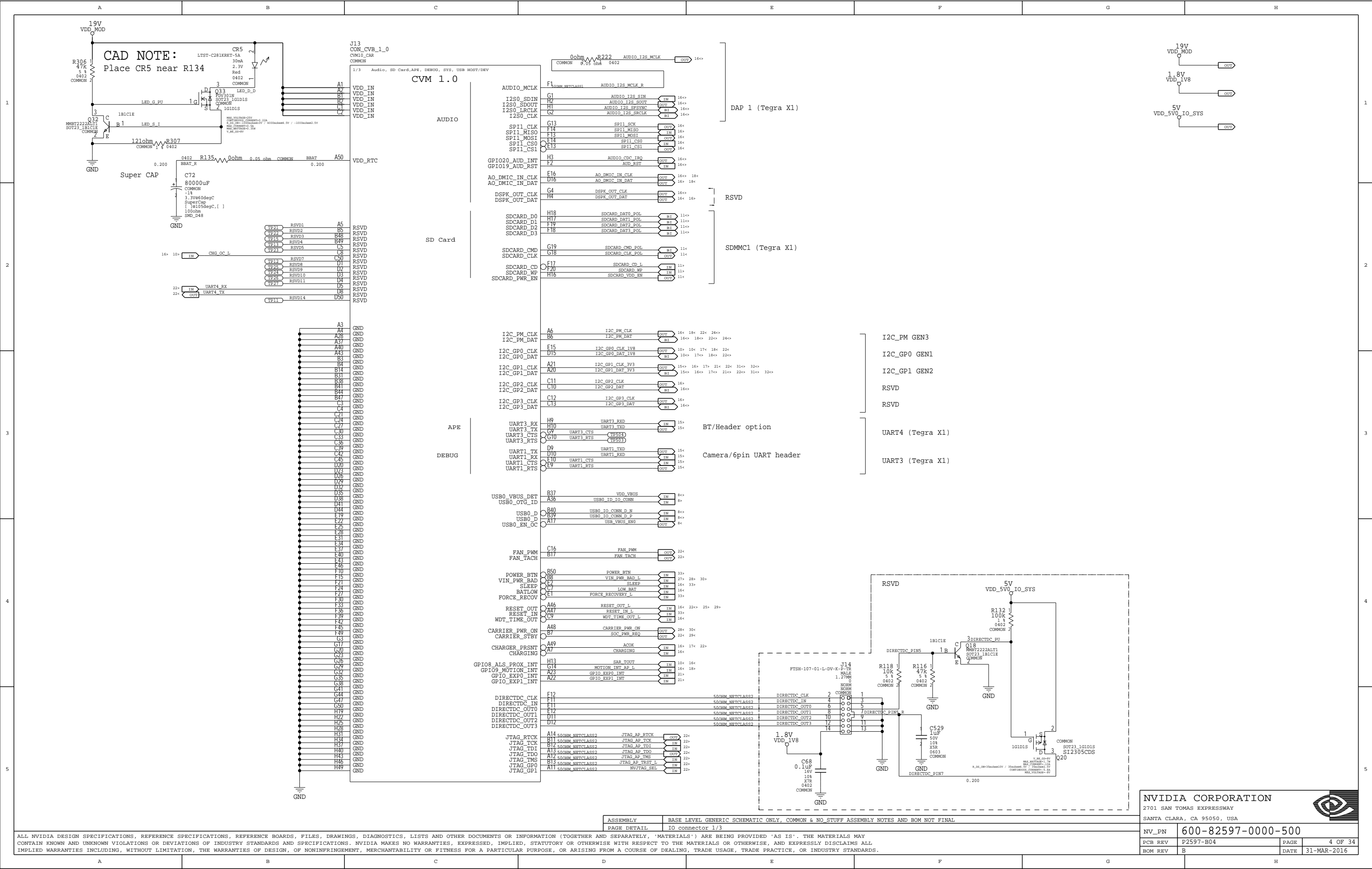
P2180 I2C Port Assignments

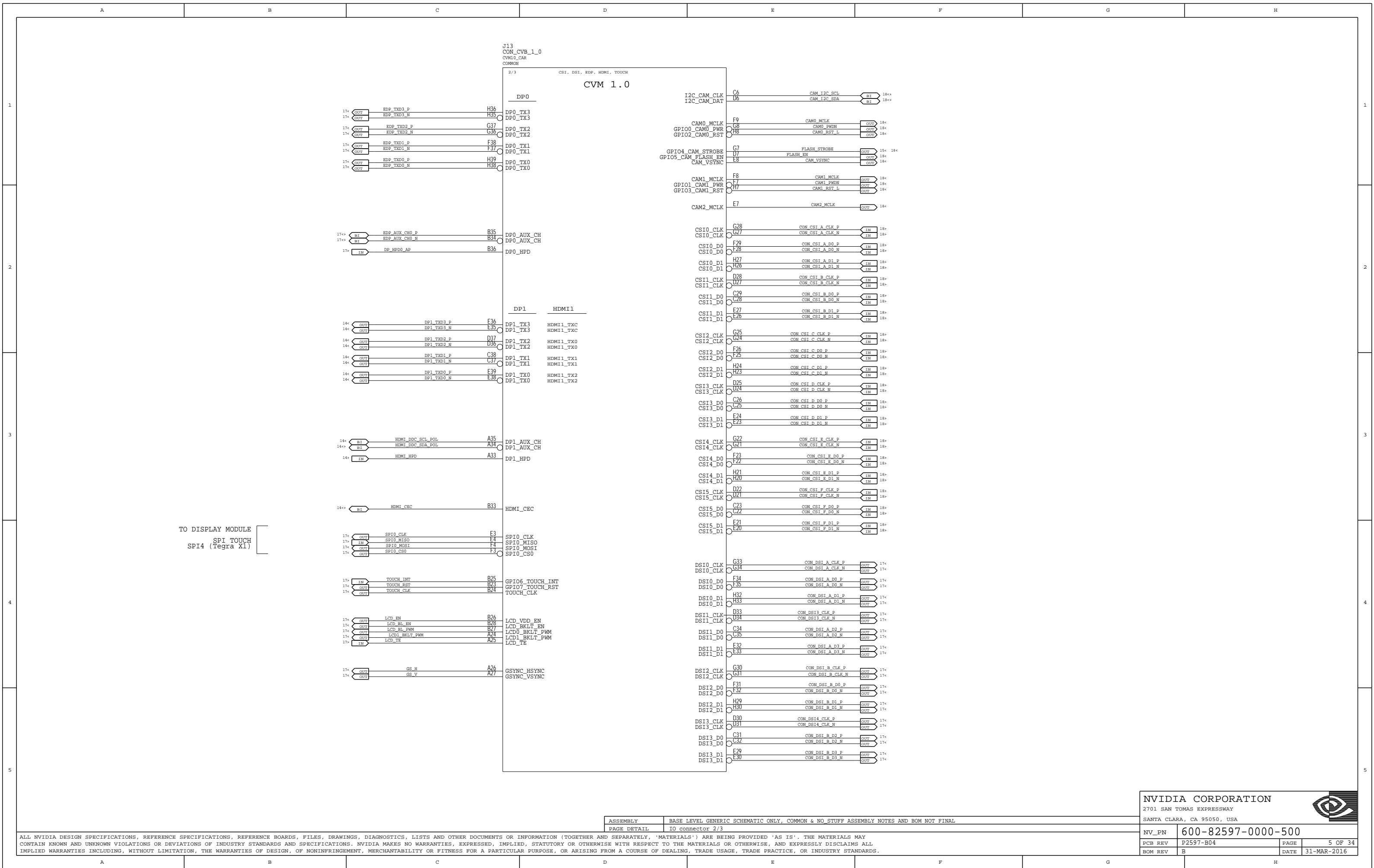
Slave Device	BUS:Device address
TMP451 (Thermal)	I2C Gen 1 : 7'h4C
ADS1015 (ACA detection)	I2C Gen 2 : 7'h4A
INA226 (Power measurement)	I2C Gen 2 : 7'h46
INA3221 (Power measurement)	I2C Gen 2 : 7'h40

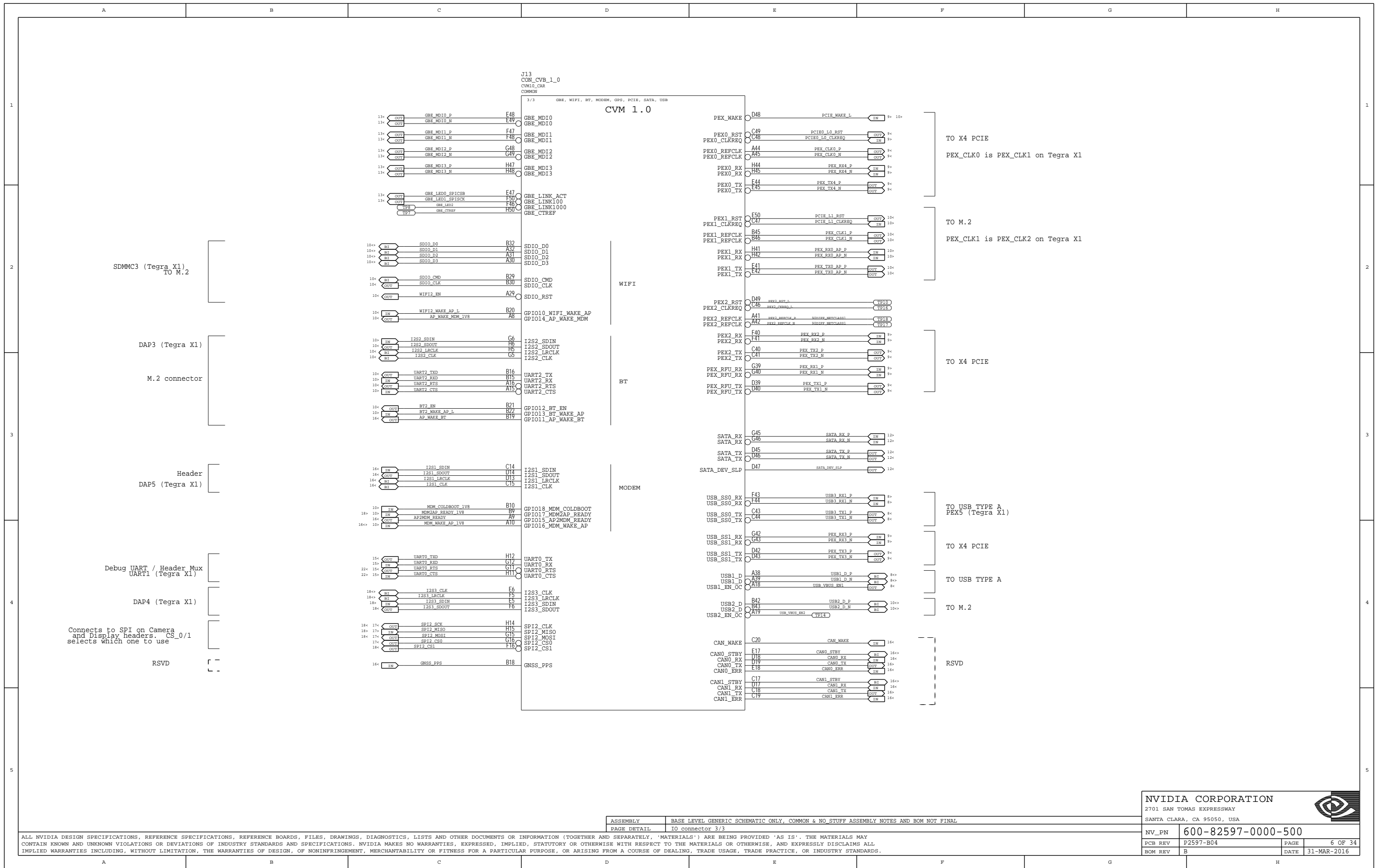


Power Tree

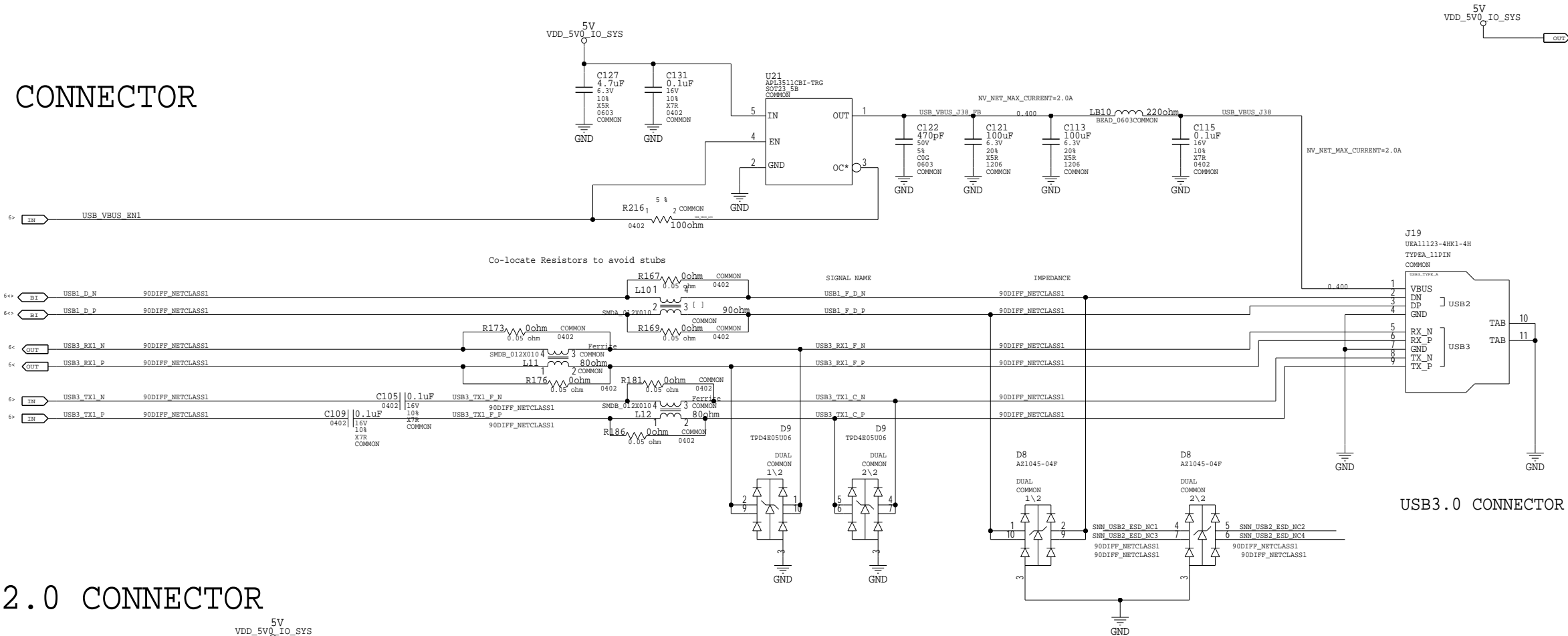




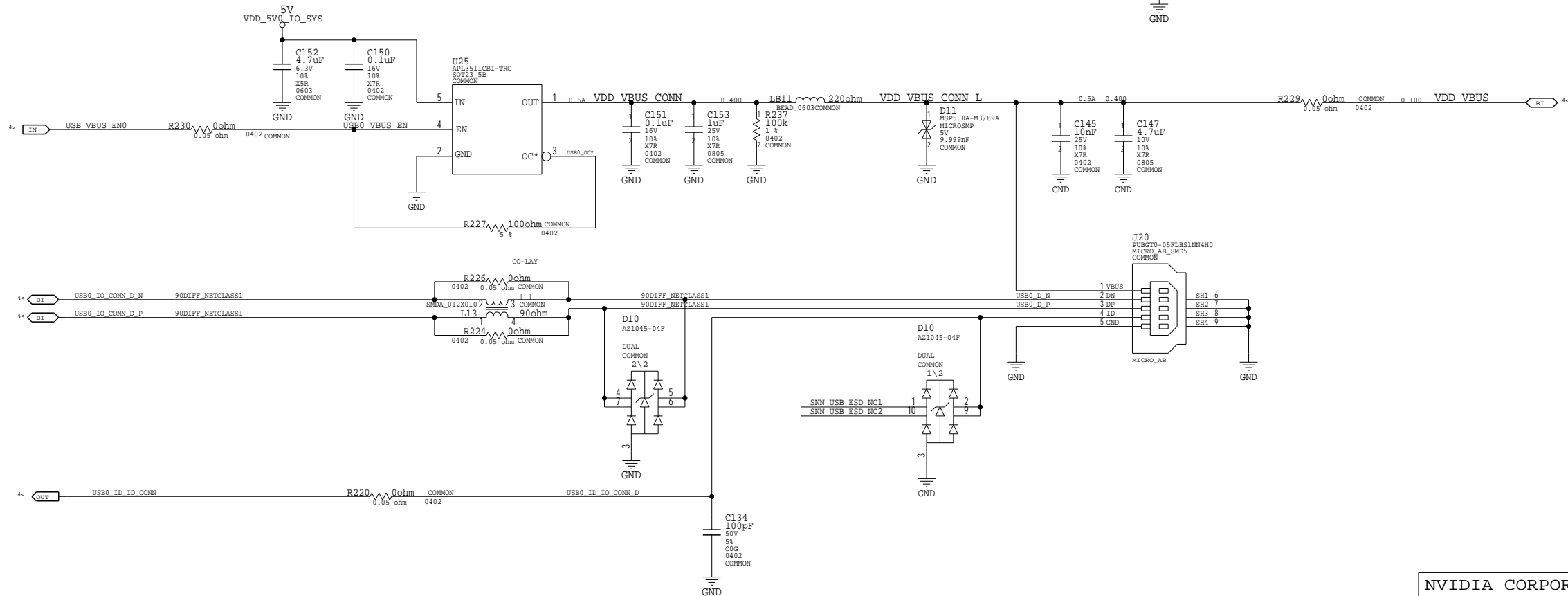




USB 3.0 TYPE A CONNECTOR



MICRO AB USB 2.0 CONNECTOR



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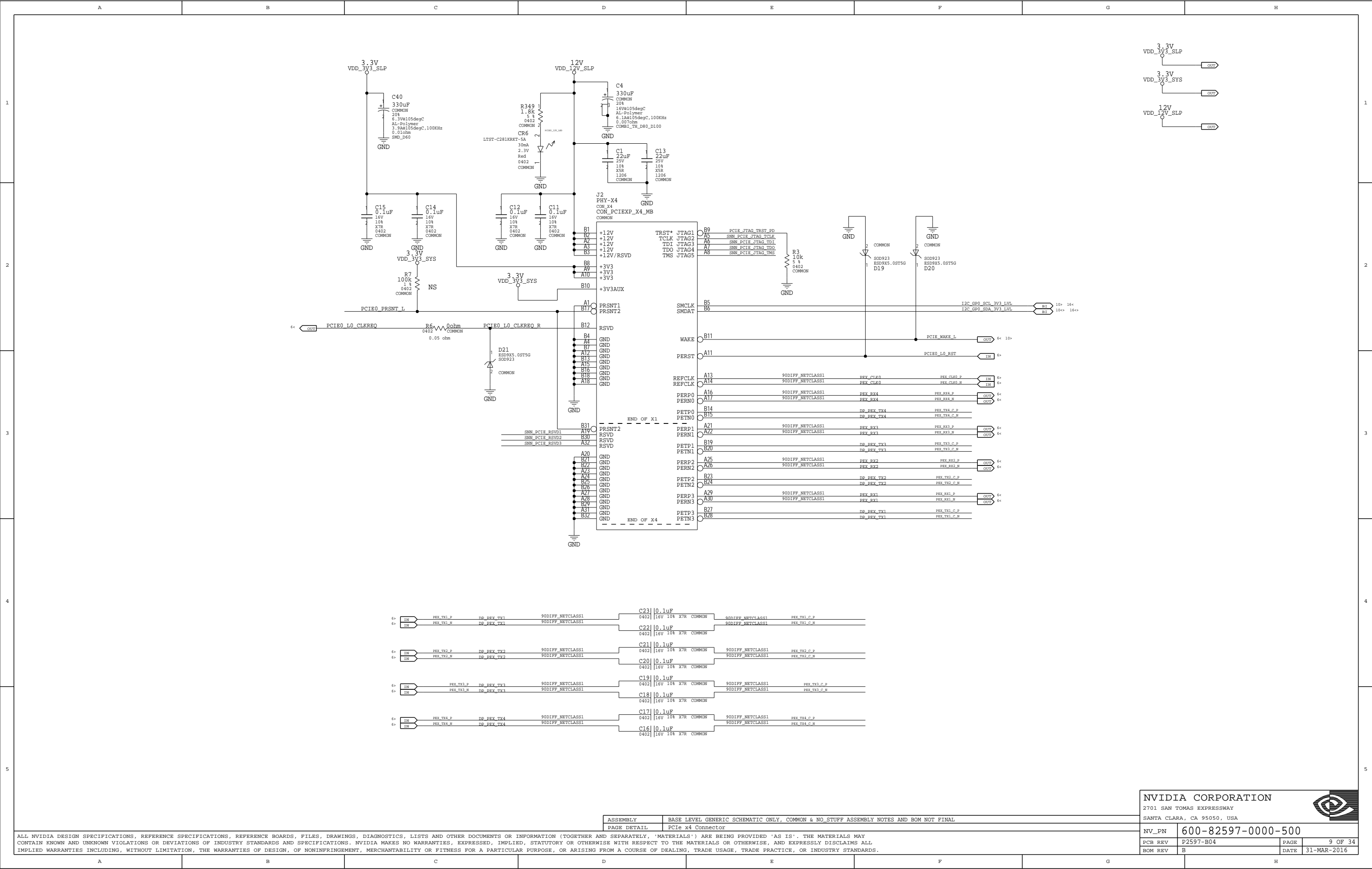
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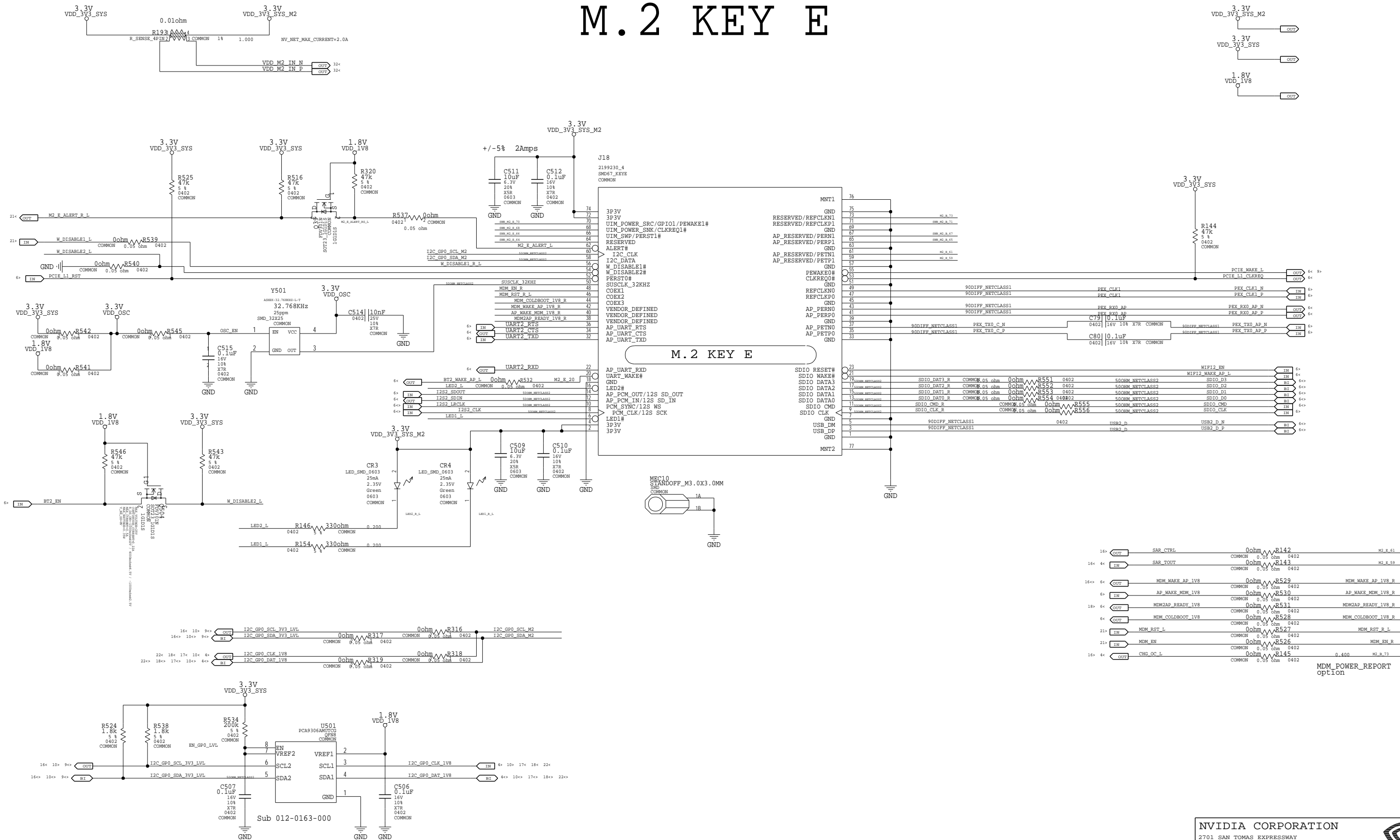
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PAGE DETAIL	PCIe x4 Connector

M.2 KEY E



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PAGE DETAIL	M.2 KEY E

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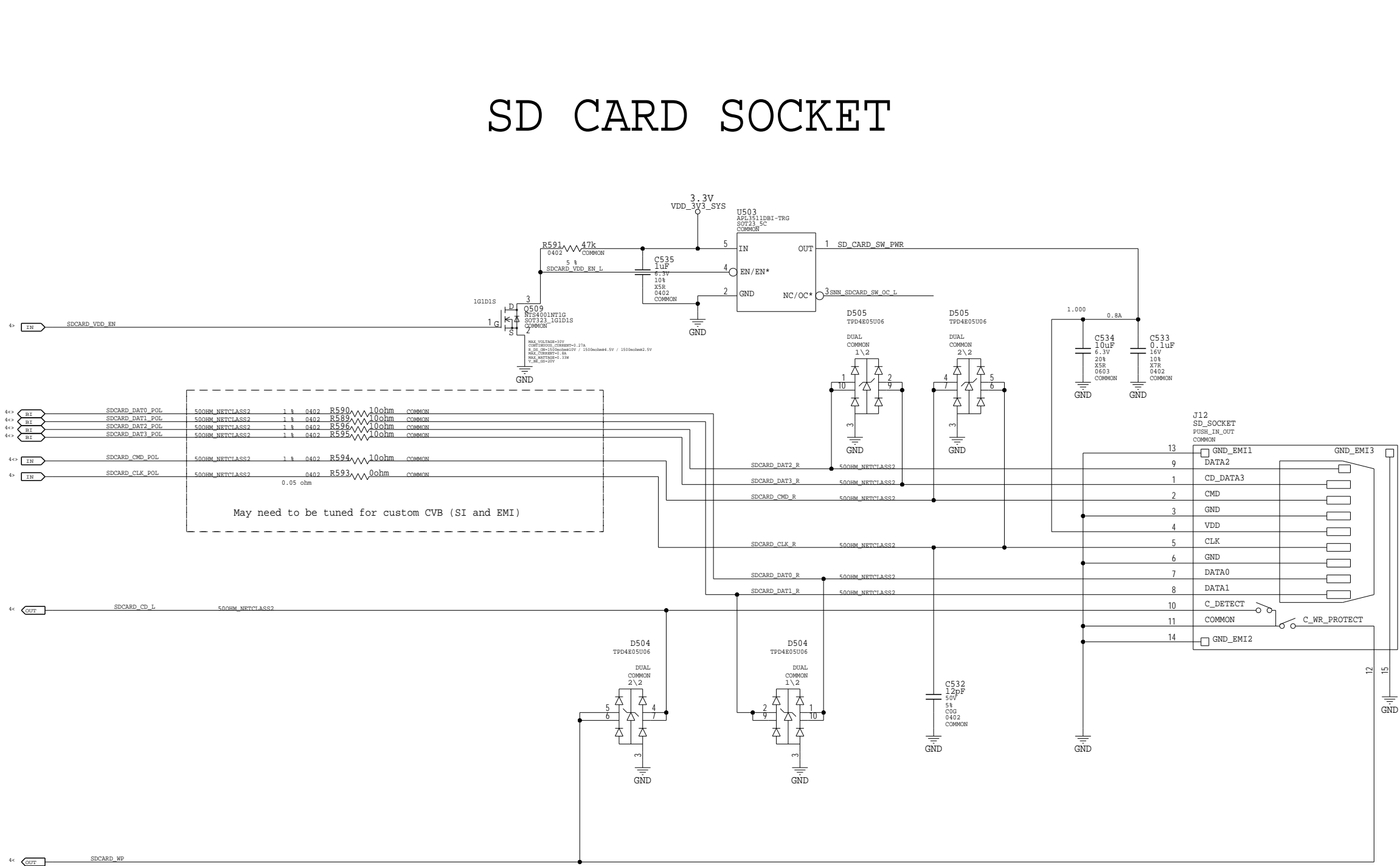
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SD CARD SOCKET



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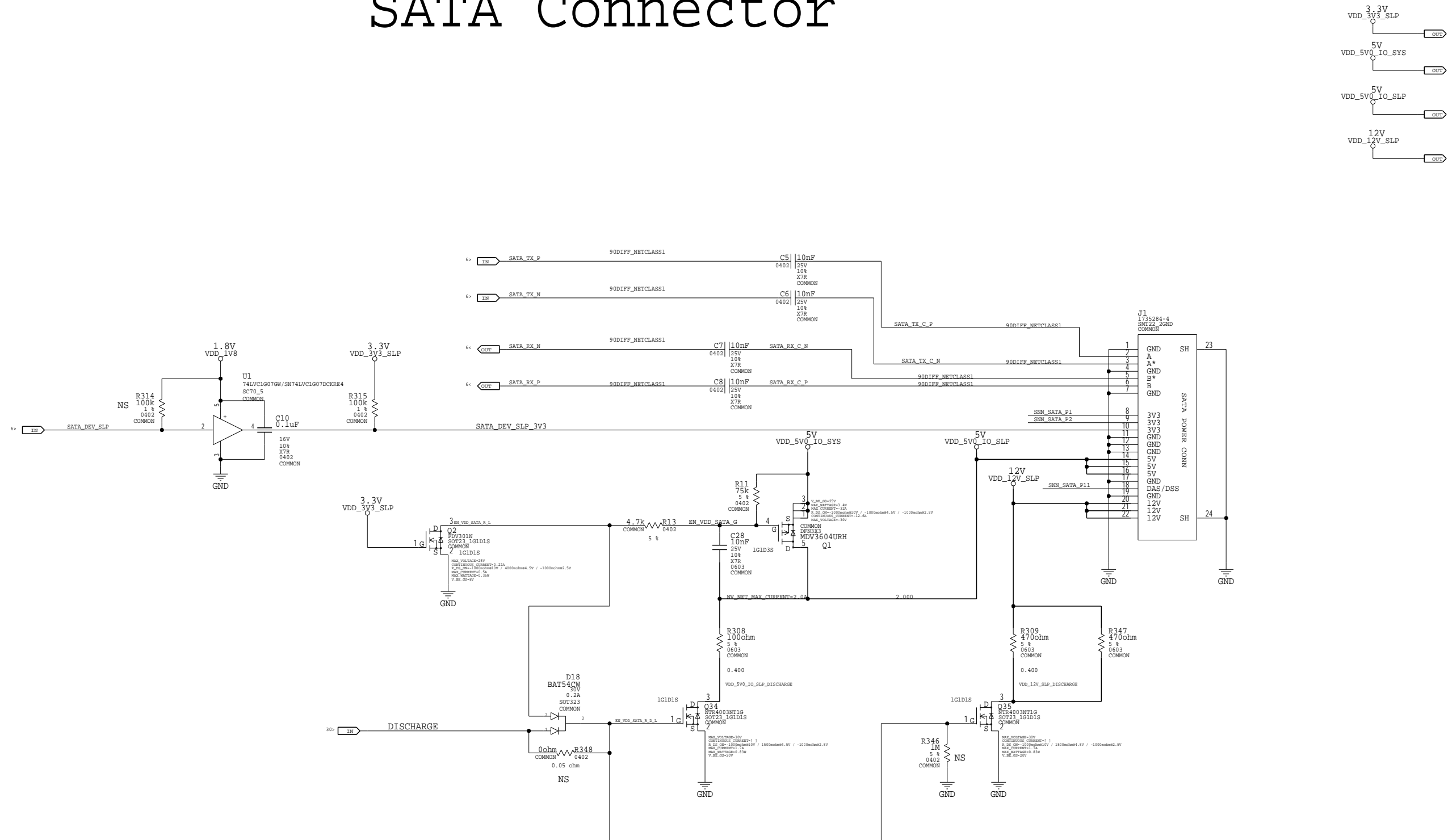
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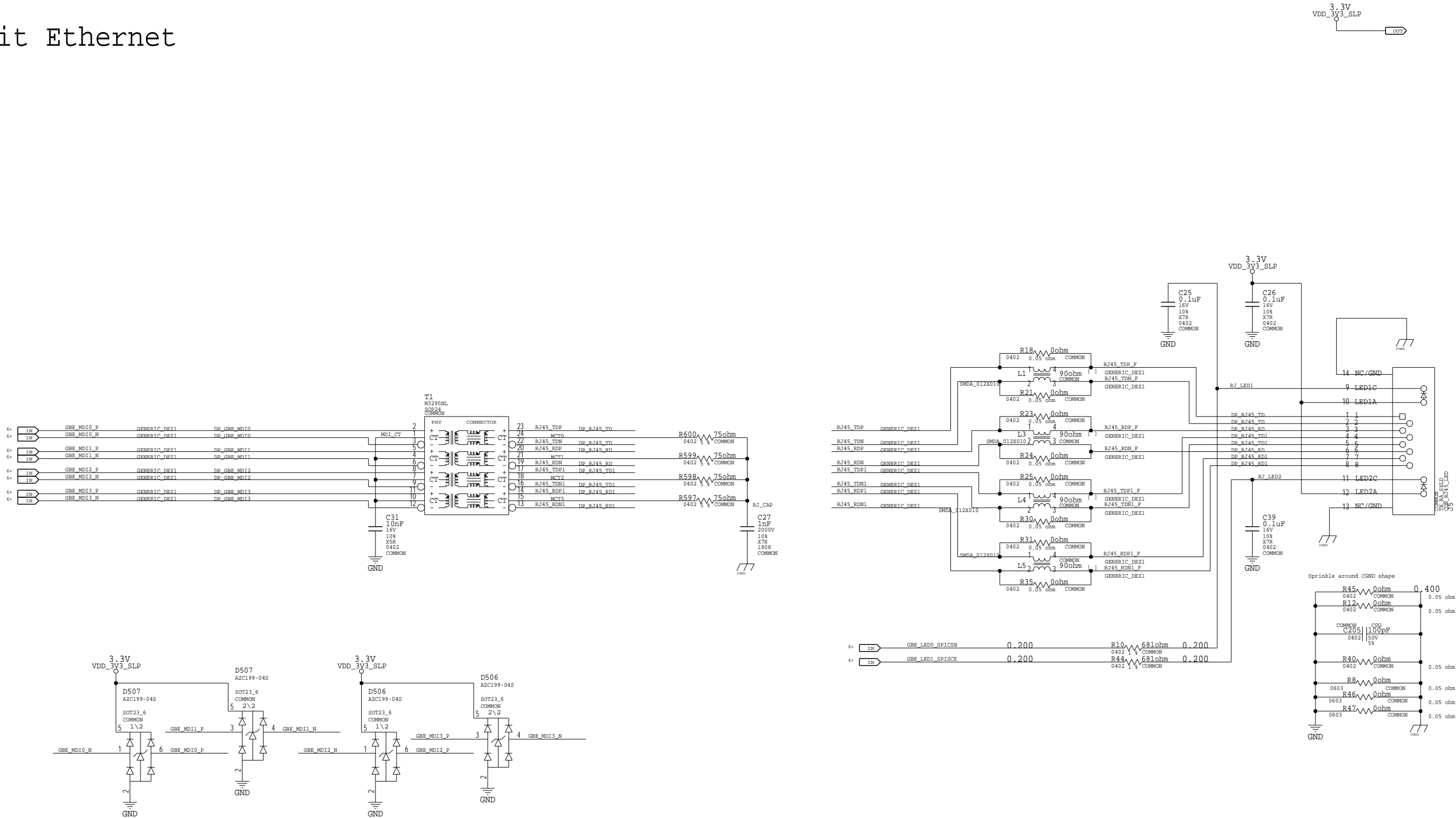
SATA Connector



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Gigabit Ethernet



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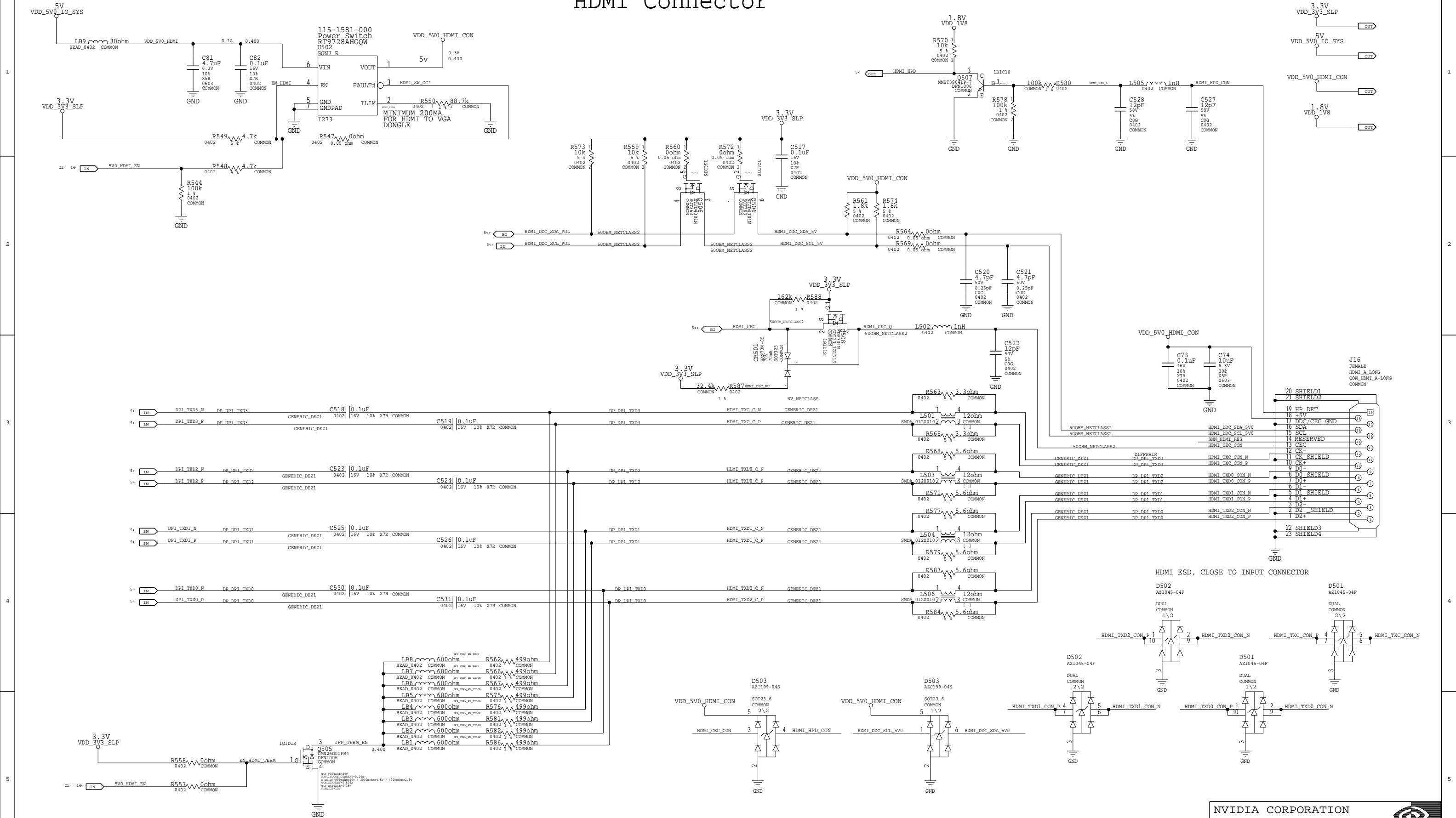
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HDMI Connector



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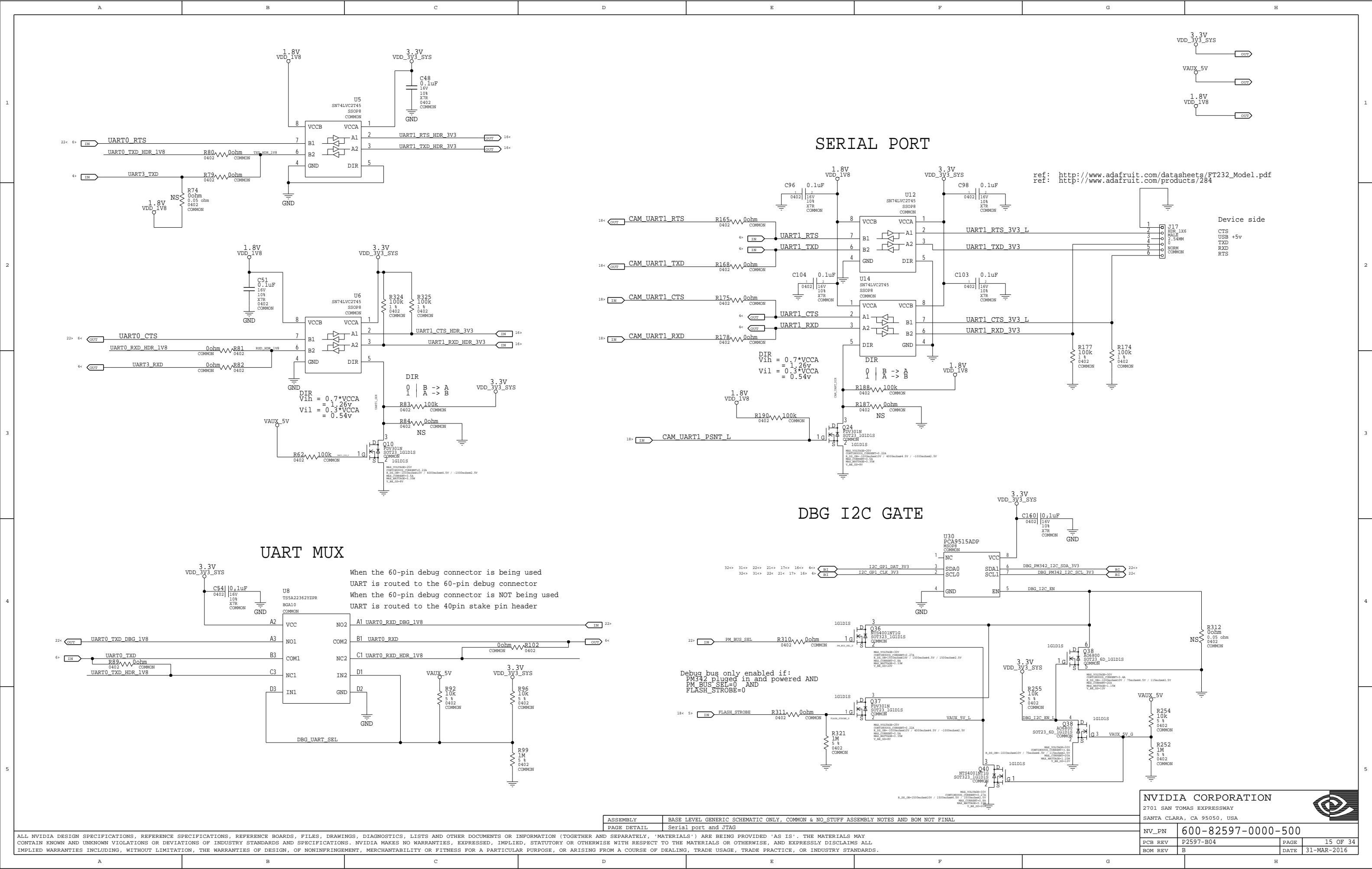
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UART MUX

When the 60-pin debug connector is being used
UART is routed to the 60-pin debug connector
When the 60-pin debug connector is NOT being used
UART is routed to the 40pin stake pin header

SERIAL PORT

DBG I2C GATE

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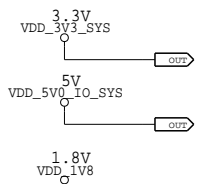
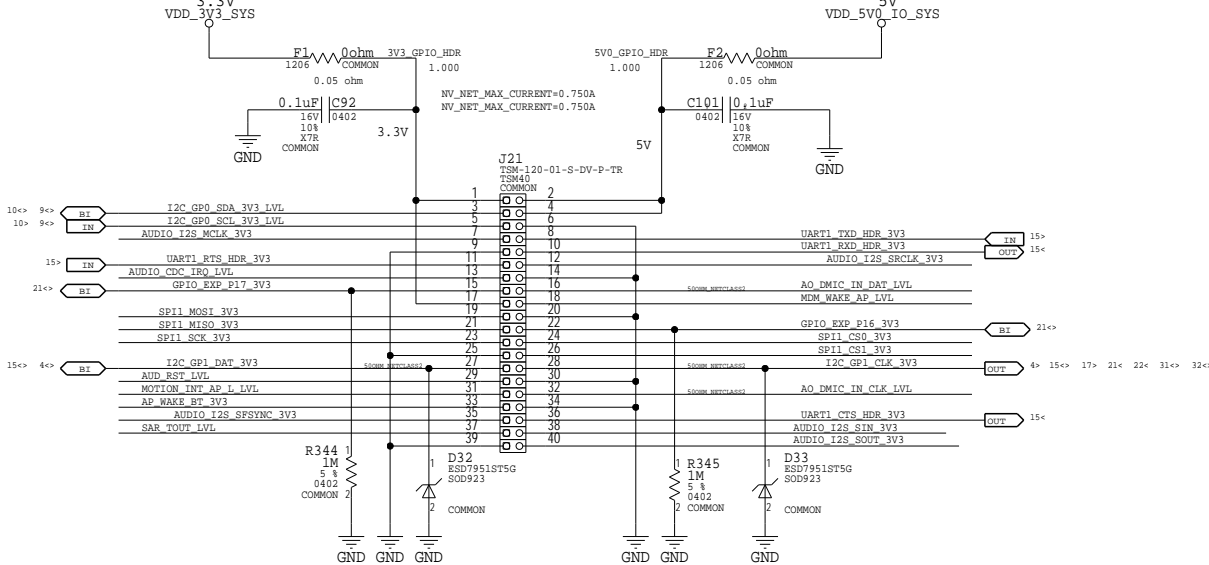
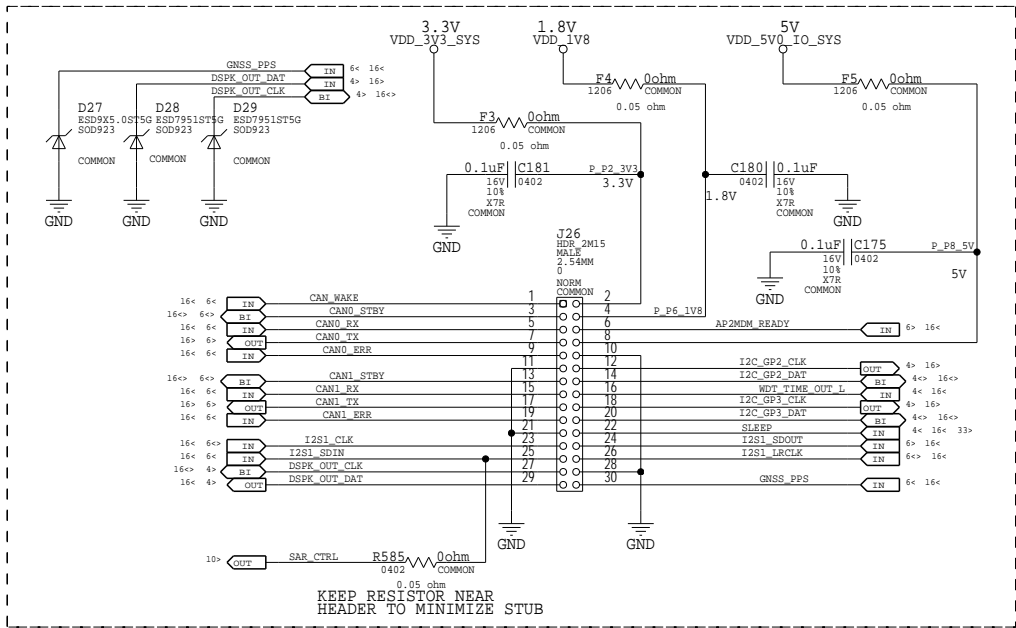
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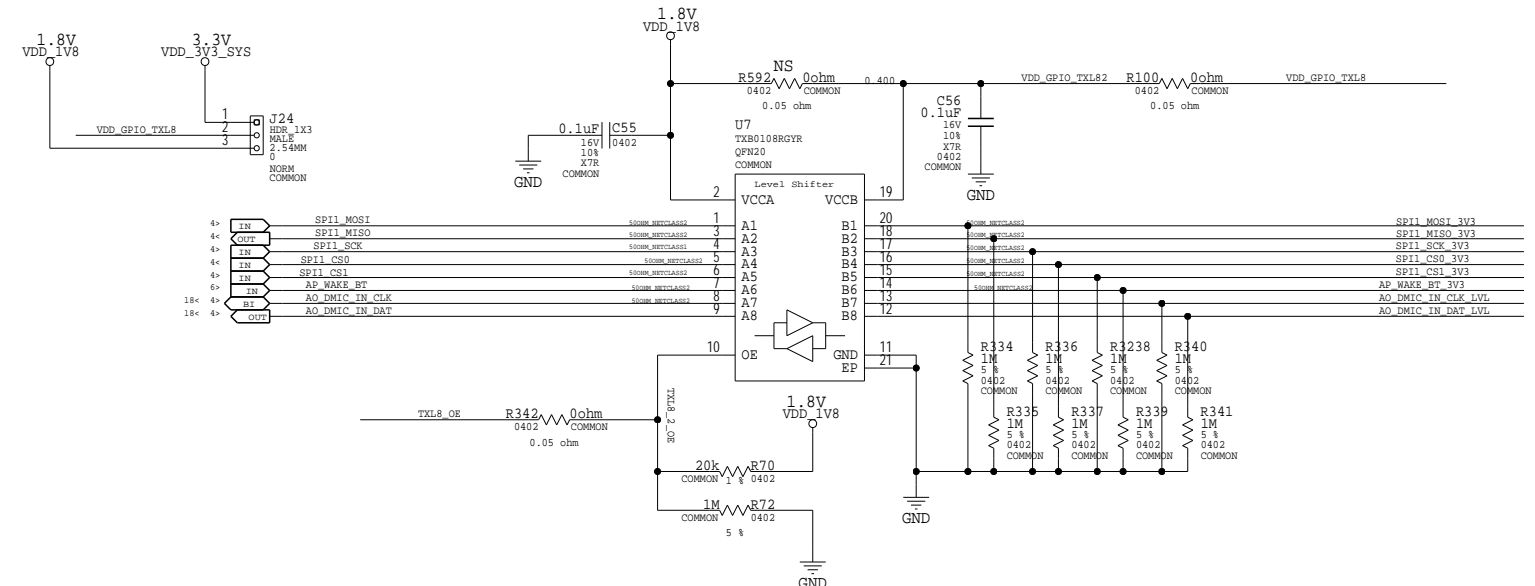
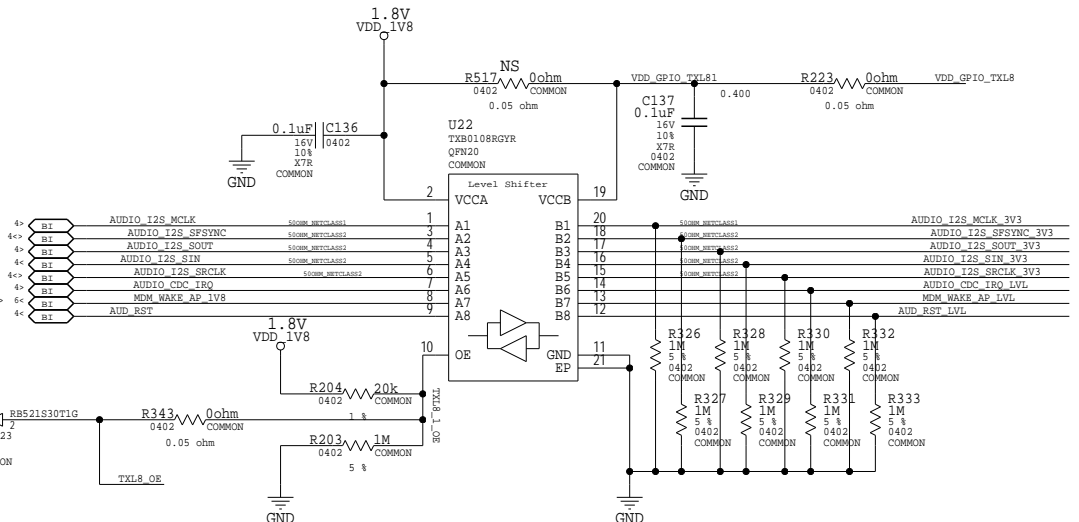
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PAGE DETAIL	Serial port and JTAG

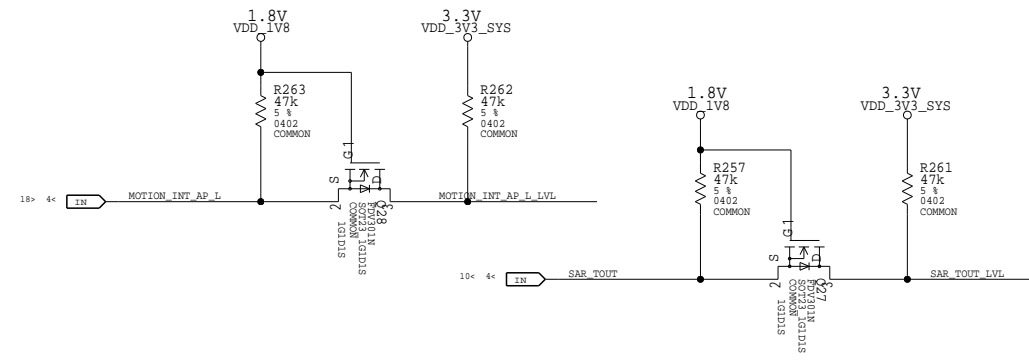
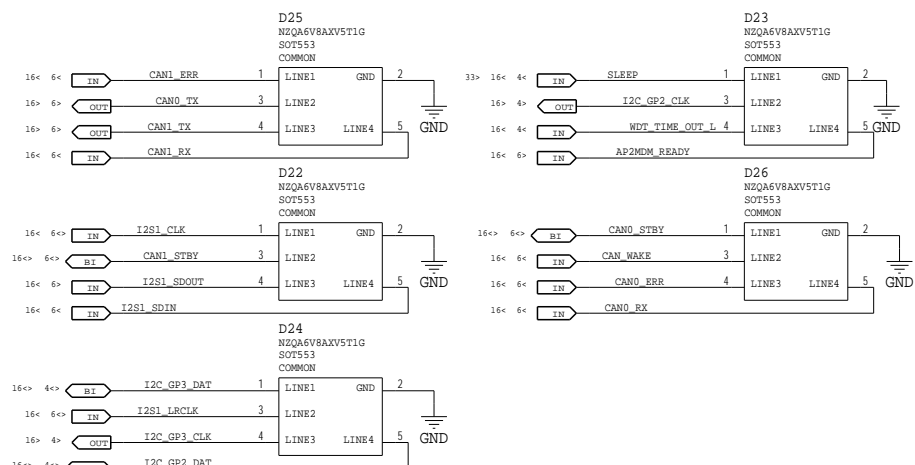
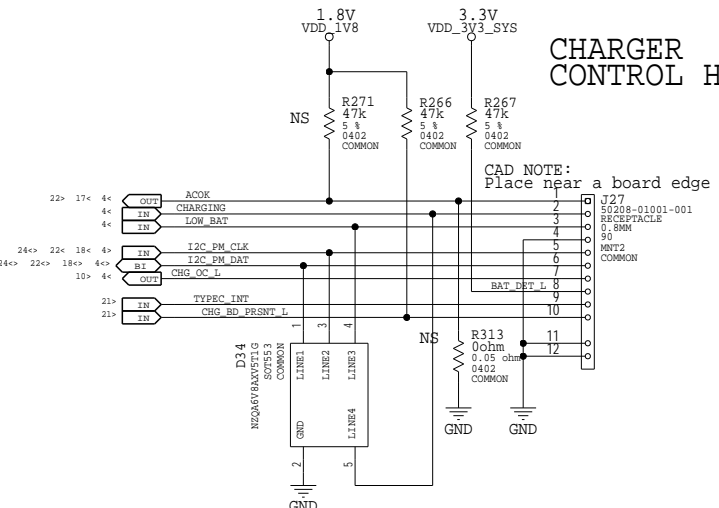
GPIO Expansion Headers



GPIO PK0 I2S5B_FS
GPIO PK2 I2S5B_SDO
GPIO PK1 I2S5B_SDIN



CHARGER CONTROL HDR



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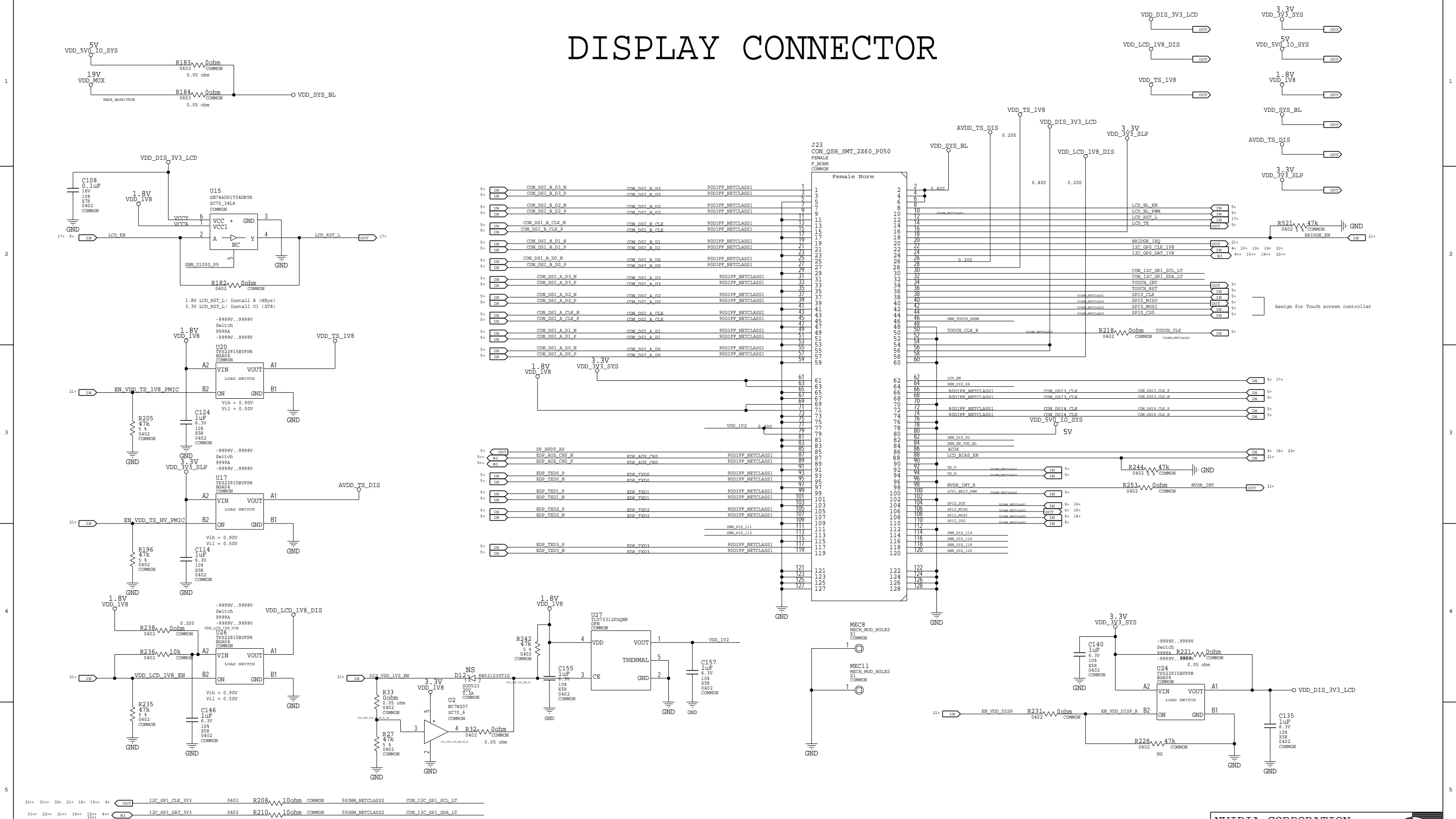


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PAGE DETAIL	IO Expansion Connector

DISPLAY CONNECTOR



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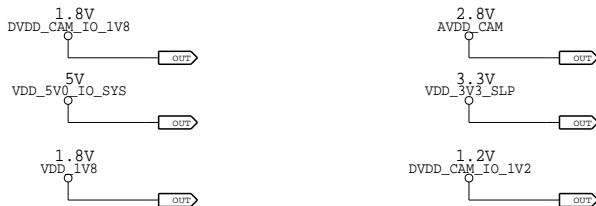
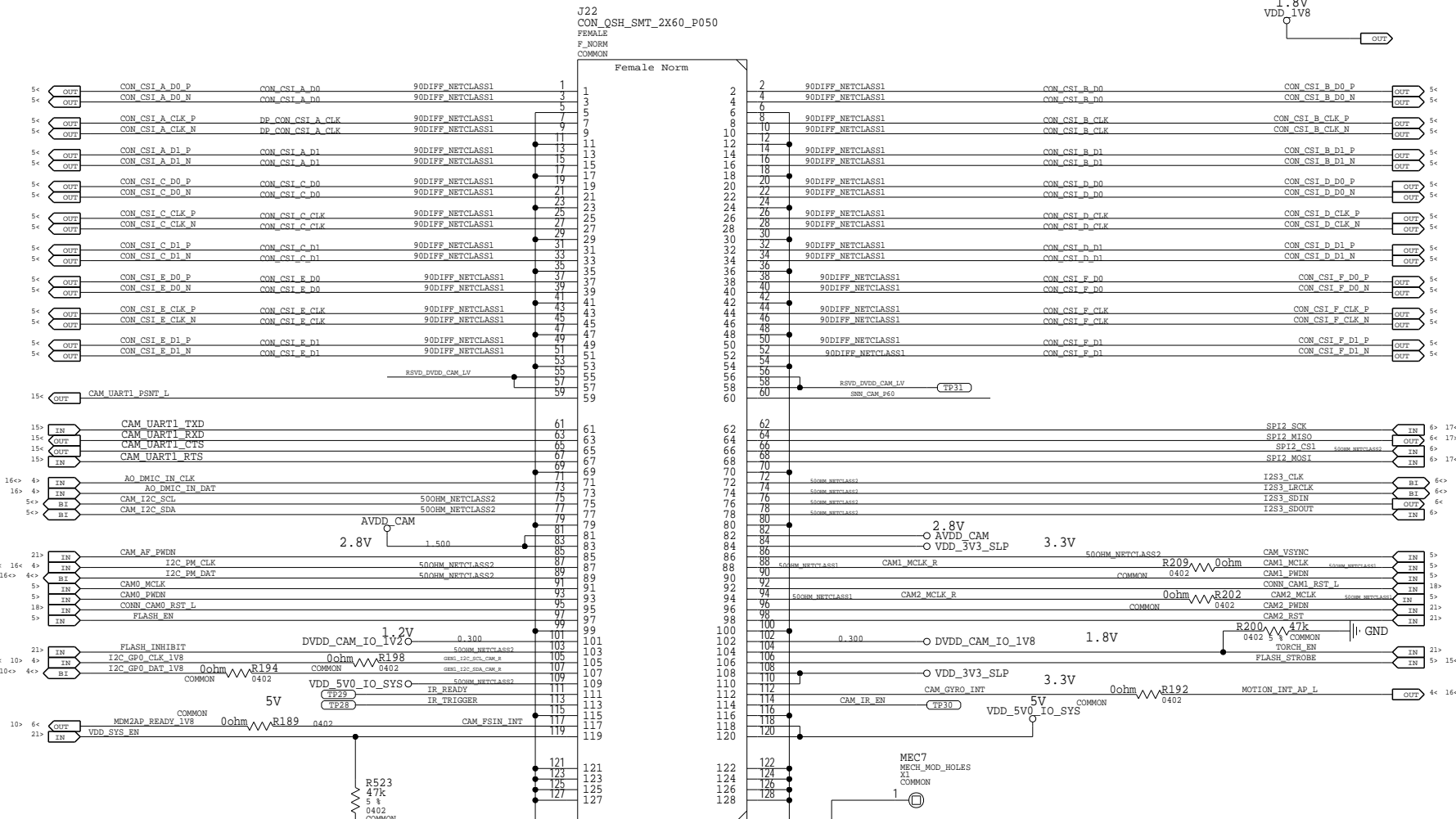
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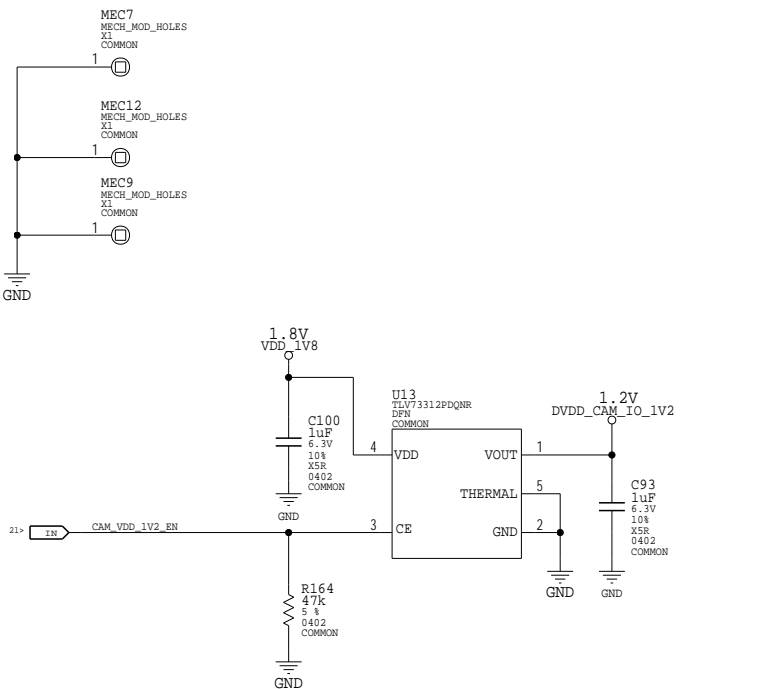
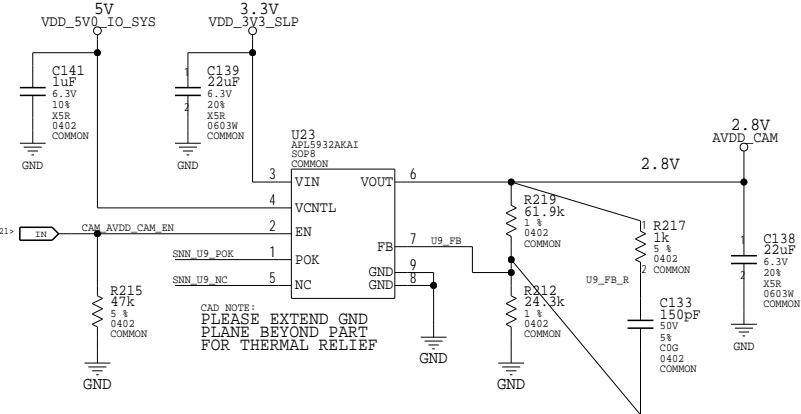
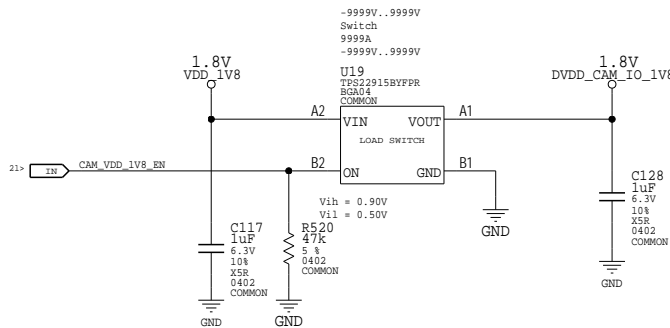
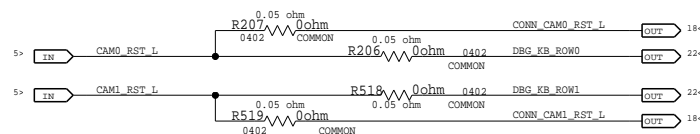
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Camera Expansion



DEBUG GPIO STUFF OPTIONS



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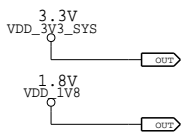
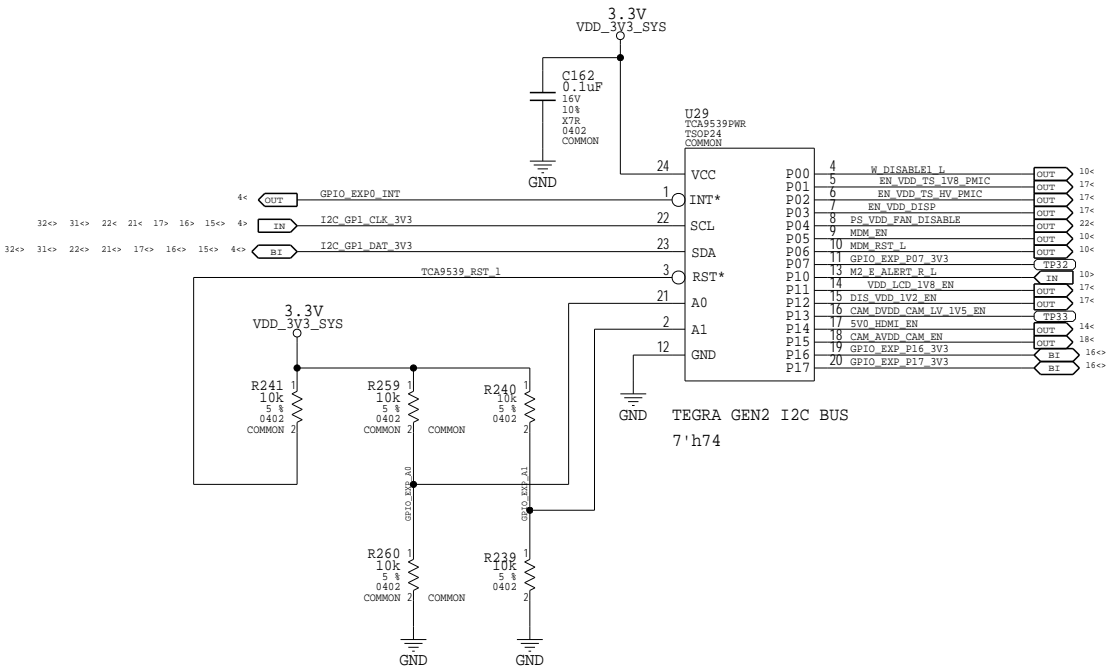
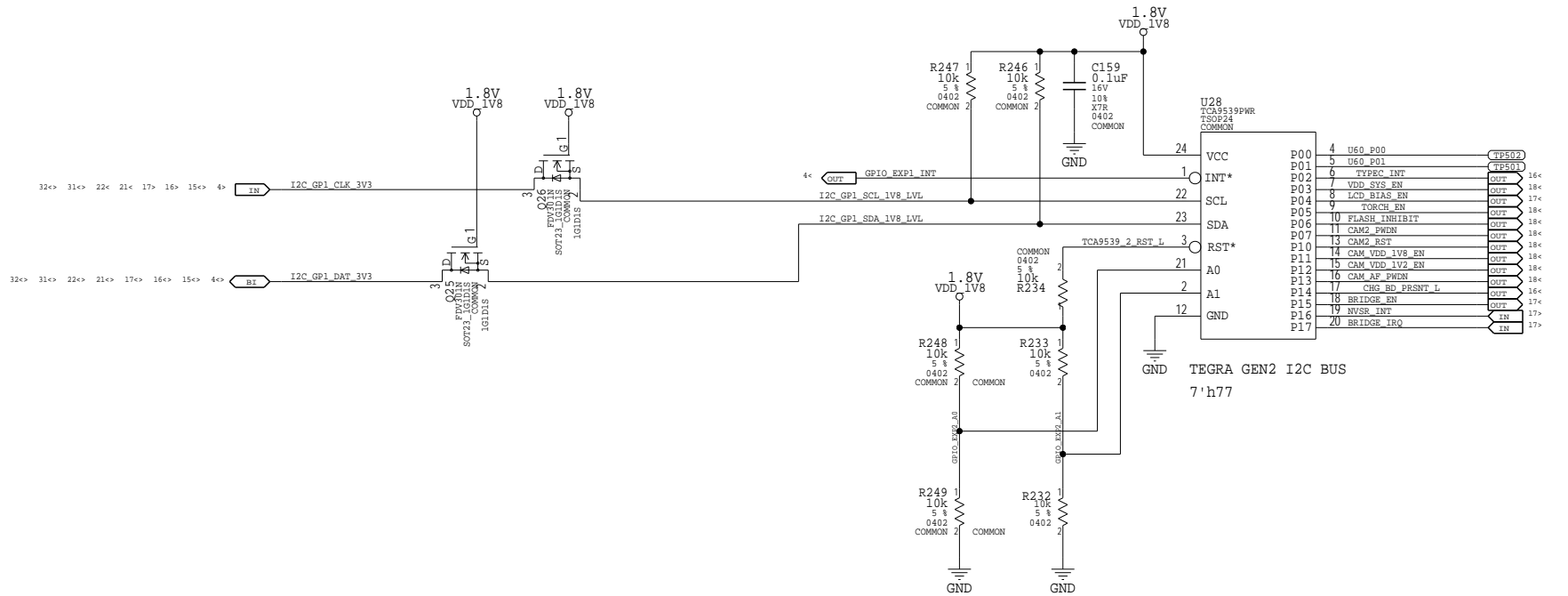
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GPIO EXPANDERS



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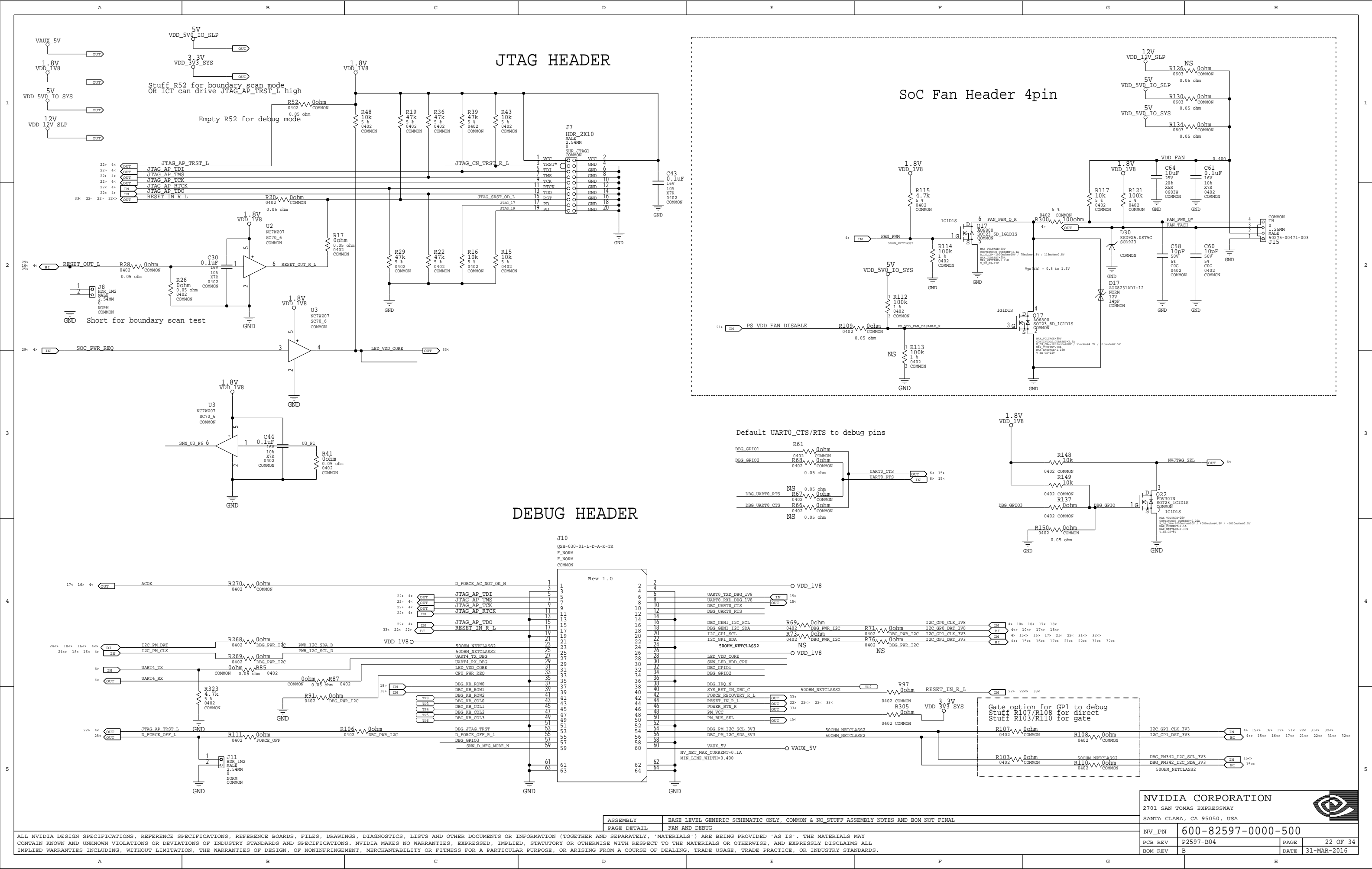
NV_PN 600-82597-0000-500

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BOM REV B

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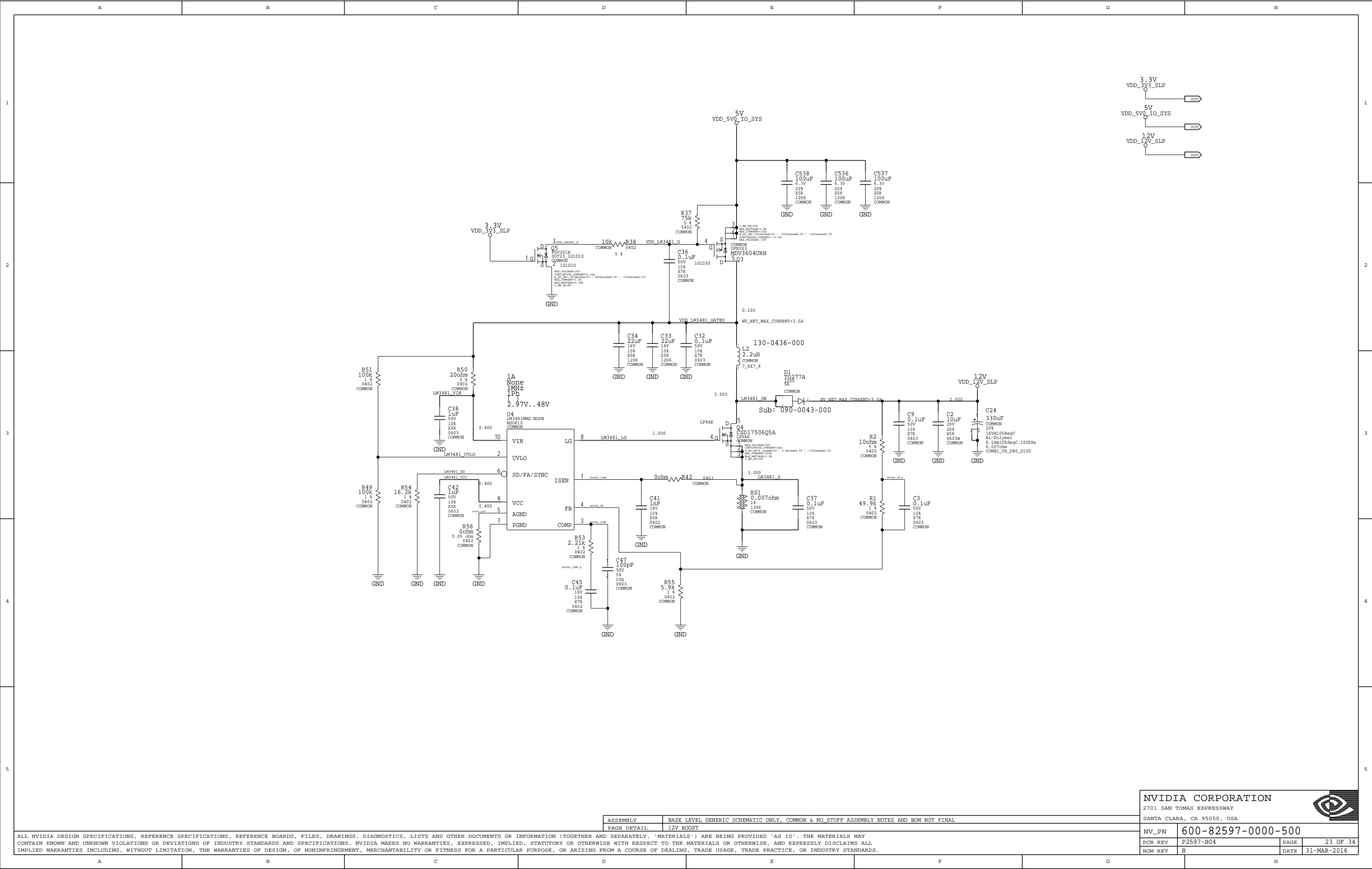
DATE 31-MAR-2016



JTAG HEADER

SoC Fan Header 4pin

DEBUG HEADER



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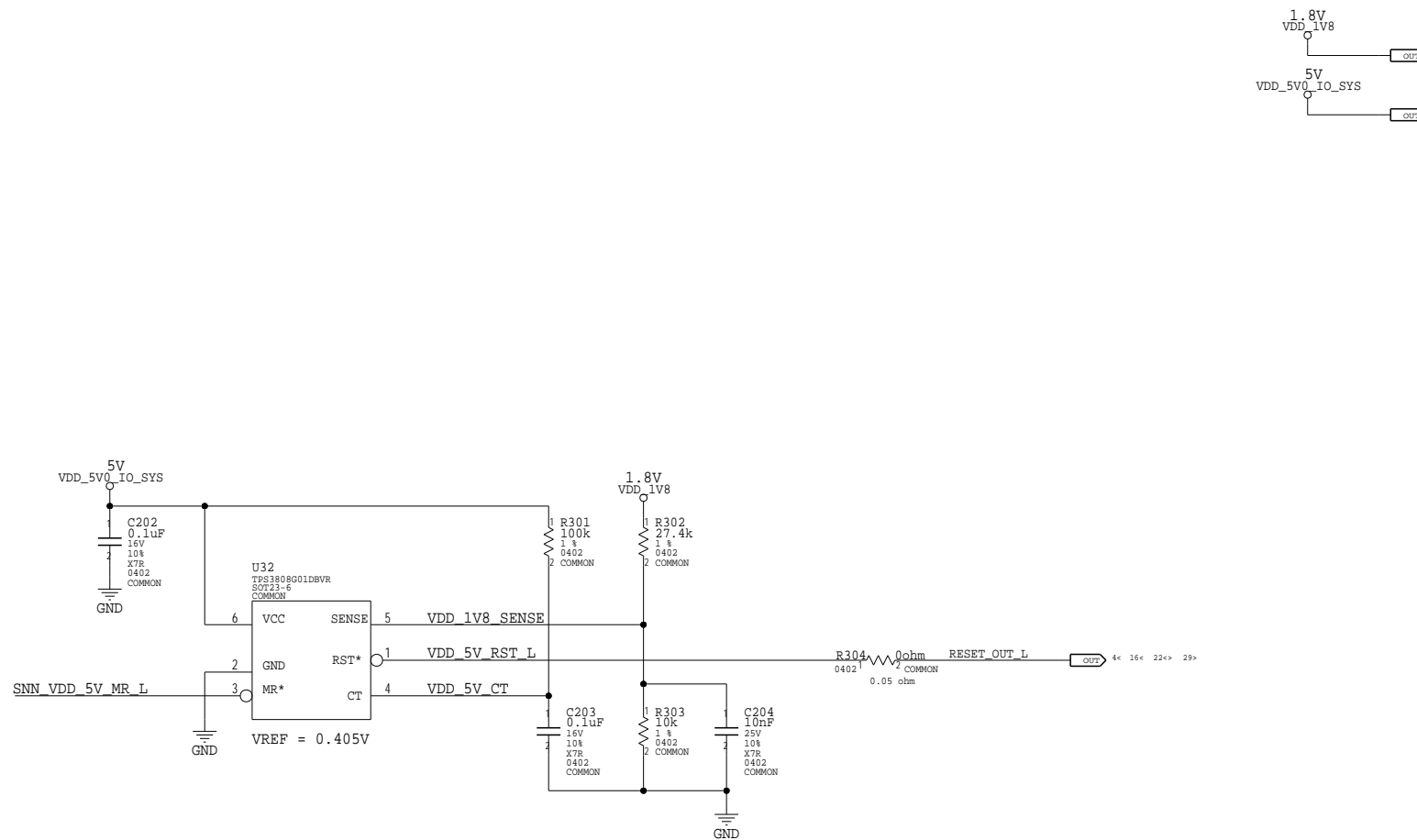
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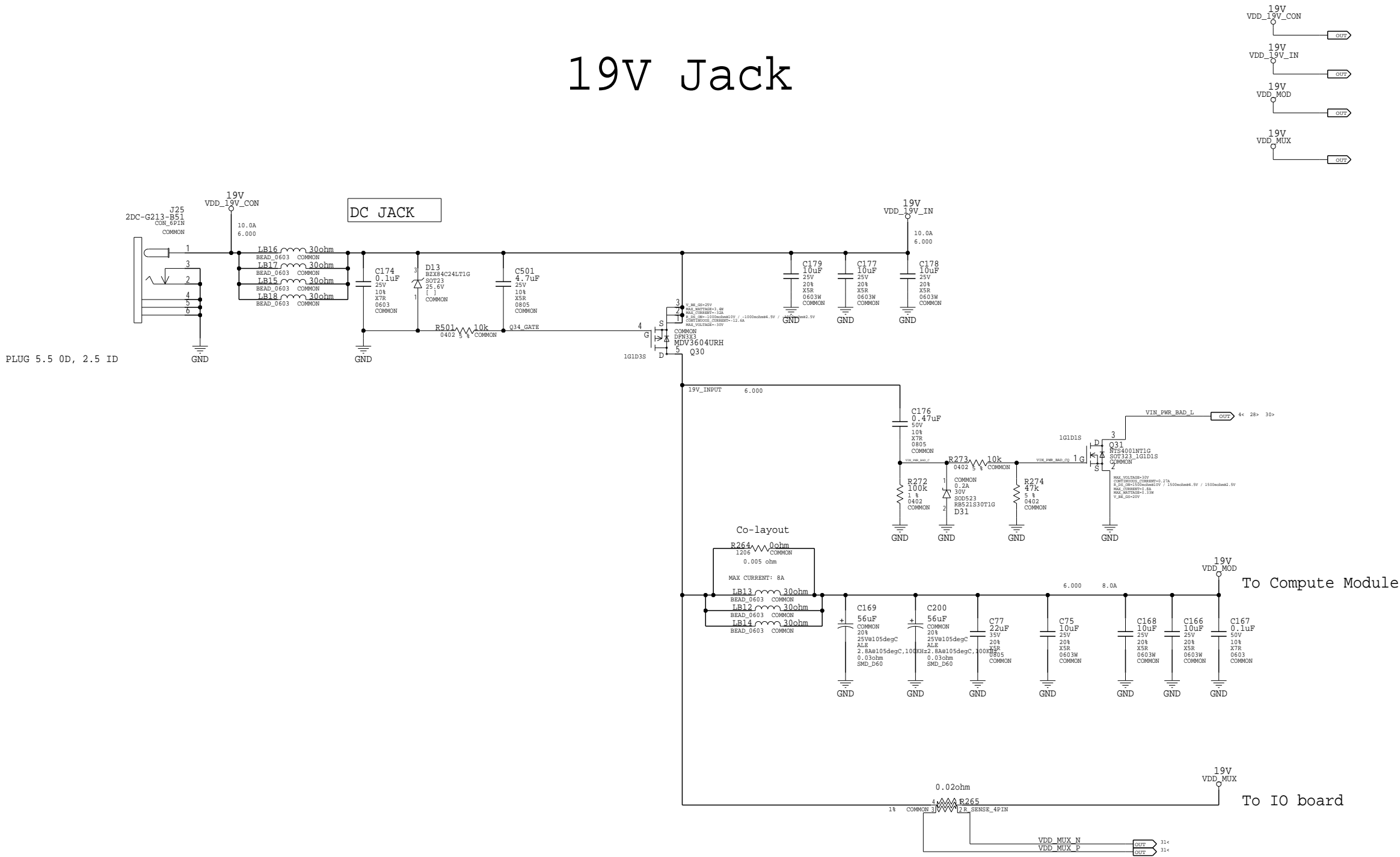
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PCB REV	P2597-B04	PAGE	26 OF 34																																							
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19V Jack



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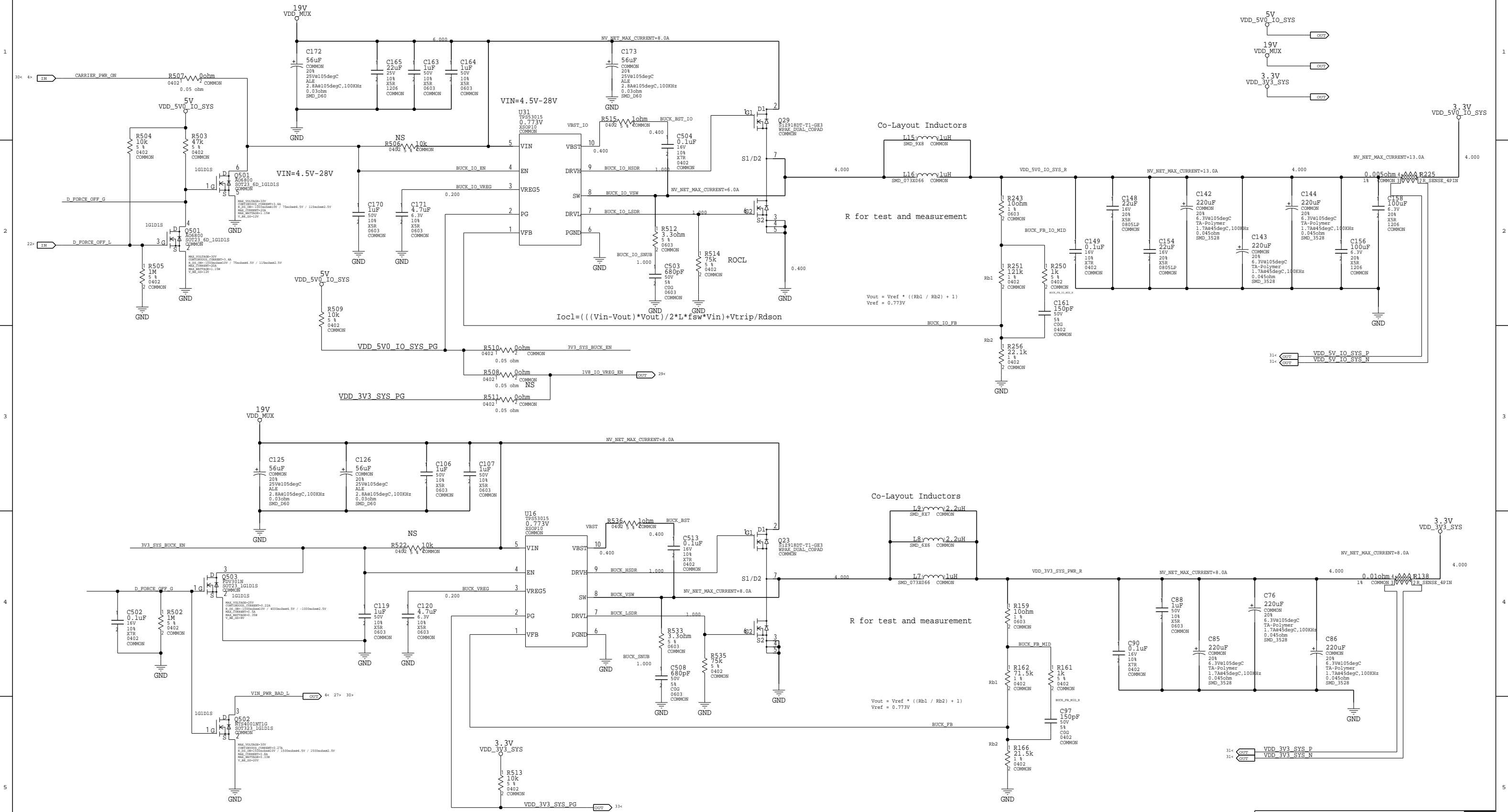
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5V & 3V3 SYS POWER SUPPLIES



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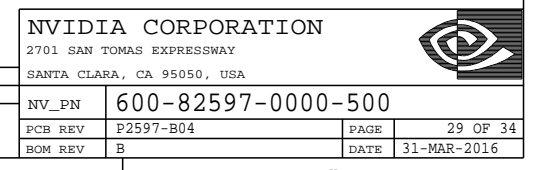


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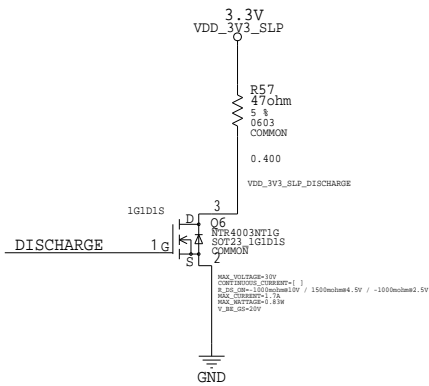
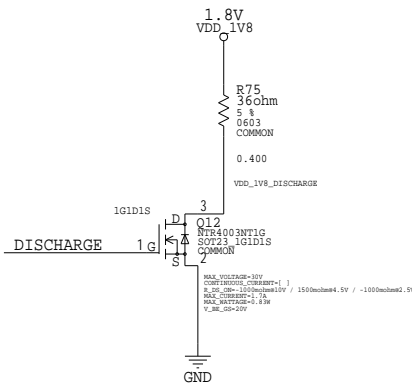
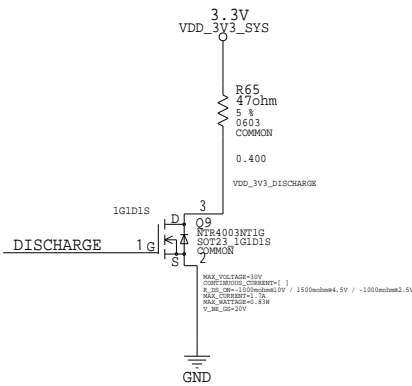
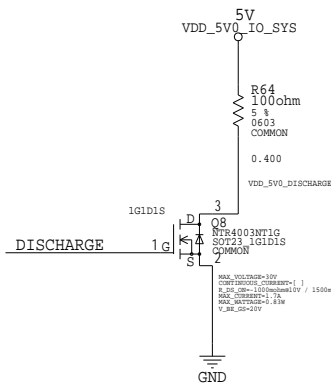
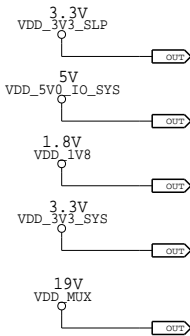
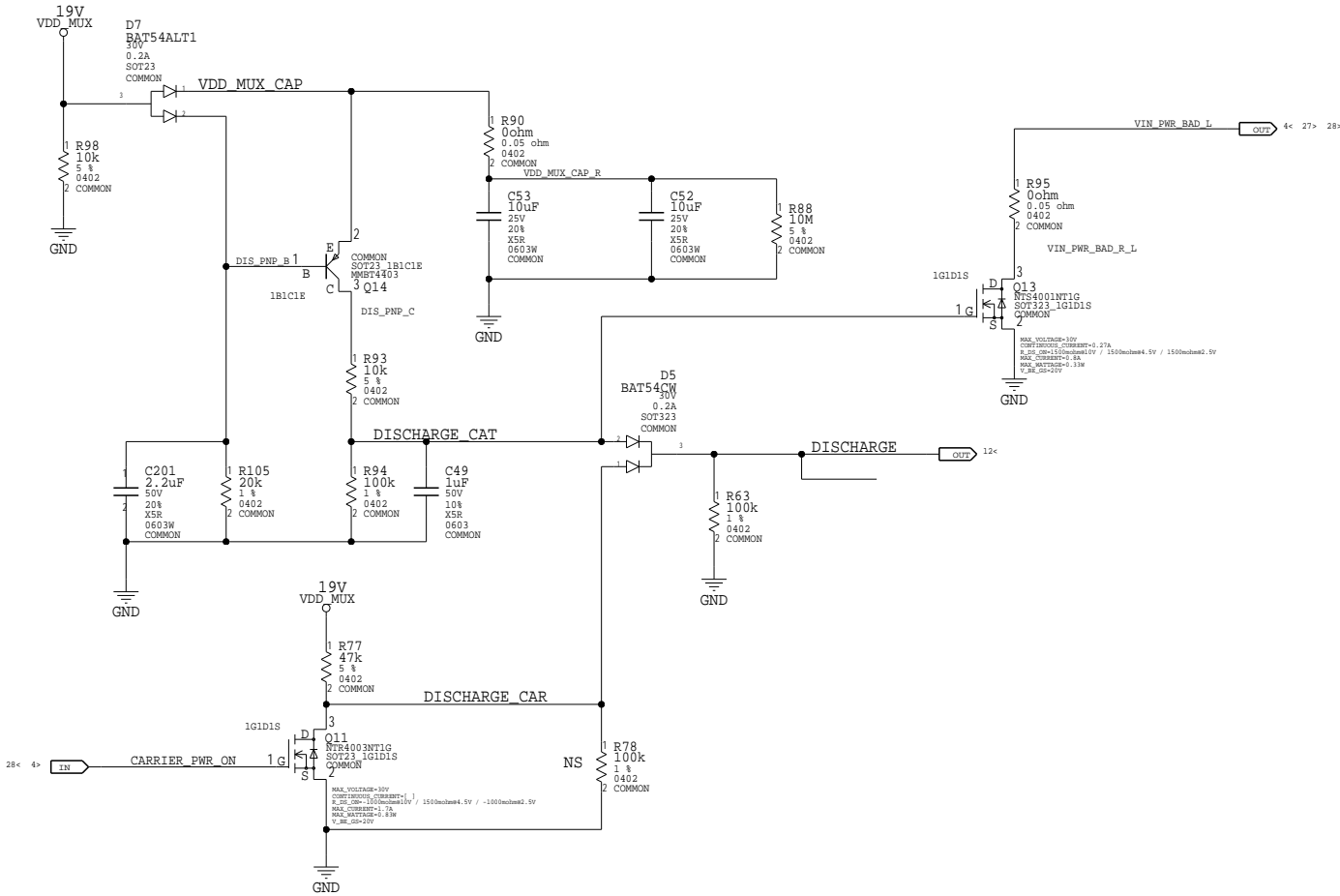
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	5V & 3V3 Vregs



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RAIL DISCHARGE



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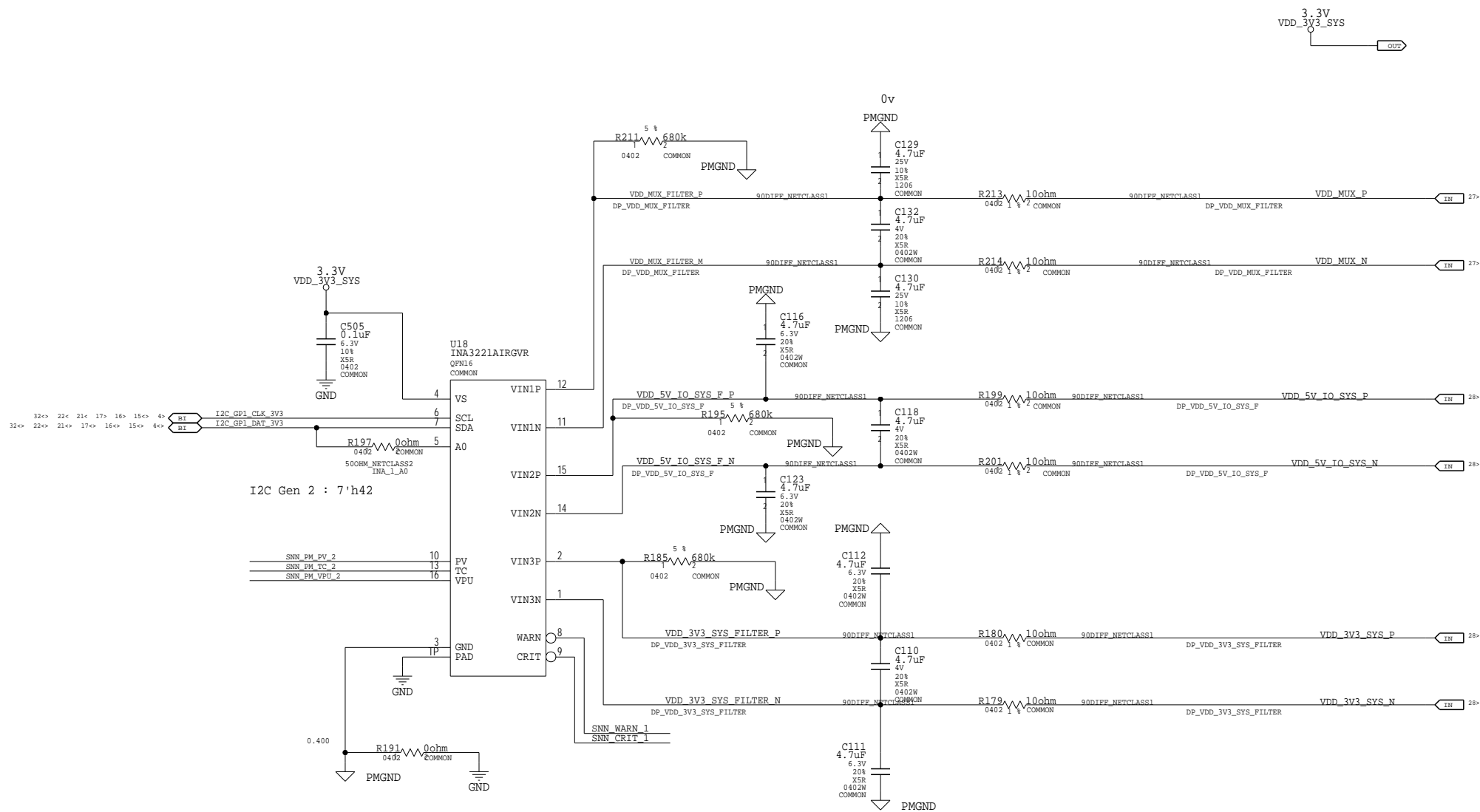


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POWER MONITORS I



DC JACK to IO board

5V SYSTEM

3V3 SYSTEM

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POWER MONITORS II

The schematic diagram illustrates the power monitoring circuitry for the POWER MONITORS II. It features several key sections:

- VDD_3V3 IO SLP FILTER P/N:** This section shows the filtering of the VDD_3V3 IO_SLP signal. It includes capacitors C94 and C95 (4.7uF, 6.3V), resistors R170 and R171 (10ohm), and PMGND3 connections.
- VDD_1V8 IO P/N:** This section shows the filtering of the VDD_1V8 IO signal. It includes capacitors C89 and C91 (4.7uF, 6.3V), resistors R153 and R160 (10ohm), and PMGND3 connections.
- VDD_M2 IO FILT P/N:** This section shows the filtering of the VDD_M2 IO signal. It includes capacitors C84 and C83 (4.7uF, 6.3V), resistors R141 and R139 (680k, 10ohm), and PMGND3 connections.
- I2C Gen 2 :** This section shows the I2C Gen 2 interface, including pins BI, SCL, SDA, A0, PV, TC, VPU, GND PAD, IP, WARN, and CRIT.
- U10 INA3221AIRGVR:** This is the main monitoring IC, connected to various pins including VS, SCL, SDA, A0, PV, TC, VPU, GND PAD, IP, WARN, and CRIT.

Labels on the right side of the diagram indicate the following signals:

- 3V3 RUN RAIL
- 1.8V SYSTEM
- M.2 3.3V

ASSEMBLY		PAGE DETAIL	
BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL		Power Monitor II	

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POWER MONITORS II

3.3V
VDD_3V3_SYS

3V3 RUN RAIL

1.8V SYSTEM

M.2 3.3V

I2C Gen 2 : 7'h43

SNN PM2 PV 1
SNN PM2 TC 1
SNN PM2 VPU 1

U10
INA3221A1RGVR
QFN16
COMMON

VIN1P
VIN1N
VIN2P
VIN2N
VIN3P
VIN3N
WARN
CRIT

VS
SCL
SDA
A0
PV
TC
VPU
GND PAD
IP

0.400
0.05 ohm
0402
COMMON
GND

PMGND3

DP_VDD_3V3_IO_SLP_FILTER P
DP_VDD_3V3_IO_SLP_FILTER N
VDD_3V3_IO_SLP_FILTER P
VDD_3V3_IO_SLP_FILTER N
VDD_1V8_IO_FILTER P
VDD_1V8_IO_FILTER N
VDD_M2_IO_FILT P
VDD_M2_IO_FILT N
DP_VDD_M2_IO_FILT
DP_VDD_M2_IO_FILT

R163
680k
0402
COMMON

R153
10ohm
0402
COMMON

R160
10ohm
0402
COMMON

R140
10ohm
0402
COMMON

R139
10ohm
0402
COMMON

R147
0.05 ohm
0402
COMMON

C516
0.1uF
6.3V
10%
X5R
0402
COMMON

C87
4.7uF
6.3V
20%
X5R
0402W
COMMON

C89
4.7uF
4V
20%
X5R
0402W
COMMON

C91
4.7uF
6.3V
20%
X5R
0402W
COMMON

C94
4.7uF
6.3V
20%
X5R
0402W
COMMON

C95
4.7uF
6.3V
20%
X5R
0402W
COMMON

PMGND3

90DIFF_NETCLASS1

VDD_3V3_IO_SLP_P
VDD_3V3_IO_SLP_N
VDD_1V8_IO_P
VDD_1V8_IO_N
VDD_M2_IN_P
VDD_M2_IN_N

IN
IN
IN
IN
IN
IN

29<
29<
29<
29<
10<
10<

ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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[illegible]

POWER MONITORS II

3.3V
VDD_3V3_SYS

3V3 RUN RAIL

1.8V SYSTEM

M.2 3.3V

I2C Gen 2 : 7'h43

SNN PM2 PV 1
SNN PM2 TC 1
SNN PM2 VPU 1

U10
INA3221A1RGVR
QFN16
COMMON

VIN1P
VIN1N
VIN2P
VIN2N
VIN3P
VIN3N
WARN
CRIT

VS
SCL
SDA
A0
PV
TC
VPU
GND PAD
IP

0.400
0.05 ohm
0402
COMMON
GND

PMGND3

DP_VDD_3V3_IO_SLP_FILTER P
DP_VDD_3V3_IO_SLP_FILTER N
VDD_3V3_IO_SLP_FILTER P
VDD_3V3_IO_SLP_FILTER N
VDD_1V8_IO_FILTER P
VDD_1V8_IO_FILTER N
VDD_M2_IO_FILT P
VDD_M2_IO_FILT N
DP_VDD_M2_IO_FILT
DP_VDD_M2_IO_FILT

R163
680k
0402
COMMON
R153
10ohm
0402
COMMON
R170
10ohm
0402
COMMON
R171
10ohm
0402
COMMON
R152
10ohm
0402
COMMON
R160
10ohm
0402
COMMON
R140
10ohm
0402
COMMON
R139
10ohm
0402
COMMON
R147
10ohm
0402
COMMON

C516
0.1uF
6.3V
10%
X5R
0402
COMMON
C87
4.7uF
6.3V
20%
X5R
0402W
COMMON
C89
4.7uF
4V
20%
X5R
0402W
COMMON
C91
4.7uF
6.3V
20%
X5R
0402W
COMMON
C94
4.7uF
6.3V
20%
X5R
0402W
COMMON
C95
4.7uF
6.3V
20%
X5R
0402W
COMMON
C78
4.7uF
4V
20%
X5R
0402W
COMMON
C83
4.7uF
6.3V
20%
X5R
0402W
COMMON
C84
4.7uF
6.3V
20%
X5R
0402W
COMMON

PMGND3

90DIFF_NETCLASS1

0v

OUT

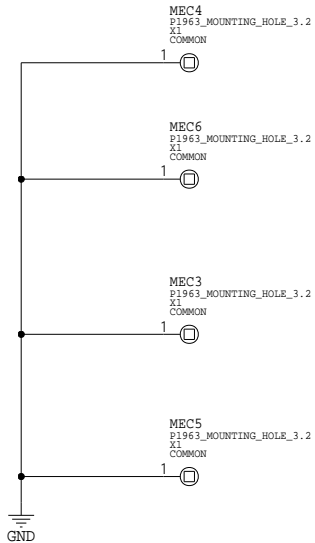
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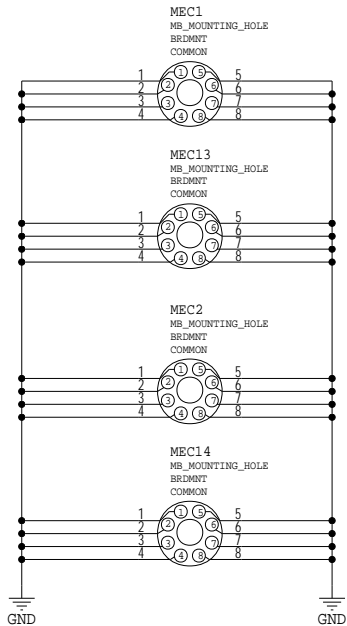
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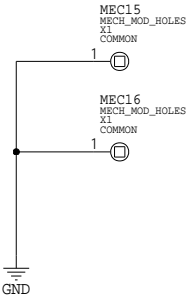
MODULE MOUNTING STANDOFFS



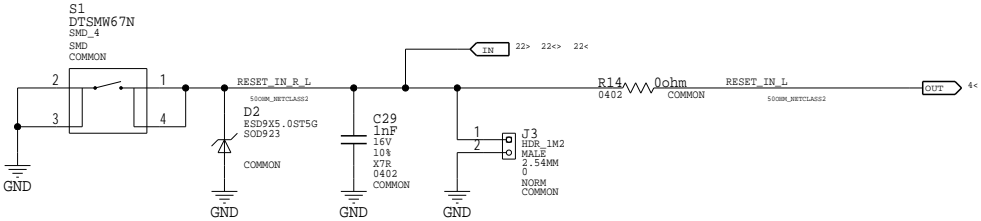
FOUR CORNER miniITX MOUNTING HOLES



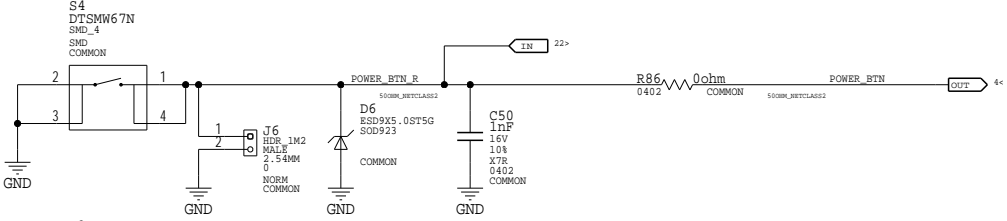
Antenna bracket mount



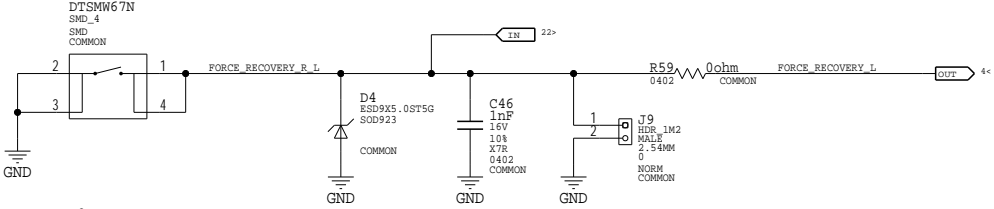
RESET



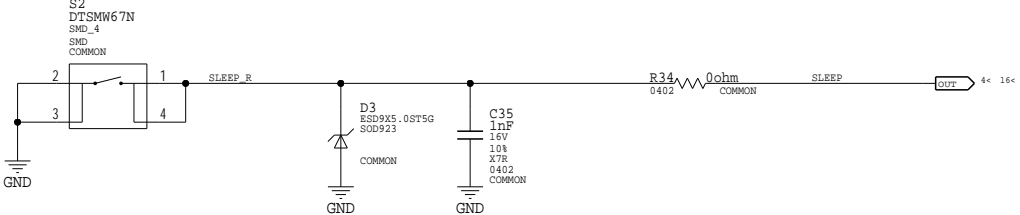
POWER



RECOVERY

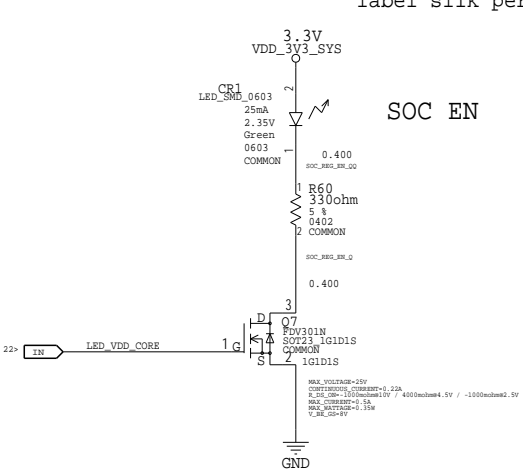


VOL DOWN

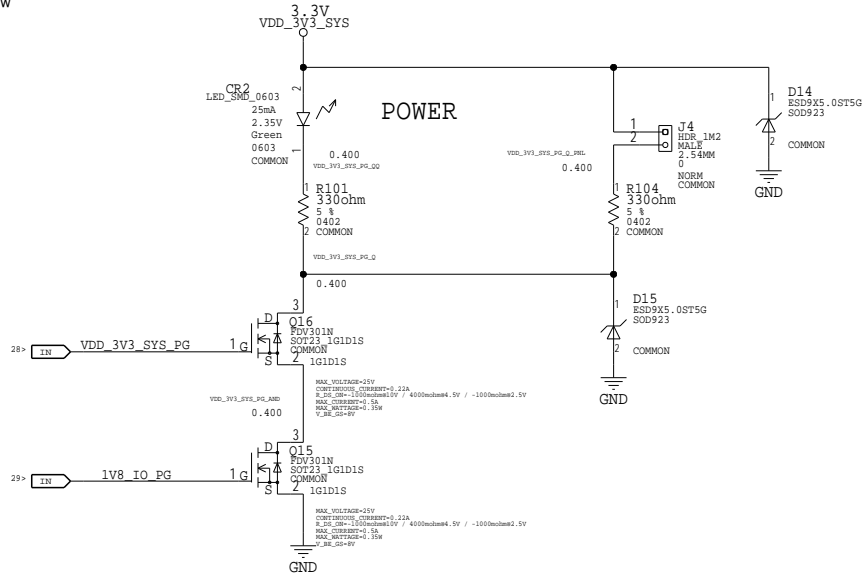


CAD NOTE:
Please place LEDs near the
power button in the front
label slik per text below

SOC EN



POWER



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Revision History

P2597-B03

- Page 4:
- Added a red LED to indicate power is active on the CVM
- Page 8:
- Replaced U21 due to EOL on previous part
- Page 9:
- Changed an unused pull up to a TVS device on PCIe RST
PCI_E_WAKE_L and PCIe_CLKREQ
- Page 10:
- Change R524 and R538 to 1.8k (tune for gyro bypass)
- Page 10:
- Changed M.2 I2C to 1.8v
- Page 12:
- Added discharge for VDD_5V0_IO_SLP and VDD_12V_SLP
Added a red LED to 12v at PCIe connector
Changed DEV_SLP buffer to OD
- Page 13:
- Changed R9 to 100pF cap C205 (EU emissions)
- Page 14:
- Changed R548 to 4.7k ohm and R544 to 100k
- Page 15:
- Changed DBG I2C MUX to I2C repeater with enable
Added pull ups on inputs to U6
- Page 16:
- Added 1206 0ohm resistors on J26
Added pull downs on J21 side of U22 and U7
Added reset connection to U22 and U7
Added ESD protection
- Page 22:
- Added pull-up on J10 pin 48 for direct INA support
Added 0ohm resistor on the fan PWM to allow always on
Added a pull down on UART4_TX
Added ESD protection to pins 4 and 6 of Q17
- Page 24:
- Changed U11 EEPROM to AT24C02D-MAHM-T
- Page 25:
- Added supervisor to hold Tegra in reset until 1.8v up
- Page 27:
- Added additional bulk site on VDD_MOD
- Page 28:
- Changed 5v and 3.3v VR FETs for better thermal perf
- Page 30:
- Added C201 and changed C49 to 1uF to filter DC loss
- Page 33:
- Added ESD option for power LED

P2597-B04

Corrected minor solderpaste issue

- Page 12:
- Stuffed R315
- Page 14:
- Changed R563 and R565 to 3.3ohm
- Page 25:
- Unstuffed page

BOM rev B

- Page 23:
- Changed C36 to 0.1uF
- Page 30:
- Changed C201 to 2.2uF and R105 to 20k

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