Nome	Sintaxe	Tradução Inst. Reais	Significado
Move	move \$rt,\$rs	add \$rt,\$rs,\$zero	R[rt]=R[rs]
Clear	clear \$rt	add \$rt,\$zero,\$zero	R[rt]=0
Not	not \$rt, \$rs	nor \$rt, \$rs, \$zero	R[rt]=~R[rs]
Load Address	la \$rd, LabelAddr	<pre>lui \$rd, LabelAddr[31:16]; ori \$rd,\$rd, LabelAddr[15:0]</pre>	<pre>\$rd = Label Address</pre>
Load Immediate	li \$rd, IMMED[31:0]	<pre>lui \$rd, IMMED[31:16]; ori \$rd,\$rd, IMMED[15:0]</pre>	<pre>\$rd = 32 bit Immediate value</pre>
Branch unconditionally	b Label	beq \$zero,\$zero,Label	PC=Label
Branch and link	bal Label	bgezal \$zero,Label	R[31]=PC+8; PC=Label
Branch if greater than	bgt \$rs,\$rt,Label	slt \$at,\$rt,\$rs; bne \$at, \$zero,Label	if(R[rs]>R[rt]) PC=Label
Branch if less than	blt \$rs,\$rt,Label	<pre>slt \$at,\$rs,\$rt; bne \$at,\$zero,Label</pre>	if(R[rs] <r[rt]) pc="Label</td"></r[rt])>
Branch if greater than or equal	bge \$rs,\$rt,Label	slt \$at,\$rs,\$rt; beq \$at,\$zero,Label	if(R[rs]>=R[rt]) PC=Label
Branch if less than or equal	ble \$rs,\$rt,Label	<pre>slt \$at,\$rt,\$rs; beq \$at,\$zero,Label</pre>	if(R[rs]<=R[rt]) PC=Label
Branch if greater than unsigned	bgtu \$rs,\$rt,Label		if(R[rs]>R[rt]) PC=Label
Branch if greater than zero	bgtz \$rs,Label		if(R[rs]>0) PC=Label
Branch if equal to zero	beqz \$rs,Label		if(R[rs]==0) PC=Label
Multiplies and returns only first 32 bits	mul \$d, \$s, \$t	mult \$s, \$t; mflo \$d	\$d = \$s * \$t
Divides and returns quotient	div \$d, \$s, \$t	div \$s, \$t; mflo \$d	\$d = \$s / \$t
Divides and returns remainder	rem \$d, \$s, \$t	div \$s, \$t; mfhi \$d	\$d = \$s % \$t