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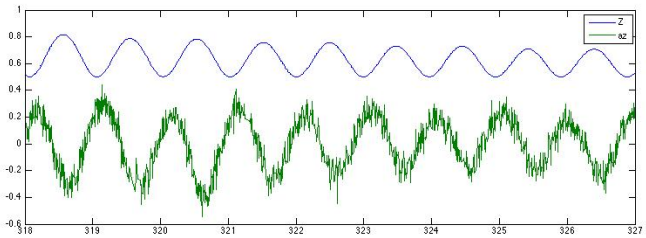
Semester Thesis

Sensor Fusion / State Estimation for a Kite Power Plant



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Sensor Fusion / State Estimation for a Kite Power Plant

Description

Working within the context of the SwissKitePower project,

- Develop and implement a data fusion algorithm that provides a real-time estimation of the kite's position, velocity and orientation using the output from multiple sensors.
- Perform laboratory and field tests to validate and quantify the performance boundaries of the estimator.
- Document the results in a report and presentation.

Tasks

Sensor Selection and preliminary testing:

Researchers at FHNW and ETH have already selected and procured a number of sensors and performed preliminary tests. These sensors include:

- Xsens – Commercial GPS + IMU with extended Kalman filter implemented in on-board DSP. http://www.xsens.com/en/general/mti-g

- ArduPilot – Open source GPS + IMU system with DCM (direction cosine matrix) calculation implemented in on-board microprocessor. http://diydrones.com/profiles/blogs/ardupilot-mega-home-page

- X-IMU – Early commercial IMU with integrated storage and Bluetooth, some sensor fusion implemented on-board. http://www.x-io.co.uk/node/9

In addition, the following sensors have been ordered and will be implemented and tested on the FHNW groundstation during the next set of bachelor thesis projects:

- Line angle sensors from TWK - Both the vertical and horizontal angles and angular rates of change of the kite line

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will be measured using the following sensors. When combined with the length of the line, an estimation of kite position and velocity are possible.
http://www.twk.de/data/pdf/11278fe0.pdf

- Differential GPS system – A DGPS from Novatel has been ordered which consists of two receivers, one which will go on the kite and another on the ground which measures and transmits the correction information.
http://www.novatel.com/assets/Documents/Papers/OEMStar.pdf

Working with the FHNW students, these systems should be tested and the results analyzed to determine the best suitable combination of sensors for the system. Additional sensors, such as the PixIMU from ETH and the new version of the ArduIMU can also be tested and potentially used in the system. First testing can be made using a centrifuge, which is available at FHNW to understand how the various GPSs and IMU's perform under high g-loads and dynamic conditions. Preliminary tests of this nature have been performed and their results documented in a report which is available.

State Estimator Development:

Based on the results of the first task, a first version of the estimation software should be developed and implemented on an appropriate platform. Most likely this can be done on a PC using Labview or Matlab to acquire and process the incoming data streams and to perform the calculations required. A definition should be made for what sensor values will be passed from the FHNW groundstation to the PC which will perform the calculations as well as what form of output will be given. It is possible that not all sensors are available and the algorithm has to be able to deal with different sensor setups. This should be defined during an initialization phase. Different state estimation algorithms should be implemented and tested. Care should be taken how to evaluate the performance of the different algorithms. As a start the conclusion of the Master Thesis of Héjj Andreás "Kalman-filter based position and attitude estimation algorithms for an Inertial Measurement Unit" can be used. From there on it has to be investigated how we can use the model information of the kite system to improve the state estimation. It can either be used for the state propagation of the INS algorithm directly or apply another Kalman filter in an outer loop to estimate the trajectory.

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Testing and Validation:

Working with FHNW students and staff, the estimator should be tested in the loop and its output used in some preliminary stabilizing and tracking controllers. The implementation of the controllers themselves will be the responsibility of the project supervisors but the estimator should provide a robust estimate of kite position, velocity and orientation so that the appropriate control actions can be calculated. The performance goals to be achieved are:

- Kite stabilized at zenith for > 1 min.
- Figures of eight flown at constant line length for > 1 min.

Procedures

Time schedule

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Abstract

Bla Bla Bla

Chapter 1

Introduction

1.1 Kite Power in General and the SwissKitePower Project

At a time when windmills were already quite commonly used for power generation, Loyd came up with the idea to use kites to convert wind energy to electricity. In 1980 he wrote a seminal paper exploring the possibility of generating electrical power using the pulling force of tethered airfoils, i.e., kites [1]. He describes his concept as follows:

> A kite's aerodynamic surface converts wind energy into motion of the kite. This motion may be converted into useful power by driving turbines on the kite or by pulling a load on the ground. [...] Not simply facing into the wind, such kites would fly a closed path downwind from the tether point. The kite's motion would be approximately transverse to the wind, in the same sense that a wind turbine's blade moves transverse to the wind. The crosswind airspeed of a kite with this trajectory is increased above the wind speed by the lift-to-drag ratio L/D. The resultant aerodynamic lift is sufficient to support a kite and to generate power. [1]

Today, several research groups around the world are investigating this subject and working on prototypes. For example the University of Torino have already tested a prototype [2] and Massimo Ippolito has founded a company named KiteGen that is also located in Torino. At the University of Delft the group of Prof. Dr. Wubbo Oeckels is developing kites to produce energy with "Laddermills" [3] and at the K. U. Leuven the group of Prof. Moritz Diehl is working on the Highwind project [4]. Furthermore the SkySails company is already using wind power to pull large cargo ships [5] and Ampyx Power, a spin-off from T.U.Delft is working on their PowerPlane device.

In Switzerland the research efforts are coordinated in the SwissKitePower Project [6]. SwissKitePower is a collaborative research and development project between FHNW (University of Applied Sciences Northwestern Switzerland), ETHZ (Swiss

Federal Institute of Technology Zurich), EMPA (Swiss Federal Laboratories for Materials Testing and Research) and Alstom Switzerland AG. The goals of the project are to develop 'novel wind energy extraction technology' using tethered airfoils, or kites, and to promote this innovative new technology to the world.

1.2 Related Work

There are many publications on the topic of IMU/GPS data fusion for navigation purposes. As a starting point of our work we used the Master Thesis of András Héjj "Kalman-filter based position and attitude estimation algorithms for an Inertial Measurement Unit" [7]. In an other Master project at the University of Southern Denmark Ushanthan Jeyabalan implemented a Kalman Filter using a spherical pendulum model [8]. Several other publications investigated the use of a Kalman Filter for IMU/GPS data fusion in different applications. Sukkarieh applied it to land vehicles [9], Kim used it for unmanned areal vehicles in highly dynamic flight situations [10] and Crassidis used a Sigma Point Kalman Filter and compared it to an EKF. This list of course is not exhaustive. A much broader overview over the various approaches to multisensor data fusion in target tracking can be found in the survey article of Smith and Singh [11].

1.3 Motivation and Methods

In order to successfully implement a control algorithm on a kite, it is essential that a precise and fast position estimation is available. Due to the slow update rate of the GPS units and their limited reliability, a Kalman Filter will be used to integrate IMU measurements, which consist of acceleration, rate of turn and magnetic field, with the GPS position and velocity estimations. A standard Kalman Filter, one that could also be used in an airplane for example, assumes no knowledge aboout forces acting on the body. Such an estimator will already enhance the position estimation from the raw GPS input since it incorporates more measurements. However, a kite can only move on a restricted surface due to it being thethered to the groundstation. An extended Kalman Filter could take advantage of that knowledge and further improve the estimator's performance. Further integrating an aerodynamical model of the kite could give more information about the forces acting on it and would reduce the estimator's dependency on precise sensor output.

In order to be able to compare the performance of the different estimators, it is neccessary to know the exact location and orientation of the kite at all times. In practice it is nearly impossible to obtain such a ground truth for a kite flying around in the air. Therefore we decided to investigate the benefits of an accurate physical model on the performance of a Kalman Filter using box suspended by a string. (See figure ...) This setup can be modeled as a spherical pendulum which has the advantage that all the forces acting on it are known. In addition, we are able to test the algorithms indoors using a Vicon System (add reference!!) that gives us

a very accurate ground truth of the box's position and orientation. Since there is obviously no GPS reception indoors, the GPS output needs to be simulated using the Vicon's position output, reducing its frequency and adding an appropriate level of noise.

Chapter 2

IMUs

For estimating the kite's state measurements from different sensors are needed. In so called inertial measurements units (IMU) several sensors are embedded. The most important difference between the the IMUs are in what sensors are embedded, with which rate do they provide the data, what is their range and sensitivity and how much signal processing is already done by the IMU.

The Swiss Kite Power Project has the following options of IMUs to choose:

MTi-G The MTi-G development kit is a commercial product from the Dutch company Xsens. The unit has an accelerometer, gyroscope, magnetometer, pressure sensor and GPS with antenna included. It exist two output data formats. It can be chosen wether the output is raw data or calibrated data. The calibrated data from the sensors without GPS gives the data in $[m/s^2]$ and takes a offset calibration test into account. In addition to that is the GPS data processed with an Extended Kalman Filter in the calibrated output mode.

PX4 The PX4 is a open-source/open-hardware IMU used and developed by the PIXHAWK Project of the Computer Vision and Geometry Lab of ETH Zurich. The unit contains a temperature and pressure sensor, an accelerometer, a gyroscope and a magnetometer. The IMU additionally provides a counter for each sensor output. The output of the sensors is raw data. In the estimation algorithm (see chapter 3) only the embedded accelerometer a BMA180 from Bosch (see the data sheet in appendix A.1), the gyroscope a L3GD20 from STMicroelectronics (see the data sheet in appendix A.2) and the magnetometer a HMC5883L from Honeywell(see the data sheet in appendix A.3) is used.

x-IMU The x-IMU is a product of the company x-io Technologies. It has as well a temperature sensor, a accelerometer, a gyroscope and a magnetometer. The setting of the x-IMU was done by the FHNW. It provides only raw data. The data sheets of the sensors can be found in the appendix B.

2.1 Centrifuge Test

There are several performance requirements on an IMU installed on a kite. One of them is the dependency on g-loads because on a kite several g loads can appear. Therefore a centrifuge test was carried out in corporation with the Fachhochschule Nordwestschweiz (FHNW)

2.1.1 Set-up

The setting of the centrifuge is described in (âĂę..Figure.....). It is provided by the FHNW. A arm is rotated by a motor. The IMUs are set into a box at the end of the arm. The sensors are put next to each other to have the almost the same measurements in all sensors. The Box can be seen on the picture in (âĂę.Figure....). Obviously is the motion of the box describing a circle with a radius (he distance between the center and the center of the box) of $0.75m$. The motor is able to rotate the arm with a velocity of about $10m/s$. With formula $a = \omega * r^2$ we get maximum acceleration of about $8g$. There is no software for the data collection of the measured velocity implemented. Therefore we have no ground truth to compare the sensor data with. The motor is driven in order to have 5 steps between $1.62g$ and $7.8g$ $(ca.1.6g; 2.4g3.7g; 5.4g; 6.9g; 7.8g)$ of centripetal acceleration.

The PX4 and Xsens are connected together. Both, the PX4 and the Xsens measurements are written on the SD card which is attached on the PX4 Unit. The timestamp is taken from the GPS clock for the Xsens as well as for the PX4 sensor data at the time when they are written on the SD card. This results in easy and accurate synchronization between the two IMUs. To get the time synchronized with the third IMU, the x-IMU is synchronized to the computer's time. Additionally the 3 sensors are hit for having a estimation of how accurate the synchronization is.

2.1.2 Result

The raw data from the x-IMU is scaled by Raphael Mueller bringing it in the common units m/s^2 for the accelerometer, deg/s for the gyroscope and gauss for the magnetometer.

The PX4 was set by the group of the PixHawk Project. How the output of the sensors have to be scaled to bring them in the required units is shown in table 2.1. The scale factor describes by how much the output has to be multiplied to get the data converted in the units described in 4th row. The MTi-G has also raw output data but no clear explanation in the data sheet (âĂę..) on how to get to the required units. Therefore, were the MTi-G data scaled to bring it more or less to the same order as the other two IMUs are. In (...figure...) we can see the plot of the GPS data. Until 4.83e4 s is the centrifuge not in motion. The mean value of this period is the taken as the ground truth to calculate the the average error of the GPS signal. The mean value of the north component is $47.48deg$ for the east component $8.2138deg$ and for the down component $415.74m$. The coordinates of Winidsch, where the

Sensor	Sensitivity	Scale Factor	Unit	Comment
Accelerometer BMA180	$2048LSB/g$	$output * 9.81/2048$	m/s^2	Sensitivity range: $+/-4g$
Gyroscope L3GD20	$17.5mdps/digit$	$output * 17.5/1000$	deg/s	
Magnetometer HMC5883L	$1370LSB/g$	$output/1370$	gauss	

Table 2.1: This table shows how the raw data output of the PX4 has to be sclaed to get the right units.

test takes place is $47.4806deg$, $8.2222deg$ and $357m$. By taking the average absolute difference between the GPS data and the mean value calculated before, an error of the GPS can be estimated: $1.08 * 10^{-5}deg$, $1.37 * 10^{-5}deg$ and $2.49m$ for north, east, down respectively. After $4.83 * 10^4s$ the noise is increasing. At this time the centrifuge starts rotating. The calculated errors in this period are: $1.68 * 10^{-5}deg$, $2.27 * 10^{-5}deg$ and $2.89m$ for north east, down respectively. After $4.87 * 10^4s$ the noise look very high. This is when we have a centripetal acceleration of more than $6.7g$. The estimated noise is: $1.04 * 10^{-4}deg$, $1.02 * 10^{-4}deg$ and $13.01m$. Since in non of this periods a cosine of sine behavior of the north and east component can be seen all three components should be stable in the ideal case. The error values a summarized in table 2.2. Due to the fact that the velocity is the derivative of

Period	Average error (north/east/down)
$4.80 * 10^4s - 4.83 * 10^4s$	$1.08 * 10^{-5}deg/1.37 * 10^{-5}deg/2.49m$
$4.83 * 10^4s4.87 * 10^4s$	$1.68 * 10^{-5}deg/2.27 * 10^{-5}deg/2.89m$
$4.87 * 10^4s4.91 * 10^4s$	$1.04 * 10^{-4}deg/1.02 * 10^{-4}deg/13.01m$

Table 2.2: The average error of the postion in different time segments

the position of the GPS the amplitude of the error behaves similar. The periods with the correspondent average error is shown in table 2.3. In figure 2.3 and figure

Period	Average error(x/y/z)
$4.80e4s - 4.83e4s$	$5.54m/6.05m/6.57m$
$4.83e4s4.87e4s$	$101.86m/138.96m/27.36m$
$4.87e4s4.91e4s$	$157.20m/123.56m/58.78m$

Table 2.3: The average error of the velocity in different time segments

2.4 the accelerometer and gyroscope measurements are shown. As expected do we have highest acceleration in x direction and the fastest rotational speed in z direction. In the accelerometer x axis and the gyroscope z axis measurement can be seen the 5 steps of different rotational speed. The very first step is a test rotation followed by the hit on the sensors which react with a peak. Since the sensitivity of

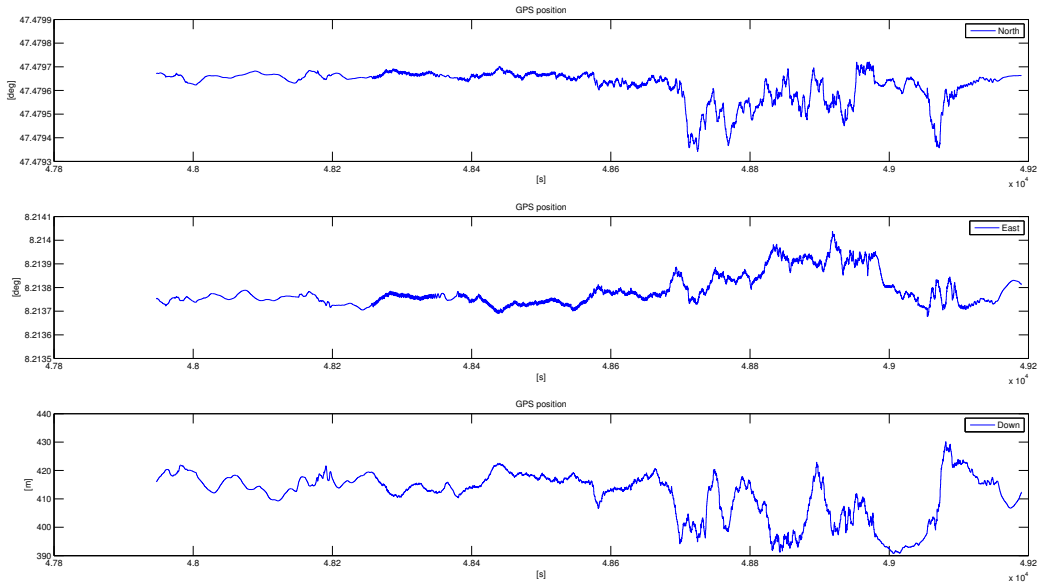

Figure 2.1: GPS Position

the PX4 accelerometer is set to $+/-4g$, the output of accelerometer in x direction is limited to $39.24m/s^2$. The acceleration in y direction is shows small steps due to the placement of the sensors slightly besides the center of the box.The gyroscope from the XTi-G shows a limitation in measuring more than $403deg/s$. The x-axis and y-axis should be zero for the gyroscope since the rotation is in two dimensional. Obviously is the noise again increasing with a higher rotation speed.This can be clearly seen in the acceleration in z direction which should be constant at $-9.81m/s$, the gravitation. It looks like the noise level of the PX4 is the highest before the x-IMU and the MTI-G which has the lowest. This can be traced back on the high sensitivity set up of the PX4 accelerometer.

In figure **??** the magnetometer output is plotted. There is a miss alignment between the x-IMU,MTi-G and the PX4 which cannot be explained by the authors. The range of the maximum value and the minimum value of the PX4,MTi-G and the x-IMU is in x and y direction $0.4gauss$. This is the expected range in the region of Zurich. In this sense, if the the output is added with an offset in order to get the range to $+/-0.2gauss$, the measurements should be correct. The PX4 has a mean value of 0.3893 gauss while the ground truth is $0.4268gauss$. The noise of the magnetometer is in the x-IMU higher than in the other two IMUs.

In figure 2.6 a closer look on the x axis of the magnetometer and accelerometer and on the y axis of the gyroscope is presented. The form of the curve has sine behavior, what we would expect again.

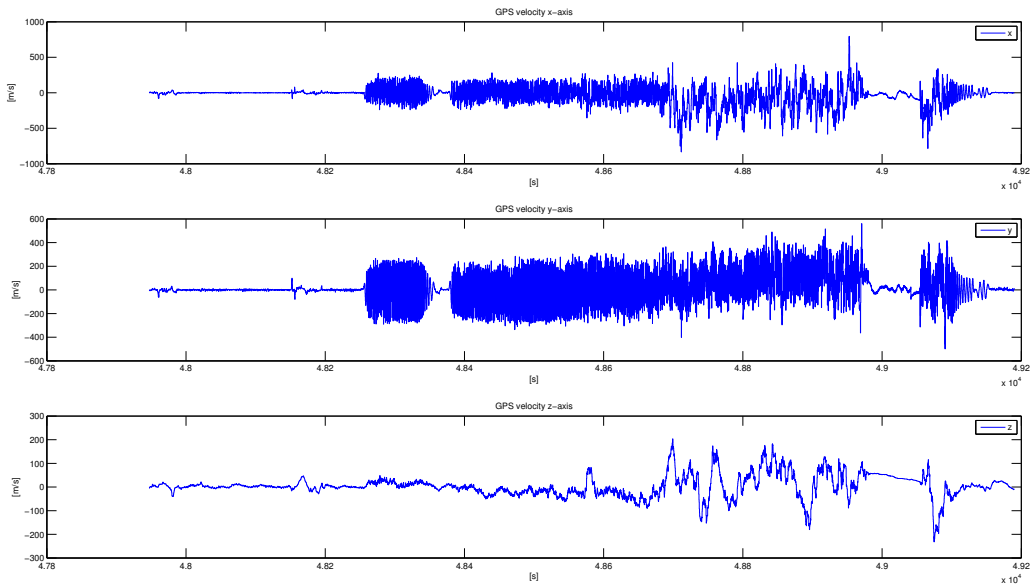

Figure 2.2: GPS velocity

2.1.3 Conclusion

All IMUs work in the same range of noise level. With an increasing rotational velocity and therefore a higher centripetal acceleration, the average error is increasing in all sensors, except in the magnetometer. There could not be found a noise acceleration dependency. In a next experiment also the recording of rotational velocity should be carried out in order to generate a ground truth to compare the it with the IMU datas. It can then be made some more observations to compare the quality of the sensors with each other. Finally the sensitivity of the accelerometer of the PX4 unit should be set in a way to be able to observe the whole range or the applied and tested centripetal acceleration.

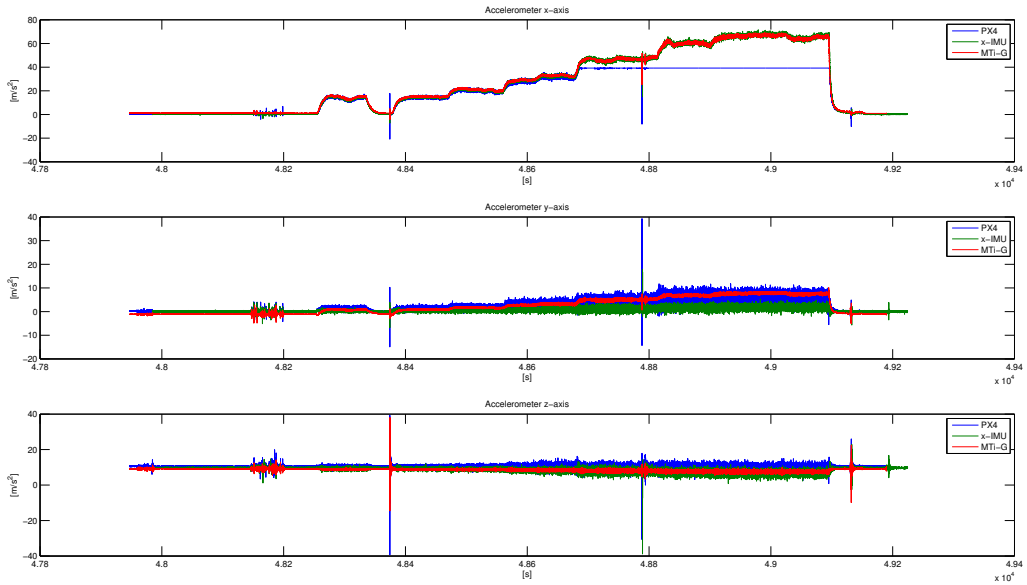

Figure 2.3: Accelerometer

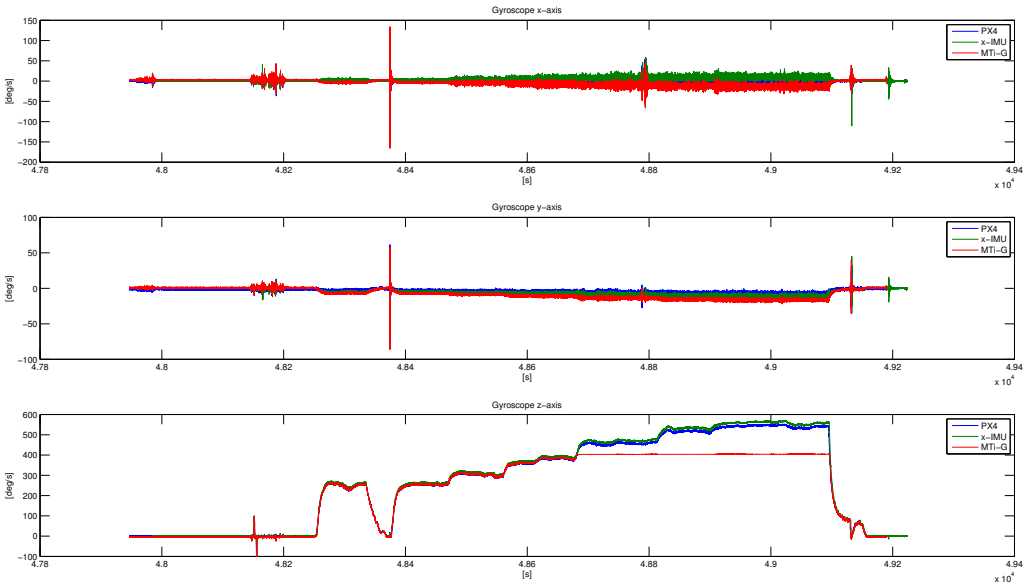

Figure 2.4: Gyrometer

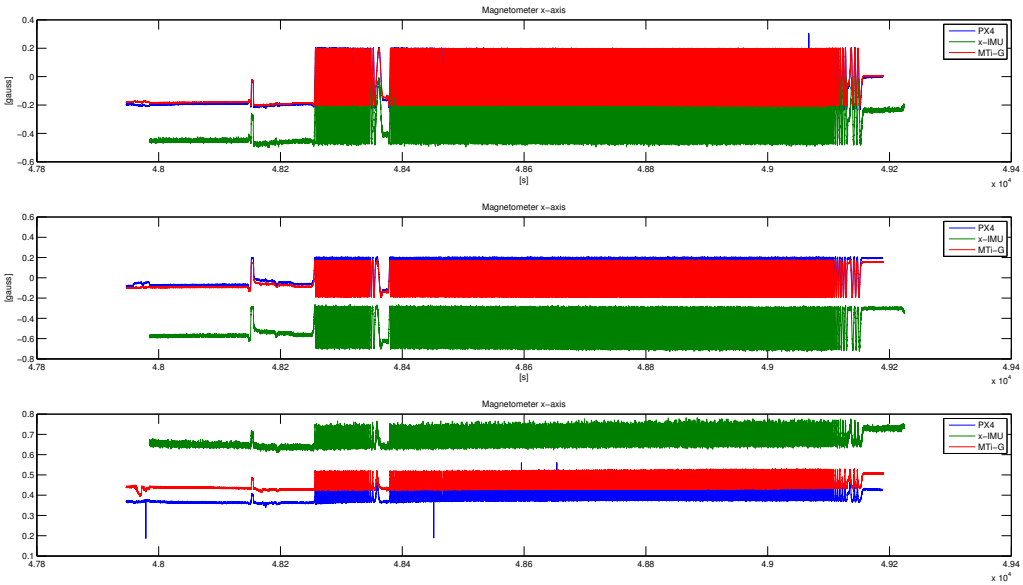

Figure 2.5: Magnetometer

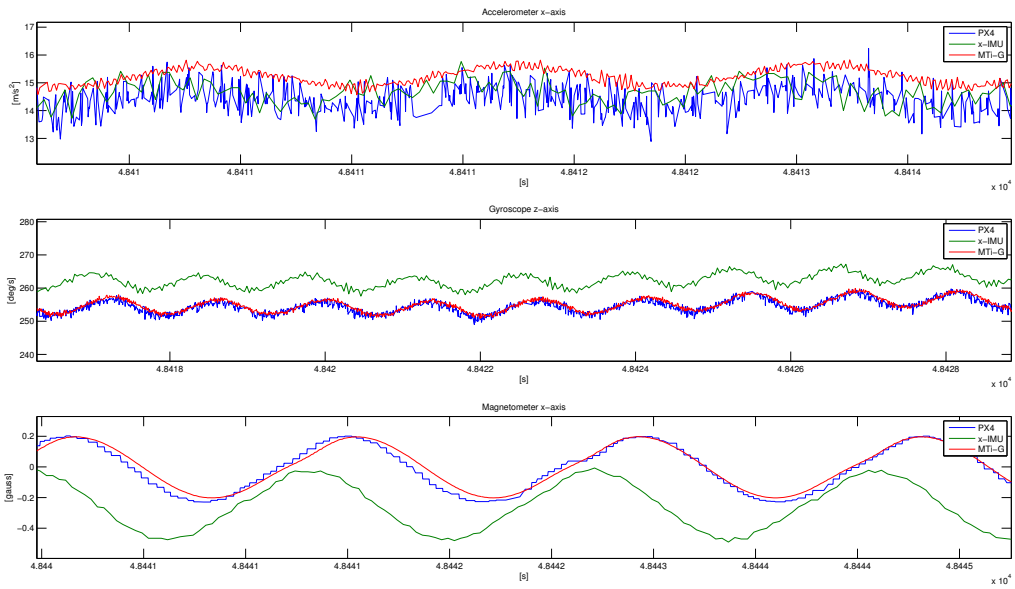

Figure 2.6: A closer look in time on the three IMU sensors.

Chapter 3

State Estimation

In this chapter is first an introduction in the Kalman Filter and the modified version called Extendend Kalman Filter given. In a second step will the state estimation algorithm, developed during this thesis explained. This gives an overview over the whole code and describes how the parameters were set and how a sensor data outage is handled. Section 3.3 and 3.4 will focus on the two essential parts of the algorithm, how the states are estimated and how the measurements are estimated.

3.1 Extended Kalman Filter

Discrete Kalman Filter

We will first give a short introduction to the Kalman Filter in general and its mathematical justification.

> The Kalman filter is an extremely effective versatile procedure for combining noisy sensor outputs to estimate the state of a system with uncertain dynamics.

[âĂęangu...] It was published in 1960 by R.E.Kalman. The Filter gained a strong impact in the area of autonomous or assisted navigation [..pap...]. Systems in which the filter is estimating the state $x \in R^n$ can be described by the following linear stochastic difference equation.

$$x_{k+1} = A_k * x_k + B_k * u_k + w \tag{3.1}$$

The next equation shows the relation between the state and the measurement $z \in R^n$.

$$z_k = H_k * x_k + D_k * u_k + v \tag{3.2}$$

Where the random variables w and v stand for the process and the measurement noise, which are assumed to be independent, white and normal probability distributions.

> The $n \times n$ matrix A in equation 3.1 relates the state at time step k to the state at step $k+1$, in the absene of either a dirving function or process noise. The $n \times l$ matrix B relates the control input $u \in R^l$ to the state x. The $m \times m$ matrix H in the measurement equation 3.2 relates to the state to the measurement z_k.

[.pap.] In most navigation applications, the noisy sensors are a GPS receiver and an inertial navigation system or other sensors like for example speed sensors. The states of a system are described by the position, velocity, attitude and attitude rate [.angu..].

Mathematical Background

In figure 3.1 the structure of the algorithm is sketched for a better understanding of the filter's mathematical background. In a first step the state at $k+1$ is estimated

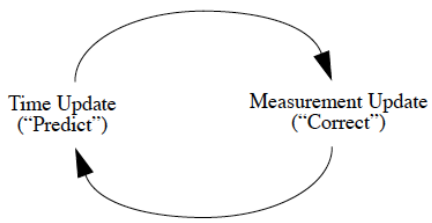

Figure 3.1: A simple structure of the algorithm

based on 3.1. This estimation is called a priori state estimation and written as $\hat{x}_k^-$. In a second step the a priori state estimation is corrected by the knowledge of measurements z_k. This corrected estimation is called the a posteriori estimation and written as $\hat{x}_k$.

Now two error can be defined with it's a error covariances. First the error of the a priori estimation

$$e^- = x_k - \hat{x}_k^- \tag{3.3}$$

and second the error of the a posteriori estimation

$$e = x_k - \hat{x}_k \tag{3.4}$$

with the a priori estimate error covariance

$$P_k^- = E[e^- e^{-T}] \tag{3.5}$$

and the a posteriori error covariance.

$$P_k = E[ee^T] \tag{3.6}$$

The Kalman Filter is calculating the a posteriori estimation, the one we are finally looking for. This calculation is a linear combination between the a priori estimated state and the difference of the the estimated measurement $x_k * H$ and the actual measurement z_k weighted with the Kalman gain K. This difference $z_k - H_k \hat{x}_k^-$ is called residual and tells us how accurate the estimation of the measurements is. This is summarized in equation 3.7.

$$\hat{x}_k^- * K * (z_k - H_k \hat{x}_k^-) \tag{3.7}$$

The Kalman gain K is the heart of the Kalman Filter. K, a $n \times n$ Matrix is chosen in a way to minimize the a posteriori error covariance shown in equation **??**. With some calculations the following

$$K = \frac{P_k^- * H_k^T}{(H_k * P_k^- * H_k^T + R_k)} \tag{3.8}$$

can be derived for the Kalman gain K.[..pap..]] This concept uses the information of a normal gaussian distribution of the noise mentioned in (..equ2..). P_k is minimized using the Maximum Likelihood Estimation and is called the Gaussian Maximum-Likelihood Estimator [âĂę]. A more detailed derivation of the mathematics is shown in [..maybeck..] and [..angu..].

Algorithm

With equations described in the section above, the estimation and correction step can be summarized as shown in figure 3.2. For a fine tuning of the filter often the

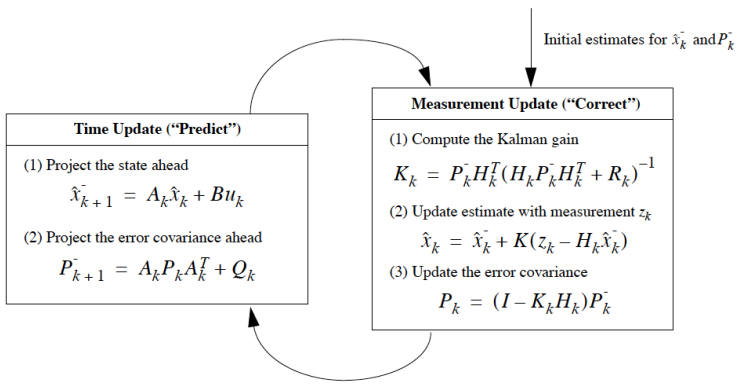

Figure 3.2: The prediction and the correction step with their corresponding equations.

measurement error covariance matrix R_k and process noise Q_k can be used. R_k contains the information how accurate the sensors and therefore the measurements are expected to be. This can be estimated in a first round with some static sensor

test or can be found in the data sheets of the sensors. The matrix Q_k describes how correct the propagation model described by the matrix A_k is believed to be. In this sense as higher the values and therefore the noise of R_k and Q_k the less influence do the measurements or the propagation model respectively have on the estimated state. Having a diagonal matrix with constant values over time, does not represent the reality, but brings it to a form which is fast stable and easier tunable[..pap..].

Extended Kalman Filter (EKF)

In reality the process to estimate the new state and the measurement relationship to the process is non-linear.

$$x_{k+1} = f(x_k, u_k, w) z_k = h(x_k, v_k) \tag{3.9}$$

One of the solution to overcome this problem is the Extended Kalman Filter shortly EKF. The EKF is linearizing the this functions with a first order Taylor-Series around the current state. This can be summerized with the following equation:

$$x_{k+1} \approx \hat{x}_{k+1} + A(x_k - \hat{x}_k) + w \qquad z_k \approx \hat{z}_k + H(x_k - \hat{x}_k) + v \tag{3.10}$$

Where A and H are the Jacobian matrix of the function f and h.

$$A_{i,j} = \frac{\partial f_i}{\partial x_j}(\hat{x}_k, u_k, 9) \qquad H_{i,j} = \frac{\partial h_i}{\partial x_j}(\hat{x}_k, u_k, 9) \tag{3.11}$$

This brings us to the summarized equations of the EKF in figure 3.3.

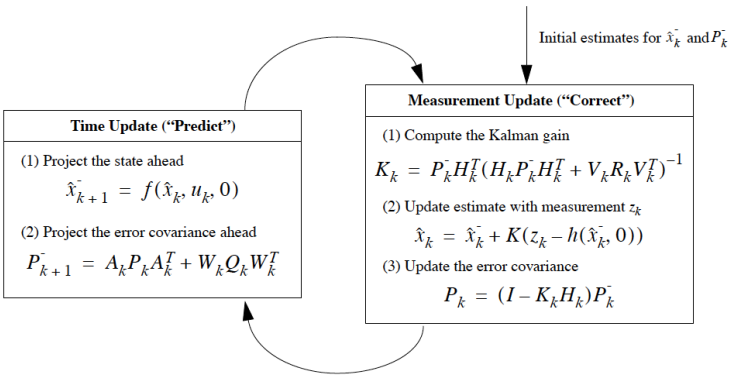

Figure 3.3: The prediction and correction step of the EKF with their corresponding equations.

3.2 Algorithm for State Estimation

In this chapter we will present the structure of the state estimation algorithm as we implemented it in MATLAB. As mentioned before, the goal is to get an estimation of the system's state as precise as possible using an Extended Kalman Filter. The Algorithm can be split in several main tasks. First the physical relations between the state x_k and the state x_{k+1} has to be defined and summarized in a propagation model. This is needed to calculate the a priori state estimation as described in chapter 3.1. Since this step is crucial for the accuracy of the algorithm, it is further explained in chapter 3.3. A second key role plays the measurement estimation which corrects the a priori state estimation and calculates the a posteriori state estimation. A more detailed explanation of this correction can be found in chapter 3.4. A third question to be elaborated is how the algorithm has to behave if no sensor data is available or if not all sensors provide their outputs with the same frequency. In the last paragraph we will explain how the error covariances were chosen.

Orientation

The filter has to handle two different coordinates frames. One is the inertial frame and the other the body frame. The inertial frame is the global frame. The position and the velocity both provided by the GPS are in the inertial frame. The origin of the inertial frame lies at the suspension point of the pendulum/kite. The body frame is a coordinate system on the kite. Its z-axis always points in the direction of the line and its origin lies at the center of gravity of the kite. The sensor measurements from the IMU are all in the body frame. Figure 3.4 contains an illustration of these two coordinate systems.

The euler angles describe how the inertial frame has to be rotated to bring into the body frame. With other words, the euler angles tell us the orientation of the body frame. With the direct cosine matrix (DCM) we can transform a vector from the inertial frame into the body frame and vise versa. For example can the accelerometer data which is given in body frame coordinates be transformed into the inertial frame, where the propagation of the states is calculated.[..angus..]

Degrees of Freedom

As stated in the introduction, we implemented two different versions of the state estimation algorithm. A standard implementation assuming a free mass and one version that exploits the constraints given by the knowledge that the mass is oscillatingly suspended at a fixed point. These two versions are quite similar and share a lot of code, but one crucial point where they differ from each other is the number of degrees of freedom (DoF). The free mass model uses 12 DoF, namely position, velocity, attitude and attitude rate. Thus the state vector consists of 12 variables. The pendulum model uses only 6 true degrees of freedom: Three angles representing the position and attitude as well as their respective rates representing velocity and

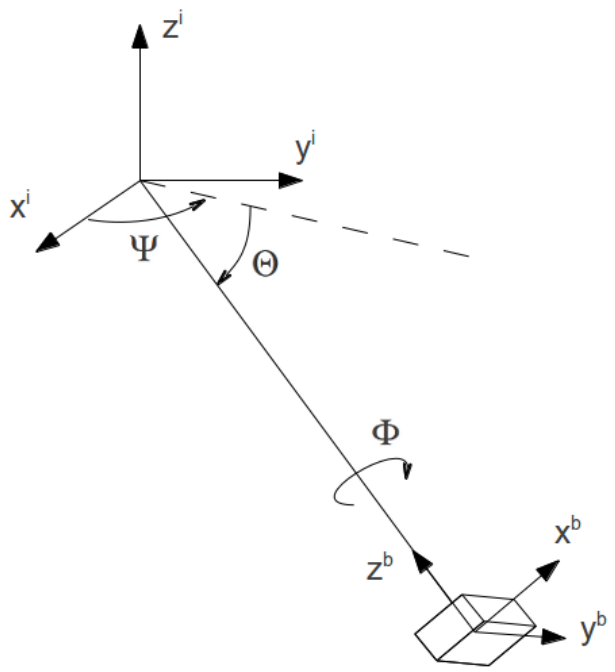

Figure 3.4: The definition of the inertial and body frame as well as the convention for the angles in the pendulum model.

attitude rate. The definition of these angles can be seen in figure 3.4.

States and Measurements

The state vector in the free mass model with the dimension of 12 looks as follows:

$$x = \begin{pmatrix} x \\ y \\ z \\ \dot{x} \\ \dot{y} \\ \dot{z} \\ \phi \\ \theta \\ \psi \\ \dot{\phi} \\ \dot{\theta} \\ \dot{\psi} \end{pmatrix} \tag{3.12}$$

The first six variables are position and velocity in the inertial frame. The angles and angular rates are Euler angles with the convention ZY'X". This means that in order to get from the inertial frame to the body frame the following three rotations have to be performed: a rotation with angle ψ around the z-axis in the inertial frame, a rotation with angle θ around the new y-axis and a last rotation with angle ϕ around the new x-axis.

The state vector in the pendulum model has eight elements. Even tough only 6 DoF are assumed, two additional variables, the radius and the change in radius, are included in the state to ensure the possibility of loosening the constraint of a fixed line length and implementing a spring model as suggested later on in the outlook section. Thus the state vector is defined as follows:

$$x = \begin{pmatrix} \Phi \\ \Theta \\ \Psi \\ r \\ \dot{\Phi} \\ \dot{\Theta} \\ \dot{\Psi} \\ \dot{r} \end{pmatrix} \tag{3.13}$$

For the definition of the angles Φ, Θ and Ψ see figure 3.4.

The measurement vector is the same for the free mass model as well as for the pendulum model. It consits of the position (pos) and the velocity (vel) of the GPS, the acceleration (acc) from the accelerometer and the rate of turn (gyro) from the gyroscope and the orientation (mag) from the magnetometer. Each of them in all

three dimensions give us the measurement vector z with a dimension of 15.

$$z = \begin{bmatrix} pos\ x \\ pos\ y \\ pos\ z \\ vel\ x \\ vel\ y \\ vel\ z \\ acc\ x \\ acc\ y \\ acc\ z \\ gyro\ x \\ gyro\ y \\ gyro\ z \\ mag\ x \\ mag\ y \\ mag\ z \end{bmatrix} \tag{3.14}$$

Structure of the Algorithm

In 3.5 the schematic of the algorithm is shown. Each of the blocks will now successive explained.

Block 1, totalTime: The filter estimates with constant rate the state of the system. This rate is independent on any output rate of the sensors. In the first block the time at which the state is estimated is set. It is the old time totalTime added with the constant time step t.

Block 2, Propagation: During the second block the a priori state of the system is estimated with the help of the physical model. How and why the physical model is defined is explained in chapter 3.3. After this step the vector x_{est} is up to date.

Block 3, measurement availability: If there is no new measurement until the time of the a priori estimated state, the correction step is not executed. This allows the algorithm to run the ekf with a higher rate, then the IMU provide data. To summarize: If we have no new data from the sensors the system just keeps propagating based on the physical model.

Block 4, finding the closest measurement: In this block it is searched for the closest measurement to the time of the a priori estimated state in block 2. If until the time of the estimation several sensor values are available only the newest and therefore most accurate value is taken for the correction.

Block 5, measurement selection: Mostly not all sensors of an IMU provide an output with the same rate. Here it is tested, weather we have a new sensor

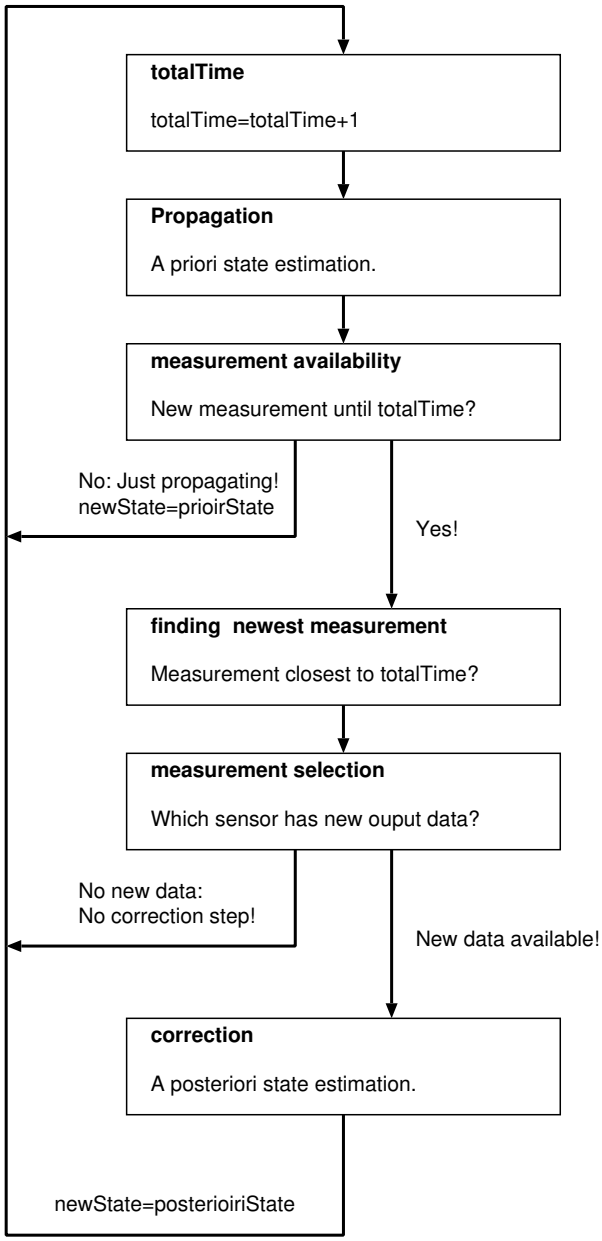

Figure 3.5: The graphical represenetation of the algorithm's structure.

value or is it still the one of the previous estimation. The correction step in block 5 is only for the new data executed. The other one still just propagate.

Block 6, correction: As last step the correction of the a priori estimation takes place and the posteriori estimation is calculated. How the relationship between the state and the measurements look like is explained in chapter 3.4

Error Covariance

For the measurement error covariance the noise of the different sensors are taken from the data sheets. But they were manually scaled according to have more accurate and stable filter. For the propagation model the covariance was estimated on how accurate the equations are. But also in this case were they manually adjusted afterwards. For an easier handling only the diagonal elements have a value. The off diagonal values are all zero.

Jacobian Matrix

In chapter 3.1 the matrixes H and A were derived. Since the physical model and relations between state and the measurements are non linear, H and A are the Jacobian matrixes of the functions f and h. For having an accurate as possible solution the Jacobian was in a first version calculated analytically with symbolic toolbox from MathWorks. The Jacobian matrix then has to be evaluated in every iteration step. Simulating 0.01 seconds took the filter much longer than 10 minutes. It was then decided to rewrite the algorithm calculating the Jacobian matrixes numerical. The function ekf.m [..ekfwebsite..]from MathWorks was restructured to match the requirements of this algorithm. It uses a complex step differentiation to calculate the derivatives of the function f and h [..papCompDiff..].

3.3 State Estimation Model

In order to propagate the state of the system x_k to the a priori state estimation x_{k+1}^- the filter needs to be able to predict in what state the system will be at time t_{k+1} based on its state at time t_k. In the most basic case, the assumption is that there exists no knowledge about the forces acting on the body. This leads to the so called "free mass model". However, in the case of a kite tethered to a ground station, the body is not able to move freely in three dimensions, but its movement is in a first approximation limited to a sphere with a given radius. This means, that one of the main forces acting on the body, the centripedal force, can be accounted for in the prediction. Furthermore an aerodynamical model of the kite might be able to predict also other forces than the centripedal force. In order to explore the benefits of such a model, we decided to use a spherical pendulum for the resons described in the introduction. In that case, all the forces acting on the body are known and the degrees of freedom are further reduced due to the bridled suspension. In the following sections, these two models are going to be described in detail.

Free Mass Model

The dynamics of the body are described by a system of first order differential equations describing the change in the state variables.

$$\dot{x} = g(x, t) \tag{3.15}$$

In this case the model is time invariant and thus g is not time dependant.

$$\dot{x} = g(x) \tag{3.16}$$

Since there is no knwoledge about the forces acting on the body, this set of equation looks rather simple:

$$g(x) = \begin{bmatrix} x_4 \\ x_5 \\ x_6 \\ 0 \\ 0 \\ 0 \\ x_{10} \\ x_{11} \\ x_{12} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.17}$$

Pendulum

Again the dynamics are described by a system of time invariant first order differential equations.

$$\dot{x} = g(x) \tag{3.18}$$

Due to the gravitation and the centripedal force being the only forces acting on the body, we can derive an exact set of differential equations that govern the motion of a spherical pendulum. Therefore we use the Euler-Lagrange-Equation to derive the differential equations as suggested in [12, 156ff].

With the kinetic energy

$$T = \frac{1}{2} m r^2 (\dot{\Theta}^2 + \dot{\Psi}^2 \cos^2 \Theta) \tag{3.19}$$

and the potential energy

$$V = -mr \sin \Theta \tag{3.20}$$

the Lagrangian is defined by:

$$L = T - V = \frac{1}{2}mr^2(\dot{\Theta}^2 + \dot{\Psi}^2\cos^2\Theta) + mr\sin\Theta \tag{3.21}$$

Substituting the Lagrangian into Euler-Lagrange-Equation

$$\frac{\partial L}{\partial \Psi} - \frac{d}{dt}\frac{\partial L}{\partial \dot{\Psi}} = 0 \tag{3.22}$$

and solving for $\ddot{\Psi}$ results in:

$$\ddot{\Psi} = 2\tan\Theta\dot{\Theta}\dot{\Psi} \tag{3.23}$$

And similarly for $\ddot{\Theta}$:

$$\frac{\partial L}{\partial \Theta} - \frac{d}{dt}\frac{\partial L}{\partial \dot{\Theta}} = 0 \tag{3.24}$$

$$\ddot{\Theta} = \frac{\cos\Theta(g - r\sin\Theta\dot{\Psi}^2)}{r} \tag{3.25}$$

The third degree of freedom, the body's rotation about its z-axis, is assumed to be constant. However, due to the convention of the euler angles, a change in phi contributes an additional term to the z component of the rotation vector in the body frame. (For further explanation see section ...) To compensate for that, the second derivative of Φ is not zero but defined as follows:

$$\frac{d}{dt}w_z^{body} = \frac{d}{dt}(\dot{\Phi} - \sin\Theta\dot{\Psi}) = 0 \tag{3.26}$$

$$\ddot{\Phi} = \cos\Theta\dot{\Theta}\dot{\Psi} + \sin\Theta\ddot{\Psi} \tag{3.27}$$

With the radius assumed to be constant, the fourth and eighth state variable (r and $\dot{r}$) are not changing and thus their time derivatives are zero.

Therefore the set of differential equations is given by:

$$g(x) = \begin{bmatrix} x_5 \\ x_6 \\ x_7 \\ 0 \\ \cos x_2\dot{x_2}\dot{x_3} + \sin x_2\ddot{x_3} \\ \dfrac{\cos x_2(g - r\sin x_2\dot{x_3}^2)}{r} \\ 2\tan x_2\dot{x_2}\dot{x_3} \\ 0 \end{bmatrix} \tag{3.28}$$

Solving the Differential Equations

So far we have derived the sets of differential equations that contain all the knowledge we have about the systems. To calculate the a priori state estimation x_{k+1}^{-} from the state of the system x_k we now only need to solve these sets of differnetial equations. This is done numerically using the classical fourth-order Runge-Kutta method [13]. Note that in our case g(x) is time invariant.

$$k_1 = hg(t_n, x_n) \tag{3.29}$$
$$k_2 = hg(t_n + \frac{1}{2}h, x_n + \frac{1}{2}k_1) \tag{3.30}$$
$$k_3 = hg(t_n + \frac{1}{2}h, x_n + \frac{1}{2}k_2) \tag{3.31}$$
$$k_4 = hg(t_n + h, x_n + k_3) \tag{3.32}$$
$$x_{n+1} = x_n + \frac{1}{6}k_1 + \frac{1}{3}k_2 + \frac{1}{3}k_3 + \frac{1}{6}k_4 + \mathcal{O}(h^5) \tag{3.33}$$

3.4 Sensor Estimation Model

An illustration of the relation between the position and velocity in (y, x, z) or (dx, dy, dz) and the two angles Φ, Θ and Ψ is shown in figure 3.4. With this sketch, the assumption of a constant radius and the fact that the velocity is the derivative of the position we get to the equations:

$$pos\ x = R * cos(\Theta)cos(\Psi) \tag{3.34}$$
$$pos\ y = R * sin(\Psi)cos(\Theta) \tag{3.35}$$
$$pos\ z = R * sin(\Theta) \tag{3.36}$$
$$vel\ x = -sin(\Theta)cos(\Psi) * R * \dot{\Theta} - cos(\Theta)sin(\Psi) * R * \dot{\Psi} \tag{3.37}$$
$$vel\ y = -sin(\Theta)sin(\Psi) * R * \dot{\Theta} + cos(\Theta)cos(\Psi) * R * \dot{\Psi} \tag{3.38}$$
$$vel\ z = -cos(\Theta) * R * \dot{\Theta} \tag{3.39}$$
$$\tag{3.40}$$

The centripetal acceleration always accting in z direction of the sensor can be calculated by the formula:

$$a_{cp} = \frac{v^2}{R} \tag{3.41}$$

We then have the an additional acceleration of the earth gravitation. The earth gravitation is in the inertial frame only in z direction and has to be transformed with the DCM_{bi} from the inertial in the body frame. Finally the acceleration can be written as:

$$acc = \begin{bmatrix} 0 \\ 0 \\ \frac{v^2}{R} \end{bmatrix} + DCM_{bi} * \begin{bmatrix} 0 \\ 0 \\ g \end{bmatrix} \tag{3.42}$$

The magnetic field is a constant value in Zurich. By transforming that into the body frame again with the help of the DCM_{bi}, the expected measurement from the magnetometer is calculated:

$$mag = DCM_{bi} * \begin{bmatrix} 0.2145 \\ 0.0060 \\ 0.4268 \end{bmatrix} [gauss] \tag{3.43}$$

The gyroscope measurement is directly represented by the rate of the euler angles Φ,$\dot{\Theta}$ and $\dot{\Psi}$. Since the euler angular rate has to be transformed into the body frame coordinates and additinally has a converstion about which axes is rotated the first, what the gyroscope has not,a transformation matrix has to be used as follows:

$$gyro = \begin{bmatrix} 1 & 0 & -sin(\Theta) \\ 0 & cos(\Phi) & sin(\Phi)cos(\Theta) \\ 0 & -sin(\Phi) & cos(\Phi)cos(\Theta) \end{bmatrix} * \begin{bmatrix} \dot{\Psi} \\ \dot{\Theta} \\ \dot{\Phi} \end{bmatrix} \tag{3.44}$$

Because the position of the senors is not at the center of mass of the pendulum, an additional displacement vector has to be added to the position (compare figure 3.6). With transforming the distance between the center of mass and the sensor into the inertial frame, the position is adjusted. The displacement gives an additional velocity which is the crossproduct of the rate of rotation and the displacement from the center of mass. By the derivative of this additional velocity the additional acceleration is calculated. The displcement has no influence on the gyrometer measurement and the magnetometer.

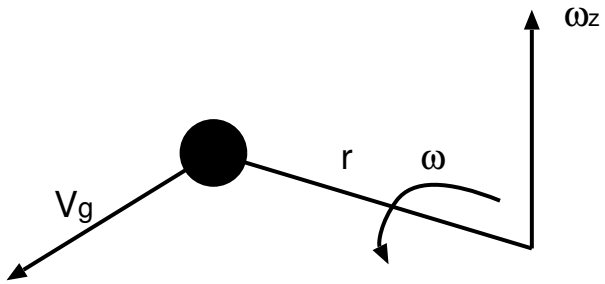

Figure 3.6: The black dot represents the sensor, while r is the distance between the center of mass of the pendulum and the sensor.

Chapter 4

Results - Vicon Test

4.1 Set up

4.2 Evaluation

4.2.1 short vs long radius

4.2.2 Outage and Sensor rate

4.2.3 Pixhawk vs Xsens

Chapter 5

Conclusion

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Appendix A

Data Sheets of the PX4 sensors

A.1 Data Sheet of the Accelerometer

BMA180
Digital, triaxial acceleration sensor

Bosch Sensortec

BOSCH
Invented for life

General description

The BMA180 is an ultra high performance digital triaxial acceleration sensor, aiming for low power consumer market applications.

The BMA180 allows high accurate measurement of accelerations in 3 perpendicular axes and thus senses tilt, motion, shock and vibration in cell phones, handhelds, computer peripherals, man-machine interfaces, virtual reality features and game controllers.

The BMA180 is highly configurable in order to give the designer full flexibility when integrating the sensor into his system. All features can be set by software via the digital interface. Here the user can choose between an I²C and an SPI (4-wire) interface mode.

BMA180 target applications

- Navigation (INS / Dead Reckoning)
- High accurate tilt detection (e.g. tilt compensated compass)
- Pointing and menu scrolling
- Display profile switching (portrait / landscape)
- Gaming
- Drop detection for warranty logging
- Shock detection
- Step-counting

Sensor operation

The BMA180 represents a new generation of digital acceleration sensors with a unique performance and feature set within 3 mm x 3 mm x 0.9 mm standard LGA package.

Key features BMA180
▶ All parameters and features user programmable
▶ 7 user programmable g-ranges and 10 selectable bandwidth settings
▶ Low-power consumption
▶ Ultra-low-power self-wake-up mode
▶ User programmable interrupt engine
▶ 0g offset regulation and in-field offset re-calibration with ultra-high accuracy
▶ SPI (4-wire) / I²C interface
▶ RoHS compliant, halogen-free

Technical data		BMA180
Sensitivity axes		x/y/z
Measurement range (switchable via SPI / I²C)		±1g, ±1.5g, ±2g, ±3g, ±4g, ±8g, ±16g
Sensitivity (calibrated)		1g: 8192LSB/g 1.5g: 5460LSB/g 2g: 4096LSB/g 3g: 2730LSB/g 4g: 2048LSB/g 8g: 1024LSB/g 16g: 512LSB/g
Resolution		14bit ⇨ 0.244mg (±2g range) (switchable 12 bit option)
Nonlinearity		±0.15% FS (±2g range)
Zero-g offset (ex-factory)		±15mg
Zero-g offset (after offset fine tuning)		±5mg
Zero-g offset temperature drift		±0.5mg/K
Noise density		150µg/√Hz
Bandwidth (switchable via SPI/I²C)	low pass	10Hz ... 1200Hz
	high pass	1Hz
	band pass	0.2 ... 300Hz
Digital input / output		SPI & I²C, interrupt pin
Supply voltages	V_{DD}	1.62 ... 3.6V
	V_{DDIO}	1.20 ... 3.6V
Current consumption		650µA
Temperature range		-40°C ... +85°C

One of the key elements of the BMA180 is the intelligent interrupt engine that gives the hard- and software designer full control. Various motion detection scenarios can be identified by the BMA180 and signaled to the system via a simple interrupt pin. By using the digital serial interface, the exact details of the motion event that triggered the interrupt can be read-out.

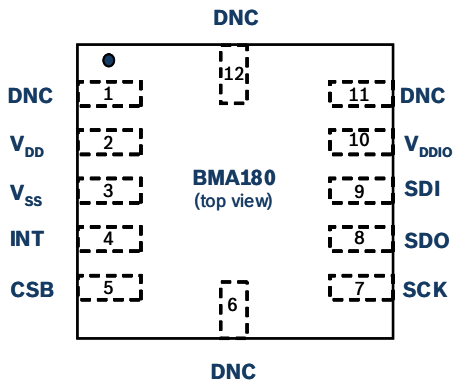
Following motion detection use case scenarios are supported by the interrupt engine:

- Any-motion (slope) detection
- Tap sensing
- Low-g/high-g detection
- Data-ready with sample skipping option
- Self-wake-up

The interrupts can be conveniently configured by the user and thus perfectly support the integration of the BMA180 into the user's system environment.

Another important feature of the BMA180 acceleration sensor is the power management module. This module allows for optimizing the sensor's power consumption in-line with the specific user requirements. Thus, it is not necessary to operate the sensor at full power for all application scenarios all the time. For some use cases the power consumption drastically shrinks to just a fraction of what would be required in full performance mode. Moreover this feature of the BMA180 allows for an intelligent system power management and thus significant reduction of the whole system's power consumption. In particular, this helps increasing battery life-time of any kind of mobile device.

BMA180 Pin configuration (top view)



Pin No.	Name	Function
1	DNC	Do not connect
2	VDD	Analog supply voltage
3	VSS	Ground
4	INT	Interrupt output
5	CSB	SPI chip select
6	DNC	Do not connect
7	SCK	Serial clock
8	SDO	Serial data output
9	SDI	Serial data in/out
10	VDDIO	Digital interface power supply
11	DNC	Do not connect
12	DNC	Do not connect

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A.2 Data Sheet of the Gyroscope

L3GD20

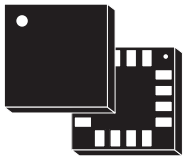
MEMS motion sensor: three-axis digital output gyroscope

Features

- Three selectable full scales (250/500/2000 dps)
- I^2C/SPI digital output interface
- 16 bit-rate value data output
- 8-bit temperature data output
- Two digital output lines (interrupt and data ready)
- Integrated low- and high-pass filters with user-selectable bandwidth
- Wide supply voltage: 2.4 V to 3.6 V
- Low voltage-compatible IOs (1.8 V)
- Embedded power-down and sleep mode
- Embedded temperature sensor
- Embedded FIFO
- High shock survivability
- Extended operating temperature range (-40 °C to +85 °C)
- ECOPACK® RoHS and “Green” compliant

Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics



LGA-16 (4x4x1 mm)

Description

The L3GD20 is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface capable of providing the measured angular rate to the external world through a digital interface (I^2C/SPI).

The sensing element is manufactured using a dedicated micro-machining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The L3GD20 has a full scale of ±250/±500/ ±2000 dps and is capable of measuring rates with a user-selectable bandwidth.

The L3GD20 is available in a plastic land grid array (LGA) package and can operate within a temperature range of -40 °C to +85 °C.

Table 1. Device summary

Order code	Temperature range (°C)	Package	Packing
L3GD20	-40 to +85	LGA-16 (4x4x1 mm)	Tray
L3GD20TR	-40 to +85	LGA-16 (4x4x1 mm)	Tape and reel

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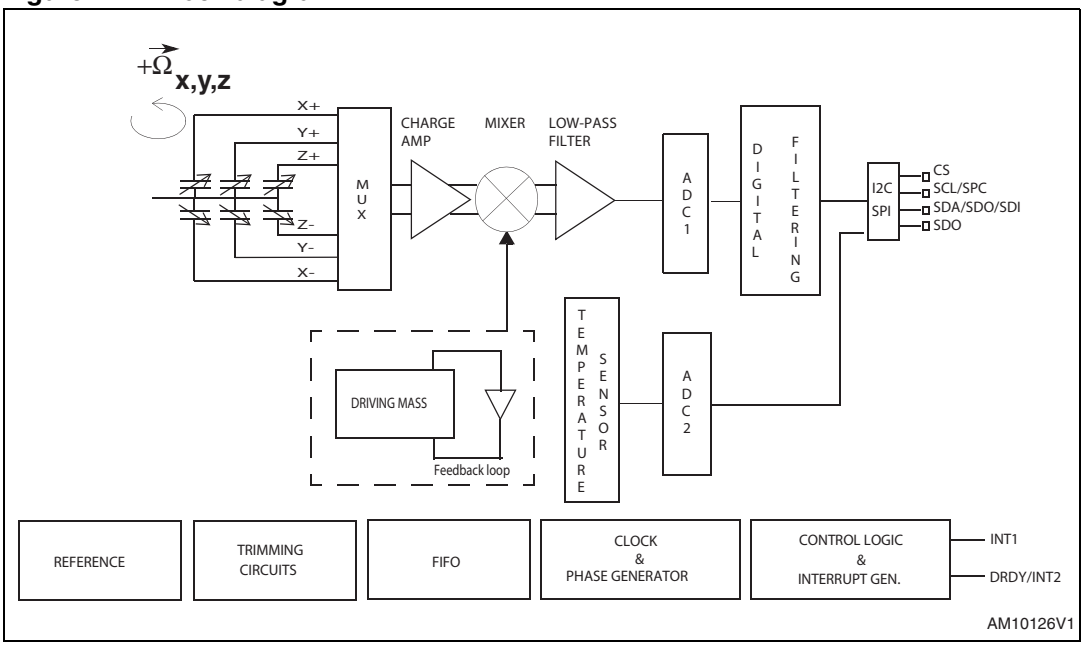
1 Block diagram and pin description

Figure 1. Block diagram



Note: The vibration of the structure is maintained by drive circuitry in a feedback loop. The sensing signal is filtered and appears as a digital signal at the output.

1.1 Pin description

Figure 2. Pin connection

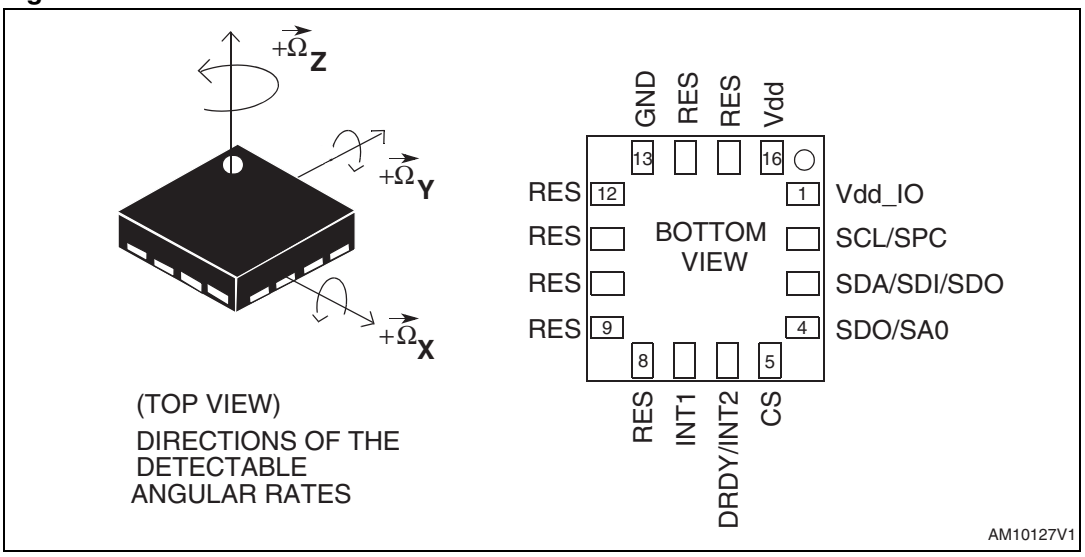


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO(1)	Power supply for I/O pins
2	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
5	CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
6	DRDY/INT2	Data ready/FIFO interrupt (Watermark/Overrun/Empty)
7	INT1	Programmable interrupt
8	Reserved	Connect to GND
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND
12	Reserved	Connect to GND
13	GND	0 V supply
14	Reserved	Connect to GND with ceramic capacitor(2)
15	Reserved	Connect to Vdd
16	Vdd(3)	Power supply

1. 100 nF filter capacitor recommended.
2. 1 nF min value must be guaranteed under 11 V bias condition.
3. 100 nF plus 10 µF capacitors recommended.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted.

Table 3. Mechanical characteristics(1)

Symbol	Parameter	Test condition	Min.	Typ.(2)	Max.	Unit
FS	Measurement range	User-selectable		±250		dps
				±500		
				±2000		
So	Sensitivity	FS = 250 dps		8.75		mdps/digit
		FS = 500 dps		17.50		
		FS = 2000 dps		70		
SoDr	Sensitivity change vs. temperature	From -40 °C to +85 °C		±2		%
DVoff	Digital zero-rate level	FS = 250 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±75		
OffDr	Zero-rate level change vs. temperature	FS = 250 dps		±0.03		dps/°C
		FS = 2000 dps		±0.04		dps/°C
NL	Non linearity	Best fit straight line		0.2		% FS
Rn	Rate noise density			0.03		dps/ (√Hz
ODR	Digital output data rate			95/190/ 380/760		Hz
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V. The operational power supply range is specified in *Table 4*.
2. Typical specifications are not guaranteed.

2.2 Electrical characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

Table 4. Electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		2.4	3.0	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.71		Vdd+0.1	V
Idd	Supply current			6.1		mA
IddSL	Supply current in sleep mode(4)	Selectable by digital interface		2		mA
IddPdn	Supply current in power-down mode	Selectable by digital interface		5		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses; in this condition the measurement chain is powered off.
4. Sleep mode introduces a faster turn-on time relative to power-down mode.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

Table 5. Electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ.(2)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

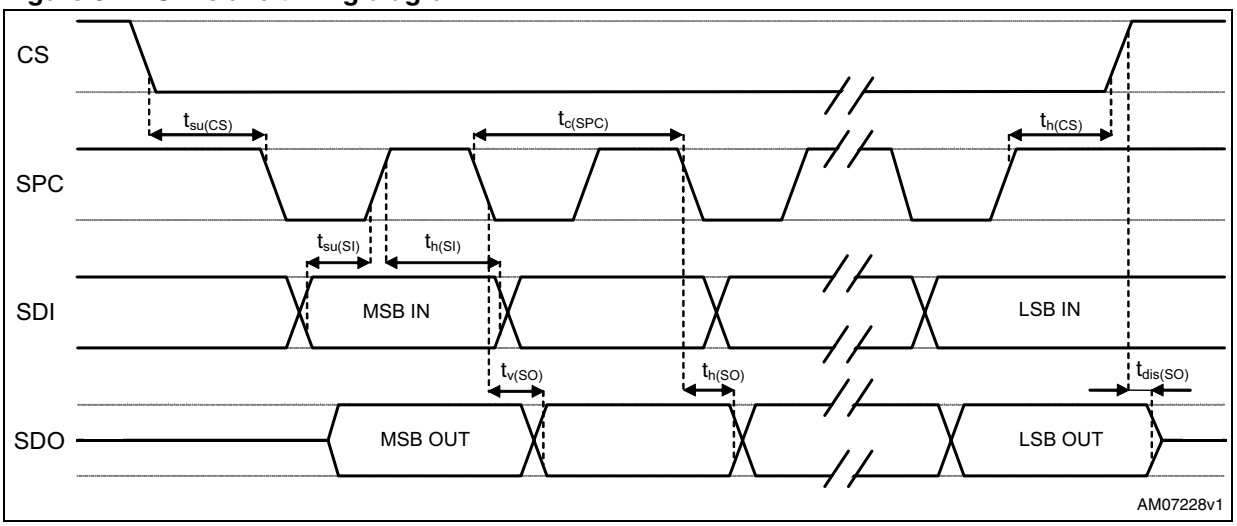
Subject to general operating conditions for Vdd and T_{op}.

Table 6. SPI slave timing values

Symbol	Parameter	Value[1]		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	6		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at a 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results; not tested in production.

Figure 3. SPI slave timing diagram [a]



a. Measurement points are at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output port.

2.4.2 I²C - Inter IC control interface

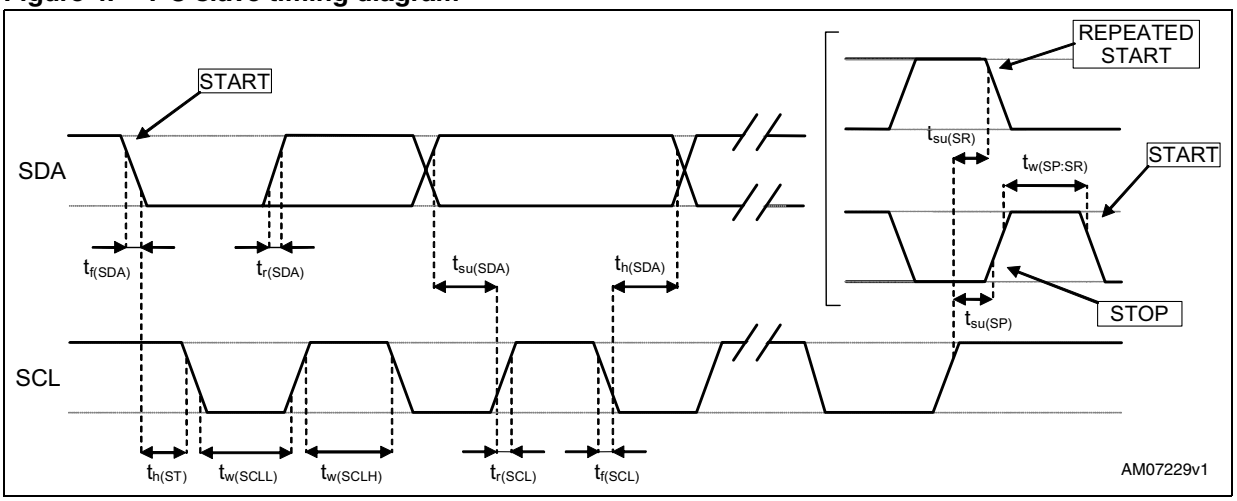
Subject to general operating conditions for Vdd and T_{op}.

Table 7. I²C slave timing values (TBC)

Symbol	Parameter	I²C standard mode(1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement; not tested in production.
2. Cb = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram (b)



b. Measurement points are at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	*g*
ESD	Electrostatic discharge protection	2 (HBM)	kV
		1.5 (CDM)	kV
		200 (MM)	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

2.6 Terminology

2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counter-clockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

2.7 Soldering information

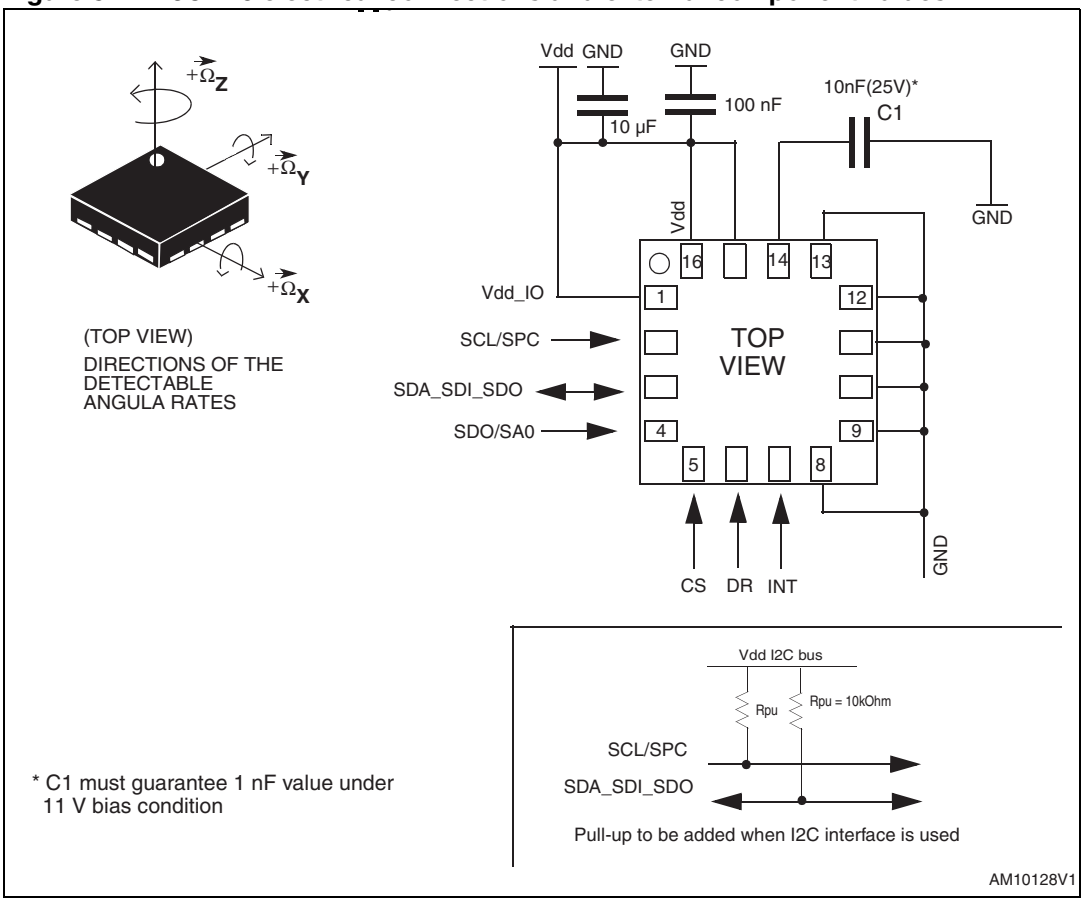
The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

3 Application hints

Figure 5. L3GD20 electrical connections and external component values



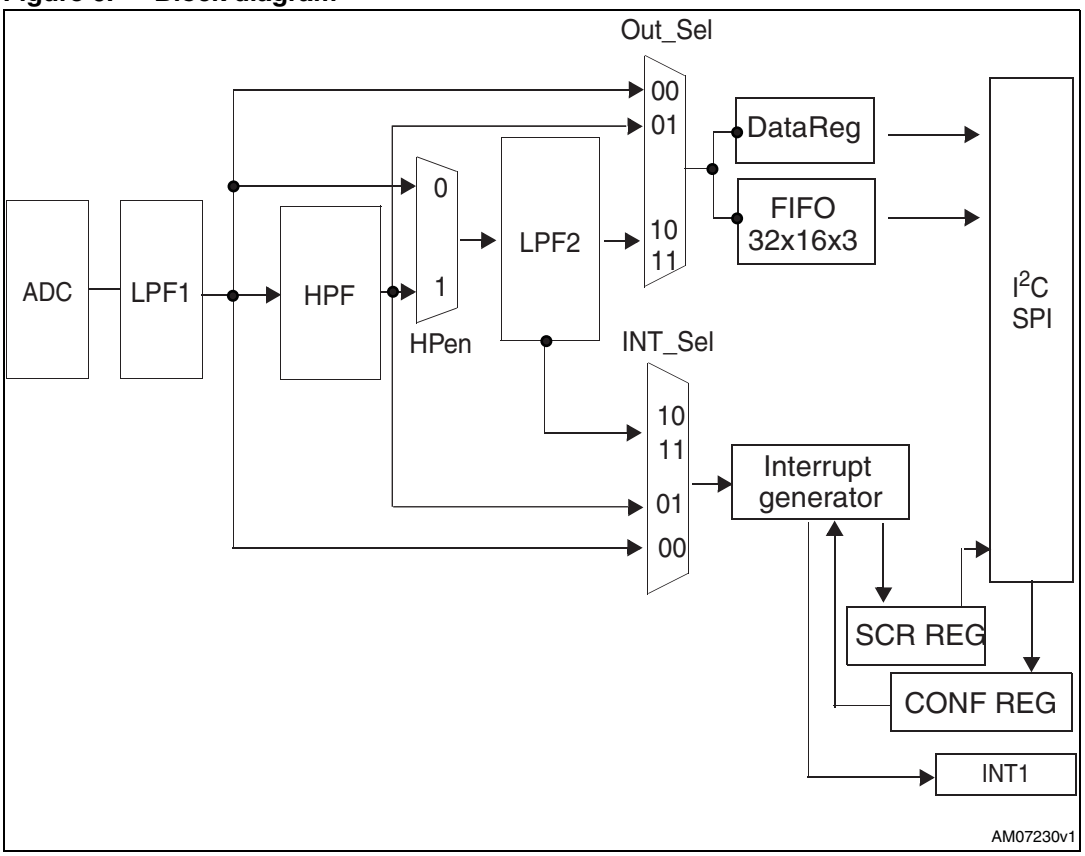
Power supply decoupling capacitors (100 nF + 10 µF) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd_IO are not connected together, 100 nF and 10 µF decoupling capacitors must be placed between Vdd and common ground, and 100 nF between Vdd_IO and common ground. Capacitors should be placed as near as possible to the device (common design practice).

4 Digital main blocks

4.1 Block diagram

Figure 6. Block diagram



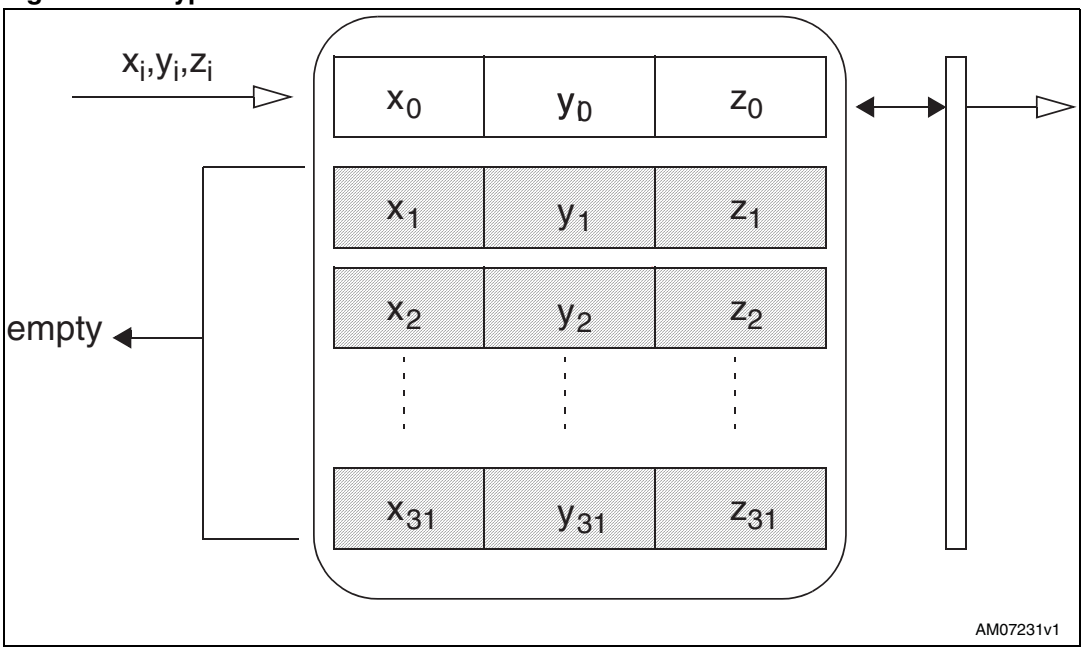
4.2 FIFO

The L3GD20 embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in the FIFO_CTRL_REG (2Eh). Programmable Watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3 (22h) and event detection information is available in FIFO_SRC_REG (2Fh). Watermark level can be configured to WTM4:0 in FIFO_CTRL_REG (2Eh).

4.2.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 7* below, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.

Figure 7. Bypass mode

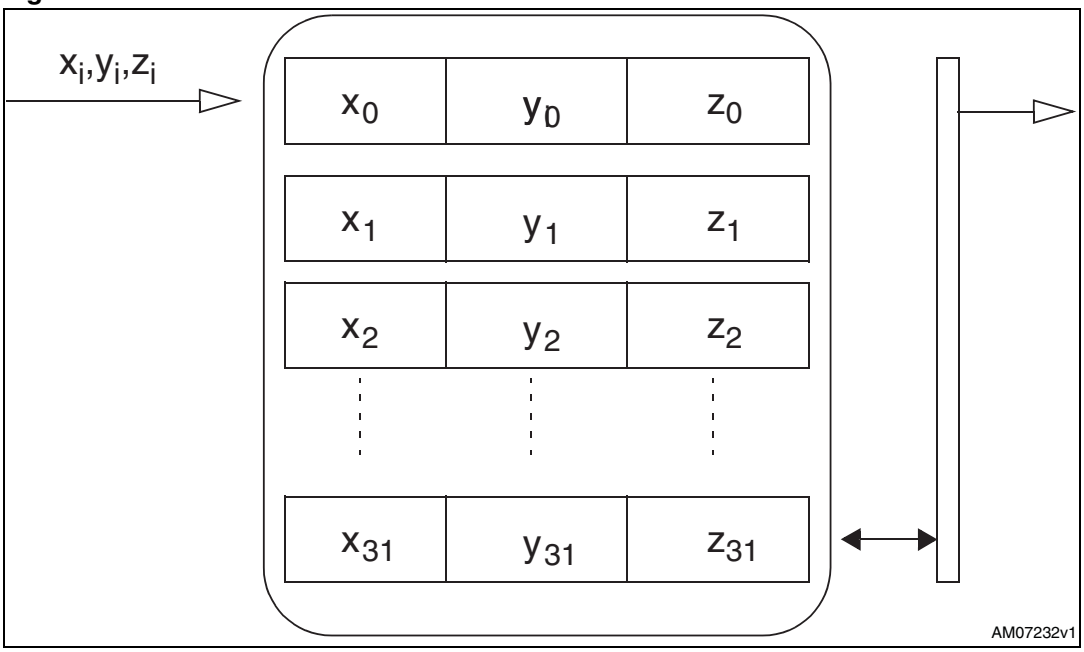


4.2.2 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit into CTRL_REG3 (22h)) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of FIFO_CTRL_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, the FIFO_CTRL_REG (2Eh) must be written back to Bypass mode.

FIFO mode is represented in *Figure 8: FIFO mode*.

Figure 8. FIFO mode

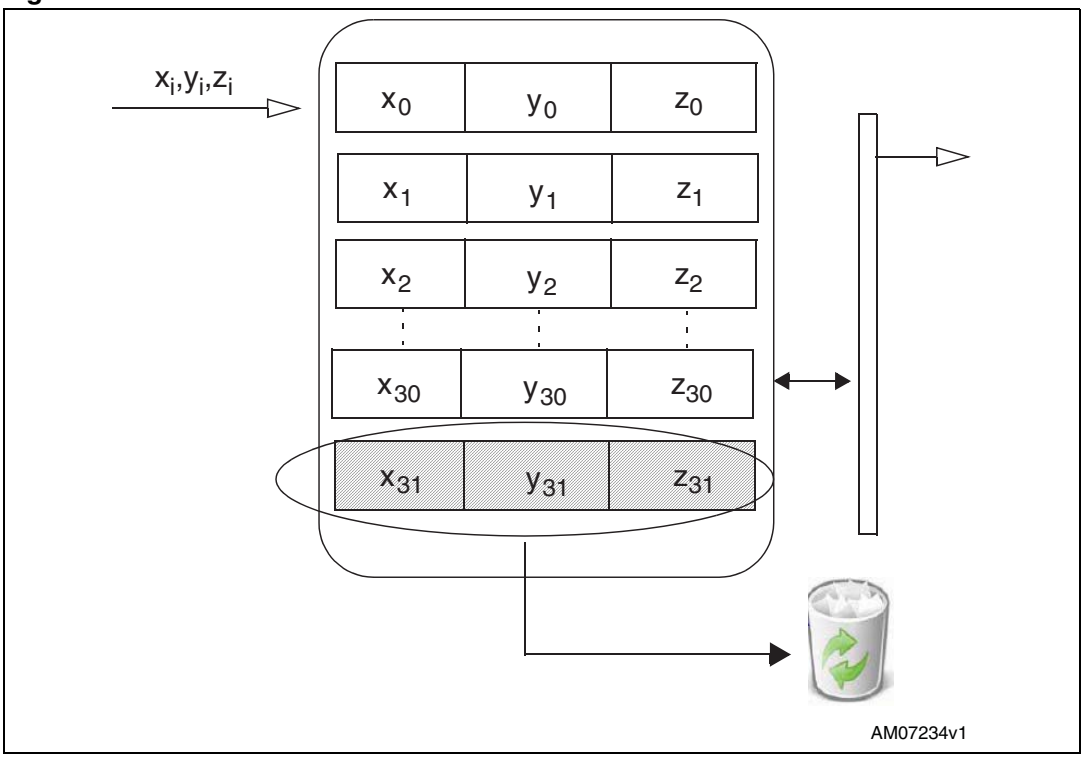


4.2.3 Stream mode

In Stream mode, data from yaw, pitch and roll measurement are stored in the FIFO. A watermark interrupt can be enabled and set as in the FIFO mode.The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3 (22h).

Stream mode is represented in *Figure 9: Stream mode*.

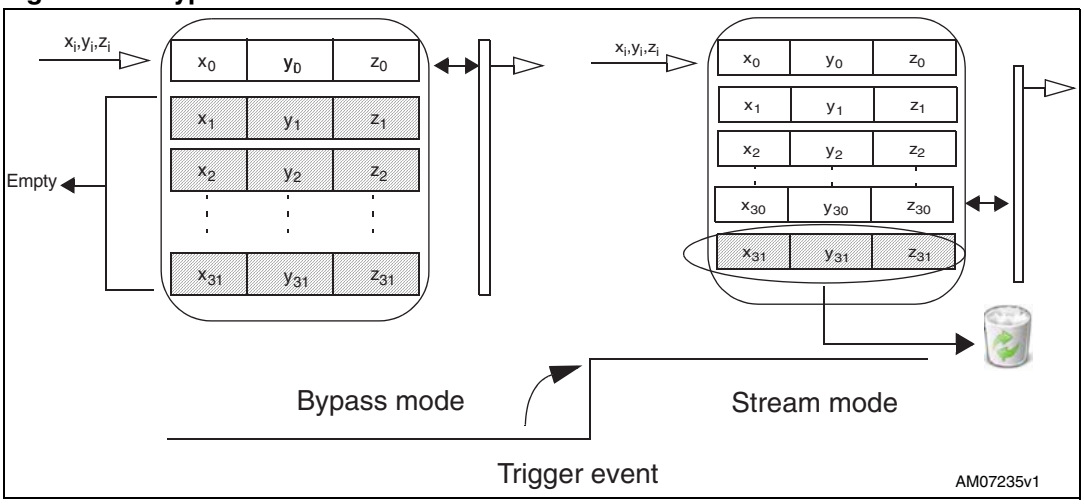
Figure 9. Stream mode



4.2.4 Bypass-to-stream mode

In Bypass-to-stream mode, the FIFO begins operating in Bypass mode and once a trigger event occurs (related to INT1_CFG (30h) register events), the FIFO starts operating in Stream mode. Refer to *Figure 10* below.

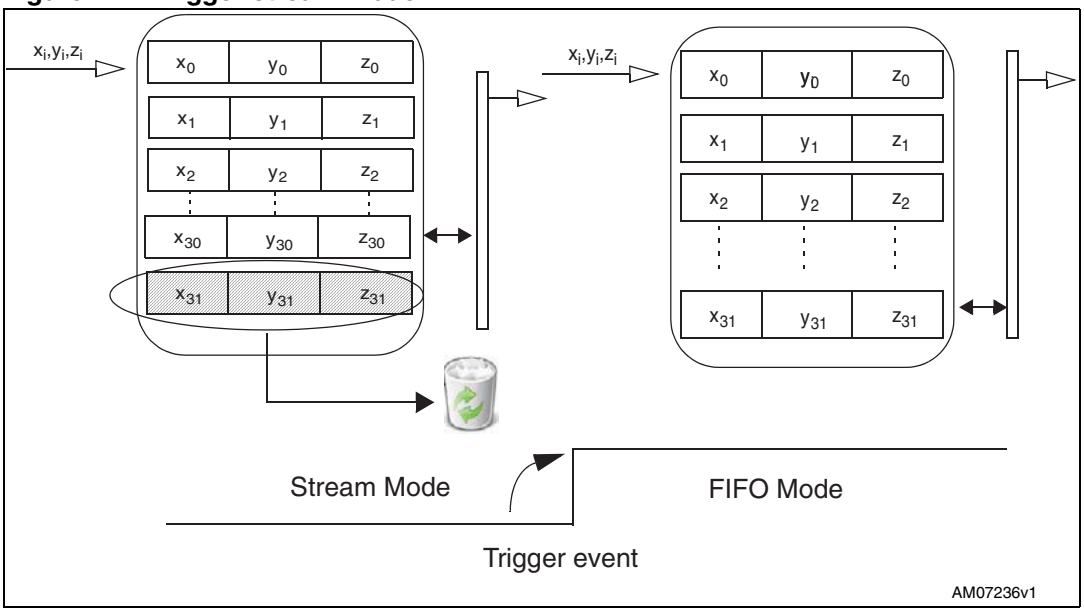
Figure 10. Bypass-to-stream mode



4.2.5 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled on pin DRDY/INT2 by setting the I2_WTM bit in CTRL_REG3 (22h) in order to be raised when the FIFO is filled to the level specified in the WTM4:0 bits of FIFO_CTRL_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to INT1_CFG (30h) register events), the FIFO starts operating in FIFO mode. Refer to *Figure 11* below.

Figure 11. Trigger stream mode



4.2.6 Retrieve data from FIFO

FIFO data is read through OUT_X (Addr reg 28h,29h), OUT_Y (Addr reg 2Ah,2Bh) and OUT_Z (Addr reg 2Ch,2Dh). When the FIFO is in Stream, Trigger or FIFO mode, a read operation of the OUT_X, OUT_Y or OUT_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll and yaw data is placed in the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst (X,Y & Z with auto-incrementing address) operations can be used. When data included in OUT_Z_H (2Dh) is read, the system restarts to read information from addr OUT_X_L (28h).

5 Digital interfaces

The registers embedded in the L3GD20 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO) I^2C less significant bit of the device address

5.1 I^2C serial interface

The L3GD20 I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 10. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated with the L3GD20 is 110101xb. The **SDO** pin can be used to modify the less significant bit of the device address. If the SDO pin is connected to voltage supply, LSb is ‘1’ (address 1101011b). Otherwise, if the SDO pin is connected to ground, the LSb value is ‘0’ (address 1101010b). This solution allows to connect and address two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obligated to generate an acknowledge after each byte of data received.

The I²C embedded in the L3GD20 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 11* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 11. SAD+read/write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	110101	0	1	11010101 (D1h)
Write	110101	0	0	11010100 (D0h)
Read	110101	1	1	11010111 (D3h)
Write	110101	1	0	11010110 (D2h)

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to ‘1’ while SUB(6-0) represents the address of the first register to be read.

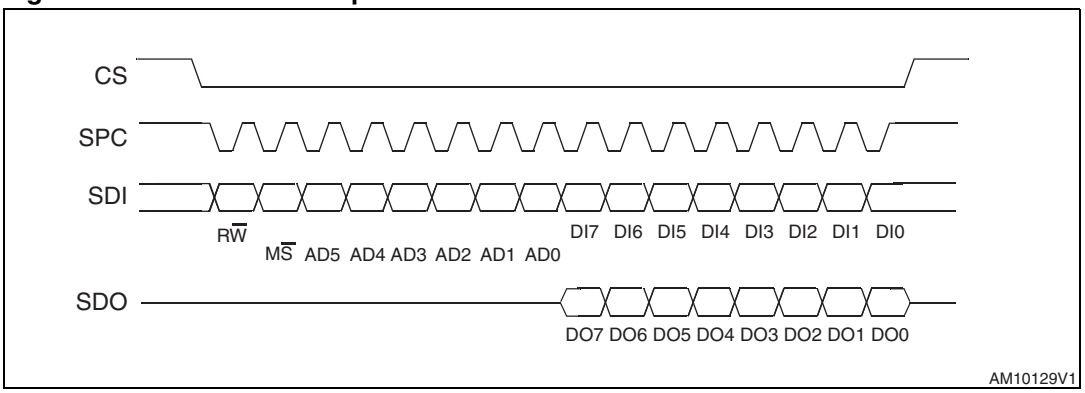
In the communication format presented, MAK is Master Acknowledge and NMAK is No Master Acknowledge.

5.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 12. Read and write protocol



CS is the Serial Port Enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address will be auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

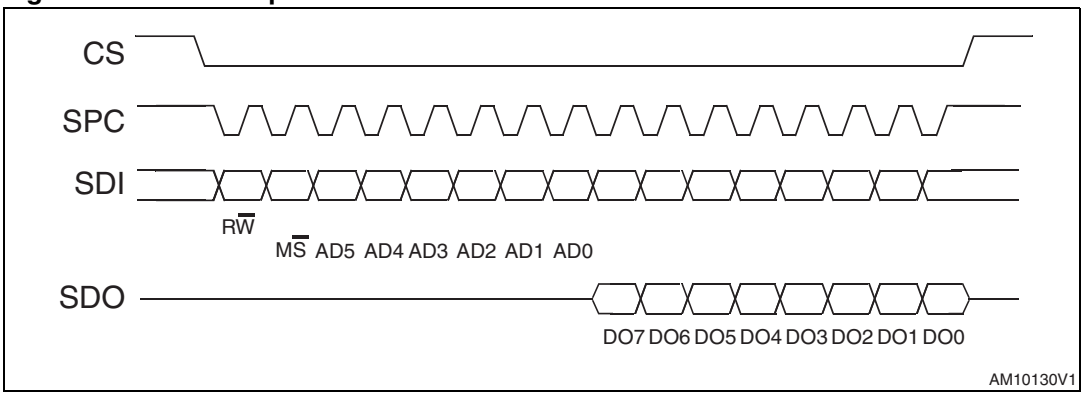
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods will be added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 13. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

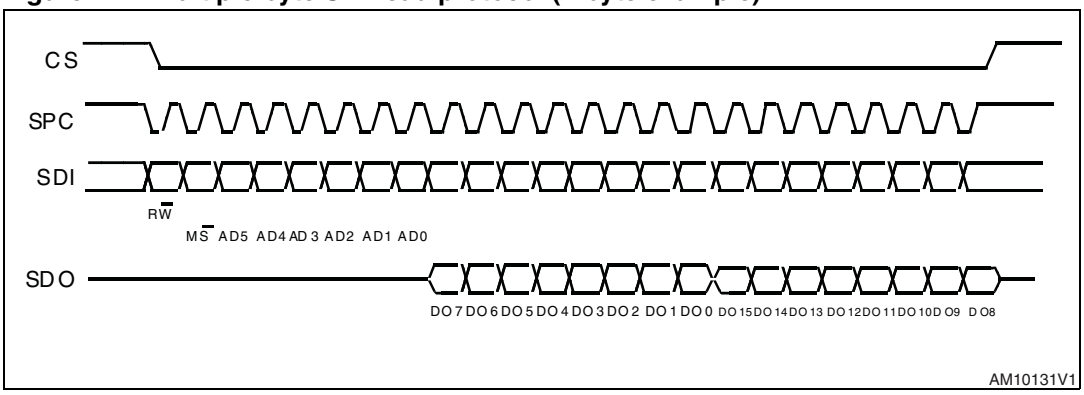
bit 1: M$\overline{S}$ bit. When 0 do not increment address; when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

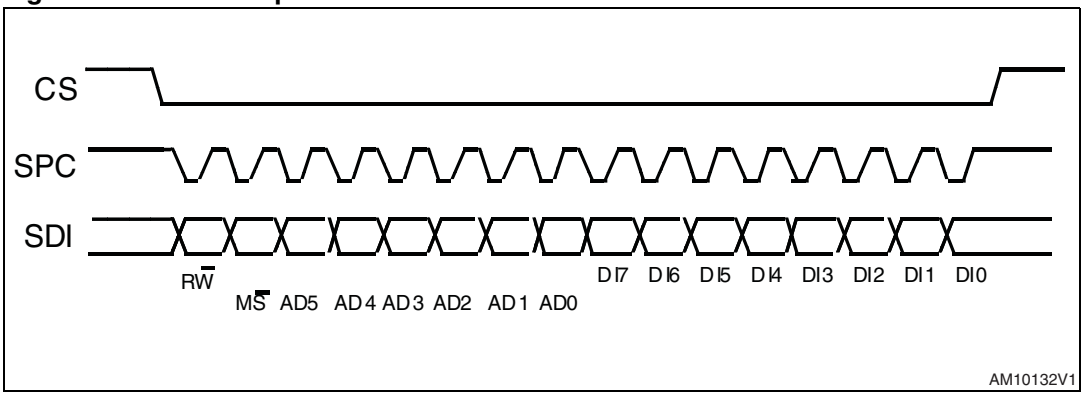
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 14. Multiple byte SPI read protocol (2-byte example)



5.2.2 SPI write

Figure 15. SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

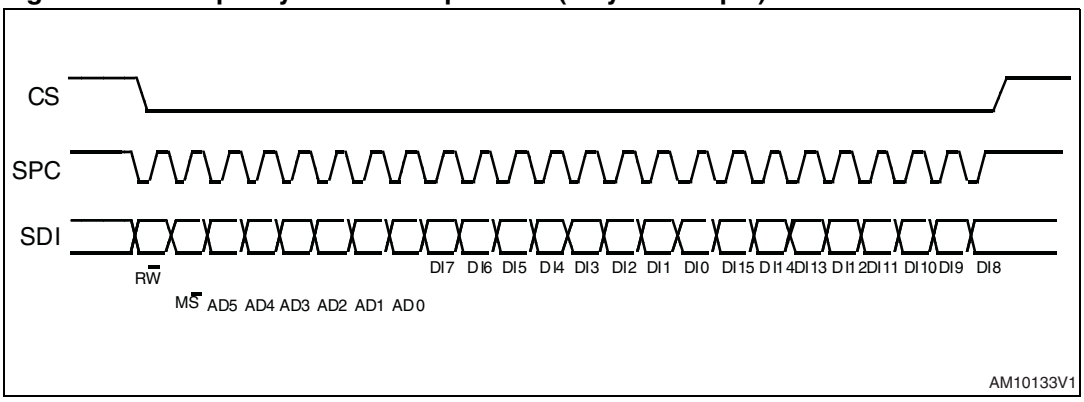
bit 1: M$\overline{S}$ bit. When 0, do not increment address; when 1, increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

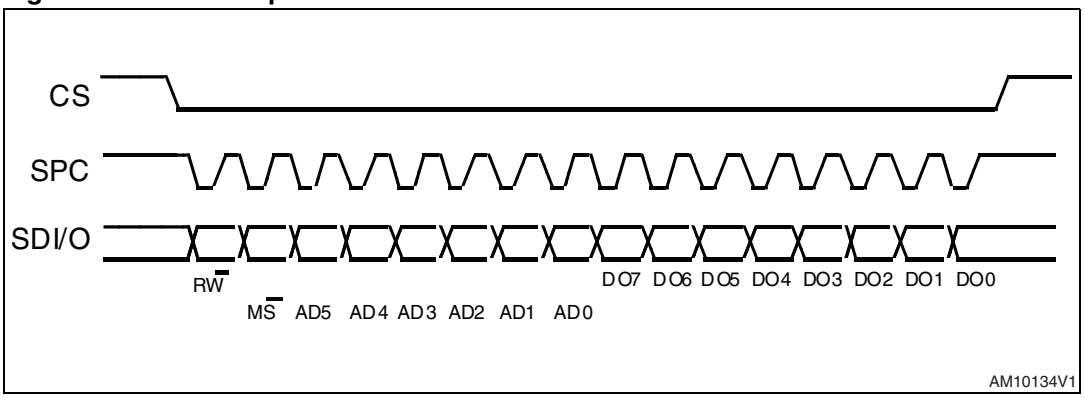
Figure 16. Multiple byte SPI write protocol (2-byte example)



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the bit SIM (SPI serial interface mode selection) to ‘1’ in CTRL_REG2.

Figure 17. SPI read protocol in 3-wire mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, do not increment address; when 1, increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wire mode.

6 Output register mapping

The table below provides a listing of the 8-bit registers embedded in the device, and the related addresses:

Table 16. Register address map

Name	Type	Register address		Default
		Hex	Binary	
Reserved	-	00-0E	-	-
WHO_AM_I	r	0F	000 1111	11010100
Reserved	-	10-1F	-	-
CTRL_REG1	rw	20	010 0000	00000111
CTRL_REG2	rw	21	010 0001	00000000
CTRL_REG3	rw	22	010 0010	00000000
CTRL_REG4	rw	23	010 0011	00000000
CTRL_REG5	rw	24	010 0100	00000000
REFERENCE	rw	25	010 0101	00000000
OUT_TEMP	r	26	010 0110	output
STATUS_REG	r	27	010 0111	output
OUT_X_L	r	28	010 1000	output
OUT_X_H	r	29	010 1001	output
OUT_Y_L	r	2A	010 1010	output
OUT_Y_H	r	2B	010 1011	output
OUT_Z_L	r	2C	010 1100	output
OUT_Z_H	r	2D	010 1101	output
FIFO_CTRL_REG	rw	2E	010 1110	00000000
FIFO_SRC_REG	r	2F	010 1111	output
INT1_CFG	rw	30	011 0000	00000000
INT1_SRC	r	31	011 0001	output
INT1_TSH_XH	rw	32	011 0010	00000000
INT1_TSH_XL	rw	33	011 0011	00000000
INT1_TSH_YH	rw	34	011 0100	00000000
INT1_TSH_YL	rw	35	011 0101	00000000
INT1_TSH_ZH	rw	36	011 0110	00000000
INT1_TSH_ZL	rw	37	011 0111	00000000
INT1_DURATION	rw	38	011 1000	00000000

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

7.1 WHO_AM_I (0Fh)

Table 17. WHO_AM_I register

1	1	0	1	0	1	0	0

Device identification register.

7.2 CTRL_REG1 (20h)

Table 18. CTRL_REG1 register

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen

Table 19. CTRL_REG1 description

DR1-DR0	Output data rate selection. Refer to *Table 20*
BW1-BW0	Bandwidth selection. Refer to *Table 20*
PD	Power-down mode enable. Default value: 0 (0: power-down mode, 1: normal mode or sleep mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR<1:0> is used for ODR selection. **BW <1:0>** is used for Bandwidth selection.

In the *Table 20* all frequencies resulting in combinations of DR / BW bits are reported.

Table 20. DR and BW configuration setting

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	00	95	12.5
00	01	95	25
00	10	95	25

Table 20. DR and BW configuration setting (continued)

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

A combination of **PD, Zen, Yen, Xen** is used to set device to different modes (power-down / normal / sleep mode) in accordance with *Table 21* below.

Table 21. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

7.3 CTRL_REG2 (21h)

Table 22. CTRL_REG2 register

0(1)	0(1)	HPM1	HPM1	HPCF3	HPCF2	HPCF1	HPCF0

1. These bits must be set to ‘0’ to ensure proper operation of the device

Table 23. CTRL_REG2 description

HPM1-HPM0	High-pass filter mode selection. Default value: 00 Refer to *Table 24*
HPCF3-HPCF0	High-pass filter cutoff frequency selection Refer to *Table 25*

Table 24. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 25. High-pass filter cut off frequency configuration [Hz]

HPCF3-0	ODR=95 Hz	ODR=190 Hz	ODR=380 Hz	ODR=760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45
1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

7.4 CTRL_REG3 (22h)

Table 26. CTRL_REG1 register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 27. CTRL_REG3 description

I1_Int1	Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT1. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT1. Default value 0. (0: high; 1:low)
PP_OD	Push-pull / Open drain. Default value: 0. (0: push- pull; 1: open drain)
I2_DRDY	Date-ready on DRDY/INT2. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY/INT2 Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)

7.5 CTRL_REG4 (23h)

Table 28. CTRL_REG4 register

BDU	BLE	FS1	FS0	-	0(1)	0(1)	SIM

1. This value must not be changed.

Table 29. CTRL_REG4 description

BDU	Block data update. Default value: 0 (0: continuos update; 1: output registers not updated until MSb and LSb reading)
BLE	Big/little endian data selection. Default value 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS1-FS0	Full scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

7.6 CTRL_REG5 (24h)

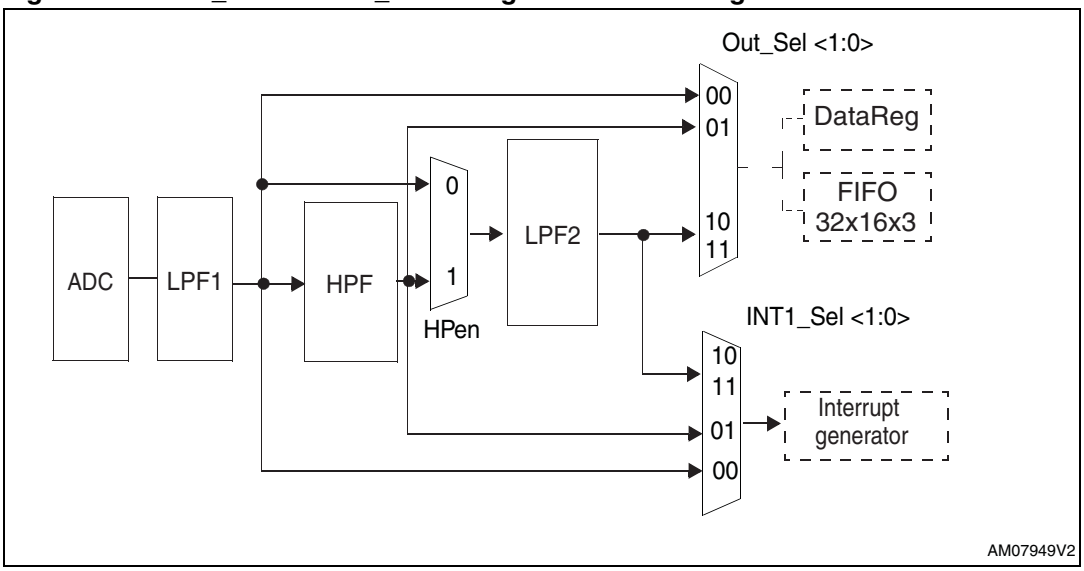
Table 30. CTRL_REG5 register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

Table 31. CTRL_REG5 description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
HPen	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled See Figure 20)
INT1_Sel1- INT1_Sel0	INT1 selection configuration. Default value: 0 (See *Figure 20*)
Out_Sel1- Out_Sel1	Out selection configuration. Default value: 0 (See *Figure 20*)

Figure 18. INT1_Sel and Out_Sel configuration block diagram



7.7 REFERENCE/DATACAPTURE (25h)

Table 32. REFERENCE register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 33. REFERENCE register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

7.8 OUT_TEMP (26h)

Table 34. OUT_TEMP register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 35. OUT_TEMP register description

Temp7-Temp0	Temperature data

Temperature data (1LSB/deg - 8-bit resolution). The value is expressed as two's complement.

7.9 STATUS_REG (27h)

Table 36. STATUS_REG register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 37. STATUS_REG description

ZYXOR	X, Y, Z -axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available;1: new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

7.10 OUT_X_L (28h), OUT_X_H (29h)

X-axis angular rate data. The value is expressed as two's complement.

7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

7.13 FIFO_CTRL_REG (2Eh)

Table 38. REFERENCE register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

Table 39. REFERENCE register description

FM2-FM0	FIFO mode selection. Default value: 00 (see *Table 40*)
WTM4-WTM0	FIFO threshold. Watermark level setting

Table 40. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

7.14 FIFO_SRC_REG (2Fh)

Table 41. FIFO_SRC register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 42. FIFO_SRC register description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

7.15 INT1_CFG (30h)

Table 43. INT1_CFG register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 44. INT1_CFG description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

7.16 INT1_SRC (31h)

Interrupt source register. Read only register.

Table 45. INT1_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 46. INT1_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Reading at this address clears INT1_SRC IA bit (and eventually the interrupt signal on the INT1 pin) and allows the refresh of data in the INT1_SRC register if the latched option was chosen.

7.17 INT1_THS_XH (32h)

Table 47. INT1_THS_XH register

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 48. INT1_THS_XH description

THSX14 - THSX9	Interrupt threshold. Default value: 0000 0000

7.18 INT1_THS_XL (33h)

Table 49. INT1_THS_XL register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 50. INT1_THS_XL description

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000

7.19 INT1_THS_YH (34h)

Table 51. INT1_THS_YH register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 52. INT1_THS_YH description

THSY14 - THSY9	Interrupt threshold. Default value: 0000 0000

7.20 INT1_THS_YL (35h)

Table 53. INT1_THS_YL register

THSR7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 54. INT1_THS_YL description

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000

7.21 INT1_THS_ZH (36h)

Table 55. INT1_THS_ZH register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 56. INT1_THS_ZH description

THSZ14 - THSZ9	Interrupt threshold. Default value: 0000 0000

7.22 INT1_THS_ZL (37h)

Table 57. INT1_THS_ZL register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 58. INT1_THS_ZL description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000

7.23 INT1_DURATION (38h)

Table 59. INT1_DURATION register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 60. INT1_DURATION description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following definitions:

Wait = ‘0’: the interrupt falls immediately if the signal crosses the selected threshold

Wait = ‘1’: if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 19. Wait disabled

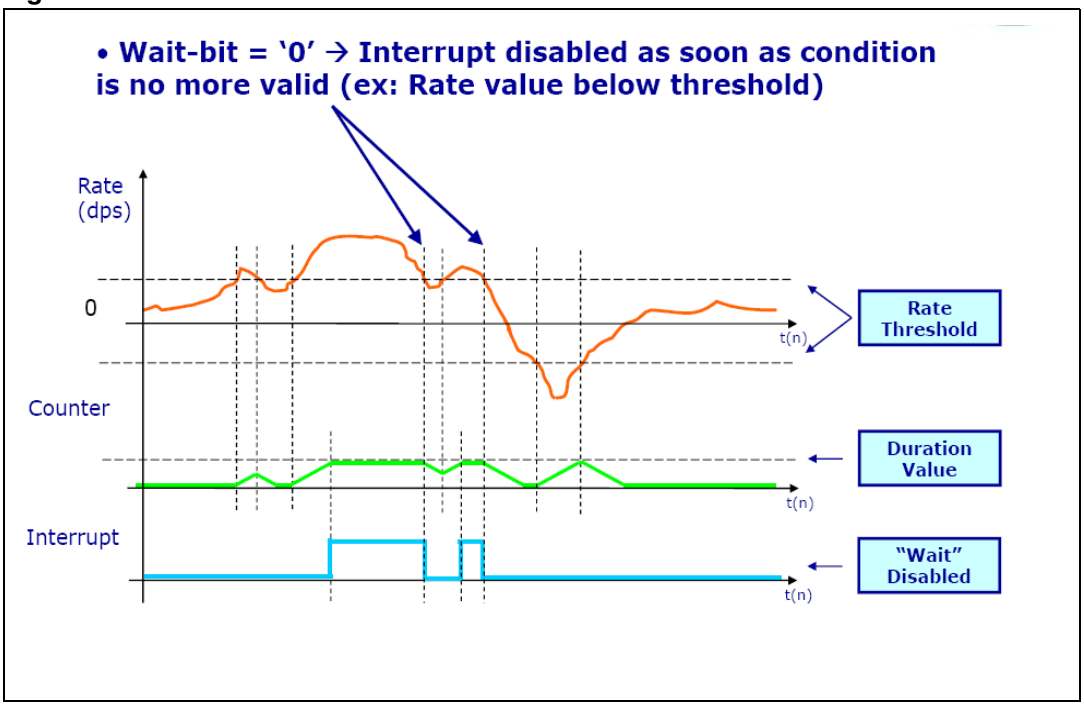
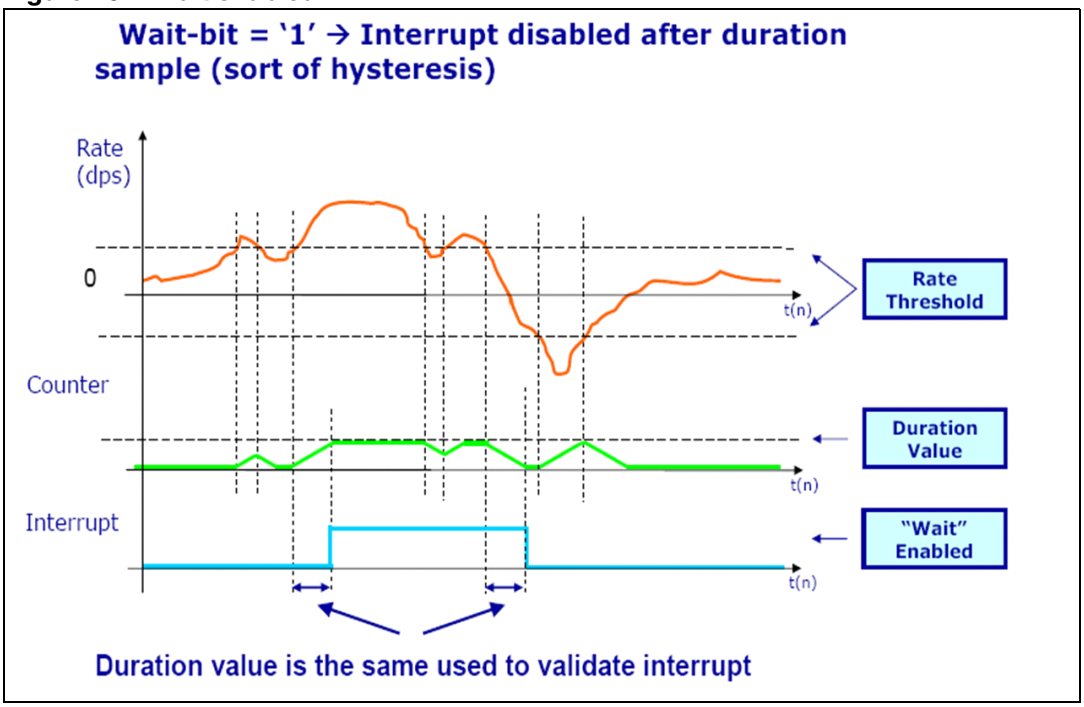


Figure 20. Wait enabled



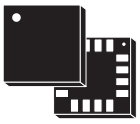
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

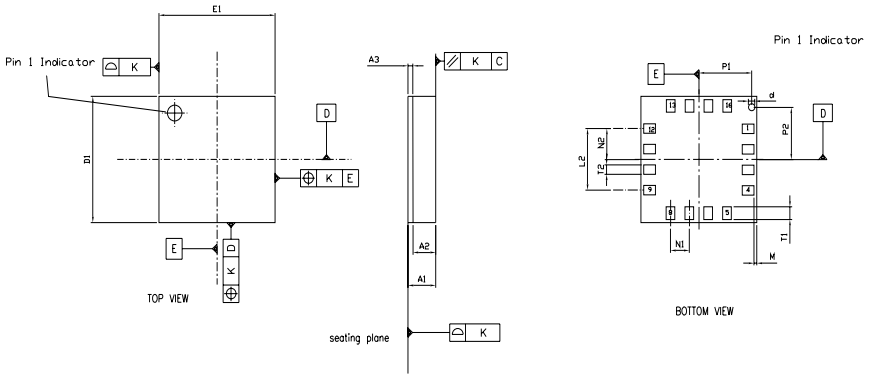
Figure 21. LGA-16: mechanical data and package dimensions

Ref.	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1			1.000			0.0394
A2		0.785			0.0309	
A3		0.200			0.0079	
d		0.300			0.0118	
D1	3.850	4.000	4.150	0.1516	0.1575	0.1634
E1	3.850	4.000	4.150	0.1516	0.1575	0.1634
L2		1.950			0.0768	
M		0.100			0.0039	
N1		0.650			0.0256	
N2		0.975			0.0384	
P1		1.750			0.0689	
P2		1.525			0.0600	
T1		0.400			0.0157	
T2		0.300			0.0118	
k		0.050			0.0020	

Outline and mechanical data



LGA-16 (4x4x1mm)
Land Grid Array Package



9 Revision history

Table 61. Document revision history

Date	Revision	Changes
18-Aug-2011	1	Initial release.

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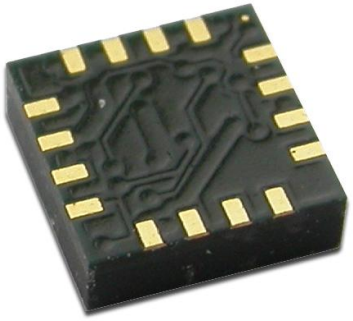
A.3 Data Sheet of the Magnetometer

3-Axis Digital Compass IC HMC5883L

Honeywell

Advanced Information

The Honeywell HMC5883L is a surface-mount, multi-chip module designed for low-field magnetic sensing with a digital interface for applications such as low-cost compassing and magnetometry. The HMC5883L includes our state-of-the-art, high-resolution HMC118X series magneto-resistive sensors plus an ASIC containing amplification, automatic degaussing strap drivers, offset cancellation, and a 12-bit ADC that enables 1° to 2° compass heading accuracy. The I^2C serial bus allows for easy interface. The HMC5883L is a 3.0x3.0x0.9mm surface mount 16-pin leadless chip carrier (LCC). Applications for the HMC5883L include Mobile Phones, Netbooks, Consumer Electronics, Auto Navigation Systems, and Personal Navigation Devices.



The HMC5883L utilizes Honeywell's Anisotropic Magnetoresistive (AMR) technology that provides advantages over other magnetic sensor technologies. These anisotropic, directional sensors feature precision in-axis sensitivity and linearity. These sensors' solid-state construction with very low cross-axis sensitivity is designed to measure both the direction and the magnitude of Earth's magnetic fields, from milli-gauss to 8 gauss. Honeywell's Magnetic Sensors are among the most sensitive and reliable low-field sensors in the industry.

FEATURES	BENEFITS
3-Axis Magnetoresistive Sensors and ASIC in a 3.0x3.0x0.9mm LCC Surface Mount Package	Small Size for Highly Integrated Products. Just Add a Micro-Controller Interface, Plus Two External SMT Capacitors Designed for High Volume, Cost Sensitive OEM Designs Easy to Assemble & Compatible with High Speed SMT Assembly
12-Bit ADC Coupled with Low Noise AMR Sensors Achieves 2 milli-gauss Field Resolution in ±8 Gauss Fields	Enables 1° to 2° Degree Compass Heading Accuracy
Built-In Self Test	Enables Low-Cost Functionality Test after Assembly in Production
Low Voltage Operations (2.16 to 3.6V) and Low Power Consumption (100 µA)	Compatible for Battery Powered Applications
Built-In Strap Drive Circuits	Set/Reset and Offset Strap Drivers for Degaussing, Self Test, and Offset Compensation
I^2C Digital Interface	Popular Two-Wire Serial Data Interface for Consumer Electronics
Lead Free Package Construction	RoHS Compliance
Wide Magnetic Field Range (+/-8 Oe)	Sensors Can Be Used in Strong Magnetic Field Environments with a 1° to 2° Degree Compass Heading Accuracy
Software and Algorithm Support Available	Compassing Heading, Hard Iron, Soft Iron, and Auto Calibration Libraries Available
Fast 160 Hz Maximum Output Rate	Enables Pedestrian Navigation and LBS Applications

SPECIFICATIONS (* Tested at 25°C except stated otherwise.)

Characteristics	Conditions*	Min	Typ	Max	Units
Power Supply					
Supply Voltage	VDD Referenced to AGND VDDIO Referenced to DGND	2.16 1.71	2.5 1.8	3.6 VDD+0.1	Volts Volts
Average Current Draw	Idle Mode Measurement Mode (7.5 Hz ODR; No measurement average, MA1:MA0 = 00) VDD = 2.5V, VDDIO = 1.8V (Dual Supply) VDD = VDDIO = 2.5V (Single Supply)	- -	2 100	- -	µA µA
Performance					
Field Range	Full scale (FS)	-8		+8	gauss
Mag Dynamic Range	3-bit gain control	±1		±8	gauss
Sensitivity (Gain)	VDD=3.0V, GN=0 to 7, 12-bit ADC	230		1370	LSb/gauss
Digital Resolution	VDD=3.0V, GN=0 to 7, 1-LSb, 12-bit ADC	0.73		4.35	milli-gauss
Noise Floor (Field Resolution)	VDD=3.0V, GN=0, No measurement average, Standard Deviation 100 samples (See typical performance graphs below)		2		milli-gauss
Linearity	±2.0 gauss input range			0.1	±% FS
Hysteresis	±2.0 gauss input range		±25		ppm
Cross-Axis Sensitivity	Test Conditions: Cross field = 0.5 gauss, Happlied = ±3 gauss		±0.2%		%FS/gauss
Output Rate (ODR)	Continuous Measurment Mode Single Measurement Mode	0.75		75 160	Hz Hz
Measurement Period	From receiving command to data ready		6		ms
Turn-on Time	Ready for I2C commands Analog Circuit Ready for Measurements		200 50		µs ms
Gain Tolerance	All gain/dynamic range settings		±5		%
I^2C Address	8-bit read address 8-bit write address		0x3D 0x3C		hex hex
I^2C Rate	Controlled by I^2C Master			400	kHz
I^2C Hysteresis	Hysteresis of Schmitt trigger inputs on SCL and SDA - Fall (VDDIO=1.8V) Rise (VDDIO=1.8V)		0.2*VDDIO 0.8*VDDIO		Volts Volts
Self Test	X & Y Axes Z Axis		±1.16 ±1.08		gauss
	X & Y & Z Axes (GN=5) Positive Bias X & Y & Z Axes (GN=5) Negative Bias	243 -575		575 -243	LSb
Sensitivity Tempco	T_A = -40 to 125°C, Uncompensated Output		-0.3		%/°C
General					
ESD Voltage	Human Body Model (all pins) Charged Device Model (all pins)			2000 750	Volts
Operating Temperature	Ambient	-30		85	°C
Storage Temperature	Ambient, unbiased	-40		125	°C

HMC5883L

Characteristics	Conditions*	Min	Typ	Max	Units
Reflow Classification	MSL 3, 260 °C Peak Temperature				
Package Size	Length and Width	2.85	3.00	3.15	mm
Package Height		0.8	0.9	1.0	mm
Package Weight			18		mg

Absolute Maximum Ratings (* Tested at 25°C except stated otherwise.)

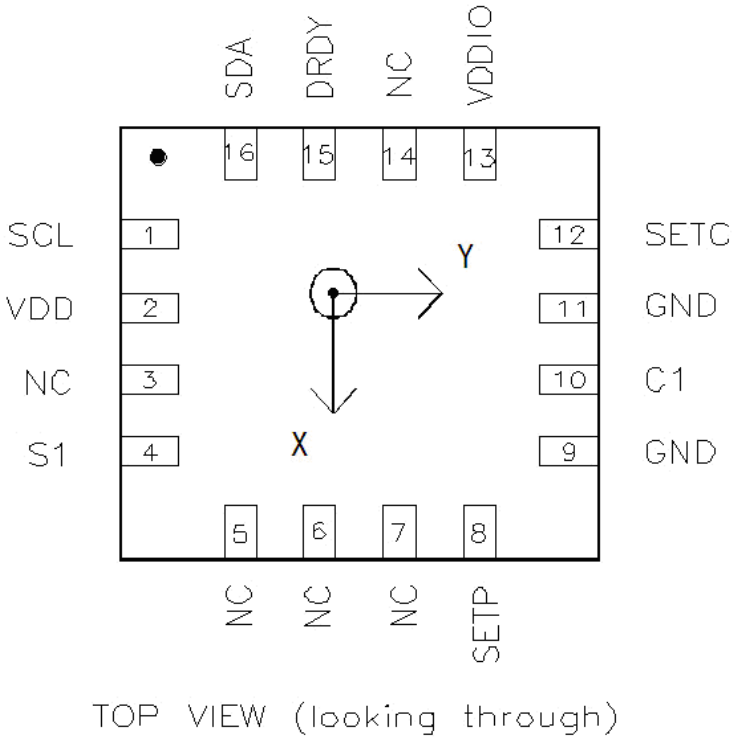
Characteristics	Min	Max	Units
Supply Voltage VDD	-0.3	4.8	Volts
Supply Voltage VDDIO	-0.3	4.8	Volts

PIN CONFIGURATIONS

Pin	Name	Description
1	SCL	Serial Clock – I^2C Master/Slave Clock
2	VDD	Power Supply (2.16V to 3.6V)
3	NC	Not to be Connected
4	S1	Tie to VDDIO
5	NC	Not to be Connected
6	NC	Not to be Connected
7	NC	Not to be Connected
8	SETP	Set/Reset Strap Positive – S/R Capacitor (C2) Connection
9	GND	Supply Ground
10	C1	Reservoir Capacitor (C1) Connection
11	GND	Supply Ground
12	SETC	S/R Capacitor (C2) Connection – Driver Side
13	VDDIO	IO Power Supply (1.71V to VDD)
14	NC	Not to be Connected
15	DRDY	Data Ready, Interrupt Pin. Internally pulled high. Optional connection. Low for 250 µsec when data is placed in the data output registers.
16	SDA	Serial Data – I^2C Master/Slave Data

Table 1: Pin Configurations

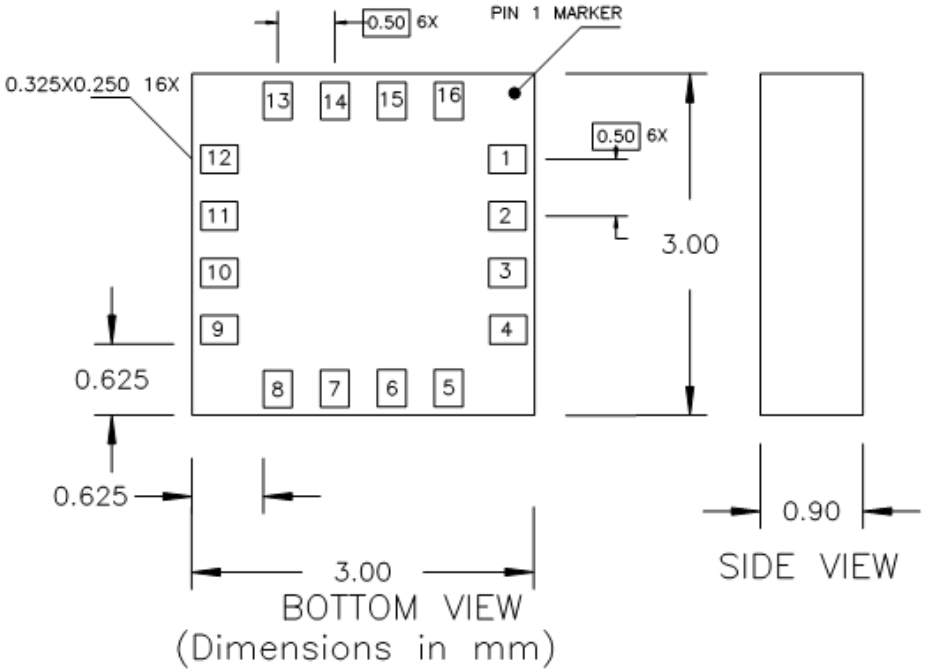
HMC5883L



Arrow indicates direction of magnetic field that generates a positive output reading in Normal Measurement configuration.

PACKAGE OUTLINES

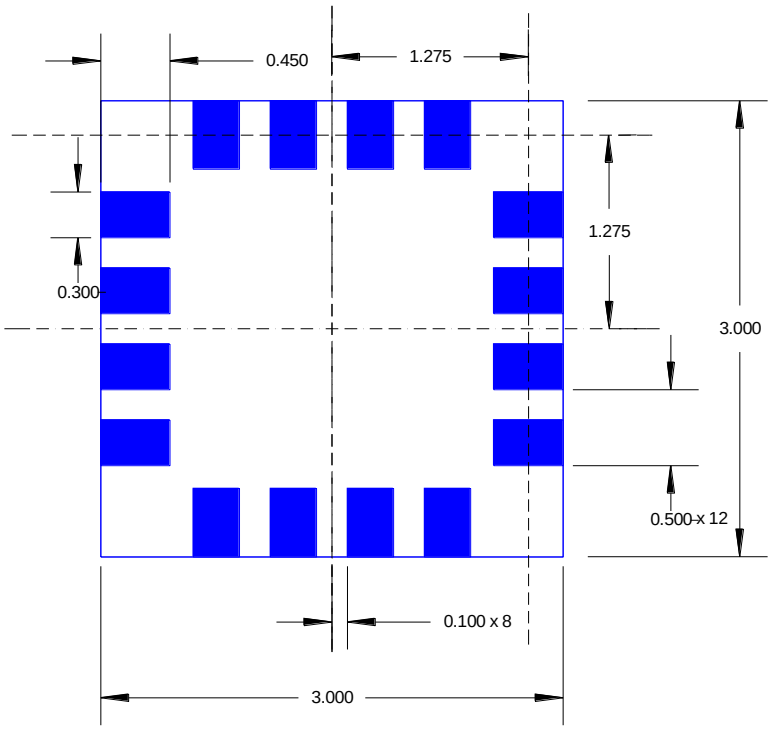
PACKAGE DRAWING HMC5883L (16-PIN LPCC, dimensions in millimeters)



MOUNTING CONSIDERATIONS

The following is the recommend printed circuit board (PCB) footprint for the HMC5883L.

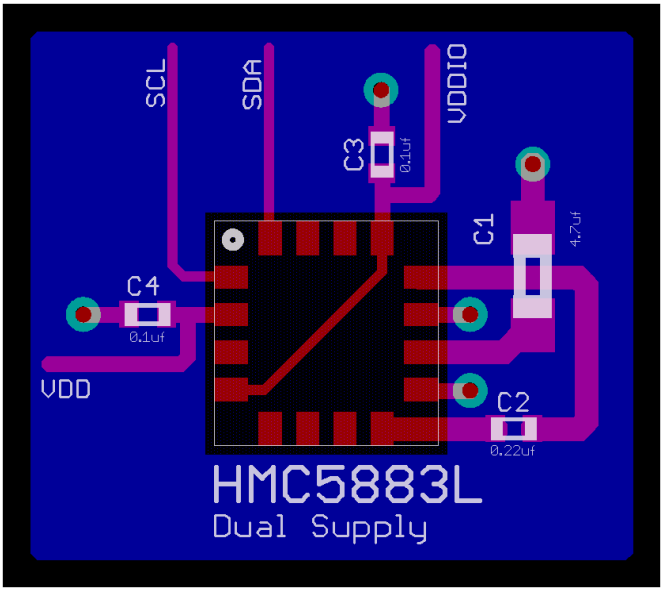
HMC5883L

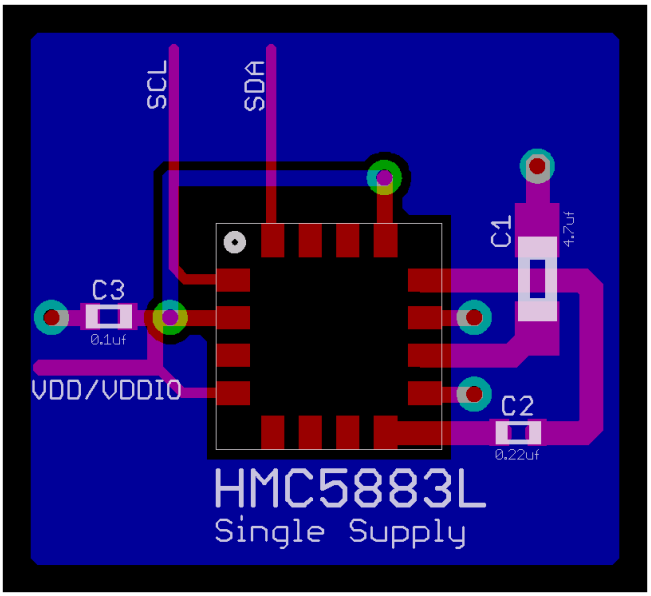


HMC5883 Land Pad Pattern
(All dimensions are in mm)

LAYOUT CONSIDERATIONS

Besides keeping all components that may contain ferrous materials (nickel, etc.) away from the sensor on both sides of the PCB, it is also recommended that there is no conducting copper under/near the sensor in any of the PCB layers. See recommended layout below. Notice that the one trace under the sensor in the dual supply mode is not expected to carry active current since it is for pin 4 pull-up to VDDIO. Power and ground planes are removed under the sensor to minimize possible source of magnetic noise. For best results, use non-ferrous materials for all exposed copper coding.





HMC5883L

PCB Pad Definition and Traces

The HMC5883L is a fine pitch LCC package. Refer to previous figure for recommended PCB footprint for proper package centering. Size the traces between the HMC5883L and the external capacitors (C1 and C2) to handle the 1 ampere peak current pulses with low voltage drop on the traces.

Stencil Design and Solder Paste

A 4 mil stencil and 100% paste coverage is recommended for the electrical contact pads.

Reflow Assembly

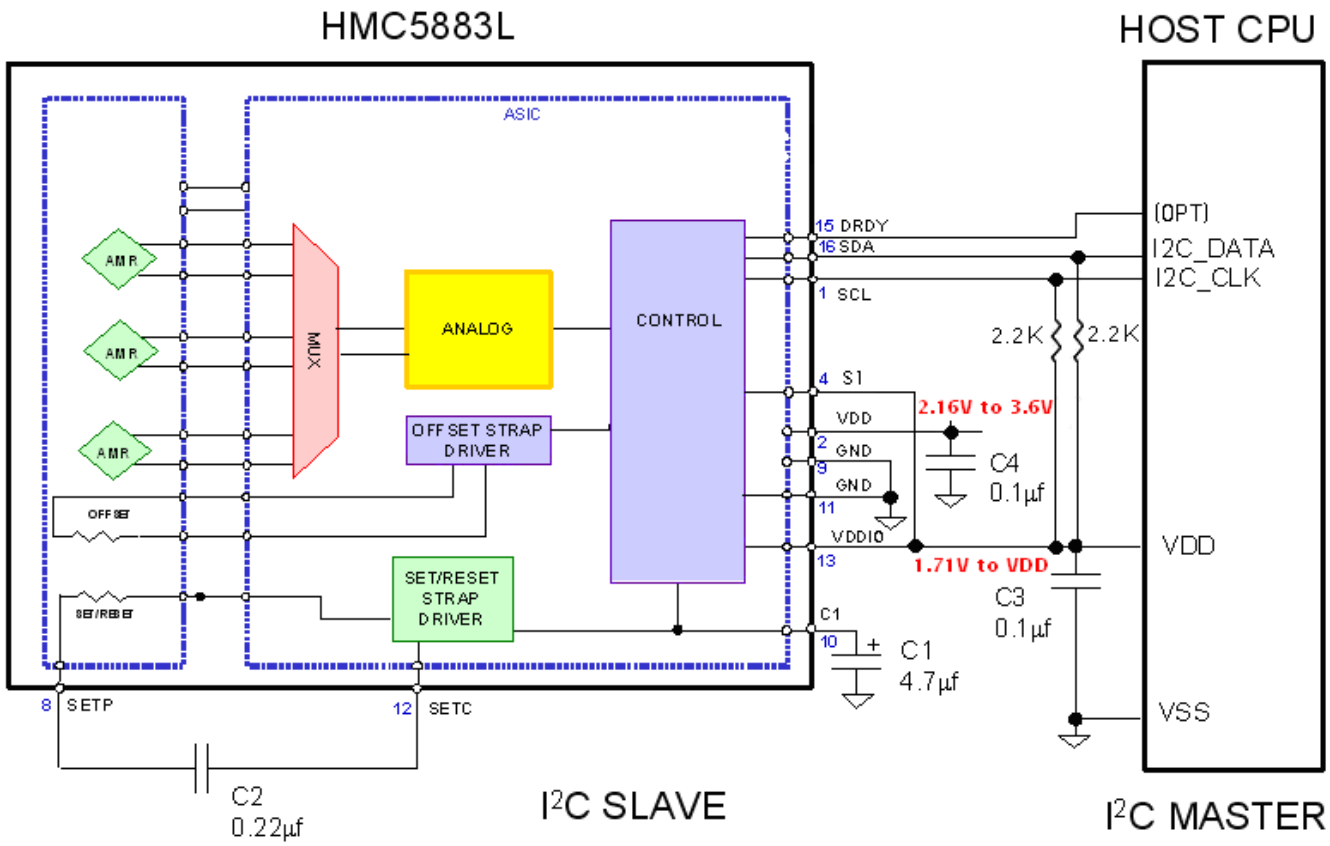
This device is classified as MSL 3 with 260°C peak reflow temperature. A baking process (125°C, 24 hrs) is required if device is not kept continuously in a dry (< 10% RH) environment before assembly. No special reflow profile is required for HMC5883L, which is compatible with lead eutectic and lead-free solder paste reflow profiles. Honeywell recommends adherence to solder paste manufacturer's guidelines. Hand soldering is not recommended. Built-in self test can be used to verify device functionalities after assembly.

External Capacitors

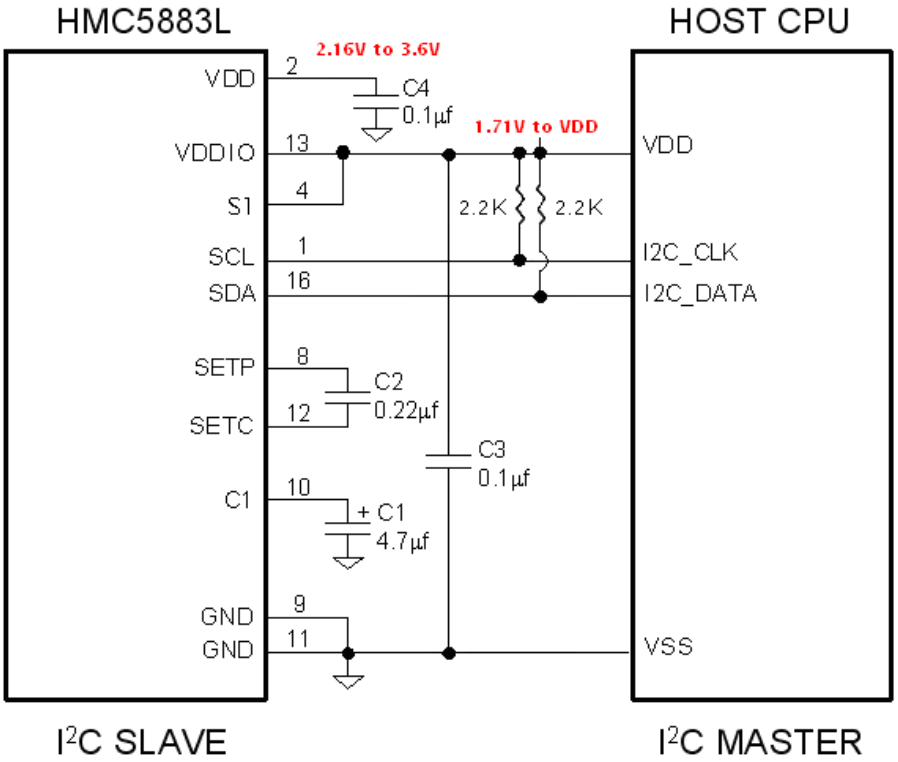
The two external capacitors should be ceramic type construction with low ESR characteristics. The exact ESR values are not critical but values less than 200 milli-ohms are recommended. Reservoir capacitor C1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C2 nominally 0.22 µF in capacitance. Low ESR characteristics may not be in many small SMT ceramic capacitors (0402), so be prepared to up-size the capacitors to gain Low ESR characteristics.

INTERNAL SCHEMATIC DIAGRAM

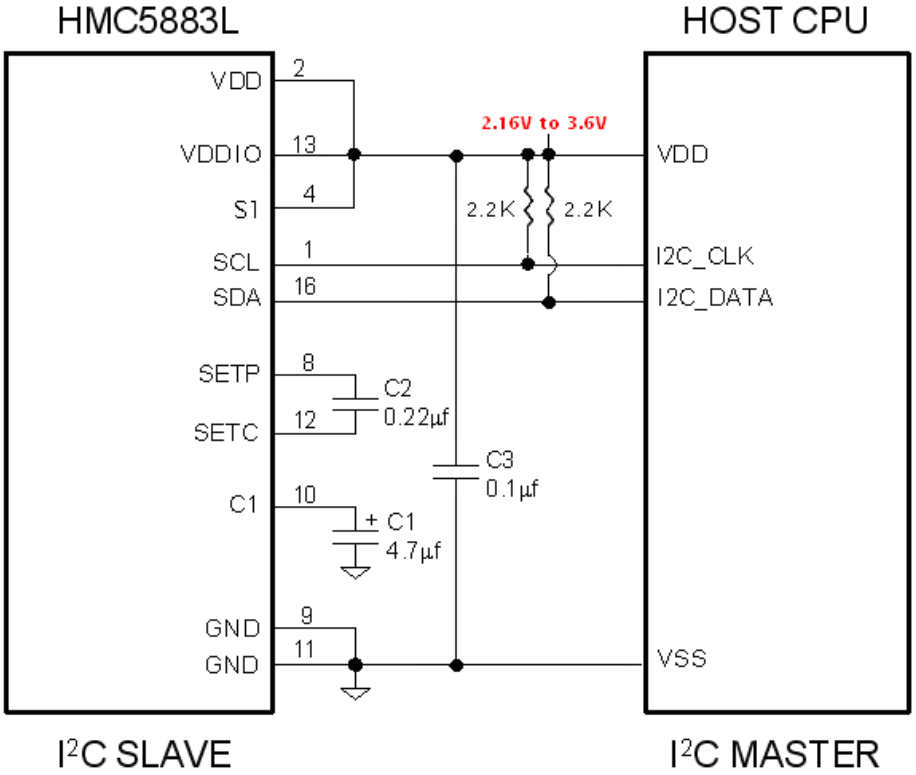
HMC5883L



DUAL SUPPLY REFERENCE DESIGN



SINGLE SUPPLY REFERENCE DESIGN

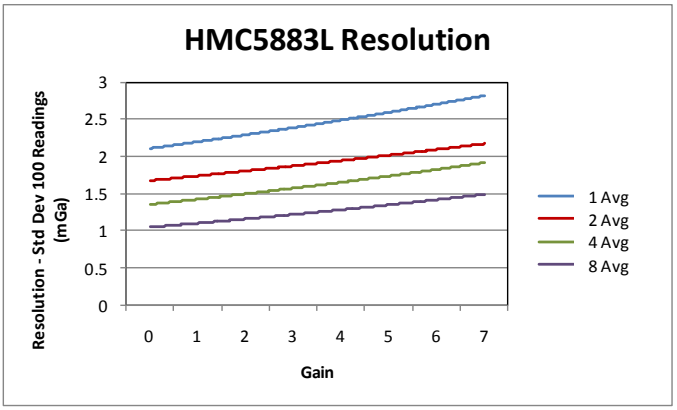


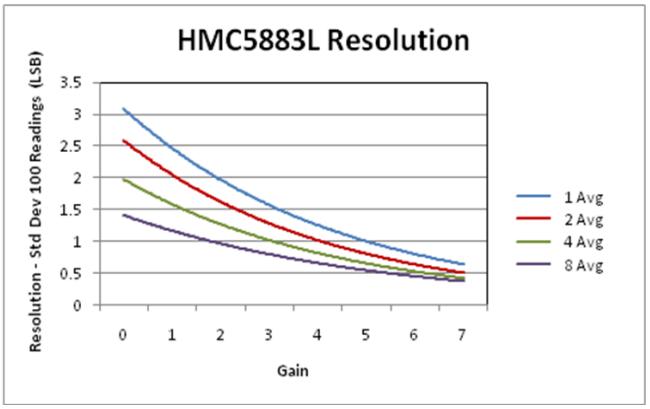
HMC5883L

PERFORMANCE

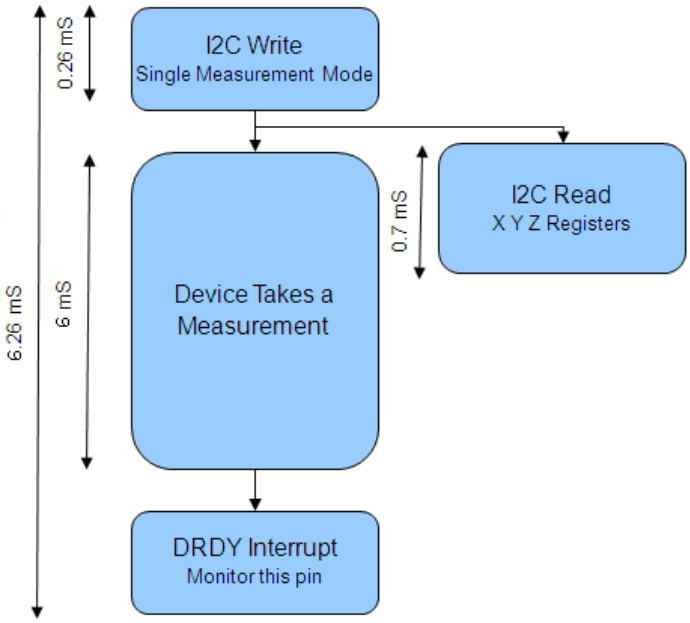
The following graph(s) highlight HMC5883L's performance.

Typical Noise Floor (Field Resolution)





Typical Measurement Period in Single-Measurement Mode



** Monitoring of the DRDY Interrupt pin is only required if maximum output rate is desired.*

BASIC DEVICE OPERATION

Anisotropic Magneto-Resistive Sensors

The Honeywell HMC5883L magnetoresistive sensor circuit is a trio of sensors and application specific support circuits to measure magnetic fields. With power supply applied, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output. The magnetoresistive sensors are made of a nickel-iron (Permalloy) thin-film and patterned as a resistive strip element. In the presence of a magnetic field, a change in the bridge resistive elements causes a corresponding change in voltage across the bridge outputs.

These resistive elements are aligned together to have a common sensitive axis (indicated by arrows in the pinout diagram) that will provide positive voltage change with magnetic fields increasing in the sensitive direction. Because the output is only proportional to the magnetic field component along its axis, additional sensor bridges are placed at orthogonal directions to permit accurate measurement of magnetic field in any orientation.

Self Test

To check the HMC5883L for proper operation, a self test feature in incorporated in which the sensor is internally excited with a nominal magnetic field (in either positive or negative bias configuration). This field is then measured and reported. This function is enabled and the polarity is set by bits MS[n] in the configuration register A. An internal current source generates DC current (about 10 mA) from the VDD supply. This DC current is applied to the offset straps of the magneto-resistive sensor, which creates an artificial magnetic field bias on the sensor. The difference of this measurement and the measurement of the ambient field will be put in the data output register for each of the three axes. By using this built-in function, the manufacturer can quickly verify the sensor's full functionality after the assembly without additional test setup. The self test results can also be used to estimate/compensate the sensor's sensitivity drift due to temperature.

For each "self test measurement", the ASIC:

1. Sends a "Set" pulse
2. Takes one measurement (M1)
3. Sends the (~10 mA) offset current to generate the (~1.1 Gauss) offset field and takes another measurement (M2)
4. Puts the difference of the two measurements in sensor's data output register:

   Output = [M2 – M1] (i.e. output = offset field only)

See SELF TEST OPERATION section later in this datasheet for additional details.

Power Management

This device has two different domains of power supply. The first one is VDD that is the power supply for internal operations and the second one is VDDIO that is dedicated to IO interface. It is possible to work with VDDIO equal to VDD; Single Supply mode, or with VDDIO lower than VDD allowing HMC5883L to be compatible with other devices on board.

I^2C Interface

Control of this device is carried out via the I^2C bus. This device will be connected to this bus as a slave device under the control of a master device, such as the processor.

This device is compliant with *I^2C-Bus Specification*, document number: 9398 393 40011. As an I^2C compatible device, this device has a 7-bit serial address and supports I^2C protocols. This device supports standard and fast modes, 100kHz and 400kHz, respectively, but does not support the high speed mode (Hs). External pull-up resistors are required to support these standard and fast speed modes.

Activities required by the master (register read and write) have priority over internal activities, such as the measurement. The purpose of this priority is to not keep the master waiting and the I^2C bus engaged for longer than necessary.

Internal Clock

The device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

H-Bridge for Set/Reset Strap Drive

The ASIC contains large switching FETs capable of delivering a large but brief pulse to the Set/Reset strap of the sensor. This strap is largely a resistive load. There is no need for an external Set/Reset circuit. The controlling of the Set/Reset function is done automatically by the ASIC for each measurement. One half of the difference from the measurements taken after a set pulse and after a reset pulse will be put in the data output register for each of the three axes. By doing so, the sensor's internal offset and its temperature dependence is removed/cancelled for all measurements. The set/reset pulses also effectively remove the past magnetic history (magnetism) in the sensor, if any.

For each "measurement", the ASIC:

1. Sends a "Set" pulse
2. Takes one measurement (Mset)
3. Sends a "Reset" pulse
4. Takes another measurement (Mreset)
5. Puts the following result in sensor's data output register:

Output = [Mset – Mreset] / 2

Charge Current Limit

The current that reservoir capacitor (C1) can draw when charging is limited for both single supply and dual supply configurations. This prevents drawing down the supply voltage (VDD).

MODES OF OPERATION

This device has several operating modes whose primary purpose is power management and is controlled by the Mode Register. This section describes these modes.

Continuous-Measurement Mode

During continuous-measurement mode, the device continuously makes measurements, at user selectable rate, and places measured data in data output registers. Data can be re-read from the data output registers if necessary; however, if the master does not ensure that the data register is accessed before the completion of the next measurement, the data output registers are updated with the new measurement. To conserve current between measurements, the device is placed in a state similar to idle mode, but the Mode Register is not changed to Idle Mode. That is, MD[n] bits are unchanged. Settings in the Configuration Register A affect the data output rate (bits DO[n]), the measurement configuration (bits MS[n]), when in continuous-measurement mode. All registers maintain values while in continuous-measurement mode. The I^2C bus is enabled for use by other devices on the network in while continuous-measurement mode.

Single-Measurement Mode

This is the default power-up mode. During single-measurement mode, the device makes a single measurement and places the measured data in data output registers. After the measurement is complete and output data registers are updated, the device is placed in idle mode, and the Mode Register *is* changed to idle mode by setting MD[n] bits. Settings in the configuration register affect the measurement configuration (bits MS[n])when in single-measurement mode. All registers maintain values while in single-measurement mode. The I^2C bus is enabled for use by other devices on the network while in single-measurement mode.

Idle Mode

During this mode the device is accessible through the I^2C bus, but major sources of power consumption are disabled, such as, but not limited to, the ADC, the amplifier, and the sensor bias current. All registers maintain values while in idle mode. The I^2C bus is enabled for use by other devices on the network while in idle mode.

HMC5883L

REGISTERS

This device is controlled and configured via a number of on-chip registers, which are described in this section. In the following descriptions, *set* implies a logic 1, and *reset* or *clear* implies a logic 0, unless stated otherwise.

Register List
The table below lists the registers and their access. All address locations are 8 bits.

Address Location	Name	Access
00	Configuration Register A	Read/Write
01	Configuration Register B	Read/Write
02	Mode Register	Read/Write
03	Data Output X MSB Register	Read
04	Data Output X LSB Register	Read
05	Data Output Z MSB Register	Read
06	Data Output Z LSB Register	Read
07	Data Output Y MSB Register	Read
08	Data Output Y LSB Register	Read
09	Status Register	Read
10	Identification Register A	Read
11	Identification Register B	Read
12	Identification Register C	Read

Table2: Register List

Register Access

This section describes the process of reading from and writing to this device. The devices uses an address pointer to indicate which register location is to be read from or written to. These pointer locations are sent from the master to this slave device and succeed the 7-bit address (0x1E) plus 1 bit read/write identifier, i.e. 0x3D for read and 0x3C for write.

To minimize the communication between the master and this device, the address pointer updated automatically without master intervention. The register pointer will be incremented by 1 automatically after the current register has been read successfully.

The address pointer value itself cannot be read via the I^2C bus.
Any attempt to read an invalid address location returns 0's, and any write to an invalid address location or an undefined bit within a valid address location is ignored by this device.

To move the address pointer to a random register location, first issue a "write" to that register location with no data byte following the commend. For example, to move the address pointer to register 10, send 0x3C 0x0A.

Configuration Register A

The configuration register is used to configure the device for setting the data output rate and measurement configuration. CRA0 through CRA7 indicate bit locations, with *CRA* denoting the bits that are in the configuration register. CRA7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.CRA default is 0x10.

CRA7	CRA6	CRA5	CRA4	CRA3	CRA2	CRA1	CRA0
(0)	MA1(0)	MA0(0)	DO2 (1)	DO1 (0)	DO0 (0)	MS1 (0)	MS0 (0)

Table 3: Configuration Register A

Location	Name	Description
CRA7	CRA7	Bit CRA7 is reserved for future function. Set to 0 when configuring CRA.
CRA6 to CRA5	MA1 to MA0	Select number of samples averaged (1 to 8) per measurement output. 00 = 1(Default); 01 = 2; 10 = 4; 11 = 8
CRA4 to CRA2	DO2 to DO0	Data Output Rate Bits. These bits set the rate at which data is written to all three data output registers.
CRA1 to CRA0	MS1 to MS0	Measurement Configuration Bits. These bits define the measurement flow of the device, specifically whether or not to incorporate an applied bias into the measurement.

Table 4: Configuration Register A Bit Designations

The Table below shows all selectable output rates in continuous measurement mode. All three channels shall be measured within a given output rate. Other output rates with maximum rate of 160 Hz can be achieved by monitoring DRDY interrupt pin in single measurement mode.

DO2	DO1	DO0	Typical Data Output Rate (Hz)
0	0	0	0.75
0	0	1	1.5
0	1	0	3
0	1	1	7.5
1	0	0	15 (Default)
1	0	1	30
1	1	0	75
1	1	1	Reserved

Table 5: Data Output Rates

MS1	MS0	Measurement Mode
0	0	Normal measurement configuration (Default). In normal measurement configuration the device follows normal measurement flow. The positive and negative pins of the resistive load are left floating and high impedance.
0	1	Positive bias configuration for X, Y, and Z axes. In this configuration, a positive current is forced across the resistive load for all three axes.
1	0	Negative bias configuration for X, Y and Z axes. In this configuration, a negative current is forced across the resistive load for all three axes..
1	1	This configuration is reserved.

Table 6: Measurement Modes

Configuration Register B

The configuration register B for setting the device gain. CRB0 through CRB7 indicate bit locations, with *CRB* denoting the bits that are in the configuration register. CRB7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit. CRB default is 0x20.

CRB7	CRB6	CRB5	CRB4	CRB3	CRB2	CRB1	CRB0
GN2 (0)	GN1 (0)	GN0 (1)	(0)	(0)	(0)	(0)	(0)

Table 7: Configuration B Register

Location	Name	Description
CRB7 to CRB5	GN2 to GN0	Gain Configuration Bits. These bits configure the gain for the device. The gain configuration is common for all channels.
CRB4 to CRB0	0	These bits must be cleared for correct operation.

Table 8: Configuration Register B Bit Designations

The table below shows nominal gain settings. Use the “Gain” column to convert counts to Gauss. The “Digital Resolution” column is the theoretical value in term of milli-Gauss per count (LSb) which is the inverse of the values in the “Gain” column. The effective resolution of the usable signal also depends on the noise floor of the system, i.e.

Effective Resolution = Max (Digital Resolution, Noise Floor)

Choose a lower gain value (higher GN#) when total field strength causes overflow in one of the data output registers (saturation). Note that the very first measurement after a gain change maintains the same gain as the previous setting. **The new gain setting is effective from the second measurement and on.**

GN2	GN1	GN0	Recommended Sensor Field Range	Gain (LSb/ Gauss)	Digital Resolution (mG/LSb)	Output Range
0	0	0	± 0.88 Ga	1370	0.73	0xF800–0x07FF (-2048–2047)
0	0	1	± 1.3 Ga	1090 (default)	0.92	0xF800–0x07FF (-2048–2047)
0	1	0	± 1.9 Ga	820	1.22	0xF800–0x07FF (-2048–2047)
0	1	1	± 2.5 Ga	660	1.52	0xF800–0x07FF (-2048–2047)
1	0	0	± 4.0 Ga	440	2.27	0xF800–0x07FF (-2048–2047)
1	0	1	± 4.7 Ga	390	2.56	0xF800–0x07FF (-2048–2047)
1	1	0	± 5.6 Ga	330	3.03	0xF800–0x07FF (-2048–2047)
1	1	1	± 8.1 Ga	230	4.35	0xF800–0x07FF (-2048–2047)

Table 9: Gain Settings

Mode Register

The mode register is an 8-bit register from which data can be read or to which data can be written. This register is used to select the operating mode of the device. MR0 through MR7 indicate bit locations, with *MR* denoting the bits that are in the mode register. MR7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit. Mode register default is 0x01.

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
(0)	(0)	(0)	(0)	(0)	(0)	MD1 (0)	MD0 (1)

Table 10: Mode Register

Location	Name	Description
MR7 to MR2	0	Bit MR7 is set to 1 internally after each single-measurement operation. Set to 0 when configuring mode register.
MR1 to MR0	MD1 to MD0	Mode Select Bits. These bits select the operation mode of this device.

Table 11: Mode Register Bit Designations

MD1	MD0	Operating Mode
0	0	Continuous-Measurement Mode. In continuous-measurement mode, the device continuously performs measurements and places the result in the data register. RDY goes high when new data is placed in all three registers. After a power-on or a write to the mode or configuration register, the first measurement set is available from all three data output registers after a period of $2/f_{DO}$ and subsequent measurements are available at a frequency of f_{DO}, where f_{DO} is the frequency of data output.
0	1	Single-Measurement Mode (Default). When single-measurement mode is selected, device performs a single measurement, sets RDY high and returned to idle mode. Mode register returns to idle mode bit values. The measurement remains in the data output register and RDY remains high until the data output register is read or another measurement is performed.
1	0	Idle Mode. Device is placed in idle mode.
1	1	Idle Mode. Device is placed in idle mode.

Table 12: Operating Modes

Data Output X Registers A and B

The data output X registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel X. Data output X register A contains the MSB from the measurement result, and data output X register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DXRA0 through DXRA7 and DXRB0 through DXRB7 indicate bit locations, with *DXRA* and *DXRB* denoting the bits that are in the data output X registers. DXRA7 and DXRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096. This register value will clear when after the next valid measurement is made.

DXRA7	**DXRA6**	**DXRA5**	**DXRA4**	**DXRA3**	**DXRA2**	**DXRA1**	**DXRA0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DXRB7	**DXRB6**	**DXRB5**	**DXRB4**	**DXRB3**	**DXRB2**	**DXRB1**	**DXRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 13: Data Output X Registers A and B

Data Output Y Registers A and B

The data output Y registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel Y. Data output Y register A contains the MSB from the measurement result, and data output Y register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DYRA0 through DYRA7 and DYRB0 through DYRB7 indicate bit locations, with *DYRA* and *DYRB* denoting the bits that are in the data output Y registers. DYRA7 and DYRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096. This register value will clear when after the next valid measurement is made.

DYRA7	**DYRA6**	**DYRA5**	**DYRA4**	**DYRA3**	**DYRA2**	**DYRA1**	**DYRA0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DYRB7	**DYRB6**	**DYRB5**	**DYRB4**	**DYRB3**	**DYRB2**	**DYRB1**	**DYRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 14: Data Output Y Registers A and B

Data Output Z Registers A and B

The data output Z registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel Z. Data output Z register A contains the MSB from the measurement result, and data output Z register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DZRA0 through DZRA7 and DZRB0 through DZRB7 indicate bit locations, with *DZRA* and *DZRB* denoting the bits that are in the data output Z registers. DZRA7 and DZRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096. This register value will clear when after the next valid measurement is made.

DZRA7	DZRA6	DZRA5	DZRA4	DZRA3	DZRA2	DZRA1	DZRA0
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DZRB7	**DZRB6**	**DZRB5**	**DZRB4**	**DZRB3**	**DZRB2**	**DZRB1**	**DZRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 15: Data Output Z Registers A and B

Data Output Register Operation

When one or more of the output registers are read, new data cannot be placed in any of the output data registers until all six data output registers are read. This requirement also impacts DRDY and RDY, which cannot be cleared until new data is placed in all the output registers.

Status Register

The status register is an 8-bit read-only register. This register is used to indicate device status. SR0 through SR7 indicate bit locations, with *SR* denoting the bits that are in the status register. SR7 denotes the first bit of the data stream.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
(0)	(0)	(0)	(0)	(0)	(0)	LOCK (0)	RDY(0)

Table 16: Status Register

Location	Name	Description
SR7 to SR2	0	These bits are reserved.
SR1	LOCK	Data output register lock. This bit is set when: 1.some but not all for of the six data output registers have been read, 2. Mode register has been read. When this bit is set, the six data output registers are locked and any new data will not be placed in these register until one of these conditions are met: 1.all six bytes have been read, 2. the mode register is changed, 3. the measurement configuration (CRA) is changed, 4. power is reset.
SR0	RDY	Ready Bit. Set when data is written to all six data registers. Cleared when device initiates a write to the data output registers and after one or more of the data output registers are written to. When RDY bit is clear it shall remain cleared for a 250 µs. DRDY pin can be used as an alternative to the status register for monitoring the device for measurement data.

Table 17: Status Register Bit Designations

Identification Register A

The identification register A is used to identify the device. IRA0 through IRA7 indicate bit locations, with *IRA* denoting the bits that are in the identification register A. IRA7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

The identification value for this device is stored in this register. This is a read-only register.
Register values. ASCII value *H*

IRA7	IRA6	IRA5	IRA4	IRA3	IRA2	IRA1	IRA0
0	1	0	0	1	0	0	0

Table 18: Identification Register A Default Values

Identification Register B

The identification register B is used to identify the device. IRB0 through IRB7 indicate bit locations, with *IRB* denoting the bits that are in the identification register A. IRB7 denotes the first bit of the data stream.

Register values. ASCII value *4*

IRB7	IRB6	IRB5	IRB4	IRB3	IRB2	IRB1	IRB0
0	0	1	1	0	1	0	0

Table 19: Identification Register B Default Values

Identification Register C

The identification register C is used to identify the device. IRC0 through IRC7 indicate bit locations, with *IRC* denoting the bits that are in the identification register A. IRC7 denotes the first bit of the data stream.

Register values. ASCII value *3*

IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0
0	0	1	1	0	0	1	1

Table 20: Identification Register C Default Values

I^2C COMMUNICATION PROTOCOL

The HMC5883L communicates via a two-wire I^2C bus system as a slave device. The HMC5883L uses a simple protocol with the interface protocol defined by the I^2C bus specification, and by this document. The data rate is at the standard-mode 100kbps or 400kbps rates as defined in the I^2C Bus Specifications. The bus bit format is an 8-bit Data/Address send and a 1-bit acknowledge bit. The format of the data bytes (payload) shall be case sensitive ASCII characters or binary data to the HMC5883L slave, and binary data returned. Negative binary values will be in two's complement form. The default (factory) HMC5883L 8-bit slave address is 0x3C for write operations, or 0x3D for read operations.

The HMC5883L Serial Clock (SCL) and Serial Data (SDA) lines require resistive pull-ups (Rp) between the master device (usually a host microprocessor) and the HMC5883L. Pull-up resistance values of about 2.2K to 10K ohms are recommended with a nominal VDDIO voltage. Other resistor values may be used as defined in the I^2C Bus Specifications that can be tied to VDDIO.

The SCL and SDA lines in this bus specification may be connected to multiple devices. The bus can be a single master to multiple slaves, or it can be a multiple master configuration. All data transfers are initiated by the master device, which is responsible for generating the clock signal, and the data transfers are 8 bit long. All devices are addressed by I^2C's unique 7-bit address. After each 8-bit transfer, the master device generates a 9th clock pulse, and releases the SDA line. The receiving device (addressed slave) will pull the SDA line low to acknowledge (ACK) the successful transfer or leave the SDA high to negative acknowledge (NACK).

Per the I^2C spec, all transitions in the SDA line must occur when SCL is low. This requirement leads to two unique conditions on the bus associated with the SDA transitions when SCL is high. Master device pulling the SDA line low while the SCL line is high indicates the Start (S) condition, and the Stop (P) condition is when the SDA line is pulled high while the SCL line is high. The I^2C protocol also allows for the Restart condition in which the master device issues a second start condition without issuing a stop.

All bus transactions begin with the master device issuing the start sequence followed by the slave address byte. The address byte contains the slave address; the upper 7 bits (bits7-1), and the Least Significant bit (LSb). The LSb of the address byte designates if the operation is a read (LSb=1) or a write (LSb=0). At the 9th clock pulse, the receiving slave device will issue the ACK (or NACK). Following these bus events, the master will send data bytes for a write operation, or the slave will clock out data with a read operation. All bus transactions are terminated with the master issuing a stop sequence.

I^2C bus control can be implemented with either hardware logic or in software. Typical hardware designs will release the SDA and SCL lines as appropriate to allow the slave device to manipulate these lines. In a software implementation, care must be taken to perform these tasks in code.

OPERATIONAL EXAMPLES

The HMC5883L has a fairly quick stabilization time from no voltage to stable and ready for data retrieval. The nominal 56 milli-seconds with the factory default single measurement mode means that the six bytes of magnetic data registers (DXRA, DXRB, DZRA, DZRB, DYRA, and DYRB) are filled with a valid first measurement.

To change the measurement mode to continuous measurement mode, after the power-up time send the three bytes:

0x3C 0x02 0x00

This writes the 00 into the second register or mode register to switch from single to continuous measurement mode setting. With the data rate at the factory default of 15Hz updates, a 67 milli-second typical delay should be allowed by the I^2C master before querying the HMC5883L data registers for new measurements. To clock out the new data, send:

0x3D, and clock out DXRA, DXRB, DZRA, DZRB, DYRA, and DYRB located in registers 3 through 8. The HMC5883L will automatically re-point back to register 3 for the next 0x3D query. All six data registers must be read properly before new data can be placed in any of these data registers.

Below is an example of a (power-on) initialization process for “continuous-measurement mode”:

1. Write CRA (00) – send **0x3C 0x00 0x70** (8-average, 15 Hz default, normal measurement)
2. Write CRB (01) – send **0x3C 0x01 0xA0** (Gain=5, or any other desired gain)
3. Write Mode (02) – send **0x3C 0x02 0x00** (Continuous-measurement mode)
4. Wait 6 ms or monitor status register or DRDY hardware interrupt pin
5. Loop
   Send **0x3D 0x06** (Read all 6 bytes. If gain is changed then this data set is using previous gain)
   Convert three 16-bit 2’s compliment hex values to decimal values and assign to X, Z, Y, respectively.
   Send **0x3C 0x03** (point to first data register 03)
   Wait about 67 ms (if 15 Hz rate) or monitor status register or DRDY hardware interrupt pin
   End_loop

Below is an example of a (power-on) initialization process for “single-measurement mode”:

1. Write CRA (00) – send **0x3C 0x00 0x70** (8-average, 15 Hz default or any other rate, normal measurement)
2. Write CRB (01) – send **0x3C 0x01 0xA0** (Gain=5, or any other desired gain)
3. For each measurement query:
   Write Mode (02) – send **0x3C 0x02 0x01** (Single-measurement mode)
   Wait 6 ms or monitor status register or DRDY hardware interrupt pin
   Send **0x3D 0x06** (Read all 6 bytes. If gain is changed then this data set is using previous gain)
   Convert three 16-bit 2’s compliment hex values to decimal values and assign to X, Z, Y, respectively.

HMC5883L

SELF TEST OPERATION

To check the HMC5883L for proper operation, a self test feature in incorporated in which the sensor offset straps are excited to create a nominal field strength (bias field) to be measured. To implement self test, the least significant bits (MS1 and MS0) of configuration register A are changed from 00 to 01 (positive bias) or 10 (negetive bias).

Then, by placing the mode register into single or continuous-measurement mode, two data acquisition cycles will be made on each magnetic vector. The first acquisition will be a set pulse followed shortly by measurement data of the external field. The second acquisition will have the offset strap excited (about 10 mA) in the positive bias mode for X, Y, and Z axes to create about a 1.1 gauss self test field plus the external field. The first acquisition values will be subtracted from the second acquisition, and the net measurement will be placed into the data output registers.

Since self test adds ~1.1 Gauss additional field to the existing field strength, using a reduced gain setting prevents sensor from being saturated and data registers overflowed. For example, if the configuration register B is set to 0xA0 (Gain=5), values around +452 LSb (1.16 Ga * 390 LSb/Ga) will be placed in the X and Y data output registers and around +421 (1.08 Ga * 390 LSb/Ga) will be placed in Z data output register. To leave the self test mode, change MS1 and MS0 bit of the configuration register A back to 00 (Normal Measurement Mode). Acceptable limits of the self test values depend on the gain setting. Limits for Gain=5 is provided in the specification table.

Below is an example of a “positive self test” process using continuous-measurement mode:

1. Write CRA (00) – send **0x3C 0x00 0x71** (8-average, 15 Hz default, positive self test measurement)
2. Write CRB (01) – send **0x3C 0x01 0xA0** (Gain=5)
3. Write Mode (02) – send **0x3C 0x02 0x00** (Continuous-measurement mode)
4. Wait 6 ms or monitor status register or DRDY hardware interrupt pin
5. Loop
    Send **0x3D 0x06** (Read all 6 bytes. If gain is changed then this data set is using previous gain)
    Convert three 16-bit 2’s compliment hex values to decimal values and assign to X, Z, Y, respectively.
    Send **0x3C 0x03** (point to first data register 03)
    Wait about 67 ms (if 15 Hz rate) or monitor status register or DRDY hardware interrupt pin
    End_loop
6. Check limits –
    If all 3 axes (X, Y, and Z) are within reasonable limits (243 to 575 for Gain=5, adjust these limits basing on the gain setting used. See an example below.) Then
        All 3 axes pass positive self test
        Write CRA (00) – send **0x3C 0x00 0x70** (Exit self test mode and this procedure)
    Else
        If Gain<7
            Write CRB (01) – send **0x3C 0x01 0x_0** (Increase gain setting and retry, skip the next data set)
        Else
            At least one axis did not pass positive self test
            Write CRA (00) – send **0x3C 0x00 0x70** (Exit self test mode and this procedure)
    End If

Below is an example of how to adjust the “positive self” test limits basing on the gain setting:

1. If Gain = 6, self test limits are:
    Low Limit = 243 * 330/390 = 206
    High Limit = 575 * 330/390 = 487

2. If Gain = 7, self test limits are:
    Low Limit = 243 * 230/390 = 143
    High Limit = 575 * 230/390 = 339

HMC5883L

SCALE FACTOR TEMPERATURE COMPENSATION

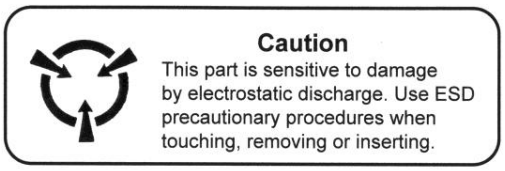
The built-in self test can also be used to periodically compensate the scaling errors due to temperature variations. A compensation factor can be found by comparing the self test outputs with the ones obtained at a known temperature. For example, if the self test output is 400 at room temperature and 300 at the current temperature then a compensation factor of (400/300) should be applied to all current magnetic readings. A temperature sensor is not required using this method.

Below is an example of a temperature compensation process using positive self test method:

1. If self test measurement at a temperature “when the last magnetic calibration was done”:
   X_STP = 400
   Y_STP = 410
   Z_STP = 420
2. If self test measurement at a different tmperature:
   X_STP = 300 (Lower than before)
   Y_STP = 310 (Lower than before)
   Z_STP = 320 (Lower than before)
   Then
   X_TempComp = 400/300
   Y_TempComp = 410/310
   Z_TempComp = 420/320
3. Applying to all new measurements:
   X = X * X_TempComp
   Y = Y * Y_TempComp
   Z = Z * Z_TempComp
   Now all 3 axes are temperature compensated, i.e. sensitivity is same as “when the last magnetic calibration was done”; therefore, the calibration coefficients can be applied without modification.
4. Repeat this process periodically or,for every Δt degrees of temperature change measured, if available.

ORDERING INFORMATION

Ordering Number	Product
HMC5883L-TR	Tape and Reel 4k pieces/reel



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Appendix B

Data Sheets of the x-IMU sensors

IMU-3000
Motion Processing Unit
Product Specification
Rev 1.1

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1 Document Information

1.1 Revision History

Revision Date	Revision	Description
05/26/2010	1.0	Initial Release
08/19/2010	1.1	• Changes for readability (multiple sections) • Modified following specifications (Section 3.1) o ZRO Tolerance o ZRO Variation over Temperature o Total RMS Noise o Noise spectral density o Temperature Sensor Operating Range • Modified following specifications (Section 3.2) o Operating Current o Digital Input: Input Capacitance • Modified Capacitance for each IO Pin for Secondary I^2C (Section 3.3) • Modified Clock Frequency Initial Tolerance for CLKSEL=0, 25°C (Section 3.4). • Modified I^2C Timing: Capacitive Load for Each Bus Line (Section 3.5) • Added Latch-up specification (Section 3.6). • Modified 3rd party accel /CS connection in diagram. (Section 7.3.1) • Added AUX register listing (Section 9). • Added AUX register description (Section 10.12). • Modified PCB Design Guidelines (Section 11.2.2). • Modified Reflow Specification (Section 11.9) • Added Environmental Compliance information (Section 13).

1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information for the IMU-3000™ Inertial Measurement Unit (IMU™). The IMU-3000 MPL Functional Specification describes in detail the Motion Processing Library: API and System Layer routines needed for interfacing to the IMU-3000.

Electrical characteristics are based upon simulation results and limited characterization data of advanced samples only. Specifications are subject to change without notice. Final specifications will be updated based upon characterization of final silicon.

1.3 Product Overview

The IMU-3000 is the world's first IMU solution with 6-axis sensor fusion for consumer applications. The IMU-3000 has an embedded 3-axis gyroscope and Digital Motion Processor™ (DMP™) hardware accelerator engine with a secondary I^2C port that interfaces to third party digital accelerometers to deliver a complete 6-axis sensor fusion output to its primary I^2C port. This combines both linear and rotational motion into a single data stream for the application. The device is ideally suited for a wide variety of consumer products requiring a rugged, low-cost motion processing solution for applications in game controllers, remote controls for broadband connected TVs and set top boxes, sports, fitness, medical and other applications. By providing an integrated sensor fusion output, the IMU-3000 offloads the intensive motion processing computation requirements from the host processor, reducing the need for frequent polling of the motion sensor output and enabling use of low cost, low power microcontrollers.

The IMU-3000 features a 3-axis digital gyro with programmable full-scale ranges of ±250, ±500, ±1000, and ±2000 degrees/sec (dps), which is useful for precision tracking of both fast and slow motions. Rate noise performance sets the industry standard at 0.01 dps/√Hz, providing the highest-quality user experience in pointing and gaming applications. Factory-calibrated initial sensitivity reduces production-line calibration requirements. The part's on-chip FIFO and dedicated I^2C-master accelerometer sensor bus simplify system timing and lower system power consumption; the sensor bus allows the IMU-3000 to directly acquire data from the off-chip accelerometer without intervention from an external processor, while the FIFO allows a system microcontrollers to burst read the sensor data and then go to sleep while the IMU collects more data. Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, a precision clock with 1% variation from -40°C to 85°C, an embedded temperature sensor, programmable interrupts, and a low 13mW power consumption. Parts are available with an I^2C serial interface, a VDD operating range of 2.1 to 3.6V, and a VLOGIC interface voltage from 1.71V to 3.6V.

By leveraging its patented and volume-proven Nasiri-Fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the IMU-3000 package size down to a revolutionary footprint of 4x4x0.9mm (QFN), while providing the highest performance, lowest noise, and the lowest cost semiconductor packaging to address a wide range of handheld consumer electronic devices. The device provides the highest robustness by supporting 10,000*g* shock in operation. The highest cross-axis isolation is achieved by design from its single silicon integration.

The IMU-3000 was designed to connect directly with a third-party 3-axis digital accelerometer, which slaves directly to the IMU-3000 master and can be clocked from the internal phase locked loop of the IMU-3000 device, providing highly accurate timing for a true 6-axis motion processing solution previously only available in costly and bulky inertial measurement units.

1.4 Applications

- Game controllers
- 3D Remote controls for Internet connected TVs and Set Top Boxes
- Health and sports monitoring
- Motion tracking
- Gesture recognition and advanced user interfaces

2 Features

The IMU-3000 Motion Processing Unit includes a wide range of features:

2.1 Sensors

- X-, Y-, Z-Axis angular rate sensors (gyros) on one integrated circuit
- Digital-output temperature sensor
- 6-axis motion processing capability using secondary I^2C interface to directly connect to a digital 3-axis third-party accelerometer
- Factory-calibrated scale factor
- High cross-axis isolation via proprietary MEMS design
- 10,000*g* shock tolerant

2.2 Digital Output

- Fast Mode (400kHz) I^2C serial interface
- 16-bit ADCs for digitizing sensor outputs
- Angular rate sensors (gyros) with applications-programmable full-scale-range of ±250°/sec, ±500°/sec, ±1000°/sec, or ±2000°/sec.

2.3 Motion Processing

- Embedded Digital Motion Processing™ (DMP™) engine supports 3D motion processing. When used together with a digital 3-axis third party accelerometer, the IMU-3000 collects the accelerometer data via a dedicated interface, while synchronizing data sampling at a user defined rate. The total data set obtained by the IMU-3000 includes 3-axis gyroscope data, 3-axis accelerometer data, and temperature data.
- FIFO buffers complete data set, reducing timing requirements on the system processor and saving power by letting the processor burst read the FIFO data, and then go into a low-power sleep mode while the IMU collects more data.
- Data collection polled or interrupt driven with on-chip programmable interrupt functionality
- Programmable low-pass filters

2.4 Clocking

- On-chip timing generator clock frequency ±2% variation over full temperature range
- Optional external clock inputs of 32.768kHz or 19.2MHz
- 1MHz clock output to synchronize with digital 3-axis accelerometer

2.5 Power

- VDD analog supply voltage range of 2.1V to 3.6V
- Flexible VLOGIC reference voltage allows for I^2C interface voltages from 1.71V to VDD
- Power consumption with all three axis active: 6.1mA
- Sleep mode: 5µA
- Each axis can be individually powered down

2.6 Package

- 4x4x0.9mm QFN plastic package
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 Electrical Characteristics

3.1 Sensor Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V, T_A=25°C.

Parameter	Conditions	Min	Typical	Max	Unit	Notes
GYRO SENSITIVITY						
Full-Scale Range	FS_SEL=0		±250		º/s	4
	FS_SEL=1		±500			4
	FS_SEL=2		±1000			4
	FS_SEL=3		±2000			4
Gyro ADC Word Length			16		Bits	3
Sensitivity Scale Factor	FS_SEL=0		131		LSB/(º/s)	1
	FS_SEL=1		65.5			3
	FS_SEL=2		32.8			3
	FS_SEL=3		16.4			3
Sensitivity Scale Factor Tolerance	25°C	-3		+3	%	1
Sensitivity Scale Factor Variation Over Temperature			±2		%	7
Nonlinearity	Best fit straight line; 25°C		0.2		%	6
Cross-Axis Sensitivity			2		%	6
GYRO ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±20		º/s	1
ZRO Variation Over Temperature	-40°C to +85°C		±0.1		º/s/ºC	7
Power-Supply Sensitivity (1-10Hz)	Sine wave, 100mVpp; VDD=2.2V		0.2		º/s	5
Power-Supply Sensitivity (10 - 250Hz)	Sine wave, 100mVpp; VDD=2.2V		0.2		º/s	5
Power-Supply Sensitivity (250Hz - 100kHz)	Sine wave, 100mVpp; VDD=2.2V		4		º/s	5
Linear Acceleration Sensitivity	Static		0.1		º/s/*g*	6
GYRO NOISE PERFORMANCE	**FS_SEL=0**					
Total RMS Noise	DLPFCFG=2 (100Hz)		0.1		º/s-rms	1
Rate Noise Spectral Density	At 10Hz		0.01		º/s/√Hz	3
GYRO MECHANICAL FREQUENCIES						
X-Axis		30	33	36	kHz	1
Y-Axis		27	30	33	kHz	1
Z-Axis		24	27	30	kHz	1
GYRO START-UP TIME	**DLPFCFG=0**					
ZRO Settling	to ±1º/s of Final		50		ms	5
TEMPERATURE SENSOR						
Range			-30 to 85		ºC	2
Sensitivity	Untrimmed		280		LSB/ºC	2
Room-Temperature Offset	35ºC		-13200		LSB	1
Linearity	Best fit straight line (-30°C to +85°C)		±1		°C	2
TEMPERATURE RANGE						
Specified Temperature Range		-40		85	ºC	2

Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Based on design, through modeling and simulation across PVT
4. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
5. Based on characterization of 5 parts over temperature
6. Tested on 5 parts at room temperature
7. Based on characterization of 48 parts on evaluation board or in socket

3.2 Electrical Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, T_A = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
VDD POWER SUPPLY						
Operating Voltage Range		2.1		3.6	V	2
Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value (see Figure in Section 4.4)	0		5	ms	2
Normal Operating Current			6.1		mA	1
	DMP disabled		5.9		mA	1
Sleep Mode Current			5		µA	4
VLOGIC REFERENCE VOLTAGE						
(Must be regulated)						
Voltage Range	VLOGIC must be ≤VDD at all times	1.71		VDD	V	
Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value (see Figure in Section 4.4)			1	ms	3, 5
Normal Operating Current			100		µA	
START-UP TIME FOR REGISTER READ/WRITE			20	100	ms	4
I^2C ADDRESS						
	AD0 = 0		1101000			1
	AD0 = 1		1101001			1
DIGITAL INPUTS (AD0, CLKIN)						
V_{IH}, High Level Input Voltage		0.7*VDD			V	5
V_{IL}, Low Level Input Voltage				0.3*VDD	V	5
C_I, Input Capacitance			< 5		pF	
DIGITAL OUTPUT (INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ	0.9*VLOGIC			V	2
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ			0.1*VLOGIC	V	2
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink current			0.1	V	2
Output Leakage Current	OPEN=1		100		nA	4
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	4

Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
4. Based on characterization of 5 parts over temperature
5. Refer to Section 4.4 for the recommended power-on procedure

3.3 Electrical Specifications, continued

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V, T_A=25°C.

Parameters	Conditions	Typical	Units	Notes
Primary I^2C I/O (SCL, SDA)				
V_{IL}, LOW-Level Input Voltage		-0.5V to 0.3*VLOGIC	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VLOGIC to VLOGIC + 0.5V	V	1
V_{hys}, Hysteresis		0.1*VLOGIC	V	1
V_{OL1}, LOW-Level Output Voltage	3mA sink current	0 to 0.4	V	1
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V	3	mA	1
	V_{OL} = 0.6V	5	mA	1
Output Leakage Current		100	nA	2
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1Cb to 250	ns	1
C_I, Capacitance for Each I/O pin		< 10	pF	
Secondary I^2C I/O (AUX_CL, AUX_DA)	**AUX_VDDIO=0**			
V_{IL}, LOW-Level Input Voltage		-0.5V to 0.3*VLOGIC	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VLOGIC to VLOGIC + 0.5V	V	
V_{hys}, Hysteresis		0.1*VLOGIC	V	
V_{OL1}, LOW-Level Output Voltage	VLOGIC > 2V; 1mA sink current	0 to 0.4	V	1
V_{OL3}, LOW-Level Output Voltage	VLOGIC < 2V; 1mA sink current	0 to 0.2*VLOGIC	V	1
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V	1	mA	1
	V_{OL} = 0.6V	1	mA	1
Output Leakage Current		100	nA	2
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1Cb to 250	ns	1
C_I, Capacitance for Each I/O pin		< 10	pF	
Secondary I^2C I/O (AUX_CL, AUX_DA)	**AUX_VDDIO=1**			
V_{IL}, LOW-Level Input Voltage		-0.5 to 0.3*VDD	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDD to VDD+0.5V	V	1
V_{hys}, Hysteresis		0.1*VDD	V	
V_{OL1}, LOW-Level Output Voltage	1mA sink current	0 to 0.4	V	1
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V	1	mA	1
	V_{OL} = 0.6V	1	mA	1
Output Leakage Current		100	nA	2
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1Cb to 250	ns	1
C_I, Capacitance for Each I/O pin		< 10	pF	

Notes:

1. Based on characterization of 5 parts over temperature
2. Typical. Randomly selected part measured at room temperature on evaluation board or in socket

3.4 Electrical Specifications, continued

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V, T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
INTERNAL CLOCK SOURCE	**CLKSEL=0,1,2,3**					
Sample Rate, Fast	DLPFCFG=0 SAMPLERATEDIV = 0		8		kHz	3
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1		kHz	3
Reference Clock Output	CLKOUTEN = 1		1.024		MHz	3
Clock Frequency Initial Tolerance	CLKSEL=0, 25°C	-5		+5	%	1
	CLKSEL=1,2,3; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLKSEL=0		-15 to +10		%	2
	CLKSEL=1,2,3		±1		%	2
PLL Settling Time	CLKSEL=1,2,3		1		ms	
EXTERNAL 32.768kHz CLOCK	**CLKSEL=4**					
External Clock Frequency			32.768		kHz	
External Clock Jitter	Cycle-to-cycle rms		1 to 2		µs	
Sample Rate, Fast	DLPFCFG=0 SAMPLERATEDIV = 0		8.192		kHz	
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1.024		kHz	
Reference Clock Output	CLKOUTEN = 1		1.0486		MHz	
PLL Settling Time			1		ms	
EXTERNAL 19.2MHz CLOCK	**CLKSEL=5**					
External Clock Frequency			19.2		MHz	
Sample Rate, Fast	DLPFCFG=0 SAMPLERATEDIV = 0		8		kHz	
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1		kHz	
Reference Clock Output	CLKOUTEN = 1		1.024		MHz	
PLL Settling Time			1		ms	

Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Typical. Randomly selected part measured at room temperature on evaluation board or in socket

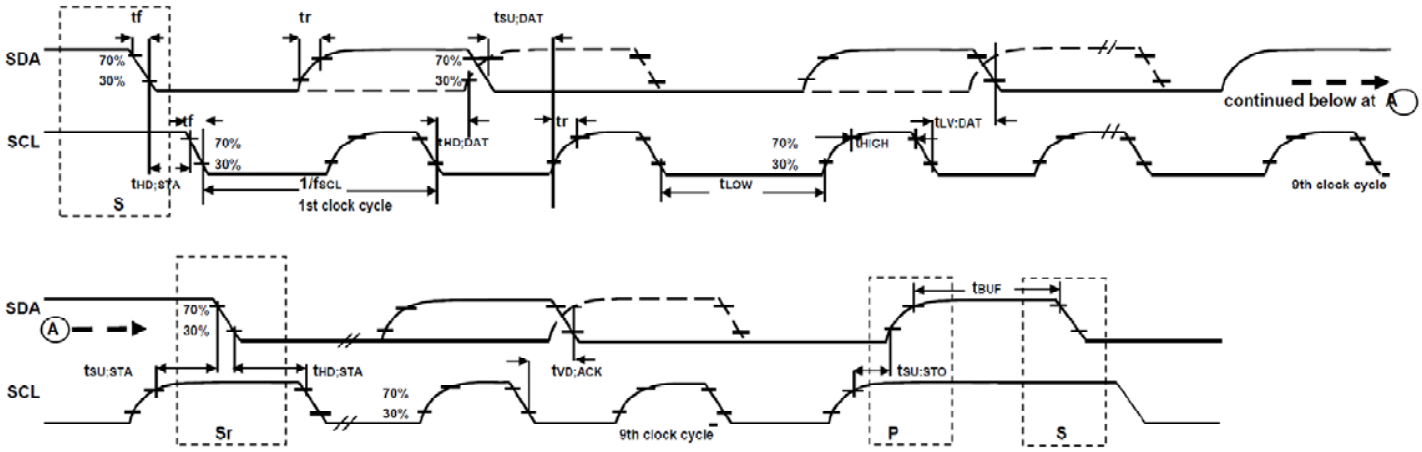
3.5 I²C Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 1.8V±5%, 2.5V±5%, 3.0V±5%, or 3.3V±5%, T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency		0		400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20 +0.1C_b		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20 +0.1C_b		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Notes:

1. Based on characterization of 5 parts over temperature on evaluation board or in socket



I²C Bus Timing Diagram

3.6 Absolute Maximum Ratings

Stress above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

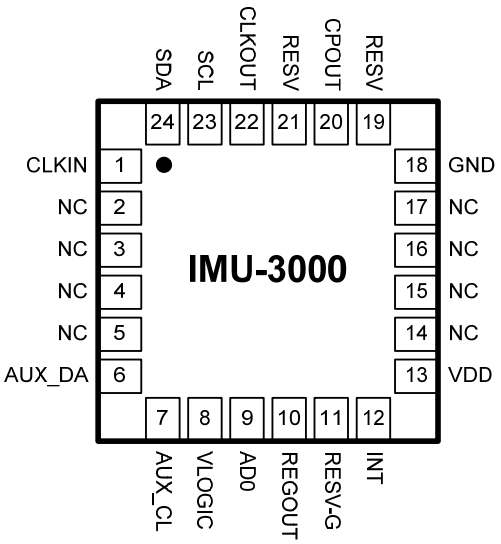
Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, VDD	-0.5V to +6V
VLOGIC Input Voltage Level	-0.5V to VDD + 0.5V
REGOUT	-0.5V to 2V
Input Voltage Level (CLKIN, AUX_DA, AD0, INT, SCL, SDA)	-0.5V to VDD + 0.5V
CPOUT (2.1V ≤ VDD ≤ 3.6V)	-0.5V to 30V
Acceleration (Any Axis, unpowered)	10,000*g* for 0.3ms
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	1.5kV (HBM); 200V (MM)
Latch-up	60mA @ 125°C JEDEC Condition "B"

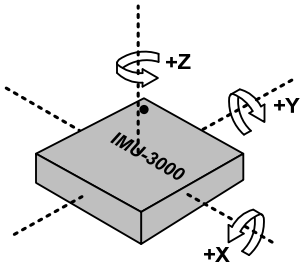
4 Applications Information

4.1 Pin Out and Signal Description

Pin Number	Pin Name	Pin Description
1	CLKIN	External reference clock input
6	AUX_DA	Interface to a 3rd party accelerometer, SDA pin. Logic levels are set to be either VDD or VLOGIC. See Section 7 for more details.
7	AUX_CL	Interface to a 3rd party accelerometer, SCL pin. Logic levels are set to be either VDD or VLOGIC. See Section 7 for more details.
8	VLOGIC	Digital I/O supply voltage. VLOGIC must be ≤ VDD at all times.
9	AD0	I^2C Slave Address LSB
10	REGOUT	Regulator filter capacitor connection
11	RESV-G	Reserved – Connect to Ground.
12	INT	Interrupt digital output (totem pole or open-drain)
13	VDD	Power supply voltage and Digital I/O supply voltage
18	GND	Power supply ground
19	RESV	Reserved. Do not connect.
20	CPOUT	Charge pump capacitor connection
21	RESV	Reserved. Do not connect.
22	CLKOUT	1MHz clock output for third-party accelerometer synchronization
23	SCL	I^2C serial clock
24	SDA	I^2C serial data
2, 3, 4, 5, 14, 15, 16, 17	NC	Not internally connected. May be used for PCB trace routing.

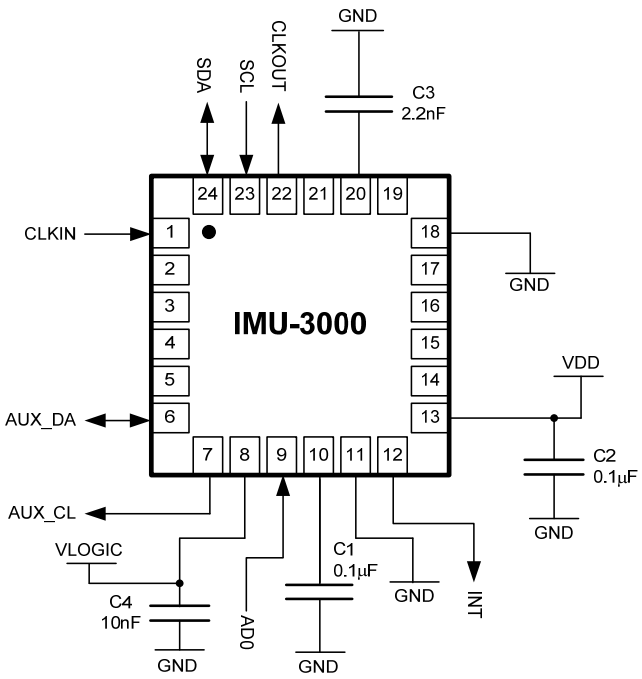


QFN Package (Top View)
24-pin, 4mm x 4mm x 0.9mm



Orientation of Axes of Sensitivity and Polarity of Rotation

4.2 Typical Operating Circuit

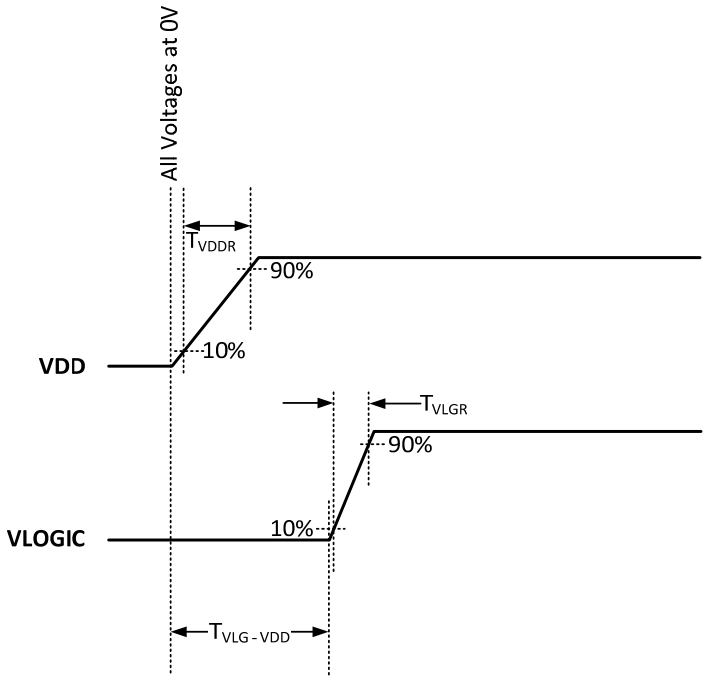


Typical Operating Circuit

4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
VDD Bypass Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 4V	1
Regulator Filter Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 2V	1
Charge Pump Capacitor	C3	Ceramic, X7R, 2.2nF ±10%, 50V	1
VLOGIC Bypass Capacitor	C4	Ceramic, X7R, 10nF ±10%, 4V	1

4.4 Recommended Power-on Procedure

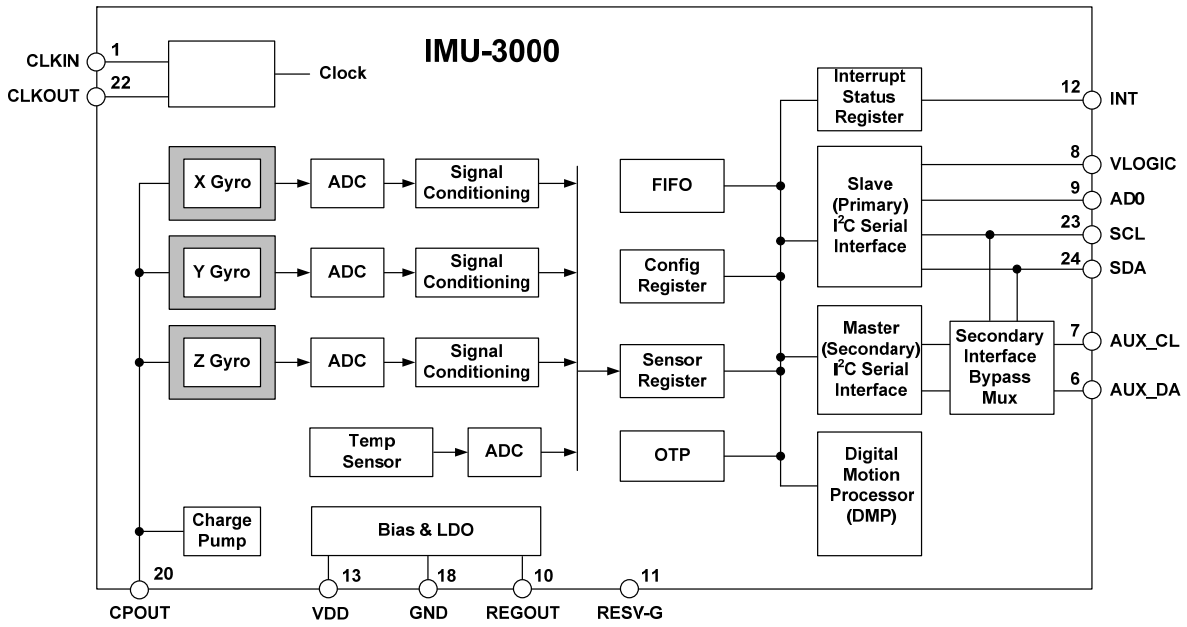


Power-Up Sequencing

1. T_{VDDR} is VDD rise time: Time for VDD to rise from 10% to 90% of its final value
2. T_{VDDR} is ≤10msec
3. T_{VLGR} is VLOGIC rise time: Time for VLOGIC to rise from 10% to 90% of its final value
4. T_{VLGR} is ≤1msec
5. $T_{VLG\text{-}VDD}$ is the delay from the start of VDD ramp to the start of VLOGIC rise
6. $T_{VLG\text{-}VDD}$ is 0 to 20msec but VLOGIC amplitude must always be ≤VDD amplitude
7. VDD and VLOGIC must be monotonic ramps

5 Functional Overview

5.1 Block Diagram



5.2 Overview

The IMU-3000 is comprised of the following key blocks / functions:

- Three-axis MEMS rate gyroscope sensors with 16-bit ADCs and signal conditioning
- Digital Motion Processor (DMP)
- Primary I^2C serial communications interface
- Secondary I^2C serial interface for 3rd party accelerometer
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDO
- Charge Pump

5.3 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The IMU-3000 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X, Y, and Z axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

5.4 Digital Motion Processor

The embedded Digital Motion Processor (DMP) is located within the IMU-3000 and offloads computation of motion processing algorithms from the host processor. The DMP acquires and processes data from the on-

chip gyroscopes and an external accelerometer. The resulting data can be read from IMU-3000's FIFO. The DMP has access to certain of the IMU's external pins, which can be used for synchronizing external devices to the motion sensors, or generating interrupts for the application.

The purpose of the DMP is to offload both timing requirements and processing power from the host processor. Typically, motion processing algorithms should be run at a high rate, often around 200Hz, in order to provide accurate results with low latency. This is required even if the application updates at a much lower rate; for example, a low power user interface may update as slowly as 5Hz, but the motion processing should still run at 200Hz. The DMP can be used as a tool in order to minimize power, simplify timing and software architecture, and save valuable MIPS on the host processor for use in the application.

5.5 Primary I^2C Serial Communications Interface

The IMU-3000 communicates to a system processor using the I^2C serial interface; the device always acts as a slave when communicating to the system processor. The logic level for communications to the master is set by the voltage on the VLOGIC pin. The LSB of the of the I^2C slave address is set by pin 9 (AD0).

5.6 Secondary I^2C Serial Interface for Third-Party Accelerometer

The IMU-3000 has a secondary I^2C bus for communicating to an off-chip 3-axis digital output accelerometer. This bus has two operating modes: I^2C Master Mode, where the IMU-3000 acts as a master to an external accelerometer connected to the secondary I^2C bus; and Pass-Through Mode, where the IMU-3000 directly connects the primary and secondary I^2C buses together, to allow the system processor to directly communicate with the external accelerometer.

Secondary I^2C Bus Modes of Operation:

- I^2C Master Mode: allows the IMU-3000 to directly access the data registers of an external digital accelerometer. In this mode, the IMU-3000 directly obtains sensor data from an accelerometer thus allowing the on-chip DMP to generate sensor fusion data without intervention from the system applications processor. In I^2C master mode, the IMU-3000 can be configured to perform burst reads, returning the following data from the accelerometer:
    - X accelerometer data (2 bytes)
    - Y accelerometer data (2 bytes)
    - Z accelerometer data (2 bytes)
- Pass-Through Mode: allows an external system processor to act as master and directly communicate to the external accelerometer connected to the secondary I^2C bus pins (AUX_DA and AUX_CL). This is useful for configuring the accelerometer, or for keeping the IMU-3000 in a low-power mode, when only the accelerometer is to be used. In this mode, the secondary I^2C bus control logic (third-party accelerometer Interface block) of the IMU-3000 is disabled, and the secondary I^2C pins AUX_DA and AUX_CL (Pins 6 and 7) are connected to the main I^2C bus (Pins 23 and 24) through analog switches.

Secondary I^2C Bus I/O Logic Levels

The logic levels of the secondary I^2C bus can be programmed to be either VDD or VLOGIC (see Sections 7 and 8).

6 Clocking

6.1 Internal Clock Generation

The IMU-3000 has a flexible clocking scheme, allowing for a variety of internal or external clock sources for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, the DMP, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- Any of the X, Y, or Z gyros (MEMS oscillators with a variation of ±1% over temperature range)

Allowable external clocking sources are:

- 32.768kHz square wave
- 19.2MHz square wave

Which source to select for generating the internal synchronous clock depends on the availability of external sources and the requirements for power consumption and clock accuracy. Most likely, these requirements will vary by mode of operation. For example, in one mode, where the biggest concern is power consumption, one may wish to operate the Digital Motion Processor of the IMU-3000 to process accelerometer data, while keeping the gyros off. In this case, the internal relaxation oscillator is a good clock choice. However, in another mode, where the gyros are active, selecting the gyros as the clock source provides for a more-accurate clock source.

Clock accuracy is important, since timing errors directly affect the distance and angle calculations performed by the Digital Motion Processor (or by extension, by any processor).

There are also start-up conditions to consider. When the IMU-3000 first starts up, the device operates off of its internal clock, until programmed to operate from another source. This allows the user, for example, to wait for the MEMS oscillators to stabilize before they are selected as the clock source.

6.2 Clock Output

In addition, the IMU-3000 provides a clock output, which allows the device to operate synchronously with an external digital 3-axis accelerometer. Operating synchronously provides for higher-quality sensor fusion data, since the sampling instant for the sensor data can be set to be coincident for all sensors.

6.3 Sensor Data Registers

The sensor data registers contain the latest gyro and temperature data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime, however, the interrupt function may be used to determine when new data is available.

6.4 FIFO

The IMU-3000 contains a 512-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines what data goes into it, with possible choices being gyro data, accelerometer data, temperature readings, and auxiliary ADC readings. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

6.5 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) Digital Motion Processor Done (programmable function); (3) new data is available to be read (from the FIFO and Data registers); and (4) the IMU-3000 did not receive an acknowledge from the accelerometer on the Secondary I^2C bus. The interrupt status can be read from the Interrupt Status register.

6.6 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the IMU-3000 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

6.7 Bias and LDO

The bias and LDO section generates the internal supply and the reference voltages and currents required by the IMU-3000. Its inputs are an unregulated VDD of 2.1V to 3.6V and a VLOGIC - logic reference supply voltage - of 1.71V to VDD. The LDO output is bypassed by a 0.1µF capacitor at REGOUT.

6.8 Charge Pump

An on-board charge pump generates the high voltage required for the MEMS oscillators. Its output is bypassed by a 2.2nF capacitor at CPOUT.

7 Digital Interface

7.1 I²C Serial Interface

The internal registers of the IMU-3000 can be accessed using I²C at up to 400kHz.

Serial Interface

Pin Number	Pin Name	Pin Description
8	VLOGIC	Digital I/O supply voltage. VLOGIC must be ≤ VDD at all times.
9	AD0	I²C Slave Address LSB
23	SCL	I²C serial clock
24	SDA	I²C serial data

7.1.1 I²C Interface

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The IMU-3000 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400kHz.

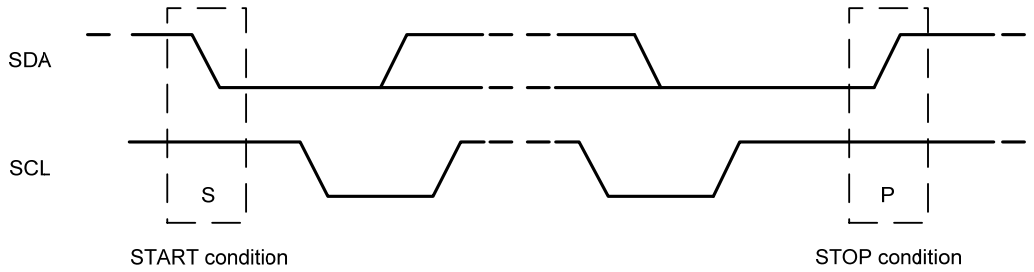
The slave address of the IMU-3000 is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin ADO. This allows two IMU-3000s to be connected to the same I²C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin ADO is logic low) and the address of the other should be b1101001 (pin AD0 is logic high). The I²C address is stored in the WHO_AM_I register.

I²C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

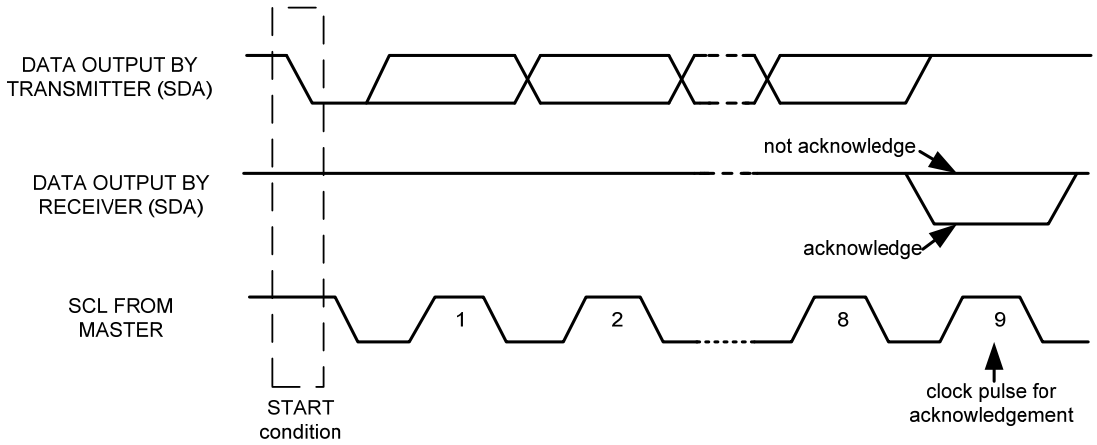


START and STOP Conditions

Data Format / Acknowledge

I^{2}C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

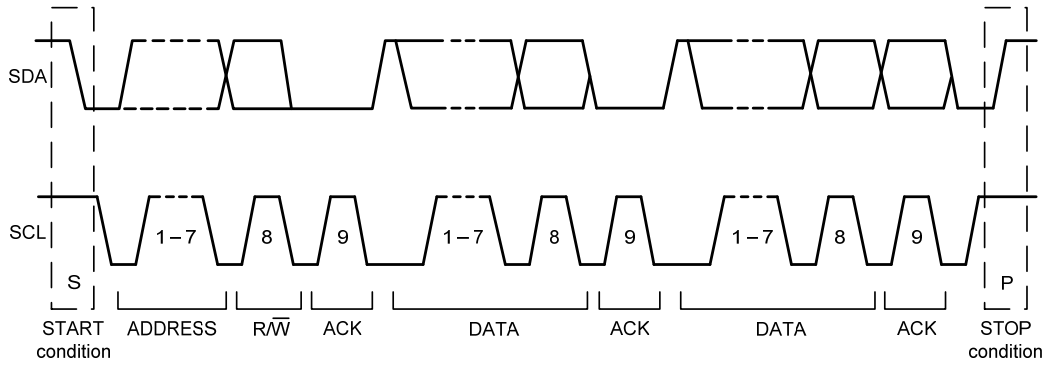
If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).



Acknowledge on the I^{2}C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.



Complete I^{2}C Data Transfer

To write the internal IMU-3000 registers, the master transmits the start condition (S), followed by the I^2C address and the write bit (0). At the 9th clock cycle (when the clock is high), the IMU-3000 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the IMU-3000 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the IMU-3000 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal IMU-3000 registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the IMU-3000, the master transmits a start signal followed by the slave address and read bit. As a result, the IMU-3000 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

I^2C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I^2C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	IMU-3000 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Serial Interface Considerations

7.2 Supported Interfaces

The IMU-3000 supports I^2C communications on both its primary (microprocessor) serial interface and its secondary (accelerometer) interface.

7.3 Logic Levels

The IMU-3000 accelerometer bus I/O logic levels are set to be either VDD or VLOGIC, as shown in the table below.

I/O Logic Levels vs. *AUX_VDDIO bit*

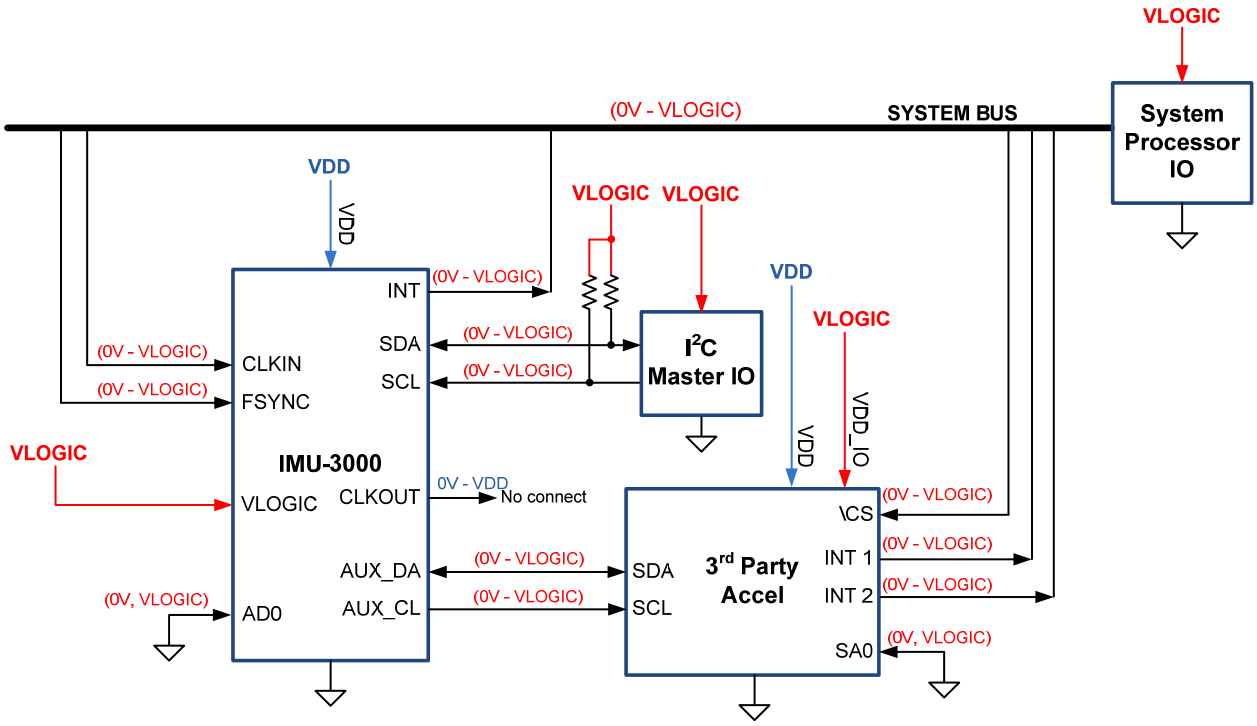
AUX_VDDIO	**MICROPROCESSOR LOGIC LEVELS** (Pins: SDA, SCL, AD0, CLKIN, INT)	**ACCELEROMETER LOGIC LEVELS** (Pins: AUX_DA, AUX_CL)
0	VLOGIC	VLOGIC
1	VLOGIC	VDD

Notes:
1. CLKOUT has logic levels that are always referenced to VDD
2. The power-on-reset value for *AUX_VDDIO* is 0.

VLOGIC may be set to be equal to VDD or to another voltage, such that at all times VLOGIC is ≤ VDD. When *AUX_VDDIO* is set to 0 (its power-on-reset value), VLOGIC is the reference voltage for both the microprocessor system bus and the accelerometer secondary bus, as shown in the figure of Section 8.2.1. When *AUX_VDDIO* is set to 1, VLOGIC is the reference voltage for the microprocessor system bus and VDD is the reference voltage for the accelerometer secondary bus, as shown in the figure of Section 8.2.2.

7.3.1 *AUX_VDDIO* = 0

The figure below shows logic levels and voltage connections for AUX_VDDIO = 0. Note that the actual configuration will depend on the type of third-party accelerometer used.



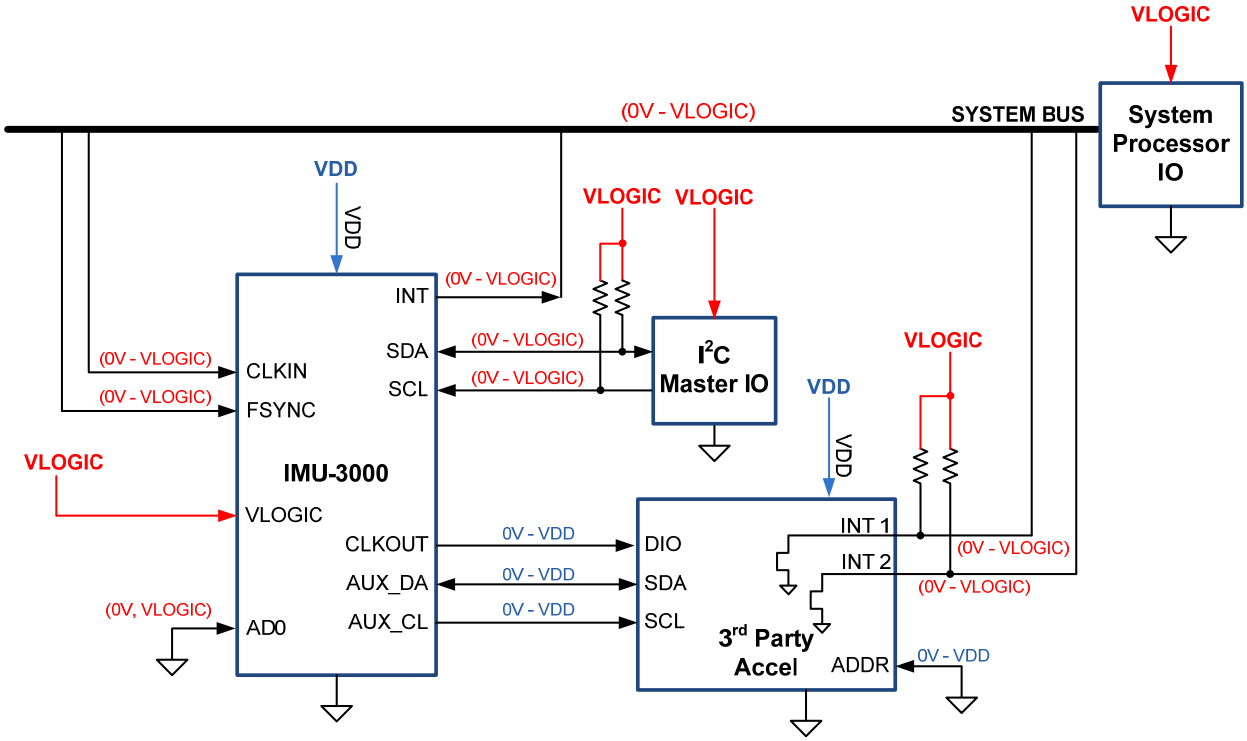
Notes:

1. The AUX_*VDDIO* register bit determines the I/O voltage levels of AUX_DA and AUX_CL (0 = set output levels relative to VLOGIC)
2. CLKOUT is always referenced to VDD
3. Other IMU-3000 logic I/O are always referenced to VLOGIC

I/O Levels and Connections for *AUX_VDDIO* = 0

7.3.2 *AUX_VDDIO* = 1

When *AUX_VDDIO* is set to 1 by the user, VLOGIC is the reference voltage for the microprocessor system bus and VDD is the reference voltage for the accelerometer secondary bus, as shown in the figure below. This is useful when interfacing to a third-party accelerometer where there is only one supply for both the logic and analog sections of the 3rd party accelerometer.



Voltage/ Configuration	Configuration 1	Configuration 2
VLOGIC	1.8V±5%	3.0V±5%
VDD	2.5V±5%	3.0V±5%
AUX_VDDIO	1	1

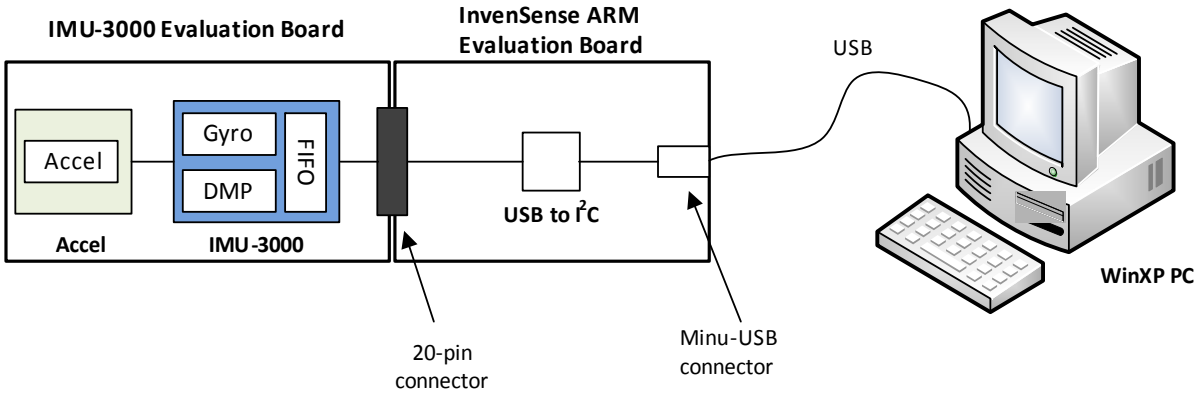
Notes:

1. The *AUX_VDDIO* register bit determines the I/O voltage levels of AUX_DA and AUX_CL (1 = set output levels relative to VDD)
2. CLKOUT is always referenced to VDD
3. Other IMU-3000 logic I/O are always referenced to VLOGIC
4. If third-party accelerometer logic levels are referenced to VDD; setting INT1 and INT2 to open-drain configuration provides voltage compatibility when VDD ≠ VLOGIC.
   When VDD = VLOGIC, INT1 and INT2 may be set to push-pull outputs, and the external pull-up resistors will not be needed.

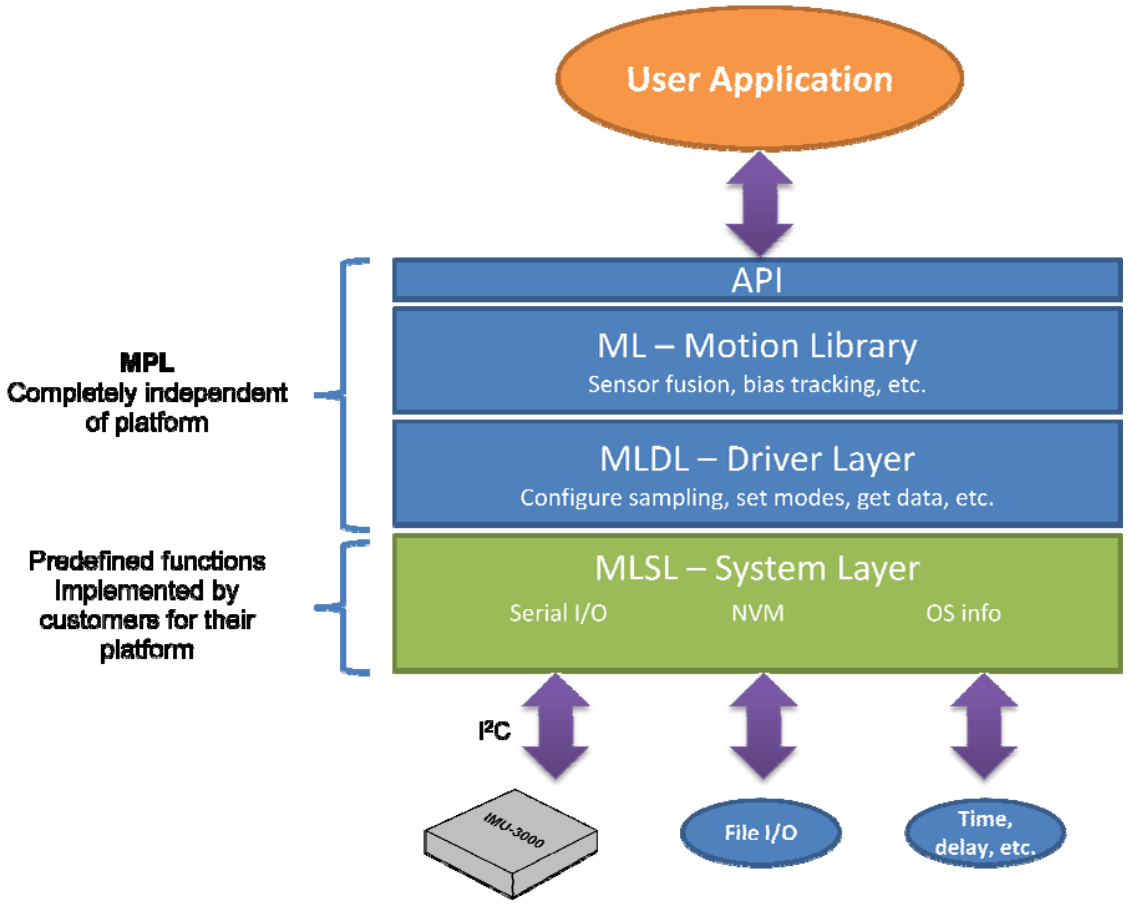
I/O Levels and Connections for Two Example Power Configurations (*AUX_VDDIO* = 1)

8 Motion Processing Library (MPL)

To assist in the rapid development and deployment of products using the IMU-3000, InvenSense provides a Motion Processing Library (MPL) software development kit that has been verified to work in the hardware and software environment shown in the figure below.



The MPL contains the core algorithm engines for motion processing, and includes an API layer which provides a simple interface into using these engines (see figure below).



The MPL communicates with the System Layer, which is a platform-specific interface into the hardware and software environment; this System Layer software must be implemented by the customer for his particular environment. The software development kit includes shell functions to speed up the development of this System Layer software. The MPL is independent of the Operating System (OS) since the System Layer software handles OS-specific requirements.

The purpose of the DMP is to offload both timing requirements and processing requirements from the host processor. Typically, raw data integration (sensor fusion) should be run at a high rate, often around 200Hz, in order to provide accurate results with low latency. This is required even if the application updates at a much lower rate; for example, a low power user interface may update as slowly as 5Hz, but the sensor fusion should still run at 200Hz. The DMP can be used to minimize power, simplify timing and software architecture, and saving valuable MIPS on the host processor for use in the application.

The IMU-3000 MPL Functional Specification describes in detail the API and System Layer routines needed for interfacing to the IMU-3000.

8.1 Demo Software

InvenSense provides demonstration software in the form of source code and a compiled demonstration that runs on a PC running Windows XP. This software works in conjunction with the hardware shown in the figure at the top of Section 8. The PC demo software provides the functionality that allows a user to become familiar with the use of gyros and accelerometers.

9 Register Map

Addr (Hex)	Addr (Decimal)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	WHO_AM_I	R/W	0	ID						-
C	12	X_OFFS_USRH	R/W	X_OFF_H							
D	13	X_OFFS_USRL	R/W	X_OFF_L							
E	14	Y_OFFS_USRH	R/W	Y_OFFS_H							
F	15	Y_OFFS_USRL	R/W	Y_OFFS_L							
10	16	Z_OFFS_USRH	R/W	Z_OFFS_H							
11	17	Z_OFFS_USRL	R/W	Z_OFFS_L							
12	18	FIFO_EN	R/W	TEMP_ OUT	GYRO_ XOUT	GYRO_ YOUT	GYRO_ ZOUT	AUX_ XOUT	AUX_ YOUT	AUX_ ZOUT	FIFO_ FOOTER
13	19	AUX_VDDIO	R/W	0	0	0	0	0	AUX_ VDDIO	0	0
14	20	AUX_SLV_ ADDR	R/W	CLKOUT EN	AUX_ID						
15	21	SMPLRT_DIV	R/W		SMPLRT_DIV						
16	22	DLPF_FS	R/W	0	0	0	FS_SEL		DLPF_CFG		
17	23	INT_CFG	R/W	ACTL	OPEN	LATCH_ INT_EN	INT_ ANYRD_ 2CLEAR	I2C_MST _ERR_E N	IMU_ RDY_ EN	DMP_ DONE _EN	RAW_ RDY_ EN
18	24	AUX_BURST_AD DR	R/W	BURST_ADDR							
1A	26	INT_STATUS	R	FIFO_FU LL	-	-		I2C_MST _ERR	IMU_ RDY	DMP_ DONE	RAW_ DATA_ RDY
1B	27	TEMP_OUT_H	R	TEMP_OUT_H							
1C	28	TEMP_OUT_L	R	TEMP_OUT_L							
1D	29	GYRO_XOUT_H	R	GYRO_XOUT_H							
1E	30	GYRO_XOUT_L	R	GYRO_XOUT_L							
1F	31	GYRO_YOUT_H	R	GYRO_YOUT_H							
20	32	GYRO_YOUT_L	R	GYRO_YOUT_L							
21	33	GYRO_ZOUT_H	R	GYRO_ZOUT_H							
22	34	GYRO_ZOUT_L	R	GYRO_ZOUT_L							
23	35	AUX_XOUT_H	R	AUX_XOUT_H							
24	36	AUX_XOUT_L	R	AUX_XOUT_L							
25	37	AUX_YOUT_H	R	AUX_YOUT_H							
26	38	AUX_YOUT_L	R	AUX_YOUT_L							
27	39	AUX_ZOUT_H	R	AUX_ZOUT_H							
28	40	AUX_ZOUT_L	R	AUX_ZOUT_L							
35	53	DMP_REG1	R/W	RESERVED1							
36	54	DMP_REG2	R/W	RESERVED2							
37	55	DMP_REG3	R/W	RESERVED3							
38	56	DMP_REG4	R/W	RESERVED4							
39	57	DMP_REG5	R/W	RESERVED5							
3A	58	FIFO_COUNTH	R	-	-	-	-	-	-	FIFO_COUNT_H	
3B	59	FIFO_COUNTL	R	FIFO_COUNT_L							
3C	60	FIFO_R	R	FIFO_DATA							
3D	61	USER_CTRL	R/W	DMP_EN	FIFO_EN	AUX_IF_EN	-	AUX_IF_RST	DMP_RST	FIFO_RST	GYRO_RST
3E	62	PWR_MGM	R/W	H_RESET	SLEEP	STBY_XG	STBY_YG	STBY_ZG	CLK_SEL		

10 Register Description

This section details each register within the InvenSense IMU-3000 gyroscope. Note that any bit that is not defined should be set to zero in order to be compatible with future InvenSense devices.

The register space allows single-byte reads and writes, as well as burst reads and writes. When performing burst reads or writes, the memory pointer will increment until either (1) reading or writing is terminated by the master, or (2) the memory pointer reaches registers 57 or 60.

10.1 Register 0 – Who Am I

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	ID						-

Description:
This register is used to verify the identity of the device.
Parameters:

ID Contains the I^2C address of the device, which can be changed by writing to this register.
0 This register bit must be set to 0 when writing to this register.

The Power-On-Reset value of Bit6: Bit1 is 110 100.

The Power-On-Reset value of Bit7 is 0.

10.2 Registers 12 to 17 – Gyro Offsets

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C	12	X_OFFS_H							
D	13	X_OFFS_L							
E	14	Y_OFFS_H							
F	15	Y_OFFS_L							
10	16	Z_OFFS_H							
11	17	Z_OFFS_L							

Description:
These registers are used to remove DC bias from the sensor outputs. The values in these registers are subtracted from the gyro sensor values before going into the sensor registers (see registers 29 to 34).

Parameters:
X_OFFS_H/L 16-bit offset (high and low bytes) of X gyro offset (2's complement)
Y_OFFS_H/L 16-bit offset (high and low bytes) of Y gyro offset (2's complement)
Z_OFFS_H/L 16-bit offset (high and low bytes) of Z gyro offset (2's complement)

10.3 Register 18 – FIFO Enable

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
12	18	TEMP_ OUT	GYRO_ XOUT	GYRO_ YOUT	GYRO_ ZOUT	AUX_ XOUT	AUX_ YOUT	AUX_ ZOUT	FIFO_ FOOTER	00h

Description:
This register determines what data goes into the IMU-3000 FIFO, which is a 512 byte First-In-First-Out buffer (see register 60). Sensor data is automatically placed into the FIFO after each ADC sampling period is complete. The ADC sample rate is controlled by register 21.

The order at which the data is put into the FIFO is from MSB to LSB, which means that it will match the order shown in the parameter detail below. Two bytes are used for each reading. For example, if Gyro X, Gyro Y, Gyro Z, and FIFO_FOOTER are configured to go into the FIFO, then each sample period the following 8 bytes would be inserted into the FIFO, as shown below:

Gyro X High byte	Gyro X Low byte	Gyro Y High byte	Gyro Y Low byte	Gyro Z High byte	Gyro Z Low byte	FIFO_FOOTER High byte	FIFO_FOOTER Low byte

Parameters:

TEMP_OUT	Setting this inserts the Temperature reading into FIFO
GYRO_XOUT	Setting this inserts the X Gyro reading into FIFO
GYRO_YOUT	Setting this inserts the Y Gyro reading into FIFO
GYRO_ZOUT	Setting this inserts the Z Gyro reading into FIFO
AUX_XOUT	Setting this inserts the X Accelerometer reading into FIFO
AUX_YOUT	Setting this inserts the Y Accelerometer reading into FIFO
AUX_ZOUT	Setting this inserts the Z Accelerometer reading into FIFO
FIFO_FOOTER	Last word (2 bytes) for FIFO read. Described in more detail in Section 60

10.4 Registers 19 – AUX (Accel) VDDIO

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
13	19	0	0	0	0	0	AUX_ VDDIO	0	0	00h

Description:
This register determines the I/O logic levels for the secondary I^2C bus clock and data lines (AUX_CL, AUX_DA). 1=VDD, 0=VLOGIC.

Parameters:

AUX_VDDIO	I/O logic levels for the secondary I^2C bus clock and data lines (AUX_CL, AUX_DA). 1=VDD, 0=VLOGIC.
0	Load zeros into Bits 0, 1, 3-7.

10.5 Register 20 – AUX (Accel) Slave Address

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
14	20	CLKOUTEN	AUX_ID							00h

Description:
This register contains the enable bit for the reference clock output and the 7-bit slave address of the external 3rd party accelerometer.

The CLKOUTEN bit is used to enable (1) or disable (0) the reference clock output at the CLKOUT pin.

AUX_ID, the 7-bit accelerometer slave address, is used to access the accelerometer so that its sensor reading can be automatically read during each sample period at the same time as the gyro sensors.

When reading the external accelerometer registers, the IMU-3000 takes over the secondary I^2C bus, as a master to the accel, performing a burst read of the sensor registers. For this interface to be active, the AUX_*IF_EN* flag in the User Control register (61) must be set (set to 1).

Whenever changing this register, the secondary accel interface must be reset with AUX_*IF_RST* to take effect. Refer to the User Control register (61).

Parameters:

CLKOUTEN The enable bit for the reference clock output that is provided at the CLKOUT pin. 1=clock output enabled; 0=clock output disabled.

AUX_ID Contains the I^2C address of the external accelerometer. The address can be changed by writing to this register.

10.6 Register 21 – Sample Rate Divider

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
15	21	SMPLRT_DIV								00h

Description:
This register determines the sample rate of the IMU-3000 gyros. The analog gyros are sampled internally at either 1kHz or 8kHz, determined by the *DLPF_CFG* setting (see register 22). This sampling is then filtered digitally and delivered into the sensor registers after the number of cycles determined by this register. The sample rate is given by the following formula:

$F_{sample} = F_{internal} / (divider+1)$, where $F_{internal}$ is either 1kHz or 8kHz

As an example, if the internal sampling is at 1kHz, then setting this register to 7 would give the following:

$F_{sample} = 1kHz / (7 + 1) = 125Hz$, or 8ms per sample

Parameters:

SMPLRT_DIV Sample rate divider: 0 to 255

10.7 Register 22 – DLPF, Full Scale

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
16	22	0	0	0	FS_SEL		DLPF_CFG			00h

Description:

This register configures parameters related to the sensor acquisition.

The *FS_SEL* parameter allows setting the full-scale range of the gyro sensors, as described in the table below.

FS_SEL

FS_SEL	Gyro Full-Scale Range
0	±250°/sec
1	±500°/sec
2	±1000°/sec
3	±2000°/sec

The *DLPF_CFG* parameter sets the digital low pass filter configuration. It also determines the internal analog sampling rate used by the device as shown in the table below.

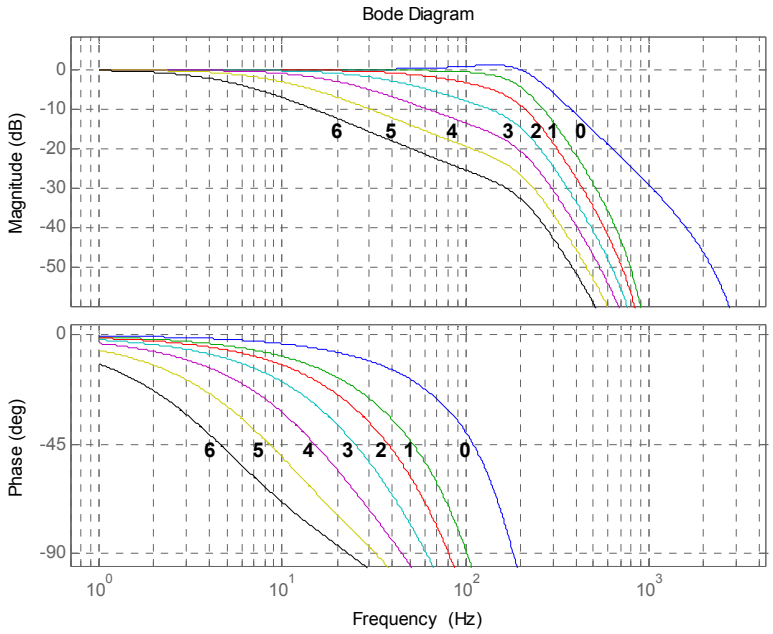
DLPF_CFG

DLPF_CFG	Low Pass Filter Bandwidth	Analog Sample Rate
0	256Hz	8kHz
1	188Hz	1kHz
2	98Hz	1kHz
3	42Hz	1kHz
4	20Hz	1kHz
5	10Hz	1kHz
6	5Hz	1kHz
7	Reserved	Reserved

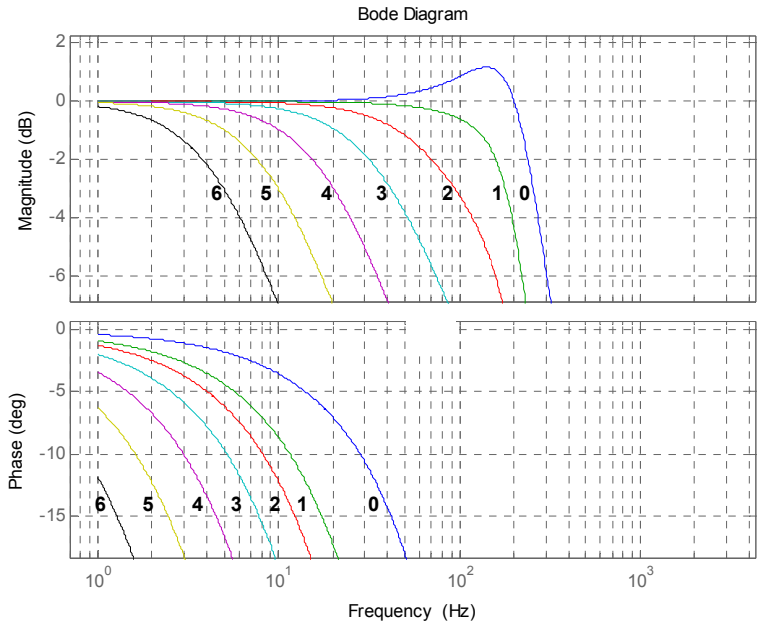
Parameters:

FS_SEL Full scale selection for gyro sensor data
DLPF_CFG Digital low pass filter configuration
0 Load zeros into Bits 5-7 of the DLPF, Full Scale register

DLPF Characteristics: The gain and phase responses of the digital low pass filter settings (*DLPF_CFG*) are shown below:



Gain and Phase vs. Digital Filter Setting



Gain and Phase vs. Digital Filter Setting, Showing Passband Details

10.8 Register 23 – Interrupt Configuration

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
17	23	ACTL	OPEN	LATCH_INT_EN	INT_ANYRD_2CLEAR	I2C_MST_ERR_EN	IMU_RDY_EN	DMP_DONE_EN	RAW_RDY_EN	00h

Description:

This register configures the interrupt operation of the IMU-3000. The interrupt output pin (INT) configuration can be set, the interrupt latching/clearing method can be set, and the triggers for the interrupt can be set. If LATCH_INT_EN = 1, the INT pin is held active until the interrupt status register is cleared.

Note that if the application requires reading every sample of data from the IMU-3000, it is best to enable the raw data ready interrupt (*RAW_RDY_EN*). This allows the application to know when new sample data is available.

Parameters:

ACTL	Logic level for INT output pin – 1=active low, 0=active high
OPEN	Drive type for INT output pin – 1=open drain, 0=push-pull
LATCH_INT_EN	Latch mode – 1=latch until interrupt is cleared, 0=50µs pulse
INT_ANYRD_2CLEAR	Interrupt status register clear method – 1=clear by reading any register, 0=clear by reading interrupt status register (26) only
I2C_MST_ERR_EN	Enable interrupt when accelerometer on secondary I^2C bus does not acknowledge IMU-3000
IMU_RDY_EN	Enable interrupt when device is ready (PLL ready after changing clock source)
DMP_DONE_EN	Enable interrupt when DMP is done (programmable functionality)
RAW_RDY_EN	Enable interrupt when data is available

10.9 Register 24 – AUX (Accel) Burst Read Address / Secondary I^2C Bus I/O Level

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
18	24	BURST_ADDR								00h

Description:

This register configures the burst-mode-read starting address for an accelerometer attached to the secondary I^2C bus of the IMU-3000, and determines the I/O logic levels of the secondary I^2C bus clock and data lines (AUX_CL, AUX_DA).

Parameters:

AUX_VDDIO	I/O logic levels for the secondary I^2C bus clock and data lines (AUX_CL, AUX_DA; 1=VDD, 0=VLOGIC)
BURST_ADDR	Burst-mode-read starting address for external accelerometer attached to secondary I^2C bus of the IMU-3000.

10.10 Register 26 – Interrupt Status

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
1A	26	FIFO_FULL	-	-	-	I2C_MST _ERR	IMU_ RDY	DMP_ DONE	RAW_ DATA_ RDY	00h

Description:

This register is used to determine the status of the IMU-3000 interrupt. Whenever one of the interrupt sources is triggered, the corresponding bit will be set. The polarity of the interrupt pin (active high/low) and the latch type (pulse or latch) has no affect on these status bits.

In normal use, the *RAW_DATA_RDY* interrupt is used to determine when new sensor data is available in either the sensor registers (27 to 34) or in the FIFO (60).

Interrupt Status bits get cleared as determined by INT_ANYRD_2CLEAR in the interrupt configuration register (23).

Parameters:

FIFO_FULL	FIFO has overflowed. Cleared when Register 26 is read and when *FIFO_RST* (register 61) is set.
I2C_MST_ERR	The IMU-3000 did not receive an acknowledge from the accelerometer on the secondary I^2C bus when the IMU-3000 was acting as a master
IMU_RDY	PLL ready
DMP_DONE	Digital Motion Processor (DMP) is done
RAW_DATA_RDY	Raw data or FIFO data is ready

10.11 Registers 27 to 40 – Sensor Registers

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value*
1B	27	TEMP_OUT_H								00h
1C	28	TEMP_OUT_L								00h
1D	29	GYRO_XOUT_H								00h
1E	30	GYRO_XOUT_L								00h
1F	31	GYRO_YOUT_H								00h
20	32	GYRO_YOUT_L								00h
21	33	GYRO_ZOUT_H								00h
22	34	GYRO_ZOUT_L								00h
23	35	AUX_XOUT_H								00h
24	36	AUX_XOUT_L								00h
25	37	AUX_YOUT_H								00h
26	38	AUX_YOUT_L								00h
27	39	AUX_ZOUT_H								00h
28	40	AUX_ZOUT_L								00h

*Default Value applies if sensor is disabled.

Description:

These registers contain the gyro, temperature sensor, and accelerometer (aux) data for the IMU-3000. At any time, these values can be read from the device; however it is best to use the interrupt function to determine when new data is available.

If the FIFO is used, the contents of these registers are automatically copied into the FIFO at each sample period, and then this data can be read from the FIFO (register 60).

Before being placed into these registers, the gyro sensor data is first manipulated by the full scale setting (register 22) and the offset settings (registers 12 to 17).

Parameters:

TEMP_OUT_H/L 16-bit temperature data (2's complement data format)
GYRO_XOUT_H/L 16-bit X gyro output data (2's complement data format)
GYRO_YOUT_H/L 16-bit Y gyro output data (2's complement data format)
GYRO_ZOUT_H/L 16-bit Z gyro output data (2's complement data format)
AUX_XOUT_H/L 16-bit X aux (accel) output data (as available from aux)
AUX_YOUT_H/L 16-bit Y aux (accel) output data (as available from aux)
AUX_ZOUT_H/L 16-bit Z aux (accel) output data (as available from aux)

10.12 Registers 53 to 57 – DMP Registers

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35	53	RESERVED1							
36	54	RESERVED2							
37	55	RESERVED3							
38	56	RESERVED4							
38	57	RESERVED5							

Description:
The data for these registers is included in a source code file supplied by InvenSense, and is used for the Digital Motion Processor (DMP) operation. This data is only necessary if the DMP is enabled using the User Control register (register 61).

Parameters:
RESERVED1 Reserved data1 for the DMP
RESERVED2 Reserved data2 for the DMP
RESERVED3 Reserved data3 for the DMP
RESERVED4 Reserved data4 for the DMP
RESERVED5 Reserved data5 for the DMP

10.13 Registers 58 to 59 – FIFO Count

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3A	58	-	-	-	-	-	-	FIFO_COUNT_H		00h
3B	59	FIFO_COUNT_L								00h

Description:
These registers indicate how many bytes of valid data are contained in the FIFO. The FIFO can contain up to 512 bytes of data

If the FIFO gets filled up completely, the length will read 512. In this state, the IMU-3000 continues to put new sensor data into the FIFO, thus overwriting old FIFO data. Note, however, that the alignment of sensor data can change in this overflow condition. InvenSense recommends resetting the FIFO if an overflow condition occurs (use register 61), which will clear out the FIFO.

Parameters:
FIFO_COUNT_H/L Number of bytes currently in FIFO

10.14 Register 60 – FIFO Data

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3C	60	FIFO_DATA								00h

Parameters:
FIFO_DATA Contains the FIFO data

Description:
This is the output register of the FIFO. Each read of this register gets the oldest contents of the IMU-3000 FIFO buffer; thus the data is read out in the same order that the IMU-3000 put the data in. If the FIFO operation is enabled, the IMU-3000 puts new data into the FIFO at each sample interval. The data that goes in is determined by the FIFO enable register (18).

A burst read or write is required for reading or writing *multiple* bytes to or from this register, since any read or write on this register causes an auto increment and a prefetch to occur.

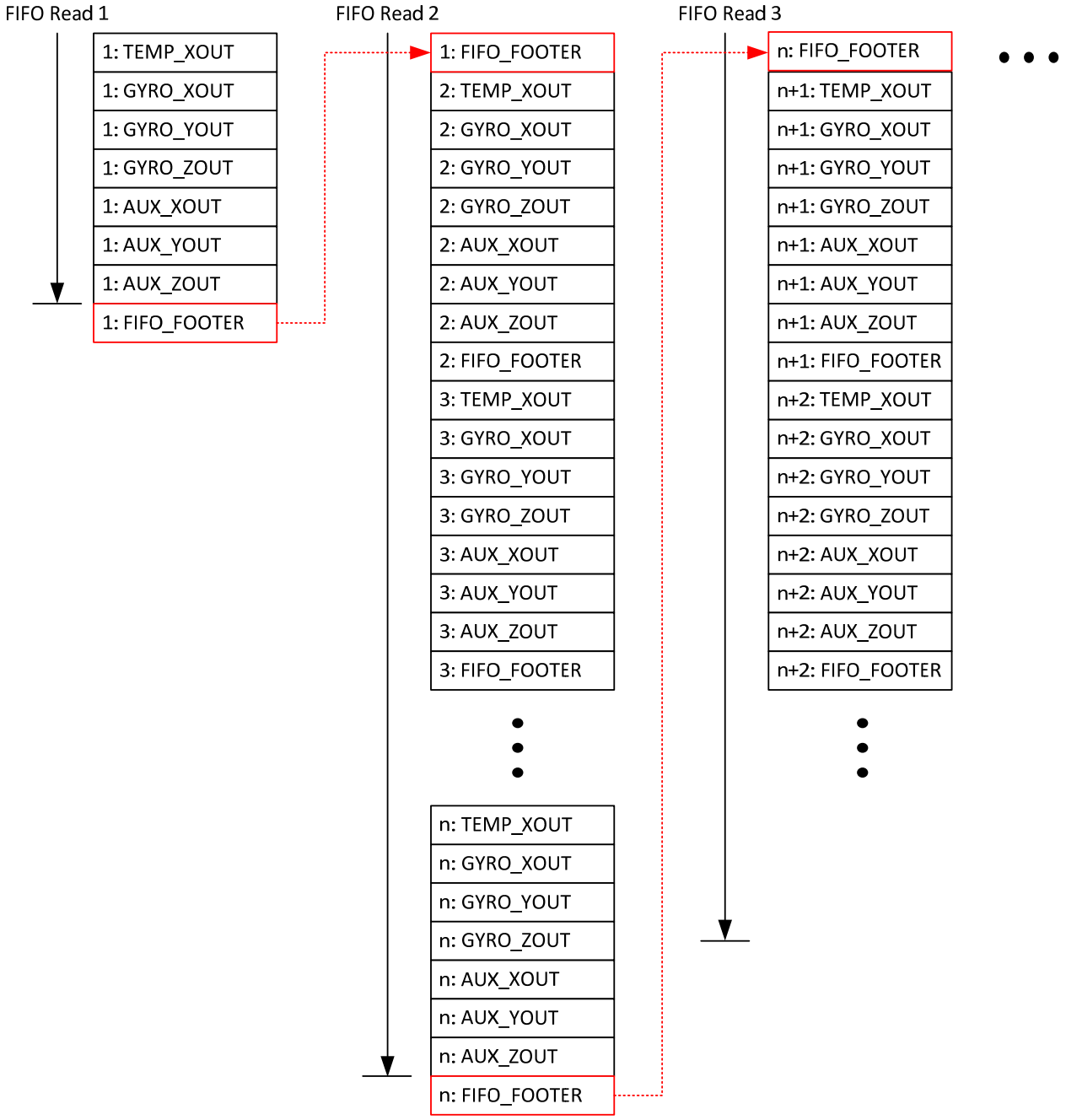
Proper operation of the FIFO requires that at least one word (2 bytes) of data be left in the FIFO during any read operation. To implement this, it is recommended that one extra two byte word (FIFO_FOOTER) be added to the end of the FIFO data so that all desired data can be read at each cycle, leaving the extra word remaining in the FIFO. This extra word will be read out (first) during the next read operation on the FIFO.
Data is read into the FIFO in the following order:

TEMP_OUT	Temperature high and low bytes (2 bytes)
GYRO_XOUT	X Gyro high and low bytes (2 bytes)
GYRO_YOUT	Y Gyro high and low bytes (2 bytes)
GYRO_ZOUT	Z Gyro high and low bytes (2 bytes)
AUX_XOUT	X Accelerometer high and low bytes (2 bytes)
AUX_YOUT	Y Accelerometer high and low bytes (2 bytes)
AUX_ZOUT	Z Accelerometer high and low bytes (2 bytes)
FIFO_FOOTER	*Last word for FIFO read (2 bytes)*

For example, if it is desired to obtain temperature, gyro, and accelerometer data from the FIFO, then one should also add FIFO_FOOTER into the FIFO enable register (18) in addition to the desired data. As shown in the figure below, the first time data is written to the FIFO, the FIFO will contain: *TEMP_OUT, GYRO_XOUT, GYRO_YOUT, GYRO_ZOUT, AUX_XOUT, AUX_YOUT, AUX_ZOUT,* and *FIFO_FOOTER*. The first FIFO read will read all but the *FIFO_FOOTER* data, which will be read in the 2nd FIFO read. In the 2nd FIFO read, the *FIFO_FOOTER* data that was left over from the previous read is read out first, followed by all but the last *FIFO_FOOTER* data in the FIFO. This pattern of reading is continued, as shown in the figure.

Note that the first FIFO read is similar to the subsequent reads in that one word of data is always left in the FIFO. It differs, though, in that the in subsequent reads the leftover data from the previous read is read first; however, for the first read there is no leftover data from a previous read.

If the FIFO is allowed to overflow, it operates as a circular buffer in which at any time it contains the most recent 512 bytes. Recommended operation in this mode is to disable data going into the FIFO prior to reading the FIFO to avoid pointer conflicts. After halting the FIFO input, the 512 bytes in the FIFO should be read out in a single burst read. The first byte read will not be valid.



Reading from the FIFO

(Note that AUX_XOUT, AUX_YOUT, and AUX_ZOUT are the X, Y, and Z accelerometer outputs, respectively.)

10.15 Register 61 – User Control

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3D	61	DMP_EN	FIFO_EN	AUX_IF_EN	-	AUX_IF_RST	DMP_RST	FIFO_RST	GYRO_RST	00h

Description:
This register is used to enable various modes on the IMU-3000, as well as reset these functions.

For each of the functions that can be enabled, the function should be reset at the same time to assure it works properly. Note that the reset bits in the register are automatically cleared after the function is reset.

For example, to enable the FIFO set both the *FIFO_EN* and the *FIFO_RST* bits. This will start the FIFO storage on the next sample period.

As an additional example, for an external processor to communicate directly to the external accelerometer (i.e. have the secondary I^2C bus be directly connected to the primary I^2C bus), the AUX*_IF_EN* bit should be cleared and the AUX*_IF_RST* bit should be set. This will allow the I^2C bus to pass through the IMU-3000 and allow the processor to control the accelerometer device (as well as the IMU). Pass through mode is useful for allowing the processor to configure the accelerometer, since the IMU-3000 can perform burst reads on the accelerometer, but is not set up to configure the device.

Parameters:

DMP_EN	Enable Digital Motion Processor (DMP)
FIFO_EN	Enable FIFO operation for sensor data
AUX_IF_EN	Enable IMU as master to accelerometer interface via secondary I^2C (clear bit to configure primary I^2C bus to pass through directly to the secondary I^2C bus)
AUX_IF_RST	Reset secondary accelerometer interface function; set this whenever changing AUX*_IF_EN*
DMP_RST	Reset DMP function; set this whenever changing *DMP_EN*
FIFO_RST	Reset FIFO function; set this to clear FIFO or when changing *FIFO_EN*
GYRO_RST	Reset gyro analog and digital functions

10.16 Register 62 – Power Management

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3E	62	H_RESET	SLEEP	STBY_XG	STBY_YG	STBY_ZG	CLK_SEL			00h

Description:

This register is used to manage the power control, select the clock source, and to issue a master reset to the device.

H_RESET is used to reset the device and set the internal registers to the power-up default settings.

STBY_XG, STBY_YG, and *STBY_ZG* are used to place the gyros into a standby or active mode (1=standby; 0=normal operating mode).

Setting the *SLEEP* bit in the register puts the device into a low power sleep mode. In this mode, only the serial interface and internal registers remain active, allowing for a very low standby current. Clearing this bit puts the device back into normal mode. The individual standby selections for each of the gyros should be used if any of them are not used by the application.

The *CLK_SEL* setting determines the device clock source as follows:

CLK_SEL

CLK_SEL	Clock Source
0	Internal oscillator
1	PLL with X Gyro reference
2	PLL with Y Gyro reference
3	PLL with Z Gyro reference
4	PLL with external 32.768kHz reference
5	PLL with external 19.2MHz reference
6	Reserved
7	Stop clock and synchronous reset clock state

On power up, the IMU-3000 defaults to the internal oscillator. It is highly recommended that the device is configured to use one of the gyros (or an external clock) as the clock reference, due to the improved stability.

Parameters:

H_RESET	Reset device and internal registers to the power-up-default settings
SLEEP	Enable low power sleep mode
STBY_XG	Put gyro X in standby mode (1=standby, 0=normal)
STBY_YG	Put gyro Y in standby mode (1=standby, 0=normal)
STBY_ZG	Put gyro Z in standby mode (1=standby, 0=normal)
CLK_SEL	Select device clock source

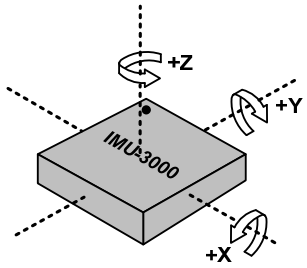
11 Assembly

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in Quad Flat No leads package (QFN) surface mount integrated circuits. The following six best practices will ensure higher quality in assembly.

1. Do not leave parts out of the original moisture-sealed bags for more than 48 hours before assembly
2. Do not solder the center pad
3. Do not place large insertion components, such as buttons, switches, connectors, or shielding boxes at a distance of less than 6 mm from the MEMS gyro
4. Do use Electrostatic Discharge (ESD) protection at or better than 200V, preferably 150V, to prevent Machine Model (MM) type ESD damage
5. Do use ESD protection measures to ensure that personnel prevent Human Body Model (HBM) type ESD damage
6. Do not mechanically impact or shock the package in any of the production processes

11.1 Orientation

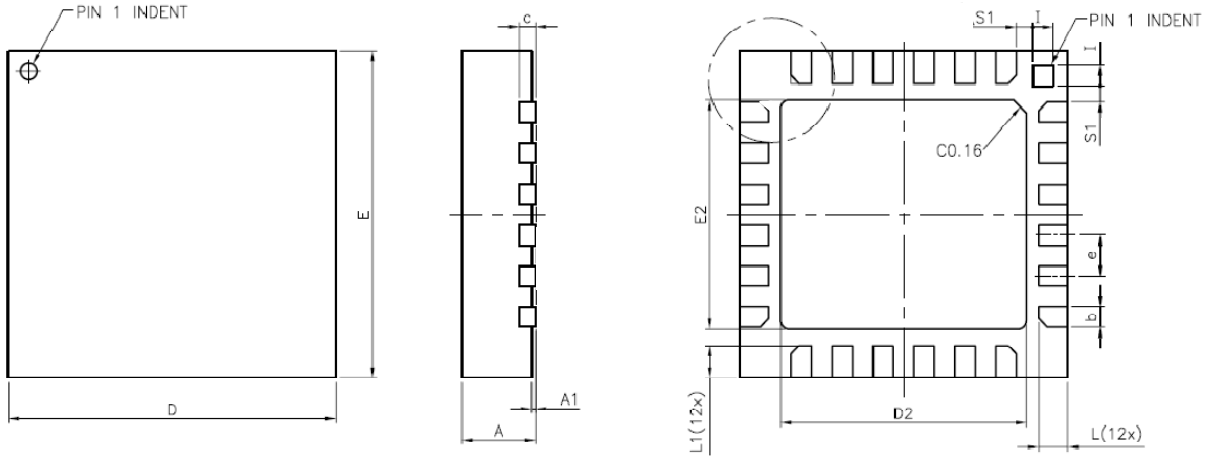
The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation.

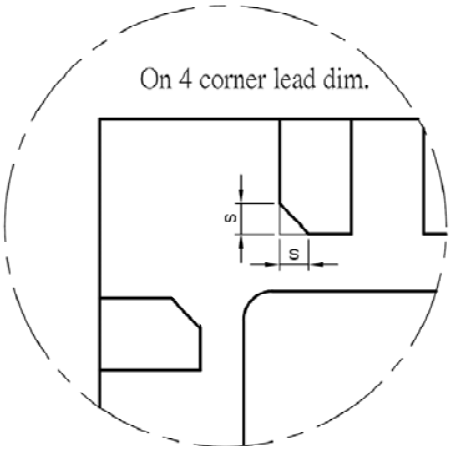


Orientation of Axes of Sensitivity and Polarity of Rotation

11.2 PCB Layout Guidelines

11.2.1 Package Dimensions



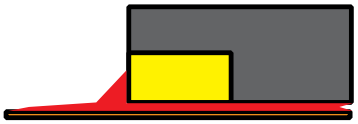


NOTE:
1.THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE

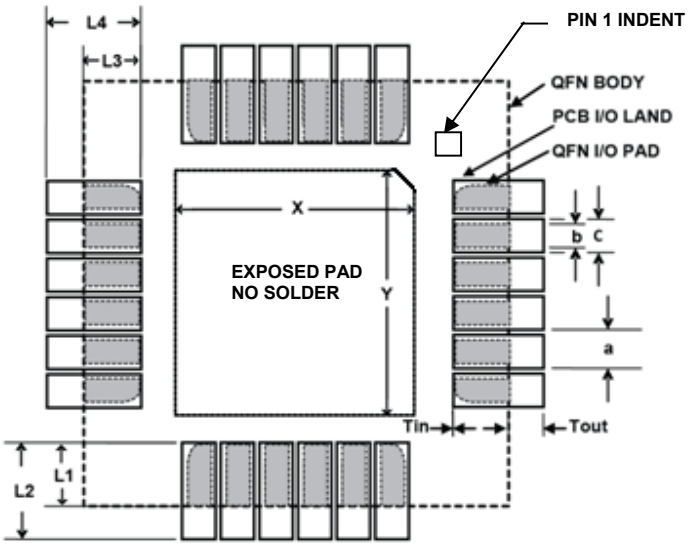
SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	——	0.20 REF.	——
D	3.90	4.00	4.10
D2	2.95	3.00	3.05
E	3.90	4.00	4.10
E2	2.75	2.80	2.85
e	——	0.50	——
L	0.30	0.35	0.40
L1	0.35	0.40	0.45
I	0.20	0.25	0.30
s	0.05	——	0.15
S1	0.15	0.20	0.25

11.2.2 PCB Design Guidelines

The Pad Diagram is shown in Figure 2 using a JEDEC type extension with solder rising on the outer edge. The Pad Dimensions Table shows pad sizing (mean dimensions) for the IMU-3000 product.



JEDEC type extension with solder rising on outer edge



Pad Diagram

Nominal Package I/O Pad Dimensions (mm)	
Pad Pitch (a)	0.50
Pad Width (b)	0.25
Pad Length (L1)	0.40
Pad Length (L3)	0.35
Exposed Pad Width (X)	2.80
Exposed Pad Length (Y)	3.00
I/O Land Design Dimensions Guidelines (mm)	
Land Width (c)	0.35
Outward Extension (Tout)	0.40
Inward Extension (Tin)	0.05
Land Length (L2)	0.80
Land Length (L4)	0.75

Pad Dimensions Table (for figure above)

InvenSense MEMS Gyros sense rate of rotation. In addition, gyroscopes sense mechanical stress coming from the PCB. This PCB stress is minimized with simple design rules:

1. Component Placement – Testing indicates that there are no specific design considerations other than generally accepted industry design practices for component placement near the IMU-3000 gyroscope to prevent noise coupling and thermo-mechanical stress.
2. The area below the MEMS gyro (on the same side of the board) must be defined as a keep-out area. It is strongly recommended to not place any structure in top metal layer underneath the keep-out area.
3. Traces connected to pads should be as much symmetric as possible. Symmetry and balance for pad connection will help component self alignment and will lead to better control of solder paste reduction after reflow.
4. Testing indicates that 3-Volt peak-to-peak signals run under the gyro package or directly on top of the package of frequencies from DC to 1MHz do not affect the operation of the MEMS gyro. However, routing traces or vias under the MEMS gyro package such that they run under the exposed die pad is prohibited.
5. To achieve best performance over temperature and to prevent thermo-mechanical package stress, do not place large insertion components like buttons, connectors, or shielding boxes at a distance of less than 6 mm from the MEMS gyro.

11.2.3 Exposed Die Pad Precautions

The IMU-3000 has very low active and standby current consumption. The exposed die pad is not required for heat sinking, and should not be soldered to the PCB since soldering to it contributes to performance changes due to package thermo-mechanical stress. There is no electrical connection between the pad and the die.

11.2.4 Gyro Removal from PCB

Never apply high mechanical force while removing MEMS gyros from PCB. Otherwise, the QFN package leads can be removed and failure analysis of the gyro unit will be impossible. Tweezers are practical.
Do not apply a pulling force upward. Instead apply a gentle force sideward while heating. When sufficient heat has been applied, the unit will start to slide sideways and can now be pulled gently upwards with the tweezers.
In any case, mechanical or thermo-mechanical overstress during manual handling and soldering, (especially contact between the soldering iron or hot air gun and the package) has to be avoided.
If safe removal of the suspected component is not possible or deemed too risky, send the whole PCB or the part of the PCB containing the defective component back to InvenSense. If requested, we will return the PCB after we have removed the gyro.

11.3 Trace Routing

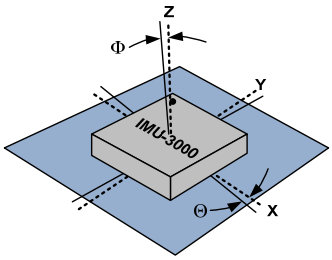
Testing indicates that 3-Volt peak-to-peak signals run under the gyro package or directly on top of the package of frequencies from DC to 1MHz do not affect the operation of the MEMS gyro. However, routing traces or vias under the MEMS gyro package such that they run under the exposed die pad is prohibited.

11.4 Component Placement

Do not place large insertion components such as keyboard or similar buttons, connectors, or shielding boxes at a distance of less than 6 mm from the MEMS gyro. Maintain generally accepted industry design practices for component placement near the IMU-3000 to prevent noise coupling and thermo-mechanical stress.

11.5 PCB Mounting and Cross-Axis Sensitivity

Orientation errors of the gyroscope mounted to the printed circuit board can cause cross-axis sensitivity in which one gyro responds to rotation about another axis, for example, the X-axis gyroscope responding to rotation about the Y or Z axes. The orientation mounting errors are illustrated in the figure below.



Package Gyro Axes (·····) Relative to PCB Axes (——) with Orientation Errors (Θ and Φ)

The table below shows the cross-axis sensitivity as a percentage of the specified gyroscope's sensitivity for a given orientation error.

Cross-Axis Sensitivity vs. Orientation Error

Orientation Error (θ or Φ)	Cross-Axis Sensitivity (sinθ or sinΦ)
0º	0%
0.5º	0.87%
1º	1.75%

The specification for cross-axis sensitivity in Section 3 includes the effect of the die orientation error with respect to the package.

11.6 MEMS Handling Instructions

MEMS (Micro Electro-Mechanical Systems) are a time-proven, robust technology used in hundreds of millions of consumer, automotive and industrial products. MEMS devices consist of microscopic moving mechanical structures. They differ from conventional IC products even though they can be found in similar packages. Therefore, MEMS devices require different handling precautions than conventional ICs prior to mounting onto printed circuit boards (PCBs).

The IMU-3000 gyroscope has a shock tolerance of 10,000*g*. InvenSense packages its gyroscopes as it deems proper for protection against normal handling and shipping. It recommends the following handling precautions to prevent potential damage.

- Individually packaged or trays of gyroscopes should not be dropped onto hard surfaces. Components placed in trays could be subject to *g*-forces in excess of 10,000*g* if dropped.
- Printed circuit boards that incorporate mounted gyroscopes should not be separated by manually snapping apart. This could also create *g*-forces in excess of 10,000*g.*

11.7 ESD Considerations

Establish and use ESD-safe handling precautions when unpacking and handling ESD-sensitive devices.

- The Tape-and-Reel moisture-sealed bag is an ESD approved barrier. The best practice is to keep the units in the original moisture sealed bags until ready for assembly.
- Restrict all device handling to ESD protected work areas that measure less than 200V static charge, or better, to less than 150V. Ensure that all workstations are properly grounded.
- Store ESD sensitive devices in ESD safe containers until ready for use.
- Ensure that personnel are properly grounded to prevent ESD.

11.8 Gyroscope Surface Mount Guidelines

Any material used in the surface mount assembly process of the MEMS gyroscope should be free of restricted RoHS elements or compounds. Pb-free solders should be used for assembly.

In order to assure gyroscope performance, several industry standard guidelines need to be considered for surface mounting. These guidelines are for both printed circuit board (PCB) design and surface mount assembly and are available from packaging and assembly houses.

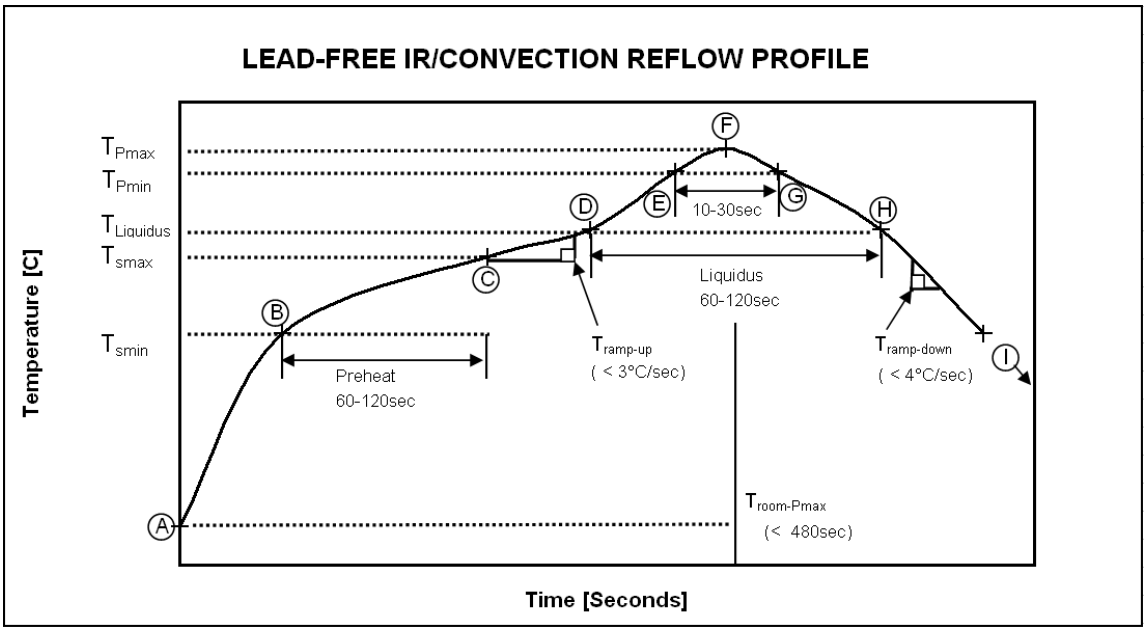
When using MEMS gyroscope components in plastic packages, package stress due to PCB mounting and assembly could affect the output offset and its value over a wide range of temperatures. This is caused by the mismatch between the Coefficient Temperature Expansion (CTE) of the package material and the PCB. Care must be taken to avoid package stress due to mounting.

11.9 Reflow Specification

The IMU-3000 gyroscope was qualified in accordance with IPC/JEDEC J-STD-020C. This standard classifies proper packaging, storage and handling to avoid subsequent thermal and mechanical damage during assembly solder reflow attachment. Classification specifies a bake cycle, moisture soak cycle in a temperature humidity oven, followed by three solder reflow cycles and functional testing for qualification. All temperatures refer to the topside of the QFN package, as measured on the package body surface. The peak solder reflow classification temperature requirement is (260 +5/-0°C) for lead-free soldering of components less than 1.6 mm thick.

Lower Production solder-reflow temperatures are recommended to use. Check the recommendations of the solder manufacturer. For optimum results, production solder reflow processes should use lower temperatures, reduce exposure to high temperatures, and use lower ramp-up and ramp-down rates than those listed in the qualification profile shown below.

Production reflow should never exceed the maximum constraints listed in the table and figure below for the qualification profile, as these represent the maximum tolerable ratings for the device.



Approved IR/Convection Solder Reflow Curve

Temperature Set Points for IR / Convection Reflow Corresponding to Figure Above

Step	Setting	CONSTRAINTS		
		Temp (°C)	Time (sec)	Rate (°C/sec)
A	Troom	25		
B	T_{Smin}	150		
C	T_{Smax}	200	$60 < t_{BC} < 120$	
D	$T_{Liquidus}$	217		$r_{(TLiquidus-TPmax)} < 3$
E	T_{Pmin} [255°C, 260°C]	255		$r_{(TLiquidus-TPmax)} < 3$
F	T_{Pmax} [260°C, 265°C]	260	$t_{AF} < 480$	$r_{(TLiquidus-TPmax)} < 3$
G	T_{Pmin} [255°C, 260°C]	255	$10 < t_{EG} < 30$	$r_{(TPmax-TLiquidus)} < 4$
H	$T_{Liquidus}$	217	$60 < t_{DH} < 120$	
I	T_{room}	25		

Note: T_{Pmax} must not exceed the Classification temperature (260°C).

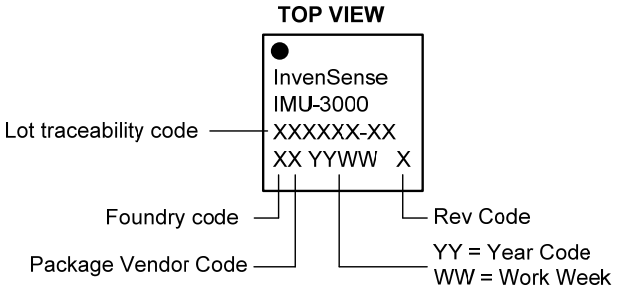
11.10 Storage Specifications

The storage specification of the IMU-3000 gyroscope conforms to IPC/JEDEC J-STD-020C Moisture Sensitivity Level (MSL) 3.

Storage Specifications for IMU-3000

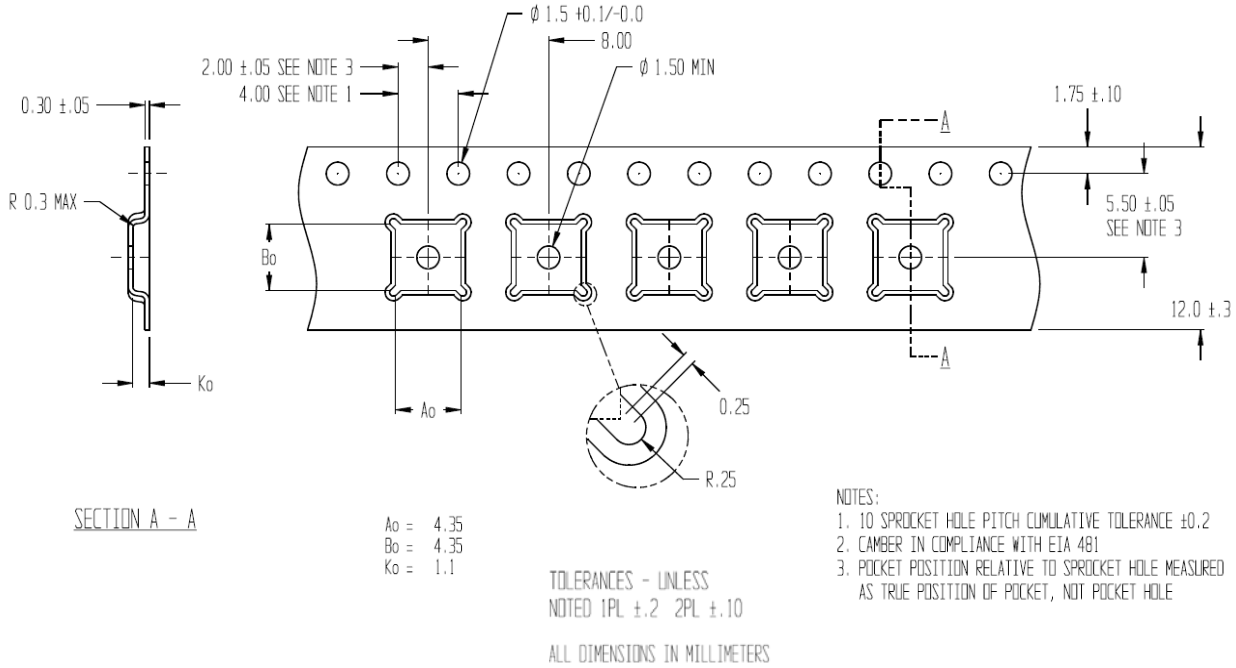
Calculated shelf-life in moisture-sealed bag	12 months -- Storage conditions: <40°C and <90% RH
After opening moisture-sealed bag	168 hours -- Storage conditions: ambient ≤30°C at 60% RH

11.11 Package Marking Specification

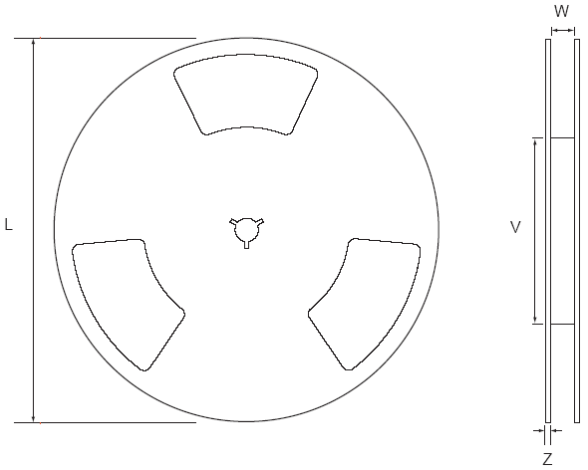


Package Marking Specification

11.12 Tape & Reel Specification



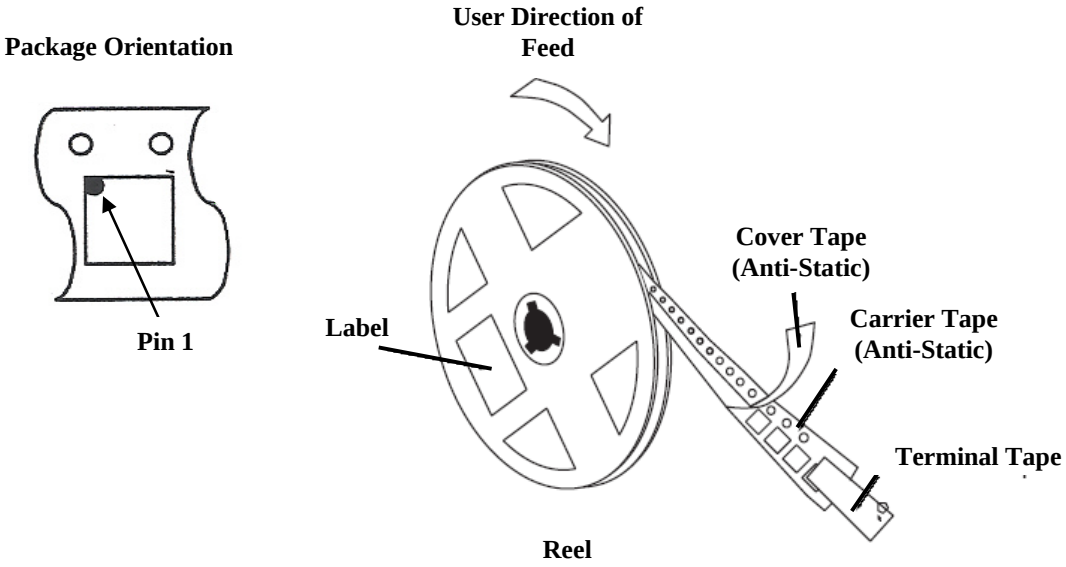
Tape Dimensions



Reel Outline Drawing

Reel Dimensions and Package Size

PACKAGE SIZE	REEL (mm)			
	L	V	W	Z
4x4	330	100	13.2	2.2

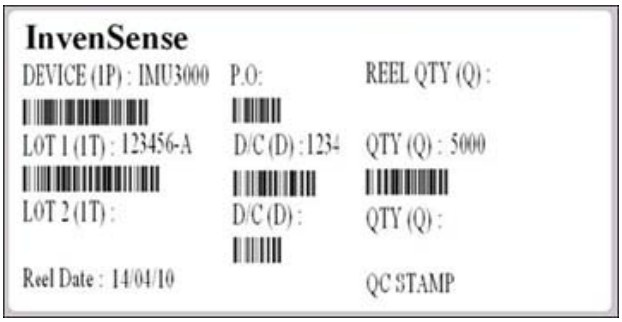


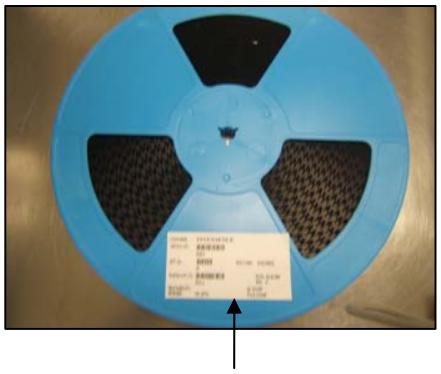
Tape and Reel Specification

Reel Specifications

Quantity Per Reel	5,000
Reels per Box	1
Boxes Per Carton (max)	3
Pieces per Carton (max)	15,000

11.13 Label





Location of Label

11.14 Packaging

Moisture Barrier Bag With Labels

Moisture-Sensitive Caution Label

Reel in Box

Box with Tape & Reel Label

12 Reliability

12.1 Qualification Test Policy

InvenSense's products complete a Qualification Test Plan before being released to production. The Qualification Test Plan follows the JEDEC 47D Standards, "Stress-Test-Driven Qualification of Integrated Circuits," with the individual tests described below.

12.2 Qualification Test Plan

Accelerated Life Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
High Temperature Operating Life (HTOL/LFR)	JEDEC JESD22-A108C, Dynamic, 3.63V biased, Tj>125°C [read-points 168, 500, 1000 hours]	3	77	(0/1)
Steady-State Temperature Humidity Bias Life (1)	JEDEC JESD22-A101C, 85°C/85%RH [read-points 168, 500 hours], Information Only 1000 hours]	3	77	(0/1)
High Temperature Storage Life	JEDEC JESD22-A103C, Cond. A, 125°C Non-Bias Bake [read-points 168, 500, 1000 hours]	3	77	(0/1)

Device Component Level Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
ESD-HBM	JEDEC JESD22-A114F, Class 2 (1.5KV)	1	3	(0/1)
ESD-MM	JEDEC JESD22-A115-A, Class B (200V)	1	3	(0/1)
Latch Up	JEDEC JESD78B Level 2, 125C, ±100mA	1	6	(0/1)
Mechanical Shock	JEDEC JESD22-B104C, Mil-Std-883, method 2002, Cond. D, 10,000*g's*, 0.3ms, ±X,Y,Z – 6 directions, 5 times/direction	3	5	(0/1)
Vibration	JEDEC JESD22-B103B, Variable Frequency (random), Cond. B, 5-500Hz, X,Y,Z – 4 times/direction	3	5	(0/1)
Temperature Cycling (1)	JEDEC JESD22-A104D Condition N, -40°C to +85°C, Soak Mode 2, 100 cycles	3	77	(0/1)

Board Level Tests

TEST	Method/Condition/	Lot Quantity	Sample / Lot	Acc / Reject Criteria
Board Mechanical Shock	JEDEC JESD22-B104C,Mil-Std-883, method 2002, Cond. D, 10,000*g's*, 0.3ms, +-X,Y,Z – 6 directions, 5 times/direction	1	5	(0/1)
Board T/C	JEDEC JESD22-A104D Condition N, -40°C to +85°C, Soak Mode 2, 100 cycles	1	40	(0/1)

(1) – Tests are preceded by MSL3 Preconditioning in accordance with JEDEC JESD22-A113F

13 Environmental Compliance

The IMU-3000 is RoHS and Green compliant.

The IMU-3000 is in full environmental compliance as evidenced in report HS-IMU-3000, Materials Declaration Data Sheet.

Environmental Declaration Disclaimer:
InvenSense believes this environmental information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

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LSM303DLH

Sensor module: 3-axis accelerometer and 3-axis magnetometer

Features

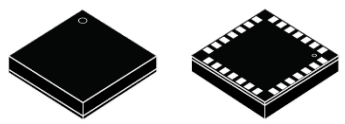
- Analog supply voltage: 2.5 V to 3.3 V
- Digital supply voltage IOs: 1.8 V
- Power-down mode
- 3 magnetic field channels and 3 acceleration channels
- ±1.3 to ±8,1 gauss magnetic field full-scale
- ±2 *g*/±4 *g*/±8 *g* dynamically selectable full-scale
- 16-bit data out
- I^2C serial interface
- 2 independent programmable interrupt generators for free-fall and motion detection
- Embedded self-test
- Accelerometer sleep-to-wakeup function
- 6D orientation detection
- ECOPACK® RoHS and "Green" compliant (see *Section 10*)

Applications

- Compensated compassing
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Intelligent power-saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LSM303DLH is a system-in-package featuring a 3D digital linear acceleration sensor



LGA-28L (5x5x1.0 mm)

and a 3D digital magnetic sensor. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are realized using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics. The LSM303DLH has a linear acceleration full-scale of ±2 *g* / ±4 *g* / ±8 *g* and a magnetic field full-scale of ±1.3 / ±1.9 / ±2.5 / ±4.0 / ±4.7 / ±5,6 / ±8.1 gauss, both fully selectable by the user. The LSM303DLH includes an I^2C serial bus interface that supports standard mode (100 kHz) and fast mode (400 kHz). The internal self-test capability allows the user to check the functioning of the whole module in the final application. The system can be configured to generate an interrupt signal by inertial wakeup/free-fall events, as well as by the position of the device itself. Thresholds and timing of interrupt generators are programmable on the fly by the end user. Magnetic and accelerometer parts can be enabled or put in power-down mode separately. The LSM303DLH is available in a plastic land grid array (LGA) package, and is guaranteed to operate over an extended temperature range from -30 to +85 °C.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packing
LSM303DLH	-30 to +85	LGA-28	Tray
LSM303DLHTR			Tape and reel

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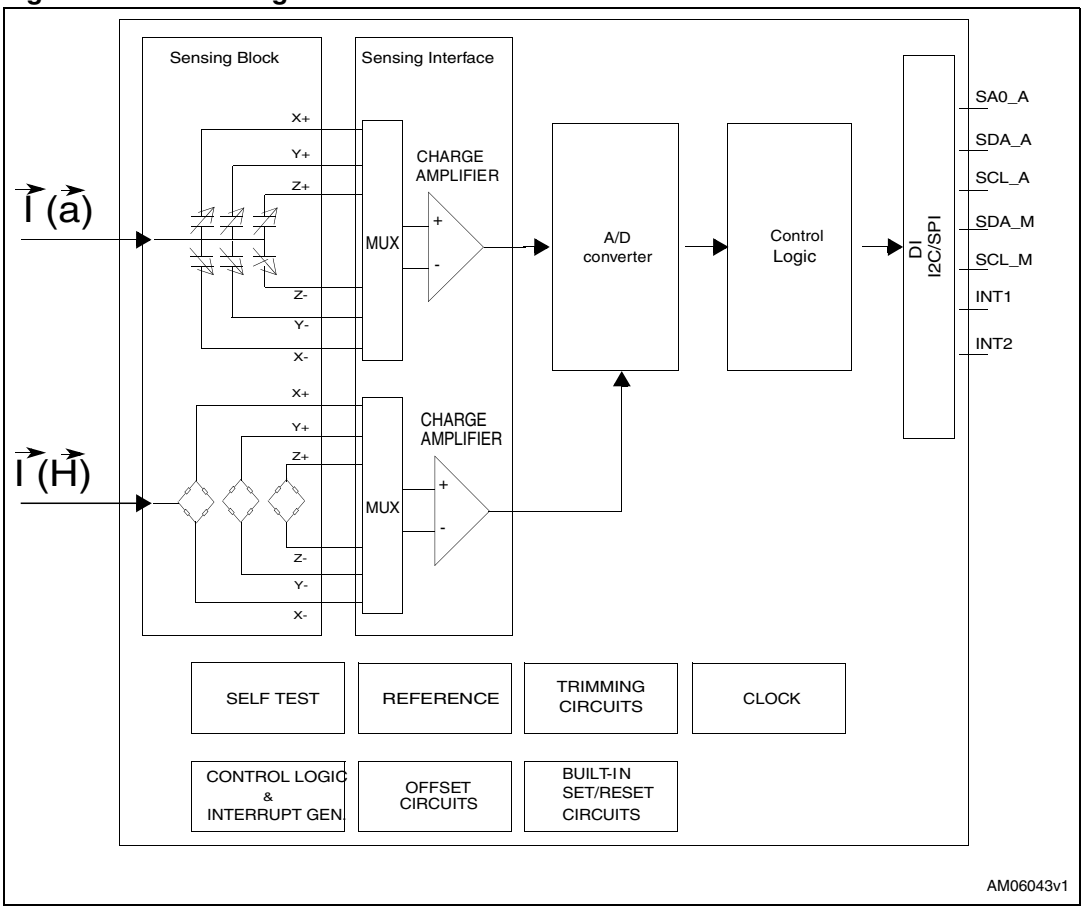
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

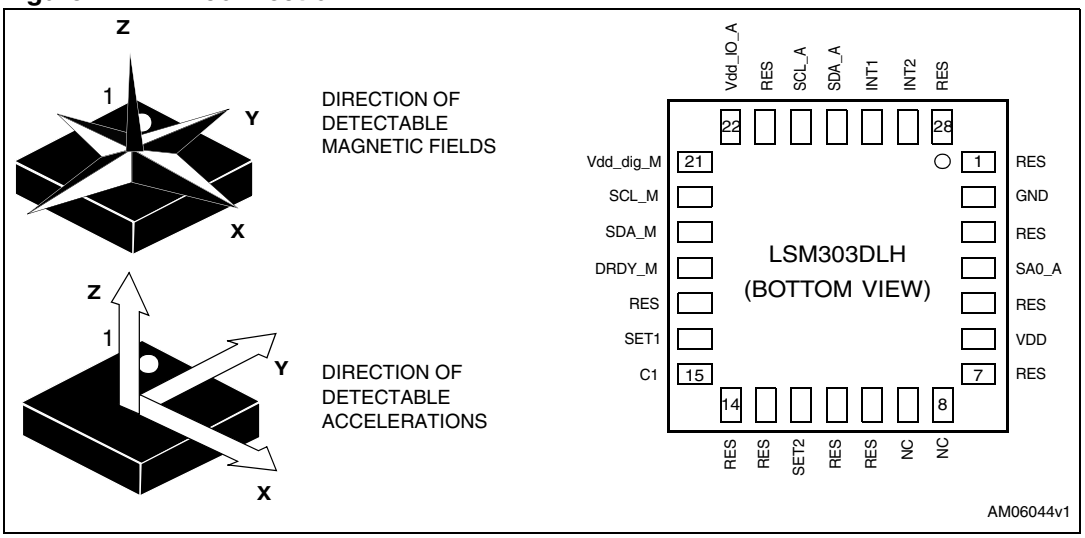


Table 2. Pin description

Pin#	Name	Function
1	Reserved	Connect to GND
2	GND	0 V supply
3	Reserved	Connect to GND
4	SA0_A	Linear acceleration signal I^2C less significant bit of the device address (SA0)
5	Reserved	To be connected to Vdd I^2C bus
6	Vdd	Power supply
7	Reserved	Connect to Vdd
8	NC	Not connected
9	NC	Not connected
10	Reserved	Leave unconnected
11	Reserved	Leave unconnected
12	SET2	S/R capacitor connection (C2)
13	Reserved	Leave unconnected
14	Reserved	Leave unconnected
15	C1	Reserved capacitor connection (C1)
16	SET1	S/R capacitor connection (C2)
17	Reserved	Connect to GND
18	DRDY_M	Magnetic signal interface data ready - test point
19	SDA_M	Magnetic signal interface I^2C serial data (SDA)
20	SCL_M	Magnetic signal interface I^2C serial clock (SCL)
21	Vdd_dig_M	Magnetic sensor digital power supply
22	Vdd_IO_A	Linear acceleration signal interface power supply for I/O pins
23	Reserved	Connect to Vdd_IO_A
24	SCL_A	Linear acceleration signal interface I^2C serial clock (SCL)
25	SDA_A	Linear acceleration signal interface I^2C serial data (SDA)
26	INT1	Inertial interrupt 1
27	INT2	Inertial interrupt 2
28	Reserved	Connect to GND

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[a]

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]	FS bit set to 00		±2.0		g
		FS bit set to 01		±4.0		
		FS bit set to 11		±8.0		
M_FS	Magnetic measurement range	GN bits set to 001		±1.3		gauss
		GN bits set to 010		±1.9		
		GN bits set to 011		±2.5		
		GN bits set to 100		±4.0		
		GN bits set to 101		±4.7		
		GN bits set to 110		±5.6		
		GN bits set to 111		±8.1		
LA_So	Linear acceleration sensitivity	FS bit set to 00 12 bit representation	0.9	1	1.1	m*g*/digit
		FS bit set to 01 12 bit representation	1.8	2	2.2	
		FS bit set to 11 12 bit representation	3.5	3.9	4.3	
M_GN	Magnetic gain setting	GN bits set to 001 (X,Y)		1055		LSB/ gauss
		GN bits set to 001 (Z)		950		
		GN bits set to 010 (X,Y)		795		
		GN bits set to 010 (Z)		710		
		GN bits set to 011 (X,Y)		635		
		GN bits set to 011 (Z)		570		
		GN bits set to 100 (X,Y)		430		
		GN bits set to 100 (Z)		385		
		GN bits set to 101 (X,Y)		375		
		GN bits set to 101 (Z)		335		
		GN bits set to 110 (X,Y)		320		
		GN bits set to 110 (Z)		285		
		GN bits set to 111[2] (X,Y)		230		
		GN bits set to 111[2] (Z)		205		

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.5 V to 3.3 V.

Table 3. Mechanical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_TCSo	Linear acceleration sensitivity change vs. temperature	FS bit set to 00		±0.01		%/°C
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy(3),(4)	FS bit set to 00		±20		m*g*
LA_TCOff	Linear acceleration zero-*g* level change vs temperature	Max delta from 25 °C		±0.1		m*g*/°C
LA_An	Acceleration noise density	FS bit set to 00		218		µ*g*/√Hz
LA_Vst	Linear acceleration self-test output change(5),(6),(7)	FS bit set to 00 X axis		300		LSb
		FS bit set to 00 Y axis		-300		LSb
		FS bit set to 00 Z axis		350		LSb
M_CAS	Magnetic cross-axis sensitivity	Cross field = 0.5 gauss Happlied = ±3 gauss		±1		%FS/ gauss
M_EF	Maximum exposed field	No permitting effect on zero reading			10000	gauss
M_ST	Magnetic self test	Positive bias mode, GN bits set to 100 on X, Y axis		270		LSB
		Positive bias mode, GN bits set to 100 on Z axis		255		LSB
M_R	Magnetic resolution	Vdd = 3 V		8		mgauss
M_DF	Disturbing field	Sensitivity starts to degrade. User S/R pulse to restore sensitivity			20	gauss
Top	Operating temperature range		-30		+85	°C

1. Typical specifications are not guaranteed
2. Verified by wafer level test and measurement of initial offset and sensitivity
3. Typical zero-*g* level offset value after MSL3 preconditioning
4. Offset can be eliminated by enabling the built-in high-pass filter
5. The sign of “Self-test output change” is defined by the CTRL_REG4 STsign bit (*Table 29*), for all axes.
6. Self-test output changes with the power supply. “Self-test output change” is defined as $OUTPUT[LSb]_{(CTRL_REG4\ ST\ bit=1)} - OUTPUT[LSb]_{(CTRL_REG4\ ST\ bit=0)}$. 1LSb=4*g*/4096 at 12bit representation, ±2 *g* full-scale
7. Output data reach 99% of final value after 1/ODR+1ms when enabling self-test mode, due to device filtering

2.2 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.5		3.3	V
Vdd_IO_A	Accelerometer module power supply for I/O		1.71	1.8	Vdd+0.1	V
Vdd_dig_M	Magnetic module digital power supply		1.71	1.8	2.0	V
Vdd I2C Bus	Magnetic module I^2C bus power supply		1.71	1.8	Vdd+0.1	V
Idd	Current consumption in normal mode(2)			0.83		mA
IddPdn	Current consumption in power-down mode	T = 25°C		3		µA
Top	Operating temperature range		-30		+85	°C

1. Typical specifications are not guaranteed.
2. Magnetic sensor setting ODR = 7.5 Hz. Accelerometer sensor ODR = 50 Hz.

2.3 Communication interface characteristics

2.3.1 Accelerometer sensor I²C - inter IC control interface

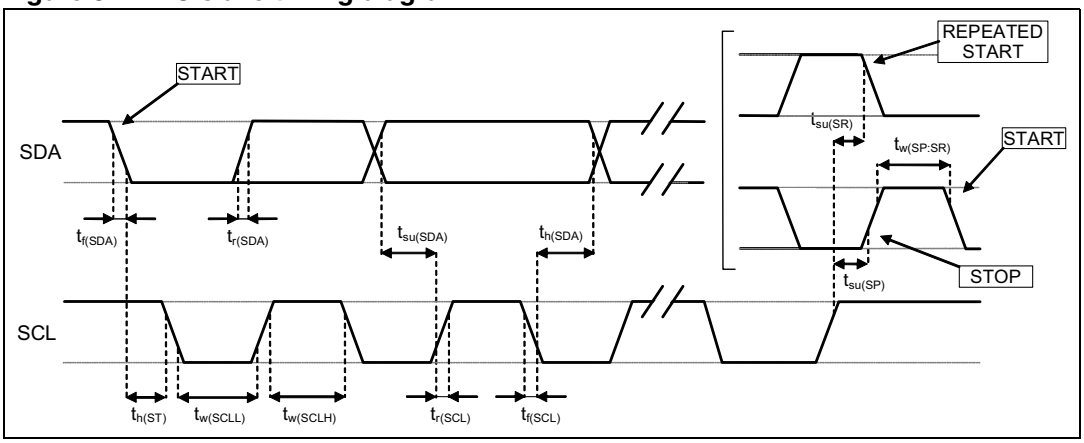
Subject to general operating conditions for Vdd and top.

Table 5. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	KHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	ns
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		µs
$t_{su(SP)}$	STOP condition setup time	4		0.6		µs
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		µs

1. Data based on standard I²C protocol requirement, not tested in production.
2. Cb = total capacitance of one bus line, in pF.

Figure 3. I²C slave timing diagram (b)



b. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both port.

2.3.2 Magnetic field sensing I^2C digital interface

This magnetic sensor IC has a 7-bit serial address and supports I^2C protocols with standard and fast modes (100 kHz and 400 kHz, respectively), but does not support high-speed mode (Hs).

External pull-up resistors are required to support the standard and fast modes. Depending on the application, the internal pull-ups may be used to support slower data speeds than specified by I^2C standards.

This device does not contain 50 ns spike suppression, as required by fast mode operation in the I^2C bus specification.

Activities required by the master (register read and write) have priority over internal activities, such as measurement. The purpose of this priority is to prevent the master waiting and the I^2C bus being engaged for longer than necessary.

3 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vin	Input voltage on any control pin (SCL, SDA)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
T_{OP}	Operating temperature range	-30 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C

This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part.

This is an ESD sensitive device, improper handling can cause permanent damages to the part.

4 Terminology

4.1 Linear acceleration sensitivity

Linear acceleration sensitivity describes the gain of the accelerometer sensor and can be determined e.g. by applying 1 *g* acceleration to it. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, a ±1 g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

4.2 Zero-*g* level

Zero-*g* level Offset (LA_TyOff) describes the deviation of an actual output signal from the ideal output signal if no linear acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 g on both the X and Y axes, whereas the Z axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature; see "Linear acceleration zero-*g* level change vs temperature" (LA_TCOff) in *Table 3.* The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a group of sensors.

4.3 Sleep-to-wakeup

The "sleep-to-wakeup" function, in conjunction with low-power mode, allows further reduction of system power consumption and the development of new smart applications. The LSM303DLH may be set to a low-power operating mode, characterized by lower date rate refreshing. In this way the device, even if sleeping, continues sensing acceleration and generating interrupt requests.

When the sleep-to-wakeup function is activated, the LSM303DLH is able to automatically wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth. With this feature the system may be efficiently switched from low-power mode to full-performance depending on user-selectable positioning and acceleration events, thus ensuring power-saving and flexibility.

5 Functionality

The LSM303DLH is a system-in-package featuring a 3D digital linear acceleration and 3D digital magnetic field detection sensor.

The system includes specific sensing elements and an IC interfaces capable of measuring both the linear acceleration and magnetic field applied to it, and to provide a signal to the external world through an I^2C serial interface with separated digital ouput.

The sensing system is manufactured using specialized micromachining processes, while the IC interfaces are realized using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM303DLH features two data-ready signals (RDY) which indicate when a new set of measured acceleration data and magnetic data are available, thus simplifying data synchronization in the digital system that uses the device.

The LSM303DLH may also be configured to generate an inertial *wakeup* and *free-fall* interrupt signal according to a programmed acceleration event along the enabled axes. Both free-fall and wakeup can be used simultaneously on two different accelerometer interrupts.

5.1 Factory calibration

The IC interface is factory calibrated for linear acceleration sensitivity (LA_So), and linear acceleration Zero-*g* level (LA_TyOff).

The trimming values are stored inside the device in non-volatile memory. When the device is turned on, the trimming parameters are downloaded into the registers to be used during normal operation. This allows the use of the device without further calibration.

5.2 Linear acceleration self-test operation

Self-test allows the checking of sensor functionality without moving it. The self-test function is off when the self-test bit (ST) of CTRL_REG4_A (control register 4) is programmed to ‘0‘. When the self-test bit of CTRL_REG4_A is programmed to ‘1‘ an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full-scale through the device sensitivity. When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

5.3 Magnetic self-test operation

To check the magnetic sensor for proper operation, a self-test feature is incorporated in which the sensor offset straps are excited to create a nominal field strength (bias field) to be measured. To implement this self-test, the least significant bits (MS1 and MS0) of configuration register A are changed from 00 to 01 (0x12 or 0b000xxx01).

By placing the mode register into single-conversion mode (0x01), two data acquisition cycles are made on each magnetic vector.

The first acquisition is a set pulse followed shortly by measurement data of the external field. The second acquisition has the offset strap excited in the positive bias mode to create about a 0.6 *gauss* self-test field plus the external field. The first acquisition values are subtracted from the second acquisition, and the net measurement is placed into the data output registers.

To leave self-test mode, change the MS1 and MS0 bits of the configuration register A back to 0x00. Also, change the mode register if single-conversion mode is not the intended next mode of operation.

Table 7. Magnetic ST (positive bias)

Symbol	GN bits setting	Test axis	Min.	Typ.(1)	Max.	Unit
ST_M	GN bits set to 001	X,Y axis		655		LSB
		Z axis		630		
	GN bits set to 010	X,Y axis		495		
		Z axis		470		
	GN bits set to 011	X,Y axis		395		
		Z axis		375		
	GN bits set to 100	X,Y axis		270		
		Z axis		255		
	GN bits set to 101	X,Y axis		235		
		Z axis		225		
	GN bits set to 110	X,Y axis		200		
		Z axis		190		
	GN bits set to 111(2)	X,Y axis		140		
		Z axis		135		

1. Typical specifications are not guaranteed

6 Application hints

Figure 4. LSM303DLH electrical connection 1 - recommended for I²C fast mode

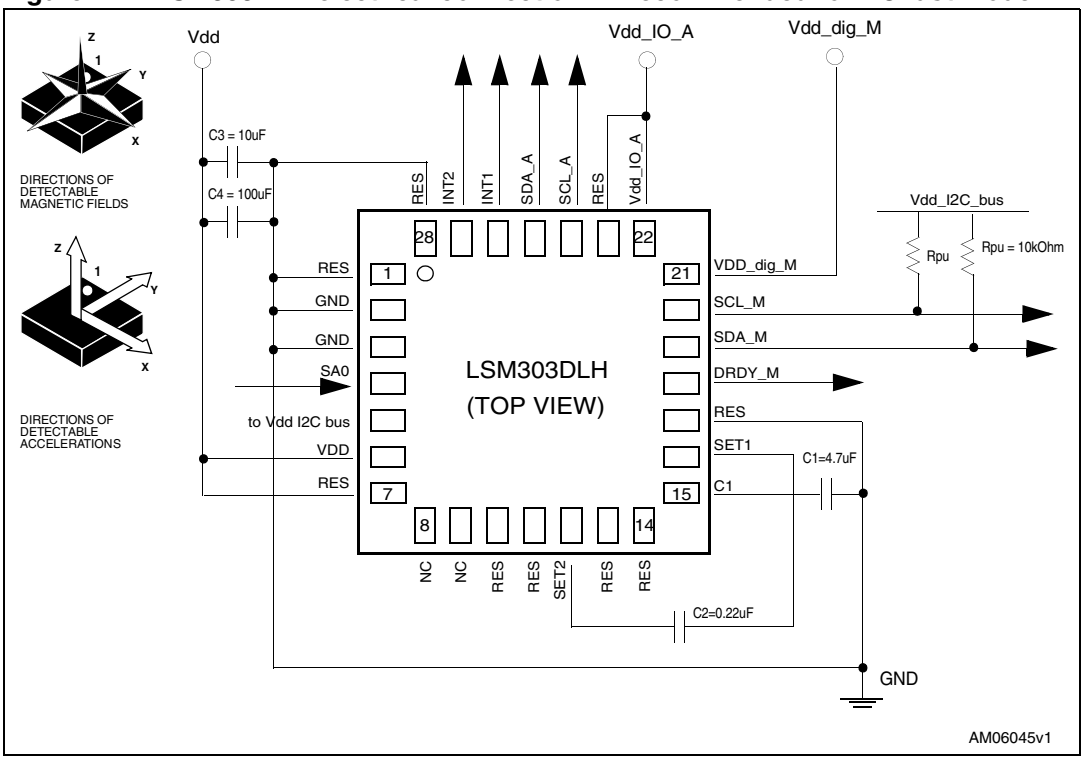
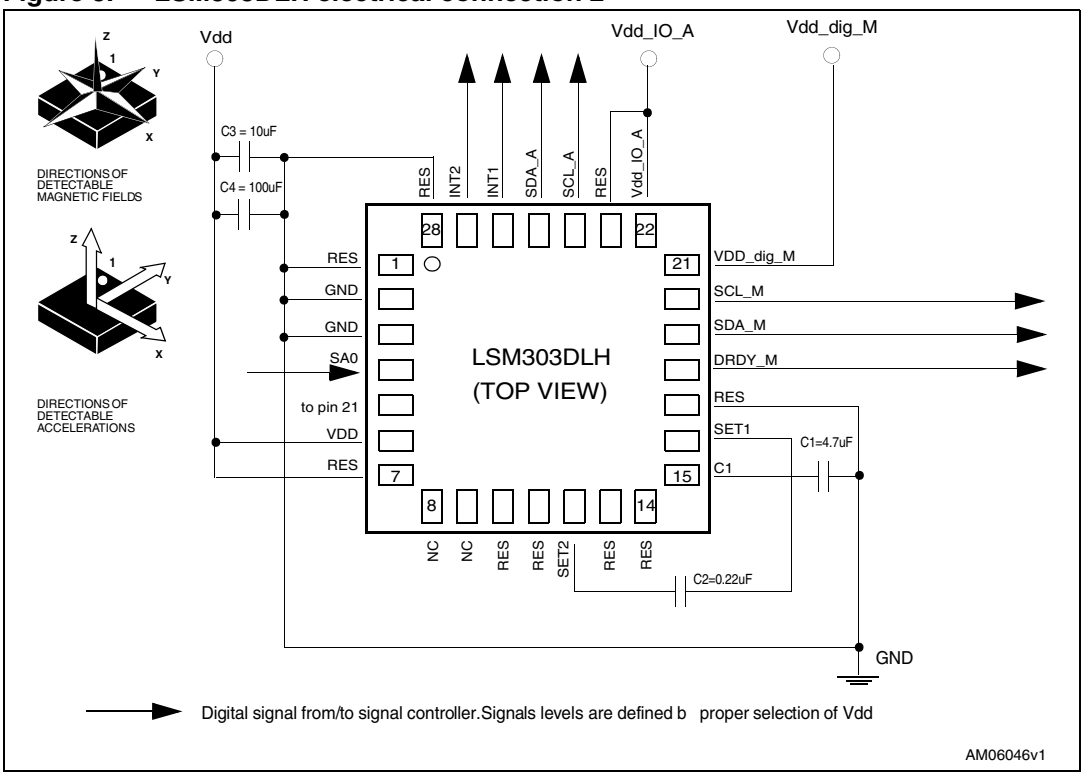


Figure 5. LSM303DLH electrical connection 2



6.1 External capacitors

The C1 and C2 external capacitors should have a low SR value ceramic type construction. Reservoir capacitor C1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C2 nominally 0.22 µF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C4=100 *nF* ceramic, C3=10 *µF* Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to obtain proper behavior of the IC (refer to *Figure 4*).

The functionality of the device and the measured acceleration/magnetic field data is selectable and accessible through the I^2C interface.

The functions, the threshold and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I^2C interface.

6.2 Pull-up resistors

Pull-up resistors are placed on the two I^2C bus lines.

6.3 Digital interface power supply

This digital interface dedicated to the linear acceleration signal is capable of operating with a standard power supply (Vdd) or using a dedicated power supply (Vdd_IO_A).

This digital interface dedicated to the magnetic field signal requires a dedicated power supply (Vdd_dig_M).

The table below shows the modes available in the various power supply conditions.

Table 8. Operational mode and power supply for magnetic field sensing

Vdd_dig_M	Vdd	Mode supported	Description
High	High	All except off	Digital I/O pins: range from GND to Vdd_I2C_bus / Vdd_dig_M. Device fully functional. Digital logic blocks are powered from Vdd_dig_M supply, including all onboard clocks.
High	Low	Power down	Digital I/O pins: range from GND to Vdd_I2C_bus / Vdd_dig_M. Device measurement functionality not supported. Device I^2C bus and register access supported.

6.4 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/

6.5 High current wiring effects

High current in wiring and printed circuit traces can be the cause of errors in magnetic field measurements for compassing.

Conducto-generated magnetic fields add to earth's magnetic field, creating errors in compass heading computation.

Keep currents that are higher than 10 mA a few millimeters further away from the sensor IC.

7 Digital interfaces

The registers embedded inside the LSM303DLH are accessible through two separate I^2C serial interfaces: one for the accelerometer core and the other for the magnetometer core. The two interfaces can be connected together on the PCB.

Table 9. Serial interface pin description

Pin name	Pin description
SCL_A	I^2C serial clock (SCL) for accelerometer
SDA_A	I^2C serial data (SDA) for accelerometer
SCL_M	I^2C serial clock (SCL) for magnetometer
SDA_M	I^2C serial data (SDA) for magnetometer

7.1 I^2C serial interface

The LSM303DLH I^2C is a bus slave. The I^2C is employed to write the data into the registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 10. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface.

7.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the 8th bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM303DLH behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto-increment. If the MSb of the SUB field is ‘1’, the SUB (register address) is automatically increased to allow multiple data read/write.

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing a real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

7.1.2 Linear acceleration digital interface

For linear acceleration, the default (factory) 7-bit slave address is 001100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b) otherwise if the SA0 pad is connected to ground, LSb value is '0' (address 0011000b). This solution permits connecting and addressing two different accelerometers to the same I^2C lines.

The slave address is completed with a read/write bit. If the bit was '1' (read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with direction unchanged. *Table 14* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 14. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format , MAK is Master Acknowledge and NMAK is No Master Acknowledge.

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD +W		SUB		SR	SAD +R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

7.1.3 Magnetic field digital interface

The system communicates via a two-wire I^2C bus system as a slave device. The interface protocol is defined by the I^2C bus specification. The data rate is the standard mode 100 kbps or 400 kbps rates as defined by the I^2C bus specifications. The bus bit format is an 8-bit data/address send and a 1-bit acknowledge bit. The format of the data bytes (payload) shall be case-sensitive ASCII characters or binary data to the magnetic sensor slave, and binary data returned. Negative binary values will be in two's complement form.

For magnetic sensor, the default (factory) 7-bit slave address is 0011110b (0x3C) for write operations, or 00111101b (0x3D) for read operations.

The Serial Clock (SCL_M) and Serial Data (SDA_M) lines have optional internal pull-up resistors, but require resistive pull-up (Rp) between the master device (usually a host microprocessor) and the LSM303DLH. Pull-up resistance values of about 10 kΩ are recommended with a nominal 1.8 V digital supply voltage (Vdd_dig_M).

The SCL_M and SDA_M lines in this bus specification can be connected to a host of devices. The bus can be a single master to multiple slaves, or it can be a multiple master configuration. All data transfers are initiated by the master device which is responsible for generating the clock signal, and the data transfers are 8 bits long. All devices are addressed by the unique 7-bit address of the I^2C. After each 8-bit transfer, the master device generates a 9th clock pulse, and releases the SDA_M line.

The receiving device (addressed slave) pulls the SDA_M line low to acknowledge (ACK) the successful transfer, or leaves the SDA_M high to negative acknowledge (NACK). As per the I^2C specification, all transitions in the SDA_M line must occur when SCL_M is low. This requirement leads to two unique conditions on the bus associated with the SDA_M transitions when SCL_M is high. The master device pulling the SDA line low while the SCL_M line is high indicates the Start (S) condition, while the Stop (P) condition is indicated by the SDA_M line pulled high while the SCL_M line is high. The I^2C protocol also allows for the Restart condition, in which the master device issues a second start condition without issuing a stop.

All bus transactions begin with the master device issuing the start sequence followed by the slave address byte. The address byte contains the slave address; the upper 7 bits (bits7-1), and the least significant bit (LSb). The LSb of the address byte designates if the operation is a read (LSb=1) or a write (LSb=0). At the 9th clock pulse, the receiving slave device issues the ACK (or NACK). Following these bus events, the master sends data bytes for a write operation, or the slave clocks out data with a read operation. All bus transactions are terminated with the master issuing a stop sequence.

I^2C bus control can be implemented with either hardware logic or in software. Typical hardware designs release the SDA_M and SCL_M lines as appropriate to allow the slave device to manipulate these lines. In a software implementation, care must be taken to perform these tasks in code.

Table 16. SAD+Read/Write patterns

Command	SAD[6:0]	R/W	SAD+R/W
Read	0011110	1	00111101 (3Dh)
Write	0011110	0	00111100 (3Ch)

Magnetic signal interface reading/writing

The interface uses an address pointer to indicate which register location is to be read from or written to. These pointer locations are sent from the master to this slave device and succeed the 7-bit address plus 1 bit read/write identifier.

To minimize the communication between the master and magnetic digital interface of the LSM303DLH, the address pointer is updated automatically without master intervention.

This automatic address pointer update has two additional features. First, when address 12 or higher is accessed the pointer updates to address 00, and secondly when address 09 is reached, the pointer rolls back to address 03. Logically, the address pointer operation functions as shown below.

- if address pointer = 09, then address pointer = 03
- while if address pointer $\geq$12, then address pointer = 0
- while address pointer = address pointer + 1
- the address pointer value itself cannot be read via the I^2C bus.

Any attempt to read an invalid address location returns 0's, and any write to an invalid address location or an undefined bit within a valid address location is ignored by this device.

8 Register mapping

The tables given below provide a listing of the 8-bit registers embedded in the device and the related addresses:

Table 17. Register address map

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
Reserved (do not modify)			00 - 1F			Reserved
CTRL_REG1_A	TAB.13	rw	20	010 0000	00000111	
CTRL_REG2_A	TAB.13	rw	21	010 0001	00000000	
CTRL_REG3_A	TAB.13	rw	22	010 0010	00000000	
CTRL_REG4_A	TAB.13	rw	23	010 0011	00000000	
CTRL_REG5_A	TAB.13	rw	24	010 0100	00000000	
HP_FILTER_RESET_A	TAB.13	r	25	010 0101		Dummy register
REFERENCE_A	TAB.13	rw	26	010 0110	00000000	
STATUS_REG_A	TAB.13	r	27	010 0111	00000000	
OUT_X_L_A	TAB.13	r	28	010 1000	output	
OUT_X_H_A	TAB.13	r	29	010 1001	output	
OUT_Y_L_A	TAB.13	r	2A	010 1010	output	
OUT_Y_H_A	TAB.13	r	2B	010 1011	output	
OUT_Z_L_A	TAB.13	r	2C	010 1100	output	
OUT_Z_H_A	TAB.13	r	2D	010 1101	output	
Reserved (do not modify)			2E - 2F			Reserved
INT1_CFG_A	TAB.13	rw	30	011 0000	00000000	
INT1_SOURCE_A	TAB.13	r	31	011 0001	00000000	
INT1_THS_A	TAB.13	rw	32	011 0010	00000000	
INT1_DURATION_A	TAB.13	rw	33	011 0011	00000000	
INT2_CFG_A	TAB.13	rw	34	011 0100	00000000	
INT2_SOURCE_A	TAB.13	r	35	011 0101	00000000	
INT2_THS_A	TAB.13	rw	36	011 0110	00000000	
INT2_DURATION_A	TAB.13	rw	37	011 0111	00000000	
Reserved (do not modify)			38 - 3F			Reserved
CRA_REG_M	TAB.15	rw	00	00000000	00010000	
CRB_REG_M	TAB.15	rw	01	00000001	00100000	
MR_REG_M	TAB.15	rw	02	00000010	00000011	
OUT_X_H_M	TAB.15	r	03	00000011	output	

Table 17. Register address map (continued)

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
OUT_X_L_M	TAB.15	r	04	00000100	output	
OUT_Y_H_M	TAB.15	r	05	00000101	output	
OUT_Y_L_M	TAB.15	r	06	00000110	output	
OUT_Z_H_M	TAB.15	r	07	00000111	output	
OUT_Z_L_M	TAB.15	r	08	00001000	output	
SR_REG_Mg	TAB.15	r	09	00001001	00000000	
IRA_REG_M	TAB.15	r	0A	00001010	01001000	
IRB_REG_M	TAB.15	r	0B	00001011	00110100	
IRC_REG_M	TAB.15	r	0C	00001100	00110011	

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibrated values. Their content is automatically restored when the device is powered up.

9 Registers description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The register address, composed of 7 bits, is used to identify them and to write the data through the serial interface.

9.1 Linear acceleration register

For linear acceleration sensors, the default (factory) 7-bit slave address is 001100xb.

9.1.1 CTRL_REG1_A (20h)

Table 18. CTRL_REG1_A register

PM2	PM1	PM0	DR1	DR0	Zen	Yen	Xen

Table 19. CTRL_REG1_A description

PM2 - PM0	Power mode selection. Default value: 000 (000: Power-down; Others: refer to *Table 20*)
DR1, DR0	Data rate selection. Default value: 00 (00:50 Hz; others: refer to *Table 21*)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

PM bits allow selection between power-down and two operating active modes. The device is in power-down mode when the PD bits are set to “000” (default value after boot). *Table 20* shows all the possible power mode configurations and respective output data rates. Output data in the low-power modes are computed with a low-pass filter cut-off frequency defined by DR1, DR0 bits.

DR bits, in the normal-mode operation, select the data rate at which acceleration samples are produced. In low-power mode they define the output data resolution. *Table 21* shows all the possible configurations for the DR1 and DR0 bits.

Table 20. Power mode and low-power output data rate configurations

PM2	PM1	PM0	Power mode selection	Output data rate [Hz] ODR_{LP}
0	0	0	Power-down	--
0	0	1	Normal mode	ODR

Table 20. Power mode and low-power output data rate configurations (continued)

PM2	PM1	PM0	Power mode selection	Output data rate [Hz] ODR_{LP}
0	1	0	Low-power	0.5
0	1	1	Low-power	1
1	0	0	Low-power	2
1	0	1	Low-power	5
1	1	0	Low-power	10

Table 21. Normal-mode output data rate configurations and low-pass cut-off frequencies

DR1	DR0	Output data rate [Hz] ODR	Low-pass filter cut-off frequency [Hz]
0	0	50	37
0	1	100	74
1	0	400	292
1	1	1000	780

9.1.2 CTRL_REG2_A (21h)

Table 22. CTRL_REG2_A register

BOOT	HPM1	HPM0	FDS	HPen2	HPen1	HPCF1	HPCF0

Table 23. CTRL_REG2_A description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
HPM1, HPM0	High-pass filter mode selection. Default value: 00 (00: normal mode; Others: refer to *Table 24*)
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register)
HPen2	High-pass filter enabled for interrupt 2 source. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPen1	High-pass filter enabled for interrupt 1 source. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPCF1, HPCF0	High-pass filter cut-off frequency configuration. Default value: 00 (00: HPc=8; 01: HPc=16; 10: HPc=32; 11: HPc=64)

The **BOOT** bit is used to refresh the content of internal registers stored in the Flash memory block. At device power-up, the content of the Flash memory block is transferred to the

internal registers related to trimming functions to permit good device behavior. If, for any reason, the content of the trimming registers was changed, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to ‘1’ the content of internal Flash is copied to the corresponding internal registers and is used to calibrate the device. These values are factory-trimmed and are different for every accelerometer. They permit good device behavior and normally do not have to be modified. At the end of the boot process, the BOOT bit is again set to ‘0’.

Table 24. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode (reset reading HP_RESET_FILTER)

HPCF[1:0]. These bits are used to configure the high-pass filter cut-off frequency f_t,which is given by:

$$f_t = \ln\left(1 - \frac{1}{HPc}\right) \cdot \frac{f_s}{2\pi}$$

The equation can be simplified to the following approximated equation:

$$f_t = \frac{f_s}{6 \cdot HPc}$$

Table 25. High-pass filter cut-off frequency configuration

HPcoeff2,1	f_t [Hz] Data rate = 50 Hz	f_t [Hz] Data rate = 100 Hz	f_t [Hz] Data rate = 400 Hz	f_t [Hz] Data rate = 1000 Hz
00	1	2	8	20
01	0.5	1	4	10
10	0.25	0.5	2	5
11	0.125	0.25	1	2.5

9.1.3 CTRL_REG3_A (22h)

Table 26. CTRL_REG3_A register

IHL	PP_OD	LIR2	I2_CFG1	I2_CFG0	LIR1	I1_CFG1	I1_CFG0

Table 27. CTRL_REG3_A description

IHL	Interrupt active high, low. Default value: 0 (0: active high; 1:active low)
PP_OD	Push-pull/open drain selection on interrupt pad. Default value 0. (0: push-pull; 1: open drain)
LIR2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
I2_CFG1, I2_CFG0	Data signal on INT 2 pad control bits. Default value: 00. (see table below)
LIR1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
I1_CFG1, I1_CFG0	Data signal on INT 1 pad control bits. Default value: 00. (see table below)

Table 28. Data signal on INT 1 and INT 2 pad

I1(2)_CFG1	I1(2)_CFG0	INT 1(2) Pad
0	0	Interrupt 1 (2) source
0	1	Interrupt 1 source OR interrupt 2 source
1	0	Data ready
1	1	Boot running

9.1.4 CTRL_REG4_A (23h)

Table 29. CTRL_REG4_A register

BDU	BLE	FS1	FS0	STsign	0	ST	---

Table 30. CTRL_REG4_A description

BDU	Block data update. Default value: 0 (0: continuos update; 1: output registers not updated between MSB and LSB reading)
BLE	Big/little endian data selection. Default value 0. (0: data LSB @ lower address; 1: data MSB @ lower address)
FS1, FS0	Full-scale selection. Default value: 00. (00: ±2 *g*; 01: ±4 *g*; 11: ±8 *g*)
STsign	Self-test sign. Default value: 00. (0: self-test plus; 1 self-test minus)
ST	Self-test enable. Default value: 0. (0: self-test disabled; 1: self-test enabled)

The **BDU** bit is used to inhibit output register updates between the reading of the upper and lower register parts. In default mode (BDU = ‘0’), the lower and upper register parts are updated continuously. If it is not certain to read faster than output data rate, it is recommended to set BDU bit to ‘1’. In this way, after the reading of the lower (upper) register part, the content of that output register is not updated until the upper (lower) part is read also. This feature avoids reading LSB and MSB related to different samples.

9.1.5 CTRL_REG5_A (24h)

Table 31. CTRL_REG5_A register

0	0	0	0	0	0	TurnOn1	TurnOn0

Table 32. CTRL_REG5_A description

TurnOn1, TurnOn0	Turn-on mode selection for sleep-to-wake function. Default value: 00.

TurnOn bits are used for turning on the **sleep-to-wake** function.

Table 33. Sleep-to-wake configuration

TurnOn1	TurnOn0	Sleep-to-wake status
0	0	Sleep-to-wake function is disabled
1	1	Turned on: The device is in low-power mode (ODR is defined in CTRL_REG1_A)

By setting the TurnOn [1:0] bits to 11, the “sleep-to-wake” function is enabled. When an interrupt event occurs, the device goes into normal mode, increasing the ODR to the value defined in CTRL_REG1_A. Although the device is in normal mode, CTRL_REG1_A content is not automatically changed to “normal mode” configuration.

9.1.6 HP_FILTER_RESET_A (25h)

Dummy register. Reading at this address instantaneously zeroes the content of the internal high-pass filter. If the high-pass filter is enabled, all three axes are instantaneously set to 0 *g*. This makes it possible to surmount the settling time of the high-pass filter.

9.1.7 REFERENCE_A (26h)

Table 34. REFERENCE_A register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 35. REFERENCE_A description

Ref7 - Ref0	Reference value for high-pass filter. Default value: 00h.

This register sets the acceleration value taken as a reference for the high-pass filter output.

When the filter is turned on (at least one FDS, HPen2, or HPen1 bit is equal to ‘1’) and HPM bits are set to “01”, filter out is generated taking this value as a reference.

9.1.8 STATUS_REG_A(27h)

Table 36. STATUS_REG_A register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 37. STATUS_REG_A description

ZYXOR	X, Y and Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous one before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous one)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous one)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous one)
ZYXDA	X, Y and Z axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

9.1.9 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data. The value is expressed as two’s complement.

9.1.10 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data. The value is expressed as two’s complement.

9.1.11 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data. The value is expressed as two’s complement.

9.1.12 INT1_CFG_A (30h)

Table 38. INT1_CFG_A register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 39. INT1_CFG_A description

AOI	AND/OR combination of interrupt events. Default value: 0. (See *Table 40*)
6D	6 direction detection function enable. Default value: 0. (See *Table 40*)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Configuration register for Interrupt 1 source.

Table 40. Interrupt 1 source configurations

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6 direction movement recognition
1	0	AND combination of interrupt events
1	1	6 direction position recognition

9.1.13 INT1_SRC_A (31h)

Table 41. INT1_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 42. INT1_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 1 source register. Read-only register.

Reading at this address clears INT1_SRC_A IA bit (and the interrupt signal on INT 1 pin) and allows the refreshing of data in the INT1_SRC_A register if the latched option was chosen.

9.1.14 INT1_THS_A (32h)

Table 43. INT1_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 44. INT1_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

9.1.15 INT1_DURATION_A (33h)

Table 45. INT1_DURATION_A register

0	D6	D5	D4	D3	D2	D1	D0

Table 46. INT2_DURATION_A description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

9.1.16 INT2_CFG_A (34h)

Table 47. INT2_CFG_A register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 48. INT2_CFG_A description

AOI	AND/OR combination of interrupt events. Default value: 0. (See table below)
6D	6 direction detection function enable. Default value: 0. (See table below)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Configuration register for Interrupt 2 source.

Table 49. Interrupt mode configuration

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6 direction movement recognition
1	0	AND combination of interrupt events
1	1	6 direction position recognition

9.1.17 INT2_SRC_A (35h)

Table 50. INT2_SRC_A register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 51. INT2_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X Low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 2 source register. Read-only register.

Reading at this address clears INT2_SRC_A IA bit (and the interrupt signal on INT 2 pin) and allows the refreshing of data in the INT2_SRC_A register if the latched option was chosen.

9.1.18 INT2_THS_A (36h)

Table 52. INT2_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 53. INT2_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

9.1.19 INT2_DURATION_A (37h)

Table 54. INT2_DURATION_A register

0	D6	D5	D4	D3	D2	D1	D0

Table 55. INT2_DURATION_A description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

9.2 Magnetic field sensing register description

The magnetometer core contains a set of registers which are used to control its behavior and to retrieve magnetic field data. The register's address, composed of 8 bits, is used to identify them and to read/write the data through the serial interface.

For magnetic field sensing interface, the default (factory) 7-bit slave address is 00111100b (0x3C) for write operations, or 00111101b (0x3D) for read operations.

9.2.1 CRA_REG_M (00h)

The configuration register A is used to configure the device for setting the data output rate and measurement configuration. CRA0 through CRA7 indicate bit locations, with *CRA* denoting the bits that are in the configuration register. CRA7 denotes the first bit of the data stream. The number in parentheses indicates the default value of that bit.

Table 56. CRA_REG_M register

0	0	0	DO2	DO1	DO0	MS1	MS0

Table 57. CRA_REG_M description

CRA7 to CRA5	These bits must be cleared for correct operation.
DO2 to DO0	Data output rate bits. These bits set the rate at which data is written to all three data output registers
MS1 to MS0	Measurement configuration bits. These bits define the measurement flow of the device, specifically whether or not to incorporate an applied bias to the sensor into the measurement

Table 58. CRA_REG M description

DO2	DO1	DO0	Minimum data output rate (Hz)
0	0	0	0.75
0	0	1	1.5
0	1	0	3.0
0	1	1	7.5
1	0	0	15
1	0	1	30
1	1	0	75
1	1	1	Not used

Table 59. CRA_REG_M description

MS1	MS0	Magnetic sensor operating mode
0	0	Normal measurement configuration (default). In normal measurement configuration the device follows normal measurement flow.
0	1	Positive bias configuration.
1	0	Negative bias configuration.
1	1	This configuration is not used

9.2.2 CRB_REG_M (01h)

The configuration register B for setting the device gain. CRB0 through CRB7 indicate bit locations, with *CRB* denoting the bits that are in the configuration register. CRB7 denotes the first bit of the data stream. The number in parentheses indicates the default value of that bit.

Table 60. CRA_REG register

GN2	GN1	GN0	0	0	0	0	0

Table 61. CRA_REG description

CRB7 to CRB5	Gain configuration bits. These bits configure the gain for the device. The gain configuration is common for all channels
CRB7 to CRB5	This bit must be cleared for correct operation

Table 62. Gain setting

GN2	GN1	GN0	Sensor input field range [Gauss]	Gain X/Y and Z [LSB/Gauss]	Gain Z [LSB/Gauss]	Output range
0	0	1	±1.3	1055	950	0xF800–0x07FF (-2048–2047)
0	1	0	±1.9	795	710	
0	1	1	±2.5	635	570	
1	0	0	±4.0	430	385	
1	0	1	±4.7	375	335	
1	1	0	±5.6	320	285	
1	1	1	±8.1	230	205	

9.2.3 MR_REG_M (02h)

The mode register is an 8-bit register from which data can be read or to which data can be written. This register is used to select the operating mode of the device. MR0 through MR7 indicate bit locations, with *MR* denoting the bits that are in the mode register. MR7 denotes

the first bit of the data stream. The number in parentheses indicates the default value of that bit.

Table 63. MR_REG

0	0	0	0	0	0	MD1	MD0

Table 64. MR_REG description

MR7 to MR2	These bits must be cleared for correct operation
MR1 to MR0	Mode select bits. These bits select the operation mode of this device.

Table 65. Magnetic sensor operating mode

MD1	MD0	Mode
0	0	Continuous-conversion mode: the device continuously performs conversions and places the result in the data register. RDY goes high when new data is placed in all three registers. After a power-on or a write to the mode or configuration register, the first measurement set is available from all three data output registers after a period of 2/fDO, and subsequent measurements are available at a frequency of fDO, where fDO is the frequency of data output.
0	1	Single-conversion mode: the device performs a single measurement, sets RDY high and returns to sleep mode. Mode register returns to sleep mode bit values. The measurement remains in the data output register and RDY remains high until the data output register is read or another conversion is performed.
1	0	--
1	1	Sleep mode. Device is placed in sleep mode

9.2.4 OUT_X_M (03-04h)

The data output X registers are two 8-bit registers, data output register H and data output register L. These registers store the measurement result from channel X.

Data output X register H contains the MSB from the measurement result, and data output X register L contains the LSB from the measurement result.

The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DXRH0 through DXRH7 and DXRL0 through DXRL7 indicate bit locations, with DXRH and DXRL denoting the bits that are in the data output X registers. DXRH7 and DXRL7 denote the first bit of the data stream.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096 in 2's complement form. This register value clears after the next valid measurement is made.

Table 66. OUTXH_M register

DXRH7	DXRH6	DXRH5	DXRH4	DXRH3	DXRH2	DXRH1	DXRH0

The content of this register is the MSB magnetic field data for X-axis.

Table 67. OUTXL_M register

DXRL7	DXRL6	DXRL5	DXRL4	DXRL3	DXRL2	DXRL1	DXRL0

The content of this register is the LSB magnetic field data for X-axis.

9.2.5 OUT_Y_M (05-06h)

The data output Y registers are two 8-bit registers, data output register H and data output register L. These registers store the measurement result from channel Y.

Data output Y register H contains the MSB from the measurement result, and data output Y register L contains the LSB from the measurement result.

Table 68. OUT_YH_M register

DYRH7	DYRH6	DYRH5	DYRH4	DYRH3	DYRH2	DYRH1	DYRH0

The content of this register is the MSB magnetic field data for Y-axis.

Table 69. OUT_YL_M register

DYRL7	DYRL6	DYRL5	DYRL4	DYRL3	DYRL2	DYRL1	DYRL0

The content of this register is the LSB magnetic field data for Y-axis.

9.2.6 OUT_Z_M (07-08h)

The data output Z registers are two 8-bit registers, data output register H and data output register L. These registers store the measurement result from channel Z.

Data output Z register H contains the MSB from the measurement result, and data output Z register L contains the LSB from the measurement result.

Table 70. OUTZH_M register

DZRH7	DZRH6	DZRH5	DZRH4	DZRH3	DZRH2	DZRH1	DZRH0

The content of this register is the MSB magnetic field data for Z-axis.

Table 71. OUTZL_M register

DZRL7	DZRL6	DZRL5	DZRL4	DZRL3	DZRL2	DZRL1	DZRL0

The content of this register is the LSB magnetic field data for Z-axis.

9.2.7 SR_REG_M (09h)

When one or more of the output registers are read, new data cannot be placed in any of the output data registers until all six data output registers are read. This requirement also

impacts DRDY and RDY, which cannot be cleared until new data is placed in all the output registers.

Status register

The status register (SR) is an 8-bit read-only register. This register is used to indicate device status. SR0 through SR7 indicate bit locations, with *SR* denoting the bits that are in the status register. SR7 denotes the first bit of the data stream.

Table 72. SR register

0	0	0	0	0	REN	LOC	RDY

Table 73. Status register bit designations

MD1	MD0	Mode
SR7 to SR3	0	These bits must be cleared for correct operation
SR2	REN	Regulator enabled bit. This bit is set when the internal voltage regulator is enabled. This bit is cleared when the internal regulator is disabled.
SR1	LOCK	Data output register lock. This bit is set when some, but not all, of the six data output registers have been read. When this bit is set, the six data output registers are locked and any new data is not placed in these registers until one of four conditions are met: one, all six have been read or the mode changed, two, a POR is issued, three, the mode is changed, or four, the measurement is changed.
SR0	RDY	Ready bit. Set when data is written to all six data registers. Cleared when the device initiates a write to the data output registers, when in off mode, and after one or more of the data output registers are written to. When RDY bit is clear, it shall remain cleared for a minimum of 5 µs. The DRDY pin can be used as an alternative to the status register for monitoring the device for conversion data.

9.2.8 IR_REG_M (0Ah/0Bh/0Ch)

The identification registers (IR) are used to identify the device. IR0 through IR7 indicate bit locations, with IRA/IRB/IRC denoting the bits that are in the identification registers A, B & C. IRA7/IRB7/IRC7 denotes the first bit of the data stream.

The identification value for this device is stored in this register. This is a read-only register.

Register values. ASCII value *H*

Table 74. IRA_REG_M

0	1	0	0	1	0	0	0

Table 75. IRB_REG_M

0	0	1	1	0	1	0	0

Table 76. IRC_REG_M

0	0	1	1	0	0	1	1

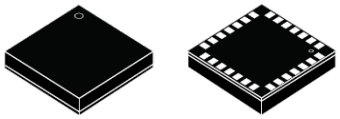
10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

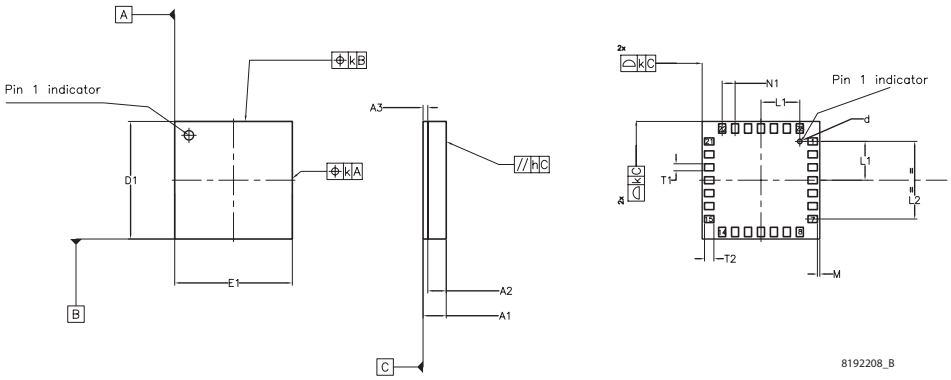
Figure 6. LGA-28: mechanical data and package dimensions

Dimensions			
Ref.	mm		
	Min.	Typ.	Max.
A1			1
A2		0.785	
A3		0.200	
D1	4.850	5.000	5.150
E1	4.850	5.000	5.150
L1		1.650	
L2		3.300	
N1		0.550	
M	0.040	0.100	0.160
T1	0.260	0.300	0.340
T2	0.360	0.400	0.440
d		0.200	
k		0.050	
h		0.100	

Outline and mechanical data



LGA-28 (5x5x1)
Land Grid Array Packages



11 Revision history

Table 77. Document revision history

Date	Revision	Changes
18-Dec-2009	1	First issue.

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