LAB3 CEG2136
ARITHMETIC LOGIC UNIT

PRELAB

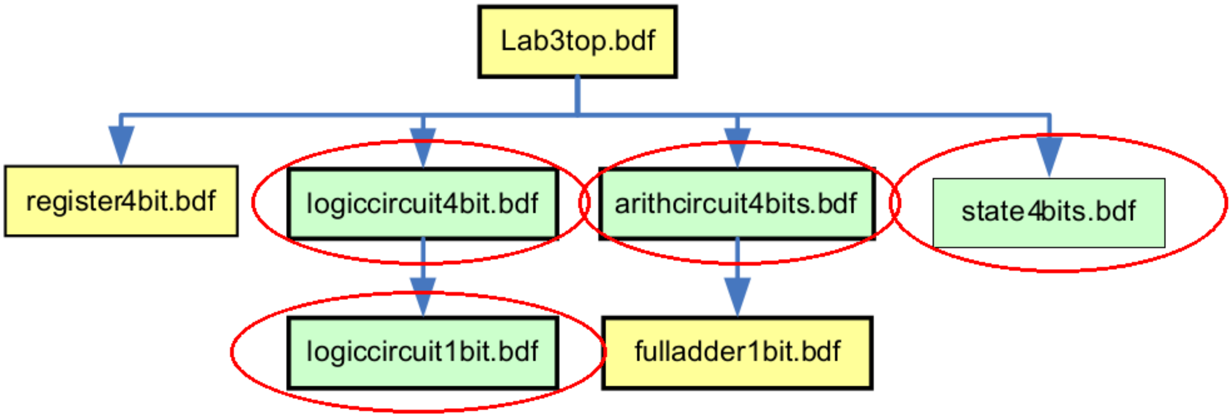


Figure 3: Hierarchy of the files

OPTIONAL: A 4-bit register made from D Flip Flops. The Diagram is already provided in Figure 8 on page 6 of the lab manual.

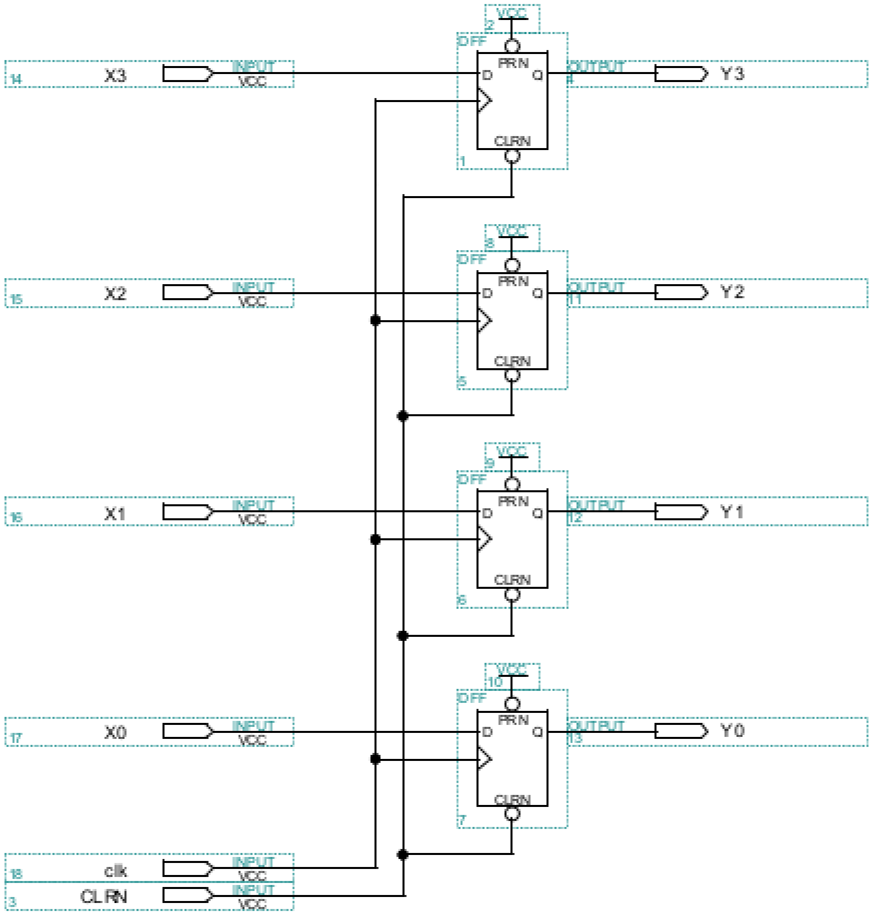


Figure 8: Diagram of a 4-bit register

5.3.1 REQUIRED: Show a 1 bit Logic and Shift Circuit (logiccircuit1bit.bdf)

S2	S1	S0	CL_i
0	0	0	$CL_i \leftarrow 0$
0	0	1	$CL_i \leftarrow 1$
0	1	0	$CL_i \leftarrow A_i \wedge B_i$
0	1	1	$CL_i \leftarrow A_i \vee B_i$
1	0	0	$CL_i \leftarrow A_i \oplus B_i$
1	0	1	$CL_i \leftarrow A_i \wedge \overline{B}$
1	1	0	$CL_i \leftarrow A_{i-1}$
1	1	1	$CL_i \leftarrow A_{i+1}$

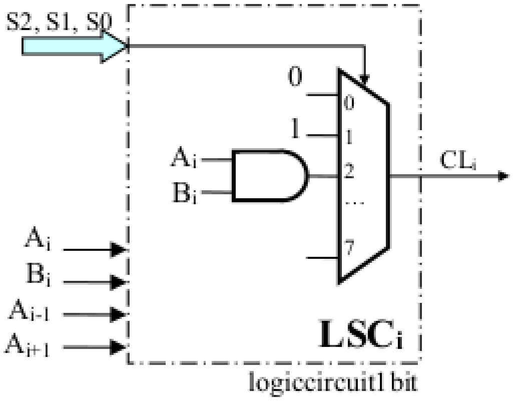
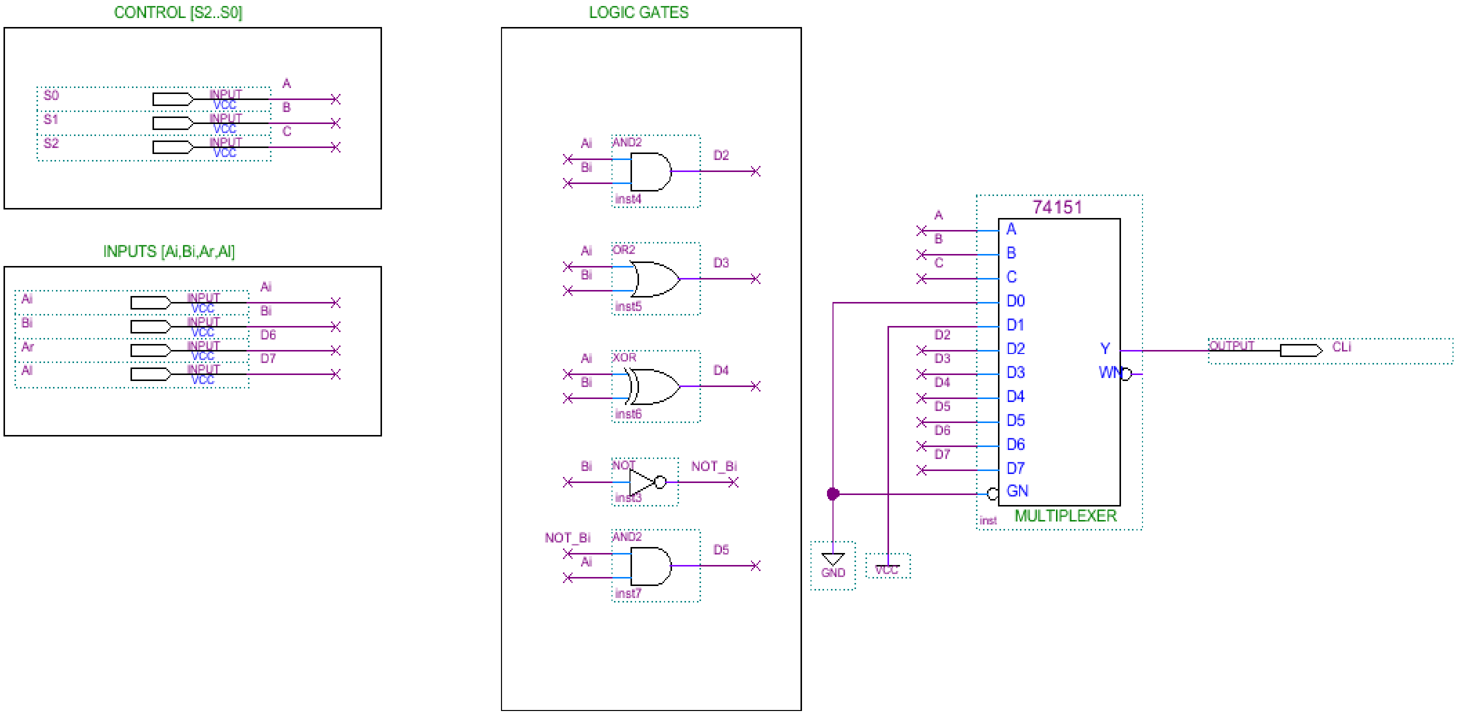
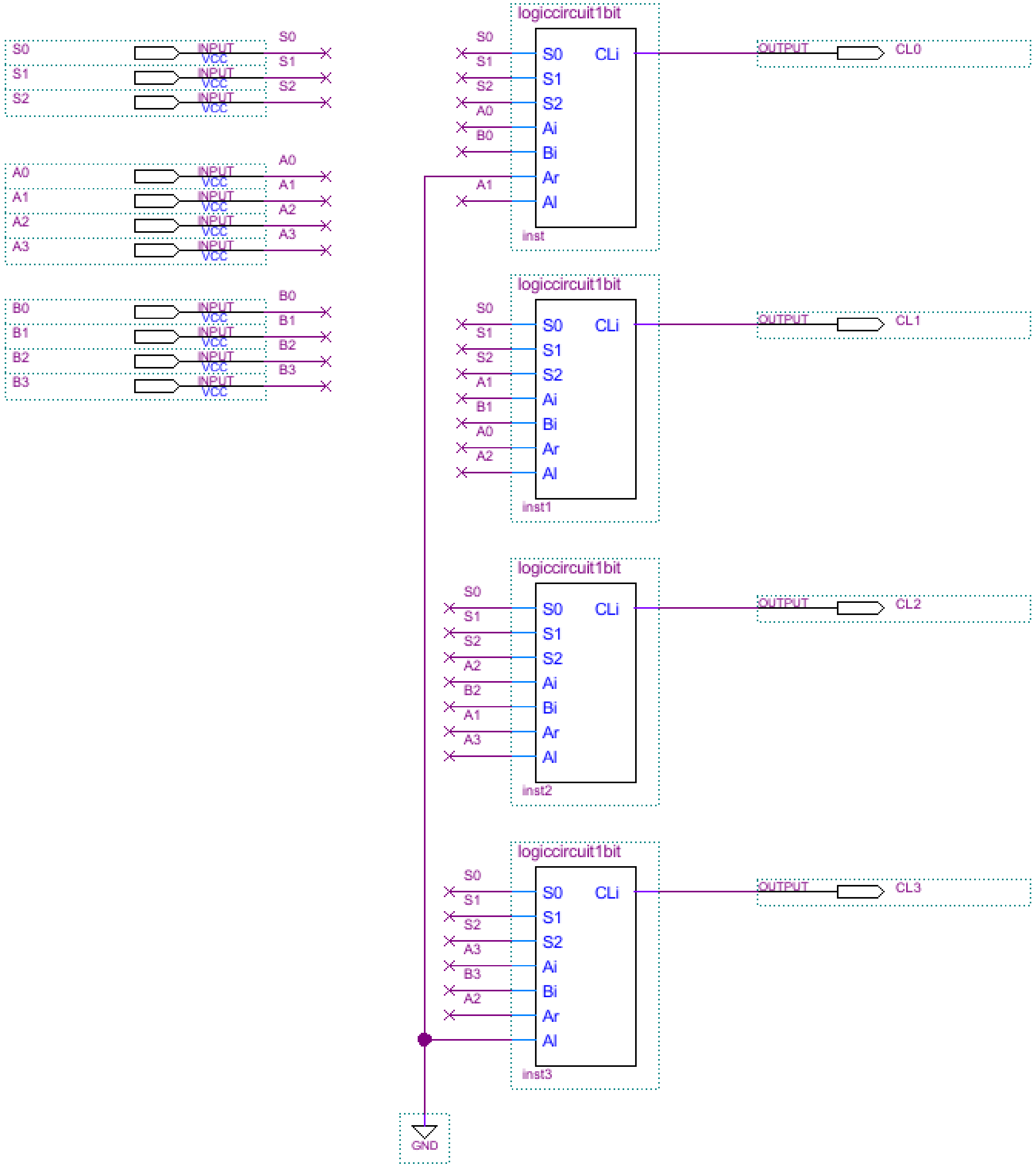


Fig. 4: LSC$_i$ incomplete logic diagram



5.3.2 REQUIRED: Show a 4-bits Logic and Shift Circuit (logiccircuit4bits.bdf)



OPTIONAL: Show a 1-bit Full Adder (fulladder1bit.bdf). The diagram is already provided in Figure 9 on page 7 of the lab manual.

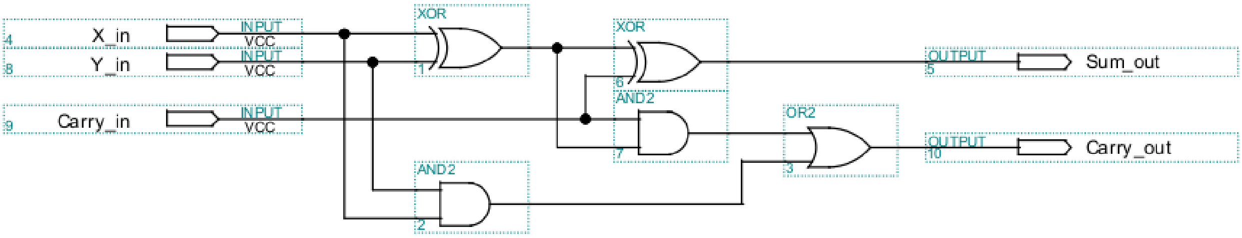
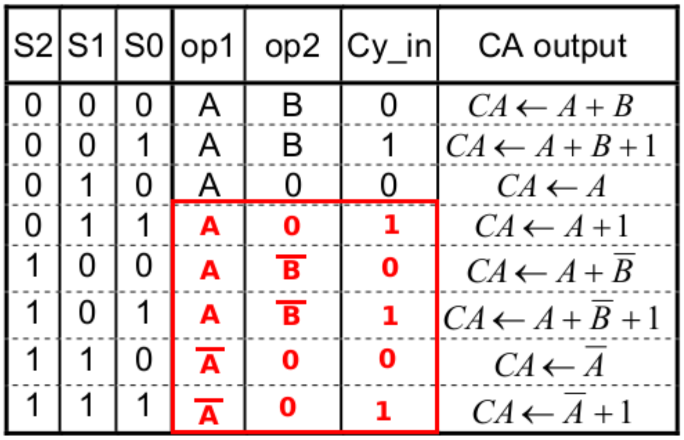


Figure 9: Logic diagram of a full adder (marked $\sum$ in Fig. 6)

5.4.1 REQUIRED: Complete the Truth table for a 1-bit Arithmetic Circuit (AC or 1-bitfulladder) corresponding to Figure 5 on Page 4

Complete the following truth table with the corresponding values derived from Table 1.



S2	S1	S0	op1	op2	Cy_in	CA output
0	0	0	A	B	0	$CA \leftarrow A + B$
0	0	1	A	B	1	$CA \leftarrow A + B + 1$
0	1	0	A	0	0	$CA \leftarrow A$
0	1	1	A	0	1	$CA \leftarrow A + 1$
1	0	0	A	$\overline{B}$	0	$CA \leftarrow A + \overline{B}$
1	0	1	A	$\overline{B}$	1	$CA \leftarrow A + \overline{B} + 1$
1	1	0	$\overline{A}$	0	0	$CA \leftarrow \overline{A}$
1	1	1	$\overline{A}$	0	1	$CA \leftarrow \overline{A} + 1$

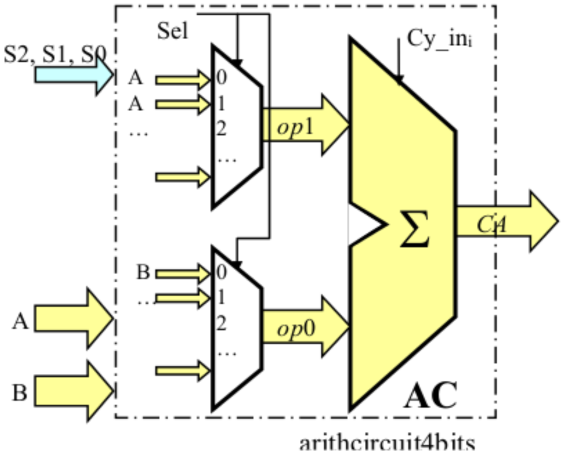
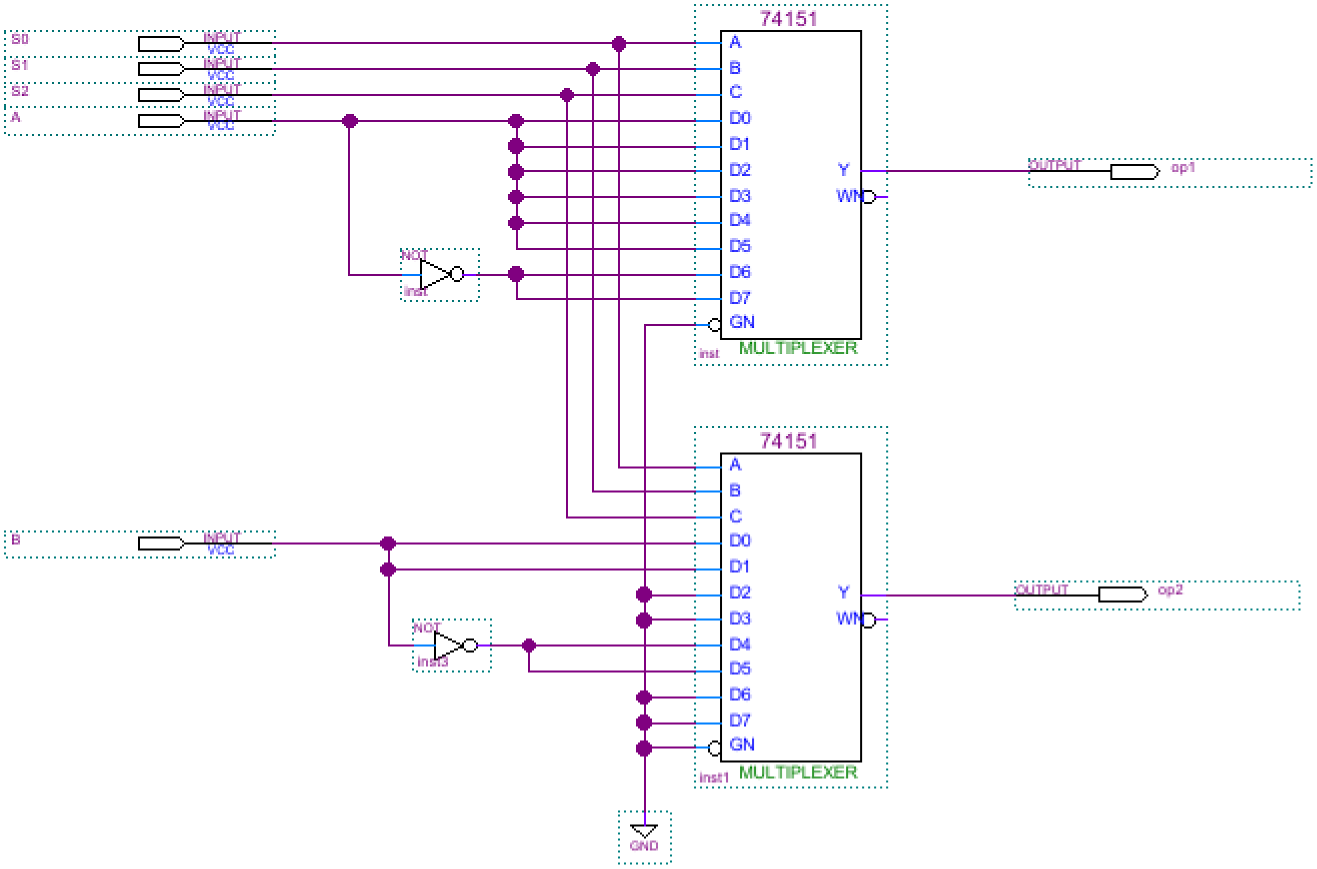


Fig. 5: AC block diagram

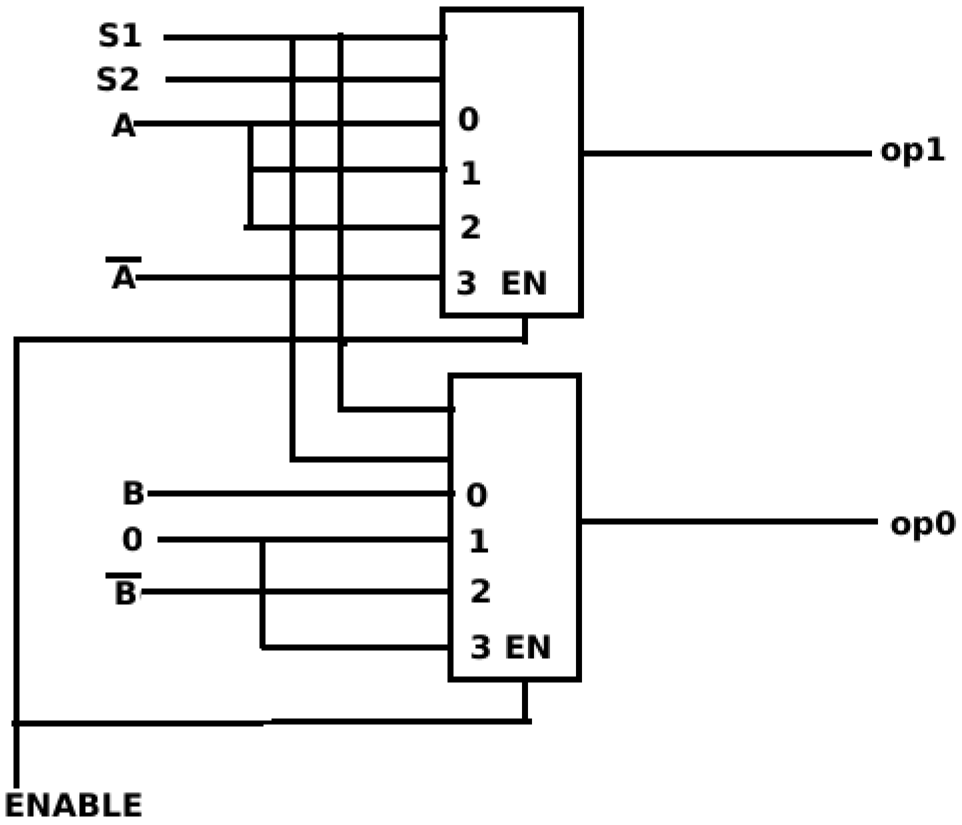
5.4.2 REQUIRED: Two possible ways.

First Alternative (Not Efficient): Using two 8-to-1 multiplexers with S0,S1 and S2 as Select



5.4.2 REQUIRED (CONT.)

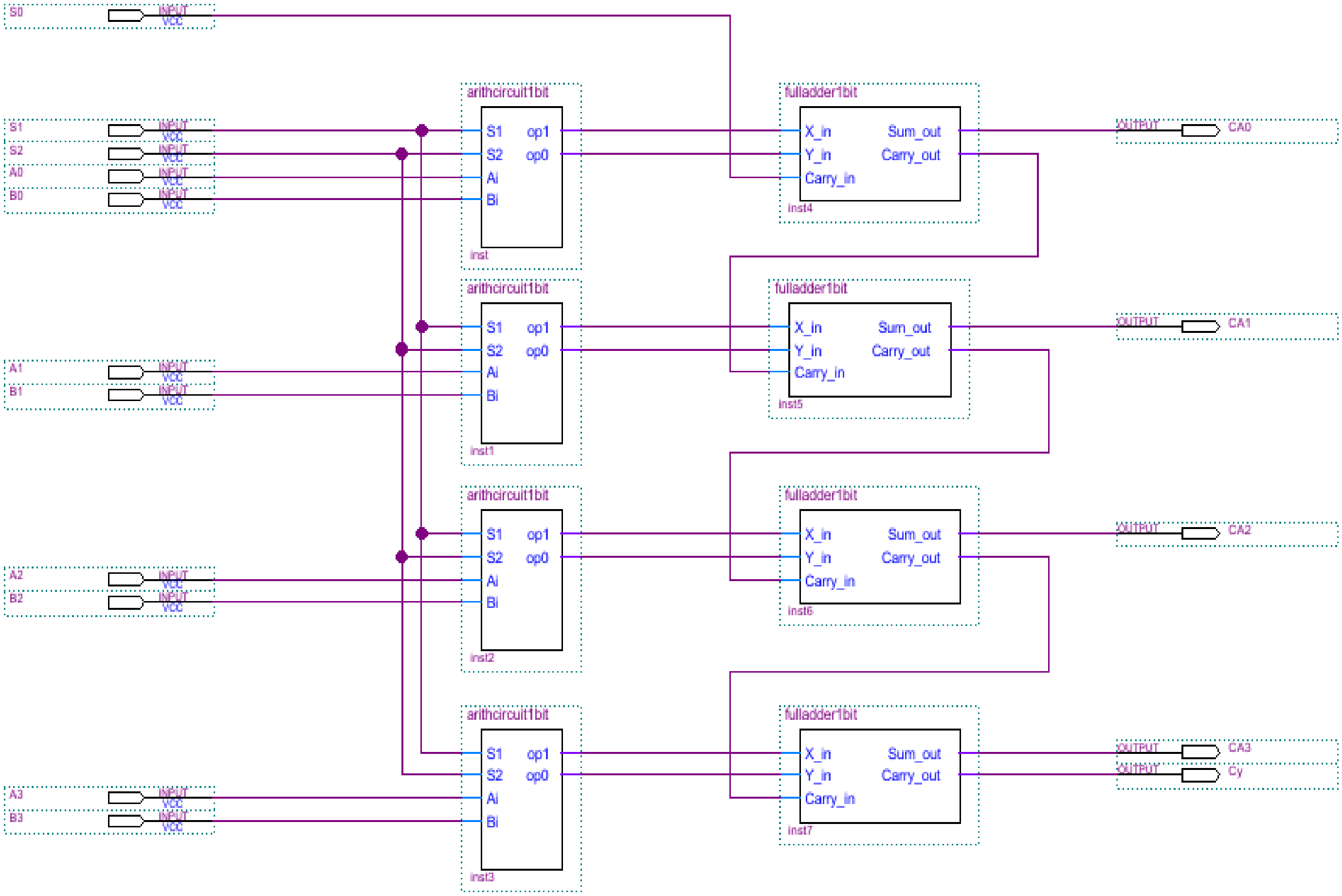
Second Alternative (Efficient): Using two 4-to-1 multiplexers with S2 and S1 as Select



5.4.3. REQUIRED. Equation for Cy (Can be obtained from K-maps for example)

$$Cy=S0$$

5.4.4 REQUIRED. Complete block diagram for ACi



5.5 REQUIRED. Complete block diagram for Aci

Z=(C3 OR C2 OR C1 OR C0)'
S=C3
Cy=S3 AND Cy_in
V=Cy_in1 XOR Cy_in2

Bonus if there is an overflow here

Table 5: Sequence of micro-operations to simulate

Clock Cycle	RTL Micro-operations	S3	S2	S1	S0	'op1←A	op2←B	C	V,Z,N,Cy	S_{16}	A_{16}	B_{16}	C_{16}	St_{16}
1	$A \leftarrow "1010", B \leftarrow "0011", C \leftarrow A \wedge \overline{B}$	0	1	0	1	1010	0011	1000	1010					
2	$A \leftarrow "0110", C \leftarrow a\text{shl } A$	0	1	1	0	0110	xxxx	1100	0010 1					
3	$A \leftarrow "0011", B \leftarrow "0101", C \leftarrow A + B$	1	0	0	0	0011	0101	1000	1010					
4	$A \leftarrow "1100", C \leftarrow A + 1$	1	0	1	1	1100	xxxx	1101	0010					
5	$A \leftarrow "0011", B \leftarrow "0101", C \leftarrow A \oplus B$	0	1	0	0	0011	0101	0110	0000					
6	$A \leftarrow "1010", C \leftarrow \overline{A}$	1	1	1	0	1010	xxxx	0101	0000					
7	$C \leftarrow "0000'$	0	0	0	0	xxxx	xxxx	0000	0100					
8	$A \leftarrow "0101", B \leftarrow "0011", C \leftarrow A + \overline{B} + 1$	1	1	0	1	0101	0011	0010	0001					
9	$A \leftarrow "1110", C \leftarrow A$	1	0	1	0	1110	xxxx	1110	0010					
10	$A \leftarrow "0110", C \leftarrow \overline{A} + 1$	1	1	1	1	0110	xxxx	1110	0010					
11	$A \leftarrow "0101", B \leftarrow "0011", C \leftarrow A \wedge B$	0	0	1	0	0101	0011	0001	0000					
12	$A \leftarrow "0001", B \leftarrow "0010", C \leftarrow A + B + 1$	1	0	0	1	0001	0010	0100	0000					
13	$A \leftarrow "1101", C \leftarrow a\text{shr } A$	0	1	1	1	1101	xxxx	1110	0010					
14	$A \leftarrow "0110", B \leftarrow "0101", C \leftarrow A + \overline{B}$	1	1	0	0	0110	0101	0000	0101					
15	$C \leftarrow "1111"$	0	0	0	1	xxxx	xxxx	1111	xxxx					
16	$A \leftarrow "1100", B \leftarrow "1010", C \leftarrow A \vee B$	0	0	1	1	1100	1010	1110	0010					

Some students may use inverted S3 (i.e 0⇄1)
This is also corrected