Analog Circuit-Blocks for designing an Artificial Neural Network

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Abstract

In the paper, the authors propose to realize a feed-forward artificial neural network with a single hidden layer using CMOS based analog circuit blocks. The proposed circuit blocks are analog multiplier, current subtractor and activation function circuitry. A hardware implementation of the sigmoid activation function is proposed. The network is capable of solving non-linearly separable problems and successfully realizes the XOR gate. The weights have been calculated through the back-propagation (BP) algorithm implemented in MATLAB. Our aim would be to separately implement the three individual circuit components in eSim and then verify the corresponding outputs results with those mentioned in the paper.

1 Reference Circuit Details

The basic operations required in an ANN are multiplication, subtraction, summation, and an activation function. Therefore, in the referenced paper, the corresponding analog blocks of such mathematical operations have been designed using CMOS technology.

The authors use two types of multipliers due to network connection requirements. For the input layer, a Gilbert Cell-based multiplier has been employed to multiply the input signals with the corresponding weights. Conversely, a variable gain amplifier has been utilized in the second layer since there was a need for a two-quadrant multiplier. Two different subtractor blocks have been designed using different transistor sizes in order to comply with the input current levels of two different multipliers. The differential input currents are subtracted so that a single current output is obtained. This current is then used as an input to the activation function block.

The authors design a hardware implementation of the sigmoid function. This circuit takes a current input signal and maps it into the voltage domain. The smooth current-voltage relationship of MOSFETs has been leveraged to mimic the characteristics of the sigmoid function.

For the NAND and OR gates the Gilbert Cell-based multiplier is preferred because the first layer can be designed in fully differential topology. The second layer, which realizes the operation of the AND gate, the VGA topology is chosen as it takes one input voltage coming from the output of the sigmoid functon.

2 Reference Circuit

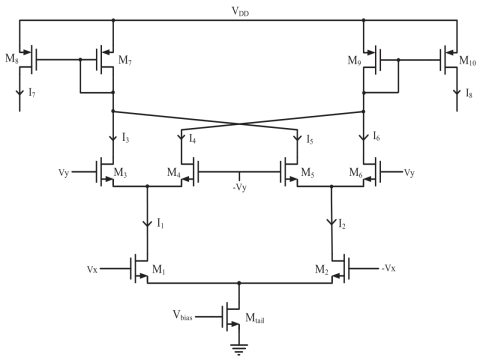

Figure 1: Reference circuit diagram.

3 Reference Circuit Waveforms

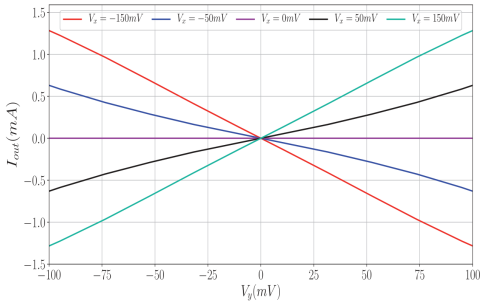

Figure 2: Reference waveform.

References

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