Simulation Report - Week 4

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1. Introduction

This week I am looking into applications of op-amp circuits. It is interesting that op-amps find use in various application circuits such as *subtractor circuits, averaging circuits, voltage-to-current converters, (low voltage) dc/ac voltage meter,* etc. I have chosen to discuss about voltage-to-current converter circuit (with floating load) and how voltage follower circuits can be modified to have very high input impedance. The second topic was supposed to be a simple one but I randomly stumbled upon this topic and from there, it was a *journey down the rabbit hole* of reading datasheets, reading solutions and asking questions on electronics.stackexchange.com.

2. Simulation Details

- Environment: LTspiceXVII
- Important component(s): LM741 op-amp IC
- Reference Book: Gayakwad[1]

2.1 Voltage to current converter

It is possible to design a simple voltage-to-current converter using just an op-amp. Note that the design shown in figure 1(i) has the load resistor R_1 *floating* as in it is not connected to the ground. We apply the input voltage to the non-inverting terminal and the feedback voltage across the resistance R_2 drives the inverting terminal.

Assume that $v_i n$ in the input voltage signal and v_f is the feedback voltage. Now we know that for an op-amp,

$$v_{id} = v_{in} - v_f$$

But as per the properties of op-amp, $v_{id} \approxeq 0$, since A is very large, therefore we can write:

$$v_{in} = v_f$$
$$v_{in} = R_2 i_o$$
$$i_o = \frac{v_{in}}{R_2}$$

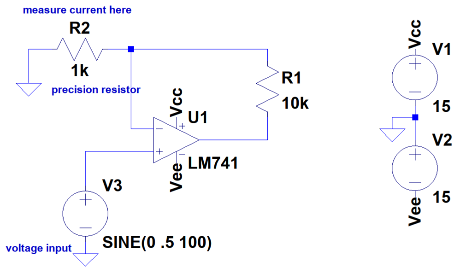
where i_o is the output current.

Here it is evident that in this circuit, the input voltage v_{in} is appearing as the current i_o. It is advised to use a *precision resistor* for R_2 so that the output current i_o will be precisely fixed. Figure 1(ii) shows how a input signal with amplitude 0.5 mV leads to an output current of i_o of (0.5 mA / 1kΩ) = 500μA.

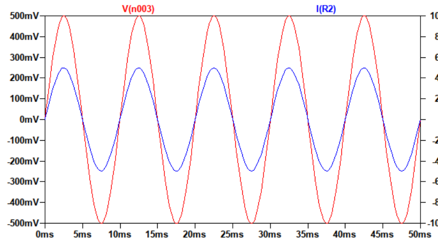
2.2 Very High Input Impedance circuit

The following discussion mainly involves the voltage follower circuit that has the highest input resistance of any op-amp circuit. For this reason, this circuit finds its use in reducing voltage error caused by source loading and to isolate high-impedance sources from the circuitry in the following stage. In simple words due to the high input impedance of the voltage follower, it does not "suck" (for lack of other words) too much current from the previous stages (and "disturb" them) and as it also has quite low output impedance, it is capable of driving the circuits at the following stages.

Now voltage followers are of two types, (a) dc-coupled and (b) ac-coupled. We shall discuss each of them below:

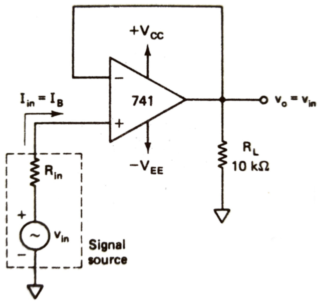


(i) Circuit schematic

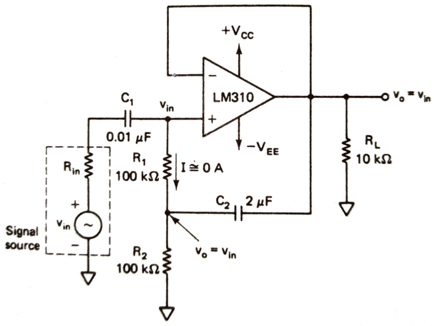


(ii) Sample output plot

Figure 1: Voltage to current converter (floating load)



(i) DC-coupled voltage follower



(ii) AC-coupled voltage follower

A. DC-coupled voltage follower

In DC-coupled voltage followers (see figure 2(i)), the input voltage is directly applied to the non-inverting input terminal. The bias current I_B of the op-amp can flow through the input source resistance R_{in}. It is possible to maintain the DC biasing, the bias currents are connected through the ground (more on this later).

In case of high input source resistance, R_{in} and if the bias current of the op-amp is in the range of 1mA-100nA, the voltage drop across the resistance will be large, $V_{drop} = I_B R_{in}$. This will lead to error in the voltage at the non-inverting input, the output and input voltage will not be equal. The voltage follower is not functioning well! To remedy this, we should use an op-amp with low input bias current (when working from high input source resistances), preferably with values near and lower than 10nA.

B. AC-coupled voltage follower

If we are working with AC signals we first need to get rid of the DC offset so we put a *coupling capacitor* in series with the signal input. The capacitor here acts as a high pass filter as it has low impedance for high frequency signals but acts as an open circuit for low frequency signals like DC.

$$\text{For high values of frequency } f, X_C = \frac{1}{2\pi f C} \approx 0$$

$$\text{and for DC signals, } f = 0, X_C = \frac{1}{0} \approx \infty$$

Now we need to care about the DC biasing of the op-amp, so we add a bias resistor R_1 to provide a path for the bias current I_B to ground. To know more about why we need to do this, read this application note by Renesas on *How to Bias Op-Amps Correctly*[2]. But by adding this bias resistor, we also created a path for the AC input signal to flow to the ground and therefore, drastically reduced the input resistance of the entire follower circuit. In fact, the resistance of the circuit as seen by the input source is equal to the bias resistance.

We can solve this and restore the high input impedance of the circuit by *bootstrapping*[3][4], we first add a resistor R_2 in between the bias resistor R_1 and the ground, then connect the output of the op-amp and the node in between the two resistors R_1 and R_2 via a capacitor C_2. Due to the capacitor C_2, the path through it, is open circuit for the DC bias current so this helps separate the DC bias that is coming from the ground and the AC signal coming from the output of the op-amp.

After the circuit has been bootstrapped, we observe that the input signal is applied through the coupling capacitor C_1 to the top of R_1 and simultaneously, the output voltage is coupled through the capacitor C_2 to the bottom of R_1. Now as the op-amp here is working as a voltage follower, the gain of the circuit is 1 (output signal is identical to the input signal) and if we calculate the drop across the resistor R_1, we get $(v_{in} - v_o)$ which is ≈ 0. So the current through R_1 is almost zero and as the only path for the input signal is through the op-amp, the input resistance is once again, very high.

The final design is shown in figure 2(ii). Looking back, we realize that the op-amp circuit is properly biased as the DC bias current can flow down to the ground via R_1 and R_2 but it can't flow through the path in which C_2 is present. The input impedance was lowered as in our previous design the AC input signal could flow through the bias resistor R_1, but we see that after bootstrapping this path has minimal current flow and this issue has been fixed.

As mentioned in the introduction, I couldn't have written this note if helpful (and more experienced) users at `stackexchange` didn't clarify my doubts[5].

References

[1] Ramakant A. Gayakwad. *Op-Amps and Linear Integrated Circuits.* PHI Learning Pvt. Ltd., New Delhi-110001, fourth edition, 2010.

[2] Renesas Electronics. How to Bias Op-Amps Correctly. https://www.renesas.com/in/en/document/apn/how-bias-op-amps-correctly?language=en.

[3] partykid. how to increase input impedance via bootstraping? https://electronics.stackexchange.com/questions/188896/how-to-increase-input-impedance-via-bootstraping.

[4] hari-t o. Concept of Bootstrapping in Electronics. https://electronics.stackexchange.com/questions/515272/concept-of-bootstrapping-in-electronics.

[5] kickstart7962. Explanation about op-amp bias resistor and bootstrapping. https://electronics.stackexchange.com/questions/586839/explanation-about-op-amp-bias-resistor-and-bootstrapping.