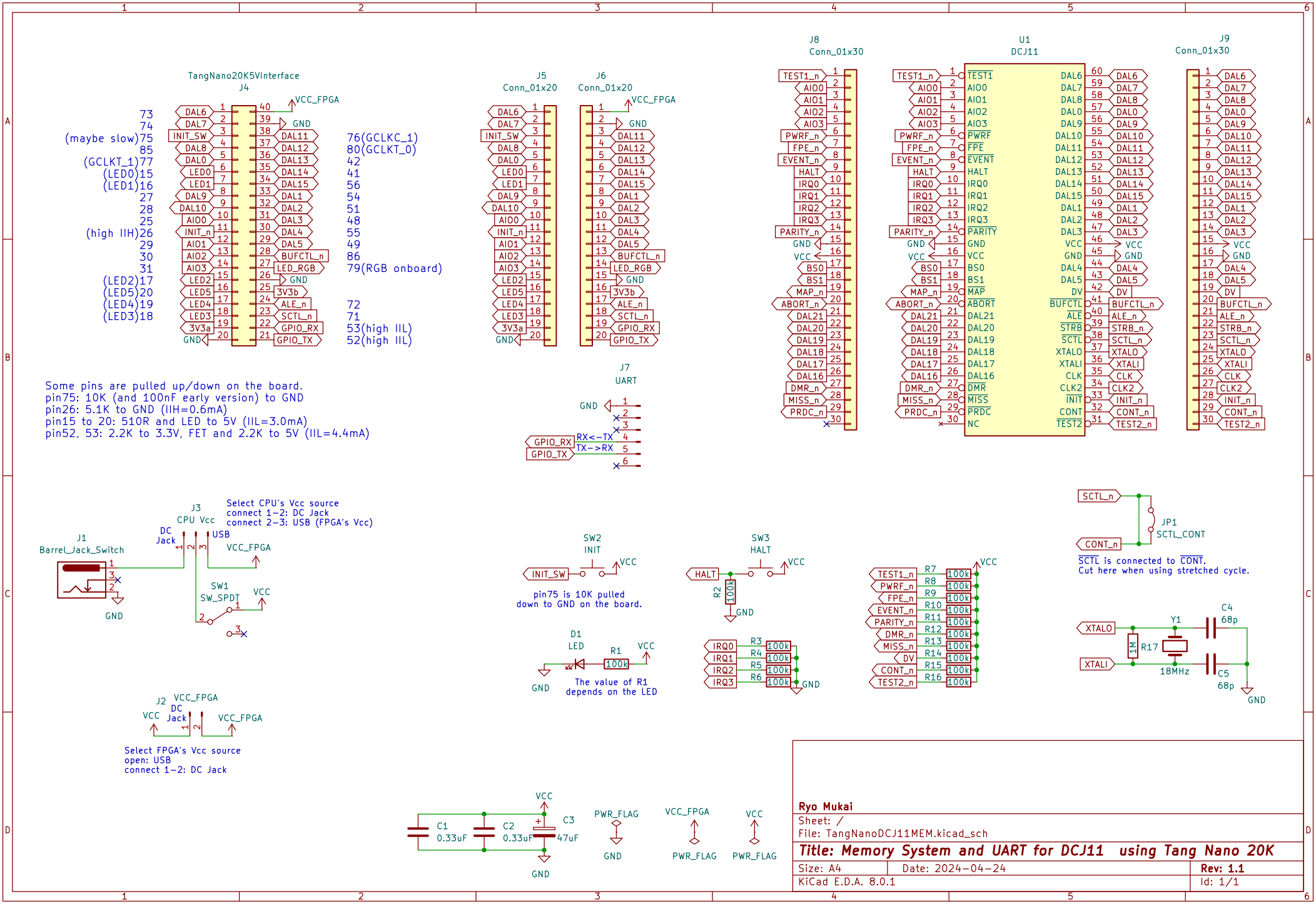
TangNano20K5VInterface
J4
J5
Conn_01x20
J6
Conn_01x20
J8
Conn_01x30
U1
DCJ11
J9
Conn_01x30
J7
UART
Some pins are pulled up/down on the board.
pin75: 10K (and 100nF early version) to GND
pin26: 5.1K to GND (IIH=0.6mA)
pin15 to 20: 510R and LED to 5V (IIL=3.0mA)
pin52, 53: 2.2K to 3.3V, FET and 2.2K to 5V (IIL=4.4mA)
J1
Barrel_Jack_Switch
J3
CPU Vcc
Select CPU's Vcc source
connect 1-2: DC Jack
connect 2-3: USB (FPGA's Vcc)
SW1
SW_SPDT
SW2
INIT
pin75 is 10K pulled
down to GND on the board.
SW3
HALT
D1
LED
The value of R1
depends on the LED
JP1
SCTL_CONT
SCTL is connected to CONT.
Cut here when using stretched cycle.
Y1
18MHz
J2
Select FPGA's Vcc source
open: USB
connect 1-2: DC Jack
Ryo Mukai
Sheet: /
File: TangNanoDCJ11MEM.kicad_sch
Title: Memory System and UART for DCJ11 using Tang Nano 20K
Size: A4
Date: 2024-04-24
Rev: 1.1
KiCad E.D.A. 8.0.1
Id: 1/1