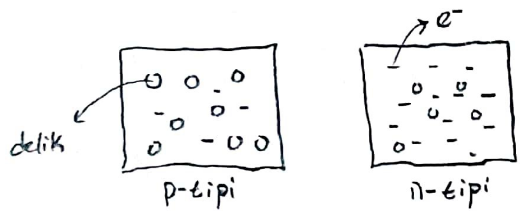
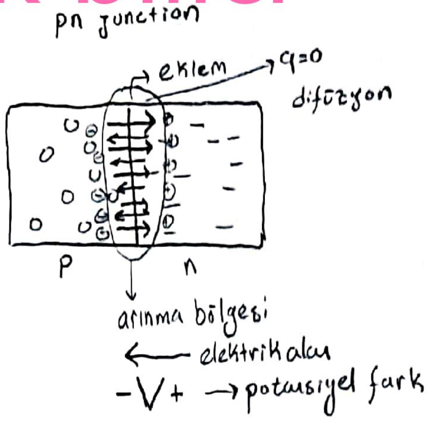
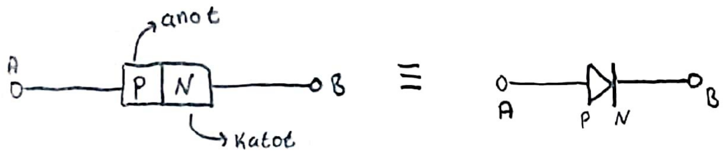
Elektronik Devreler Notları

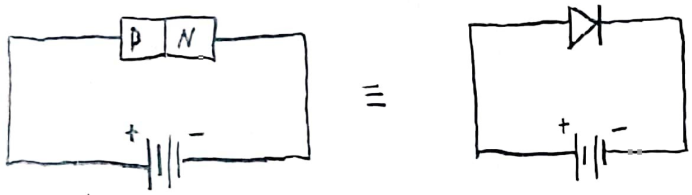
şafak bilici

Diyot



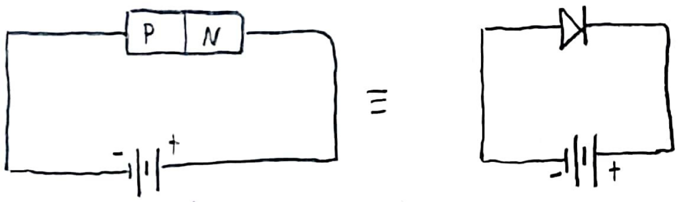






forward bias

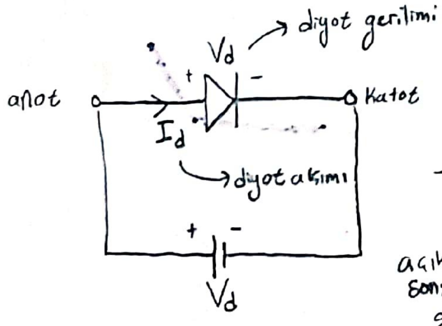
diyodun iletime geçirebilmek için kısa devre gibi davranır

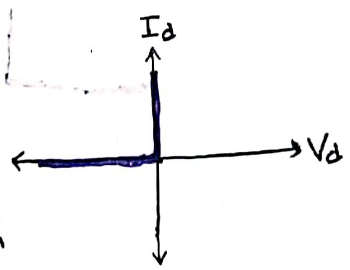


reverse bias

arınma bölgesi büyür

diyot iletime geçmez





açık devrede sonsuz akım geçer

Gerçekte:

$$I_d = I_r\left[\exp(qV_D/nkT)-1\right]$$

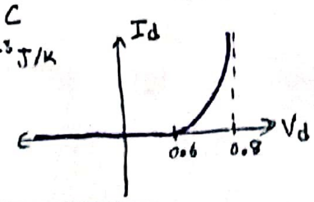
I_d → diyot akımı

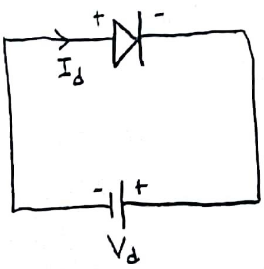
I_r → sızıntı akım

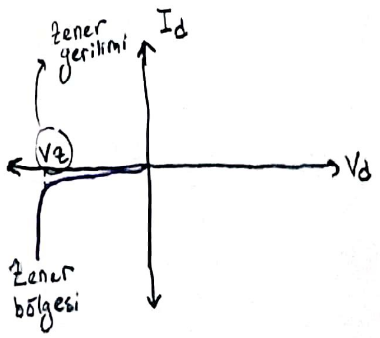
$n = 1, 2$

$q = 1{,}6 \times 10^{-19}\ C$

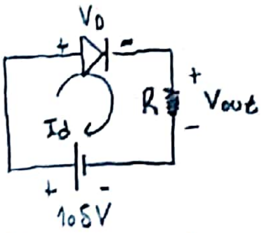
$k = 1{,}38 \times 10^{-23}\ J/K$



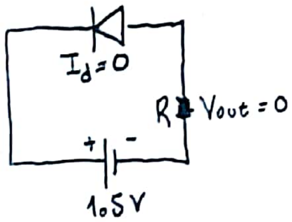




Diyotların DC Analizi



(a) Forward biased



(b) reverse biased

$1{,}5V - V_D - V_{out} = 0$

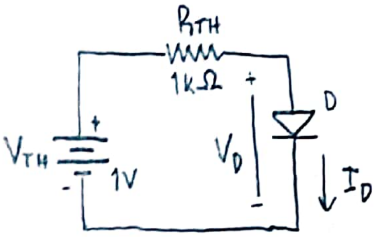
$V_{out} = 1{,}5V - V_D$

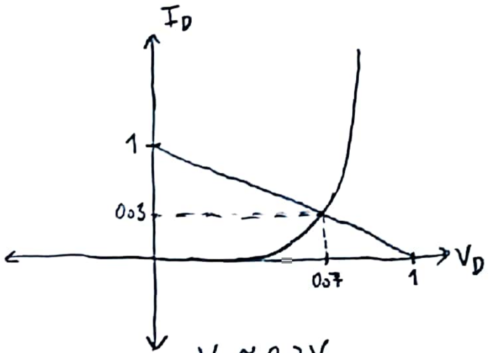
$V_D = 0{,}7V$

$V_{out} = 1{,}5V - 0{,}7V$

$= 0{,}8V$

$V_{out} = 0$





$V_D \approx 0{,}7V$

$I_D \approx 0{,}3mA$

$1V - V_R - V_D = 0$

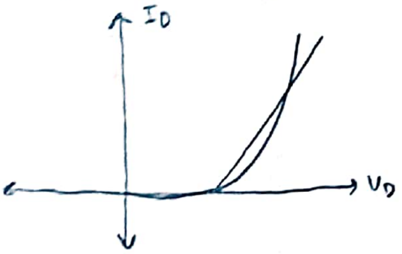
$V_R = 1V - V_D$

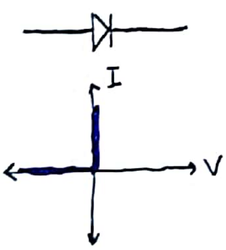
$I_D \cdot R_{TH} = 1V - V_D$

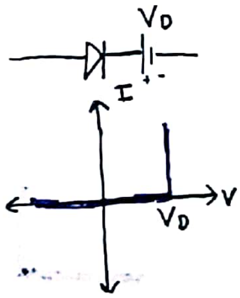
doğru denklemi

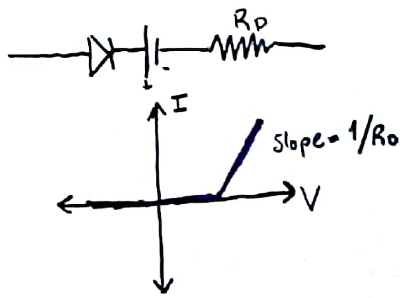
$$I_D = \boxed{\frac{1V - V_D}{R_{TH}} = \frac{-V_D}{R_{TH}} + \frac{1V}{R_{TH}}}$$

Parçalı Doğru Varsayımı Analizi

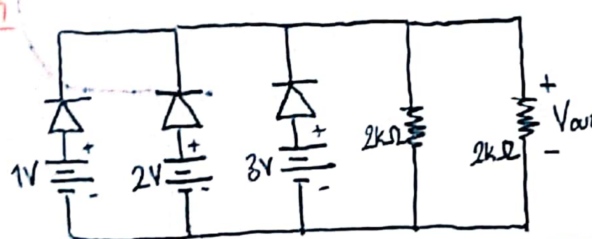


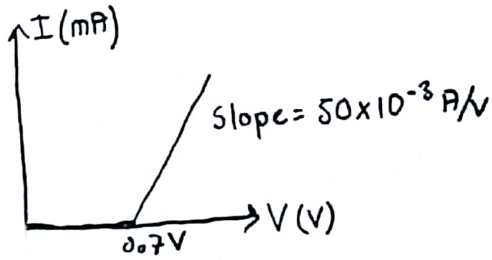




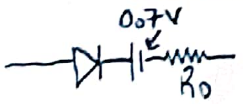


Örnek:

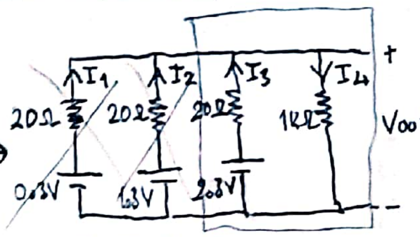




$V_{out} = ?$



$R_D = \frac{1}{slope} = 20\Omega \longrightarrow$



$I_1 = -50mA \longrightarrow$ diyot kapalı

$I_2 = 0mA \longrightarrow$ diyot kapalı

$I_3 = 50mA \longrightarrow$ diyot açık

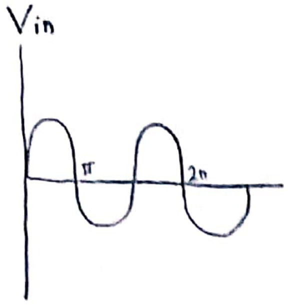
$I_1 + I_2 + I_3 = I_4$

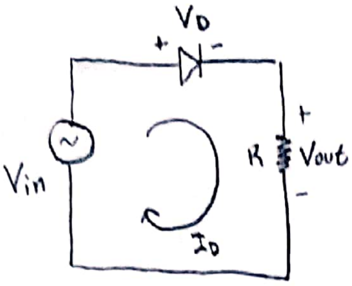
$$\frac{0{,}3 - V_{out}}{20} + \frac{1{,}3 - V_{out}}{20} + \frac{2{,}3 - V_{out}}{20} = \frac{V_{out}}{1000} \longrightarrow V_{out} = 1{,}3V$$

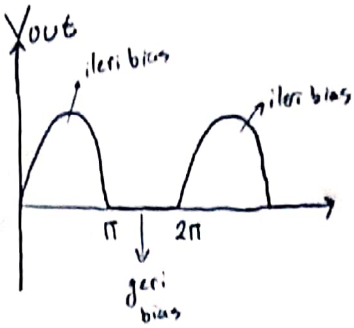
$$\longrightarrow V_{out} = \frac{2{,}3V}{1k\Omega + 20\Omega} \cdot 1k\Omega$$

$$\approx 2{,}3V$$

Doğrultucular (Rectification)

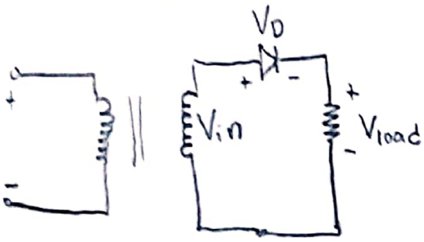


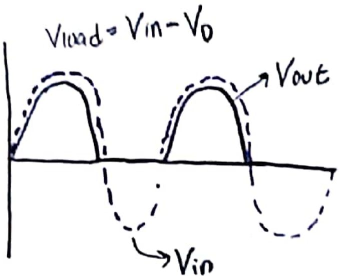




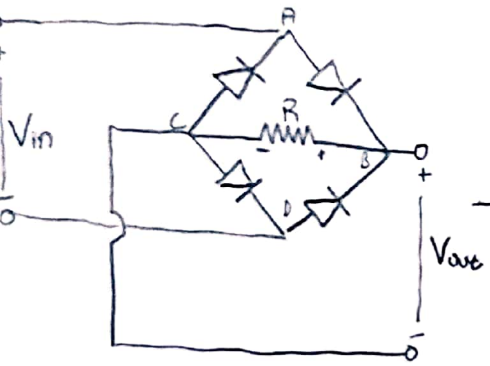
AC → DC

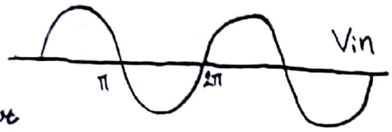
Yarım Dalga Doğrultucu (Half-Wave Rectification)

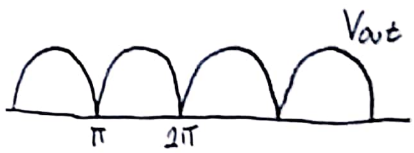




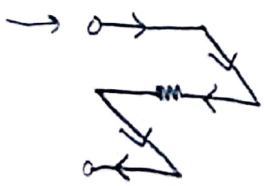
Tam Dalga Doğrultucu (Full-Wave Rectification)



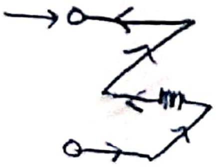




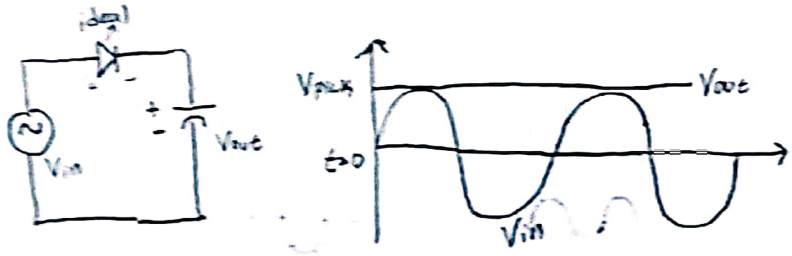
Vin → +



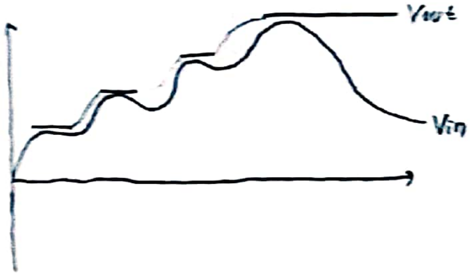
Vin → −



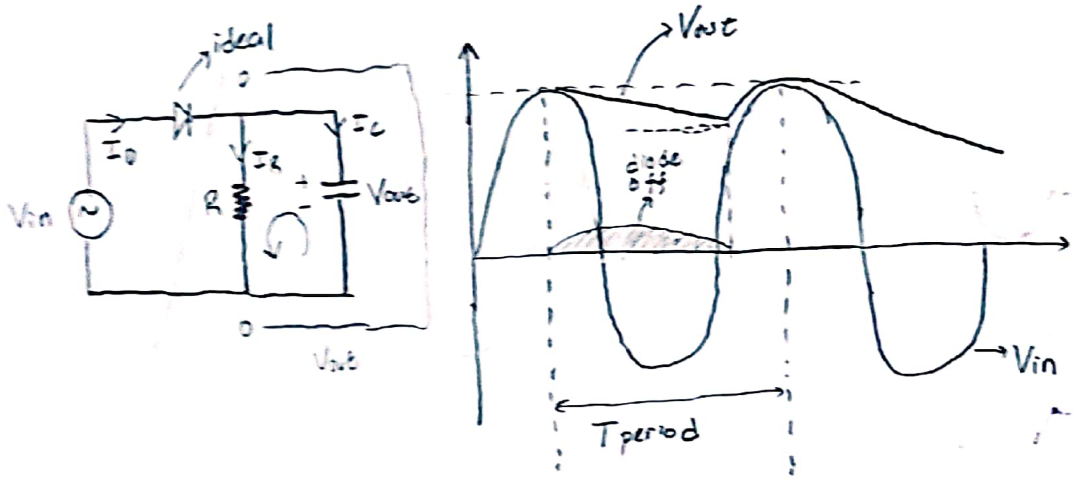
Tepe Seçiciler (Peak Detector)



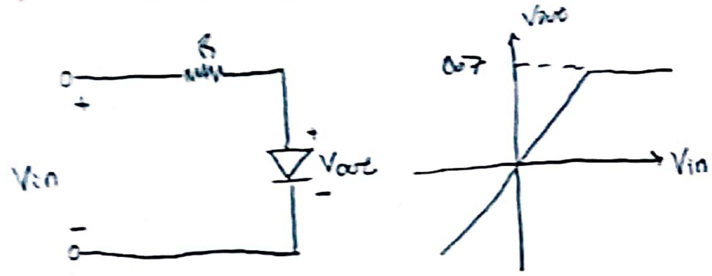
AC gerilimin tepe değerini tespit etmek için.

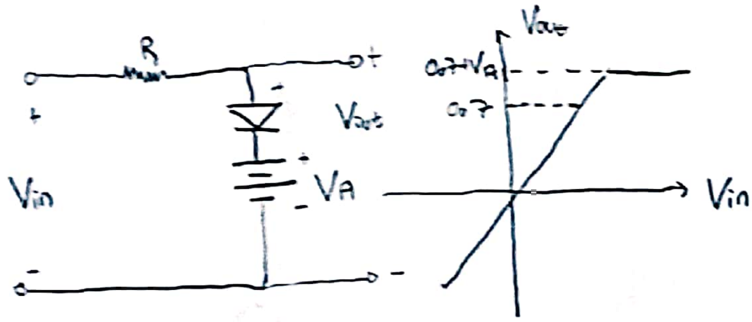


Max değeri görünce sonra düşünce Vin ters biaslanmış oluyor diot açık devre olarak davranıyor. Vout bundan dolayı değişmiyor.



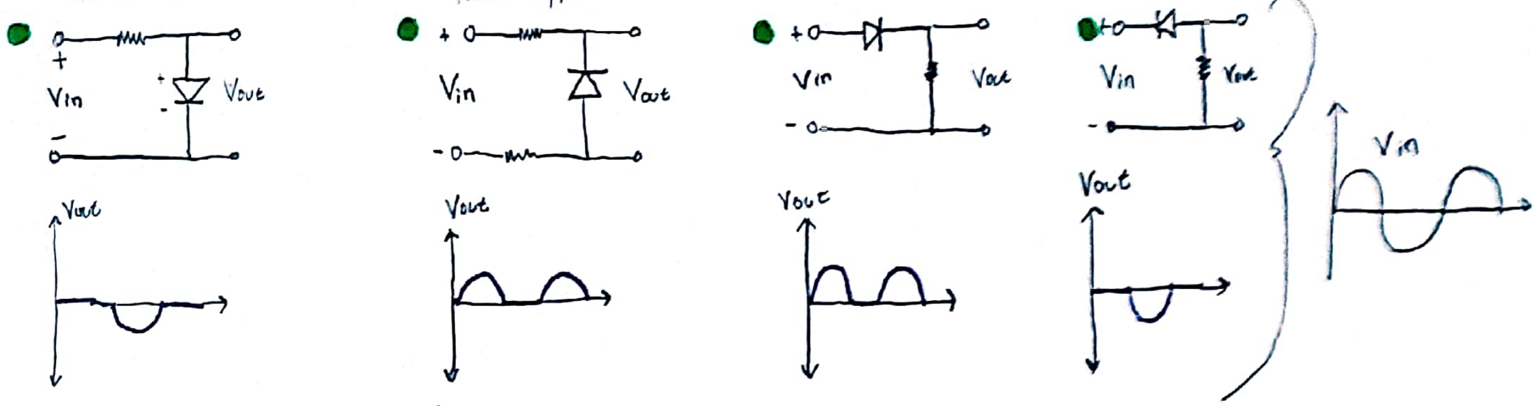
Kırpıcılar (Clippers)



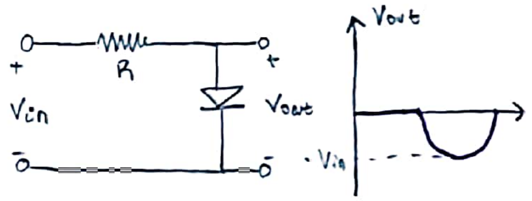


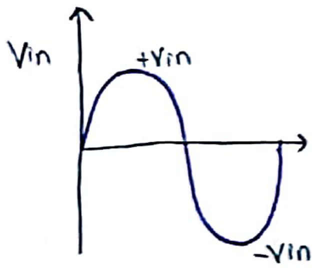
Parallel Clipper

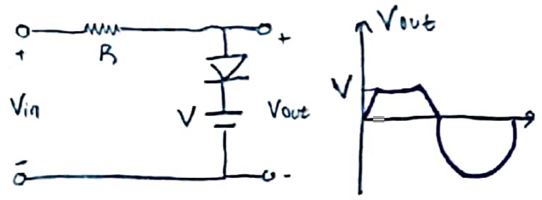
Parallel Clipper

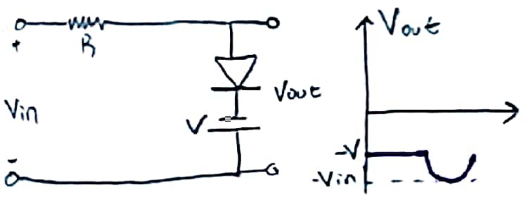


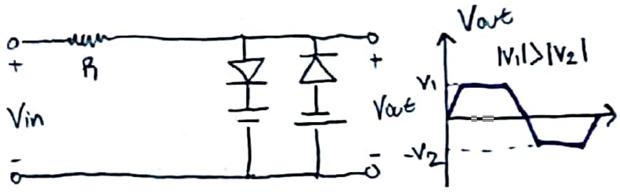
Parallel clipper circuit 'clips' any voltage that forward bias it.

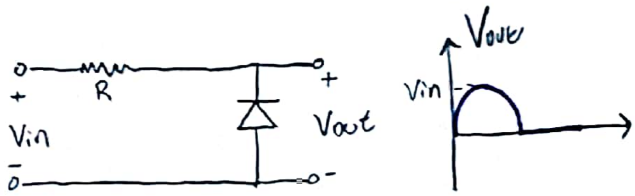
①


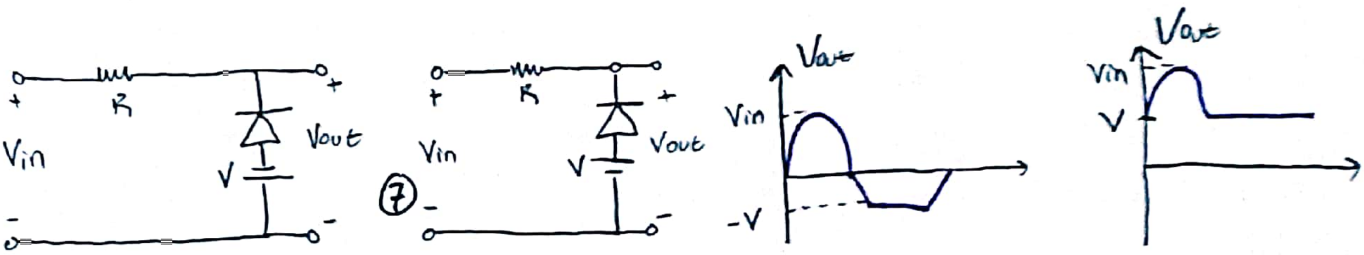


②


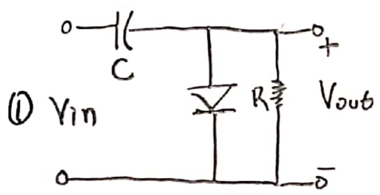
③


④


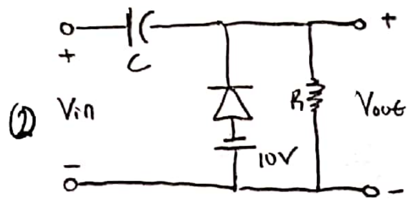
⑤


⑥ ⑦


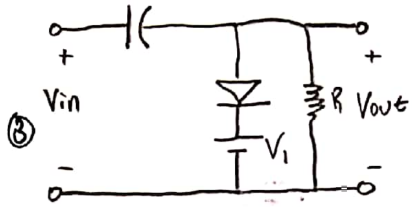
Clampers



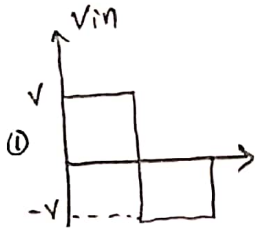
C
① Vin
R
Vout



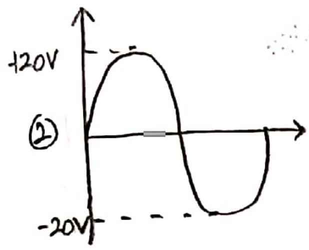
C
② Vin
R
Vout
10V



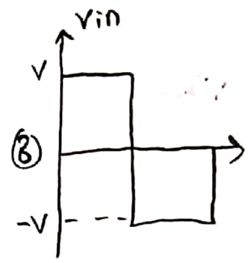
③ Vin
V_1
R Vout



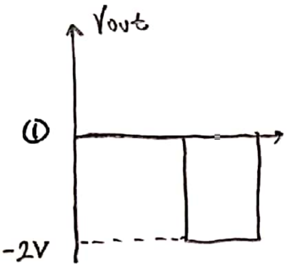
Vin
V
①
-V



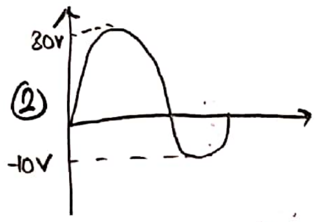
+20V
②
-20V



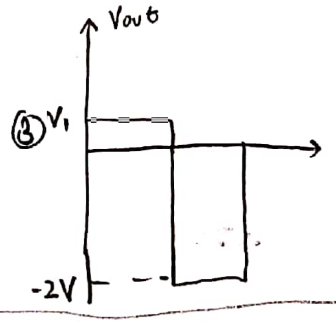
Vin
V
③
-V



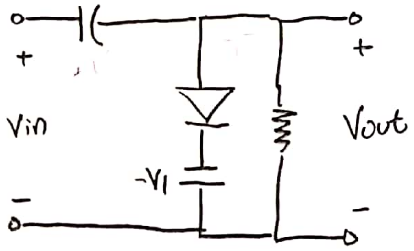
Vout
①
-2V



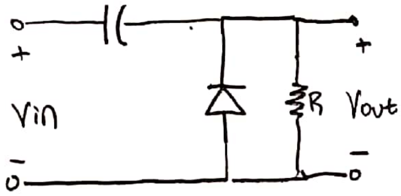
30V
②
-10V



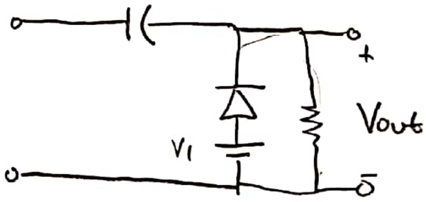
Vout
③ V_1
-2V



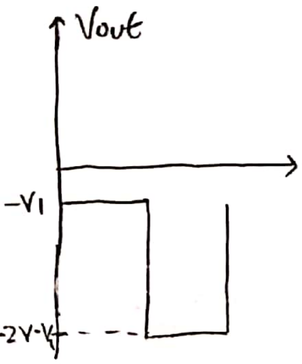
Vin
$-V_1$
Vout



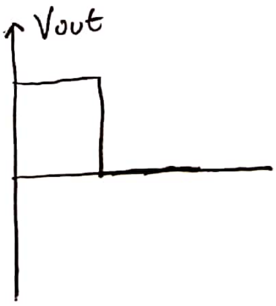
Vin
R Vout



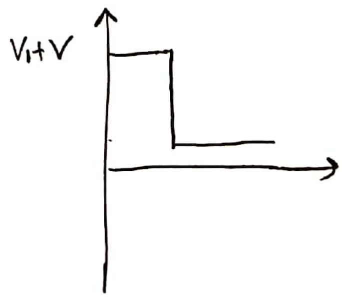
V_1
Vout



Vout
$-V_1$
$-2V-V_1$



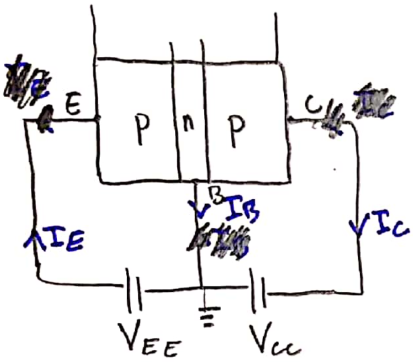
Vout



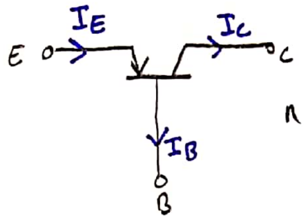
V_1+V

Transistors

- pnp, npn



$I_E = I_C + I_B$

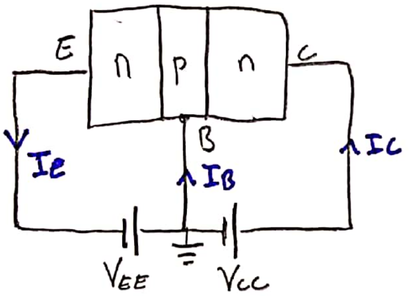


n type

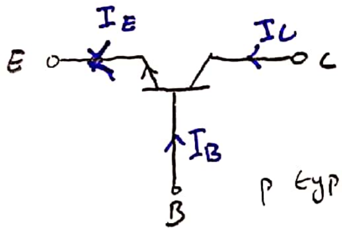
E: emiter
B: Base
C: collector

- The emitter-base junction is forward biased.
- The collector-base junction is reverse biased

$V_{CB} > 0$



$I_E = I_C + I_B$



p type

Approximations

$I_C = I_E$

$V_{BE} = 0.7V$ for silicon

Alpha

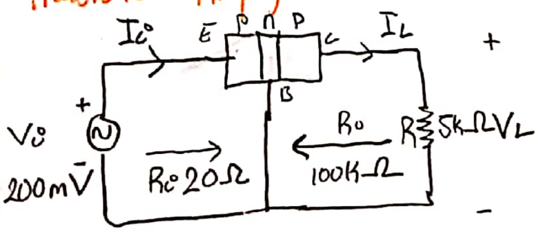
Alpha is ratio of I_C to I_E

$\alpha_{dc} = \frac{I_C}{I_E}$, $\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$

Ideally: $\alpha = 1$

In reality: $0.9 < \alpha < 0.998$

Transistor Amplification



$I_E = I_i = \frac{200mV}{20\Omega} = 10mA$

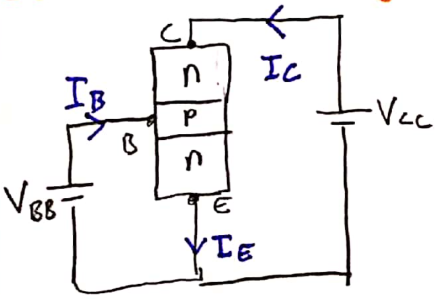
$I_C \cong I_e$

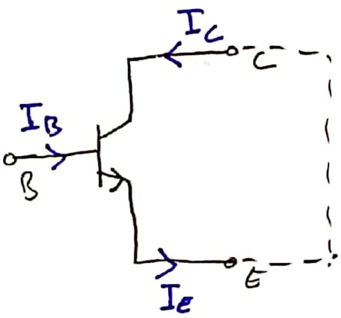
$I_C \cong 10mA \longrightarrow V_L = I_L \cdot R = 10mA \cdot 5k\Omega = 50V$

$\longrightarrow$ Voltage gain $A_V = \frac{V_L}{V_i} = \frac{50V}{200mV}$

$= 250$

Common-Emiter Configuration





$\boxed{I_E = I_C + I_B \text{ , } I_C = \alpha \cdot I_B}$ ideal currents

Beta (β)

β represents the amplification factor of a transistor.

In DC mode: $\beta_{dc} = \dfrac{I_C}{I_B}$

In AC mode: $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B}\Bigg|_{V_{CE}=\text{constant}}$

Relationship between amplification factors β and α:

$$\alpha = \frac{\beta}{\beta+1}, \quad \beta = \frac{\alpha}{\alpha-1} \longrightarrow \begin{array}{l} I_C = \beta \cdot I_B \\ I_E = (\beta+1)\cdot I_B \end{array}$$

Power Dissipation

Common Base:

$$P_{C\,max} = V_{CB} I_C$$

Common Emitter:

$$P_{C\,max} = V_{CE} I_C$$

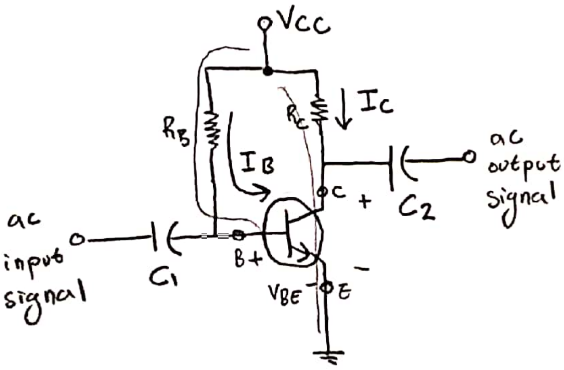
Common Collector:

$$P_{C\,max} = V_{CE} I_E$$

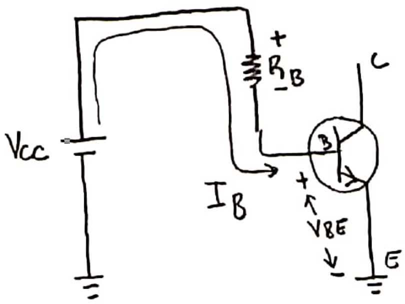
DC Biasing Circuits

- Fixed-bias circuit
- Emitter stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback.

Fixed Bias



The Base-Emitter Loop



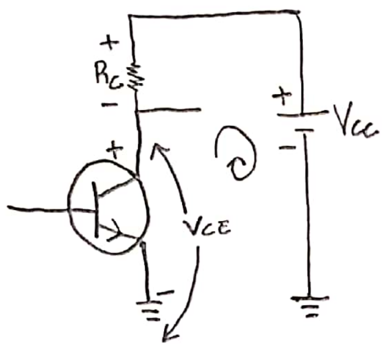
From Kirchoff's voltage law:

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Collector-Emitter Loop



Collector current:

$$I_C = \beta I_B$$

From Kirchoff's law:

$$V_{CE} = V_{cc} - I_C R_C$$

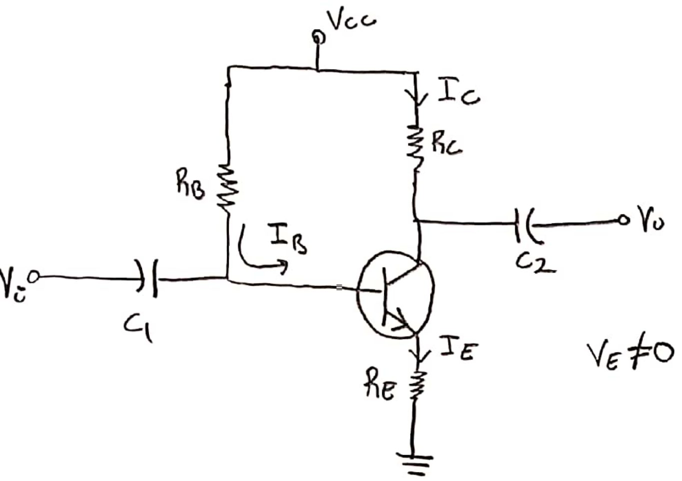
Saturation

When the transistor is operating in saturation, current through the transistor is at maximum possible value.

$$I_{C_{sat}} = \frac{V_{cc}}{R_C}$$

$$V_{CE} \cong 0$$

Emitter-Stabilized Bias Circuit



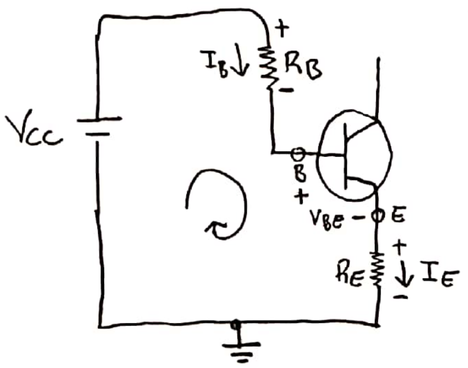
$V_E \neq 0$

Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.

$$V_{cc} - I_B \cdot R_B - V_{BE} - I_E \cdot R_E = 0$$

$$V_{cc} - I_C \cdot R_C - V_{CE} - I_E \cdot R_E = 0$$

Base Emitter Loop with R_E



From Kirchoff's voltage law:

$$V_{cc} - I_B \cdot R_B - I_E \cdot R_E - V_{BE} = 0$$

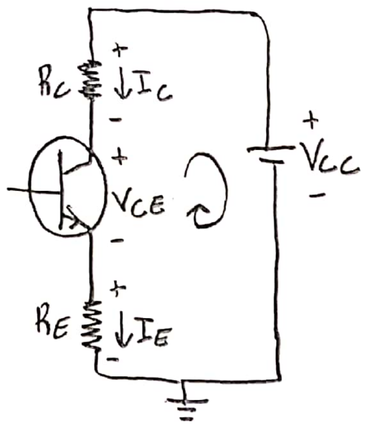
Since $I_E = (1+\beta) \cdot I_B$:

$$V_{cc} - I_B R_B - (1+\beta) \cdot I_B \cdot R_E - V_{BE} = 0$$

Solving for I_B:

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (1+\beta) \cdot R_E}$$

Collector-Emitter Loop with R_E



from Kirchoff's Law:

$$V_{CC} - I_E R_E - I_C R_C - V_{CE} = 0 \rightarrow \text{Saturation Level}$$

Since $I_E \cong I_C$:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R I_B = V_{BE} + V_E$$

$V_{CE\,cutoff}$:

$V_{CE} = V_{CC}$

$I_C = 0mA$

↓

base emitter is reverse biased

$I_{C\,sat}$:

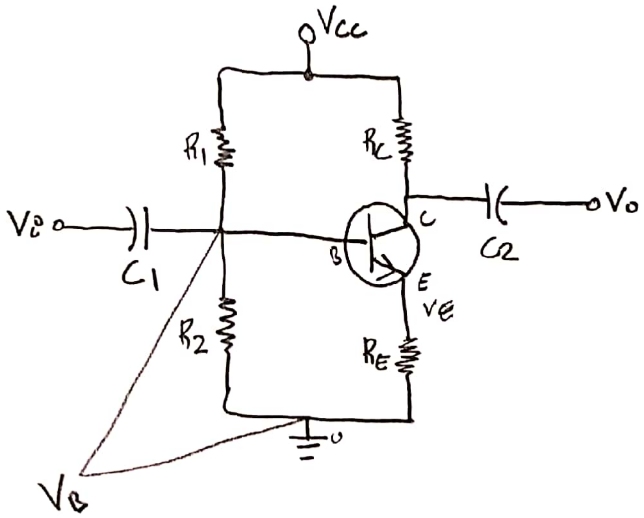
$V_{CE} = 0V$

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

↓

base-emitter is forward biased
collector-emitter is forward biased

Voltage Divider Bias



Approximate Analysis

Where $I_B \ll I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 \cdot V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10 R_2$:

$$I_E = \frac{V_E}{R_E} \text{ and } V_E = V_B - V_{BE}$$

From Kirchoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C \cdot (R_C + R_E)$$

Voltage Divider Bias Analysis

$$I_{C\,sat} = I_{C\,max} = \frac{V_{CC}}{R_C + R_E}$$

(Transistor saturation level)

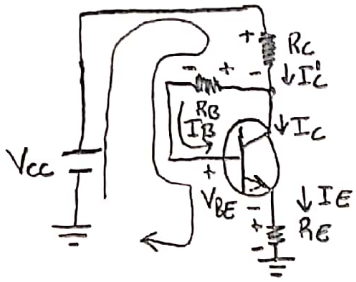
$V_{CE} = V_{CC}$
$I_C = 0mA$
(cutoff)

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$V_{CE} = 0V$
(saturation)

DC Bias with Voltage Feedback

Base-Emitter Loop



From Kirchoff's voltage law:

$$V_{CC} - I_C' R_C - I_B R_B - I_E R_E - V_{BE} = 0$$

Where $I_B \ll I_C$:

$$I_C' = I_C + I_B = I_C$$

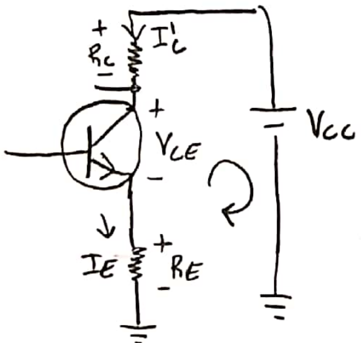
Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta \cdot I_B R_C - I_B R_B - V_{BE} - \beta \cdot I_B \cdot R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)}$$

Collector-Emitter Loop



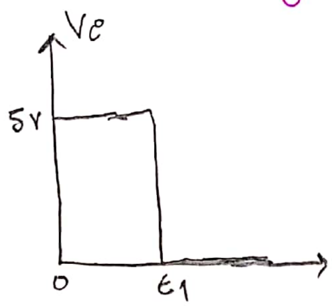
Applying Kirchoff's voltage law:

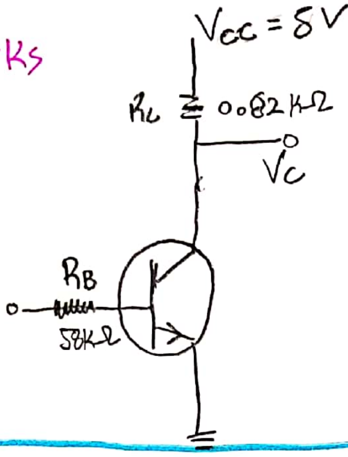
$$V_{CC} - V_{CE} - I_E R_E - I_C' R_C = 0$$

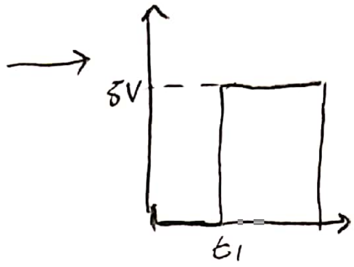
Since $I_C' \cong I_C$ and $I_C = \beta I_B$:

$$V_{CC} - V_{CE} - I_C (R_E + R_C) = 0$$

Transistor Switching Networks

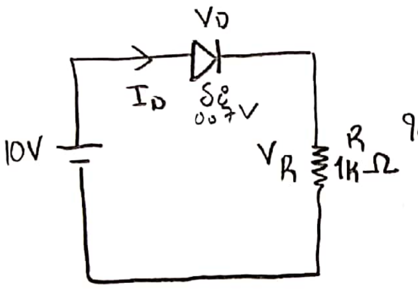


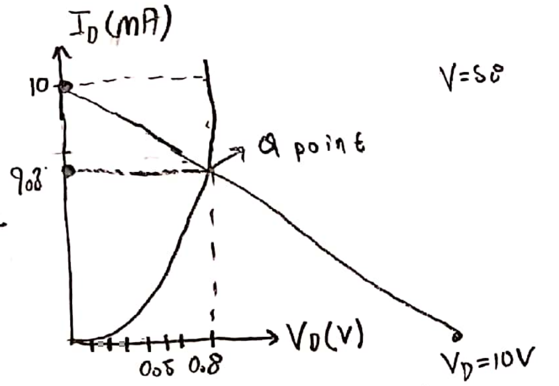




Examples

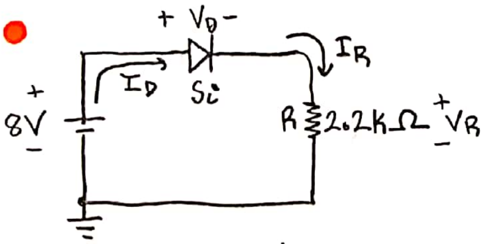
- (a) find V_{DQ} and I_{DQ}
  (b) find V_R





V=Si

akim akmaz potansiyel fark yok

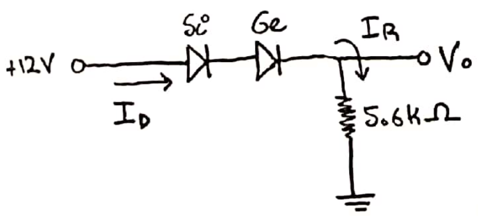


(a) determine V_D, V_R, I_D.

$V_D = 0.7V$

$V_R = E - V_D = 8V - 0.7V = 7.3V$

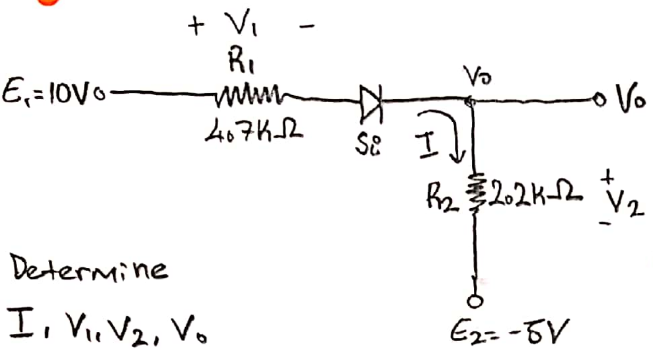
$I_D = I_R = \frac{V_R}{R} = \frac{7.3V}{2.2K\Omega} \cong 3.32mA$



Determine V_o and I_D

$V_o = 12V - V_{Si} - V_{Ge} = 12 - 0.7 - 0.3 = 11V$

$I_D = I_R = 11V / 5.6K\Omega \cong 1.96mA$



Determine

I, V_1, V_2, V_o

$$\rightarrow \frac{9.3 - V_o}{4.7K} = \frac{V_o + 5}{2.2K}$$

$$\hookrightarrow 20.46 - 2.2V_o = 4.7V_o + 23.5$$

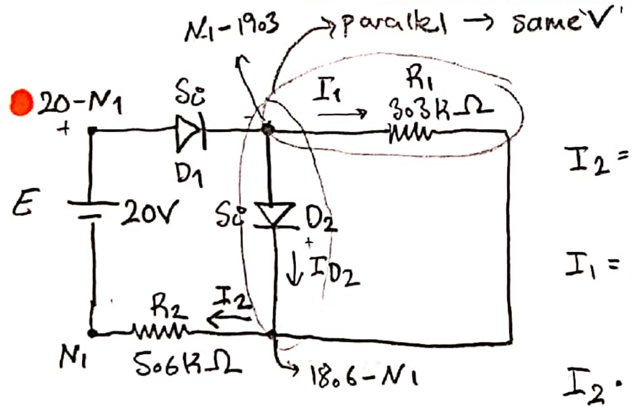
$$-3.04 = 6.9V_o$$

$$\underline{V_o \cong -0.44V}$$

$$I = \frac{V_o + 5V}{2.2K\Omega} \cong \frac{5V - 0.44}{2.2K\Omega} = 2.072mA$$

$$V_1 = I \cdot R_1 = 2.072mA \cdot 4.7K\Omega \cong 9.74V$$

$$V_2 = I \cdot R_2 = 2.072mA \cdot 2.2K\Omega \cong 4.56V$$



Determine I_1, I_2, I_{D_2}

$$I_2 = I_{D_2} + I_1$$

$$I_1 = \frac{V_{D_2}}{3.3K\Omega} = \frac{0.7V}{3.3K\Omega} = 0.212mA$$

$$I_2 \cdot R_2 = 18.6V \rightarrow I_2 = \frac{18.6V}{5.6K\Omega} = 3.32mA$$

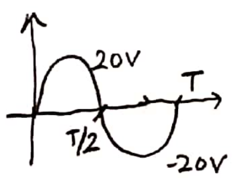
$$I_{D_2} = 3.32 - 0.212 = 3.11mA$$

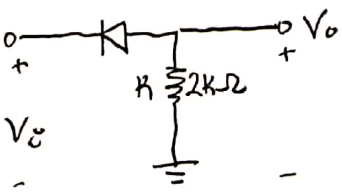
---

a) Sketch the output V_o and determine the dc level of the output for the network

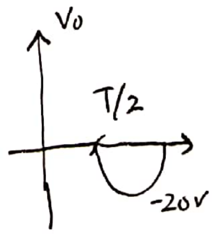
b) Repeat above since diode is replaced with silicon diode.

c) Repeat a and b if V_m is increased to 200V





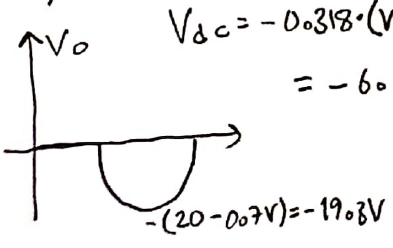
a)



$$V_{dc} = -0.318V \cdot V_m$$

$$= -0.318V \cdot 20V = -6.36V$$

b)



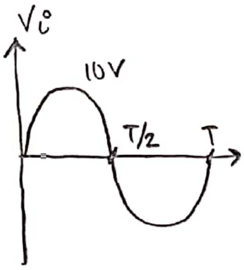
$$V_{dc} = -0.318 \cdot (V_m - 0.7V)$$

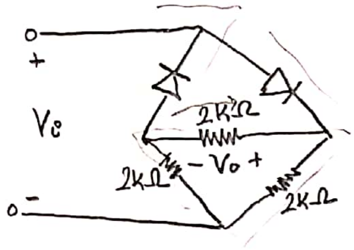
$$= -6.14V$$

c) $V_{dc} = -0.318 \cdot V_m = -0.318 \cdot 200V = -63.6V$

$V_{dc} = -0.318 \cdot (V_m - 0.7V) = -0.318 \cdot 199.3V = -63.38V$

- Determine the output waveform and calculate the output dc level and required PIV of each node.

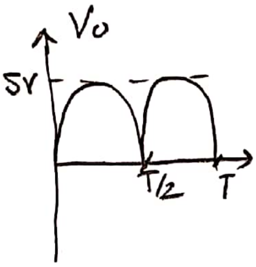




$V_i +\quad \longrightarrow \quad \frac{10V}{4k\Omega} \cdot 2k\Omega = V_o = 5V$

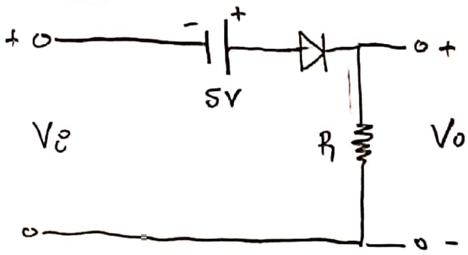
$V_i -\quad \longrightarrow \quad \frac{10V}{4k\Omega} \cdot 2k\Omega = V_o = 5V$

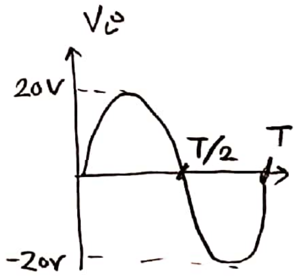
$\longrightarrow$



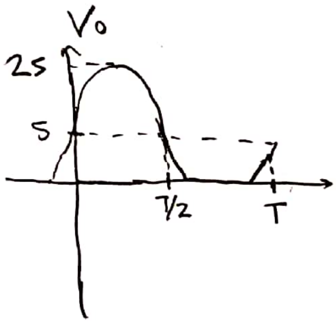
$V_{dc} = 0.636(5V) = 3.18V$

-

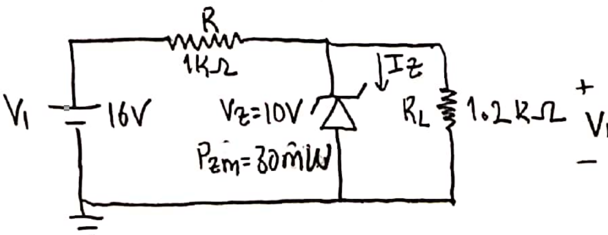




$\longrightarrow$

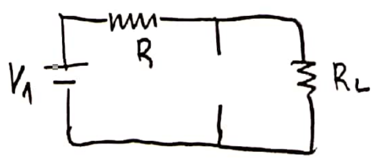


- (a) For the Zener diode network below, determine V_L, V_R, I_Z, P_Z
(b) Repeat part a for $R_L = 3k\Omega$



a) $V = \frac{R_L \cdot V_i}{R + R_L} = \frac{1.2k\Omega \cdot 16V}{1k\Omega + 1.2k\Omega} = 8.73V$

Since $8.73V < 10V = V_Z$, the diode is in the "off" state. Substituting the open circuit equivalent is:



$V_L = V = 8.73V$

$V_R = V_1 - V_L = 16V - 8.73V = 7.27V$

$I_Z = 0A$

$P_Z = V_Z I_Z = 10V \cdot 0A = 0W$

b) $V = \frac{3k\Omega \cdot 16V}{1k\Omega + 3k\Omega} = 12V$

Since $12V > 10V = V_Z$, the diode is in the "on" state.

$V_L = V = 10V$

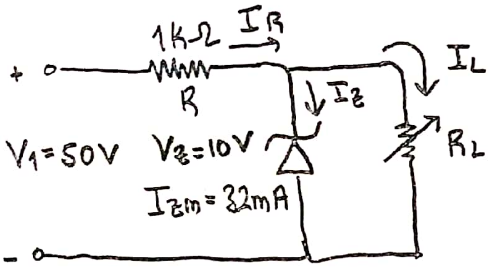
$V_R = V_1 - V_L = 16V - 10V = 6V$

$I_L = \frac{10V}{3k\Omega} = 3.33mA$

$I_R = \frac{6V}{1k\Omega} = 6mA$ $\quad \rightarrow P_Z = 10V \cdot 2.67mA = 26.7mW < 30mW$

$I_Z = I_R - I_L = 6mA - 3.33mA = 2.67mA$

(a) Determine the range of R_L and I_L that will result in V_{R_L}, being maintained at 10V.
(b) Determine the maximum W rating of the diode.



(a)
$$V = \frac{R_L \cdot 50V}{R + R_L} = \frac{R_L \cdot 50V}{1K\Omega + R_L} = 10V \rightarrow R_L = \frac{10K\Omega}{40V} = 250\Omega$$

$R_{L\,min} = 250\Omega$

$V_R = V_1 - V_L = 50V - 10V = 40V$

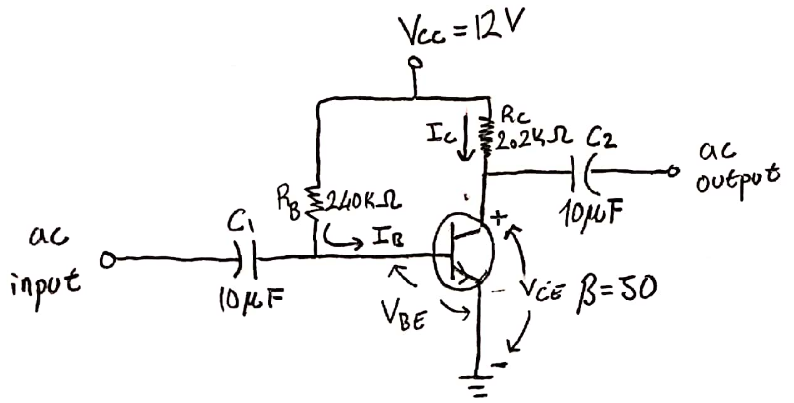
$$I_R = \frac{40V}{1K\Omega} = 40mA$$

$I_{L\,min} = I_R - I_{ZM} = 40mA - 32mA = 8mA$

$$R_{L\,max} = \frac{V_Z}{I_{L\,min}} = \frac{10V}{8mA} = 1.25K\Omega$$

(b) $P_{max} = V_Z \cdot I_{ZM} = 10V \cdot 32mA = 320mW$

Determine the following for the fixed-bias configuration. I_{BQ}, I_{CQ}, V_B, V_C, V_{BC}



$V_{CC} - I_B R_B - V_{BE} = 0$

$12V - I_B \cdot 240K\Omega - 0.7V = 0$

- $$I_B = \frac{12V - 0.7V}{240K\Omega} = 47.08\mu A$$

- $I_C = \beta \cdot I_B = 50 \cdot 47.08\mu A = 2.35mA$

$V_{CC} - I_C R_C - V_{CE} = 0$

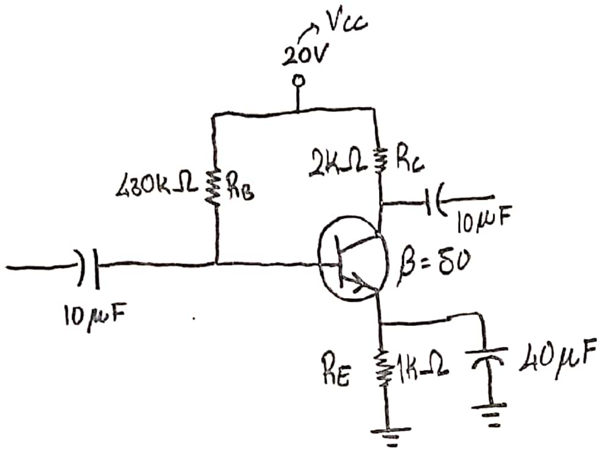
$12V - 2.35mA \cdot 2.2K\Omega - V_{CE} = 0$

$V_{CE} = 6.83V$

- $V_B = V_{BE} = 0.7V$
- $V_C = V_{CE} = 6.83V$
- $V_{BC} = V_B - V_C = 0.7V - 6.83V = -6.13V$

For the emitter bias network. Determine I_B, I_C, V_{CE}, V_C, V_E, V_B, V_{BC}

✓ ✓ ✓



$V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0$

$20V - I_B \cdot 430K\Omega - 0.7V - I_E \cdot 1K\Omega = 0 \rightarrow I_E = (\beta+1) I_B$

$20V - I_B \cdot 430K\Omega - 0.7V - (51) \cdot I_B \cdot 1K\Omega = 0$

- $I_B = \dfrac{20V - 0.7V}{430K\Omega + 51 \cdot 1K\Omega} = 40.1\,\mu A$

- $I_C = \beta \cdot I_B = 50 \cdot 40.1\,\mu A = 2.01\,mA$

$(\beta+1) \cdot I_B$

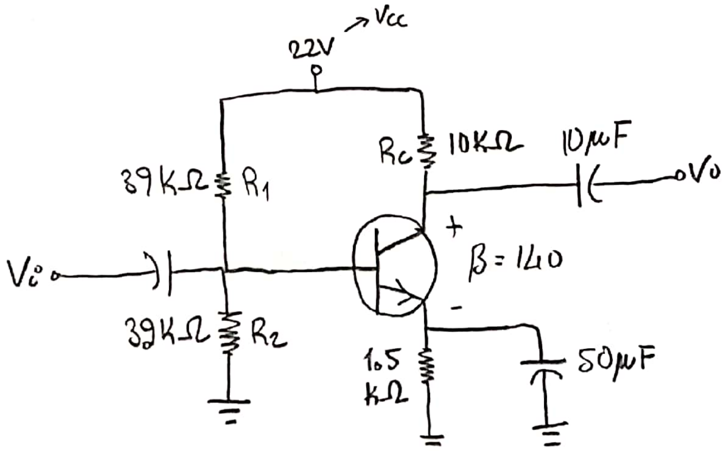
$V_{cc} - I_c R_c - V_{CE} - I_E R_E = 0$

$20V - 2.01mA \cdot 2K\Omega - V_{CE} - 51 \cdot 40.1\,\mu A \cdot 1K\Omega = 0$

- $V_{CE} = 20V - 6.08V = 13.97$

- $V_C = V_{CC} - I_C R_C = 15.98V$
- $V_E = V_C - V_{CE} = 2.01V$
- $V_B = V_{BE} + V_E = 2.71V$
- $V_{BC} = V_B - V_C = -13.27V$ (revese-bias as required)

Determine the dc bias voltage V_{CE} and the currat I_c for the voltage divider.



- $R_{Th} = R_1 \| R_2$

$= \dfrac{39K\Omega \cdot 3.9K\Omega}{39K\Omega + 3.9K\Omega} = 3.55K\Omega$ acts like R_B

- $E_{Th} = \dfrac{R_2 \cdot V_{cc}}{R_1 + R_2} = \dfrac{3.9K\Omega \cdot 22}{39K\Omega + 3.9K\Omega} = 2V$

$E_{Th} - I_B \cdot R_{Th} - V_{BE} - I_E \cdot R_E = 0$; $I_E \rightarrow (1+\beta) \cdot I_B$

- $I_B = \dfrac{E_{Th} - V_{BE}}{R_{Th} + (1+\beta) \cdot R_E} = \dfrac{2V - 0.7V}{3.55K\Omega + 141 \cdot 1.5K\Omega} = 6.5\,\mu A$

- $I_c = \beta \cdot I_B = 141 \cdot 6.5\,\mu A = 0.85\,mA$

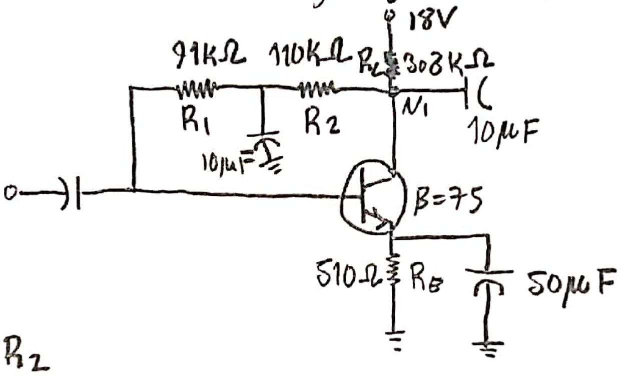
$V_{cc} - R_c I_c - V_{CE} - I_E R_E = 0$ → assume that $I_c \cong I_E$

$V_{CE} = V_{cc} - I_c (R_c + R_E)$

$V_{CE} = 22V - 0.85mA\,(10K\Omega + 1.5K\Omega)$

- $V_{CE} = 12.22V$

- Determine the dc level of I_B and V_C.



$R_B = R_1 + R_2$

$R_B = 91K\Omega + 110K\Omega = 201K\Omega$

$V_{CC} - I_B R_B - V_{BE} - \overbrace{I_E}^{(1+\beta)\cdot I_B} R_E - \underbrace{I_C}_{\beta I_B} R_C = 0$

- $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = 35.5\,\mu A$

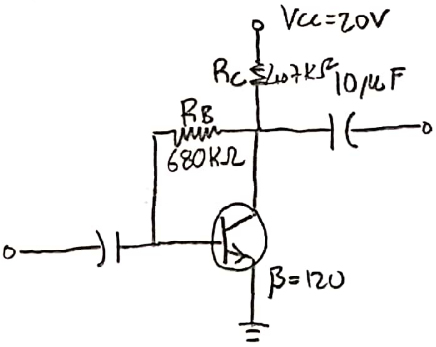
- $I_C = \beta I_B = 2.66\,mA$

- $V_{CC} - I_C R_C - V_C = 0$ for node N_1

$18V - 2.66mA \cdot 3.3K\Omega - V_C = 0$

$V_C = 9.22V$

- Determine I_C and V_{CE}, find V_B, V_C, V_E and V_{BC}



$V_{CC} - \overbrace{I_C}^{\beta I_B} R_C - I_B R_B - V_{BE} = 0$

$V_{CC} - I_B(\beta R_C + R_B) - V_{BE} = 0$

- $I_B = \dfrac{V_{CC} - V_{BE}}{(\beta R_C + R_B)} = \dfrac{20 - 0.7}{120 \cdot 4.7K\Omega + 680K\Omega} = 15.51\,\mu A$

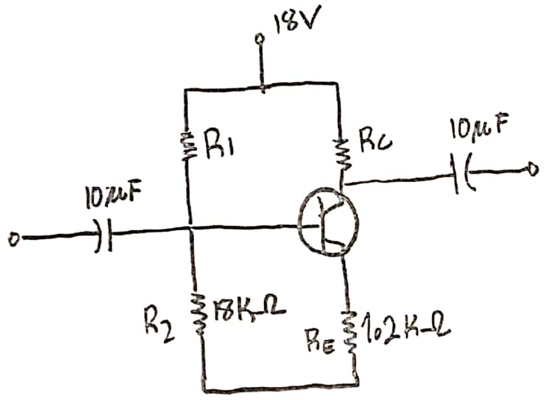
- $I_C = \beta I_B = 120 \cdot 15.51\,\mu A = 1.86\,mA$

- $V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C = 11.26V$

- $V_B = V_{BE} = 0.7V$
- $V_C = V_{CE} = 11.26V$
- $V_E = 0V$
- $V_{BC} = V_B - V_C = -10.56V$

- $I_C = 2mA$ and $V_{CE} = 10V$, determine R_1 and R_C



- $V_E = I_E R_E \cong I_C R_C$
  $= 2mA \cdot 1.2K\Omega = 2.4V$

- $V_B = V_{BE} + V_E = 0.7V + 2.4V = 3.1V$

$$V_B = \frac{V_{CC} \cdot R_2}{R_1 + R_2} = \frac{18V \cdot 18K\Omega}{18K\Omega + R_1} = 3.1V \rightarrow R_1 = 86.52\ K\Omega$$

- $R_C = \dfrac{V_{RC}}{I_C} = \dfrac{V_{CC} - V_C}{I_C}$

$V_C = V_{CE} + V_E = 10V + 2.4V = 12.4V$

$$R_C = \frac{18V - 12.4V}{2mA} = 2.8K\Omega$$

[redacted]

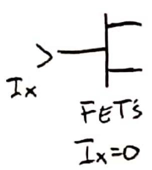
FETS and BJTs

Similarities:

- Amplifiers
- Switching devices
- Impedance matching circuits

Differences:

- FETs are voltage controlled devices. BJTs are current controlled devices.
- FETs have a higher input impedance. BJTs have higher gains.
- FETs are less sensitive to temperature variations and are more easily integrated on ICs.
- FETs are generally more static sensitive than BJTs.



FET Types

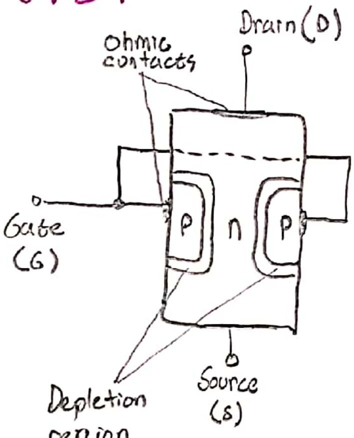
JFET: Junction Fet

MOSFET: Metal-Oxide-Semiconductor FET

D-MOSFET: Depletion MOSFET

E-MOSFET: Enhancement MOSFET

JFET

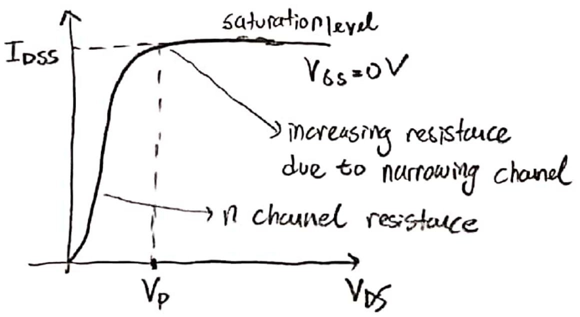


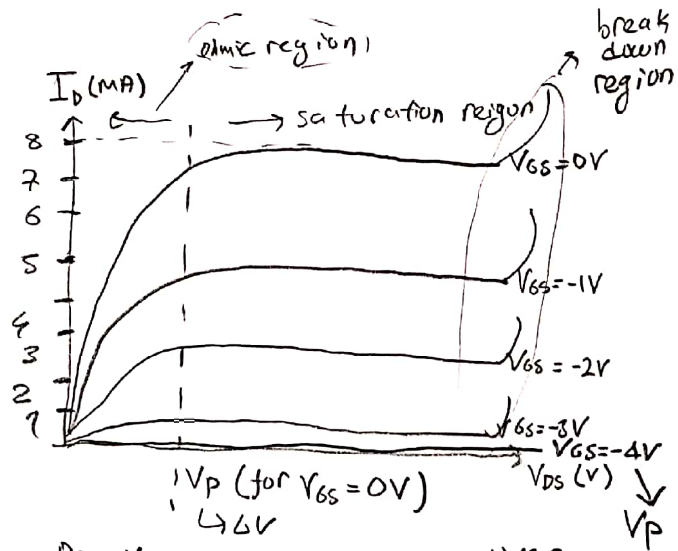
There are three basic operating conditions for a JFETs:

- $V_{GS}=0$, V_{DS} increasing to some positive value.
- $V_{GS}<0$, V_{DS} at some positive value.
- Voltage-controlled resistor.

if $V_{GS}=0$ and V_{DS} is further increased to a more positive voltage, then the depletion zone gets so large that it pinchess of the n-channell.

Saturation





Ohmic region:

- The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance r_d. As V_{GS} becomes more negative the resistance r_d increases.

$$r_d=\frac{r_o}{\left|1-\frac{V_{GS}}{V_P}\right|}$$

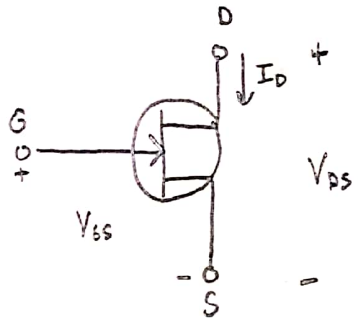
At the pinch off point: (V_P)

- Any further increase in V_{GS} does not produce any increase in I_D, V_{GS} at pinch off is denoted as V_P.
- I_D is at saturation. It's referred as I_{DSS}.
- The ohmic value of the chanel is maximum.

As V_{GS} becomes more negative:

- V_P (pinch off voltage) becomes lower
- I_D decreases ($I_D<I_{DSS}$) even though V_{DS} is increased.
- Eventually I_D reaches 0A. V_{GS} at this point is called V_P or $V_{GS(off)}$
- The depletion region increases.

N-Channel JFET symbol

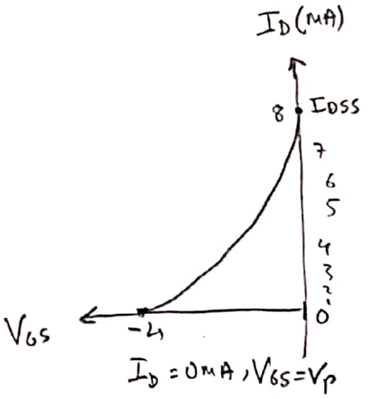


The transfer characteristic of input-to-output is not as straightforward in a JFET as it is in a BJT.

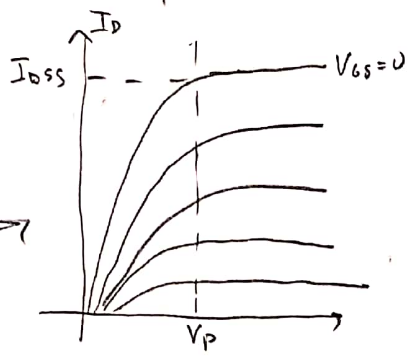
In a BJT, β indicates the relationship between I_B (input) and I_C (output).

In a JFET, the relationship between V_{GS} (input) and I_D (output) is:

$$\boxed{I_D = I_{DSS} \cdot \left[1 - \frac{V_{GS}}{V_P}\right]^2}$$



same



Plotting The JFET Transfer Curve

Using I_{DSS} and V_P values found in specification sheet, the transfer curve can be plotted according to these three steps:

Step 1

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \longrightarrow \text{solving for } V_{GS} = 0V$$

Step 2

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \longrightarrow \text{solving for } V_{GS} = V_P$$

Step 3

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \longrightarrow \text{solving for } V_{GS} = 0V \text{ to } V_P$$