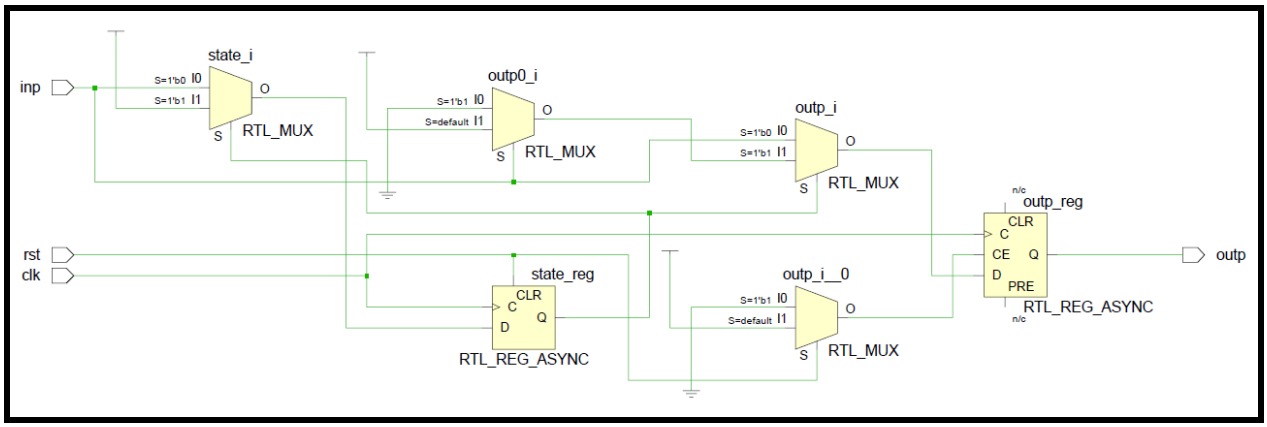
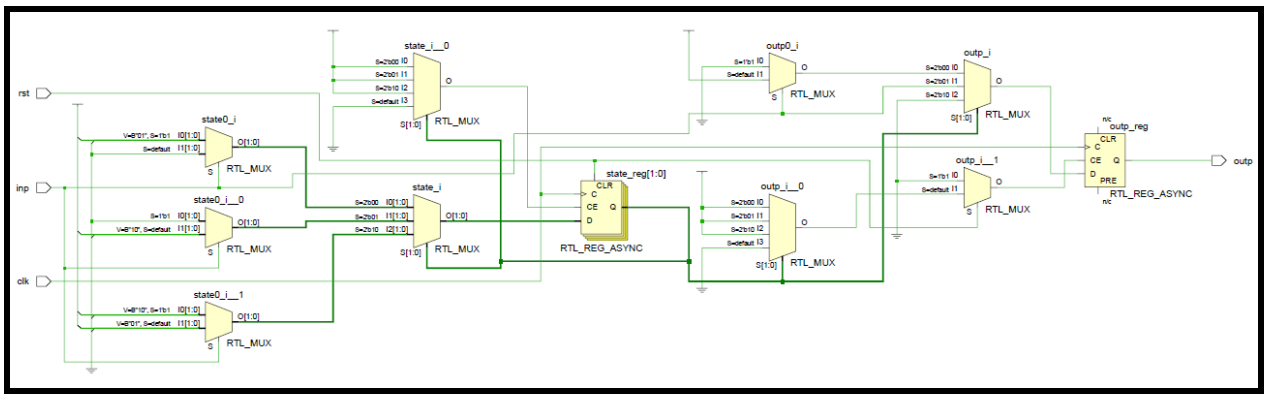
COMPUTER ORGANIZATION LABORATORY

VERILOG DESIGN OF SEQUENTIAL CIRCUITS FOR SIMPLE ARITHMETIC OPERATIONS

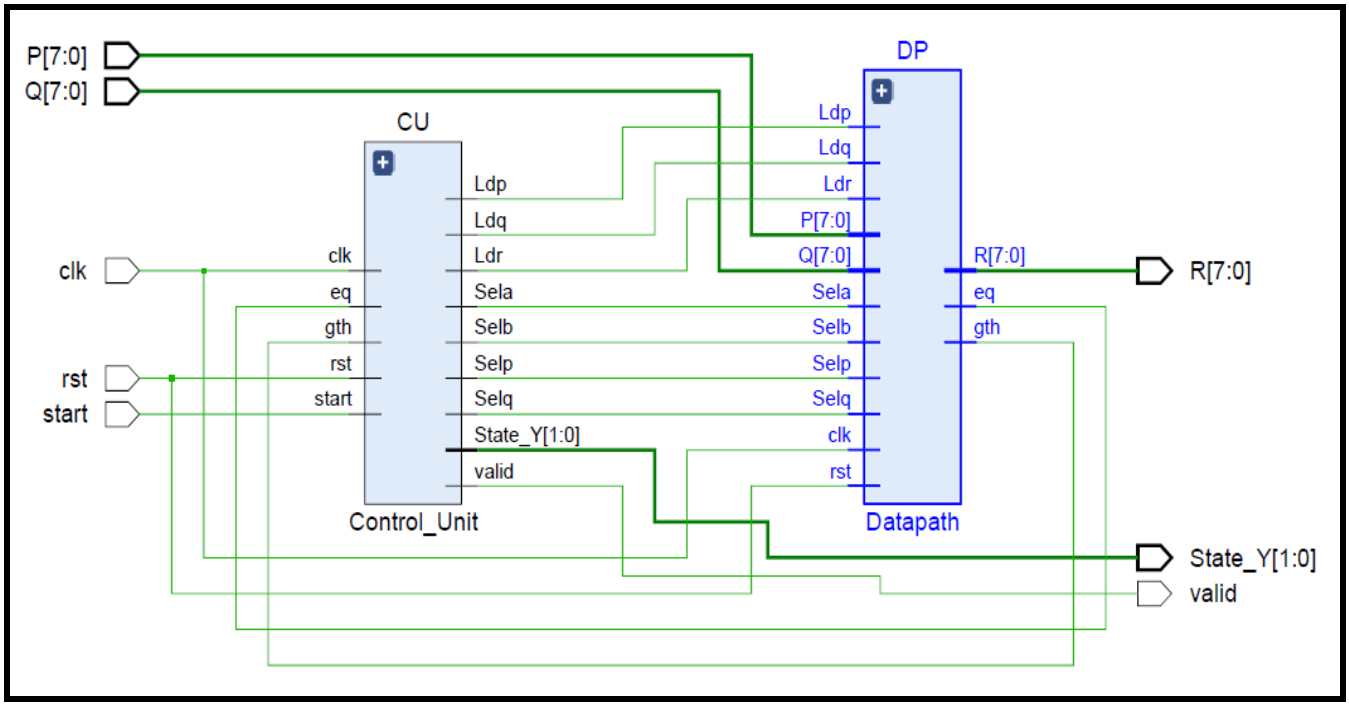
Schematic Diagrams:



Two's Complement Converter



Multiple of Three Detector



Sequential GCD Calculator

Hardware Requirements and Critical Path Delay

Board Used: Nexys4 DDR

CIRCUIT	HARDWARE REQUIREMENTS	CRITICAL PATH DELAY
Two's Complement Converter	3 Slice LUTs, 2 Slice Registers, 4 Bonded IOB, 1 BUFGCTRL	4.090 ns
Multiple of Three Detector	4 Slice LUTs, 3 Slice Registers, 4 Bonded IOB, 1 BUFGCTRL	4.090 ns
Sequential GCD Calculator	**Datapath**: 27 Slice LUTs, 24 Slice Registers **Control Path**: 5 Slice LUTs, 4 Slice Registers **Total**: 32 Slice LUTs, 28 Slice Registers, 30 Bonded IOB, 1 BUFGCTRL	6.498 ns

Maximum Usable Clock Frequency

We know, maximum usable clock frequency is the reciprocal of the critical path delay. The maximum usable clock frequencies of the 3 circuits are as follows:

- Two's Complement Converter: **244.499 MHz**
- Multiple of Three Detector: **244.499 MHz**
- Sequential GCD Calculator: **153.894 MHz**