- **Full Look-Ahead for High-Speed Operations on Long Words**

- **Input Clamping Diodes Minimize Transmission-Line Effects**

- **Darlington Outputs Reduce Turn-Off Time**

- **Arithmetic Operating Modes:**
  Addition
  Subtraction
  Shift Operand A One Position
  Magnitude Comparison
  Plus Twelve Other Arithmetic Operations

- **Logic Function Modes:**
  Exclusive-OR
  Comparator
  AND, NAND, OR, NOR
  Plus Ten Other Logic Operations

SN54LS181, SN54S181 . . . J OR W PACKAGE
SN74LS181, SN74S181 . . . DW OR N PACKAGE
(TOP VIEW)

$\overline{B0}$	1	24	V_{CC}
$\overline{A0}$	2	23	$\overline{A1}$
S3	3	22	$\overline{B1}$
S2	4	21	$\overline{A2}$
S1	5	20	$\overline{B2}$
S0	6	19	$\overline{A3}$
C_n	7	18	$\overline{B3}$
M	8	17	$\overline{G}$
$\overline{F0}$	9	16	C_{n+4}
$\overline{F1}$	10	15	$\overline{P}$
$\overline{F2}$	11	14	A = B
GND	12	13	$\overline{F3}$
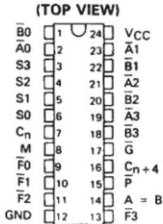
SN54LS181, SN54S181 . . . FK PACKAGE
(TOP VIEW)

S2	5	25 $\overline{A2}$
S1	6	24 $\overline{B2}$
S0	7	23 $\overline{A3}$
NC	8	22 NC
C_n	9	21 $\overline{B3}$
M	10	20 $\overline{G}$
$\overline{F0}$	11	19 C_{n+4}
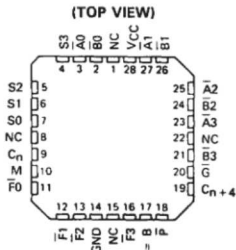
NC - No internal connection

TYPICAL ADDITION TIMES

NUMBER OF BITS	ADDITION TIMES		PACKAGE COUNT		CARRY METHOD BETWEEN ALUs
	USING 'LS181 AND 'S182	USING 'S181 AND 'S182	ARITHMETIC/ LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	24 ns	11 ns	1		NONE
5 to 8	40 ns	18 ns	2		RIPPLE
9 to 16	44 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	68 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The 'LS181 and 'S181 are arithmetic logic units (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54S182 or SN74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'S182 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under typical applications data for the 'S182.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

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description (continued)

The 'LS181 and 'S181 will accommodate active-high data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	F_0	F_1	F_2	F_3	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1, which requires an end-around or forced carry to provide A−B.

The 'LS181 or 'S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

| INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A $\geqslant$ B	A $\leqslant$ B
H	L	A $<$ B	A $>$ B
L	H	A $>$ B	A $<$ B
L	L	A $\leqslant$ B	A $\geqslant$ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of −55 °C to 125 °C; Series 74LS and 74S devices are characterized for operation from 0 °C to 70 °C.

signal designations

In both Figures 1 and 2, the polarity indicators ($\triangleright$) indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'LS181 and 'S181, together with the 'S182, can be used with the signal designation of either Figure 1 or Figure 2.

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logic symbols† and signal designations (active-low data)
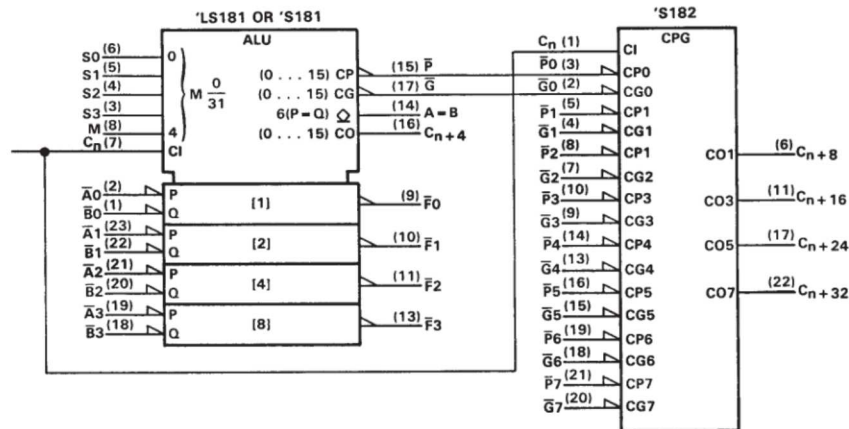
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
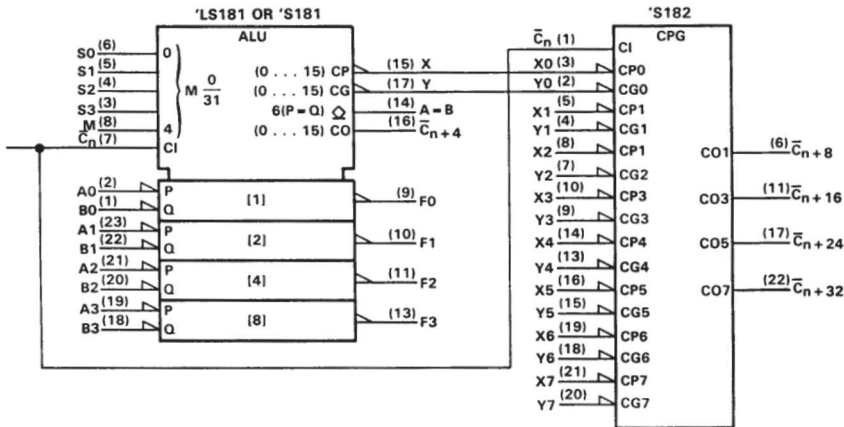Pin numbers shown are for dual-in-line and "small outline" packages.

FIGURE 1 (USE WITH TABLE 1)

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A‡	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

‡Each bit is shifted to the next more significant position.

logic symbols† and signal designations (active-high data)

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        'LS181 OR 'S181                                    'S182
             ALU                          C̄n (1)           CPG
 S0 (6) ─│0                              X0 (3)──▷│CI
 S1 (5) ─│                               Y0 (2)──▷│CP0
 S2 (4) ─│  M  0        (0...15) CP (15) X         │CG0
 S3 (3) ─│    ─────     (0...15) CG (17) Y  X1 (5)─▷│CP1
  M (8) ─│4   31        6(P=Q) ◇    (14) A=B Y1 (4)─▷│CG1
 C̄n (7)─│CI            (0...15) CO (16) C̄n+4 X2 (8)─▷│CP1                CO1 (6) C̄n+8
                                            Y2 (7)─▷│CG2
 A0 (2)──│P                                 X3 (10)─▷│CP3               CO3 (11) C̄n+16
 B0 (1)──│Q    [1]              (9) F0       Y3 (9)─▷│CG3
 A1 (23)─│P                                 X4 (14)─▷│CP4               CO5 (17) C̄n+24
 B1 (22)─│Q    [2]             (10) F1       Y4 (13)─▷│CG4
 A2 (21)─│P                                 X5 (16)─▷│CP5               CO7 (22) C̄n+32
 B2 (20)─│Q    [4]             (11) F2       Y5 (15)─▷│CG5
 A3 (19)─│P                                 X6 (19)─▷│CP6
 B3 (18)─│Q    [8]             (13) F3       Y6 (18)─▷│CG6
                                            X7 (21)─▷│CP7
                                            Y7 (20)─▷│CG7
```

†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for dual-in-line and "small outline" packages.

FIGURE 2 (USE WITH TABLE 2)

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	$F = \overline{A}$	$F = A$	$F = A$ PLUS 1
L	L	L	H	$F = \overline{A + B}$	$F = A + B$	$F = (A + B)$ PLUS 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
L	L	H	H	$F = 0$	$F = $ MINUS 1 (2's COMPL)	$F = $ ZERO
L	H	L	L	$F = \overline{AB}$	$F = A$ PLUS $A\overline{B}$	$F = A$ PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	$F = A$ MINUS B MINUS 1	$F = A$ MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	$F = A$ PLUS AB	$F = A$ PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	$F = A$ PLUS B	$F = A$ PLUS B PLUS 1
H	L	H	L	$F = B$	$F = (A + \overline{B})$ PLUS AB	$F = (A + \overline{B})$ PLUS AB PLUS 1
H	L	H	H	$F = AB$	$F = AB$ MINUS 1	$F = AB$
H	H	L	L	$F = 1$	$F = A$ PLUS A†	$F = A$ PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	$F = (A + B)$ PLUS A	$F = (A + B)$ PLUS A PLUS 1
H	H	H	L	$F = A + B$	$F = (A + \overline{B})$ PLUS A	$F = (A + \overline{B})$ PLUS A PLUS 1
H	H	H	H	$F = A$	$F = A$ MINUS 1	$F = A$

† Each bit is shifted to the next more significant position.

logic diagram (positive logic)
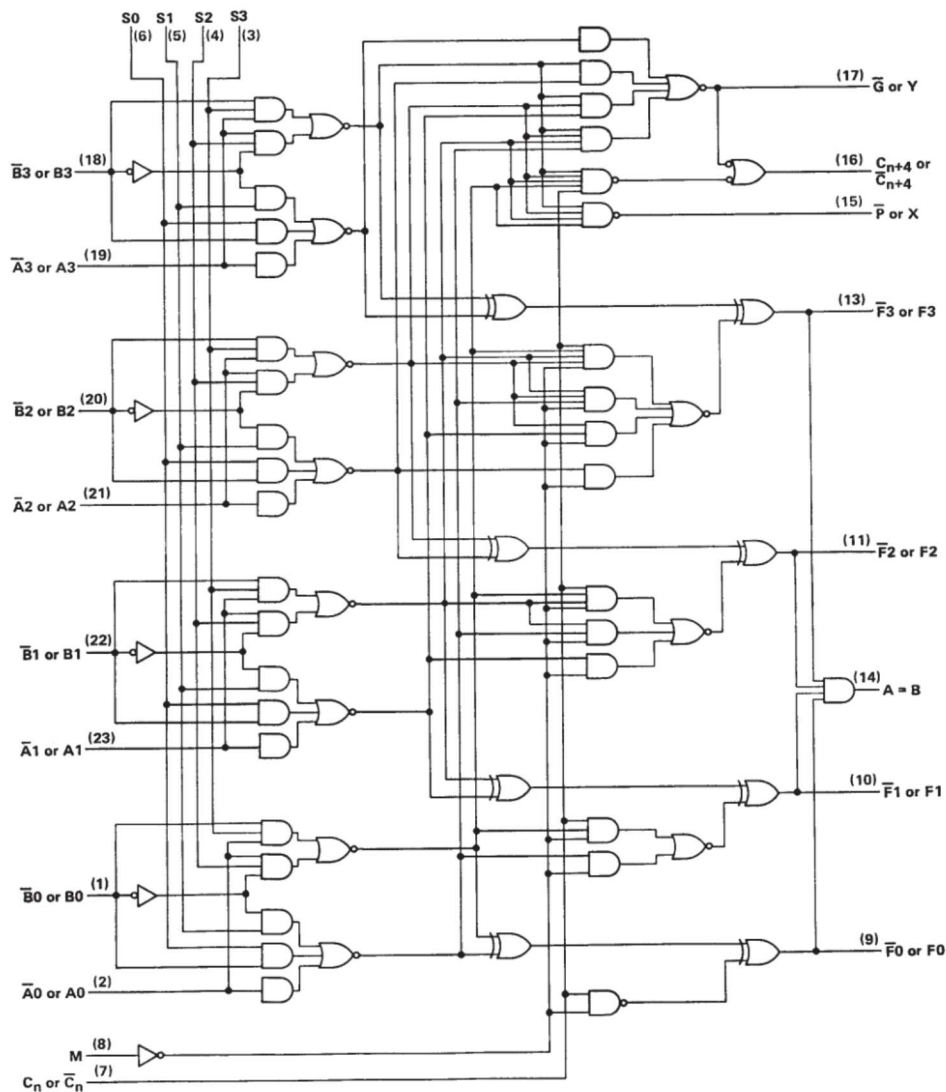
Pin numbers shown are for DW, J, N, and W packages.