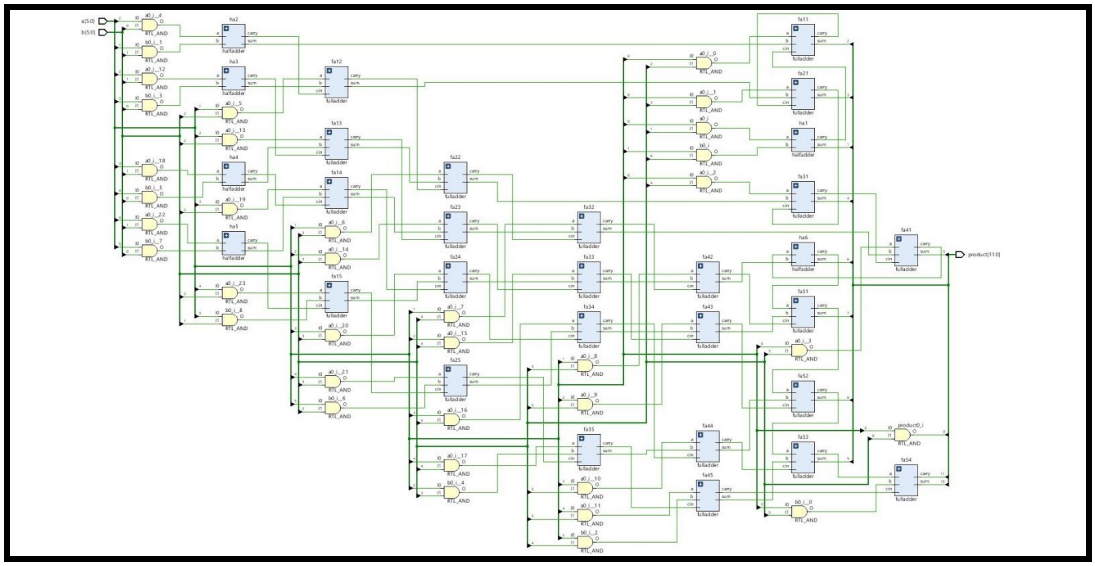
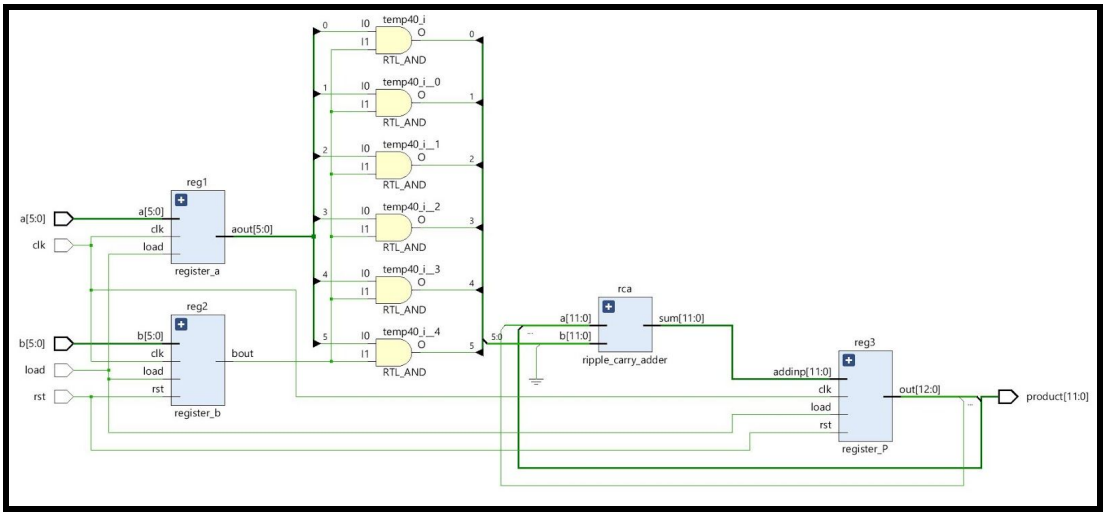
Computer Organization Laboratory

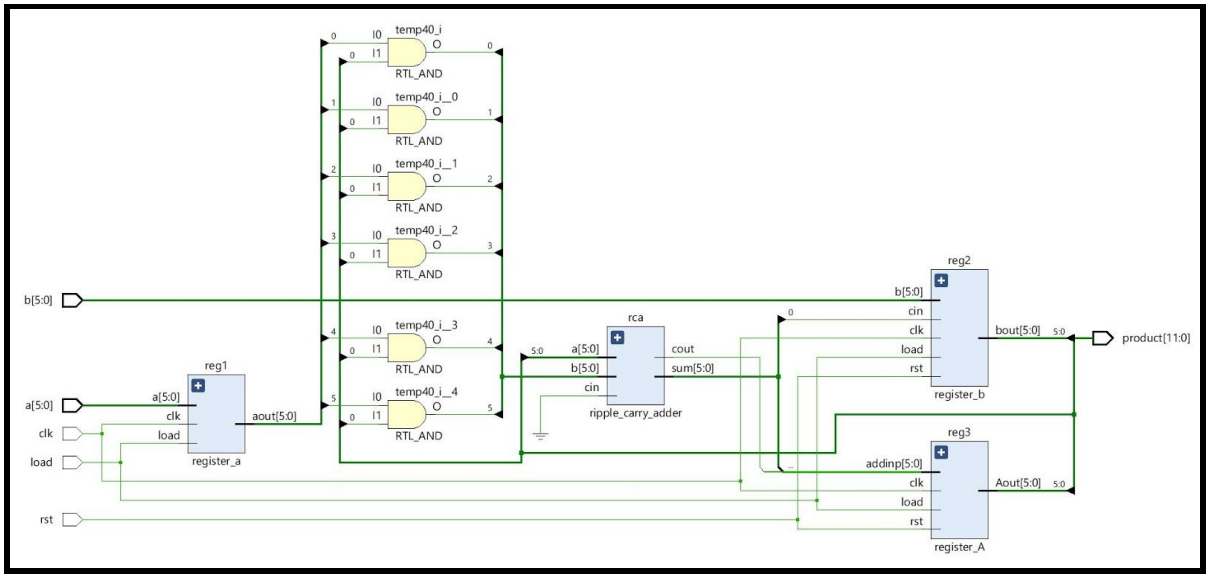
Assignment 3

Design of Unsigned Multipliers

Schematic Diagrams: (From top to Bottom: Combinational Multiplier, Sequential Multiplier (Left Shift) and Sequential Multiplier (Right Shift))







Comparison :

Multiplier Type	Hardware Requirements	Critical Path Delay (in ns)
Combinational Unsigned Binary Multiplier	43 CLB LUTs, 24 Bonded IOB	5.958
Sequential Unsigned Binary Multiplier (Left Shift Version)	29 CLB LUTs, 24 CLB Registers, 27 Bonded IOB, 1 Global Clock Buffer	2.384
Sequential Unsigned Binary Multiplier (Right Shift Version)	15 CLB LUTs, 18 CLB Registers, 27 Bonded IOB, 1 Global Clock Buffer	2.392

Maximum Usable Clock Frequency :

- Combinational Unsigned Binary Multiplier : 167.84 MHz
- Sequential Unsigned Binary Multiplier (Left Shift) : 419.46 MHz
- Sequential Unsigned Binary Multiplier (Right Shift) : 418.06 MHz

FPGA Used : Kintex Ultrascale Alphadata Board