

Operating systems :

OS : Interface b/w user & h/w

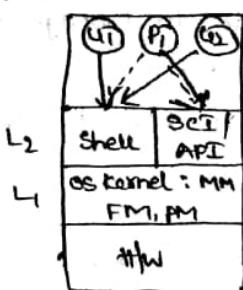
→ Collection of progs that control system

→ Resource manager (h/w & sw)

→ Set of utilities to simplify Application development

→ Acts like a Govt.

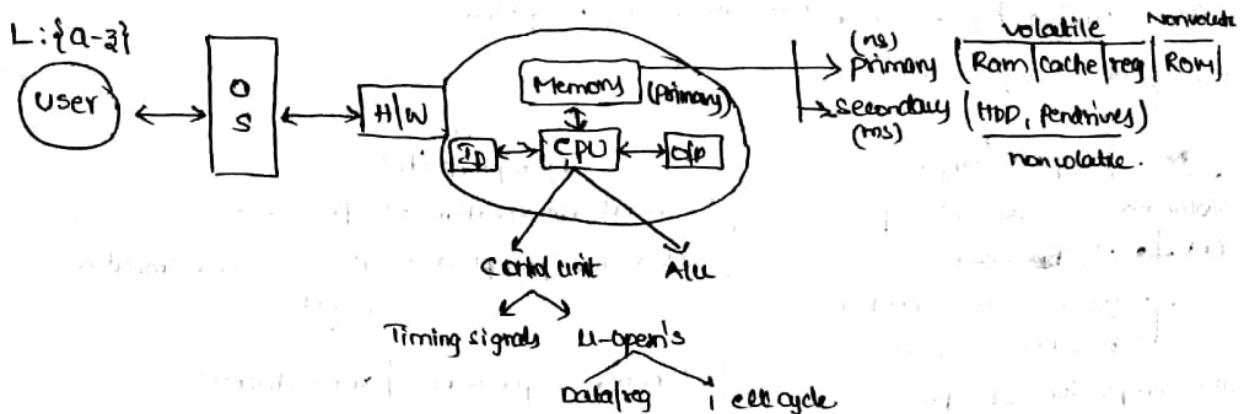
OS :



User Interface
H/W Interface

*) Von-neumann Arch (stored prog concept of computation)

→ loaded into mem for execution



Functions and Goals of os

Goals : (CEPSRR)

→ Convenience (easy to use)

→ Efficiency (utilization, managing)

→ portability (Run on any platform)

→ scalability (Accept changes)

→ Reliability (state should be always correct)

→ Robustness (small error shouldn't break os)

*) Primary Goals may change Acc to domains.

→ personal computing : Convenience (primary)
Efficiency (secondary)

→ Real time systems : Efficiency

Hard soft
(space, Airdate) (watching, arms)
Reliability Robustness

→ smart phone computing : power efficiently

Functions :

→ Device mgmt

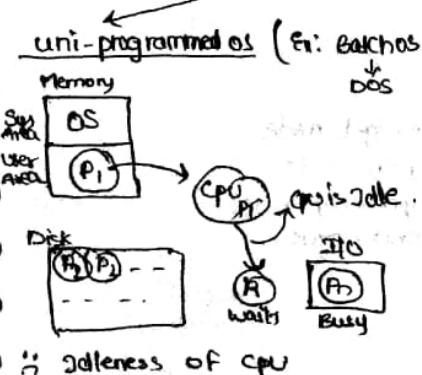
→ Memory mgmt

→ process mgmt

→ File mgmt

Types of os :

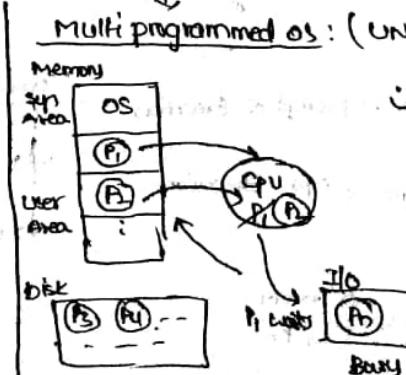
Based on disk technology



Multi programmed os : (UNIX, LINUX, WINDOWS, MAC)

↳ Max CPU utilization ie - throughput

(Num of jobs completed
Per unit time)



Definition of Multiprogramming :

- Ability of OS to manage multiple ready to run programs in memory is called Multiprogramming.
- Multiplexing of CPU among ready programs in memory is called multiprogramming

Types of Mp os :

User's view :

OS

single user OS

Multiuser OS

- All the progs in the memory
are submitted by one user
- All the progs in the memory
are submitted by many users

Based on preemption :

OS

Non-preemptive (NPr)

Voluntary release of CPU

- I/O need
- system call execution
- resource request

- Completion of process.

∴ Starvation

Poor responsiveness / Interactivity

Ex- Win 3.0

Preemptive (Pr)

Forceful deallocation of process.

Criteria for preemption : Time - Time shared OS

Priority

Shortest job first :

better responsiveness / Interactivity.

Ex- Win 95-10, UNIX, LINUX

Architectural requirements for Mpr OS Implementation :

① I/O (secondary storage) : DMA capability should be there.

Mode of transfer (I/O)

Program Controlled I/O

Interrupt driven I/O

Polling

✗ Mpr can implement directly

✓ Mpr

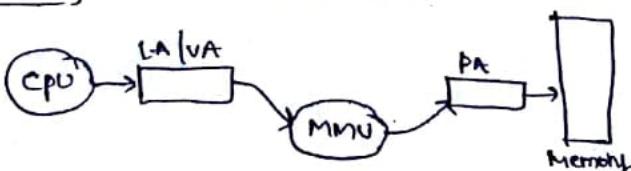
✗ processor load ↑

DMA

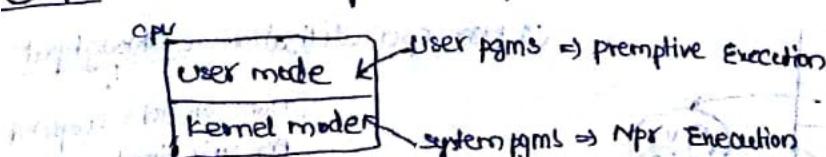
✓ Mpr

✗ processor load ↓

② Memory : Address translation need because it provides security



③ CPU : Dual mode operation reqd



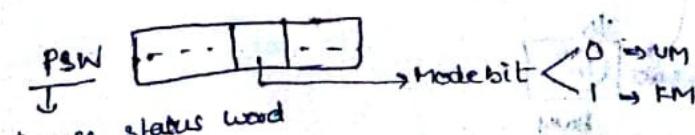
Kernel

→ privileged mode

→ System mode

→ supervisory mode

→ Monitor mode.



Mode shifting :

main()

```
int a,b,c;
a = 1; b = 2;
```

```
U C = f(a,b);
L printf("%d",c);
```

```
S fork();
```

*) User mode

Interrupt
mode

Not
ready

*) Interrupts

→ INTW (raised by devices)

→ SW (pgm driven)

At compiletime

At runtime

BSA

SVC

opcodes

PSW

modebit

1 UM

2 UM

functions

Userdefined

Library

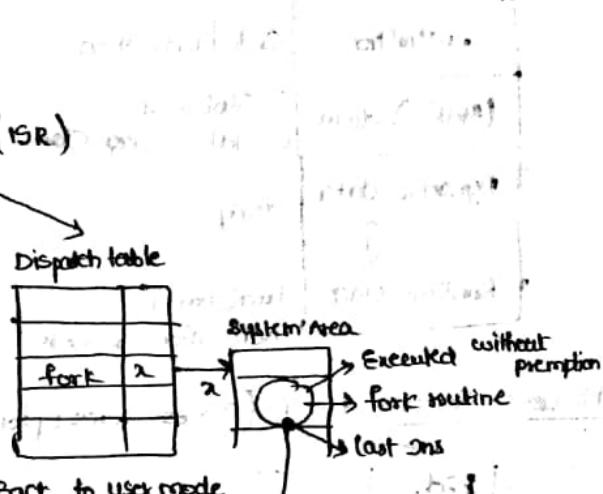
System call

f(a,b)

printf()

(defined in os)

fork()



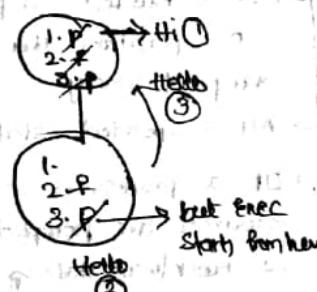
Fork system Call :

main()

1. pf("Hi")

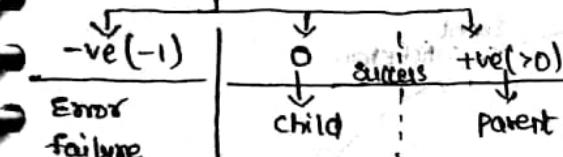
2. fork();

3. pf("Hello")



	Num of forks in series	Num of Child	Total Processes
1 fork	1	2	3
2 fork	3	4	7
3 fork	7	8	15
n fork	$2^n - 1$	2^n	$2^{n+1} - 1$

Return value of sys call



```
main()
{
    // parent
    ret = fork();
    if (ret == 0)
        // child
    else
        // parent
}
```



Child executes SP
Parent executes ELSE

→ Current state of values are copied
into child process.

Process Concepts :

(Passive Entity) (Active Entity)

Program vs process :

(•-line)

(pgm under execution)

Instructions Data

```
Static
→ fixed size
→ load time
```

```
Dynamic
→ var size
→ Run time
```

Using of resources like CPU, RAM, memory

Definitions of Process

- Program under Execution
- Instance of a program
- Active Entity
- Schedulable Unit
- Present in memory
- Unit of CPU utilization
- locus of control of OS
- animated spirit of pgm

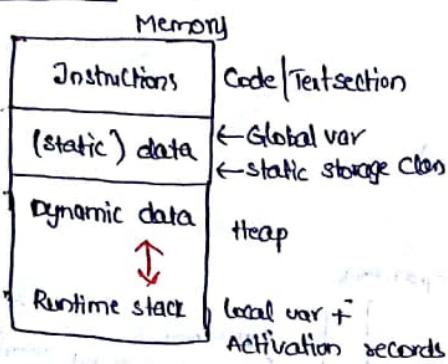
Developer's view:

Process can be viewed as ADT

<Def ; Rep ; oper's ; Attr>

Imp

Representation



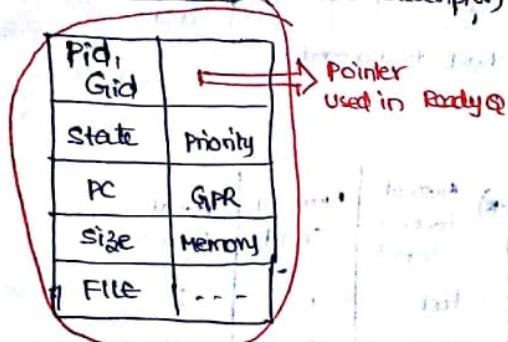
Operat's:

- * PCB is involved from creation to deletion
- create()
- schedule()
- Dispatch()
- Block()
- Suspend()
- exit()
- Delete()

Attributes:

- | | |
|------------------------|-------------|
| pid, parentid, Groupid | CPU Attr |
| PC, GPR, Type, State | |
| size(B), Memory limits | Memory Attr |
| List of open files | |
| List of open devices | |

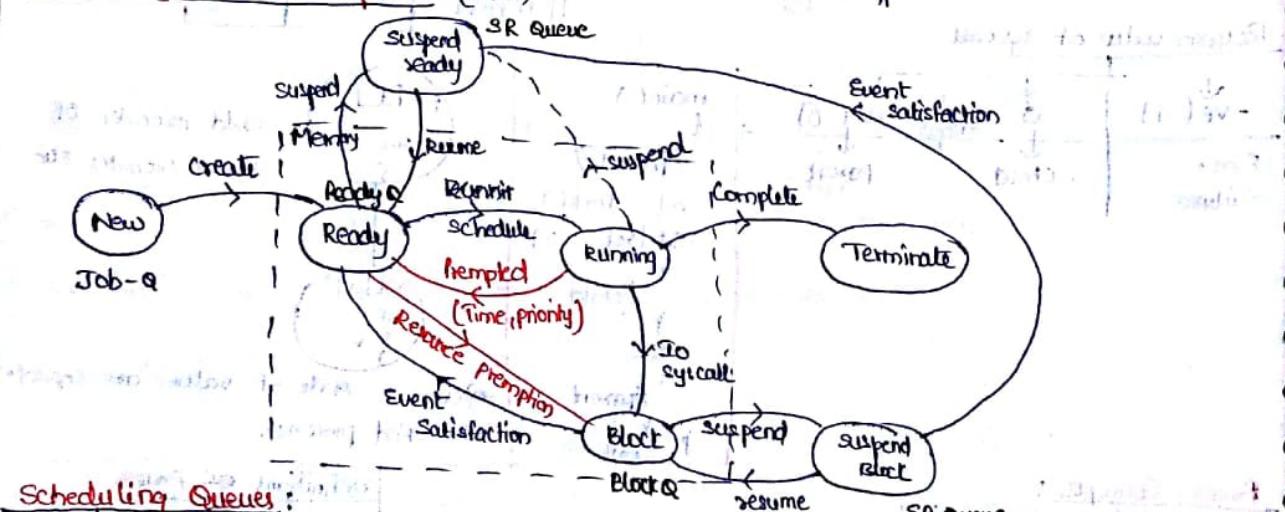
Process Control Block (Process descriptor)



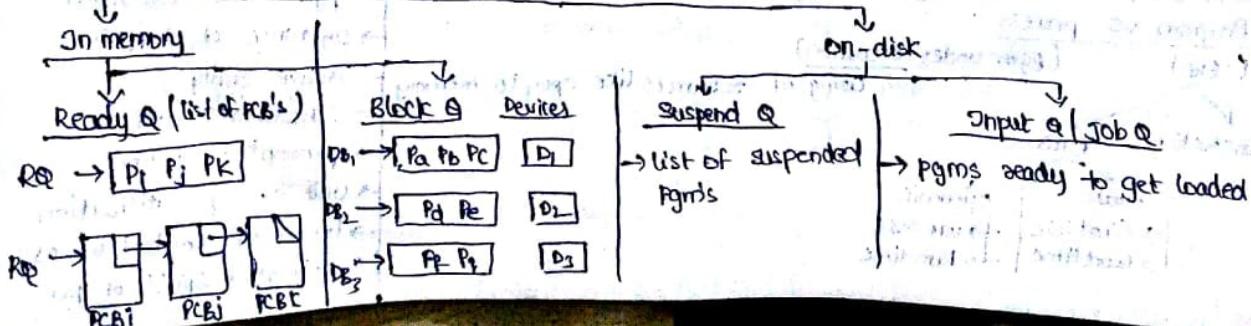
Context of process / Process Environment

- If ready not present \Rightarrow uniprogrammed OS
- Running $\xrightarrow{\text{ready}}$ ready \Rightarrow preempted as running
- Running $\xrightarrow{\text{x}} \text{ready}$ \Rightarrow Nonpreempted OS
- If a Blocked suspended process completes its I/O operation then the process would go to suspend ready.
- All suspended states are present in sec memory.
- If a process is in ready state and one of its resources are preempted then the process would go to block/wait state.

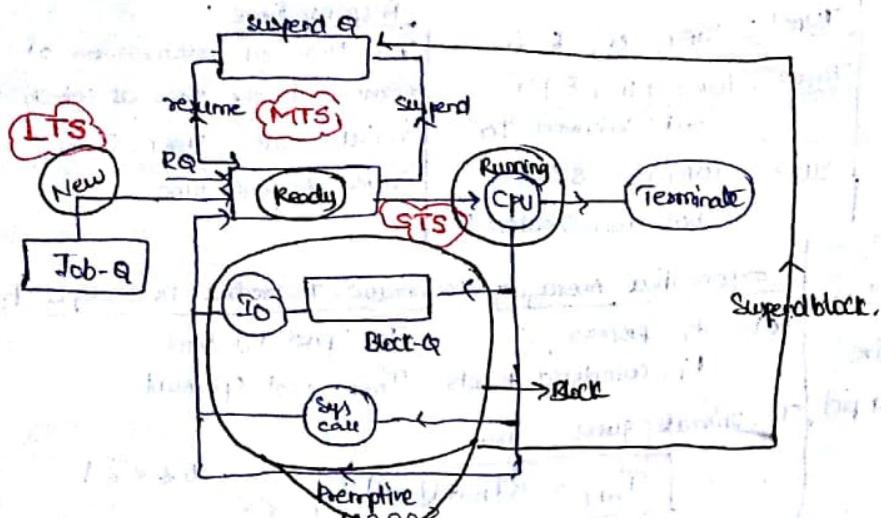
State diagram of a process (DFA)



Scheduling Queues:

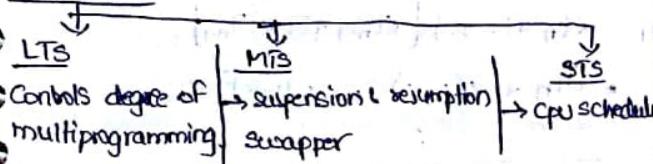


State Queuing diagram :



Schedulers & Dispatchers

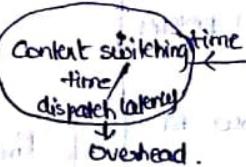
Scheduler



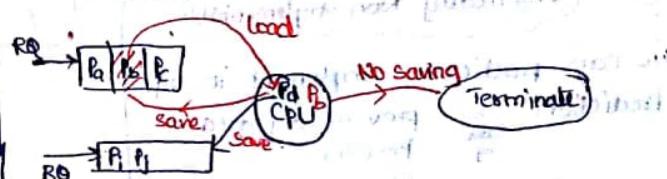
Dispatcher

→ carry out activity of Context switching

↓
saving the PCB of prompted process
and loading the PCB of next process to run on CPU.



Overhead.



* save is an option but loading is compulsion

CPU scheduling : STS

Function : select a ready process for running in CPU

Goals : Max CPU utilization (throughput)

Min Turn Around time

Min Waiting time → starvation
→ response time.

Process times

① Arrival time

② Waiting Time

③ Scheduling time

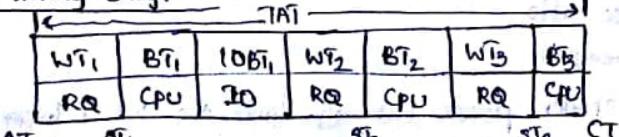
④ Burst time

⑤ IO Burst time

⑥ Completion time

⑦ Turn around time

Timing diagram :



$$TAT = CT - AT$$

$$WT = TAT - [BT + IOBT]$$

$$*) TAT(P_i) = C_i - A_i$$

$$\text{Avg TAT} = \frac{1}{n} \sum_{i=1}^n (C_i - A_i)$$

$$*) WT(P_i) = (C_i - A_i) - (BT_i + IOBT_i)$$

$$\text{Avg WT} = \frac{1}{n} \sum_{i=1}^n ((C_i - A_i) - (BT_i + IOBT_i))$$

$$*) \text{Schedule length} = \max(C_i) - \min(A_i)$$

*) Schedulable Combinations

Non preemptive - $n!$

Preemptive - ∞

$$*) \text{Throughput } (\mu) = \frac{n}{L} \text{ ie } n \rightarrow L, ? \rightarrow 1$$

CPU Scheduling Techniques :

① FCFS :

Criteria : AT

Mode of opern : Non preemptive.

Conflict resol : lower pid.

Type 1 : $IOBT = 0, S = 0$

Type 2 : $IOBT \neq 0, S \neq 0$
but concurrent IO

Type 3 : $IOBT \neq 0, S \neq 0$
but non-concurrent IO

Response time :

The time of submission of a request to the time at which the initial results, start coming is called Response time.

② SJF :

Criteria : BT

Optimal Algo.

Mode of opern : Non preemptive

Conflict resol : AT + lower pid.

Performance of SJF :

↓
favours shorter process.

Max Throughput ; starvation

Min TAT, WT (avg) to larger processes

Practical Limitation :

Before running we should know BT

Practically Non Implementable

Exponential Averaging Technique to predict next CPU BT:

Let P_i : process, T_{ij} : predicted burst
 t_i : completed bursts T_{n+1} : next cpu burst

T_1 : initial guess then.

$$T_{n+1} = \alpha t_n + (1-\alpha) T_n \quad 0 \leq \alpha \leq 1 \quad \text{①}$$

$$T_D = \alpha t_{n-1} + (1-\alpha) T_{n-1}$$

$$\text{①} \Rightarrow T_{n+1} = \alpha t_n + (1-\alpha) [\alpha t_{n-1} + (1-\alpha) T_{n-1}] \\ = \alpha t_n + \alpha(1-\alpha) t_{n-1} + (1-\alpha)^2 T_{n-1}$$

$$T_{n+1} = \alpha t_n + \alpha(1-\alpha) t_{n-1} + \alpha(1-\alpha)^2 t_{n-2} + \dots \quad : T_1$$

Exponential Averaging.

We can practically implement it by

Prediction done by pre history data of processes

History

P: lookb	Pad	101	(40)
		Size	BT

③ SRTF : (Preemptive SJF)

If preemption is done

SRTF > SJF (Powerful)

If preemption is not done

SRTF = SJF

Practically non Implementable

④ LRTF :

Criteria : BT

Mode of opern : preemptive

Conflict resol : lower pid

⑤ HRRN :

Criteria : Response ratio

Mode : Non preemptive

Favours not only shorter process but also limit the WT of longer process.

$$\text{Response ratio (RR)} = \frac{W+S}{S}$$

⑥ Priority based scheduling :

Criteria : priority (integer value)

static dynamic

Nonpr/pr

Mode : 10 100 1000 4

Mode : AT + TG

Mode : Preemptive

Performance of Round Robin :

Value of TQ

Small

- More Context switch d/t
- Improved responsiveness rather than doing useful work

very small

→ CPU is busy in Context switches

large

→ less Context switch d/t

→ less responsiveness

very large

→ similar to FCFS.

Points to remember :

Technique	Mechanism	Criteria	Mode of operation	Conflict resolution	
① FCFS	First Come First serve	AT	Npr	lower pid	
② SJF (optimal)	Shortest Job First	BT	Npr	AT + lower pid	
③ SRTF	shortest remaining time first	BT Non preempt	pr	lower pid	
④ LRTF	longest remaining time first	BT	pr	lower pid	
⑤ HRRN	Highest response ratio next	WTS / S	RR	Npr	lower pid
⑥ Priority	Priority based scheduling	(Priority) (high value)	Npr / pr	Priority + lower pid	
⑦ Round Robin	Time quantum	AT + TQ	pr	lower pid (if TQ is very low)	

Process management :

IPC ; synchronization ; Concurrency :

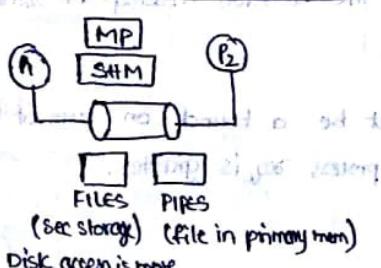
Need for synchronization : Inconsistency [wrong results]

Data loss [By speed, By heavy Context switch d/t's]

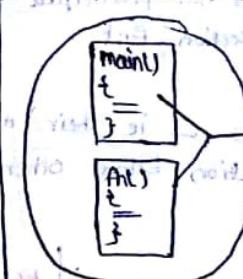
Deadlocks — process Co-operation

process competition

Inter process communication :



Intra process Communication :



- 1) Global var
- 2) parameter passing

Process Synchronization :

Competition
Cooperation

Process Competition :

Two or more processes are said to be in Competitive Synchronization if they compete for the accessibility of shared resource.

→ lack of sync among competing process leads to **Inconsistency or data loss**

Process Cooperation :

if they get affected by each other

→ lack of sync among cooperating process leads to **deadlocks**

* An Application in IPC Environment may Involve Either Completion/Co-operation/ Both type of synchronization.

Synchronization Mechanisms :

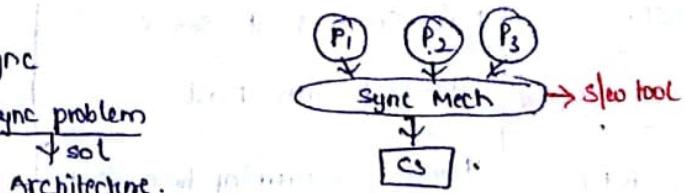
Necessary Conditions :

① Critical section : (It is the part of the pgms where shared resources are altered & manipulated)

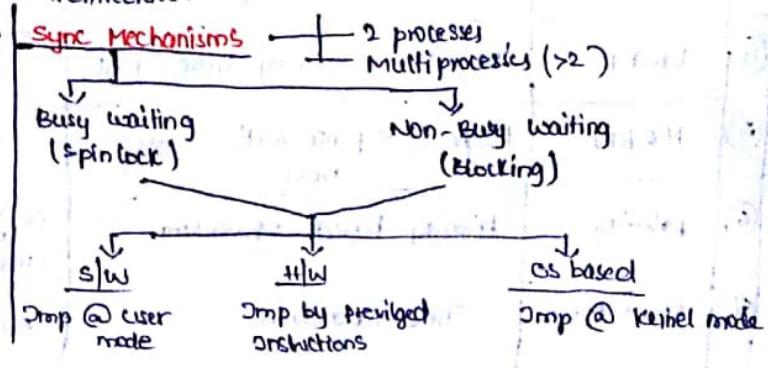
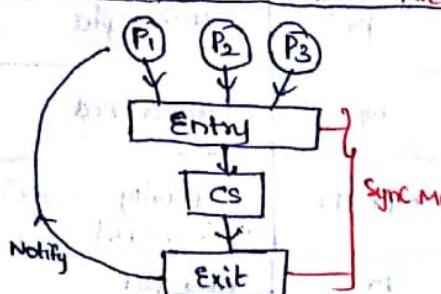
② Race Condition : The situation where multiple processes tries to access and manipulate the critical resources Concurrently and the outcome depends on the order in which they finish their update.

③ Premption : Root cause for lack of sync

* All 3 conditions are sufficient for sync problem



Synchronization Mechanism Architecture :



Requirements for sync Mech :

① Mutual Exclusion :

→ mandatory requirement

→ No two processes may be simultaneously present in cs.

② Progress :

→ No process running outside the cs ie (Ncs) should block the other Interested process from Entering cs.

→ In other words a process in Ncs should not participate in the decision making of interested Processes as to who should Enter critical section first.

③ Bounded Waiting :

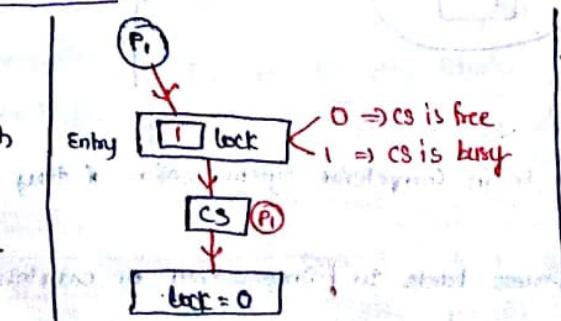
→ No process has to wait forever to access CS ie their must be a bound on num of times a process is allowed to Enter critical section before other process req is granted.

Lock variable sync Mech :

→ Busy waiting

→ SW solution

→ Multiprocess Mech



Result

ME : ✗

Progress : ✓

Bounded waiting : ✗

Implementation : (HLL)

```

int lock = 0;
{
    while(1)
    {
        a) Non-CS();
        b) while (lock != 0);
        c) lock = 1; JNZ
        d) <CS>
        exit e) lock = 0;
    }
}

```

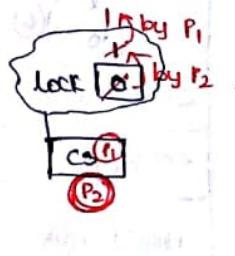
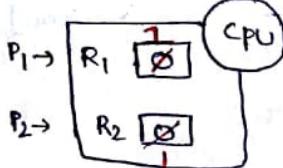
(LLL)

```

int lock = 0;
{
    while(1)
    {
        a) Non-CS();
        b) Load R1, lock
        c) CMP R1 #0
        d) JNZ stepb
        c) store lock #1
        f) <CS>
        g) store lock #0. Exit
    }
}

```

Mutual exclusion : (X)

RQ $P_1 | P_2 | P_3$ 

(low level lang)

t₁ : (P₁) : a; b; c; d; pre.
t₂ : (P₂) : a; b; c; d; e; f; pre.
t₃ : (P₁) : e; f

ME X

Progress : (✓)

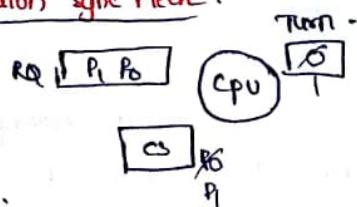
The process running in Non CS doesn't affect the interested process.

Bounded waiting :

A process after using CS again make lock=1 and Enter into CS which makes another process to starve

② Strict Alternation Sync Meth :

- Busy waiting
- slow solution
- 2 process sol



Result :
ME : ✓
Progress : ✗
Bounded waiting : ✓

Implementation :

```

int turn = rand(i,j);
void process (int i)
{
    int j = not i;
    while(1)
    {
        a) Non-CS();
        b) while (turn != i);
        c) <CS>
        d) turn=j;
    }
}

```

lowlevel

entry.

```

a) load R1,turn
b) load Rj, i ;
c) Comp R1,Rj
d) Jump to @
e) <CS>
f) load R1,turn
g) load Rj, j
h) store R1,Rj

```

turn | 0 |
P₀
i=0
j=1 ①
<CS> ③
turn=1; ④
turn=0; ⑥

Mutual Exclusion : At any time only one process is present in CS.

Progress : If turn got to P_i and it is not interested in entering to CS but P_j stops the process P_j to enter CS.

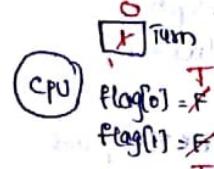
Bounded Waiting: After acquiring CS we are making turn = j , this stops the same process entering again and again in CS.

(3) peterson solution (ross of a cricket) (lock var + strict alternation)

- Busy waiting
- s/w solution
- 2 process Mch

RQ $P_0 P_1$

CS



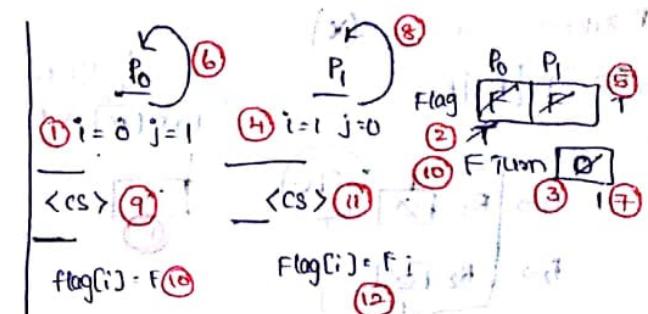
Result:

- ME: ✓
- Progress: ✓
- Bounded waiting: ✓

- Applicable to only 2 processes
- But leads to wastage of CPU time due to busy waiting.

Implementation:

```
#define N 2
#define TRUE 1
#define FALSE 0
int flag[N] = {FALSE};
int turn;
void process(int i)
{
    int j = Not i;
    while(1)
        if (i == turn)
            a) Non-CS();
        b) Flag[i] = TRUE;
        c) turn = i;
        d) while (flag[j] == TRUE || turn == i);
        e) <CS>
        f) flag[i] = FALSE
}
```



④ TSL (Test and set lock)

- Busy waiting
- H/w solution
- Multiprocess sol

→ Extension to lock var mech
↳ overcomes preemption

Syntax : $TSL(\text{target})$; returns the current value of lock (Pointed by target) &
 ↳ read ↳ write
 ↳ Atomically Executed without preemption.

Implementation :

Bool lock = FALSE

void process (int i)
{

 while(1)
 {

 a) Non-CS();

Entry b) while ($TSL(\&lock) == \text{TRUE}$);

 c) <CS>

Exit d) lock = FALSE;

Mutual exclusion :

t₁: (P₁) : a; b; pre $\xrightarrow{TSL \rightarrow F}$

t₂: (P₂) : a; b $\xrightarrow{TSL \rightarrow T}$

t₃: (P₁) : b; c; pre

t₄: (P₂) : b $\xrightarrow{TSL \rightarrow T}$

t₅: (P₁) : d;

t₆: (P₂) : b; c; d .

ME ✓

Result :

- ME : ✓
- Progress : ✓
- Bounded waiting : ✗

*) with some modifications we can make TSL guarantees bounded waiting

(6)

Bool TSL (Bool *target)

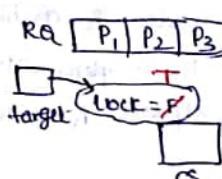
{

 Bool rv;

- rv = *target
- *target = TRUE
- return rv

Privileged instructions

ie Executed without preemption



Progress : The process running outside CS doesn't affect the unblocked process

Bounded waiting : The process that made lock = false after entering CS will again go into CS by making $TSL \rightarrow F$.

⑤ SWAP :

- Busy waiting
- H/w solution
- Multiprocess solution

→ Extension to lock var mech
↳ overcomes preemption

Result :

- ME: ✓
- Progress: ✓
- Bounded waiting: ✗

*) with some modifications in the logic (by introducing Round Robin fashion) we can make swap guarantees bounded waiting.

Implementation :

Bool lock = FALSE

void process (int i)
{

 Bool key;

 while(1)
 {

 a) Non-CS();

 b) ~~-----~~

Entry
 b) key = TRUE;
 c) do {
 swap (&lock, &key);
 } while (key == TRUE);

 d) <CS>

 e) lock = FALSE; **Exit**

Void swap (Bool *a, Bool *b)

{

 Bool temp;

 temp = *a

 *a = *b

 *b = ~~*temp~~

Privileged ins

Executed w/o preemption.

Mutual Exclusion :

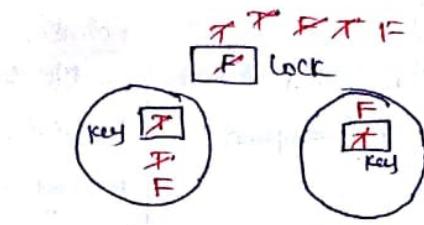
t₁: P₁ : a, b ; pre

t₂: P₂ : a, b, c(swap); pre.

t₃: P₁ : c

t₄: P₂ : c; d; e

t₅: P₁ : c; d; e



ME ✓

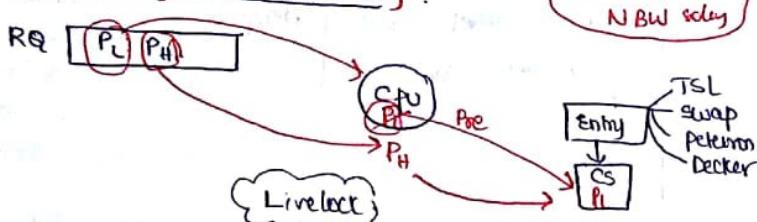
Progress : The other process running outside CS doesn't affect interested process

Bounded waiting : The process after accessing CS again enters into CS by swapping and making its Key value as False.

* Does TSL | swap guarantees Bounded waiting (without mentioning code) : Yes

Priority Inversion problem : (Arise only in Busy waiting Sync Mech)

Premptive priority based scheduling :



So we prefer NBW scheduling

Solution : ① priority inheritance : desirable

make P_L as high priority than P_H
P_L completes its execution
update P_L with its own priority

Deadlock	livelock
state : Blocked	state : Ready Running no waiting finite waiting - spinlock.

② Round Robin scheduling

Not desirable bcoz P_L gets equal chance as P_H.

(6) sleep() and wakeup() :

- Non Busy waiting
- OS based sol
- Multiprocess sol

Implementation : (Producer consumer problem)

void producer(void)

```

    {
        int itemp, in=0;
        while(1)
        {
            a) itemp = produceitem();
            b) if (Count == N)
                sleep();
            c) Buffer[in] = itemp
            d) in = in+1 mod N
            e) Count = Count + 1
            f) if (Count == 1)
                wakeup(consumer);
        }
    }
  
```

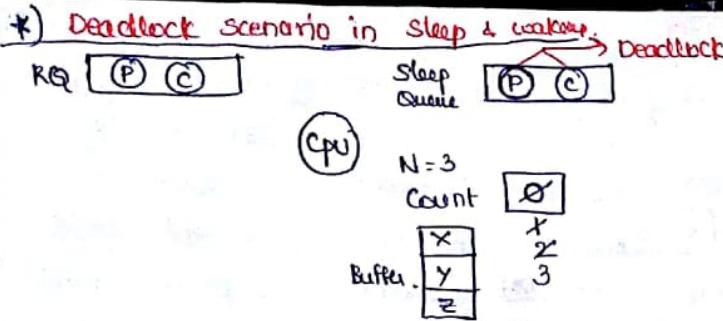
Proton Cooperation
deadlock.

Proton competition
Inconsistency
Data loss

void consumer(void)

```

    {
        int itemc, out=0;
        while(1)
        {
            a) if (Count == 0)
                load, cmp, jump
            b) itemc = Buffer[out]
            c) out = out + 1 mod N
            d) Count = Count - 1
            e) proton item(itemc);
            f) if (Count == N-1)
                wakeup(producer);
        }
    }
  
```



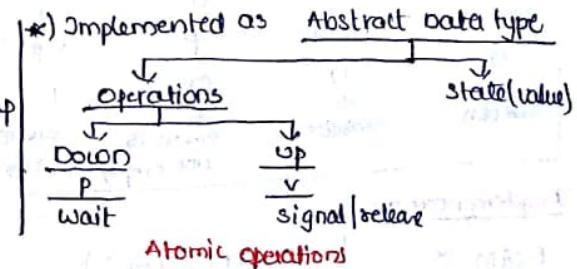
t₁ : C; L; c; J; pre
t₂ : P; (x, y, z); sleep()
t₃ : C; sleep()

(7)

③ Semaphores:

- Non busy waiting
- OS based sol
- Multiprocess mech

- General purpose utility
- Extension to sleep & wakeup
- Developed by Djikstra



Def of semaphores:

Semaphore is a variable of Semaphore datatype that takes only integral values.

Counting Semaphore:

Def : struct

{

int value;

QueueType L; → List of all PCB's of the processes that get blocked while performing down operation unsuccessfully.

Implementation:

CSEM;

s.value = 4;

! down(s)

< si >

Down(s)

{

a) s.value = s.value - 1

b) if (s.value < 0)

{

Put that process (PCB)
in S.L (queue) &
Block it (sleep implicitly)

else

return;

up (csem s)

{

a) s.value = s.value + 1

b) if (s.value <= 0)

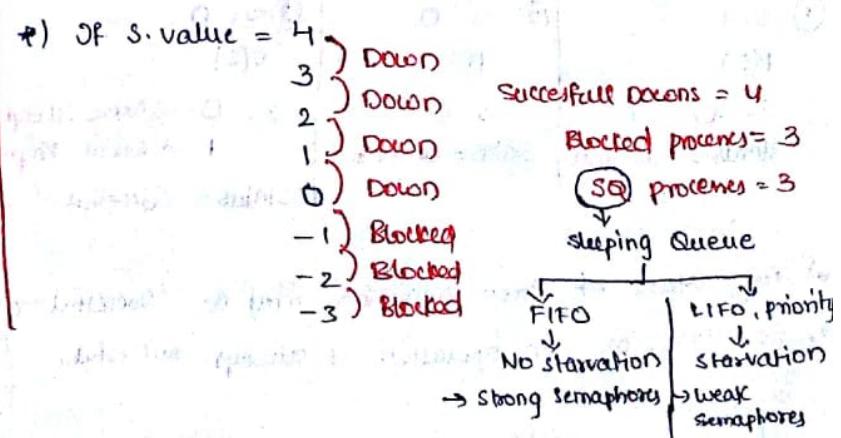
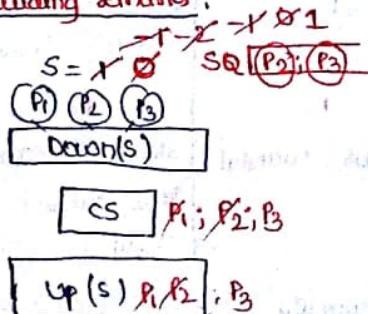
{

Select a process from S.L (queue)
wakeup();

else

return;

Concluding remarks:



*) $s = 8$; $10P; 1V; 18P; 6V; 3P; 4V; 5P; 1V$ $s = ? - 16$

*) $s = 13$; $1SP; 4V; 2P; 3V; 9P; 1V$ $s = -5$

$$x - 15 + 4 - 2 + 3 - 9 + 1 = -5$$

$$x - 18 = -5 \Rightarrow x = 13$$

Binary semaphore : (Mutex)

	0	0	0	1
Down	Down	Up	Up	Up
0	0	0	1	1
↓	↓	↓	↓	↓
success	unsucces	Queue is not Empty	Queue is Empty	Queue is Empty

Def :

struct

{
enum value (0,1);

QueueType L; \Rightarrow List of all pro's that
are blocked while
performing down
unsuccessfully.

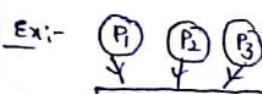
Implementation :

BSEM s
s.value = 1
;
Down(s)
 $\langle s_i \rangle$

Down (BSEM s)
{
~~if queue is not empty;~~
if (s.value == 0)
{
put this process (PCB)
in s.L (queue) &
Block it (sleep implicitly)
Else
if (s.value != 0)
s.value = 0
return;
};

up (BSEM s)
{

if (s.L(Q) is not Empty)
{
select a process from s.L (queue)
and wakeUp();
}
Else
s.value = 1;



$$s = X \emptyset \emptyset \emptyset \emptyset \emptyset \emptyset$$

SQ [P1 P2 P3]

[CS] P1 P2 P3

up(s) P1 P3

*) If $s=0 \Rightarrow$ we can't say number of blocked
processes
 \Rightarrow we may have blocked or unblocked
processes
 \Rightarrow we can conclude that a process
isn't present in CS.

*) $s = 1$; $10P; 2V; 3P; 1V; 18P; 3V$
SQ [9P] (7P) (10P) (9P) (27P) (2up)

$s=0$, SQ contains 24 processes.

Cases of Binary semaphore :

(1) $s = 1$
P(s)
 $s = 0$
status = successful

(2) $s = 0$
P(s)
 $s = 0$
status = unsuccessful

(3) $s = 0$
V(s)
 $s = 0 \Rightarrow$ Queue not empty
 $1 \Rightarrow$ Queue Empty
status = successful

(4) $s = 1$
V(s)
 $s = 1$
status = successful

(5) $s = 0$ (Initial)
V(s) (First open)
 $s = 1$
status = successful
bcz queue is definitely
empty

*) The status of down operation may be successful or unsuccessful.

*) The status of up operation is always successful.

Classical IPC problems :

Producer Consumer Implementation using semaphore:

```
#define N 100
CSEM Empty = N; < Num of Empty slots in buffer>
CSEM Full = 0; < Num of full slots in buffer>
BSEM Mutex = 1; < Used by P & C to access buffer as CS>
```

```
void producer(void)
```

```
{  
    int itemp, in = 0;  
    while(1)  
    {  
        a) Non-CS();  
        b) itemp = produceItem();  
        c) down(empty);  
        d) down(mutex);  
        e) Buffer[in] = itemp;  
        f) in = (in+1) mod N  
        g) up(mutex);  
        h) up(full);  
    }  
}
```

```
void consumer(void)
```

```
{  
    int itemc, out = 0;  
    while(1)  
    {
```

a) Non-CS();

b) down(Full);

c) down(Mutex);

d) itemc = Buffer[out];

e) out = (out+1) mod N;

f) up(mutex);

g) up(empty);

h) process-item(itemc);

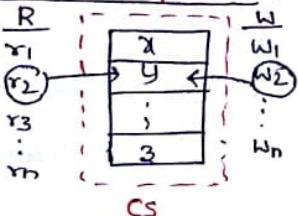
Entry

Exit

Co-operation

Co-operation

Readers writers problem :

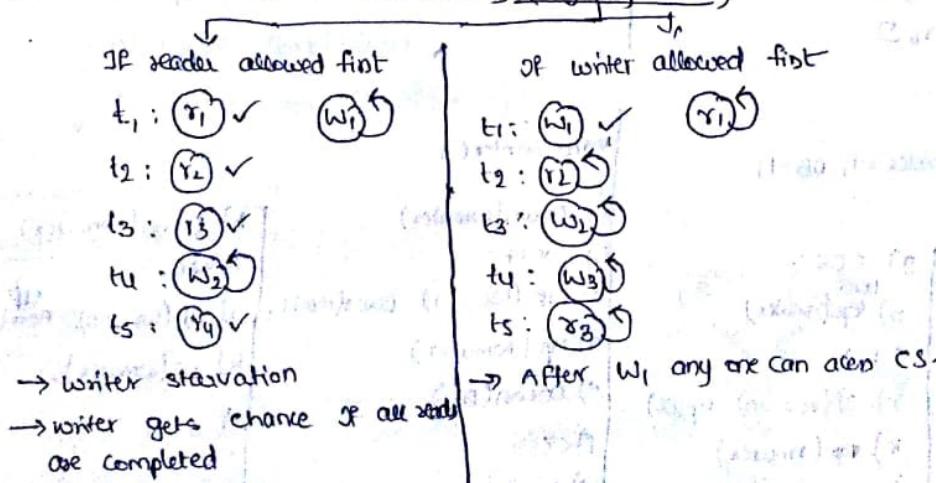


① First Reader Writer:

Prioritize reader if reader already present in CS.

Case 1 : R (or) W : Trivial (Allowed)

Case 2 : r and w arrived simultaneously (Anybody allowed)



Implementation of First reader solution using semaphores :

int rc = 0; (Reader count)

BSEM Mutex=1; < used by R_s to access rc as CS>

BSEM DB=1; < used by R_s and W_s to access DB as CS>

void writer()

{

while(1)

{

a) **Down(DB)** Entry

b) < write to DB > CS

c) **Up(DB)** Exit

}

void reader()

{

while(1)

{

a) **Down(Mutex)** Entry

b) $rc++$;

c) $if(rc == 1)$ Down(DB)

d) **Up(Mutex)**; Exit

e) < Read the DB > CS

f) **Down(Mutex)** Entry

g) $rc--$;

h) $if(rc == 0)$ Up(DB);

i) **Up(Mutex)**; Exit

* 1st reader is the leader of all other readers

1st reader → Access DB : All other R's Access DB

→ Blocks : All R's are blocked.

First writer reader problem / second reader writer problem :

Prioritize writer

case 1 : R_s / W_s : Trivial (allowed)

case 2 : R_s and W_s arrived simultaneously (writer allowed)

Special case :

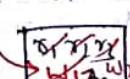
$t_1 \rightarrow r_1$	$t_6 \rightarrow r_5 \downarrow$
$t_2 \rightarrow r_2$	$t_7 \rightarrow r_1 r_2 r_3 \times$
$t_3 \rightarrow r_3$	$t_8 \rightarrow w_1 (DB)$ priority @ writer
$t_4 \rightarrow w_1 \downarrow$	$t_9 \rightarrow w_2 \downarrow$
$t_5 \rightarrow r_4 \downarrow$	$t_{10} \rightarrow r_6 \downarrow$

$t_1 \rightarrow w_1 \times$

$t_{12} \rightarrow w_2 \checkmark$

prioritize writer

$w_1 \downarrow w_2 \downarrow r_5 \downarrow$



Solution :

int rc=0, wc=0;

BSEM read1, rmutex = 1, wmutex = 1, DB=1;

void reader()

{

a) **Down(read)**

b) **Down(rmutex)**

c) $rc++$

d) $if(rc == 1)$ Down(DB);

e) **Up(rmutex)**;

g) < CS >
h) Down(wmutex)
i) $rc--$
j) $if(rc == 0)$ Up(DB);
k) Up(rmutex)
l)

Void writer()

{

a) **Down(wmutex)**

b) $wc++$

c) $if(wc == 1)$ Down(DB);

d) **Up(wmutex)**

e) **Down(DB)**

f) < CS >

g) **Up(DB)**

h) **Down(wmutex)**;

i) $wc--$

j) $if(wc == 0)$ Up(DB);

k) **Up(wmutex)**;

l)

m)

n)

o)

p)

q)

r)

s)

t)

u)

v)

w)

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Dining philosophers problem :



$N \geq 2$

Max. Concurrency = 3.

Non semaphore based soln:

① $(N-1), p \Rightarrow L-R$

$1, p \Rightarrow R-L$

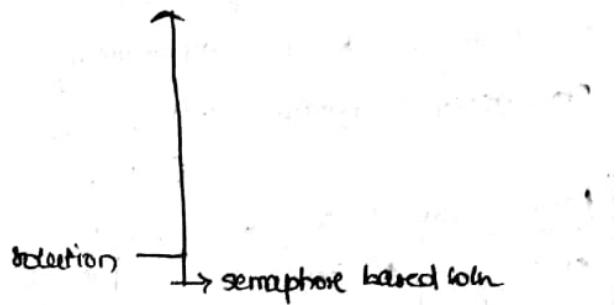
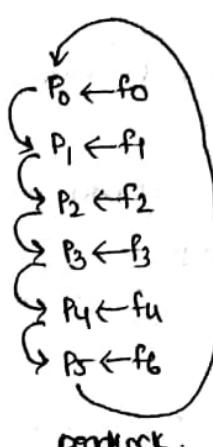
② odd $p \Rightarrow L-R$

even $p \Rightarrow R-L$

③ Providing one more Extra fork.

Implementation of dining philosophers problem :

```
#define N 6
void philosopher (int i)
{
    while(1)
    {
        a) Think(i);
        b) take_fork(i);
        c) take_fork((i+1)%N);
        d) eat(i);
        e) put_fork(i);
        f) put_fork((i+1)%N);
    }
}
```



Semaphore based solution:

```
#define N 6; BSEM S[N] - {1};
void philosopher (int i)
{
    while (1)
    {
        a) Think(i);
        b) Down (take_fork (S[i]));
        c) Down (take_fork (S[i+1])mod N);
        d) eat(i);
        e) Up (put_fork (S[i]));
        f) Up (put_fork (S[i+1])Mod n);
    }
}
```

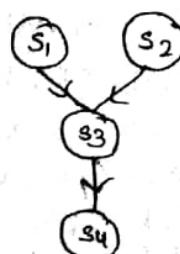
Concurrent programming :

Concurrency mechanisms :

$\rightarrow f$

$S_1 : a = b + c$
 $S_2 : d = e * f$
 $S_3 : k = a + d$
 $S_4 : l = k * m$

Precedence graph



Concurrency types:

Real | physical

(Multi CPU | Multi Core)

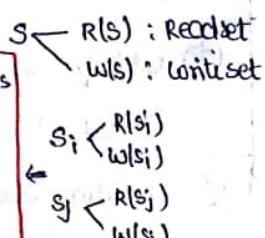
Interleaved | pseudo

(Uniprocessor system by Context switching)

Concurrency conditions:

Bernsteins concurrency conditions

1. $R(s_i) \cap W(s_j) = \emptyset$
2. $R(s_j) \cap W(s_i) = \emptyset$
3. $W(s_i) \cap W(s_j) = \emptyset$
4. $R(s_i) \cap R(s_j) = \text{may/may not} \neq \emptyset$



Ex: $s_1 : a + = ++b + ++c$

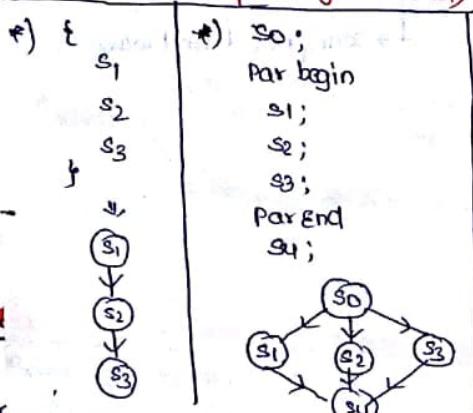
$R(s) = a, b, c$

$W(s) = a, b, c$

Concurrency mechanisms: ① (parbegin - parent) / (cobegin-coend)

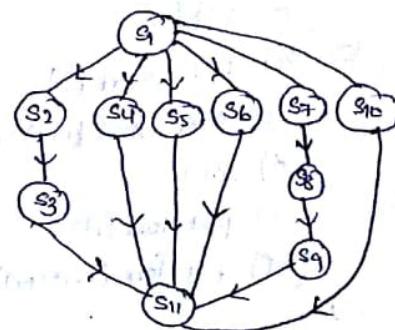
② Fork and join

(Parbegin-parent | co-begin-coend):

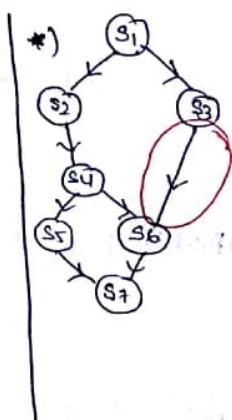
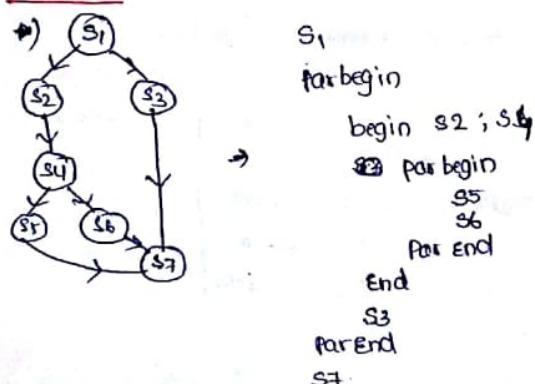


(Model 1)

* s_1
Par begin
begin $s_2; s_3$; End
 s_4
Par end
 s_{11} ;



Model 2:



⇒ Non-implementable
But implementable using
semaphores.

Parbegin-parent with Semaphore:

Bsem a,b,c,d,e,f,g = {0}; Initially

Par begin

begin $s_1; v(a); v(b)$; End

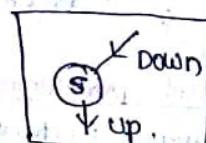
begin $p(a); s_2; s_4; v(c); v(d)$; End

begin $p(b); s_3; v(e)$; End

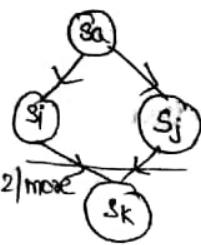
begin $p(c); s_5; v(f)$; End

begin $p(d); p(e); s_6; v(g)$; End

begin $p(f); p(g); s_7$; End



Fork and Join:



Syntax of fork:

S_a, Count = 2;

Fork L_i; L_j ;

S_i ;

;

goto L_i ;

L_i : S_j ;

L_i : join(count) ;

S_k ;

Syntax of join : join(count);

join(int count)

{

Count = Count - 1;

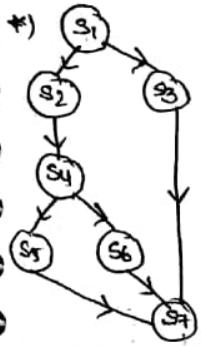
if (count != 0)

exit

else

return;

}



S_a, Count = 2;

Fork L_i ;

S_i ;

;

goto L_i ;

L_i : S_j ;

L_i : join(count) ;

S_k ;

S_l ;

Fork L₂ ;

S₅ ;

goto L₃ ;

L₁ : S₃ goto L₄ ;

L₂ : S₆ goto L₃ ;

L₃ : join(a) ;

S₅ ;

goto L₄ ;

L₁ : fork L₃ ;

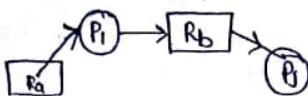
S₃ ;

Characterization:

Necessary Conditions:

a) Mutual exclusion: CS (shared resource)

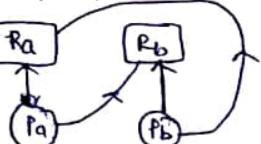
b) Hold & wait:



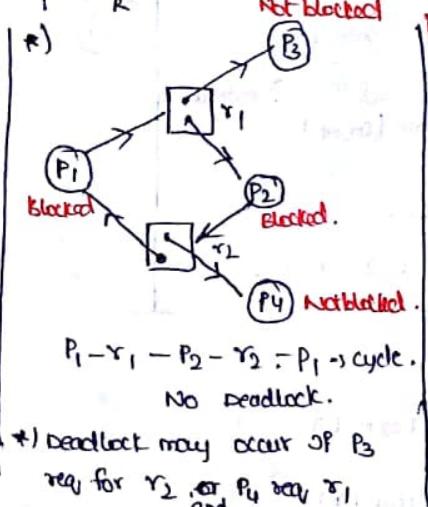
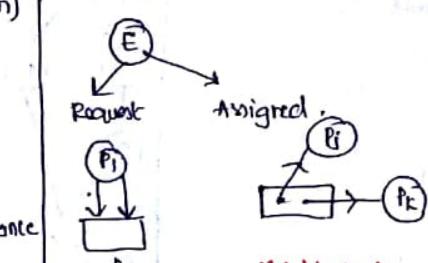
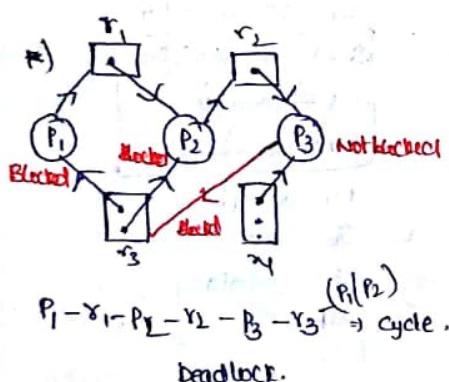
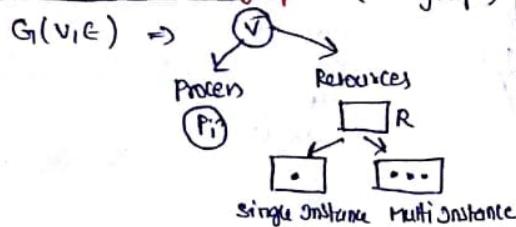
→ Every hold & wait doesn't imply deadlock.

c) No preemption: No preemption of resources may cause deadlock

d) Circular wait:



Resource Allocation graph: (Multigraph)



* Every deadlock contains cycle but every cycle doesn't lead to deadlock

Strategies

After → Deadlock happened

Deadlock detection & Recovery
(Doctors' Algo)

Deadlock Ignorance
(Ostrich Algo)

Before Deadlock happened

Deadlock prevention

Deadlock Avoidance
(Banker's Algo)

Deadlock Ignorance:

Ostrich Algo

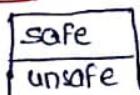
↓
Restart the Computer.

Deadlock Avoidance: (Banker's Algo)

Safety Algo

Resource seq, Algo

System State:

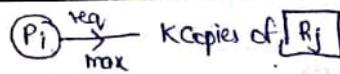


Datastructures that govern state of a system

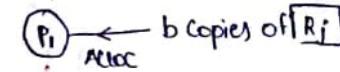
(1) n: num of processes

(ii)

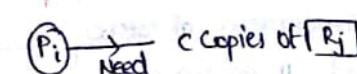
$$\textcircled{3} \quad \text{Max}[1..n, 1..m]_{n \times m} \Rightarrow \text{Max}[i,j] = k \quad \text{ie}$$



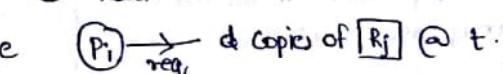
$$\textcircled{4} \quad \text{Alloc}[1..n, 1..m]_{n \times m} \Rightarrow \text{Alloc}[i,j] = b \quad \text{ie}$$



$$\textcircled{5} \quad \text{Need}[1..n, 1..m]_{n \times m} \Rightarrow \text{Need}[i,j] = c \quad \text{ie}$$



$$\textcircled{6} \quad \text{Request}[1..n, 1..m]_{n \times m} \Rightarrow \text{Req}[i,j] = d @ t \quad \text{ie}$$



$$\textcircled{7} \quad \text{Total}[1..m] \Rightarrow \text{Total}[j] = 'z' \quad \text{ie} \quad \text{There are 'z' copies of } R_j$$

$$\textcircled{8} \quad \text{Avail}[1..m] \Rightarrow \text{Avail}[j] = 'y' \quad \text{ie} \quad \text{There are 'y' copies of } R_j \text{ available @ } t$$

Safety Algo: (single instance)

	Max R	Alloc R	Need R	Avail R
P ₁	5	3	2	3
P ₂	10	5	5	8
P ₃	15	7	8	4
P ₄	8	4	4	18
P ₅	6	3	3	21
	22		25	TOTAL
				Safe

order : P₁ - P₂ - P₃ - P₄ - P₅

Multiple Instance:

	Max ABC	Alloc ABC	Need ABC	Avail ABC	Total $\rightarrow 1057$
P ₀	753	- 010	- 743	- 332	
P ₁	322	- 200	- 122	- 532	
P ₂	902	- 302	- 600	- 745	
P ₃	222	- 211	- 011	- 755	
P ₄	433	- 002	- 431	- 1057	1057
					safe
					725

order : P₁; P₃; P₄; P₀; P₂

Consider this Ex.

Resource request Algo:

Algo Resource-req (P_i, req_i, Alloc_i, Need_i, Avail)
{ }

a) Req_i \leq Need_i

b) Req_i \leq Avail_i

c) [Assume to have satisfied Req_i]

(i) Avail_i = Avail - Req_i

(ii) Alloc_i = Alloc_i + Req_i

(iii) Need_i = Need_i - Req_i

d) Run safety algo

e) If (system == safe)

Grant resources

f) Else

Deny the request

Ex:- t₁: (P₁) \rightarrow <102> req₁

	Max ABC	Alloc ABC	Need ABC	Avail ABC
P ₀	753	- 010	- 743	- 332

P ₁	322	- 200	- 122	<230>
----------------	-----	-------	-------	-------

P ₂	902	- 302	- 600	
----------------	-----	-------	-------	--

P ₃	222	- 211	- 011	
----------------	-----	-------	-------	--

P ₄	433	- 002	- 431	
----------------	-----	-------	-------	--

Run safety algo

<532>

<743>

<745>, <755>

<1057>

order : P₁; P₃; P₄; P₀; P₂

safe \rightarrow req₁ granted.

$\therefore \text{Avail} < 230 >$

t₂: (P₄) \rightarrow <330> req₂

Rejected because
Req₂ > Avail

t₃: (P₀) \rightarrow <020> req₃

	Max ABC	Alloc ABC	Need ABC	Avail ABC
P ₀	753	- 010	- 743	- 230

P ₁	322	- 302	- 020	<210>
----------------	-----	-------	-------	-------

P ₂	902	- 302	- 600	
----------------	-----	-------	-------	--

P ₃	222	- 211	- 011	
----------------	-----	-------	-------	--

P ₄	433	- 002	- 431	
----------------	-----	-------	-------	--

order: x {unsafe} \rightarrow req denied.

③ Deadlock detection & Recovery

Detection Algorithm :

When to Apply?

→ Throughput drastically decreases

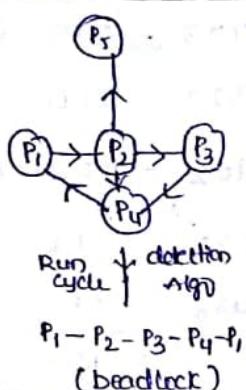
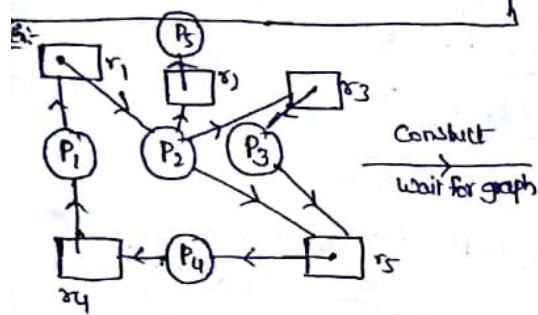
⇒ Majority processes in the main memory are blocked.

*) Banker's Algo : system safe / unsafe.
Detection Algo : safe / deadlock.

Detection when resources are single instance :

1. Construct wait for graph
2. Run cycle detection Algo
3. if cycle is present then deadlock
Else
No deadlock.

*) In single instance resource cycle is necessary and sufficient to say a process is in deadlock.



*) In multi instance resource cycle is only necessary condition for happening of deadlock.

Detection when resources are multi instance

t0	Alloc			Avail	$P_0, P_2 \rightarrow$ not blocked $P_1, P_3, P_4 \rightarrow$ Blocked majority Run detection Algo
	A	B	C		
P_0	010	-000	-000	111	
P_1	200	-202	010		
P_2	303	-000	313		
P_3	211	-100	513		
P_4	002	-002	726		
				726	

AF to ; $P_0, P_2, P_1, P_3, P_4 \rightarrow$ safe

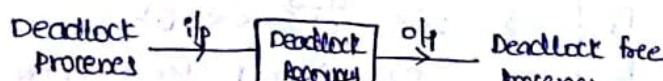
At t_1 : $P_2 \xrightarrow{\text{req}} \langle 001 \rangle$

t1	Alloc			Avail	$P_0 \rightarrow$ Deadlock
	A	B	C		
P_0	010	-000	-000	111	
P_1	200	-202	010		
P_2	303	-001			
P_3	211	-100			
P_4	002	-002			

At t_1 : $P_0 \rightarrow$ Deadlock

Blocked processes : P_1, P_2, P_3, P_4

Deadlock recovery :



Deadlock Recovery :

(Both suffer from starvation)

Process Termination

KILL ALL

→ No need to apply detection algo again

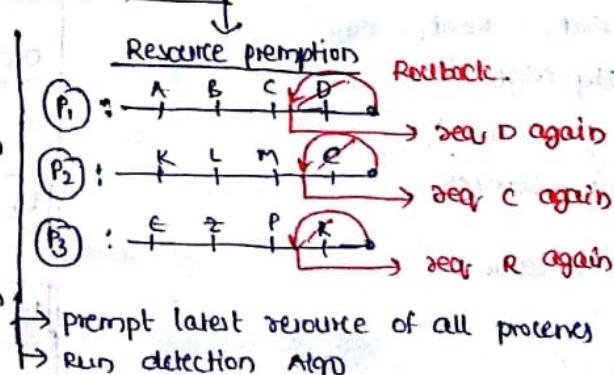
KILL ONE AT A TIME

Need to apply detection algo repeatedly.

Restart all processes

* All killed processes need to restart from the beginning

*) Process Termination and Resource preemption suffer from starvation.



Deadlock prevention

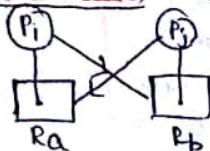
Dissatisfy one/more necessary conditions of the deadlock

→ Mutual exclusion

1) Mutual Exclusion : (X)

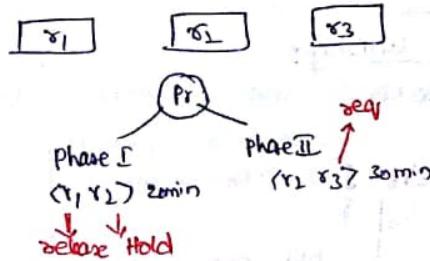
Mutual Exclusion is non-dissatisfiable due to the fact that system contains atleast one shared resource.

2) (Hold & wait) : Hold or wait



Protocol 1: process must request and be allocated to all the resources prior to its commencement

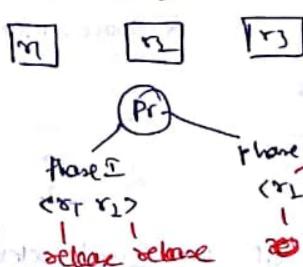
∴ under utilization of resources
Starvation.



Holding or waiting happened

Protocol 2: Release all the resources before making a fresh or new request

∴ starvation may happen



only waiting happens

3) !(No preemption) → preemption of resources.

Forceful
→ selfish spirit
→ process running on CPU forces other to preempt the resources

selfless
→ self less spirit

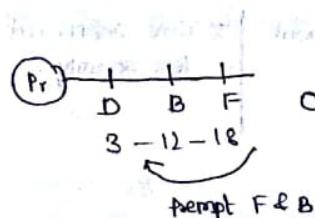
→ Process running on CPU preempts all its resources and goes to block state.

4) Circular wait :

Circular wait is dissatisfied by (i) Number all resources uniquely

(ii) Never allow a process to req a lower num resource than the last one req & allocated.

Ex:- Res	Reqd
A	9
B	12
C	8
D	3
E	25
F	18
G	28



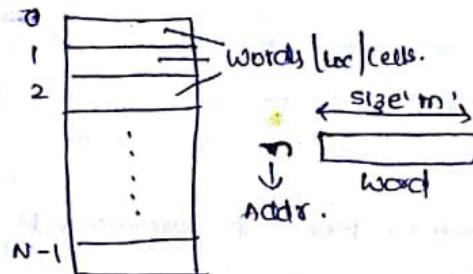
∴ suffer from starvation

↑ Demand priority

→ may/may not Available

Memory Management:

Abstract view of memory: (1D Array of words)



$N \rightarrow$ num of words
 $n \rightarrow$ Address.
 $m \rightarrow$ word size
 (bits / bytes)

$$N = 2^n \text{ words}$$

$$n = \log_2 N \text{ bits.}$$

$$N \propto n \propto m$$

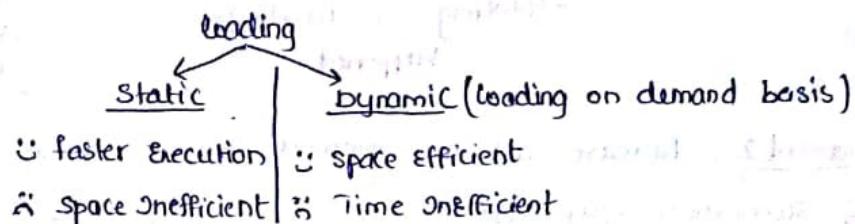
Loading vs Linking:

Prog size = 60 KB.

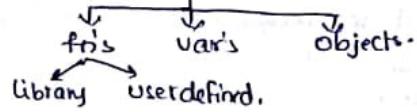
Loading:

```

main() 5KB
{
  :
  if (cond)
    BSA -> f1();
  :
  f() 10KB
  :
  BSA -> g1()
}
  
```

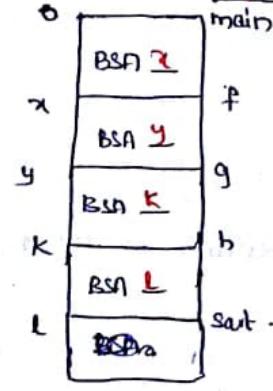


Linking: It is resolution of unresolved references



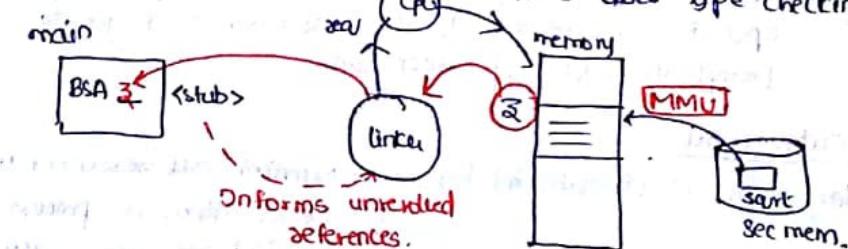
Resolution:

Static linking:



Time efficient
 More secured.

Dynamic linking:



Space efficient
 Reusability
 flexibility

Time inefficient
 less security.

Scope

- * Header files contains prototype of a fn:
 Prototype → set type
 Prototype → Name
 Prototype → Args, profile.
- * Definition of fn is present in library with (.lib) Extension
- * Declaration of fns at compile time does type checking

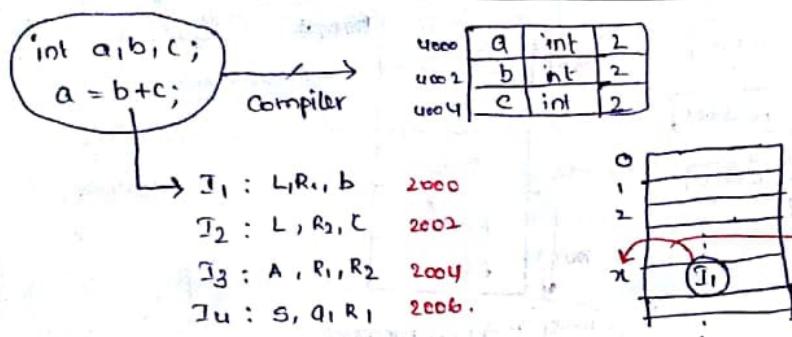
Address binding:

Association of program instructions and data units to memory locations (having address)

Deciding where to load - Address binding
 loading of ins & data - loader } difference.

Binding

→ static binding : Compile time, load time
 → dynamic binding : Runtime.



Binding time

Compile time

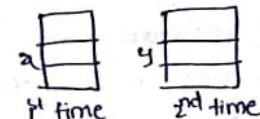
- Deciding the loc of ins / data where to load
- Allocation is not happened at compile time
- static binding
Ex:- DOS
- ∴ Inflexibility
More burden to compiler

Load time

- If Compiler doesn't do Addr binding then Loader will do Addr binding
- Compiler generates logical addresses like
I₁: 0
I₂: 2
I₃: 4
- Loader at load time in memory with base addr 2000 loads
I₁: 2000+0 : 2000
I₂: 2000+2 : 2002
I₃: 2000+4 : 2004
- static binding

dynamic binding

- ∴ More flexibility due to dynamic relocation



Runtime

Compile time binding :

of Compiler associates pgm instructions and data units to absolute address of memory

load time binding :

Compiler generates only logical offsets which are relocated to physical address by loader during load time

Runtime binding :

during Runtime binding pgms during Execution can get relocated in different areas of memory.

Functions & Goals of memory management :

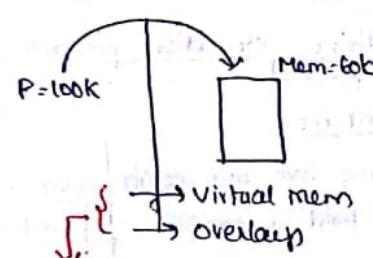
Functions : (F PAD)

→ effective utilization of memory space.

(Minimizing fragmentation levels)

→ protection
→ Free Spacing mgmt
→ De-allocation.

→ Managing execution of larger pgms in smaller mem area.



Memory management techniques :

Contiguous

→ centralized Allocation

- Ex:- partitions (2)
- overlays (1)
- Buddy systems

Non Contiguous

→ decentralized / distributed Allocation

- Ex- Paging
- Segmentation
- segmented paging
- virtual memory

Overlays :

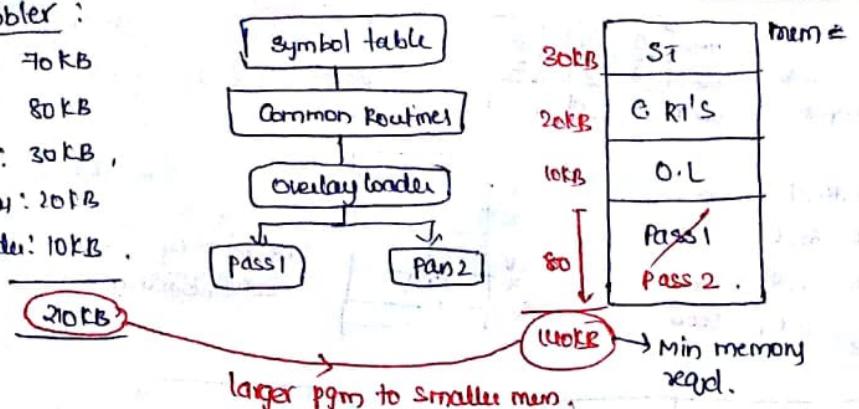
- Contiguous mem mgmt technique.

Increases multiprogramming

Throughput ↑

2 pass Assembler :

Pass 1 : 70 KB
 Pass 2 : 80 KB
 Sym table : 30 KB,
 Common Routine : 20 KB
 Overlay loader : 10 KB.



Note :

* In overlay trees the min memory required is the maximum path length.

② partitions :

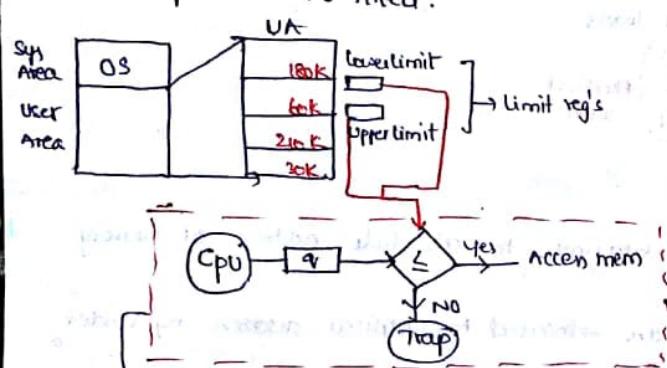
Fixed partitions

(multiprogramming with fixed tasks)

Rule : 1 partition = 1 pgm

→ Size is variable

→ Num of partitions are fixed.



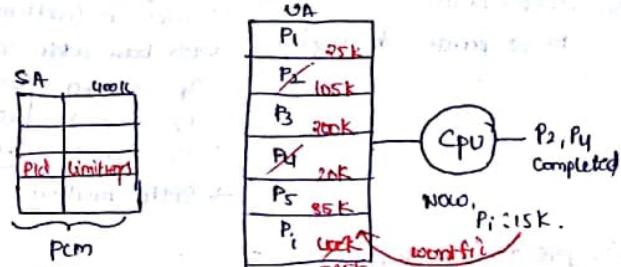
Provide security of non interfering of other pgms

→ static scheme w.r.t partitions.

variable partition

(multiprogramming with variable tasks)

PF : P₁ P₂ P₃ P₄ P₅ P₆
 req : 25K ; 10SK ; 200K ; 20K ; 85K ; 310K.



→ It consists of info like partition id, limit reg, Attributes...etc.

→ If two contiguous free holes are available then automatically merge to one hole → Coalescing

→ Dynamic scheme w.r.t partitions.

Partition Allocation policies :

First fit

→ First free big enough to hold a process.

Best fit

→ smallest free big enough to hold a process

of all

Best fit
 ⇒ waiting is present

of Available

Rest Avail fit
 ⇒ no waiting
 • default partition Alloc policy

Next fit

→ It works like first fit except that the search for free big enough partition to hold a program commences from the partition where the last alloc was made.

⇒ works faster than first fit
 Num of search open is less

Worst fit

→ largest free big enough to hold a program.

Performance issues of fixed partition :

- 1) Internal fragmentation : ✓
- 2) External fragmentation : ✗
- 3) Degree of multiprogramming : limited to num of partitions
- 4) Max process size runnable : limited to largest partition
- 5) Alloc policy : Best fit

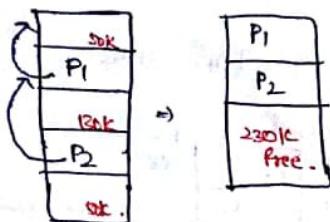
Performance issue of variable partition :

- 1) Internal fragmentation : ✗
- 2) External fragmentation : ✓ → (it is considered when all the avail free holes are greater than the process size)
- 3) Degree of multiprogramming : flexible
- 4) Max process size runnable : flexible
- 5) Alloc policy : Worst fit

So, only problem in variable partition

↓
External fragmentation
↓ solution

Compaction:



↓
Non-contiguous Allocation

- Paging
- Segmentation
- Segmented Paging
- Virtual Memory

→ Compaction is supported by runtime binding

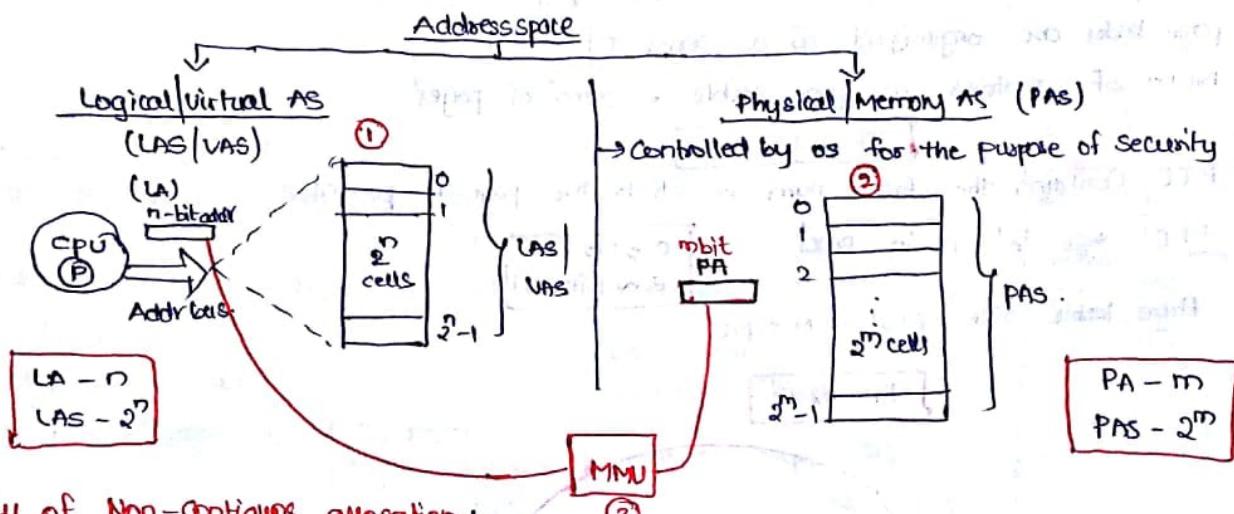
∴ Time consumption process

block of

Non-contiguous memory allocation:

Address space: (AS)

A Group of words or locations or memory cells associated with address is AS



Study of Non-contiguous allocation:

- ① organization of LAS
- ② organization of PAS
- ③ organization of MMU with translation logic

PAGING:

$$\begin{aligned} LAS &= 8 \text{ KB} & PAS &= 4 \text{ KB} \\ LA &= 13 \text{ bits} & PA &= 12 \text{ bits} \end{aligned}$$

$$\text{Pagesize} = 1 \text{ KB}$$

① organization of LAS:

- The logical AS is divided into equal size units known as pages
- Generally page size is the power of 2
- Num of pages (N) = $\frac{LAS}{PS}$
- Each page is assigned with a unique num or id known as page number, given in bits

$$\text{Page No (P)} = \log_2 N = \log_2 \frac{LAS}{PS}$$

$$N = 2^P = \frac{LAS}{PS}$$

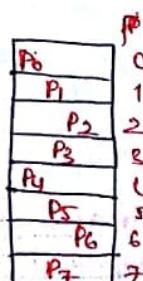
- Page offset denoted by 'd', It is used to select a byte/word within a page.

$$d = \log_2 PS$$

$$PS = 2^d$$

- Logical address format

$$LA [P | d]$$



Bits to remember:

$$\begin{array}{l} \text{(LS|PAS)} \rightarrow \text{Bytes} \\ \text{(LA|PA)} \rightarrow \text{bits.} \end{array}$$

$$\begin{array}{l} \text{(PS)} \rightarrow \text{Bytes} \quad \text{(PTE)} \rightarrow \text{Bytes} \\ \text{(P|q)} \rightarrow \text{bits.} \end{array}$$

Page frame blocks

② organization of PAS:

- PAS is divided into equal size units known as frames with the convention that

$$\text{Frame size} = \text{pagesize}$$

- Each frame holds 1 page of address space.

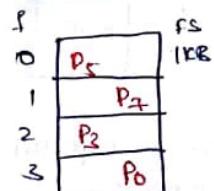
$$\text{Number of frames } (M) = \frac{\text{PAS}}{\text{BS}} / \frac{\text{PAS}}{\text{FS}}$$

$$\text{frame number } (f) = \log_2 M$$

$$M = 2^f$$

$$\text{frame offset} = \text{page offset}$$

- Physical address format PA $\boxed{P \ d}$



③ organization of MMU:

- Each process is associated with its own page table, which are stored in memory

- Page tables are organized as a series of Entries.

- Num of entries in page table = Num of pages

$$\text{PT Entries} = N$$

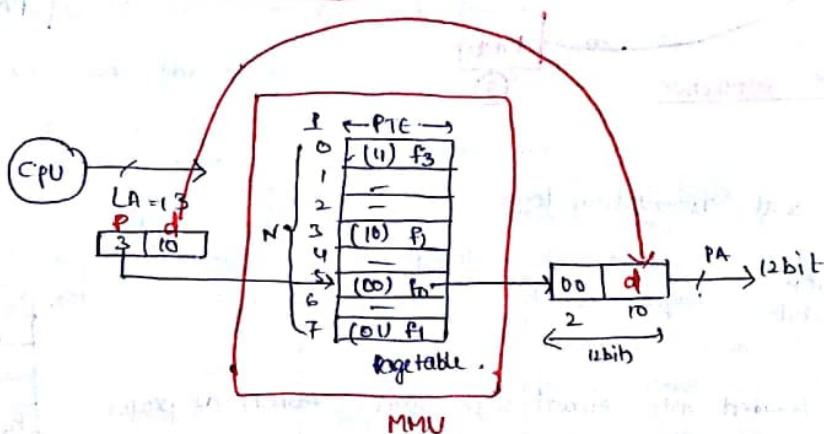
- PTE Contains the frame num in which the page is present

- PTE size 'e' is in bytes.

$$\begin{aligned} e &> 1B \\ e &\sim f \text{ [bytes]} \end{aligned}$$

$$\text{PTS} = N * \text{PTE} \quad (e)$$

$$\boxed{\text{PTS} = N * e}$$

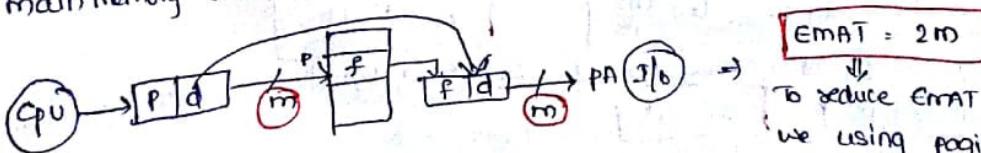


Performance of paging:

(1) Temporal issue: Goal: Reduce effective mem access time (EMAT)

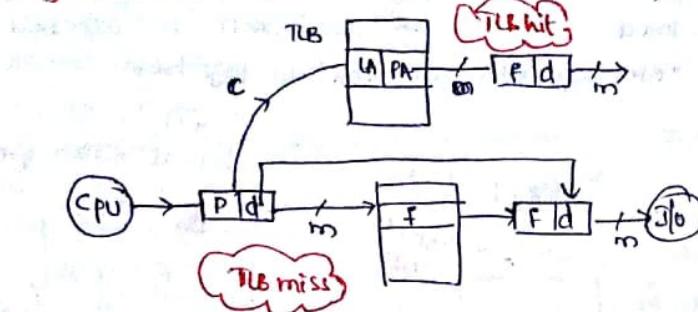
Improve throughput.

Let main memory access time be 'm'.



To reduce EMAT from $2m$ to near m , we use paging with TLB.

Paging with TLB : (Translation look aside buffer)



$C \rightarrow$ TLB mem access time
 $\alpha \rightarrow$ hit ratio
 $1-\alpha \rightarrow$ miss ratio.

$$EMAT_{TLB} = \alpha[c+m] + (1-\alpha)[c+2m]$$

(ii) special issue: Goal : Reduce pagetable size.

Ex:- IA = 32 bits
 $PS = 4KB$ $N = \frac{2^{32}}{2^{12}} = 2^8 = 1M$ pages

Assume that each entry occupies 4B

$$\therefore PTS = 4 + 1M \rightarrow 4MB/\text{proc}$$

For 100 processes

$$PTS = 400MB \rightarrow \begin{array}{l} \text{Not desirable} \\ \downarrow \text{sol} \end{array} \rightarrow \begin{array}{l} \text{Increasing page size} \\ \text{multilevel paging} \end{array}$$

$$PTS \propto N \propto \frac{LAS}{PS}$$

a) Increasing page size:

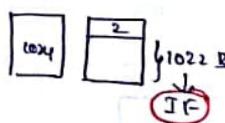
If $PS = 8KB$ then $N = 512k$
 $PTE = 512k$ entries.

But increasing page size will lead to fragmentation at last page.

Ex:- If $PS = 1024B$

Prog size $\rightarrow 1026B$

Num of pages = 2



$PS = 2B$
 $Prog\ size = 1026B$

Num of pages = 513

No IF

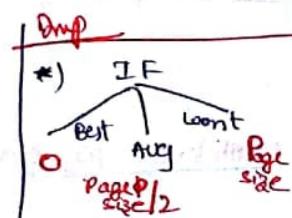
So, optimal page size should be selected.

sol \downarrow
 $\begin{cases} LAS - 's' Bytes \\ PTE - 'e' Bytes \\ PS - 'p' Bytes \end{cases} \rightarrow PTS = \frac{s}{p} \times e \quad IF = \frac{p}{2}$
 To reduce PTS + IF

$$\frac{d}{dp} \left(\frac{s}{p} \times e + \frac{p}{2} \right) = 0.$$

$$\frac{-se}{p^2} + \frac{1}{2} = 0.$$

$$p = \sqrt{2se}$$



b) multi level paging : (Paging on page table)

Paging as a concept involves 3 steps

Step 1 : Divide AS into equal size pages.

Step 2 : Store the pages in frames of PAS.

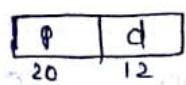
Step 3 : Access the pages of the AS in the frames through a page table.

→ Multi level paging implies paging on page table i.e. the page table is divided into pages. The pages of the page table are stored in frames of PAs, which are accessed through another page table known as outer page table or first level page table.

Eg:- let

$$LA = 32 \text{ bit}$$

$$PS = 4 \text{ KB}$$

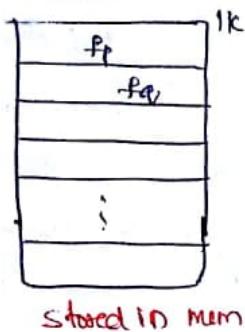


let pages in PT = 1K

$$PS_{PT} = 1 \text{ K}$$

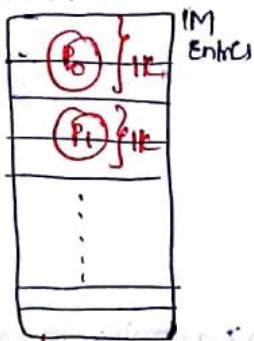
Outer PT

Step(3)



stored in mem

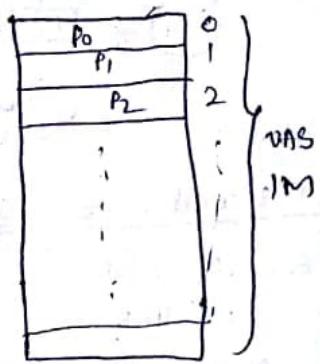
Inner PT Step(3)



↓ Step(1) memory pushed to disk

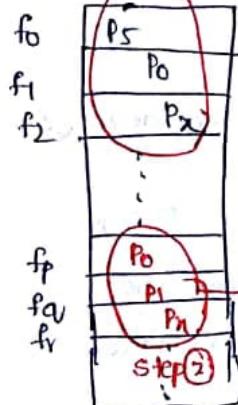
Step(1)

logical address space



Step(2)

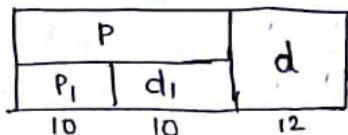
Pages of VAS



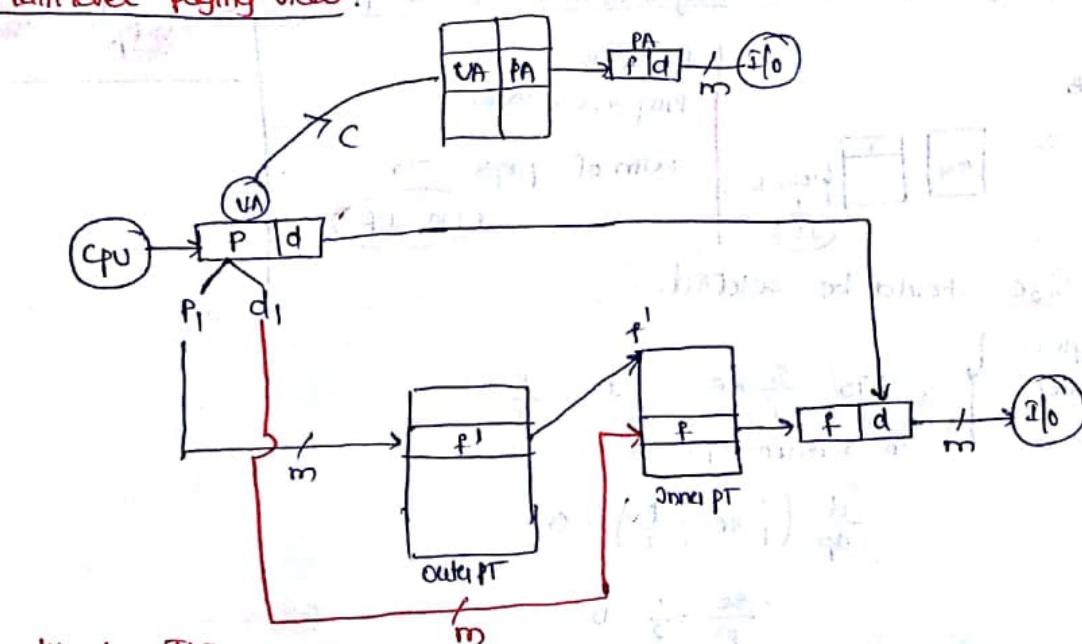
Pages of PT

main memory

Address Format:



Multi level paging view:



without TLB

$$EMAT_{1\text{p}} = 2m$$

$$EMAT_{2\text{p}} = 3m$$

⋮

$$EMAT_{n\text{p}} = (n+1)m$$

with TLB

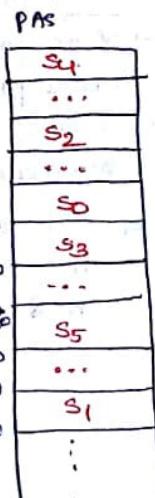
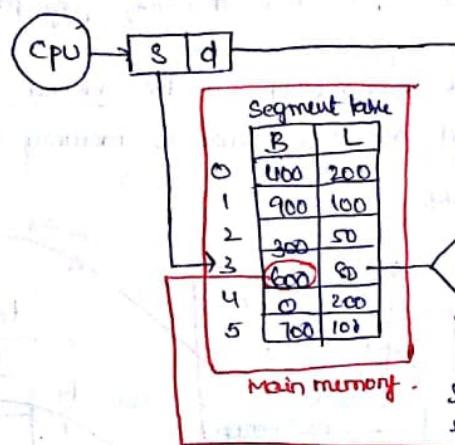
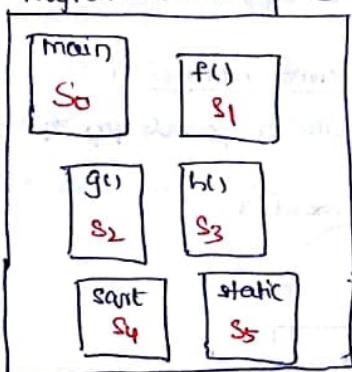
$$EMAT_{2\text{p TLB}} = \chi[c+m] + (1-\chi)[c+3m]$$

$$EMAT_{n\text{p TLB}} = \chi[c+m] + (1-\chi)[c+(n+1)m]$$

Segmentation :

- Paging doesn't preserve user view of memory allocation to programs.
- As per user view of memory allocation program is divided into logical units known as segments.
- A segment may represent a function, procedure, block or Datastructure.
- These segments are assumed to be stored in the main memory in their entirety at non-contiguous locations.
- These segments are accessible through segment table by Address translation.
- The segment table will have entries amounting to num of segments and each entry contains the base addr of the segment in PAs and size of the segment.

Program Address space



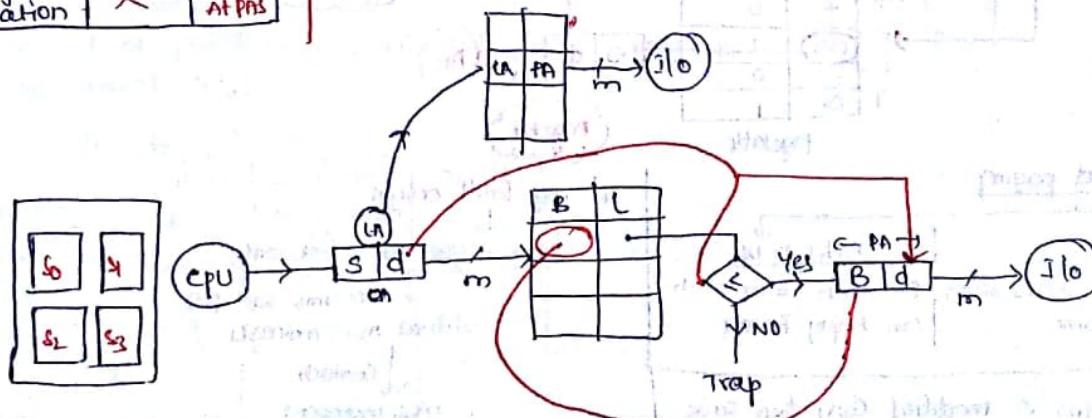
LA's	PA's
<2,15>	300+15 = 315
<3,70>	600 + 70 = 670
<5,10>	Trap
<8,21>	Trap .

Paging vs segmentation :

	IF	EF
Paging	✓ at page	X
Segmentation	X	✓ at PAs

Performance of segmentation :

$$EMAT_{TLB} = \alpha [c+m] + (1-\alpha) [c+2m]$$



*) paging is introduced in segmentation for 2 reasons

(i) To associate a smaller Address table with the process by applying paging on segment table.

(ii) To overcome external fragmentation arising in PAs while storing segments.

In this case paging is applied on segments.

The resultant Architecture is known as segmented paging architecture.

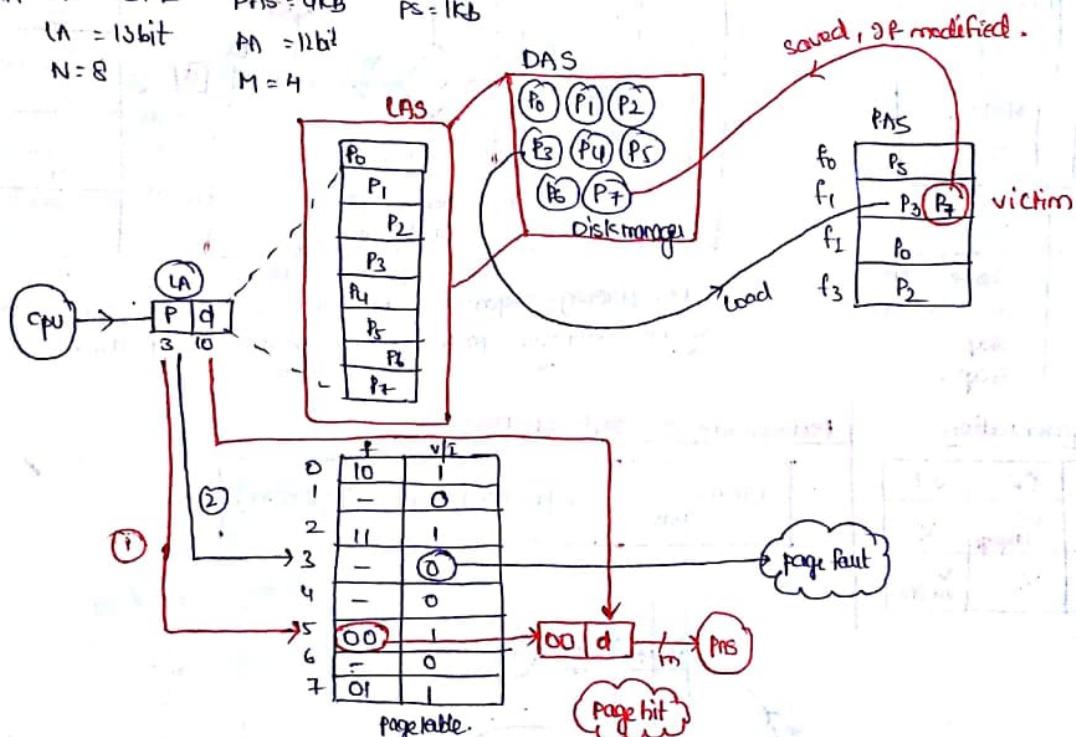
Virtual memory:

- virtual memory gives an illusion to the programmer that a huge amount of memory is available for executing programs greater than the size available at physical memory.
- Virtual memory is implemented through Demand paging

Demand paging:

- It implies loading the pages on demand basis
- program is assumed to be stored on disk in the form of pages. These pages are initially loaded in the memory depending on the num of frames available.
- The referred page in the VA may be present in the frame- (Page hit) or may not be present (Page fault)
- If the page present in memory then it is resolved using page table as in the case of simple page.
- If the page is not present in the main memory then the virtual memory manager makes arrangement to bring the faulted page from disk to memory with a possible page replacement.

Ex:- LAS = 8KB PMS = 4KB PS = 1KB
 LA = 15bit PA = 12bit
 N = 8 M = 4



*Demand paging

- | | |
|------------------------------------|--|
| put DP : | Prefetch DP |
| Execution starts with empty frames | Execution starts with non-empty frames |

- * If victim is modified Copy then save the page to disk and load the selected page to memory

- * After replacement process moves to ready Q and got scheduled and executed further

*Page fault occurs

- Process goes to block state
- informs valid page
- virtual mem manager
- contacts disk manager
- should load requested page to main mem through DMA
- If free space avail → load
- If no free space → select victim by page rep strategy

Performance of virtual memory :

1) Effective memory access time :

EMAT \rightarrow 'm'

PF service rate \rightarrow 's'

PF rate \rightarrow 'p'

Page hit rate \rightarrow '1-p'

$$\text{EMAT}_{\text{DP}} = p + s + (1-p)m$$

initially

Points to remember :

event

Technique	EMAT
Paging	$2m$
n-level paging	$(n+1)m$
Paging with TLB	$x(c+m) + (1-x)(c+2m)$
2level Paging with TLB	$x(c+m) + (1-x)(c+3m)$
n-level paging with TLB	$x(c+m) + (1-x)(c+(n+1)m)$
Segmentation	$x(c+m) + (1-x)(c+2m)$
Demand paging	$p + s + (1-p)m$

* Segmented paging without TLB = $3m$

* Segmented paging with TLB = $x(c+m) + (1-x)(c+3m)$.

2) Page replacement :

Page ref string = { set of successively unique pages referred in the given list of VA's }

Pr: $\{ \text{VA} \}$ $\{ 722; 715; 012; 834; 755; 854; 860; 011; 339; 964; 654; 555 \}$
 $P_{\text{S}} = 100$ $P_{\text{A}} = 22$

$$P_{\text{A}} = \frac{\text{VA}}{\text{PS}}$$

Ref string : $< 7; 0; 3; 7; 8; 0; 3; 9; 6; 5 >$

length of ref string (L) = 10

Num of unique pages = 7

Every process demands 'n' num of frames

Frame Allocation policies :

$n \rightarrow$ num of processes

$s_i \rightarrow$ demand of process P_i

$D \rightarrow$ Total demand ($\sum s_i$)

M : Frames Available

a_i : Allocated frames to process P_i

$M \leq D$

$M \leq \sum s_i$

Ex:- $n=5$; $\{ P_1 \dots P_5 \}$; $M=40$

	$a_i = \frac{M}{N}$	$a_i = \frac{s_i}{D} * M$	Proportional Alloc	50% rule
P_1	$5 \frac{\text{wood}}{\text{star}}$	8	2	2
P_2	$30 \frac{\text{starvation}}{\text{starvation}}$	8	15	15
P_3	10	8	5	5
P_4	15	8	7	7
P_5	20	8	10	10
	$D=80$	$M=40$	$M=39$	$M=39$

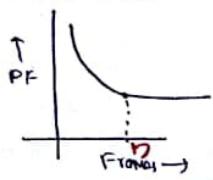
lego

Page replacement techniques :

① FIFO :

Criteria: Time of loading (TOL) \rightarrow present in page table

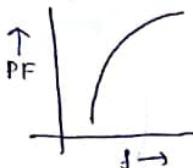
FIFO curve



Belady's Anomaly:

$< 1 \ 2 \ 3 \ 4 \ 1 \ 2 \ 5, 1 \ 2 \ 3 \ 4 \ 5 >$

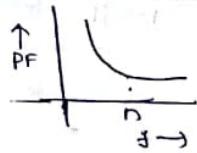
f	U/I	Tol
0	x	1 5



② Optimal page replacement :

In the Event of page fault select that page as a victim which will not be used for the longest duration of time in future references.

Optimal PR Curve :



- Practically non-implementable
- Benchmark

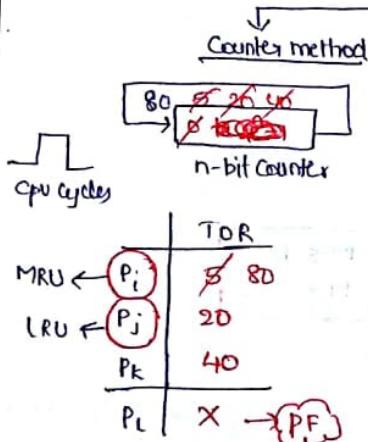
③ Least recently used (LRU) :

Criteria: Time of reference.

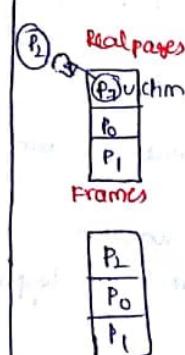
LRU Implementation :

\rightarrow In most cases LRU is very close to optimal page replacement

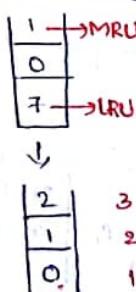
Implementation



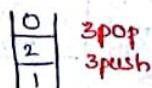
\therefore it may fail bcoz it can count upto 2^n clocks



stack method



if no page fault also the stack should be updated



worst case (bottom)
2n operations

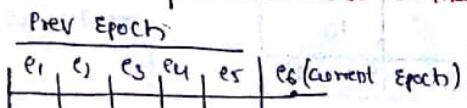
Best Case (Top next element)
4 operations

\therefore more stack overhead.

LRU approximations :

① Reference bit :

Criteria: R \rightarrow 0 \rightarrow Page not referred so far during present Epoch
1 \rightarrow page referred atleast once within current epoch.



Page table

	V/I	TTL	R	M
0	a	1	4	1 0
1	b	1	2	0 1
2	-	0	-	-
3	c	1	0	1 0 0
4	d	1	3	1 1
5	e	1	1	0 0
6	f	1	5	0 1

P_i is victim

Second chance.

P_s is victim by
second chance Algo.

② Additional reference bits :

	R ₁	R ₂	R ₃	R ₄	R ₅	R ₆	R ₇	R ₈
P _i	0	1	1	1	0	1	0	1
P _j	1	0	0	1	1	0	1	1
P _k	1	0	1	1	1	1	1	1

convert Epoch

P_j is victim.

During Every new Epoch these 8 bit reference should be left shifted which is an 0H.

③ Second chance Algo :

- It is a FIFO based Algorithm
- It can suffer from Belady Anomaly

Criteria : Time of loading + R

FIFO.

if R's are 1

④ Enhanced second chance Algo :

- Not recently used Algorithm

Criteria : R + M (Modified bit)
Refered/not Modified/not

* If we move from current Epoch to new Epoch we make all reference bits to '0'

⑤ Most recently used :

Criteria : Time of reference

⑥ Counting Algorithms

least frequently used (LFU)

Most frequently used (MFU)

least frequently used:

less count value

most frequently used

more count value

Thrashing :

→ Excessive / high paging activity

Effects

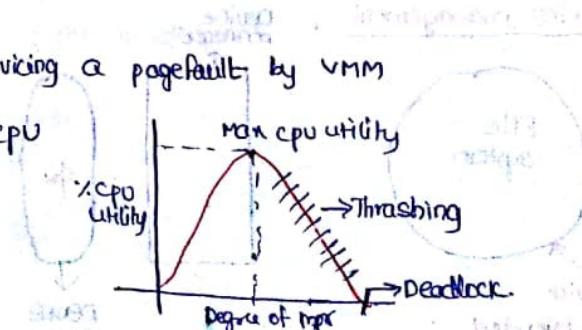
→ cost of servicing a pagefault by VMM

→ under utilization of CPU

Reasons for thrashing :

1) lack of memory (frames)

2) Degree of Multiprogramming



Control strategies of Thrashing:

Prevention:

→ Controlling degree of mpr

Detection + Recovery

Detection:

- low CPU utilization

- High degree of mpr

- High paging disk utilization

Recovery

- Decrease degree of mpr through suspension of processes.

Other reasons for thrashing:

1) Page replacement policy: Bad replacement algo

2) Page size: It influences

1) IF

2) page table size overhead

3) Thrashing → small pages more PF rate

3) Programming techniques:

Ont A [1..128, 1..128]

a) for $i \leftarrow 1$ to 128

for $j \leftarrow 1$ to 128

$A[i,j] = 1$

RMD, $P_s = 128W$

$M = 127$

Pure DP
FIFO

Case a

$f_1 [P_1 P_{128}]$

$f_2 [P_2 P_1]$

$f_3 [P_3 P_2]$

\vdots

$f_{127} [P_{127} P_{126}]$

Case b

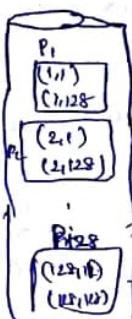
$f_1 [P_1 P_{128}]$

$f_2 [P_2 P_1]$

$f_3 [P_3 P_2]$

\vdots

$f_{127} [P_{127} P_{126}]$



$(128)^2$ PF

P_{128}

4) Data structures:

Arrays

→ Contiguous

→ less thrashing

Linked list

- non-contiguous

- more thrashing

Searching

Linear

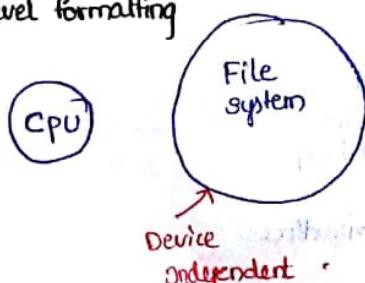
thrashing less

Binary

more thrashing

File system and Device management:

→ low level formatting



* stack : less thrashing

Hashing : more thrashing

Pointers : more thrashing

File system and Device management :

Device manager

H/W

S/W

device driver

Controller card

Hard disk,

Electro mechanical device

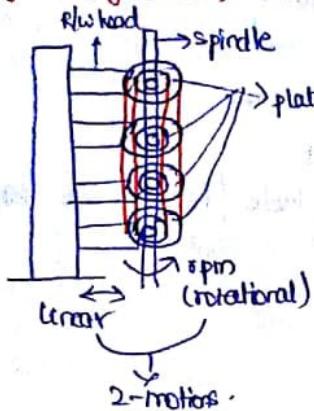
Interface

Serial Advanced Technology Attachment (SATA)

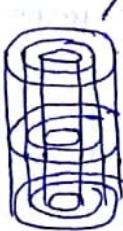
Intelligent Drive Electronics (IDE)

Small Computer System Interface (SCSI)

Physical geometry of Harddisk:



* Num of cylinders = Num of tracks.



Sector Addr Sector offset
data Error Correcting Code.
Good : Ecc matches
bad : ecc doesn't match

Disk I/O time :

$$1) \text{ Seek time} = |x-y| * \text{TTT} \text{ (Track-track time)}$$

$$2) \text{ Rotational latency} = \frac{R}{2} \text{ (universal)}$$

$$3) \text{ Transfer time} = \frac{YR}{X}$$

$$4) \text{ Data transfer rate} = \frac{X}{R} \text{ B/s}$$

$$\begin{aligned} X \times B &\rightarrow R \text{ sec.} \\ 1B &\rightarrow \frac{R}{X} \text{ sec.} \end{aligned}$$

Track size $\rightarrow X \times B$
Sector size $\rightarrow Y \times B$
Rottime $\rightarrow R$
 $X \times B \times Y \times B \rightarrow X \times Y \times B^2$
 $\frac{X \times Y \times B^2}{R} \rightarrow \frac{YR}{X}$

Disk logical structure (high level formatting)

Volumes

Primary	Extended / logical
\rightarrow Bootable	\rightarrow Non bootable
\rightarrow (OS + Data)	\rightarrow (Data)

Floppy drives

a; b;

fixed MBR

Partitions

c; d; e;

os1

os2

os3

MBR : master boot record

Partition table

Boot loader

Multi boot computer.

Booting process :

(H/w test) \leftarrow POST (Power on self test)
checks all H/w

\downarrow
checks all dp BIOS (Basic I/O system)
& dp systems

Bootstrap (Bootstrap is a pgm in ROM which loads MBR to main memory & gives control to boot loader)

Boot loader (Provides option to select os)

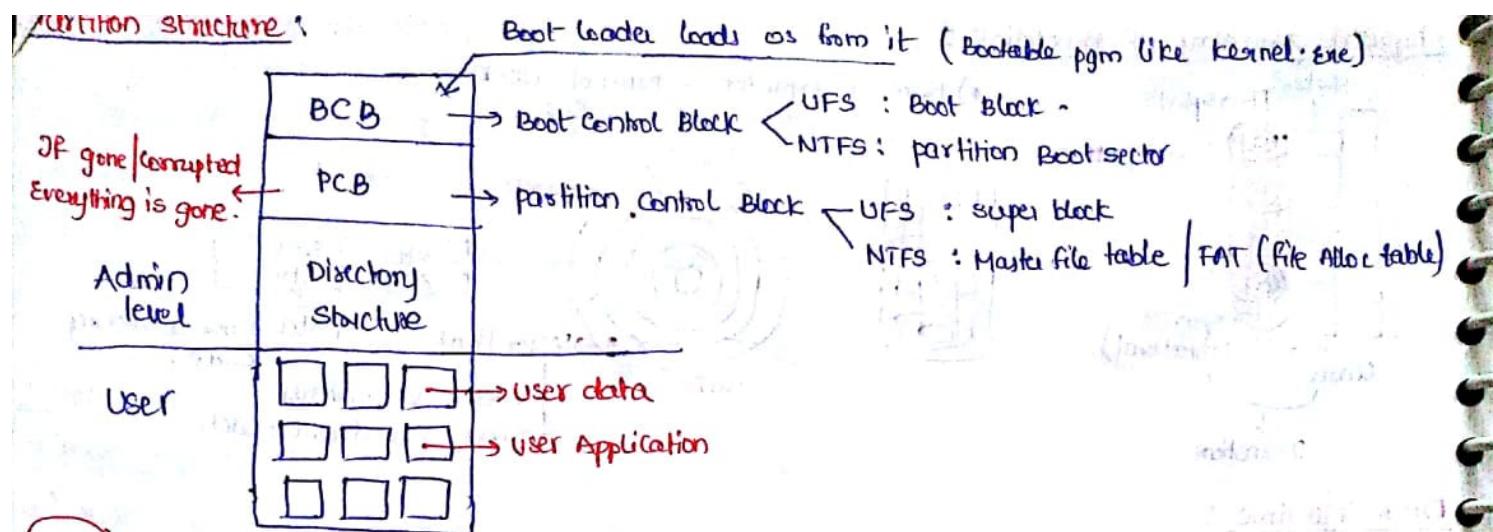
GRUB
Grand unified
Boot loader
(UNIX)

Lilo
Linux loader
(Linux)

NT LDR
Windows

shell pgm/GUI

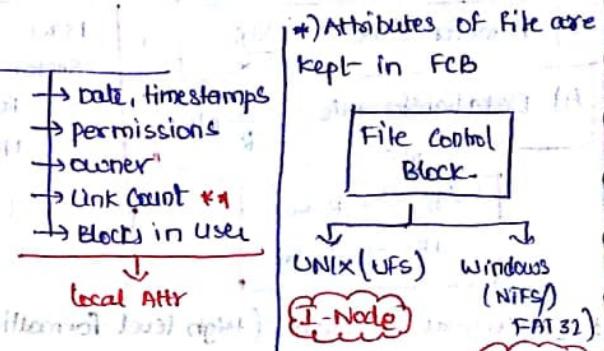
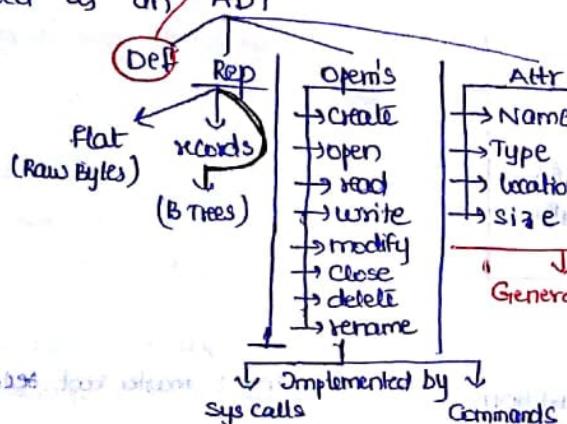
\downarrow
Booting completed.



Files & Directories :

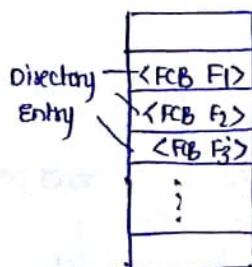
Collection of logically related records.

Viewed as an ADT



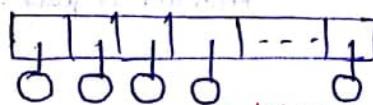
Directories : A special file which contains attributes of the file in a well organized structure.

Abstract view :



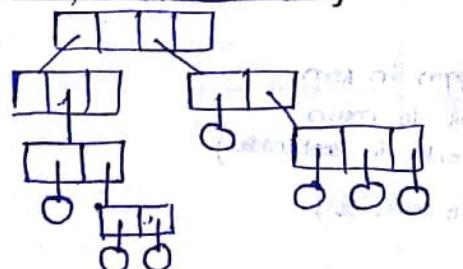
Directory structures :

① single level directory structure :

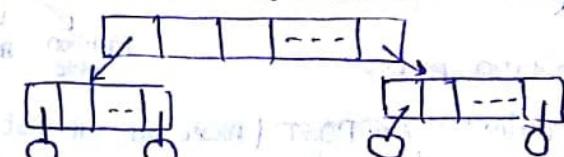


More searching time, can't have same name for the files -

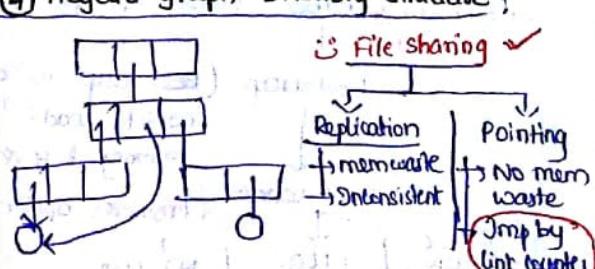
③ Tree structured directory :



② two level directory structure :

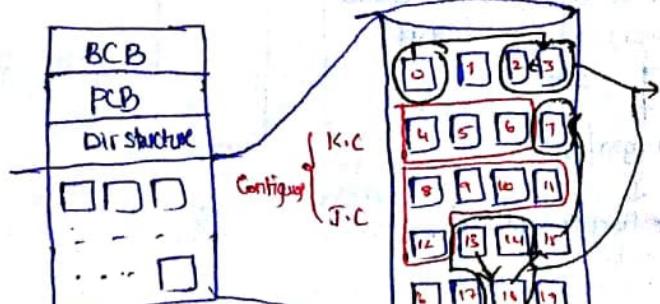


④ Acyclic graph Directory structure :



File Allocation methods :

- Contiguous Alloc
- Noncontiguous / linked Alloc
- Indexed Alloc



$\square \rightarrow$ DBA (Disk Block Address) \Rightarrow 16 bits $\rightarrow 2^{16}$, 64 KB blocks
 DBS (Disk Block Size) \Rightarrow 1KB \rightarrow Block size.
 \downarrow
 $2^{16} \text{ KB} \rightarrow 64 \text{ MB}$

Configured Alloc:

Gen	local	First DBA	Num of Blocks
F.N.	---	First DBA	Num of Blocks
K.C.	---	4	3
J.C.	---	8	5

Performance Issues

- ① IF: ✓ (last block)
- ② EF: ✓
- ③ Increased file size: Difficult to increase relocation should be performed.
Inflexible
- ④ Type of Access: seq access random access.

○ Faster

Non-Configured Alloc:

Gen	local	First DBA	Last DBA
F.N.	---	First DBA	Last DBA
K.C.	---	13	7
J.C.	---	0	2

Performance Issues:

- ① IF: ✓ (last block)
- ② EF: ✗ (Never)
- ③ Increased file size: Flexible.
- ④ Type of Access: seq access.

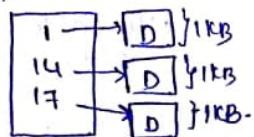
○ Slower

- pointer consumes disk space
- vulnerability of ptrs leads to file truncation.

Indexed Allocation:

Gen	local	Index Block
F.N.	---	Index Block
K.C.	---	16
J.C.	---	19

16) Index Block



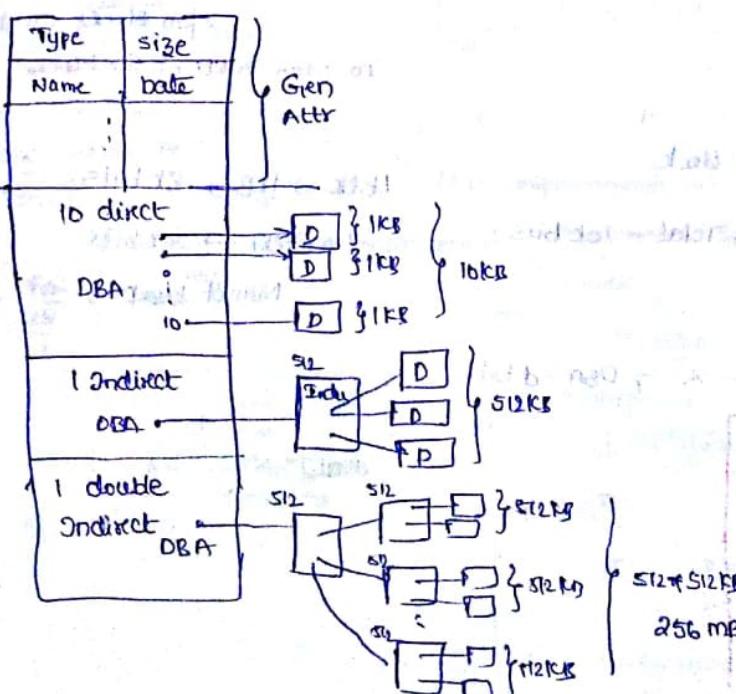
Unix Directory Implementation and Allocation method:

FN	Inode	DBA: 16 bits	wrt INode
K.C.	23	DBS: 1KB	Filesize: $10\text{KB} + 512\text{KB} + 256\text{MB}$ $= 256,522\text{ MB}$

Max file capacity: $2^{16} \times 1\text{KB} = 64\text{MB}$



I Node:



DOS | Windows Directory Structure :

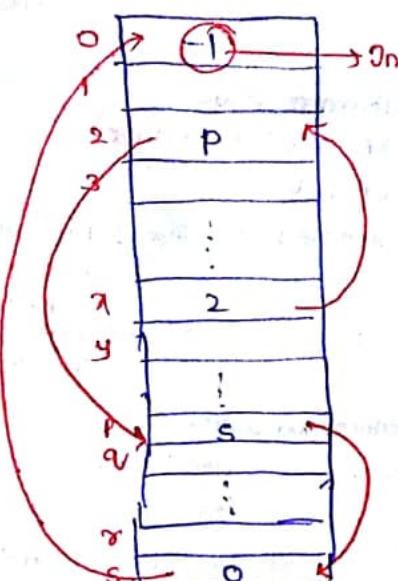
Gen	Local
FN	First DBA
K.C	2

* Num of Entries in FAT = Num of blocks

* FAT entries holds addresses DBA of next datablock in use by file

* Fat entry size = DBA bits.

File Alloc table (FAT) / Master File table



(Circular Linked Allocation)

$$DBS = 1KB, DBA = 16 \text{ bits}, \text{Disk Size} = 20MB, \text{Blocks} = 20K$$

* linked list of free blocks.

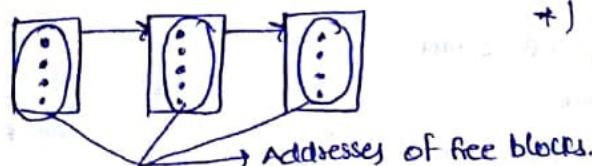
Disk free space mgmt:

Free space Allocation techniques :

① Free Linked List (FLL) :



② Free list :



+ Best policy to Allocate free blocks because no searching is reqd

$$1 \text{ BLK} \rightarrow \frac{1KB}{16} \rightarrow 512 \text{ Addr.}$$

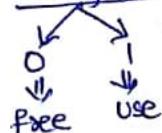
$$20K \text{ blocks} \rightarrow \frac{20K}{512} \text{ Addr.}$$

→ [No Block] worst case

To store addr of free blocks

③ Bit map / Bit vector:

- Associate a binary bit with each block



→ Total → 20k bits.

$$1 \text{ BLK} \rightarrow 1KB \rightarrow 8k \text{ bits.}$$

$$20K \text{ blocks} \rightarrow 20k \text{ bits}$$

$$\text{Num of blocks} \approx \frac{20K}{8K} \approx 2.5$$

bits to remember::

Num of Blocks - B , Block size - X , DBA - d bits.

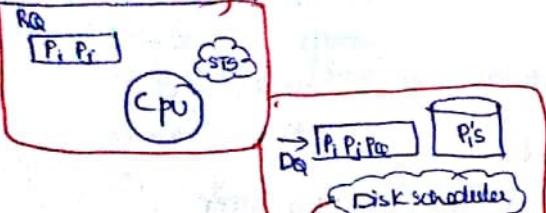
① Disk size - BX

② Max num of disk blocks - 2^d

③ Max disk size - $2^d + 2$

④ $B \leq 2^d$

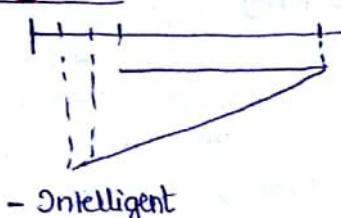
Disk scheduling :



* processes present in block state

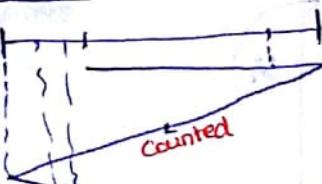
Objective:
To optimize num of seeks of a disk

(4) look :

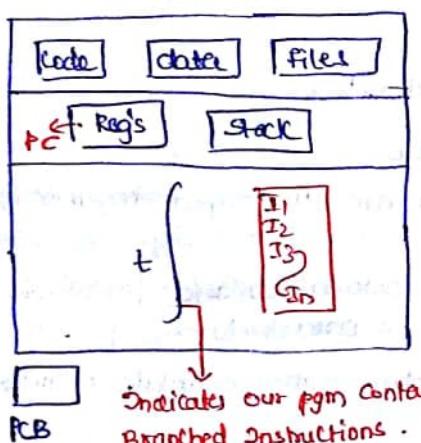


- Intelligent

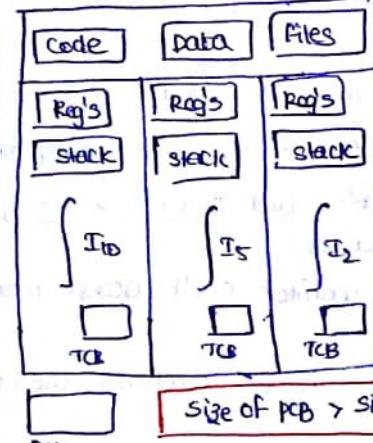
(5) C-scan :



Multithreaded process :



Indicates our program contains branched instructions.



size of PCB > size of TCB

Thread definition :

- light-weight process
- unit of CPU utilization
- Active Entity

- *) - Resource sharing
- economical (cost effective)
- $|TCB| < |PCB|$
- ↳ faster thread switching than context switching

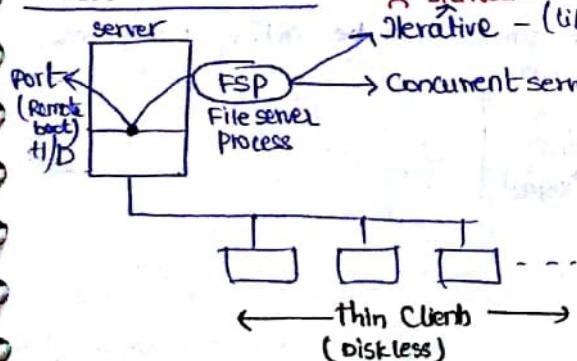
more performance

computation speedup in Multicore Arch



Evolution of Threading :

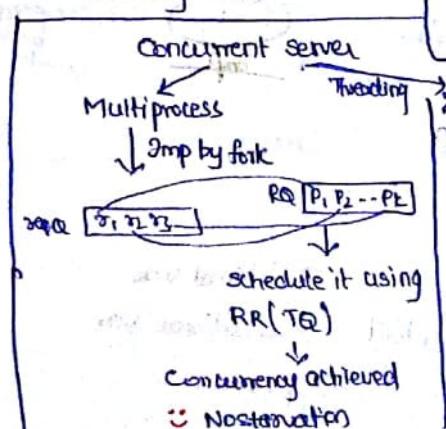
Client server Arch



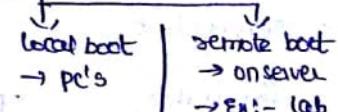
↳ starvation

Iterative - (like uniprogrammed OS)

Multiprocess + Threading



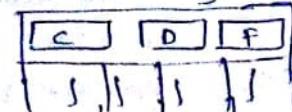
*) Booting :



↳ if k processes should run off k copies of (code, data) files

↳ SQL

Threading



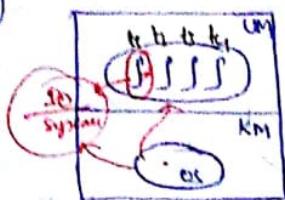
Types of threads :

1) User level threads (Java threads, POSIX threads)

2) Kernel level threads

↳ (portable as interface for UNIX)

*)

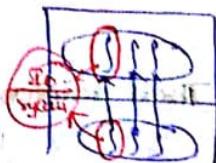


In OS view the seq made by process 'p'

so, the OS blocks the total process therefore t2 to t5 get blocked Even though it is active.

Resolution

Making multithreads in kernel mode



User level thread :

- Thread mgmt. can be done by user

- ⚡ Flexibility

Transparency

Fastest Context switching (bcoz of no mode shifting)

(Horizontal switching rather than vertical switching.)

Monitors : (Hansen)

*) Semaphore : If it is not programmed well it leads to deadlock.

→ Monitor is implemented as an ADT in the programming language

↳ collection of procedures, variables and data structures that are all grouped together in a special kind of module or package.

*) procedures that run outside the monitor can't access monitor internal variables (abstraction) & datastructures

*) However they can activate monitor member functions, which again can manipulate monitor datastructures & internal variables.

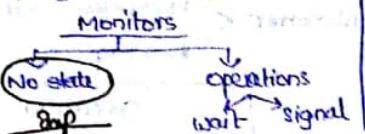
*) Monitors also contain condition variables along with mutex lock

*) Condition variables are associated with wait and signal operations which are used to meet the sync requirements of the application.

*) Monitors have an important property that only one process can be active at any time

*) Semaphores

↓ state (value)
operations
up down



Producer Consumer problem :

Monitor prod_cons
begin

 Integer Count → Internal vars
 Condition Empty, Full → Conditional var
 Procedure Enter → procedure
 begin

```

        JF (count == N) full.wait();
        Buffer[in] = itemp;
        in = (in + 1) % N;
        Count = count + 1;
    end JF (count == 1) Empty.signal();
Procedure remove → procedure .
begin
    JF (Count == 0) Empty.wait();
    itemc = Buffer[out];
    out = (out + 1) % N
    Count = count - 1;
    JF (Count == N - 1) full.signal();
end
Init : count = 0;
End monitor;

Procedure producer
begin
    while (True)
    {
        a) produce item(&itemp);
        b) prod-cons. enter;
    }
end.

```

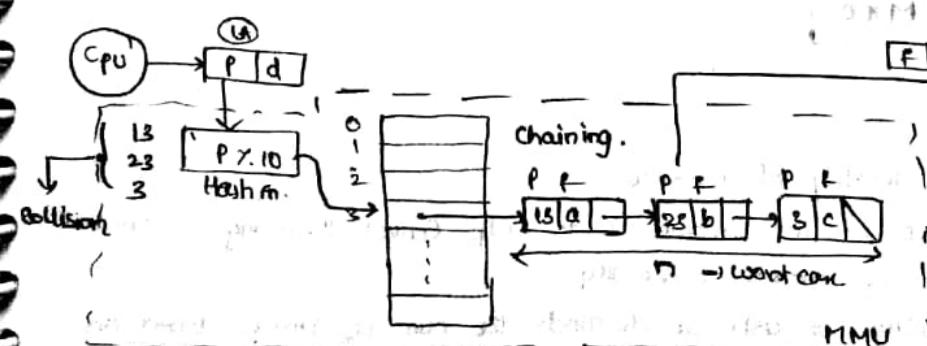
outside fn wants to access monitor so implicitly mutual lock is applied so that one process can run on monitor.

Hashed paging:

To reduce page table size

Multilevel paging Hashed paging

Inverted paging



Space Efficient

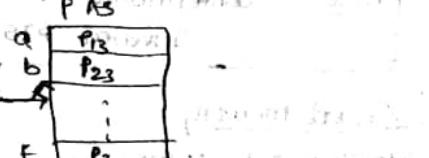
$O(n) \rightarrow$ sequential access.

Procedure Consumer

```

begin
    while (True)
    {
        a) temp = prod-cons. remove;
        b) process item(temp);
    }
}

```

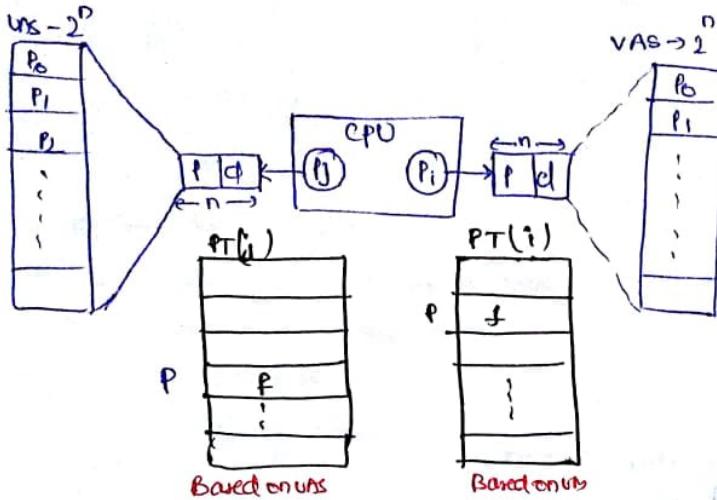


Conventional paging: $O(1)$

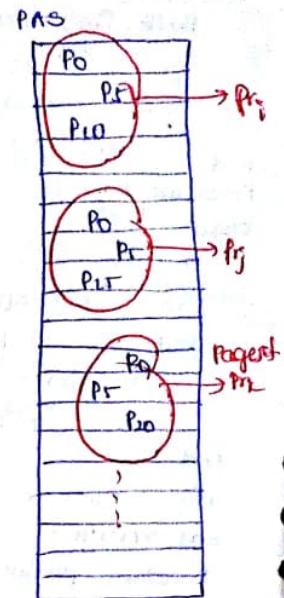
Inverted paging:

- reduce page table size
- implements global page table.

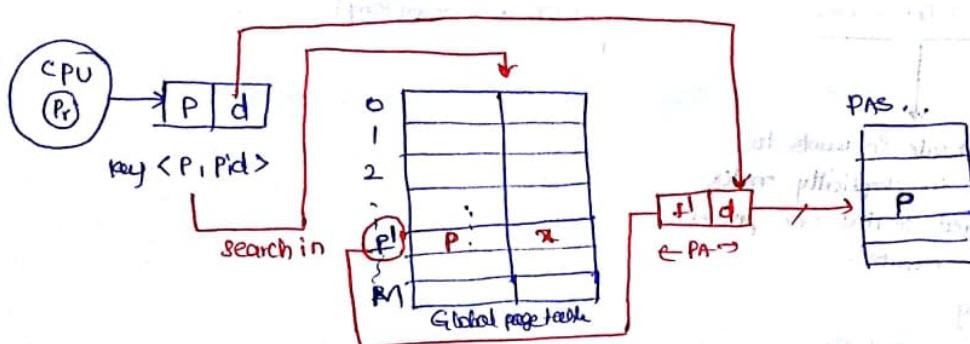
Generally.



Frame table	
Page number	Pf
0	P0
1	P0
2	P0
3	P0
4	P0
5	P0
6	P0
7	P0
8	P1
9	P1
10	P1
11	P1
12	P1
13	P1
14	P1
15	P1
16	P1
17	P1
18	P1
19	P1
20	P1
21	P1
22	P1
23	P1
24	P1
25	P1
26	P1
27	P1
28	P1
29	P1
30	P1
31	P1



Address translation in Inverted paging:



∴ searching is $O(n)$ | ∴ space optimization is present in Inverted paging

Note: Conventional PTS = $N \times e$
Inverted PTS = $M \times e$

Virtual memory

Working set strategy:

- Based on the principle of locality of reference
- Primary objective of the working set model is to help control thrashing ie controlling page fault rate and also utilize memory efficiently
- By applying principle of locality, it asks or demands the num of frames based on size of locality in which the program is executing
- The size of locality is estimated by applying or by determining working set window size of the process at every time

Consider a pgm

```

10 KB main()
{
    f();
}
5 KB f()
{
    g();
}

```

```

20 KB gl()
{
    h();
}
2 KB h()
{
    scanf();
}
18 KB

```

Prog size : 55 KB

let PS : 1 KB

Num of pages = 55

By frame alloc
(50% rule)

Asks 27 frames

↓
memory wastage may happen

because of demanding 10 pages, 5 pages,
20 pages, 2 pages, 18 pages -- etc.

To Control this we dynamically allot frames.

At runtime:

Ref string

Prk : 7, 0, 1, 2, 0, 1, 7, 6, 7, 0, 1, 3, 15, 18, 17, 16, 15 | 33 35 38 39 42 40 33 36 35 36 26

Now,

Working set window = $\{ \text{set of unique pages referred by process } k \text{ from time } t_i \text{ during past } \Delta \text{ references} \}$

Here

$\Delta \rightarrow$ Guess value

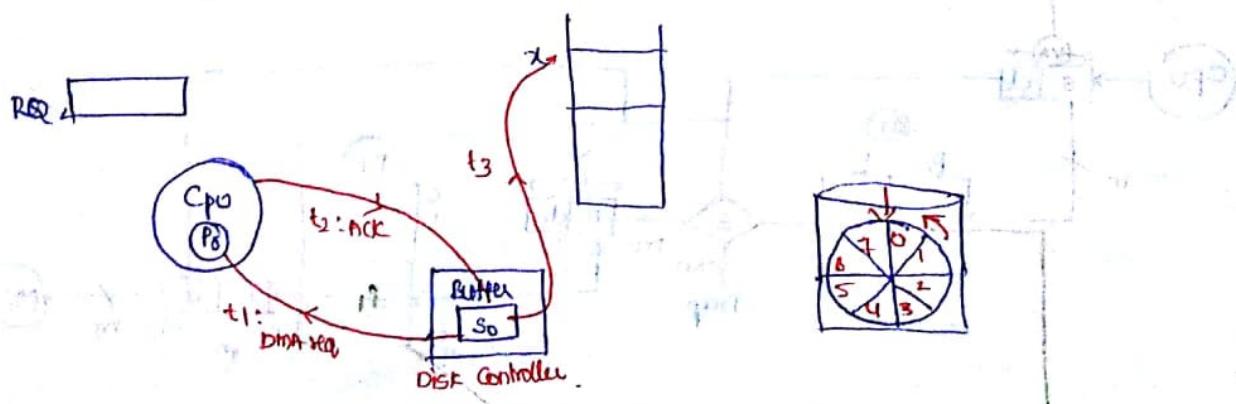
let $\Delta = 10$

$WSW_k^{\Delta=10} = \{ 33, 34, 35, 36, 38, 39, 40, 42 \}$

\downarrow
Size of working set window
 \rightarrow Always moving

* let $n = \text{num of processes}$
 $WSWS_i = \text{working set window size}$
 $D = \sum_{i=1}^n WSWS_i$, $M = \text{Frames Avail}$
 If $D = M$
 \rightarrow No Thrashing
 $D < M$
 \rightarrow No Thrashing
 \rightarrow more processes can be included
 If $D > M$
 \rightarrow Thrashing

Disk Interleaving:



Total time for transferring = $t_1 + t_2 + t_3$

Delay due to DMA off

At this time the disk head scans some more sector and it is instant

solution for the problems is.

HW sol

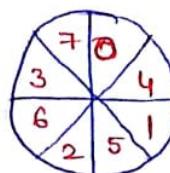
Providing more buffers

i) Cachiering

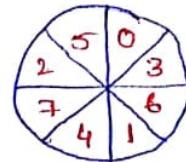
SW solution

Interleaving

Single Interleaving



double Interleaving



Segmented paging:

~~External fragmentation~~

→ Paging is used in segmentation to overcome the problem of external fragmentation

→ Segment is divided into pages and pages are stored in frames of memory which later are accessed through page table.

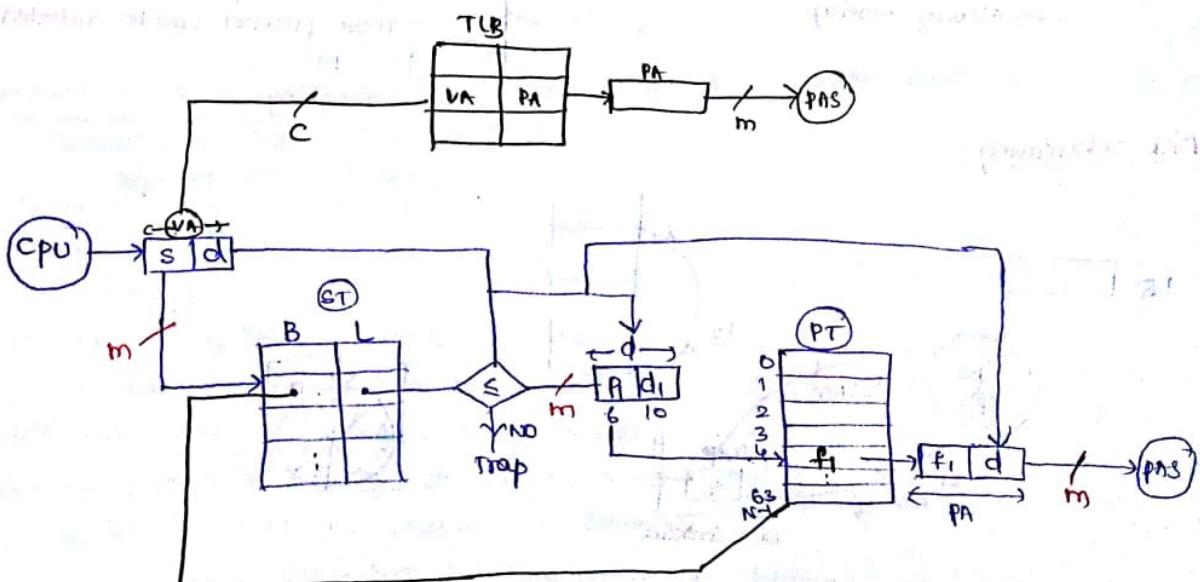
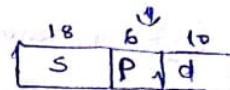
Every segment is referred through page table and page table is accessed through Segment table.

Ex:- VA : 34 bits $\langle 18, 16 \rangle$

max Num of seg = 2^{18} , max seg size = 2^{16} = 64KB

let PS = 1KB, So, for each seg, Num of pages = $\frac{64KB}{1KB} = 64$

ie



$$*) EMAT \text{ without TLB} = 3m$$

$$EMAT \text{ with TLB} = x[c+m] + (1-x)[c+3m]$$

—The End—