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REPORT ON LAB 4
COMBINATIONAL CIRCUITS

Lab Task:

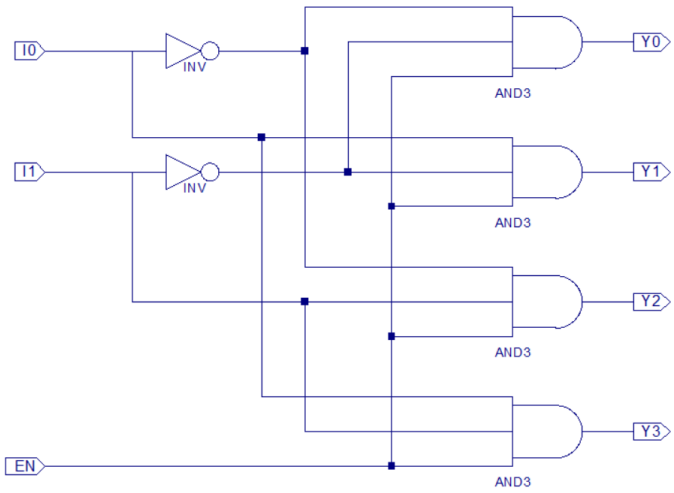
- Building a 2-to-4 decoder, simulating it and creating a symbol for it.
- Building a 3-to-8 decoder using two 2-to-4 decoders and other gates, simulating it and creating a symbol for it.
- Designing an 8-to-1 multiplexer using a 3-to-8 decoder and several other gates.
- Building it and simulating using several inputs.
- Test it using BASYS 2 board.

2 to 4 Decoder

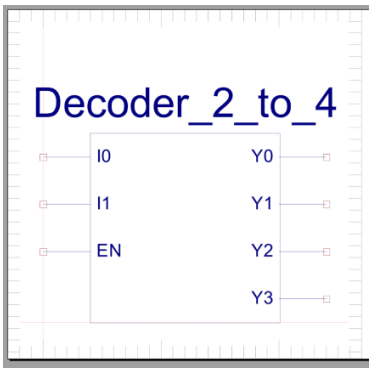
Truth table:

I1	I0	EN	Y3	Y2	Y1	Y0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0
X	X	0	0	0	0	0

Schematic Circuit:



Symbol:

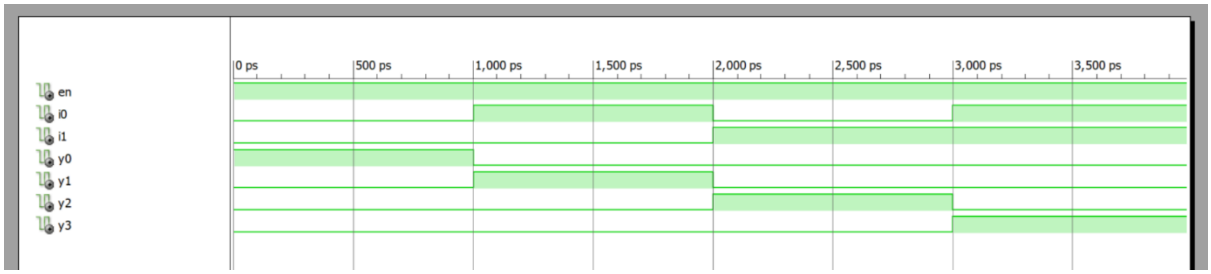


Test bench code:

```
-- *** Test Bench - User Defined Section ***
   tb : PROCESS
   BEGIN
            --Set the initial values
            I0 <= '0';
            I1 <= '0';
            EN <= '1';
            I0I1_Loop: LOOP
                WAIT FOR 1 ns;
                I0 <= NOT I0;
                WAIT FOR 1 ns;
                I0 <= NOT I0;
                I1 <= NOT I1;
            END LOOP I0I1_Loop;
      WAIT; -- will wait forever
   END PROCESS;
-- *** End Test Bench - User Defined Section ***

END;
```

Timing diagram:



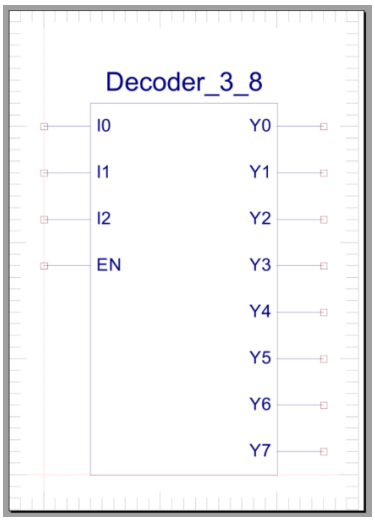
3 to 8 Decoder

Truth Table:

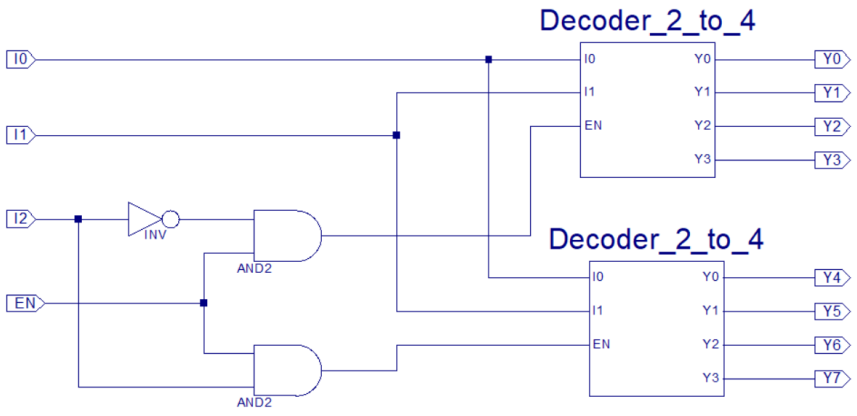
Inputs were selected by considering the index number.
160544_{10} = 0b 100 111 001 100 100 000_2
000, 100 and 001 were the inputs that I had selected

I2	I1	I0	EN	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	1	0	0	0	0

Symbol:



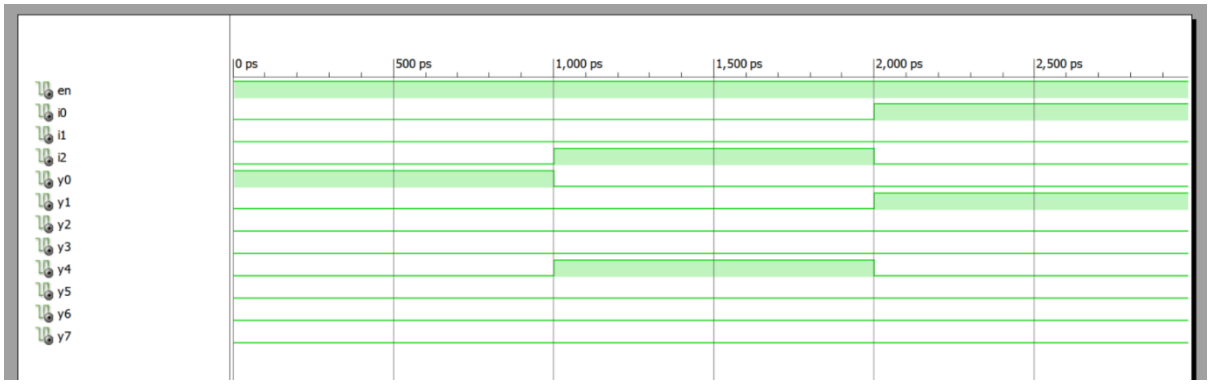
Schematic Circuit:



Test bench code:

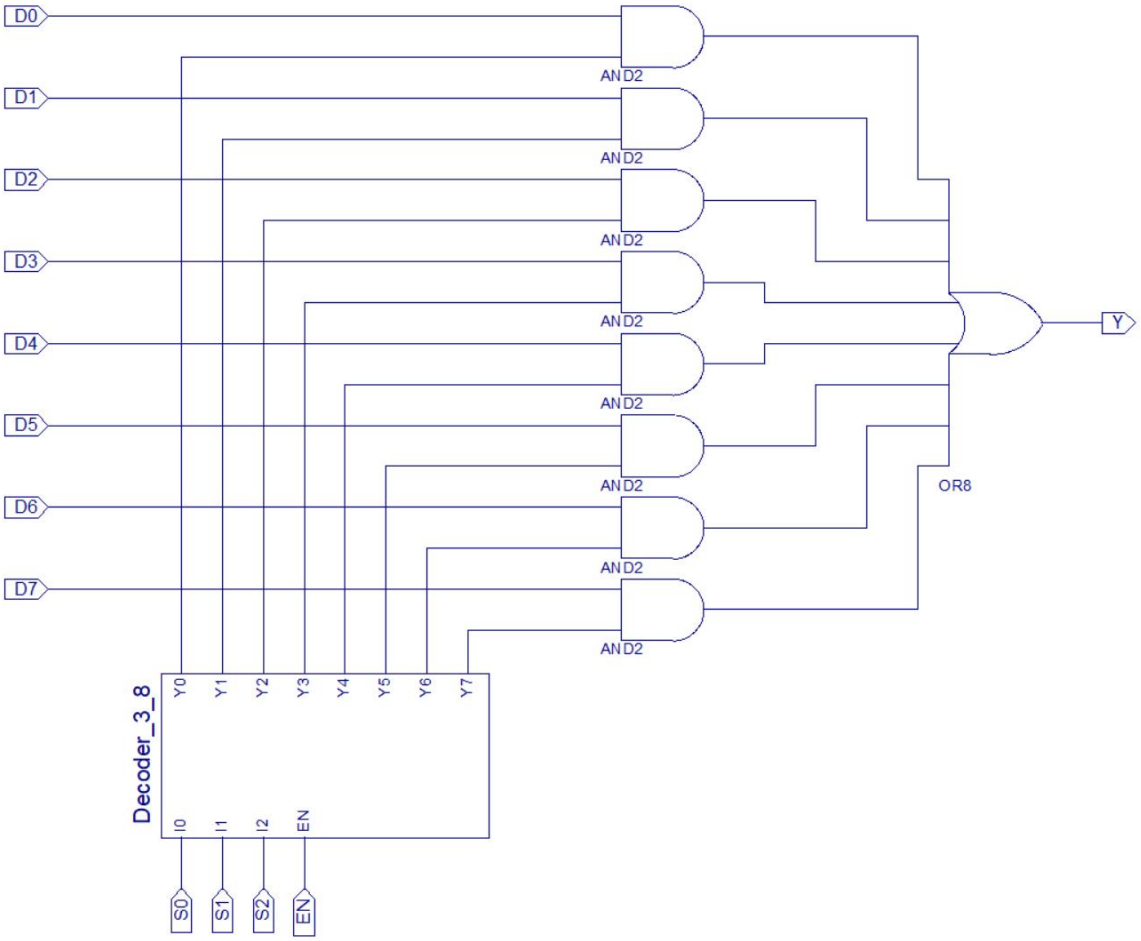
```
-- *** Test Bench - User Defined Section ***
   tb : PROCESS
   BEGIN
            EN <= '1';
            -- Index no. 160544 = 0b 100 111 001 100 100 000
            I0 <= '0';
            I1 <= '0';
            I2 <= '0';
            WAIT FOR 1 ns;
            --------------
            I0 <= '0';
            I1 <= '0';
            I2 <= '1';
            WAIT FOR 1 ns;
            --------------
            I0 <= '1';
            I1 <= '0';
            I2 <= '0';
      WAIT; -- will wait forever
   END PROCESS;
-- *** End Test Bench - User Defined Section ***
END;
```

Timing diagram:

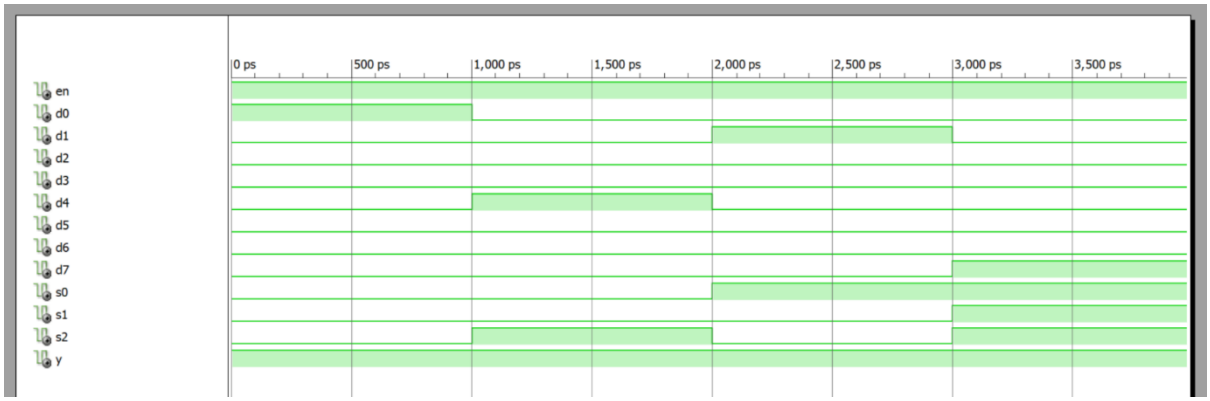


8-to-1 Multiplexer:

Schematic Circuit:



Timing diagram:



Test bench code:

```
-- *** Test Bench - User Defined Section ***
   tb : PROCESS
   BEGIN
            --Set the initial values
            en <= '1';
            D0 <= '0';
            D1 <= '0';
            D2 <= '0';
            D3 <= '0';
            D4 <= '0';
            D5 <= '0';
            D6 <= '0';
            D7 <= '0';
            S0 <= '0';
            S1 <= '0';
            S2 <= '0';
            -- Index no. 160544 = 0b 100 111 001 100 100 000
            -- 000
            D0 <= '1';
            WAIT FOR 1 ns;
            -- 100
            D0 <= '0';
            D4 <= '1';
            S2 <= '1';
            WAIT FOR 1 ns;
            -- 001
            D4 <= '0';
            D1 <= '1';
            S2 <= '0';
            S0 <= '1';
            WAIT FOR 1 ns;
            -- 111
            D1 <= '0';
            D7 <= '1';
            S1 <= '1';
            S2 <= '1';

      WAIT; -- will wait forever
   END PROCESS;
-- *** End Test Bench - User Defined Section ***
END;
```

In the above simulation, for every combination of switches the corresponding data input was changed to test whether the output reflects the specific input.

Conclusion:

At the end of the lab, I could,

- Design and develop 2-to-4 decoder, 3-to-8 decoder and 8-to-1 multiplexer using schematics design
- Verify their functionality via simulation.
- Test them using the BASYS 2 development board.