Group Members: - 1.160400H - K.Mathivathanan
2.160544C – V.Sajeevan
3.160658E – C.Vivek Vinushanth

Module: CS2052 - Computer Architecture

Report: Labs 9-10(Nano-Processor)

Report on Nano Processor

- Lab Task:

In both labs, we are assigned to design a simple Nano processor which can execute simple set of instructions. We also should design a 4-bit register bank which contains eight registers and a four-bit processor which can execute minimum four instructions. To complete the task successfully we built,

- Half Adder, Full Adder:

  These are one of the basic components in the circuit
- 4 bit add/subtract unit

  This unit can add and subtract numbers represented using 2 s complement.
- 3-bit adder:

  This unit is to increment the program counter.
- 3-bit program counter (PC):

  Program counter need to be reset to 0 when required. Hence build it was built using D flip flops with clear as an input. FDC is used to design the program counter and register bank.
- K- way b –bit multiplexers:

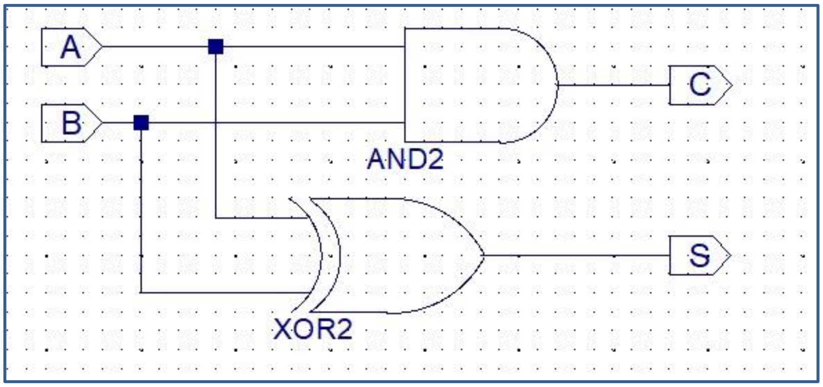
  A k-way b-bit multiplexer can take 'k' number of inputs, each with b-bits, rather than a single bit, and output is a group of b-bits. There are $\log_2 k$ control bits, and these control bits are used to enable one of the k groups of b bits.
  - ✓ Built a 2-way 3-bit multiplexer.
  - ✓ Built a 2-way 4-bit multiplexer.
  - Built a 8-way 4-bit multiplexer.
- Register:

  Can load data from a larger memory into registers where it is used for arithmetic operations and is manipulated or tested by machine instructions. Manipulated data is then often stored back to main memory, either by the same instruction or by a subsequent one. D flipflops have been used as a way of store memory.

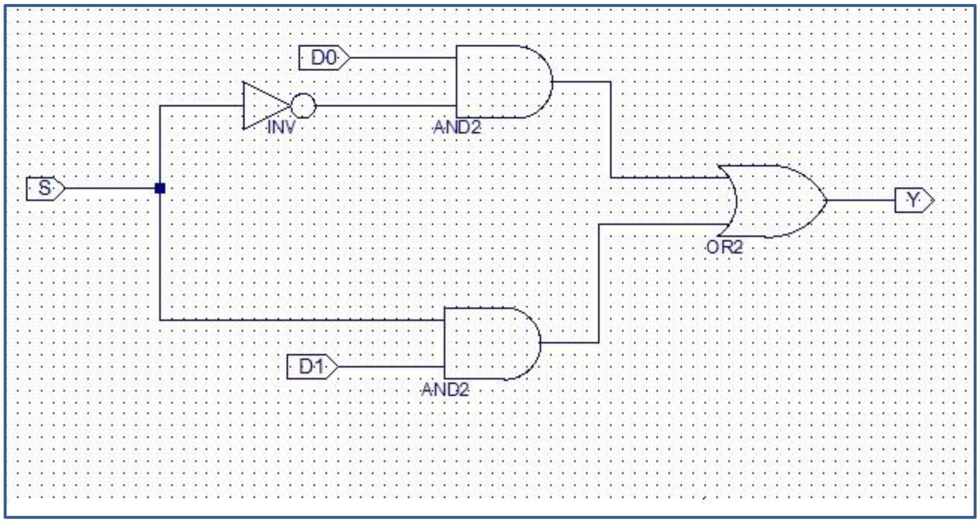
- ROM
- Instruction Decoder

✓ **<u>Schematic Diagrams and relevant Simulation diagrams</u>**

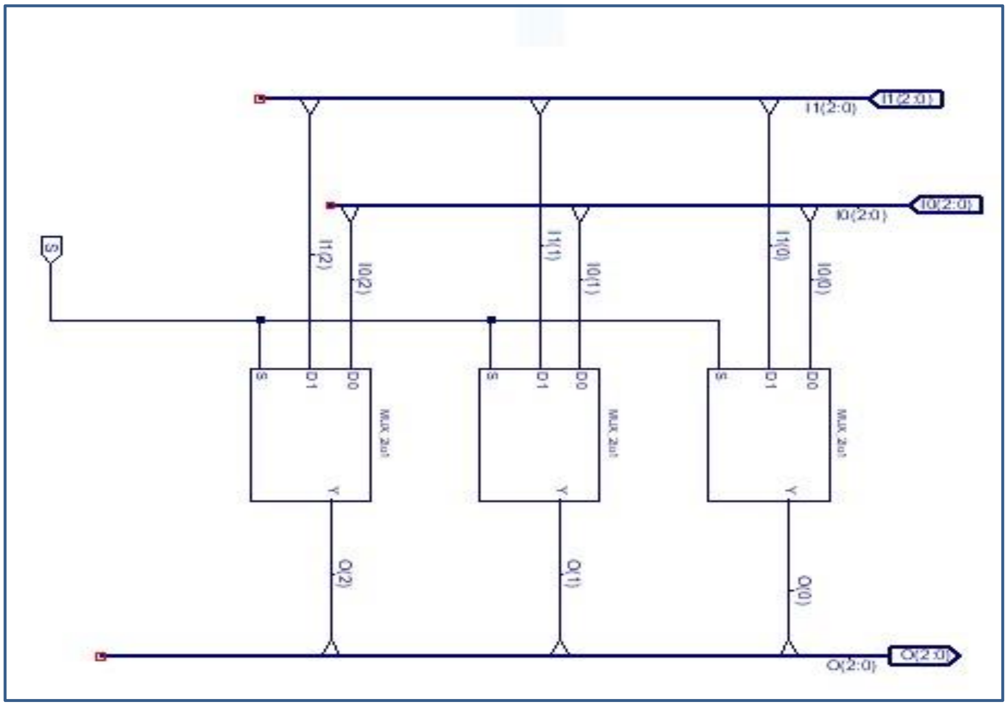
- Half Adder:



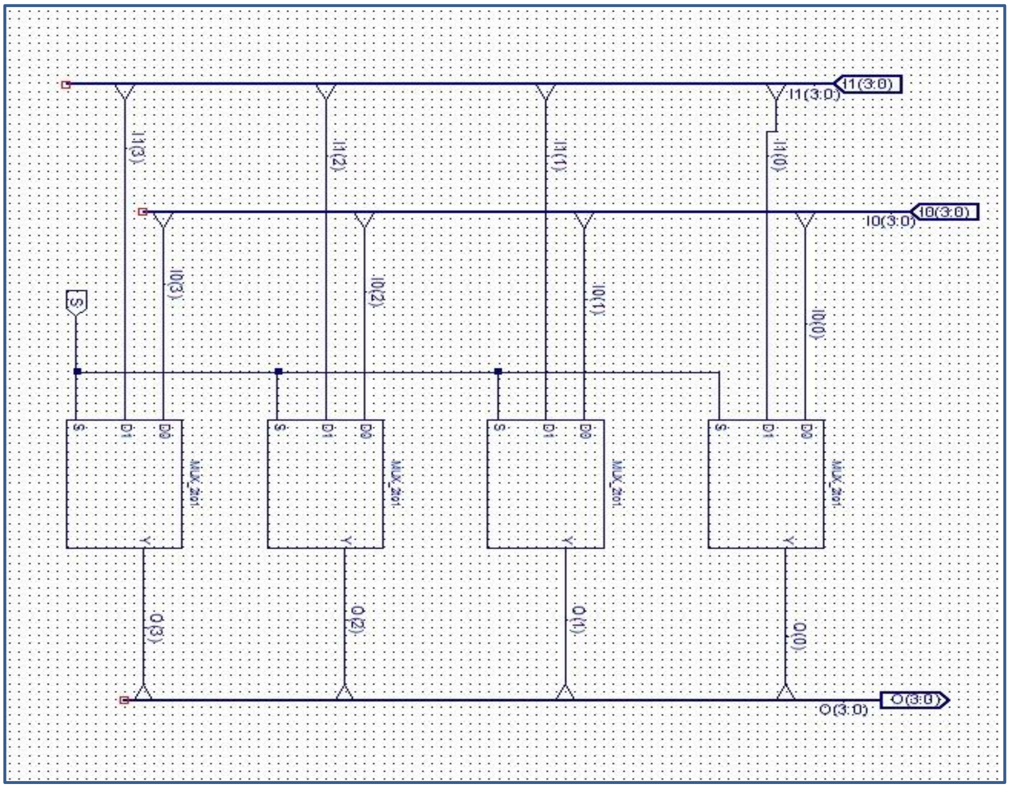
- **<u>Full</u> <u>Adder:</u>**



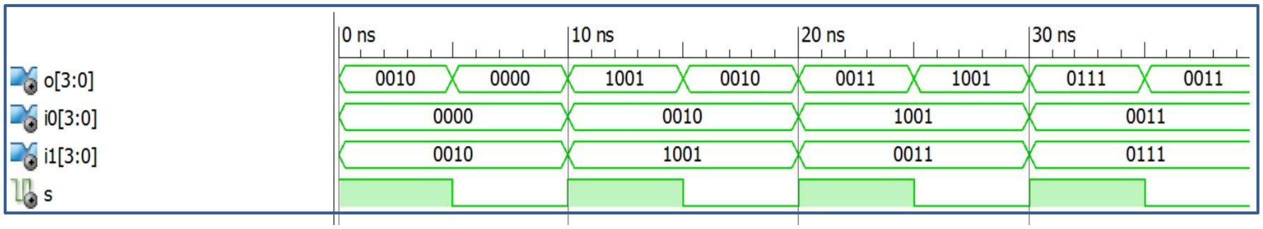
- 2 way- 3 bit Mux:



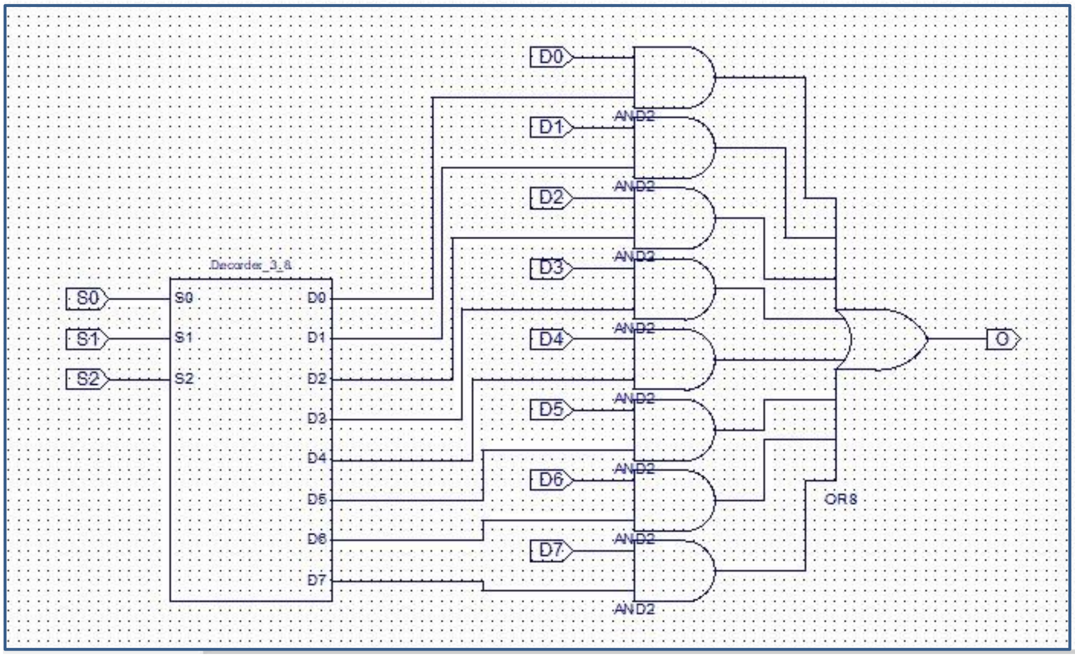
- 2 way_4 bit Mux:



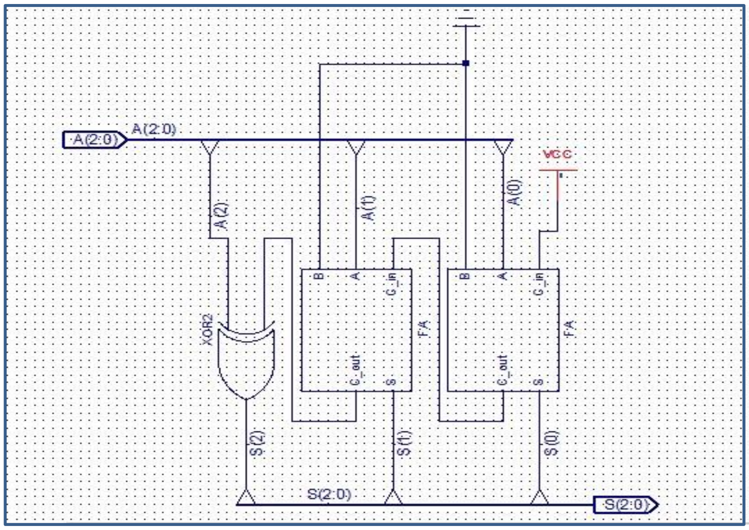
- Timing diagram for 2-way_4 bit Mux is as follows:



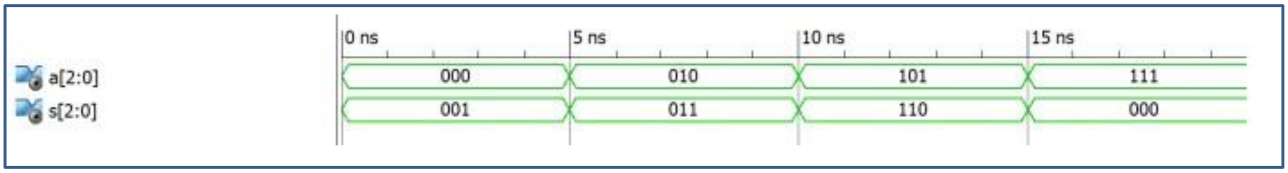
- 8 way_1 bit Mux:



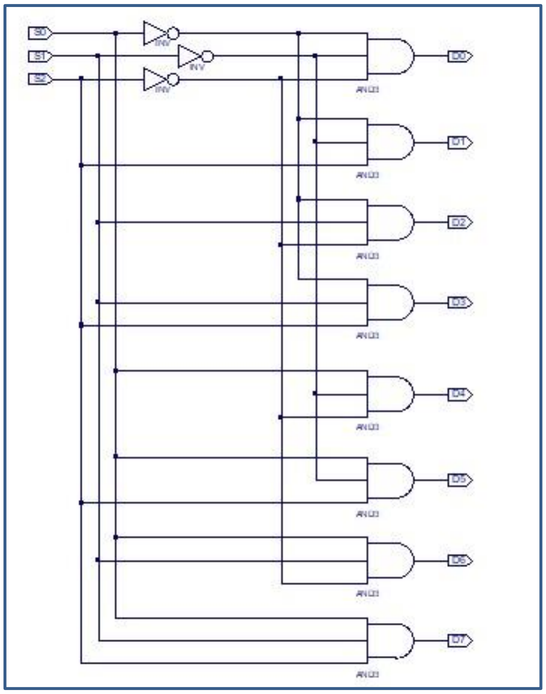
- 3 bit-Adder:



- Timing diagram for 3-bit adder:

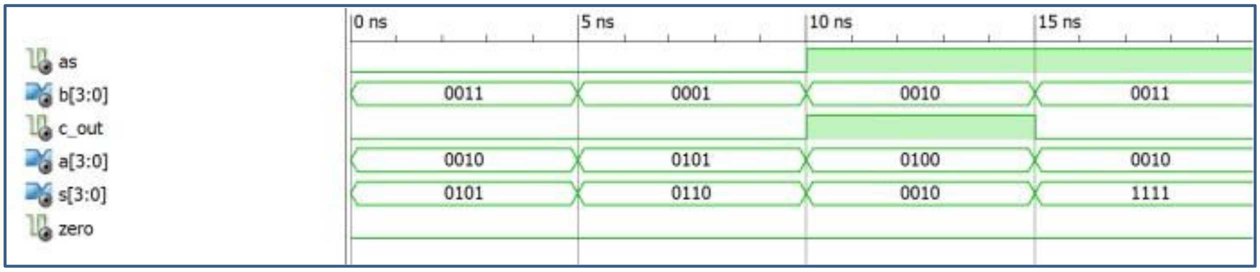


- 3_to_8 decoder:

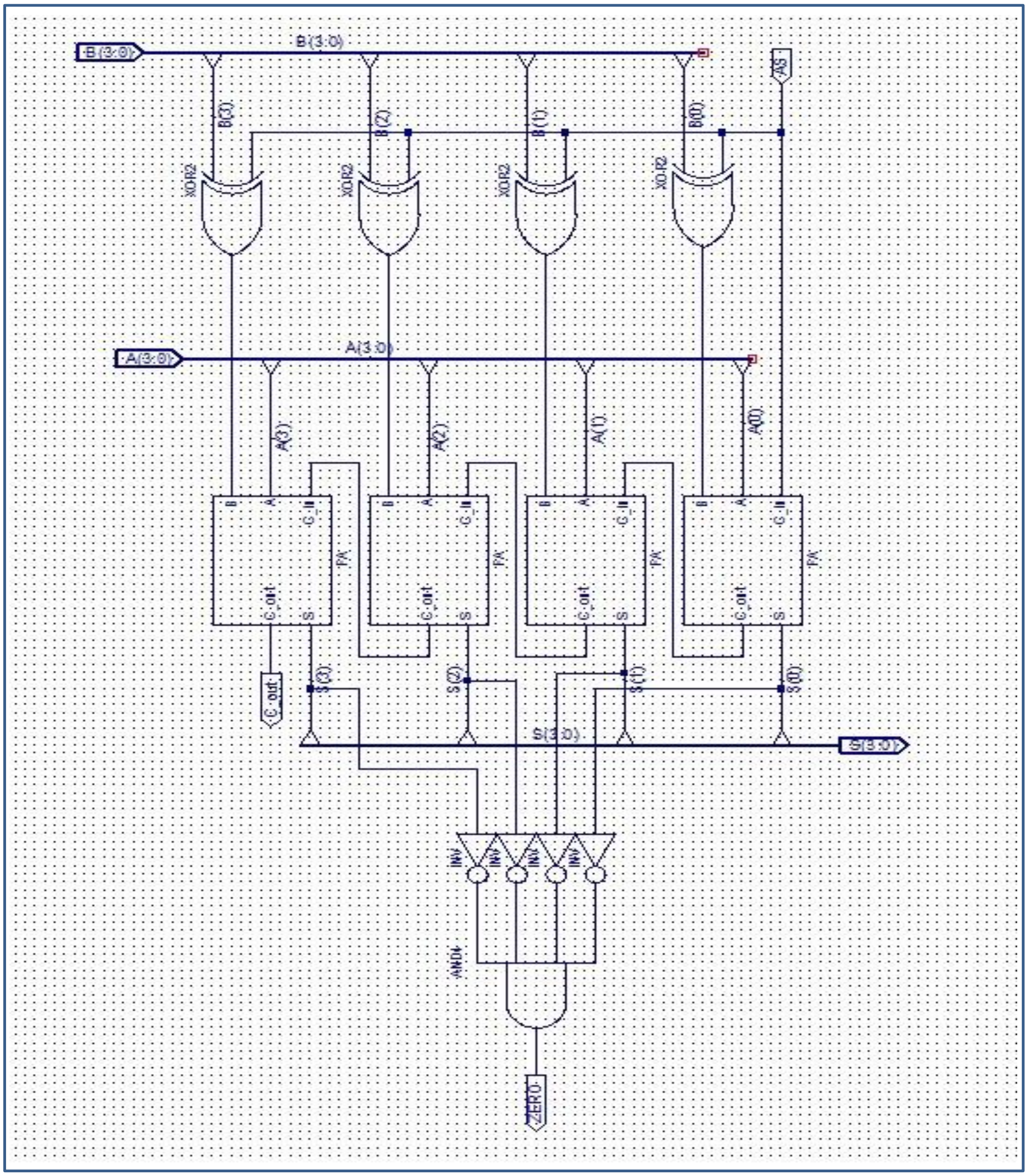


- 4_bit_Add/Sub Unit :

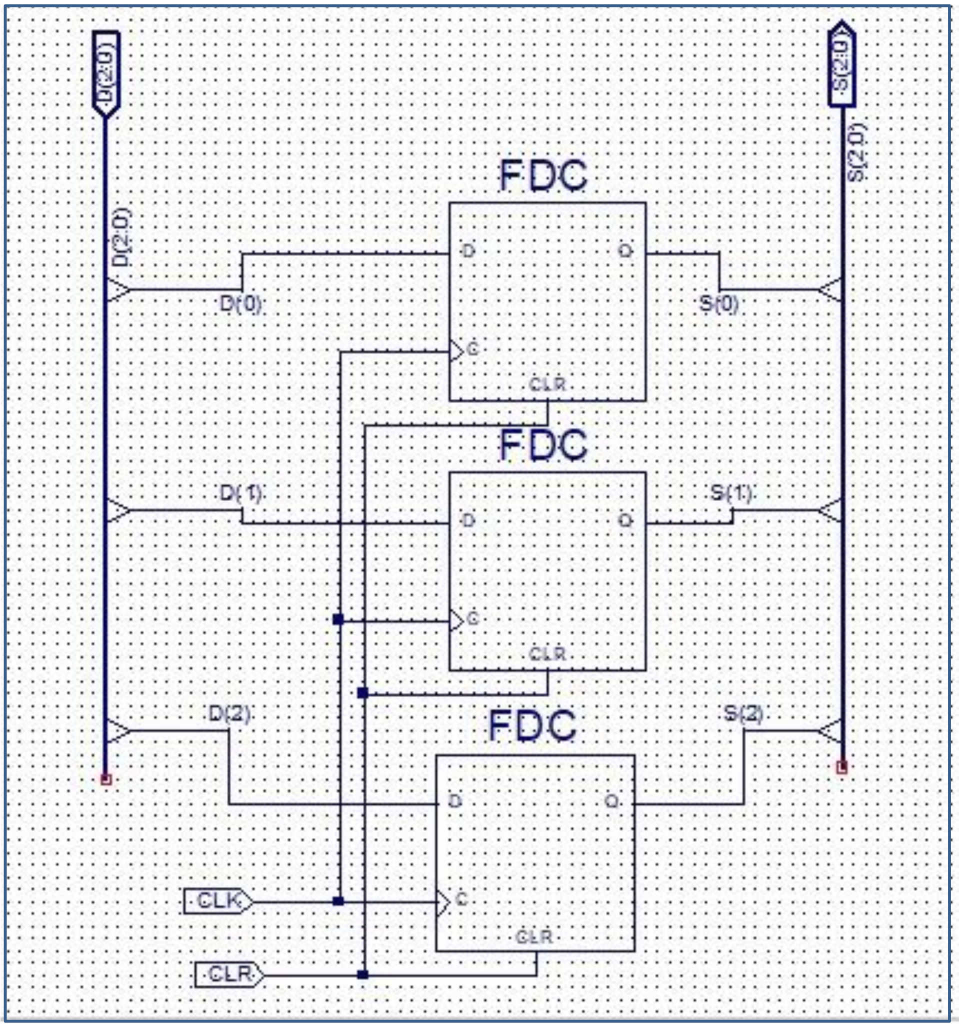
  - ✓ Timing diagram is as follows-



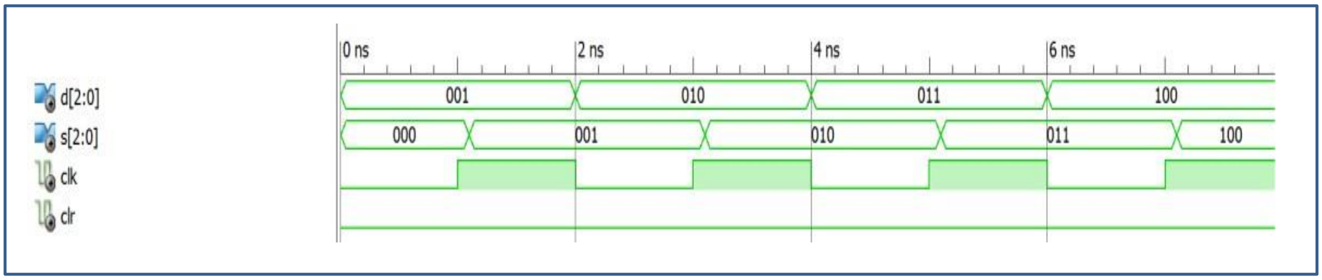
- Schematic of Add/Sub unit:



- **Program counter:**

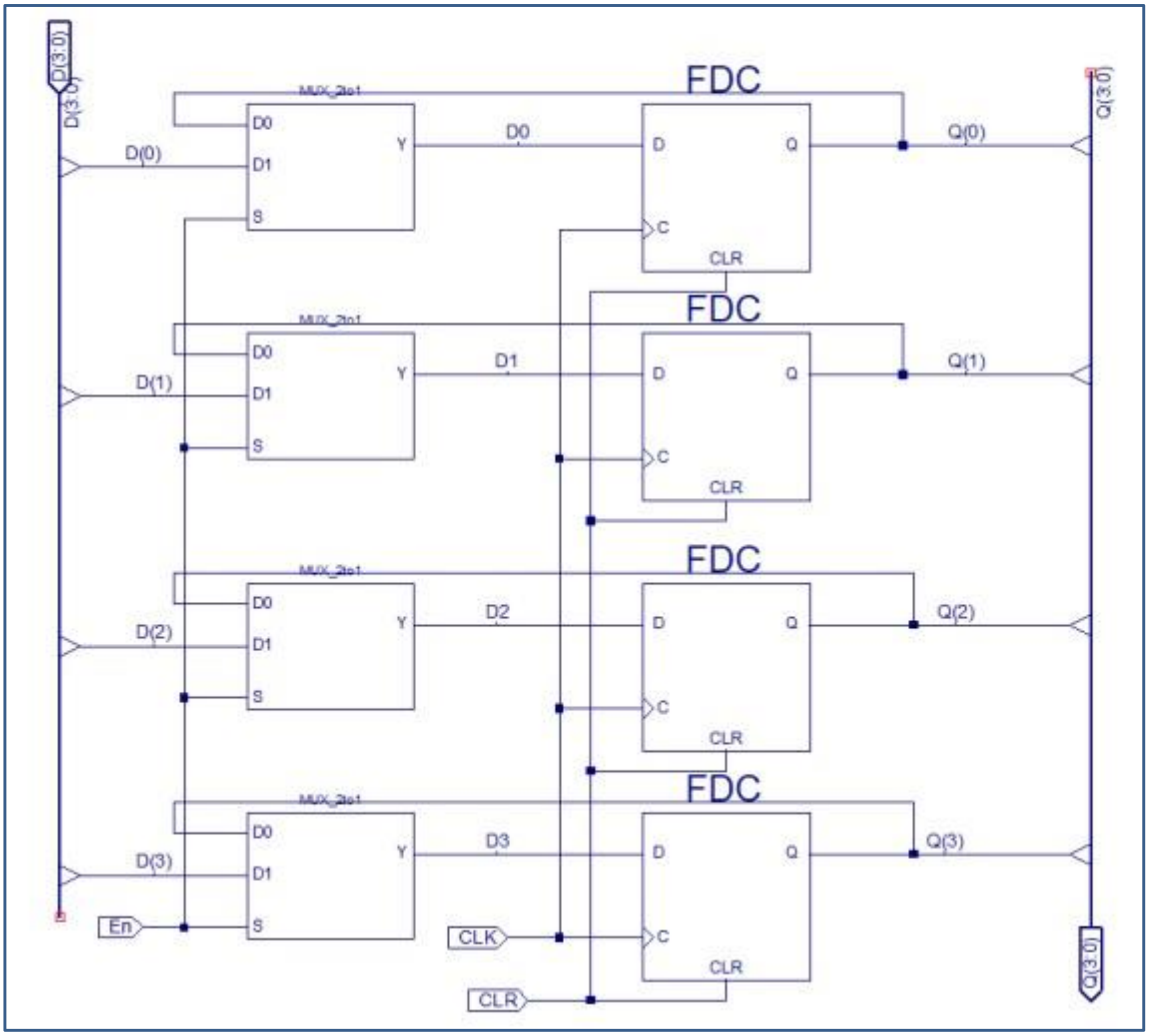


✓ Timing diagram of PC:



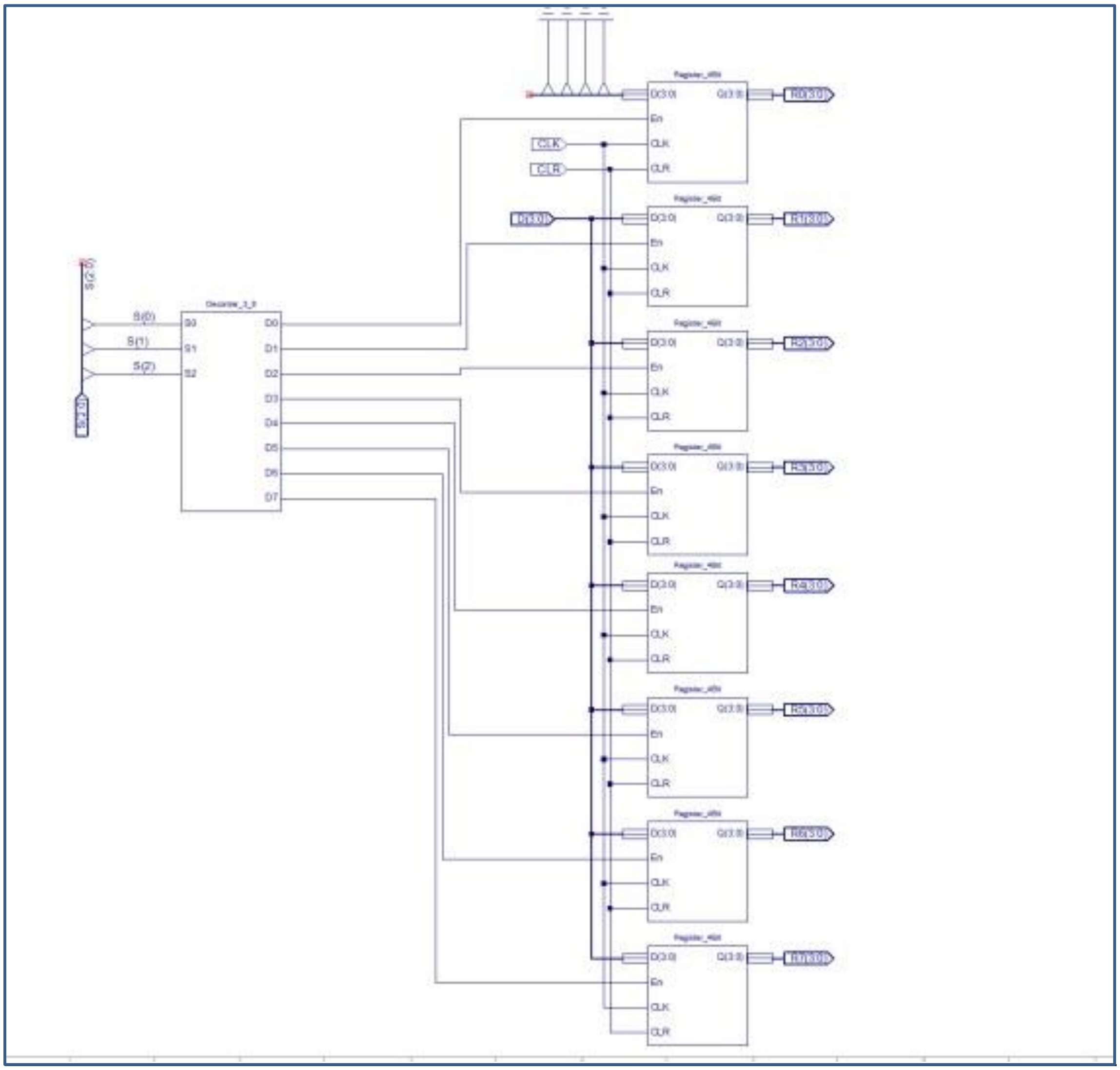
- **Register:**

Since registers store data, we used D flip-flops to make Register.

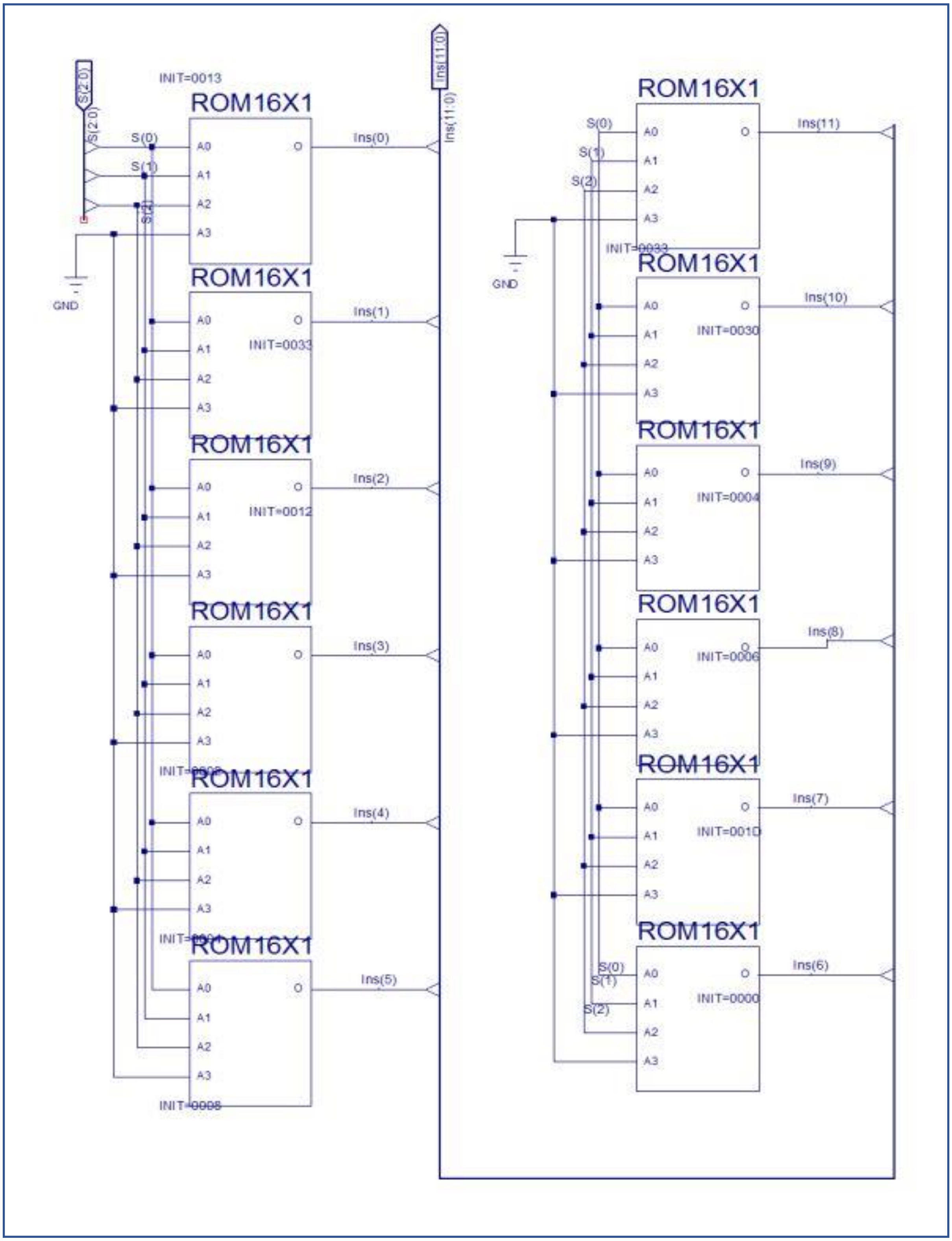


- <u>Register Bank:</u>

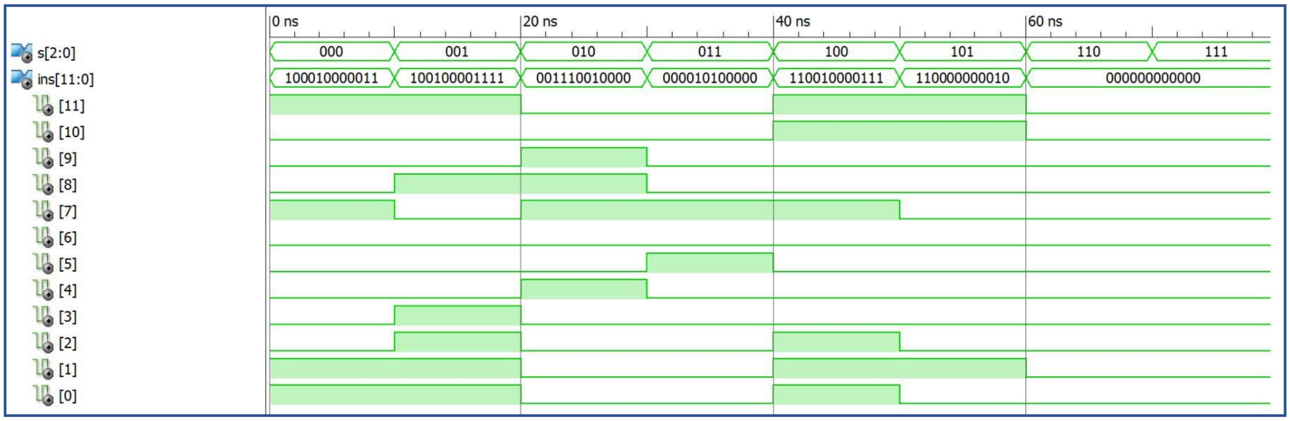
Schematic of Register bank is as follows and we created a symbol of Register bank in the name of



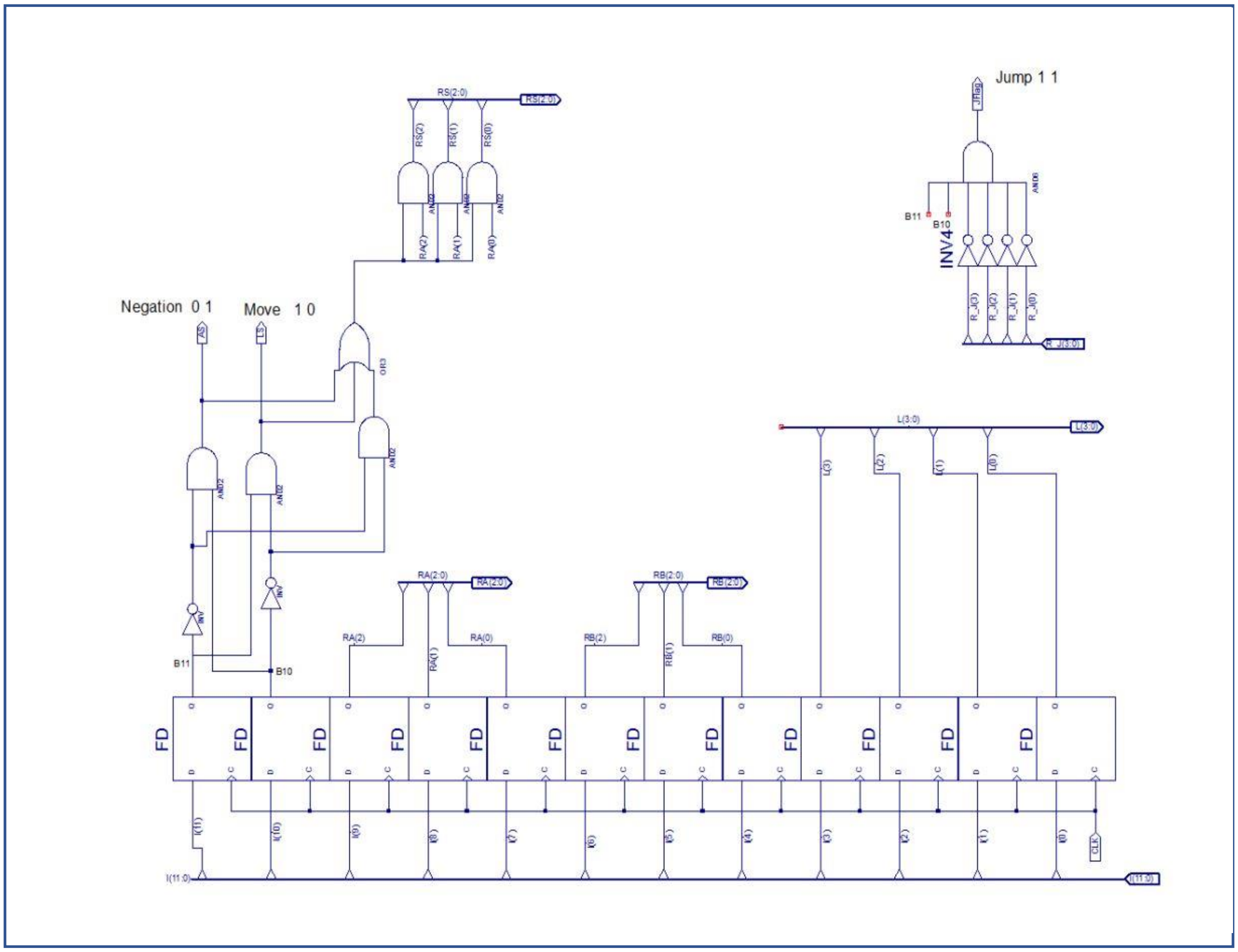
- **Schematic diagram of ROM:**



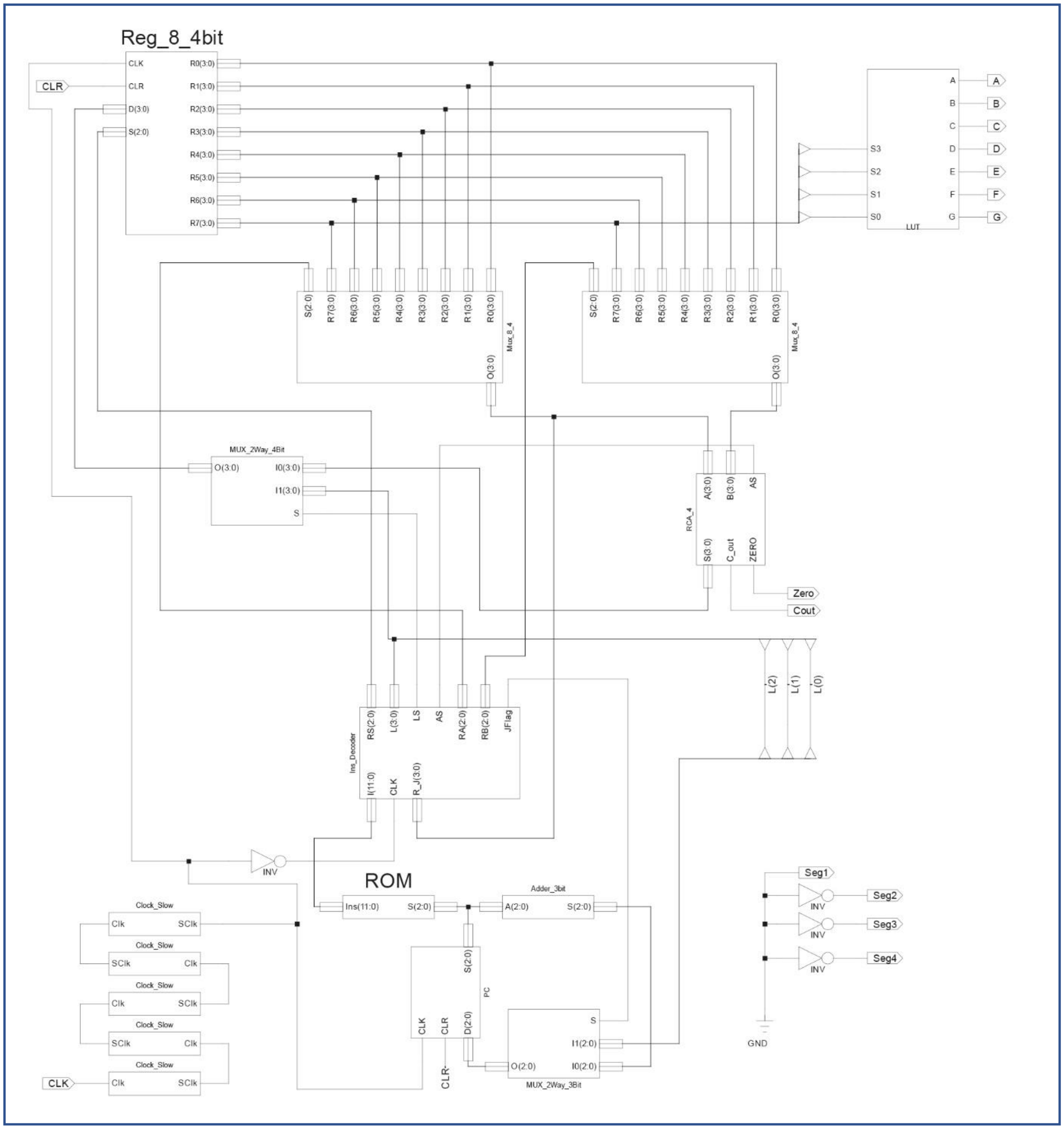
- ✓ Simulation diagram of Rom is as follows:



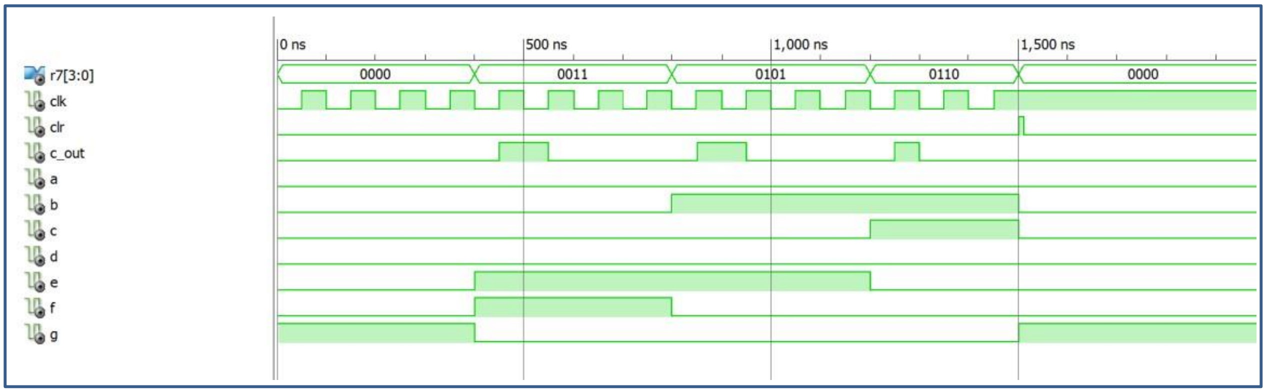
- ➢ Schematic diagram of Instruction decoder is as follows:



- Finally, we merged all the schematic files and made **Nano-Processor**. The following is the schematic diagram of Nano-Processor: -



- Simulation diagram of Nano-Processor is as follows:

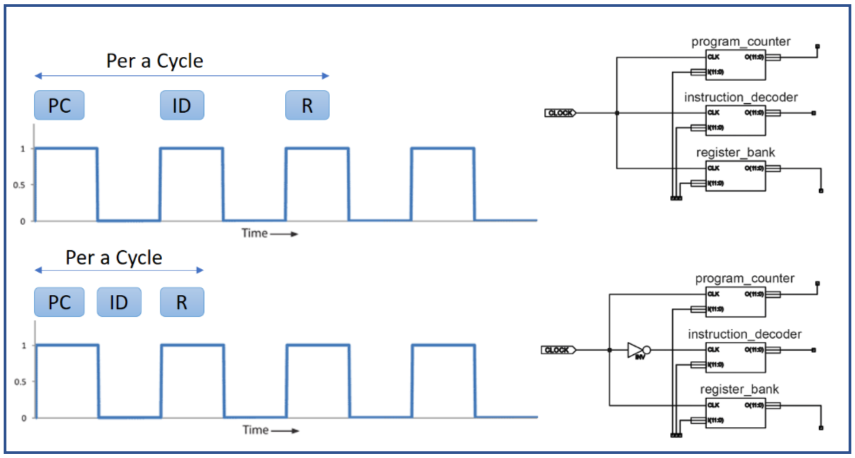


➤ Assembly program and corresponding machine code representation :

	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
MOVI R1, 3	1	0	0	0	1	0	0	0	0	0	1	1
MOVI R2, -1	1	0	0	1	0	0	0	0	1	1	1	1
ADD R7, R1	0	0	1	1	1	0	0	1	0	0	0	0
ADD R1,R2	0	0	0	0	1	0	1	0	0	0	0	0
JZR R1, 111	1	1	0	0	1	0	0	0	0	1	1	1
JZR R0, 010	1	1	0	0	0	0	0	0	0	0	1	0
	0033	0030	0004	0006	001D	0000	0008	0004	0002	0012	0033	0013

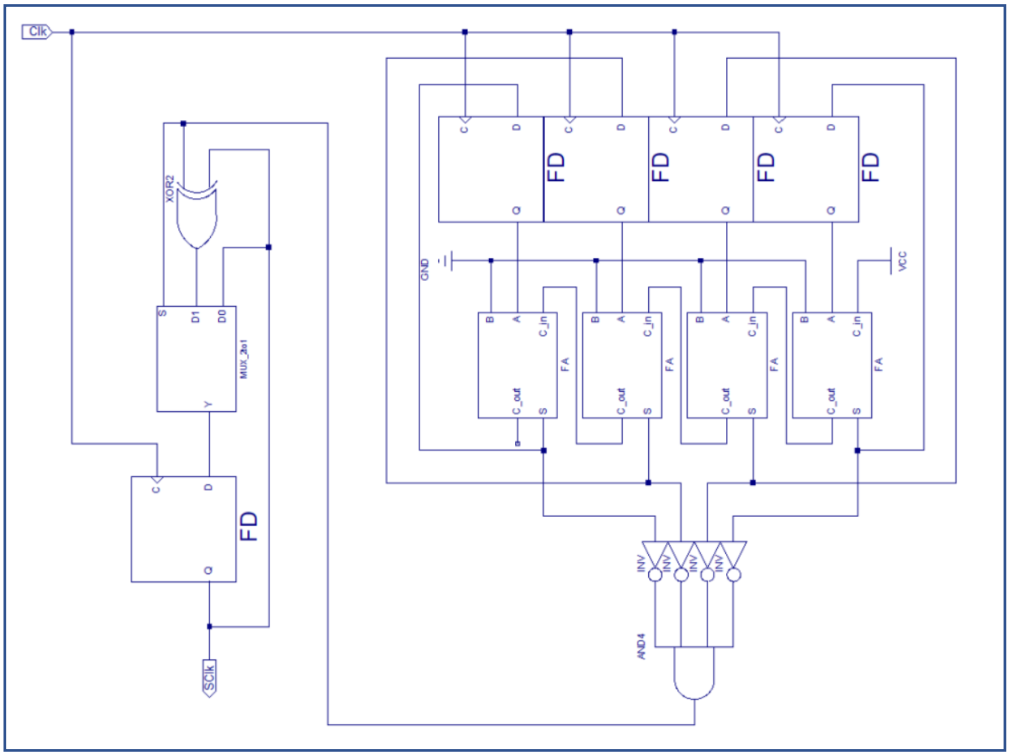
➤ Discussion:

Initially we used the default clock in BASYS which is about 50MHz. But with this clock rate we are unable to demonstrate the changes in the 7-segment display. Hence, we used a 'slowdown' mechanism using RCA and some other logics (especially the D-flip flops). We have slowed down the clock by sixteen times(X16) by a single slow down unit. Here we used 5 such units leading a 2^{20} slow down and managed to get a visible change in seven segment display.



Here in the first diagram, the instructions are executed on the rising edge only. But using a not gate the instructions are managed to be operated on both rising and falling edges as well. This could speed up the rate of instructions as well. Schematic of the 'slow down' unit is given below.

- **Schematic diagram of slow down unit:**



Conclusions from the lab:

- Simple Nano processor can be developed using ISE design suite.
- Hierarchical design is very important design technique to make complex designs.
- Instructions decoders can be developed using basic logic gates and some proper logic.
- Instruction decoders are the vital part of processor design.
- Instruction decoders are the one which decode the machine code and activate necessary components to execute the instruction.
- The amount of data can be handle by a processor is determined by register size.
- Much instructions can be fetched into processor by increasing instruction memory.
- Instruction execution can be speed up by activating them on both edges of a pulse.
- The action of program counter, the loading of instructions from ROM, decoding and activating necessary registers to load values, performing add/sub function and reloading them to registers have been studied and practical experience on how they work have been gained.

✓ Team Coordination:

Index number	Works Assigned	Time taken
160544C	Register, Instruction Decoder, Final Assembling, slow_down mechanism	6 hours
160400H	Program Counter, ROM, Register bank Worked on Look-up table, Final Assembling	5 hours
160658E	Basic Adders, All Multiplexers, Add/Sub unit, Worked on Look-up table, Final Assembling	5 hours