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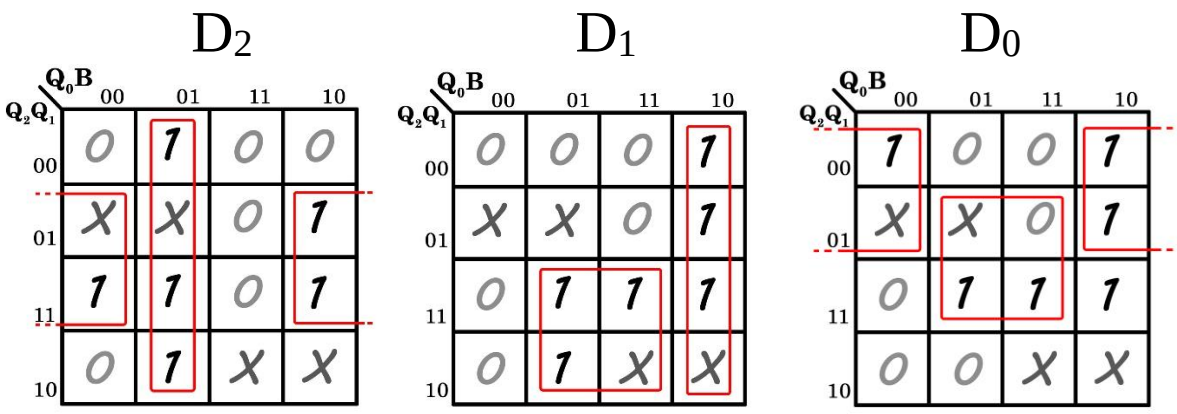
REPORT ON LAB 5
COUNTER WITH EXTERNAL INPUT

Lab Task:

- Completing the truth table for the given three bit counter by using the excitation table of a D flip flop.
- Using Karnaugh Maps to simplify the expressions for inputs D0, D1 and D2.
- Building the 3-bit counter using D Flip Flops and other logic gates.
- Verify the functionality of the counter using simulator and also using the BASYS2 board.

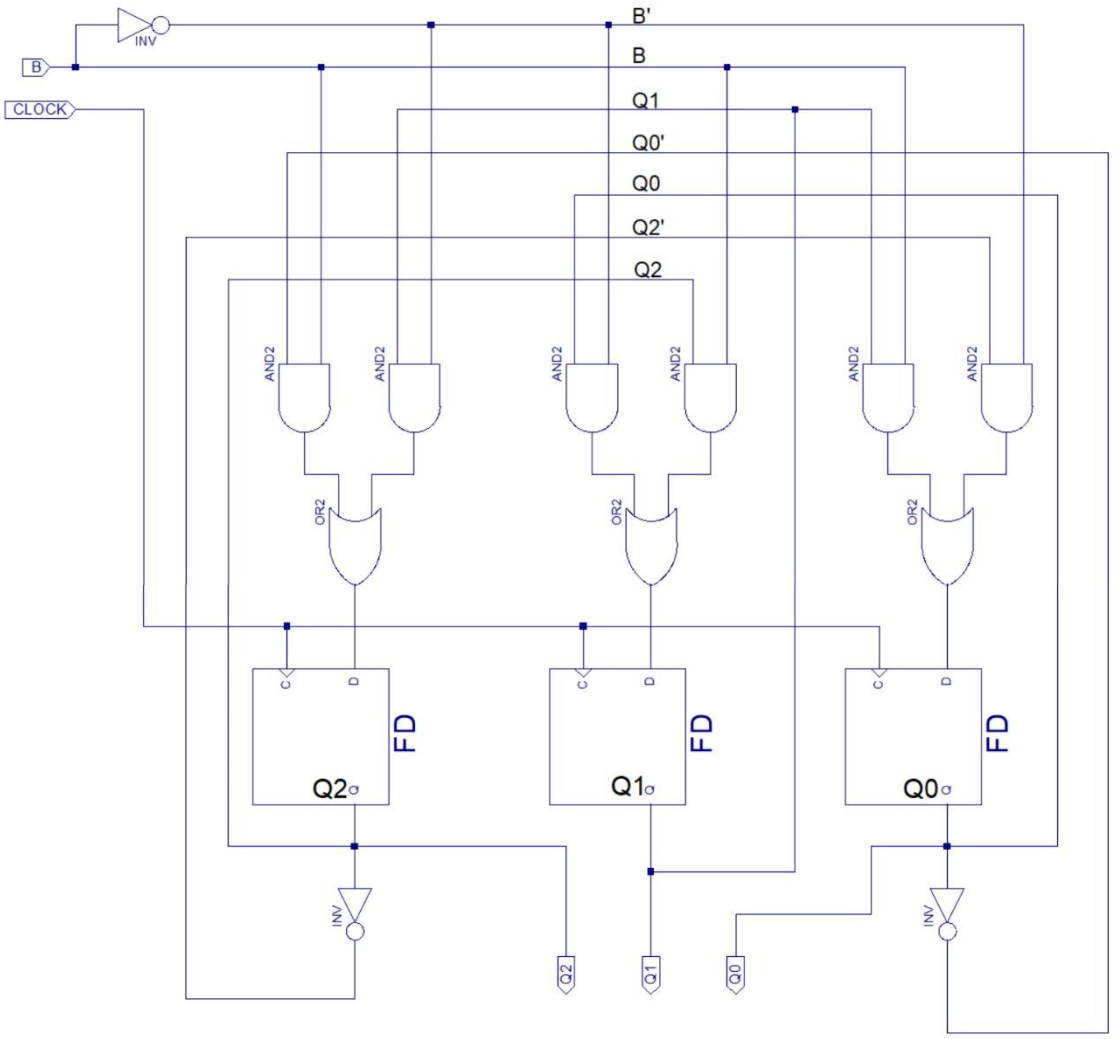
Q_t			B	Q_{t+1}			D_2	D_1	D_0
Q_2	Q_1	Q_0		Q_2	Q_1	Q_0			
0	0	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0	0	0
0	1	1	0	1	1	1	1	1	1
0	1	1	1	0	0	1	0	0	1
1	1	1	0	1	1	0	1	1	0
1	1	1	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0
1	1	0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	1	0

Karnaugh Maps:



$D_2 = \overline{Q_0}\,B + Q_1\,\bar{B}$ $\quad D_1 = Q_0\,\bar{B} + Q_2\,B$ $\quad D_0 = Q_1\,B + \overline{Q_2}\,\bar{B}$

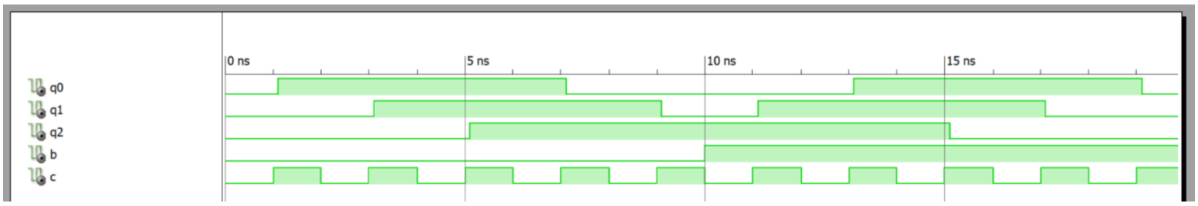
Schematic Circuit diagram:



```vhdl
-- *** Test Bench - User Defined Section ***
   tb : PROCESS
   BEGIN
        B<='0';
        CLOCK<='0';
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
```

```vhdl
        B<='1';
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
        WAIT FOR 1 ns;
        CLOCK<= NOT CLOCK;
      WAIT; -- will wit forever
   END PROCESS;
-- *** End Test Bench - User Defined Section ***
END;
```

Timing diagram:



Discussion:

The push button is not suitable to be used as the clock signal because of the bouncing problem in push buttons. Sometimes, when the push button is pressed, due to the bouncing problem the counter will be incremented many times when the push button is pressed. A proper de-bouncing circuit is required if we must use a push button without any errors (bouncing problem).

Conclusion:

After completing the lab, I can,

- Design and develop a 3-bit counter
- Count in clockwise and anti-clockwise directions based on an external input.
- Verify the functionality of it via simulation and on the development board.