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# REPORT ON LAB 2

## BEHAVIORAL SIMULATION

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### Assigned Lab Task

- ◆ Simplify the Boolean function that can find the prime numbers between 0 and 15.
- ◆ Build a logic circuit for that.
- ◆ Generate a project in Xilinx ISE Design Suite for the circuit.
- ◆ Assign various input combinations to check it.
- ◆ Use BASYS2 to verify the functionality of it.

### Simplifying the Boolean expression

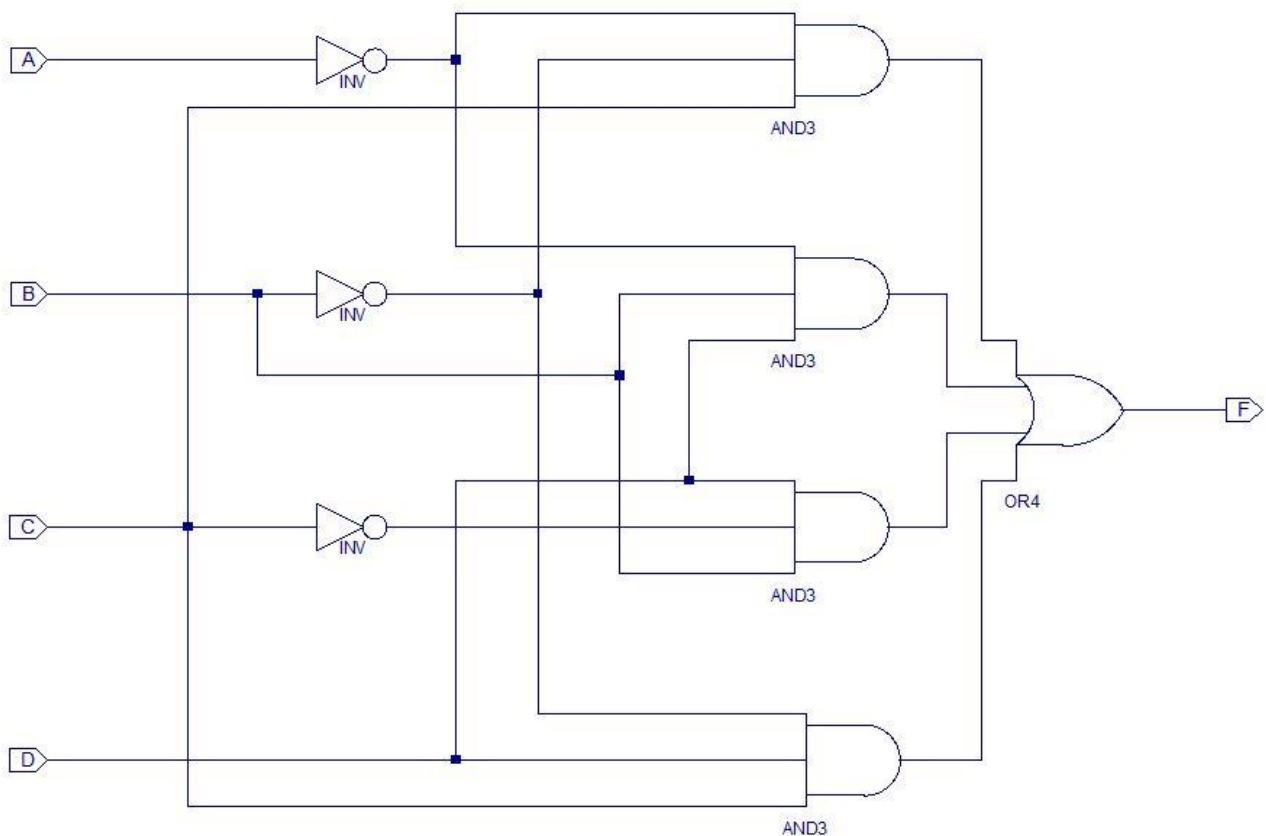
$$F(A, B, C) = \sum (2, 3, 5, 7, 11, 13)$$

### Karnaugh Map

AB \ CD	CD			
	00	01	11	10
00	00 0	01 0	03 1	02 1
01	04 0	05 1	07 1	06 0
11	12 0	13 1	15 0	14 0
10	08 0	09 0	11 1	10 0

$$F = \bar{A}\bar{B}D + \bar{A}BC + \bar{B}CD + B\bar{C}D$$

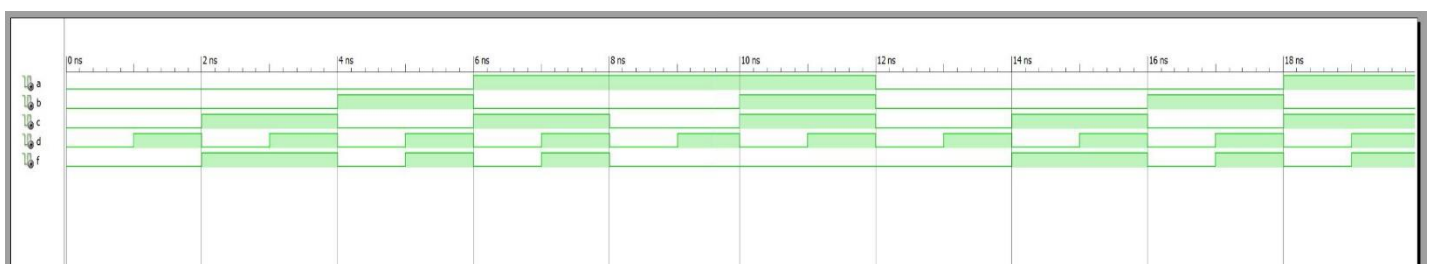
### Schematic circuit diagram from ISE



### Test Bench code having all possible inputs and outputs

```
35  -- *** Test Bench - User Defined Section ***
36  tb : PROCESS
37  BEGIN
38      -- Make sure to set initial values for A, B, C, & D
39      A <= '0';
40      B <= '0';
41      C <= '0';
42      D <= '0';
43      -- Repeat signals to form waveforms
44      ABC_loop: LOOP
45          WAIT FOR 1 ns;
46          D <= NOT D; -- invert D
47          WAIT FOR 1 ns;
48          D <= NOT D;
49          C <= NOT C;
50          WAIT FOR 1 ns;
51          D <= NOT D;
52          WAIT FOR 1 ns;
53          D <= NOT D;
54          C <= NOT C;
55          B <= NOT B;
56          WAIT FOR 1 ns;
57          D <= NOT D;
58      -- fill the rest to get proper sequence
59          WAIT FOR 1 ns;
60          D <= NOT D;
61          C <= NOT C;
62          B <= NOT B;
63          A <= NOT A;
64      END LOOP ABC_loop;
65      WAIT; -- will wait forever
66  END PROCESS;
67  -- *** End Test Bench - User Defined Section ***
68  END;
```

### Timing Diagram from ISim showing all possible inputs and outputs



### Conclusion

At the end of this lab, I was able to design and develop simple logic circuit using schematics and was able to verify the functionality of those circuits through simulation and verify its functionality on the development board.