

Reduced Stage Off-Grid and Buck-Boost Inverter Based Grid Connected Solar Photovoltaic Systems

Submitted in partial fulfillment of the requirements

of the degree of

Doctor of Philosophy

by

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This thesis is **dedicated to**.....

My **Mom and Dad** for their endless patient, support, love and blessings,

My elder brother, Dibakar Debnath, for being the supportive pillar, and for assuring me that someone is there to take care if things do not go well,

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Thesis Approval for Doctor of Philosophy

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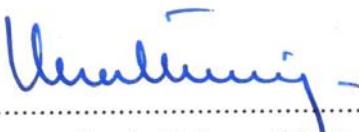
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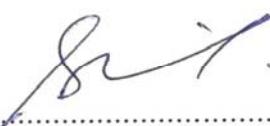
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Declaration

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Abstract

Electricity generation from renewable energy sources (RES) has gained immense interest amongst researchers in recent years owing to the concern over several factors such as global warming, climate change, dwindling reserve of fossil fuels, ever increasing energy demand, etc. Amongst available RES, solar photovoltaic (PV) is being considered as one of the most promising candidate as it is green, inexhaustible, available in abundance, suitable for small-scale and isolated applications, and there is a trend in reduction of price of solar panels. To ramp up power generation from solar energy, the ministry of new and renewable energy (MNRE), government of India, has launched the Jawaharlal Nehru National Solar Mission (JNNSM) in January, 2010. The target of JNNSM is to deploy 20 GW grid connected and 2 GW off-grid solar power by the year 2022. To facilitate the postulates of JNNSM, this thesis attempts to develop improved power electronic based solutions for evacuation of power from solar PV based stand alone and grid connected systems.

Large number of households in India, especially in the rural areas, do not have access to electricity. The solar PV based stand alone schemes are being realized as one of the most promising solution for electrification in these areas. However, the existing PV based stand alone schemes reported in the literature have one or more of the following drawbacks: (a) requirement of higher voltage level for the PV array and the battery, (b) necessity of larger number of power conversion stages, and (c) usage of a low frequency transformer to achieve voltage boosting. In order to address these issues, this thesis proposes two schemes for solar PV based stand alone systems. The first scheme is a three stage configuration which is realized based on a new boost type inverter. This inverter operates as a combination of buck-boost dc-dc converter and a full bridge dc-ac inverter. The salient features of the proposed inverter as compared to existing boost inverter topologies are: (a) minimum possible requirement in the number of semiconductor devices, (b) minimum requirement for passive elements, (c) reduced voltage stress across dc link capacitor, and (d) reduced voltage gain requirement from the equivalent dc-dc buck-boost converter incorporated inside the inverter. The inclusion of the proposed inverter has led to development of a three stage stand alone scheme which requires only seven controllable switches. The scheme also allows the use of low voltage levels for the PV array and the battery thereby eliminating concerns pertaining to the use of high voltage levels for them. The control structure of the overall stand alone scheme is presented and the overall scheme is validated through detailed simulation studies. The efficacy of the scheme is ascertained by performing exhaustive experimental validation on a laboratory prototype developed for the purpose.

The second scheme suggested for stand alone system is a two stage configuration comprising of a high frequency transformer coupled dual-input dc-dc converter (TCDIC) feeding a standard full bridge dc-ac inverter. The input of the proposed TCDIC is formed by connecting the PV array in series with the battery thereby incorporating an inherent boosting stage for the scheme. The boosting capability of TCDIC is further enhanced by incorporating a high frequency step up transformer. In addition to the boosting operation, the TCDIC can also perform maximum power point tracking (MPPT) and battery charge control. Hence all of the facilities that are achieved in the existing stand alone schemes by involving two or more stages of dc-dc converters, can be obtained by employing the proposed single stage TCDIC. A suitable control strategy for the TCDIC is devised. The effectiveness of the overall stand alone scheme incorporating the TCDIC has been substantiated by performing detailed simulation as well as experimental studies.

In order to achieve the ambitious target of JNNSM to deploy 20 GW grid connected solar power by the year 2022, the decentralized grid connected systems are seen as a promising candidate. These decentralized schemes are typically designed for low power ratings (<5 kW) and a single phase inverter is employed to form the interfacing link between the PV array and the distribution grid. Though several converter topologies exist for realizing single-phase grid connected inverter, the transformerless inverter topologies have become popular due to their advantages such as low weight, less volume, high efficiency, low cost, etc. However, the existing transformerless inverter schemes have one or more of the following drawbacks: (a) requirement of high voltage level for the PV array owing to buck nature of the inverter, (b) inability to support wide variation in PV array voltage, (c) inability to ensure flow of leakage current within permissible limit, (d) not tolerant to shoot through fault problem, (e) requirement of an additional dc-dc converter, and (f) requirement of two separate PV arrays to be operated at the same conditions. In order to address the aforementioned issues, this thesis proposes a multi-purpose transformer-less decentralized grid connected inverter scheme for solar PV applications. This inverter is based on neutral point clamped inverter structure and has the voltage buck-boost capability. It can be utilized to extract maximum power from a single as well as two separate PV arrays. While extracting maximum power from a single PV array the same converter can be utilized to negotiate local dc loads simultaneously. The aforementioned dc loads can be fed from the PV array and/or the grid. Thus the proposed converter can serve as dc to ac inverter (PV to grid), dc to dc converter (PV to dc load), and ac to dc converter (grid to dc load). The control strategies devised for the aforementioned applications of the proposed scheme is presented. The effectiveness of the proposed scheme for all of the aforementioned applications have been ascertained through detailed simulation studies. A laboratory prototype for the scheme is developed and experimental validation is carried out for the scheme when it is employed to extract maximum power from single as well as two separate PV arrays.

The schemes discussed so far in this abstract deals with low power systems, and hence, can be designed with low voltage level for the PV arrays. As the power level of the system increases, the PV voltage level is also increased by connecting several PV modules in series to form a PV string in order to reduce losses in the system. However, solar PV strings

formed by series combination of several PV modules suffer from considerable reduction in power yield when subjected to mismatched operating conditions. In order to address this issue several schemes have been reported in the literature. Amongst these schemes, the compensating power-dedicated dc-dc converter based distributed maximum power point tracking (CPDC-DMPPT) schemes seem to be the most promising ones. However, the existing CPDC-DMPPT schemes reported in the literature have one or more of the following limitations: (a) employment of voltage equalization based scheme which cannot ensure maximum power extraction from each of the serially connected PV module, (b) requirement of sensing of temperature and insolation level, (c) necessity of large number of sensors, (d) requirement of communication between local dc-dc converters, (e) incapability for realizing schemes having considerable numbers of series connected PV modules, and (f) requirement of high-end processor to realize computation-intensive algorithm. In order to address the aforementioned issues a simple CPDC-DMPPT scheme is proposed in this thesis. The main advantages of this scheme are: (a) reduced burden on the processor as only one conventional MPPT algorithm is required to be executed, (b) elimination of communication requirement between local dc-dc converters leading to improved reliability and reduction in cost, (c) elimination of requirement of module level power measurement leading to reduction in current sensor requirement, and (d) simple implementation. The implementation issues and the control philosophy of the proposed scheme are discussed utilizing the power circuit configuration of the existing flyback-converter based standard DMPPT scheme. The efficacy of the scheme is ascertained through detailed simulated performance. The experimental validation of the scheme is carried out on a scaled down laboratory prototype developed.

Keywords: boost inverter, distributed maximum power point tracking (DMPPT), grid connected inverter, maximum power point tracking (MPPT), Solar photovoltaic (PV), stand alone/off-grid system, transformerless inverter.

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List of Symbols

C	: Capacitance, F
C_{PV}	: Capacitor connected across PV array, F
C_{pv1}	: Parasitic capacitances of PV panel, F
C_{pv2}	: Parasitic capacitances of PV panel, F
D	: Semiconductor diode
d	: duty ratio of a switch
f_c	: Cut-off frequency of filter, Hz
f_g	: Frequency of grid voltage, Hz
F_s	: Switching frequency of semiconductor switch, Hz
i	: Integers
i_{bmax}	: Maximum charging current limit of the battery, A
i_{bmin}	: discharging current limit of battery, A
i_{bmax}	: maximum charging current limit of battery, A
I_{CMT}	: Common-mode current, A
I_{FBin_i}	: Input current to i^{th} flyback converter, A
I_{FBout_i}	: Balancing current supplied by the i^{th} flyback converter, A
i_g	: current being injected in to the grid, A
I_{mpp}	: Current of a PV module at its maximum power point, A
$I_{mpstring}$: Current flowing through a PV string, A
INC	: Incremental Conductance MPPT algorithm
i_{pri}	: Current flowing through primary winding of a transformer , A
I_{SC}	: Short-circuit current of a PV module, A
i_{sec}	: Current flowing through secondary winding of a transformer , A
ΔI_x	: Current ripple in x , A (peak-to-peak/2)
j	: Integers
K_i	: Integral gain of a Proportional Integral(PI) controller
K_p	: Proportional gain of a Proportional Integral(PI) controller
L	: Inductance, H
L_A	: Filter inductors at the inverter output, H
L_B	: Filter inductors at the inverter output, H
M	: Modulation index
N	: Numbers of series connected PV module in a PV string
n	: Turns ratio of transformer
N_x	: Number of element x

P_b	: Battery power, W
p_{bmax}	: Maximum power that can be absorbed by a battery without being over charged, W
p_L	: Sum of p_{load} and p_{loss} , W
p_{load}	: Load power demand, W
p_{loss}	: Loss in the system, W
p_{mpp}	: Maximum available PV power, W
$P\&O$: Perturb and Observe MPPT algorithm
P_{outFB_i}	: Power at the output end of i^{th} flyback converters, W
p_{pv}	: Power extracted from PV array, W
R	: Resistance, Ω
S_i	: Controllable Semiconductor Switch i
T_s	: Switching time period of semiconductor switch, s
v_b	: Voltage across battery, V
V_{CMT}	: Total common mode voltage , V
V_{CM}	: Common-mode voltage when differential mode voltage is zero, V
V_{DM}	: differential mode voltage, V
v_g	: Grid voltage, V
V_{mpp}	: Voltage of a PV module at its maximum power point, V
V_{oc}	: Open circuit Voltage of a PV module, V
V_{pv_ref}	: Reference voltage command of a PV module, V
v_{pri}	: Voltage across primary of a transformer respectively, V
v_{sec}	: Voltage across secondary of a transformer respectively, V
V_{string_ref}	: Reference voltage command of a PV string, V
Δv_x	: Voltage ripple in x , V (peak-to-peak/2)
\bar{x}	: Average value of variable x over a switching cycle
X	: Steady state value of variable x
\hat{x}	: Small signal perturbation of x around its steady state value X
$ X $: Absolute value of variable x
Z	: Impedance, Ω
η	: Efficiency

Chapter 1

Introduction and Literature Survey

1.1 Motivation

Electricity has been recognized as an essential requirement of human life. The socio-economic development of a country has a strong dependency on the level of consumption of electrical energy. Unfortunately, over 300 million Indian citizens have no access to electricity and majority of these population reside in rural areas [1]-[2]. However, considering the large gap between supply and demand of electrical energy so far as India is concerned, there is an urgent need to significantly enhance the present capacity of generation and distribution of electricity. Electricity generation in India is mainly based on fossil fuels. Hence significant emissions of green house gases will be experienced due to the aforementioned capacity addition and this will impact impact on climate and health related issues. Further, these fossil fuel reserves are going to be depleted in near future and as a consequence their price is continuously increasing. The aforementioned aspects have increased the attention towards electricity production from renewable energy sources (RES). Over the years, the solar PV has evolved as one of the most promising candidates amongst the available RES. It is gaining popularity due to the following reasons: (a) available in abundance, (b) continuous reduction in the price of solar PV modules, (c) inexhaustibility, (d) suitable for small-scale and isolated application, (e) cleaner and quieter operation, (f) intense research activities are being pursued to reduce cost and to increase efficiency of the power electronic converters required for evacuation of solar power, and (g) governmental subsidies and incentives [3]-[5].

To ramp up power generation from solar energy, the ministry of new and renewable energy (MNRE), government of India, has launched the Jawaharlal Nehru National Solar Mission (JNNSM) in January 2010. This mission is one of the eight missions of India's National Action Plan on Climate Change [6]. The target of JNNSM is to deploy 20 GW grid connected solar power by the year 2022. The initial focus of the grid connected schemes was directed towards large MW-scale centralized power plants only. However, the prospect of decentralized small and medium power level schemes has grown significantly in recent years owing to their several advantages such as, (a) possibility of placement near load centres thereby reducing transmission and distribution losses, (b) better utilization of space as compared to centralized schemes, (c) better power extraction owing to decentralized maximum power point tracking capability, (d) economic viability especially for private owners. These decentralized schemes feed solar power to the low tension distribution grid through suitable power electronic interface. However, the grid is not available

to about 30% of the rural population of India. The off-grid or stand alone schemes are a promising solution for electrification in these sectors. To address the problem in rural electrification, JNNSM has set up a target of 2 GW off-grid solar systems by the year 2022.

The targets set by JNNSM are ambitious both for grid-connected as well as for off-grid systems. In order to achieve these targets focussed efforts are to be made giving due considerations to all the key aspects pertaining to the issue. The various aspects to be considered are innovative technical solutions, policy framework, financial issues, education and awareness regarding solar power, etc. In this thesis the issue of obtaining innovative technical solutions is considered, and in that an attempt has been made to develop effective power electronic solutions for evacuation of power from solar PV and feed it to grid/off-grid loads in an efficient manner. Specific efforts have been made in this thesis to develop solar PV based stand alone schemes as well as decentralized grid-connected systems. All the schemes proposed in this thesis have been validated through detailed simulation as well as experimental studies.

1.2 Solar PV Based Stand Alone/Off-grid Systems for Rural Deployment

Large number of households in India, especially in the rural areas, do not have access to electricity as extension of grid is not economically viable in those areas. This is considered as one of the major barrier to the overall economic growth of the country. To address this issue several initiatives are being considered to improve the scenario of rural electrification. Majority of these schemes are targeted towards deployment of renewable energy source (RES) based stand alone/off-grid system in rural areas. Amongst various RES, solar photovoltaic is being considered as one of the most promising candidate for such applications due to the following reasons: (a) suitability for small-scale and isolated application, (b) real estate required to install PV panels is not a constraint in rural areas, (c) India is blessed with high level of solar insolation, and (d) does not require significant maintenance. The loads for such stand alone system are generally household single-phase appliances having power rating in the range of 250-500 VA.

1.2.1 Major challenges in designing a solar PV based stand alone scheme

Basic block diagram of a typical solar PV based stand alone system along with pertinent voltage levels is shown in Fig. 1.1. As power output from the solar PV is intermittent in nature, stand alone systems require the service of an energy storage element to maintain a balance between the available PV power and the power demand from the load [3]-[5]. The aforementioned energy storage element is usually realized by employing a battery bank. In addition to this, stand alone systems require the service of power electronic converters to form the required interface amongst the PV panel, the battery and the load. This power electronic interface generally consists of one dc-ac converter and two or more

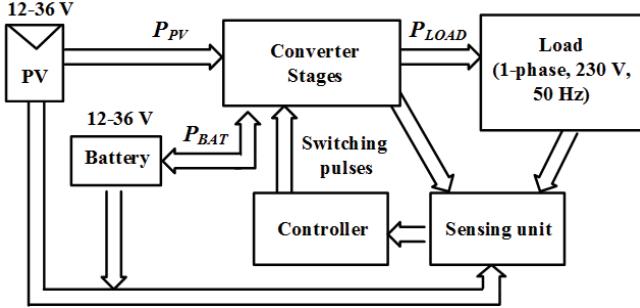


Figure 1.1: Basic structure of a typical stand alone system

dc-dc converters. The dc-ac converter is essential for stand alone schemes as the output power of the solar PV panel and the battery is in dc form whereas the load requires ac power. The service of dc-dc converters is required mainly to achieve maximum power extraction from the PV panel and to protect the battery from overcharge and over discharge. However, some of the stand alone systems also require the service of an additional dc-dc converter to realize voltage boosting. Reason for the requirement of the boost dc-dc converter is provided below.

The voltage level for household ac appliances in India is 230 V. As a result, the dc voltage at the input of the dc-ac converter needs to be maintained at around 360-400 V if a standard full bridge inverter is employed for dc-ac conversion. To obtain such a high dc voltage, higher level(s) of voltage can be chosen for PV panel and battery. However, increment in the PV panel and/or the battery voltage level makes design and installation issues of the system more involved in order to satisfy concerns pertaining to the safety of the personnel and equipment [7]. Further, increment in the PV voltage requires numbers of PV modules to be connected in series which results in considerable reduction in power yield when the serially connected modules experience different operating condition(s). This issue is discussed elaborately in Section 1.4. The voltage level of a battery bank can be increased by connecting standard 12 V batteries in series. However, use of large number of batteries increases cost and size of the system. In view of the aforementioned issues, typical low power stand alone systems generally employ lower voltage level for the PV panel and the battery. The voltage levels for PV panel and the battery are chosen in the range of 12-36 V. This leads to high voltage gain requirement from the power electronic converters. Such a high gain can be achieved by employing a low frequency step-up transformer at the inverter output. But this will increase size, weight and volume of the system. In order to address this issue, the high gain requirement (of the order of 10-15) is generally provided through intermediate dc-dc converters which interface the PV panel and the battery to the dc link of the inverter.

From the above discussions it can be concluded that major challenges in designing a PV based stand alone system with battery as an energy storage element are:

1. Maximum power extraction from the PV panel under variable insolation level, temperature and loading condition.
2. Provision of bidirectional power flow for the battery

3. Dc-ac conversion.
4. Provision for adequate voltage gain as the voltage level(s) for the PV panel and the battery is generally kept low for domestic applications.

In addition to the above mentioned challenges, a stand alone system also requires a suitable control strategy which guides it to operate in different modes of operation that a typical stand alone system encounters. These modes of operation are discussed in the following subsection.

1.2.2 Modes of operation of a stand alone system

Depending on the maximum power available from the PV panel (p_{mpp}), the load power demand (p_{load}), system loss (p_{loss}) and the state of charge (SOC) level of the battery, a stand alone system can operate in one of the following modes:

(a) **MPPT mode:** Maximum power is extracted from the PV panel when the system operates in this mode. However, in order to make operation possible in this mode, one of the following two conditions is to be satisfied: (1) $p_{mpp} > p_L$ and the surplus power can be absorbed by the battery without being over charged, (2) $p_{mpp} < p_L$ and the battery is having the capability to supply $p_L - p_{mpp}$ without getting over discharged, wherein, $p_L = p_{load} + p_{loss}$. The power extracted from the PV panel in MPPT mode is given by, $p_{pv} = p_{mpp} = (p_b + p_L)$, where p_b is the battery power which is defined as positive during charging and negative while discharging.

(b) **Non-MPPT mode:** Based on the SOC level of the battery its charging current is required to be limited to a maximum permissible limit, i_{bmax} to prevent the battery from getting damaged due to overcharge. The maximum charging current limit, i_{bmax} restricts the maximum power that can be absorbed by the battery to, $p_{bmax} = i_{bmax} \times v_b$ wherein v_b is the battery voltage. When $p_{mpp} > p_L$ and the surplus power is more than p_{bmax} , the system cannot be operated in MPPT mode as it would overcharge the battery. During this condition power extraction from PV is deliberately reduced to a value given by, $p_{pv} = (p_{bmax} + p_L)$ thereby operating the system in non-MPPT mode.

(c) **Battery-only (BO) mode:** The system operates in battery-only mode when PV power is not available. In this mode, the battery supplies the entire load demand till it reaches its discharge limit.

(d) **Shutdown mode:** The battery has to discharge when the PV power is less than the load demand. While doing so the battery may reach its discharge limit beyond which it must not be discharged further to avoid the damage of the battery. Therefore once this battery discharge limit is reached the system is made to undergo shutdown by withdrawing the gate pulses from the switches.

General criteria followed for selection of different modes are summarized in Table 1.1.

Table 1.1: Mode selection criterion for a typical stand alone system

Condition	Mode	Remark
i. $p_{mpp} > p_L$ and battery can consume $(p_{mpp} - p_L)$ ii. $p_{mpp} < p_L$ and battery can supply $(p_L - p_{mpp})$	MPPT (MP)	PV power, $p_{pv} = p_{mpp}$, $p_{bat} = p_{mpp} - p_L$
$p_{mpp} > p_L$ and battery cannot consume $(p_{mpp} - p_L)$	non-MPPT (Non-MP)	$p_{bat} = p_{bmax}$, $p_{pv} = (p_L + p_{bmax}) < p_{mpp}$
$p_{mpp} < p_L$ and battery cannot supply $(p_L - p_{mpp})$	Shutdown (SD)	Shutdown the system
$p_{mpp} = 0$ and battery can supply p_L	Battery-only (BO)	$p_{bat} = p_L, p_{pv} = 0$

1.2.3 Literature review of existing stand alone schemes

Several stand alone schemes have been reported in the literature which differ in complexity, effectiveness, component requirement, etc. Some of them have been specifically designed for household dc appliances [8]-[10] having low voltage requirement at the load terminal. Hence the voltage gain requirement from the intermediate converter(s) in these schemes are less. Stand alone systems reported in the literature for feeding ac loads having voltage rating of 230 V and thereby requiring high voltage gain from the intermediate converters can be categorized as follows:

(A) Four stage configuration

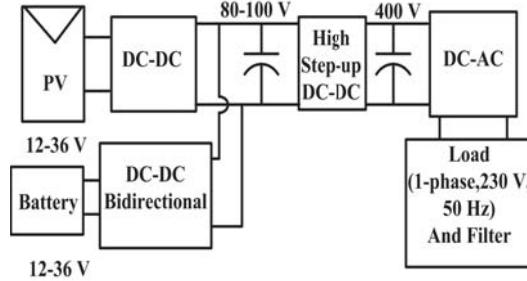


Figure 1.2: Basic structure of a conventional four stage stand alone system

Schematic block diagram of a rudimentary four stage configuration is shown in Fig. 1.2. In this case, three dc-dc converters are generally used [11] in addition to a dc-ac inverter. Out of these three dc-dc converters, one dc-dc converter is used for maximum power point tracking (MPPT); second one is used for battery charge control and the third one is used for voltage boosting. Generally non-isolated dc-dc converters are used for MPP tracking and battery charge control while a transformer coupled dc-dc converter is used to realize voltage boosting.

An alternative approach utilizing a multi-port transformer based scheme is also reported in the literature [12]-[13] and the schematic block diagram of this scheme is shown in Fig. 1.3. Although this configuration is suitable for achieving high boosting gain, it

requires a complicated control scheme for controlling power flow by varying the phase angles of terminal voltages of the transformer windings.

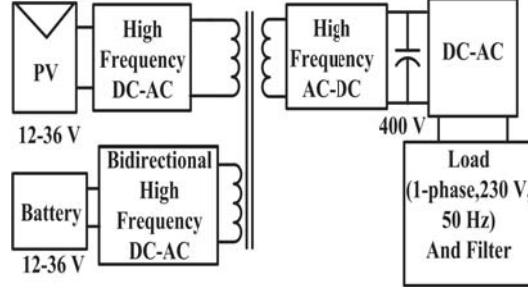


Figure 1.3: Basic structure of a multi-port transformer coupled configuration

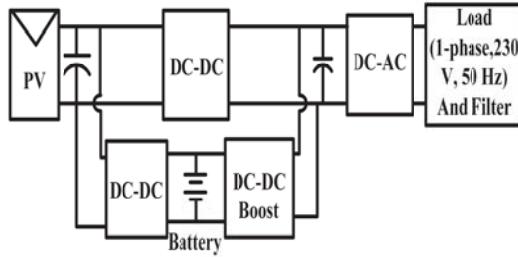


Figure 1.4: Block diagram of the stand alone scheme proposed in [14]

The higher number of power conversion stages used in both of the above approaches reduce efficiency and reliability of the system as the component count becomes more. Further, these configurations also suffer from low battery charging efficiency as two converter stages exist in the battery charging path. Further, the converter used for extracting maximum power remains idle when there is no PV power thereby reducing the utilization of the system.

In order to increase the battery charging efficiency an alternative four stage configuration is proposed in [14]. The schematic block diagram of this scheme is shown in Fig. 1.4. In this case, only one dc-dc converter stage is placed between the PV panel and the battery. Although it improves battery charging efficiency, it requires either higher voltage level for the PV panel and the battery or a fourth dc-dc converter is required to provide the necessary voltage gain. In addition to this, the control scheme is complex as a proper coordinated control and fast convergence time for the MPPT algorithm is required.

(B) Three stage configuration

Depending on the placement of the battery, these schemes can be further classified as follows:

(i) Schemes having battery placed in the cascaded path:

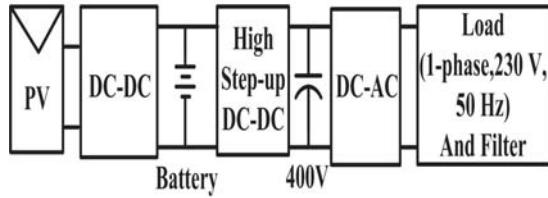


Figure 1.5: Basic structure of a three stage configuration with cascaded placement of battery

Schematic block diagram of a three stage configuration wherein the battery is placed in cascade with the other converters is shown in Fig. 1.5. This type of configuration [15]-[16] has the following drawbacks: (a) battery has to negotiate frequent unwanted charging/discharging with sudden change in the load or PV power thereby increasing stress on the battery [14], and (b) the battery voltage has to be high otherwise the step-up dc-dc converter following the battery has to be designed to achieve very high gain.

(ii) Schemes having battery placed in parallel path:

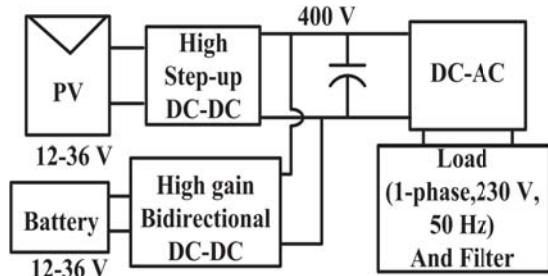


Figure 1.6: Basic structure of a three stage configuration with battery placed in the parallel path

Fig.1.6 shows the schematic block diagram of a three stage configuration wherein the battery is placed in parallel to the converters through a bidirectional converter [17]-[20]. This configuration eliminates the problem associated with the placement of battery in cascaded. However, both the dc-dc converters in this configuration are required to be designed for high gain involving high frequency transformer coupled converter topology. Hence minimum number of switches required for realizing dc-dc converters involved in the scheme is five. This is in addition to four switches for realizing the dc to ac inverter and two high frequency transformers/coupled inductors. This leads to increased cost and reduction in efficiency of the scheme.

(C) Two stage configuration

In order to achieve further reduction in the number of power conversion stages, a two stage configuration is reported in [21]. It is realized by eliminating ‘high step-up dc-dc’ converter from the configuration of Fig 1.5. However, this scheme requires higher voltage level for the PV panel and the battery in addition to the the problems associated with the placement of the battery in cascaded path [14].

(D) Single stage configuration

Single stage configuration having a lone dc-ac power conversion stage as shown in Fig. 1.7 is also reported in the literature [22]-[23]. These systems do not incorporate storage element and are employed for water pumping applications. The frequency and hence the speed of the motor driving the pump are adjusted in order to match the load power requirement with that of the available maximum power of the PV panel. However, this configuration cannot be used to supply household appliances as it is not possible to achieve both MPPT operation and load voltage control without employing energy storage element.

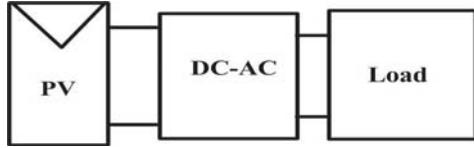


Figure 1.7: Basic structure of a single stage configuration.

1.3 Single Phase Transformer-Less Grid Connected Systems

Grid connected decentralized/distributed schemes for electrical power generation has gained interest in recent years due to its several advantages viz. less inertia, local power consumption, easy extendibility, elimination of storage requirement, etc. Recent trend is to employ renewable energy sources (RES) as the driving input for such schemes where they are connected to the distribution grid through suitable power electronic interface. Amongst the available RES, solar photovoltaic (PV) has evolved to be a prominent candidate as it is available in abundance, free and inexhaustible. General block diagram of a PV based decentralized grid connected scheme is shown in Fig 1.8. As the solar PV power is available in dc form, such scheme requires the service of a dc-ac inverter to form the interfacing link between the PV source and the ac grid. A single phase inverter is generally employed to form the aforementioned interface link as decentralized schemes are typically designed for low power rating (<5 kW). In addition to this inverter, a dc-dc converter is sometimes employed to achieve MPP tracking of the PV panel and to provide dc voltage boosting, if required. However, the use of this dc-dc converter is optional as

the MPP tracking can also be achieved through the inverter by incorporating suitable control algorithm. As the presence of this dc-dc converter leads to reduction in efficiency of the system, it is generally avoided in modern grid connected systems. The requirement of voltage boosting can be avoided by connecting more numbers of PV module in series to obtain desired voltage level. A low frequency transformer is sometimes employed at the inverter output to provide galvanic isolation between the PV panel and the grid. This transformer can also provide voltage boosting, if required. The capacitors, C_{pv1} and C_{pv2} , represent the PV parasitic capacitances which exist between the PV panel and the ground.

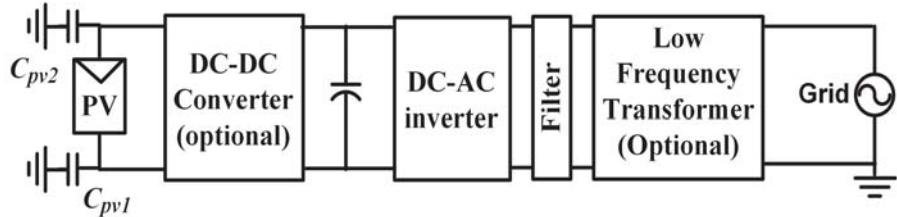


Figure 1.8: General block diagram of a PV based grid connected scheme

Existing single phase grid connected schemes can be broadly classified as: (a) topologies utilizing transformer for galvanic isolation, and (b) transformerless schemes. The schemes employing transformer to incorporate isolation between the grid and the solar panels have the following advantages: (a) prevention of dc current flow into the grid, (b) provision for voltage boosting, and (c) reduced safety concerns. However, the presence of low frequency transformer considerably increases the weight and volume of the system [24]. Schemes employing high frequency transformer for isolation have low volume and weight, but they require two stages of power conversion which reduces the overall efficiency of the system and increases the control complexity [24]-[25]. In order to eliminate the aforementioned drawbacks associated with the presence of transformer, efforts have been made to develop inverters which do not require the service of a transformer [25]. However, the transformerless inverters lack galvanic isolation between grid and the PV source. This results in flow of leakage current through parasitic capacitances present between the ground and the PV source. Leakage current present in transformerless grid connected inverters leads to additional losses, distortion in grid current, increased electromagnetic interference, and reduction in safety of the personnel in proximity of the solar panel [26]-[27]. The issues pertaining to the cause of leakage current flow and measures to be taken for its mitigation, are detailed in the following section.

1.3.1 Leakage current in transformer-less grid connected inverter

The cause of leakage current flow in grid connected PV system is due to the presence of parasitic capacitance between the PV panel and the ground. The equivalent structure of PV panel showing the presence of the parasitic capacitance is depicted in Fig. 1.9 [28]. The value of this parasitic capacitance depends on several factors viz. (a) PV panel and frame structure, (b) surface area of the cells and distance between the cells, (c) structure

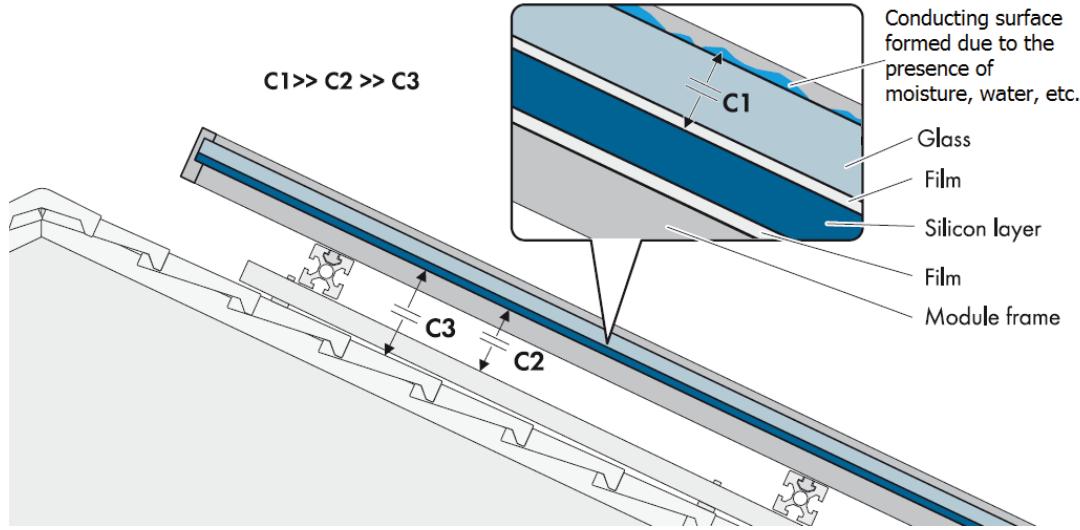


Figure 1.9: PV panel structure depicting presence of parasitic capacitance [28]

of the module frame, (d) weather conditions, (e) humidity, (f) dust or salt covering the PV panel, and (g) type of electromagnetic compatibility (EMC) filter [29]. The approximate value of this parasitic capacitance is about 60-110 nF/kW for crystalline silicon cells (monocrystalline, poly-crystalline) whereas it increases to 100-160 nF/kW for thin-film (e.g. CdTe) solar cells [28].

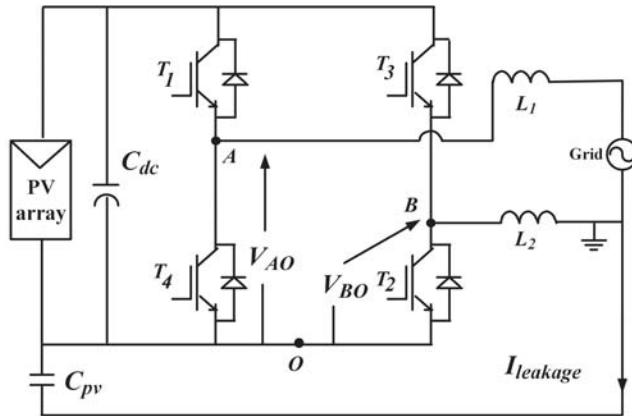


Figure 1.10: Transformerless standard H-bridge inverter depicting leakage current path through PV parasitic capacitance

The leakage current path through PV parasitic capacitance in a standard H-bridge transformerless inverter is depicted in Fig. 1.10 [32]. Here $I_{leakage}$ is the leakage current, C_{pv} is parasitic capacitance of the PV panel, and L_1 , L_2 are the filter inductances. Though only one inductor would have been sufficient to serve the purpose of filtering, two inductors are employed for this purpose the reason for which is discussed later in this Section. An

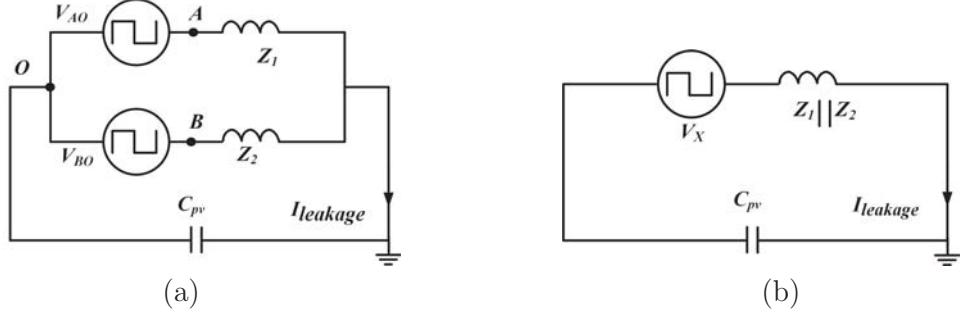


Figure 1.11: Equivalent mathematical model depicting leakage current path in a standard H-bridge inverter: (a) actual model, and (b) simplified model

equivalent mathematical model of Fig. 1.10 to analysis the leakage current of the system is depicted in Fig. 1.11(a). Here Z_1 and Z_2 are the impedances of the inductors, L_1 , and L_2 respectively. Applying Millman's/Thevenin theorem this model can be simplified further as shown in Fig. 1.11(b). The expression for the voltage, V_X shown in Fig. 1.11(b) is given by,

$$V_X = \frac{\frac{V_{AO}}{Z_1} + \frac{V_{BO}}{Z_2}}{\frac{1}{Z_1} + \frac{1}{Z_2}} = \frac{V_{AO}Z_2 + V_{BO}Z_1}{Z_1 + Z_2} \quad (1.1)$$

$$= V_{AO}\frac{Z_2}{Z_1 + Z_2} + V_{BO}\frac{Z_1}{Z_1 + Z_2} \quad (1.2)$$

wherein $Z = Z_1 + Z_2$. Rearranging/modifying (1.2) ,

$$\begin{aligned} V_X &= V_{AO}\frac{Z_2}{Z} - V_{AO}\frac{Z_1}{Z} + V_{AO}\frac{Z_1}{Z} + V_{BO}\frac{Z_1}{Z} \\ &= V_{AO}\frac{Z_2 - Z_1}{Z} + (V_{AO} + V_{BO})\frac{Z_1}{Z} \end{aligned} \quad (1.3)$$

Again rearranging/modifying (1.2) ,

$$\begin{aligned} V_X &= V_{AO}\frac{Z_2}{Z} + V_{BO}\frac{Z_1}{Z} + V_{BO}\frac{Z_2}{Z} - V_{BO}\frac{Z_1}{Z} \\ &= (V_{AO} + V_{BO})\frac{Z_2}{Z} - V_{BO}\frac{Z_2 - Z_1}{Z} \end{aligned} \quad (1.4)$$

Adding (1.3) and (1.4),

$$\begin{aligned} 2V_X &= V_{AO}\frac{Z_2 - Z_1}{Z} + (V_{AO} + V_{BO})\frac{Z_1}{Z} + (V_{AO} + V_{BO})\frac{Z_2}{Z} - V_{BO}\frac{Z_2 - Z_1}{Z} \\ 2V_X &= (V_{AO} + V_{BO}) + (V_{AO} - V_{BO})\frac{Z_2 - Z_1}{Z} \end{aligned}$$

$$V_X = \frac{V_{AO} + V_{BO}}{2} + \frac{V_{AO} - V_{BO}}{2}\frac{Z_2 - Z_1}{Z} \quad (1.5)$$

$$V_X = V_Y + \frac{V_Z}{2}\frac{Z_2 - Z_1}{Z} \quad (1.6)$$

wherein,

$$\begin{aligned} V_Y &= \frac{V_{AO} + V_{BO}}{2}, \quad \text{and,} \\ V_Z &= V_{AO} - V_{BO} \end{aligned} \quad (1.7)$$

Multiplying (1.7) with $\frac{Z_1}{Z}$,

$$V_Z \frac{Z_1}{Z} = V_{AO} \frac{Z_1}{Z} - V_{BO} \frac{Z_1}{Z} \quad (1.8)$$

Multiplying (1.7) with $\frac{Z_2}{Z}$,

$$V_Z \frac{Z_2}{Z} = V_{AO} \frac{Z_2}{Z} - V_{BO} \frac{Z_2}{Z} \quad (1.9)$$

Adding (1.2) and (1.8),

$$\begin{aligned} V_X + V_Z \frac{Z_1}{Z} &= V_{AO} \frac{Z_2}{Z} + V_{BO} \frac{Z_1}{Z} + V_{AO} \frac{Z_1}{Z} - V_{BO} \frac{Z_1}{Z} \\ V_{AO} &= V_X + V_Z \frac{Z_1}{Z} \end{aligned} \quad (1.10)$$

Adding (1.2) and (1.9),

$$\begin{aligned} V_X + V_Z \frac{Z_2}{Z} &= V_{AO} \frac{Z_2}{Z} + V_{BO} \frac{Z_1}{Z} + V_{AO} \frac{Z_2}{Z} - V_{BO} \frac{Z_2}{Z} \\ V_X + V_Z \frac{Z_2}{Z} &= V_{AO} \frac{2Z_2}{Z} + V_{BO} \frac{Z_1 - Z_2}{Z} \\ V_X + V_Z \frac{Z_2}{Z} &= (V_X + V_Z \frac{Z_1}{Z}) \frac{2Z_2}{Z} + V_{BO} \frac{Z_1 - Z_2}{Z}; \quad \text{using (1.10)} \\ V_X \left(1 - \frac{2Z_2}{Z}\right) + V_Z \left(\frac{Z_2}{Z} - \frac{2Z_1 Z_2}{Z^2}\right) &= V_{BO} \frac{Z_1 - Z_2}{Z} \\ V_X \left(\frac{Z_1 - Z_2}{Z}\right) + V_Z \left(\frac{Z_2(Z_2 - Z_1)}{Z}\right) &= V_{BO} \frac{Z_1 - Z_2}{Z} \\ V_X - V_Z \frac{Z_2}{Z} &= V_{BO} \\ V_{BO} &= V_X - V_Z \frac{Z_2}{Z} \end{aligned} \quad (1.11)$$

Substituting expression of V_X from (1.6) in (1.10),

$$\begin{aligned} V_{AO} &= V_Y + \frac{V_Z}{2} \frac{Z_2 - Z_1}{Z} + V_Z \frac{Z_1}{Z} \\ V_{AO} &= V_Y + \frac{V_Z}{2} \end{aligned} \quad (1.12)$$

Substituting expression of V_X from (1.6) in (1.11),

$$\begin{aligned} V_{BO} &= V_Y + \frac{V_Z}{2} \frac{Z_2 - Z_1}{Z} - V_Z \frac{Z_2}{Z} \\ V_{BO} &= V_Y - \frac{V_Z}{2} \end{aligned} \quad (1.13)$$

From (1.12) and (1.13), it can be observed that the term ' V_Y ' is common for both input voltages, V_{AO} and V_{BO} in the equivalent mathematical model shown in Fig. 1.11(a). Hence, V_Y is termed hereafter as the common mode voltage for the system, V_{CM} . From (1.7), it can be observed that the term ' V_Z ' is the difference between V_{AO} and V_{BO} . Hence V_Z is termed hereafter as the differential mode voltage for the system, V_{DM} .

Substituting the expressions for V_{AO} and V_{BO} from (1.12) and (1.13) respectively, Fig. 1.11 can be redrawn as shown in Fig. 1.12. Applying Millman's/Thevenin theorem the

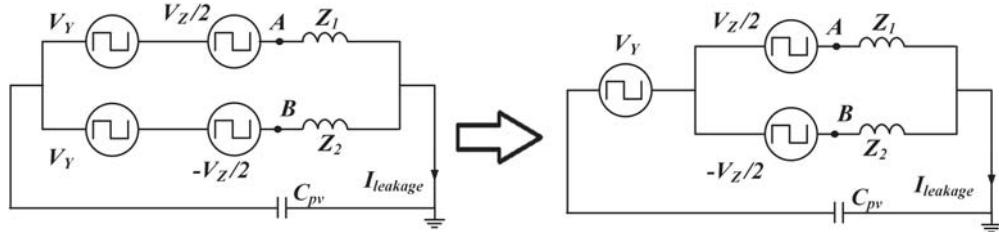


Figure 1.12: Equivalent mathematical model depicting leakage current path in a standard H-bridge inverter in terms of common mode and differential mode voltage

model shown in Fig. 1.12 can be simplified further as shown in Fig. 1.13. From Fig. 1.13

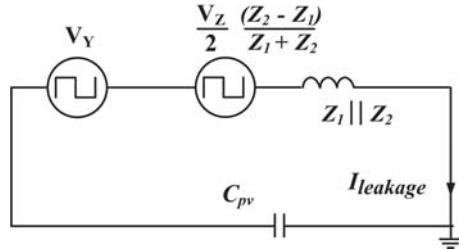


Figure 1.13: Simplified mathematical model depicting leakage current path in a standard H-bridge inverter

it can be observed that the voltages, V_Y (or V_{CM}), and V_Z (or V_{DM}) act as a forcing function for the flow of leakage current through the PV parasitic capacitance. Hence the leakage current flow can be minimized/eliminated if the aforementioned forcing functions can be made either of the following: (a) zero, (b) constant dc, or (c) having only low frequency components as the impedance offered by C_{PV} is very large at low frequency. Another possibility to eliminate leakage current is to ensure that the PV parasitic capacitances are impressed with either zero or fixed dc voltage as impedance offered by the capacitor to the dc voltage is infinite.

Effect of PWM switching strategies on leakage current in H-Bridge inverter:

In H-bridge inverter based transformerless grid connected schemes, the filter inductances, L_1 and L_2 , are kept equal so as to ensure $Z_1 = Z_2$. This eliminates the portion of forcing function involving V_Z shown in Fig. 1.13. Hence the flow of leakage current in this case depends on the magnitude and frequency of V_Y (or V_{CM}). The switching strategy for H-bridge single phase inverter is generally realized by either of the following: (a) bipolar, (b) unipolar and (c) hybrid sinusoidal pulse width modulation (SPWM) technique. The magnitude of V_{CM} for these modulation techniques are provided in Table 1.2. From this table it can be observed that V_{CM} is constant over a grid cycle in bipolar SPWM technique and hence this PWM technique generates negligible leakage current. In case of unipolar as well as in hybrid PWM technique V_{CM} has inverter switching frequency components. Hence wherein these PWM techniques are employed, there will be a considerable magnitude of leakage current in the system as less impedance is offered by C_{PV} for high frequency components present in V_{CM} . Thus, amongst the three modulation techniques, only bipolar technique can be employed for transformerless H-bridge inverter to restrict leakage current within a permissible limit. However, the efficiency of the inverter gets reduced if bipolar PWM is employed instead of unipolar or hybrid PWM based switching logic. As efficiency is a major concern in transformerless grid connected systems, bipolar technique is seldom employed. To achieve high efficiency and acceptable magnitude of leakage current several schemes have been reported in the literature which is discussed in next Subsection.

Table 1.2: Common mode voltage generated in three commonly employed modulation techniques for H-Bridge inverter

Bipolar SPWM Technique							
Positive Half Cycle				Negative Half Cycle			
Switching States in a switching cycle	V_{AO}	V_{BO}	$\frac{V_{CM}}{2} = \frac{V_{AO}+V_{BO}}{2}$	Switching States in a switching cycle	V_{AO}	V_{BO}	$\frac{V_{CM}}{2} = \frac{V_{AO}+V_{BO}}{2}$
S_1, S_2 ON	V_{PV}	0	$V_{PV}/2$	S_1, S_2 ON	V_{PV}	0	$V_{PV}/2$
S_3, S_4 ON	0	V_{PV}	$V_{PV}/2$	S_3, S_4 ON	0	V_{PV}	$V_{PV}/2$
Unipolar SPWM Technique							
Positive Half Cycle				Negative Half Cycle			
Switching States in a switching cycle	V_{AO}	V_{BO}	$\frac{V_{CM}}{2} = \frac{V_{AO}+V_{BO}}{2}$	Switching States in a switching cycle	V_{AO}	V_{BO}	$\frac{V_{CM}}{2} = \frac{V_{AO}+V_{BO}}{2}$
S_1, S_2 ON	V_{PV}	0	$V_{PV}/2$	S_3, S_4 ON	0	V_{PV}	$V_{PV}/2$
S_2, S_4 ON	0	0	0	S_1, S_3 ON	V_{PV}	V_{PV}	V_{PV}
S_1, S_2 ON	V_{PV}	0	$V_{PV}/2$	S_3, S_4 ON	0	V_{PV}	$V_{PV}/2$
S_1, S_3 ON	V_{PV}	V_{PV}	V_{PV}	S_2, S_4 ON	0	0	0
Hybrid SPWM Technique							
Positive Half Cycle				Negative Half Cycle			
Switching States in a switching cycle	V_{AO}	V_{BO}	$\frac{V_{CM}}{2} = \frac{V_{AO}+V_{BO}}{2}$	Switching States in a switching cycle	V_{AO}	V_{BO}	$\frac{V_{CM}}{2} = \frac{V_{AO}+V_{BO}}{2}$
S_1, S_2 ON	V_{PV}	0	$V_{PV}/2$	S_3, S_4 ON	0	V_{PV}	$V_{PV}/2$
S_2, S_4 ON	0	0	0	S_1, S_3 ON	V_{PV}	V_{PV}	V_{PV}

1.3.2 Literature review of single phase transformer-less grid connected inverter schemes

In order to minimize the leakage current flow within permissible limit several topologies for transformerless gird connected inverter have been reported in literature. Based on the basic philosophy employed for leakage current minimization, these topologies can be broadly classified into three groups. The first group of topologies are derived from the basic H-bridge inverter depicted in Fig. 1.10(a). These topologies attempt to maintain the common mode voltage constant by isolating the PV source from the grid during the free wheeling mode of operation for unipolar and hybrid SPWM strategies [24], [33]-[40]. The aforementioned isolation can be realized by adding additional switch(es) on the dc side [24], [33]- [35] or in the ac side [36]- [40] of the basic H-bridge inverter circuit. The power circuit configurations of two schemes wherein additional switch(es) are employed in the dc side of the inverter are depicted in Fig. 1.14. The power circuit configurations of two schemes wherein additional switch(es) are employed in the ac side of the inverter are depicted in Fig. 1.15. However, the profile of common mode voltage in the aforementioned H-bridge topologies depends on the parasitic capacitances (including junction capacitance of switches) present in the leakage current loop, their location and grid voltage magnitude [32], [41] and hence minimization of leakage current within a permissible value can not be guaranteed. Further, these topologies are based on H-bridge structure which is a buck type of inverter and hence the designed PV voltage must be kept higher than the peak amplitude of the grid voltage. Considering variation in PV voltage with environmental conditions sufficient margin has to be kept for the designed value of the PV voltage. Higher the voltage level, higher number of PV modules needs to be connected in series to form the PV panel. As the number of series connected modules increases, the possibility of reduction in power yield when PV modules are operated in mismatched condition also increases [3]- [5]. This issue is discussed in detail in Section 1.4.

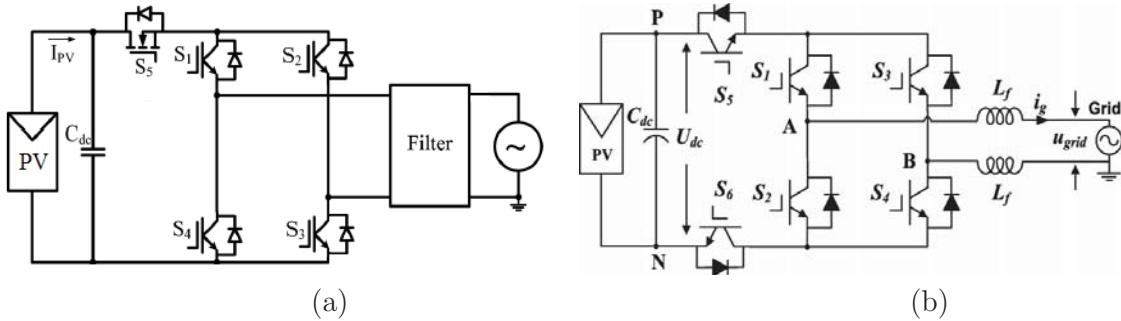


Figure 1.14: H-bridge inverter based transformerless topologies having isolation arrangement on the dc side: (a) H-5 topology from SMA Corporation [33], and (b) H-6 topology [24]

The second group of topologies attempts to minimize leakage current by clamping common mode voltage at half of the PV panel voltage [32], [41]- [45]. In order to achieve this, these topologies employs a combination of two series connected capacitors across the

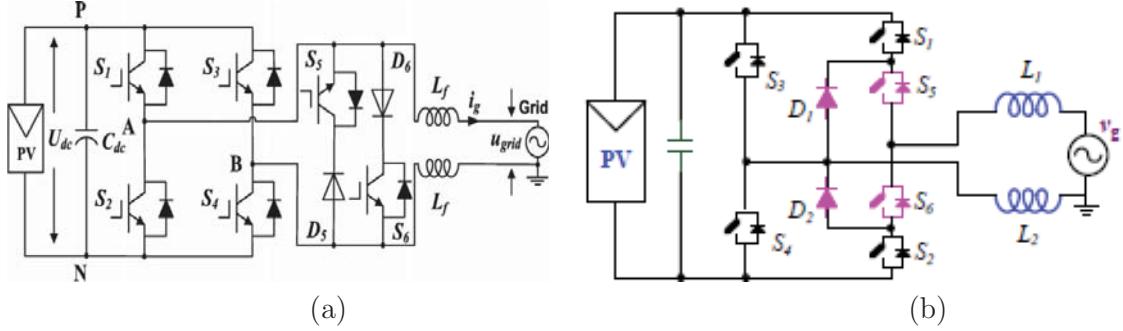


Figure 1.15: H-bridge inverter based transformerless topologies having isolation arrangement on the ac side: (a) HERIC topology from Sunways Company [36], and (b) topology presented in [40]

PV panel. The mid point of these capacitors are connected to a suitable point in inverter through diode(s)/switch(es) so as to clamp the common mode voltage constant at half of the PV panel voltage. The power circuit configuration of two such topologies are depicted in Fig. 1.16. These topologies are commonly termed as neutral point clamped (NPC) inverters and are basically derived by modifying the inverter structure discussed for the H-bridge based topologies in the previous paragraph. Hence, these topologies also require PV voltage level similar to H-bridge based inverters as they also operate in buck mode.

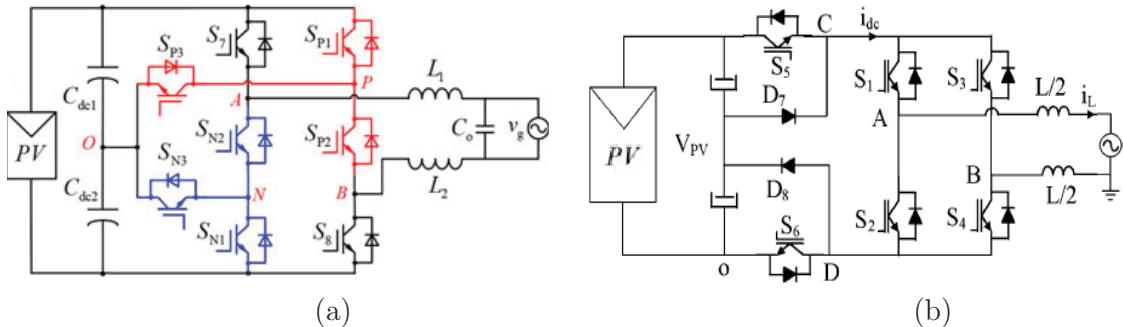


Figure 1.16: Neutral point clamped based inverter topologies: (a) topology presented in [32], and (b) topology presented in [42]

The third group of topologies attempts to minimize leakage current by ensuring either zero or constant voltage across PV parasitic capacitors. This is achieved by connecting grid neutral terminal to any of the following: (1) the negative bus of PV source [31], [46]-[48] (an example of such scheme is depicted in Fig. 1.17(a)), (2) the midpoint of the split capacitor connected across PV source (an example of such scheme is depicted in Fig. 1.17(b)) [49]- [50], and (3) the midpoint of two PV panel [51]- [53] (an example of such scheme is depicted in Fig. 1.17(c)). As the grid neutral is connected to the ground, the PV parasitic capacitors either gets shorted or they are impressed with constant voltage equal to half of the PV panel voltage. This ensures minimal leakage current flow through PV parasitic capacitances. The scheme reported in [31] requires the presence of an additional dc-dc converter. The inverter presented in [46] is of buck-boost type but is having the drawback of asymmetrical operation as viewed by the grid. The inverter proposed in [48]

is buck type of inverter. The standard NPC based inverter topologies require double the voltage than that of H-bridge inverter [49]- [50] and hence are very prone to power yield reduction under mismatched operating conditions. The schemes reported in [51]-[52] can operate satisfactorily if both the PV panels are exposed to similar physical conditions. Further, the energy output from each of the PV panels are required to be stored in a capacitor connected across that PV panel over a half cycle of the grid voltage. This demands two large capacitors, to be connected across each of the PV panels, to ensure maximum power extraction from both the panels by reducing the magnitude of voltage ripple across the panels. The schemes presented in [53] can extract maximum power from two PV panels but the inverter employed for this scheme is of buck type. This leads to same limitations as that of schemes based on H-bridge inverters.

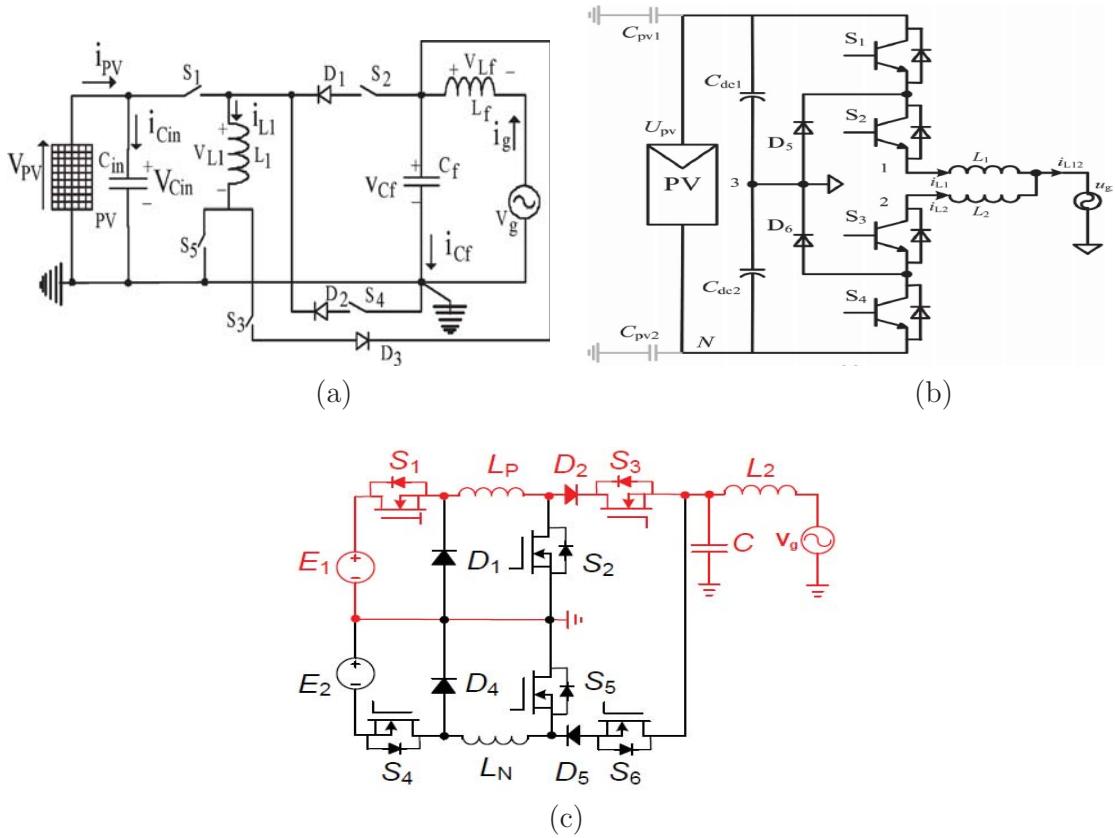


Figure 1.17: Transformerless grid connected inverter topologies where grid neutral is connected to: (a) the negative bus of PV source [47], (b) the midpoint of the split capacitor connected across PV source [49], and (c) the midpoint of two PV panel [52]

1.4 Distributed Maximum Power Point Tracking (DMPPT) Schemes

Depending on the power level, a number of PV modules are connected in series and parallel to form a PV panel. For low power systems, PV modules are generally connected in parallel. As power rating of the system increases, the PV voltage level is also increased by connecting several PV modules in series to form a PV string in order to reduce losses in the system. However, as series connected PV modules have to carry the same amount of current, performance of the system deteriorates considerably when some or all of the PV modules experience different operating condition [4]-[5]. This mismatch in operating condition can be due to several reasons viz. shading from different objects including self shadow at dusk and dawn, manufacturing process error, ageing, dust/impurity layer, orientation mismatch, etc. Due to these mismatched operating conditions, the current generation capacity of each module at their respective maximum power points (I_{mpp}) differs from each other. However, being connected in series, each module has to carry the same amount of current which is generally dictated by the maximum power point tracking (MPPT) algorithm employed to maximize the power output from that string. If this MPPT algorithm sets a current, say $I_{mpstring}$, which is less than the I_{mpp} of a module, it generates less power than its maximum capability. On the other hand, if $I_{mpstring}$ is more than I_{mpp} of a module, then also that particular module produces less power than its maximum capability till $I_{mpstring}$ is less than the short circuit current, I_{SC} of that module. Once $I_{mpstring}$ exceeds I_{SC} of a module, it operates in the second quadrant of its I-V characteristics curve. This can be inferred from the extended I-V characteristics of a PV module depicted in Fig. 1.18(a) [72]. When a PV module operates in the second quadrant of its I-V characteristic curve, it acts as a load and hence instead of generating power it absorbs power. Further, if the power consumed by a module exceeds its permissible limit, it may get damaged due to the formation of hot-spots [4]-[5]. Protection against such damage can be provided by connecting a bypass diode across each PV module [4]-[5]. This diode gets turned on when module voltage, during operation in its second quadrant, reaches the threshold voltage of the diode (Fig. 1.18(b)). When the diode gets turned on, power consumption of PV module operating in second quadrant gets restricted to a permissible value and the formation of hot-spots is thus avoided. Schemes having bypass diodes are very simple to implement and exhibit negligible losses when all the series connected PV modules operate in their respective first quadrants as the diodes remain turned off. However, when diode(s) gets turned on while PV modules operates under mismatched conditions, the PV string exhibits multiple local maximum power points [54]. An example of formation of multiple power peak points in a PV string comprising of two PV module is depicted in Fig. 1.19. Amongst all the local peak power points the point wherein the power yield is maximum is known as global MPP (GMPP). The target of the MPPT algorithm employed is to operate the system at this GMPP. However, the conventional MPPT algorithm can not be employed to track GMPP as it may get trapped in a local MPP instead of the GMPP. This issue can be addressed by employing more sophisticated MPPT algorithms commonly termed as global MPPT

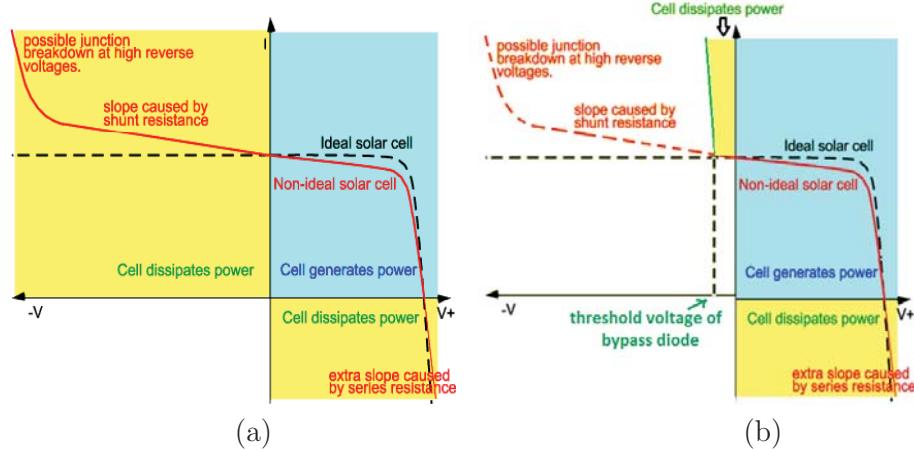


Figure 1.18: Extended I-V characteristics of a PV cell: a) without bypass diode [72] and b) with bypass diode

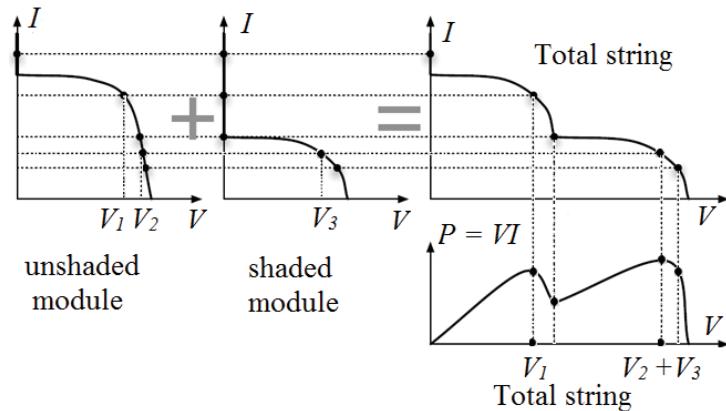


Figure 1.19: Formation of multiple power point peaks

(GMPPT) algorithms which are capable of tracking the GMPP [54]-[55]. However, the amount of power extracted from the panel while operating it at its GMPP is less than that of the sum of individual maximum power yield capability of all the PV modules. This is due to the fact that if the bypass diode of a module gets turned on then it will not generate any power even though it is having the capability to do so.

In order to extract maximum power from individual series connected PV modules the concept of distributed maximum power point tracking (DMPPT) is introduced in several schemes reported in the literature [56]-[71]. The DMPPT schemes employ additional local dc-dc converters in conjunction with a central dc to dc or dc to ac converter. These local dc-dc converters attempt to operate individual PV modules at their respective MPPs. This forms a single peak power point for the entire PV string and a conventional MPPT algorithm can be employed to track this peak power point. The aforementioned MPPT algorithm is realized utilizing the central converter which is henceforth referred

to as central MPPT algorithm. Based on the amount of power processed by the local dc-dc converters, DMPPT schemes can be classified in the following two categories: (a) full power-dedicated dc-dc converter based DMPPT (FPDC-DMPPT) schemes and (b) compensating power-dedicated dc-dc converter based DMPPT (CPDC-DMPPT) schemes [68]. In FPDC-DMPPT schemes, a dedicated dc-dc converter is connected across each series connected PV modules. Total power extracted from each of the PV modules are processed by the corresponding local dc-dc converter and hence the overall efficiency of the scheme gets considerably affected by the losses incurred in these local dc-dc converters. In CPDC-DMPPT schemes, the local converters process only a small portion of the PV power. Hence efficiency of such schemes are better as compared FPDC-DMPPT schemes. Due to the aforementioned reason CPDC-DMPPT schemes are preferred and are considered in this thesis.

A typical structure of a CPDC-DMPPT scheme is shown in Fig. 1.20 wherein flyback converters are employed as local dc-dc converters [57], [68]. The major advantages of such DMPPT schemes are: (a) each PV module can be operated at their true/approximate MPP, (b) high efficiency as the local dc-dc converters process partial power allowing most of the PV string power to be directly transmitted to the central converter, and (c) simple implementation. A brief overview of the existing CPDC-DMPPT schemes is presented in the following subsection.

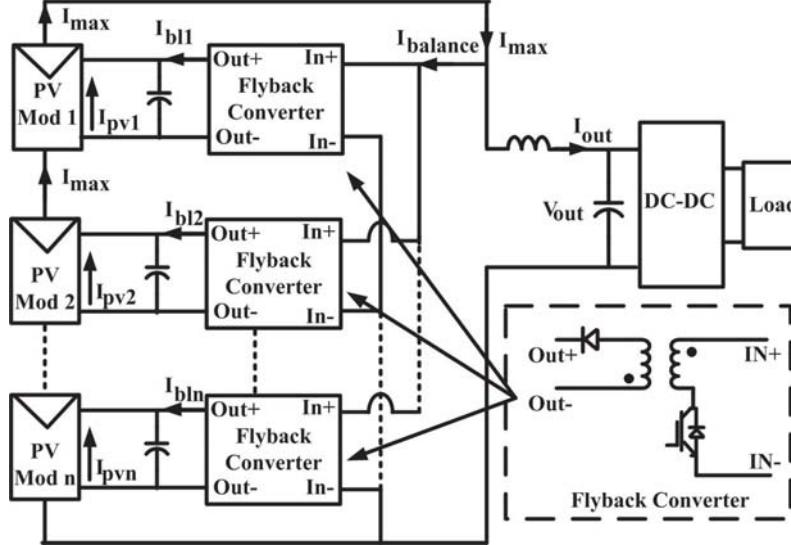


Figure 1.20: Flyback converter based CPDC-DMPPT scheme [57], [68]

1.4.1 Literature review of CPDC-DMPPT schemes

The various CPDC-DMPPT schemes reported in the literature can be broadly classified as: (a) voltage equalization based approximate MPP scheme [56]-[65], (b) model based MPP schemes [66]-[67], and (c) exact MPP schemes [56], [68]-[71].

The voltage equalization schemes are based on the assumption that the voltage at maximum power point, V_{mpp} for each module remains almost same even with wide changes in atmospheric conditions [56]-[65]. Hence, these schemes clamp the voltage across each of

the serially connected module at the same value irrespective of their operating conditions. The reference voltage command for each module is generated as, $V_{pv_ref} = V_{string_ref}/N$ wherein V_{string_ref} is the reference voltage command generated from the central MPPT algorithm for the entire string and N is the number of modules connected in series. The actual PV module voltage is forced to follow the aforesaid reference command by means of local dc-dc converters. These local converters can be connected in various configurations across individual or a group of series connected PV modules. Both isolated as well as non-isolated dc-dc converters can be employed to serve the purpose. The voltage equalization schemes are easy to implement and require only $(N + 1)$ voltage sensors and one current sensor. However, as the V_{mpp} for each module is not exactly the same under mismatched operating conditions, voltage equalization based schemes can not extract exact maximum power from each module.

The model based MPP schemes operate by sensing values of insolation level and temperature for each module [66]-[67]. The sensed values of these parameters are fed to an approximate equivalent mathematical model of the PV module which generates suitable voltage reference command for each PV module. Thus information of power negotiated by each module or that of the total string is not required for functioning of these schemes. However, such schemes heavily rely on the accuracy of the function/model used to generate reference for the voltage command. Also such model needs to be periodically upgraded to account for the factors affected by ageing.

The exact MPP schemes determines the exact MPP information of each module and accordingly controls the local converters so as to operate each of the PV module at their corresponding MPP [56], [68]-[71]. These schemes do not require sensing of insolation level or temperature for obtaining MPP information of each of the PV modules. The scheme proposed in [68] employs flyback converter as local converter to extract maximum power from serially connected PV modules. However, this scheme requires that PV string to be disconnected from the central converter periodically to obtain MPP of each of the module. During this disconnection time interval, PV power is not fed to the central converter. This results in discontinuity in power flow to the grid or load which is not desirable. The scheme proposed in [69] employs buck-boost converter as local dc-dc converters. However, in this case it is required to solve $N \times N$ matrix online and then $(N + 1)$ MPPT algorithms need to be run simultaneously. This increases computational burden on the processor. The scheme proposed in [70] discusses operation of DMPPT scheme utilizing unidirectional as well as bidirectional isolated converter based local converters. However, this scheme requires complex controller to obtain information of MPP of each PV module. In addition to these drawbacks, the aforementioned exact MPP based schemes need to sense power of every PV module to generate their reference command of V_{mpp} [68]-[70]. This requires $(N + 1)$ number of current sensors in addition to $(N + 1)$ number of voltage sensors. As a result, overall cost and wiring requirement for the system are increased. In order to avoid current sensing for each module, a scheme is proposed in [71] where the final output of the PV string is used for MPP tracking. However, this scheme requires $(N + 1)$ MPPT algorithms to run simultaneously; one for each of the controllers associated with N number of local dc-dc converters and one for the central converter. In addition to increased

computational burden, there is a possibility that the operating point obtained may not be the optimum one. This may happen as ambiguity may creep in while deciphering the effect of simultaneous perturbations in local converters. A scheme which requires a single voltage and a single current sensor is proposed in [56]. It employs multistage chopper circuit to realize local dc-dc converters. In this scheme the duty ratios of $(N - 1)$ local converters are kept fixed and the duty ratio of the remaining local converter is varied to maximize the string output power. After a certain interval, duty ratio the next local converter is varied to maximize power yield whereas duty ratio of remaining $(N - 1)$ converters are kept fixed. This process is repeated cyclically. However, this scheme encounters several constraints as follows: (a) not suitable for schemes with higher number of series connected modules, (b) owing to open loop mode of operation, control of module voltages at desired levels can not be guaranteed, (c) this scheme is not tolerant to shoot through fault and the effect of dead band on the performance of the scheme has not been evaluated, and (d) this strategy cannot be applied for schemes which employ isolated local converters.

1.5 Summary of the Literature Survey and Scope for Further Improvement

The literature review for the existing stand alone schemes presented in Section 1.2.3 reveal that they have one or more of the following limitations: (a) requirement of higher voltage level for the PV panel and the battery, (b) necessity of larger number of power conversion stages, and (c) usage of a low frequency transformer to achieve voltage boosting. In order to address these issues, efforts can be made to develop a stand alone scheme having the following features: (a) which is designed with a low voltage level(s) for the PV panel and the battery to avoid concerns as discussed in section 1.2.1, (b) which have minimum numbers of power conversion stages to improve efficiency and reliability of the system, (c) which protects the battery from over charge and over discharge thereby increasing the life time of the battery, (d) which eliminates the requirement of a low frequency transformer to make the system compact and light weight, and (e) which has a simple control strategy to enable the system to operate in all possible modes that are generally encountered in a stand alone system.

Based on the critical review of the existing decentralized transformer-less grid connected schemes it can be concluded that these schemes have one or more of the following drawbacks: (a) requirement of high voltage level for the PV panel owing to the buck nature of the inverter, (b) inability to support wide variation in PV panel voltage, (c) inability to ensure flow of leakage current within permissible limit, (d) inability to eliminate shoot through fault problem, (e) requirement of the service of an additional dc-dc converter, (f) requirement of two separate PV panels to be operated at the same conditions. In order to address the aforementioned issues effort can be made to develop a solar PV based grid connected inverter scheme having the following features: (a) incorporation of voltage buck-boost capability into the inverter so that lower voltage levels can be used for the PV panel and which also permits a wide variation in the PV panel voltage, (b) the inverter having the feature of avoiding shoot through fault, (c) capability of the inverter

for extracting maximum power from PV panel(s), (d) elimination of concerns pertaining to the flow of leakage current, (e) restriction of dc current injection into the grid and limiting the total harmonic distortion in the grid current within permissible levels.

The existing CPDC-DMPPT schemes reported in the literature have one or more of the following limitations: (a) employment of voltage equalization based scheme which cannot ensure maximum power extraction from each of the serially connected PV module, (b) requirement of sensing of temperature and insolation level, (c) necessity of large number of sensors, (d) requirement of communication among the local dc-dc converters, (e) incapability for realizing schemes having considerable numbers of series connected PV modules, (f) requirement of a high-end processor to realize computation-intensive algorithm. In order to address the aforementioned issues efforts need to be made to develop a DMPPT scheme having the following features: (a) capability of extracting maximum power from individual serially connected modules employing minimum number of sensors, (b) simple implementation ensuring less burden on the processor required for realizing the controller, (c) no requirement of having communication links among local converters, (d) suitability for schemes having large number of series connected modules, and (e) eliminating the requirement for sensing of temperature and insolation level.

1.6 Objective of the Thesis

Based on the critical review of the schemes reported in the literature for the three selected topics following objectives are set for this dissertation:

Objective for stand alone scheme: to develop solar PV based stand alone systems with battery as energy storage element for supplying off-grid single-phase household appliances while having the following features:

1. Employment of low voltage levels for the PV panel and the battery to avoid concerns pertaining to the safety of personal and equipments.
2. Having minimum number of power conversion stages to increase efficiency and reliability.
3. Incorporation of battery over charge and over discharge protection.
4. Eliminating the requirement of a low frequency transformer to make the system light weight and compact in size.
5. Having simple control strategy to enable the system to operate in all possible modes that are generally encountered in a stand alone system.
6. Assurance of quality of power supplied to the load.

Objective for single phase transformerless grid connected scheme: to develop solar PV based single phase transformer less inverter possessing the following features:

1. Inverter having voltage buck-boost capability.

2. Restriction of leakage current magnitude within permissible limit
3. Maximum power extraction from PV source
4. Elimination of shoot through fault.
5. Optimizing the number of required sensor
6. Avoidance of dc current injection into the grid and limiting the total harmonic distortion of grid current below the permissible limit.

Objective for DMPPT scheme: to propose a DMPPT scheme having the following features:

1. Reduction in the number of sensors required
2. Reduction in the burden of the processor
3. Not having any communication link between converters
4. Simple to implement while ensuring extraction of exact maximum power from series connected modules

1.7 Organization of the Thesis

The work presented in this thesis is organized in six chapters. An introduction to the thesis along with the literature survey of the selected topics of research carried out in this thesis is presented in **Chapter 1**.

Chapter 2 proposes a new boost type of inverter for PV based stand alone schemes. The operating principle of the inverter is presented. The control strategy proposed for the scheme is described. The viability of the scheme is ascertained through detailed simulation and experimental studies.

Chapter 3 presents a two stage stand alone configuration comprising of a high frequency transformer coupled dual-input dc-dc converter (TCDIC) and a standard full bridge inverter. The operating principle of TCDIC is discussed. The control strategy devised for TCDIC is presented. A brief overview of the overall stand alone scheme incorporating the TCDIC is presented. The performance of the scheme is studied in detail by performing elaborate simulation studies on Matlab/Simulink platform. The scheme is validated by performing detailed experimental studies.

Chapter 4 deals with the proposal of a multipurpose neutral point clamped (NPC) single phase transformerless grid connected converter for solar PV application. The versatility of the converter is presented through three schemes. The first scheme deals with the application of the converter in transmitting power extracted from a single PV panel

to the grid. The second scheme elaborates how the same converter can be employed to extract maximum power from two separate PV panels simultaneously while feeding the total extracted power from both the panels to the grid. The third scheme describes how the converter can cater to dc loads in addition to transmitting PV power from a single panel to the grid. The control structure devised for the aforementioned three schemes are presented in detail. The first two schemes are validated through simulation as well as experimental results whereas the third scheme is validated through detailed simulation studies.

Chapter 5 proposes a simple distributed maximum power point tracking (DMPPT) strategy to extract maximum power from individual series connected PV modules experiencing mismatched operating condition. The principle of operation of the scheme and the control strategy for the scheme is presented. The efficacy of the scheme is ascertained by performing detailed simulation studies on Matlab/Simulink platform. The experimental results obtained from scaled down laboratory prototype developed for the purpose confirm the viability of the scheme.

Chapter 6 concludes the thesis summarising the major contributions of this thesis. This chapters also includes the future scope of work that can be inspired from this thesis.

Chapter 2

Stand alone Scheme Based on A Buck-Boost Integrated Full Bridge Inverter (BBIFBI)

2.1 Introduction

The existing PV based stand alone systems employ conventional full bridge voltage source buck type of inverter for dc-ac conversion. Being a buck type of inverter, it requires a voltage to be maintained at its dc link which needs to be higher than the amplitude of the load voltage. For Indian standard in order to maintain a load voltage of 230 V, dc link voltage of the inverter is generally required to be maintained in the range of 350 to 400 V. This necessitates that the effective voltage gain of the intermediate dc-dc converters, which interface the dc link of the inverter with the PV array and battery, to be high. Hence for a PV array voltage of 36 V, the effective gain of the intermediate dc-dc converters required will be in the range of 10 to 12. Such a high gain can be realized by involving several dc-dc converter stages. However, this leads to low efficiency, and reduction in reliability due to increment in the number of converters. Effective gain of the intermediate dc-dc converters can be enhanced by employing high frequency transformer-coupled dc-dc converters wherein minimum number of controlled switches required is six [19]. This is in addition to the four switches that are required to realize the inverter. Further, involvement of two high frequency transformers leads to reduction in efficiency and also increases the size and weight of the system. In order to overcome limitations of the aforementioned schemes, a boost type of inverter can be employed thereby reducing the overall gain requirement from the dc-dc converters. However, the existing boost inverter topologies have the following drawbacks: (a) high switch count (≥ 5) [73], (b) high voltage stress across dc link capacitor [74]-[76], (c) higher number of passive element [74]-[75], and (d) complex control [75]-[76]. In order to overcome the aforementioned

The following papers are published based on the content of this Chapter:

1. D. Debnath and K. Chatterjee, “A Solar Photovoltaic Based Stand Alone Scheme Incorporating a New Boost Inverter,” accepted for publication in IET Power Electronics
2. D. Debnath and K. Chatterjee, “A buck-boost integrated full bridge inverter for solar photovoltaic based stand alone system,” in Proc. IEEE Photovoltaic Specialists conf. (PVSC), pp: 2867- 2872, June 2013.

drawbacks a new boost inverter topology is presented in this chapter. The proposed topology is obtained by integrating a dc-dc buck-boost converter with a full bridge inverter and hence is termed as buck-boost integrated full bridge inverter (BBIFBI). The proposed BBIFBI requires only four controllable switches, one diode, one dc link capacitor and one inductor. The voltage stress experienced by the dc link capacitor remains considerably low compared to that of other boost type inverter topologies. Principle of operation of BBIFBI is presented in the next Section. Subsequently a stand alone scheme is obtained incorporating the BBIFBI. The stand alone system is a three stage one consisting of two dc-dc converters and the BBIFBI. The proposed scheme is transformerless and requires only seven controllable switches. The operational features of the stand alone system along with its allied control philosophy are described in Section 2.3. In order to ascertain the effectiveness of the proposed scheme, detailed simulation studies are carried out, and the simulated performances obtained are presented in Section 2.4. A laboratory prototype of the scheme is developed and detailed experimental studies are carried out to confirm its viability, and the experimental results are presented in Section 2.5.

2.2 Principle of Operation of BBIFBI

In this section the process of derivation of BBIFBI from a combination of a buck-boost dc-dc converter and a full bridge dc-ac inverter is first elaborated. Subsequently the operating principle of BBIFBI is explained. The combination of a buck-boost dc-dc converter and a full bridge dc-ac inverter is depicted in Fig. 2.1. The buck-boost converter of Fig 2.1 is a reconfigured version of the standard buck-boost converter having its input terminals as N and M, and having its output terminals as P and N [77]-[78]. In this converter, the energy from the input source is stored in L which is then subsequently transferred to the capacitor C . When the switch T_1 is on, the inductor, L stores energy from the input source, V_{dc} . When T_1 is turned off energy stored in L is transferred to the output capacitor C through the diode, D . The voltage across L , v_L can be expressed as,

$$\begin{aligned} v_L &= V_{dc}, \text{ when } T_1 \text{ is on} \\ v_L &= -V_c, \text{ when } T_1 \text{ is off} \end{aligned}$$

Assuming continuous conduction mode (CCM) of operation and equating average voltage drop across the inductor, L to be zero, voltage across the capacitor, C can be expressed as

$$V_c = [d/(1-d)]V_{dc} \quad (2.1)$$

wherein d is the duty ratio of the switch T_1 . The dc link voltage of the dc to ac inverter, V_{out} can be expressed as,

$$\begin{aligned} V_{out} &= (V_c + V_{dc}) \\ &= [(d/(1-d)]V_{dc} + V_{dc} \\ &= [1/(1-d)]V_{dc} \end{aligned} \quad (2.2)$$

This expression for V_{out} is same as that to the expression of output voltage of a boost converter operating under CCM having V_{dc} as its input. Therefore, if M and P are considered to be output terminals, the operation of the buck-boost converter shown in Fig. 2.1 resembles to that of a boost converter. The advantages of this configuration of the buck-boost converter over the conventional configuration of boost/buck-boost converter are as follows: (a) the voltage gain requirement from the buck-boost converter is less as gain requirement in this case is $(V_{out} - V_{dc})/V_{dc}$ as compared to (V_{out}/V_{dc}) in case of the conventional topology, (b) the voltage stress across capacitor C is less by an amount $V_{out} - V_{dc}$, and (c) voltage stress across T_1 and D is V_{out} as compared to $(V_{out} + V_{dc})$ for the conventional buck-boost converter. From Fig. 2.1, it can be inferred that the full bridge inverter formed by four switches S_1 through S_4 and having P and M as input terminals, ‘sees’ a boost converter with respect to input voltage V_{dc} . Thus, the scheme shown in Fig. 2.1, can be visualized as a combination of full bridge inverter being fed from a boost converter while having the input dc source connected between terminal, N and M.

The process of combination of the two converters shown in Fig. 2.1 leads to the evolution of the proposed BBIFBI which is shown in Fig. 2.2. In this converter the switches S_1 and S_4 are shared by the buck-boost converter and the full bridge inverter. The diode D is employed to ensure that the power flow through the buck-boost converter segment is unidirectional. From Fig. 2.2 it can be inferred that the dc input to the BBIFBI is ‘ V_{dc} ’ and the ac output of the BBIFBI is ‘ V_o ’. The energy from the input source, V_{dc} is stored in L which is then subsequently transferred to the capacitor C . The inverter segment of BBIFBI sees the dc link as ‘ $V_c + V_{dc}$ ’ and by the inverting action of a standard full bridge inverter, it converts the dc link voltage to the ac voltage across the load terminal. Thus the load is fed from the total dc link voltage of ‘ $V_c + V_{dc}$ ’ wherein V_c is maintained from the energy received from V_{dc} . In the present application of BBIFBI, its input dc voltage V_{dc} (around 50-100 V, to be explained in later Section) is much less than its output ac voltage V_o (=230 V, RMS), and hence the BBIFBI is operated as a boost inverter.

The proposed converter reduces the switch count by one as compared to the scheme

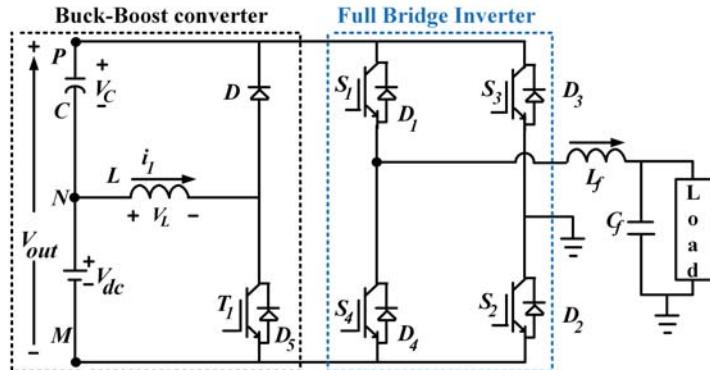


Figure 2.1: Combination of a Buck-boost converter and a full bridge inverter

shown in Fig. 2.1 while preserving all its advantages. The switches, $S_1 - S_4$ of the BBIFBI are controlled in a similar fashion to that of the conventional full bridge inverter employing unipolar sinusoidal pulse width modulation (SPWM).

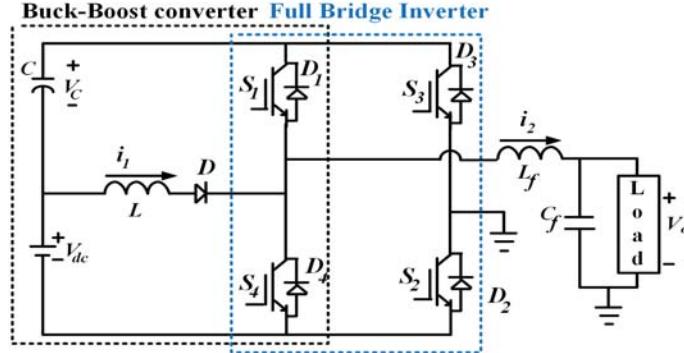


Figure 2.2: Schematic circuit diagram of the proposed BBIFBI

2.2.1 Operation of BBIFBI in positive half cycle

The switching sequence is divided into four switching states, State-1 to State-4. Each of these states are analysed for CCM as well as DCM mode of operation in the following subsections:

A. Operation in Continuous Conduction mode (CCM)

(i) State1 ($S_1 - S_2$ ON): When the initial current flowing through the inductor, L , $i_1(0)$ is greater than the initial current flowing through the inductor L_f , $i_2(0)$, diode D_1 and switch S_2 conduct and the capacitor, C gets charged till i_1 equals i_2 (Fig. 2.3a). Subsequently, C discharges to the load through $S_1 - S_2$, and the energy remaining in L is supplied to the load through S_2 . When $i_1(0) < i_2(0)$, switches S_1 and S_2 conduct while their anti-parallel diodes remain reverse biased. The capacitor, C discharges to the load through $S_1 - S_2$, and the energy stored in L is supplied to the load through S_2 (Fig. 2.3b).

(ii) State2 ($S_2 - S_4$ ON): When $i_1(0) > i_2(0)$, S_2 and S_4 conduct and current in load and L_f freewheels through S_2 and S_4 (ON as $i_1 > i_2$) and L stores energy from V_{dc} via S_4 (Fig. 2.4a). When $i_1(0) < i_2(0)$, D_4 and S_2 conduct (Fig. 2.4b). In this state current in load and L_f freewheels through S_2 and D_4 whereas L stores energy from V_{dc} and i_L increases.

(iii) State3 ($S_1 - S_2$ ON): The situation remains the same as that of state1.

(iv) State4 ($S_1 - S_3$ ON): In this state current flowing through L decreases and the capacitor C is charged. For $i_1(0) > i_2(0)$, D_1 and D_3 conduct (Fig. 2.5a) else S_1 and D_3 conduct (Fig. 2.5b).

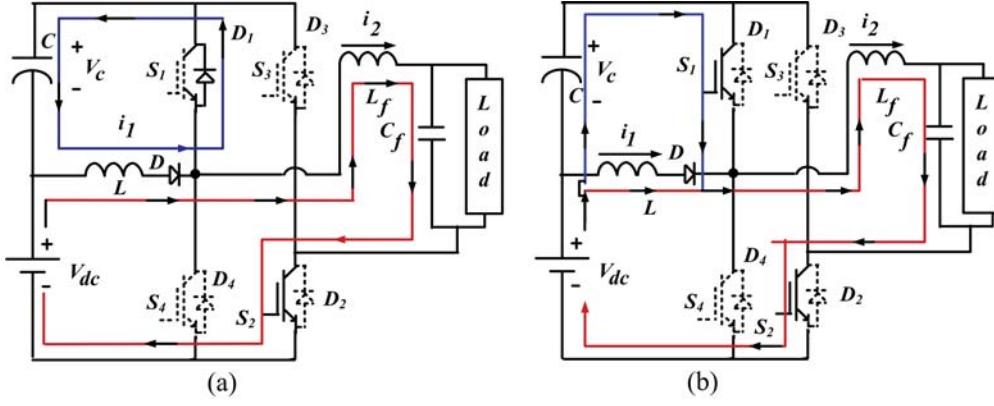


Figure 2.3: Equivalent circuit of BBIFBI in state1; a) D_1 and S_2 conducting, and b) S_1 and S_2 conducting

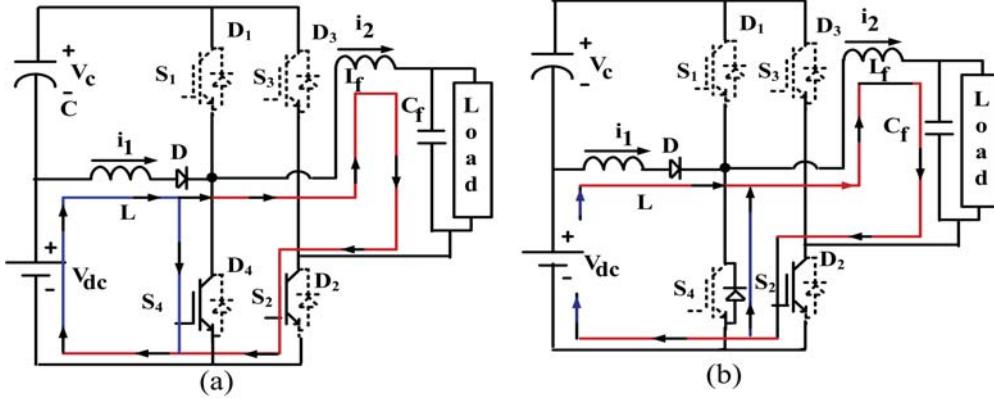


Figure 2.4: Equivalent circuit of BBIFBI in state2; a) S_2 and S_4 conducting, and b) S_2 and D_4 conducting

B. Operation in Discontinuous Conduction mode (DCM)

When the converter operates in DCM, the current i_1 flowing through the inductor, L

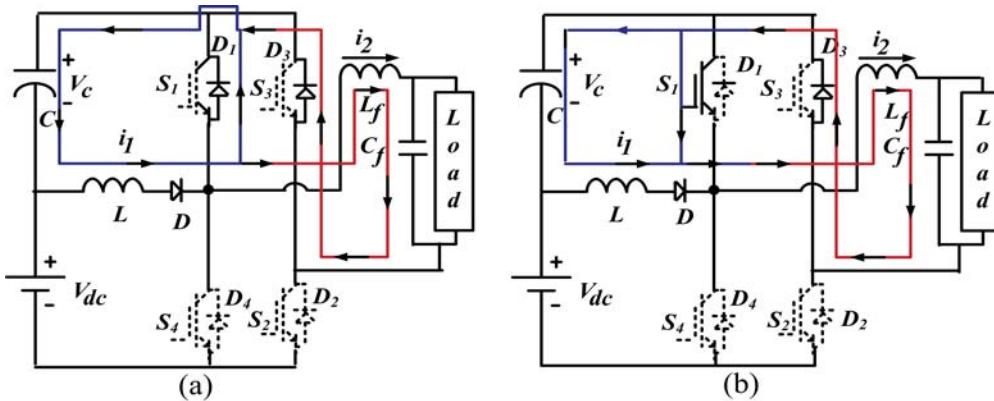


Figure 2.5: Equivalent circuit of BBIFBI in state4; a) D_1 and D_3 conducting, and b) S_1 and D_3 conducting

is greater than zero for some portion and is zero for remaining portion over a switching period. For $i_1 > 0$, the situation remains the same as that of the CCM case. When i_1 becomes zero, D gets reverse biased and the converter behaves similar to that of a standard full bridge inverter.

2.2.2 Operation of BBIFBI in negative half cycle

The switching sequence is divided into four switching states, and are described as follows:

- (i) State 1 ($S_3 - S_4$ ON): When S_3 and S_4 are ON, current flowing through L increases and the capacitor, C gets discharged.
- (ii) State 2 ($S_2 - S_4$ ON): The situation remains the same as that of state2 of the positive half cycle.
- (iii) State 3 ($S_3 - S_4$ ON): The situation remains the same as that of state1 of the negative half cycle.
- (iv) State 4 ($S_3 - S_1$ ON): The situation remains the same as that of state4 of the positive half cycle.

In CCM, the expression for V_c can be obtained by equating the average voltage across the inductor, L to zero which leads to,

$$V_c = \frac{d}{1-d} V_{dc} \quad (2.3)$$

wherein d is the duty ratio of the switch, S_4 and is given by,

$$d = \frac{1 - M \sin wt}{2} \quad (2.4)$$

wherein, M is the modulation index for unipolar SPWM scheme.

The waveform for the inductor current, i_1 in DCM mode is shown in Fig. 2.6. The expression for the inductor voltage in DCM mode is given by,

$$\begin{aligned} v_L &= V_{dc}, \text{ for the interval, } 0 < t < dT_s \\ &= -V_c, \text{ for the interval, } dT_s < t < (d + \Delta)T_s \\ &= 0, \text{ for the interval, } (d + \Delta)T_s < t < dT_s \end{aligned}$$

The peak value of inductor current is given by,

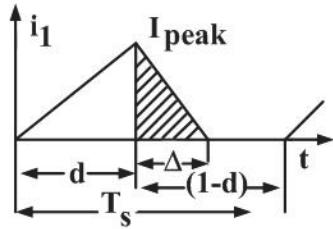


Figure 2.6: Waveform of the inductor current, i_1 in DCM

$$I_{peak} = \frac{V_{dc}}{L} dT_s$$

Equating average voltage across the inductor over a switching cycle to be zero,

$$\Delta = \frac{dV_{dc}}{V_c}$$

The average charging current of the capacitor over a switching cycle, T_s (shown in the shaded portion in Fig. 2.6) is given by,

$$\begin{aligned} I_{chsc} &= \frac{I_{peak}}{2T_s} \Delta T_s \\ &= \frac{V_{dc}^2 d^2 T_s}{2L V_c} \end{aligned} \quad (2.5)$$

Hence the average charging current of the capacitor, C over a power cycle is given by,

$$\begin{aligned} I_{chpc} &= \frac{1}{2\Pi} \int_0^{2\Pi} I_{chsc} d(\omega t) \\ &= \frac{V_{dc}^2}{8LF_s V_c} \left(1 + \frac{M^2}{2}\right) \end{aligned} \quad (2.6)$$

Now, assuming the inverter to be lossless,

$$(V_c + V_{dc}) I_{discharge} = P_l \quad (2.7)$$

wherein $I_{discharge}$ is the average discharging current of the capacitor over a power cycle and P_l is the load power. Now, under steady state condition both the average charging and discharging current of the capacitor are same so as to make the average capacitor current to be zero. Therefore, in steady state,

$$I_{dc} = I_{chpc} \quad (2.8)$$

Combining (2.6), (2.7) and (2.8),

$$V_c = \frac{V_{dc}^3 \left(1 + \frac{M^2}{2}\right)}{8P_{load}LF_s - V_{dc}^2 \left(1 + \frac{M^2}{2}\right)} \quad (2.9)$$

From (2.9), the capacitor voltage, V_c increases with increment in V_{dc} and M , and decreases with increment in P_{load} , L and F_s when the system operates in DCM. As per (2.4), the average value of the duty ratio for the switch, S_4 is 0.5. Therefore, if the buck-boost segment of BBIFBI operates in CCM, the gain of this segment is 2 when the input voltage is V_{dc} and the output voltage is V_{out} as per (3.3) and (2.3). If the buck-boost segment of BBIFBI operates in DCM, the gain of this segment is more than 2 as gain obtained in DCM mode is higher than that of CCM mode. However, from (2.4) it can be noted that duty ratio for switch S_4 varies over a wide range under unipolar SPWM switching scheme and hence a large value of L is required to ensure that the converter operates in CCM whereas a very small value of inductance is required to ascertain its operation in DCM. In order to have operation in CCM the size and weight of the inductor becomes considerable.

However, as DCM operation requires a lower value of inductance, the current rating of the switches, S_1 and S_4 and that of the inductor itself becomes considerable. Therefore, the inverter is intended to operate partly in CCM and partly in DCM over a power cycle. As a result, the overall voltage gain obtained from the buck-boost converter segment is greater than 2. As the duration for which the converter operates in CCM or DCM depends on several parameters, the voltage gain from the buck-boost converter portion is variable and is also difficult to find a closed form expression for it. In order to obtain the rough estimate of the aforementioned gain, the converter is simulated on Matlab/Simulink platform. The variation in gain with respect to different parameters are shown in Fig. 2.7.

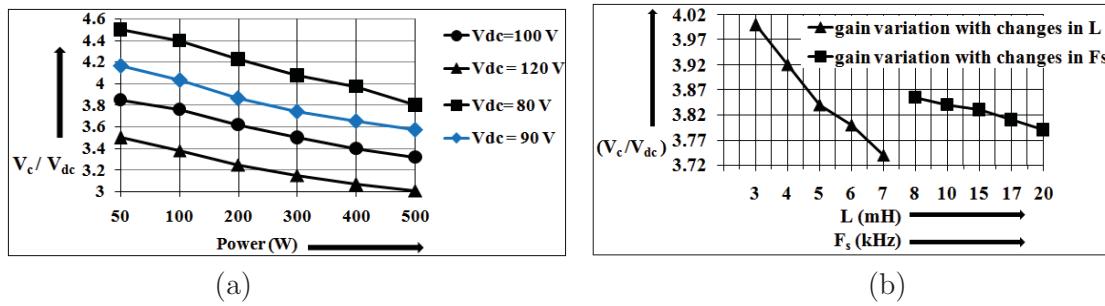


Figure 2.7: Variation of voltage gain of the buck-boost converter segment with respect to, (a) V_{dc} and P_{load} with $L = 6$ mH, $F_s = 20$ kHz, and (b) L and F_s with $V_{dc} = 90$ V, $P_{load} = 250$ W

2.3 Overall Stand Alone Scheme based on BBIFBI and Its Control Structure

Figure 2.8 depicts the schematic circuit diagram of the proposed stand alone scheme being realized by involving BBIFBI. In addition to the BBIFBI, it houses a boost converter to perform MPPT for the PV array and a bidirectional dc-dc converter for charge/discharge control of the battery. The power rating of the system is 500 VA and the voltage level for PV array (at standard test condition) and the voltage of the battery is chosen to be 36 V.

Control of BBIFBI: The inverter segment of the proposed BBIFBI is controlled in a manner similar to that of a conventional full bridge inverter employing proportional integral (PI) based closed loop control. Unipolar SPWM scheme is employed for deriving gating pulses for the four switches of BBIFBI. However, the input voltage seen by the inverter segment is $(V_c + V_{dc})$ as shown in Fig. 2.2. And this voltage has to be more than the peak of sinusoidal load voltage. Since the amplitude of the voltage to be maintained at the load terminal is 325 V ($= 230 * \sqrt{2}$), the minimum value for $(V_c + V_{dc})$ is set at 350 V to account for the voltage drops across the filter inductor and semiconductor devices of BBIFBI. The maximum value for $(V_c + V_{dc})$ is chosen as 400 V so that the

voltage stress on the semiconductor devices is also limited to 400 V. Since the input voltage of BBIFBI, V_{dc} is connected at the output terminals of the boost converter, V_{dc} must be greater than V_{pv} . In order to accommodate the variation in V_{pv} with variation in environmental conditions, the minimum value for V_{dc} is chosen as 50 V. The output voltage of the buck-boost converter segment, V_c is controlled by controlling the input voltage, V_{dc} . A plot depicting the values of V_{dc} required to control V_c at three desired values for different loading conditions is shown in Fig. 2.9. The aforementioned plot is obtained by simulating the BBIFBI on MATLAB/SIMULINK platform utilizing the parameters provided in Table 2.1. These three desired values for V_c are chosen based on the gain profiles shown in Fig. 2.7. From Fig. 2.9 it can be observed that if V_c is maintained at 335 V for $P_{load} < 50W$, at 325 V for $50 < P_{load} < 150W$ and at 300 V for $150 < P_{load} < 500W$ then $(V_c + V_{dc})$ can be maintained in the desired range of 350-400 V and V_{dc} can be maintained at a level higher than 50 V. Neglecting the system losses, the load power demand can be estimated from the following power balance equation,

$$P_{pv} + P_b = P_{load} \quad (2.10)$$

wherein P_{pv} is the PV power output, P_b is the battery power and P_{load} is the load power demand.

The control structure employed to control the capacitor voltage, V_c at the desired value is marked by the dotted rectangle in Fig. 2.10. From this figure it can be noted that V_c is controlled by manipulating V_{dc} .

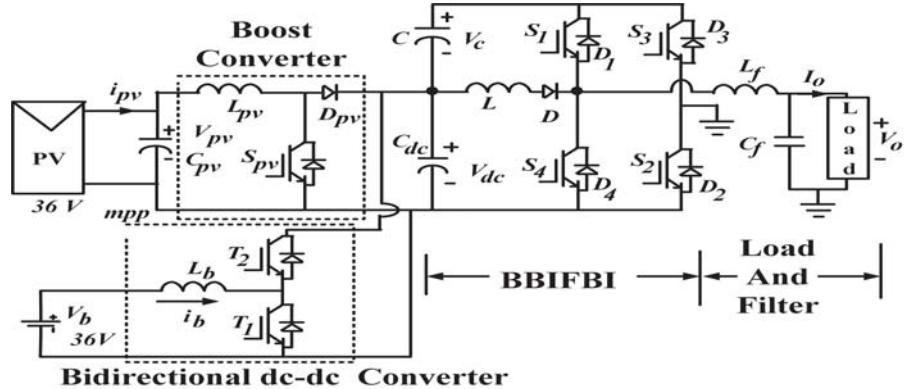


Figure 2.8: Schematic of the overall stand alone system incorporating BBIFBI

Control of boost and bidirectional dc-dc converter: The schematic diagram of the controller employed for the two dc-dc converters of the proposed stand alone scheme is shown in Fig. 2.10. The role of these two converters depends on the mode of operation of the stand alone scheme. The various modes of operation encountered in a stand alone scheme and their selection criterions are discussed in Section 1.2.2. For the present scheme, the selection of a proper mode and shifting of operation among various modes are carried out by the algorithm depicted in Fig. 2.11. This algorithm generates two mode selection signals, MP and non-MP, having magnitude either zero or one. The values of these two signals for different modes are: a) MPP mode: MP=1, non-MP =0; b) non-MPP: MP=0, non-MP =1; c) SD mode: MP=non-MP=0; and d) BO mode: MP=1, non-MP =0.

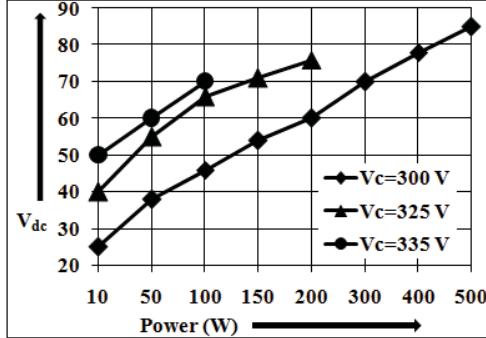


Figure 2.9: Plot showing required values of V_{dc} to maintain V_c at three desired values for different loading conditions

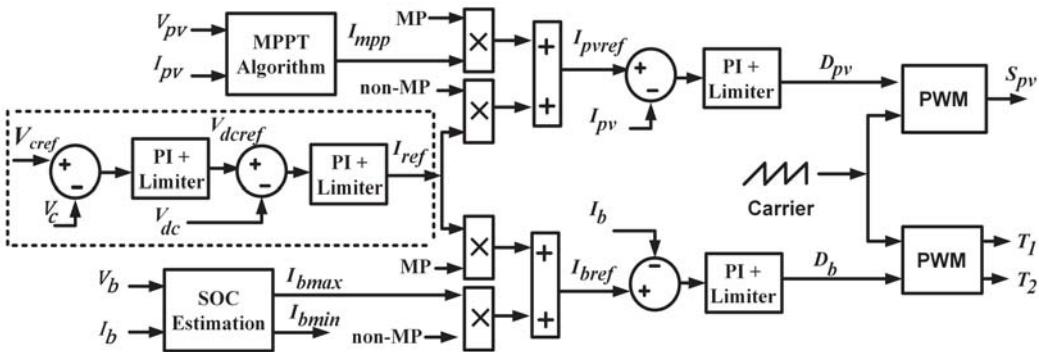


Figure 2.10: Control strategy for the two dc-dc converters of the stand alone scheme

When the system operates either in BO mode or in MPP mode with $p_{mpp} < p_{load}$, battery has to discharge to satisfy the load demand. While discharging, if the battery current becomes greater than its allowable discharge limit, i_{bmin} , the system operation is changed to SD mode to prevent over discharging of the battery. When the system enters in SD mode, gating pulses for all the switches in the stand alone schemes are withdrawn.

When the system operates in MPP mode and $p_{mpp} > p_{load}$, battery is charged with the surplus power ($p_{mpp} - p_{load}$). In order to prevent damage of the battery due to over charging, the charging current of the battery needs to be restricted to its maximum allowable limit, i_{bmax} . Therefore, when the reference current of the battery, i_{bref} tries to exceed i_{bmax} , the system operation is shifted to non-MPP mode by setting MP=0 and non-MP =1 as shown in Fig. 2.11. In non-MPP mode battery is charged with i_{bmax} and v_{dc} is controlled by the boost converter thus bypassing the MPPT algorithm. Power extracted from PV array during non-MPP mode is, $p_{pv} = (v_b * i_{bmax}) + p_{load}$, which is less than p_{mpp} . When the load demand changes during this mode, the PV power gets adjusted accordingly in order to maintain v_{dc} at the required value. If the load demand increases so that PV power falls short of supplying this load demand, the capacitors C and C_{dc} start discharging to meet the load demand, and hence, both v_c and v_{dc} start reducing. Once $(v_c + v_{dc})$ reaches minimum permissible value of 350 V, the system operation is shifted

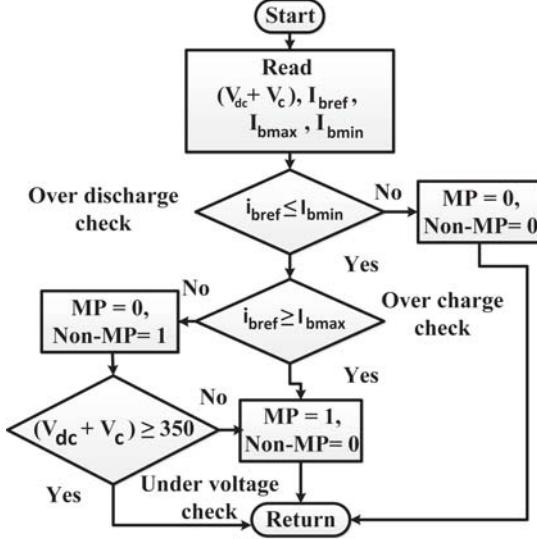


Figure 2.11: Algorithm employed for generating mode selection signals MP and non-MP

Table 2.1: Parameters considered for the Simulation Study

parameter	value
L	5 mH
C, C _{pv}	2000 μ F
L _f , L _b , L _{pv}	2 mH
C _f	5 μ F
F _s	20 kHz
C _{dc}	3000 μ F

to MPP mode by setting MP=1 and non-MP=0. Once the system enters MPP mode, battery converter starts controlling v_{dc} (and hence v_c) whereas boost converter operates to achieve MPP operation of the PV array.

The operation in MPP and BO mode is similar except that the boost converter remains idle in BO mode whereas it is controlled to achieve MPP operation in the MPP mode.

2.4 Simulated Performance

The stand alone system shown in Fig. 2.8 has been simulated on MATLAB/SIMULINK platform. Various system parameters considered for the simulation study are provided in Table 2.1.

The solar modules used in this simulation study have similar electrical characteristics to that of ‘BP 175B’ modules from BP Solar [93]. These are 175 W module and four such modules are connected in parallel to form the solar array. The electrical characteristics of the PV array so formed under standard test condition (STC) are as follows: $P_{mpp} = 700\text{W}$, $V_{mpp}=35.8\text{ V}$, $I_{mpp}=19.55\text{A}$, $V_{oc}=44.2\text{ V}$, and $I_{sc}=21.8\text{ A}$. Perturb and observe

(P & O) algorithm is used for MPPT. The SOC estimation technique for battery is not considered for the simulation study. The limit on the reference for the battery current is set manually assuming that they are generated from the SOC estimation of the battery.

Test 1: operation in MPPT Mode

This test is carried out to observe the performance of the scheme while operating in the MPPT mode with abrupt variation in the level of insolation and the load demand. The maximum limit on the battery charging current is set at 8 A (corresponding P_{bmax} being 288 W) such that the surplus power never exceeds the P_{bmax} and the system operates in MPPT mode only. The results obtained from this test are presented in Fig. 2.12.

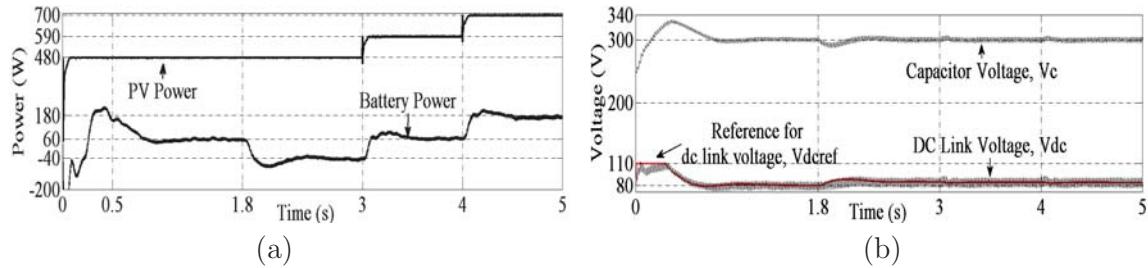


Figure 2.12: Simulated performance of the system under conditions pertaining to test 1. (a) PV and battery power, (b) capacitor voltage, v_c and the dc link voltage, v_{dc} .

Till 1.8 s, the load demand is kept at 400 W whereas insolation level is kept at 0.7 kW/m² (corresponding $P_{mpp} \approx 480$ W). This results in a surplus power of around 60 W (system loss is around 20 W). It can be inferred from Fig. 2.12(a) that PV power is 480 W whereas the battery power settles at 60 W during this period. At 1.8 s, load demand is increased to 500 W and as a result, the capacitor voltage (v_c) falls momentarily to supply this additional power demand (Fig. 2.12(b)). In order to restore v_c , v_{dc} gets increased. To increase v_{dc} at the required value, the battery starts taking less current and finally settles at a value where battery power becomes equal to $(P_{mpp} - P_{load} - P_l)$ which is -40 W. At 3 s, the insolation level is increased to 0.85 kW/m² (corresponding $P_{mpp} \approx 590$ W). This results in an increment in the v_c which is then brought down to its desired value by increasing the battery current (and hence the power consumed by the battery). At 4 s insolation level is further increased to 1 kW/m² (corresponding $P_{mpp} \approx 700$ W) and a similar sequence of events follows.

Test 2: operation in non-MPPT Mode

This test is carried out to observe the performance of the scheme while operating in non-MPPT mode. The level of insolation is kept fixed at 1 kW/m² (corresponding $P_{mpp} \approx 700$ W). The maximum limit on battery charging current is set as: 2 A (corresponding $p_{bmax} = 72$ W) till 3.5 s and 0 A after 3.5 s. The load demand is set such that the resulting

surplus power is more than the p_{bmax} to operate the system in non-MPPT mode. The results obtained from this test are presented in Fig. 2.13.

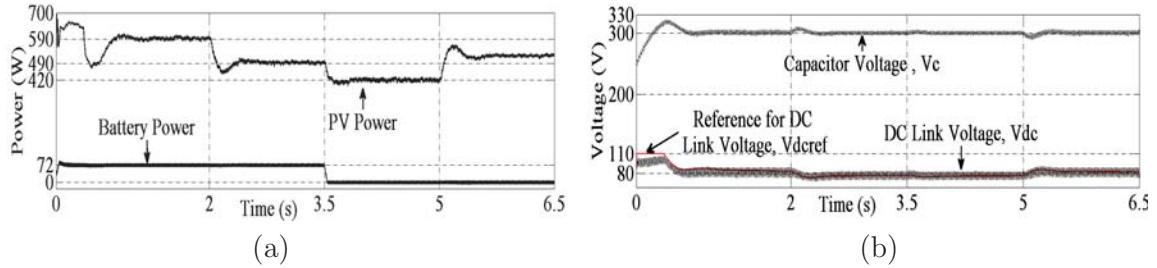


Figure 2.13: Simulated performance of the system under conditions pertaining to test 2. (a) PV and battery power, (b) capacitor voltage, V_c and the dc link voltage, V_{dc} .

Till 2 s the load demand is kept at 500 W. It can be inferred from Fig. 2.13(a) that the PV power gets settled at around 590 W during this condition which is equal to the $(p_{bmax} + p_{load} + p_l)$. At 2 s, the load demand is reduced by 100 W and as a result the PV power is also reduced by the same amount. At 3.5 s, the i_{bmax} is set to zero thereby reducing the power consumption of the battery to zero. As the load demand is still kept at 400 W the PV power is reduced to 420 W. At 5 s, the load demand is increased by 100 W and as a consequence the PV power is also increased by the same amount. It can be observed from Fig. 2.13(b) that the capacitor voltage is maintained at 300 V by adjusting the dc link voltage, v_{dc} .

Test 3: Mode change between MPPT and non-MPPT

The third test is carried out to observe the performance of the scheme during mode change from MPPT to non-MPPT and vice-versa. The battery charging current limit is set at 5 A with corresponding p_{bmax} as 180 W. The level of insolation is kept fixed at 0.8 kW/m² (corresponding $P_{mpp} \approx 550$ W). The results obtained from this test are presented in Fig. 2.14.

Till 1.8 s the load demand is kept at 500 W. This results in a surplus power around 30 W which is less than p_{bmax} and hence the system operates in MPPT mode. It can be inferred from the Fig. 2.14(a) that the PV power is 550 W and the battery power is around 30 W till 1.8 s as per expectation. At 1.8 s, the load demand is reduced to 300 W which results in a surplus power of around 230 W. This excess power starts getting dumped into the battery to maintain MPPT operation and soon the battery reaches its maximum charging current limit, i_{bmax} . At this point the signal MP becomes zero (non-MP becomes 1) and the system enters into the non-MPPT mode. It can be inferred from Fig. 2.14(a) that once the system enters into the non-MPPT mode the battery power is restricted at 180 W whereas the PV power is reduced to 500 W which is equal to $(p_{bmax} + p_{load} + p_l)$. At 3.5 s, the load demand is increased to 500 W. Since the battery is consuming 180 W, the PV power falls short to meet the load demand (as P_{mpp} for the set insolation level

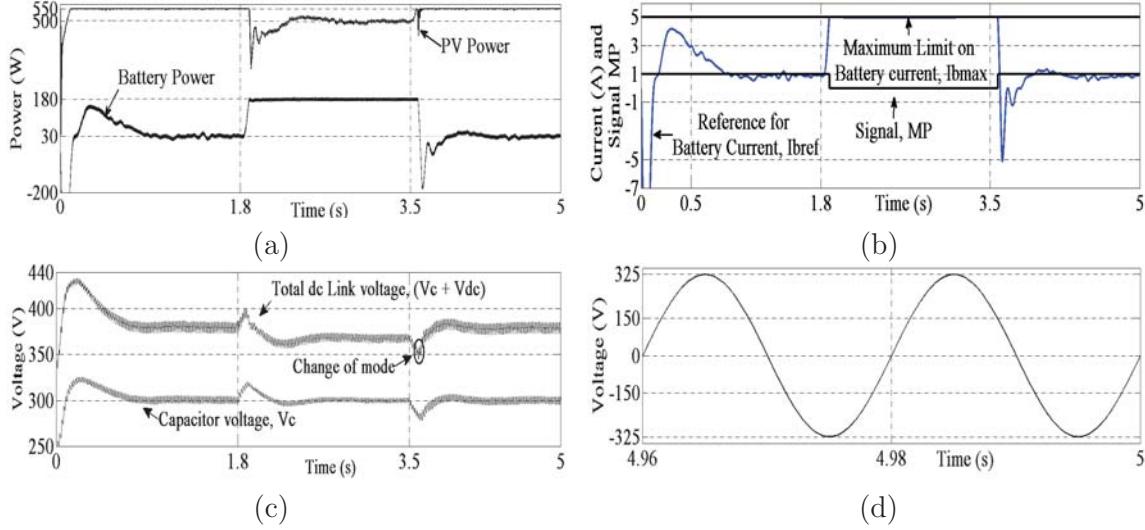


Figure 2.14: Simulated performance of the system under conditions pertaining to test 3, (a) PV and battery power, (b) Reference and maximum charging limit for the battery current; the control signal MP, (c) filtered value of the total dc link voltage, ($V_{dc} + V_c$), and (d) steady state profile of the ac load voltage.

is 550 W). In order to meet this additional demand, C and C_{dc} starts discharging and hence the total dc link voltage starts falling. Once this total dc link voltage reaches its lower permissible limit, i.e. 350 V, the signal MP becomes 1 and the mode of operation is shifted to MPPT from non-MPPT (Fig. 2.14c). It can be observed from Fig. 2.14(a) that the PV power attains its maximum value after 3.5 s indicating that the system is now operated in MPPT mode. The steady state profile of the load voltage is shown in Fig. 2.14(d).

From the aforementioned three tests it can be concluded that the proposed control strategy is suitable for operating the stand alone system in MPPT as well as in non-MPPT mode. It also allows smooth transition between these two modes by generating proper values for the signals MP and non-MP. On the other hand the capacitor voltage, v_c is also made controllable by manipulating the dc link voltage v_{dc} and hence it is possible to maintain the effective dc link voltage, i.e. $(v_{dc} + v_c)$ within the desired range of 360-400 V which is required to control the load voltage at 230 V.

2.5 Experimental Validation

The experimental validation of the scheme is carried out by utilizing a laboratory prototype developed for the purpose. The battery bank is formed by connecting three 12 V, 7 Ah batteries in series. Agilent make solar array simulator, E4360A is employed to emulate the solar array. This simulator generates I-V characteristics for the PV array based on four input commands, viz. V_{mpp} , V_{oc} , I_{mpp} , and I_{sc} . The ac loads at the inverter output are realized by employing incandescent bulbs of different ratings. The digital

control platform required to implement the control structure of the proposed scheme is realized by employing Texas Instruments floating-point DSP, TMS320F28335. The semiconductor devices employed in the prototype are as follows: (i) switches, S_{pv} , T_1 , and T_2 : IRFP4668PbF (MOSFET, 200 V, 90 A), (ii) diode, D_{pv} : DSEI60-02a (200 V, 60 A), (iii) diode, D : STTH6010 (1000 V, 60 A), and (iv) four switches of the inverter: BSM75GB120 DN2 (IGBT, 1200 V, 75 A). Other relevant parameters/elements used to realize the prototype remain the same as those used for carrying out simulation study, and are provided in Table 2.1.

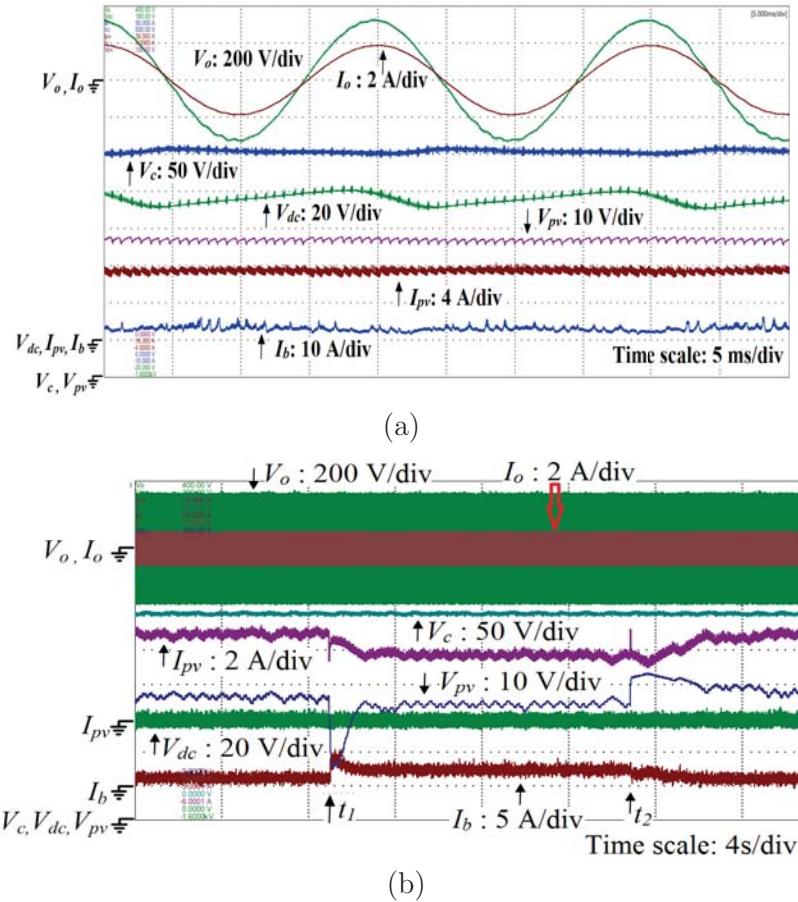


Figure 2.15: Experimental results: (a) steady state response of the system while operating in MPP mode and (b) response of the system subjected to changes in PV operating condition while operating in MPP mode

The steady state response of the system while operating in MPP mode and negotiating 300 W load is shown in Fig. 2.15(a). The MPP values for the PV array are set at $V_{mpp} = 36V$ and $I_{mpp} = 7A$. From Fig. 2.15(a) it can be inferred that the PV voltage and current attain their prescribed values indicating operation of the system in MPP mode. Further, the capacitor voltage, v_c is maintained at 300 V as v_{dc} is being maintained at 76 V. The ac load voltage is controlled at 230 V and is sinusoidal. The battery is discharged to meet the load demand.

The response of the system while it is being subjected to changes in PV operating condition while operating in MPP mode is shown in Fig. 2.15(b). The load demand is kept fixed at 160 W. The changes in PV operating condition is realized by providing step changes in the MPP values, V_{mpp} and I_{mpp} of the solar array simulator. The values of V_{mpp} and I_{mpp} are set as follows: 36 V and 5 A till the instant t_1 , 34 V and 4 A during the interval t_1 to t_2 , and 36 V and 5 A beyond t_2 . From Fig. 2.15(b) it can be observed that the system tracks new set point of the MPP satisfactorily.

The response of the system subjected to step changes in load demand while operating in MPP mode is shown in Fig. 2.16(a). The MPP values for the PV array are kept fixed at $V_{mpp} = 34$ V and $I_{mpp} = 3$ A. The changes in load demand are done as follows: 100 W till instant t_1 , 160 W during the interval t_1 to t_2 , and 100 W beyond t_2 . From Fig. 2.16(a) it can be noted that the PV operating points are maintained at their respective MPP points irrespective of step changes in the load demand. The battery current gets adjusted to accommodate the load demand. The capacitor voltage, v_c is maintained at 300 V as v_{dc} is being properly adjusted. The load voltage is controlled satisfactorily at 230 V irrespective of step changes in load demand.

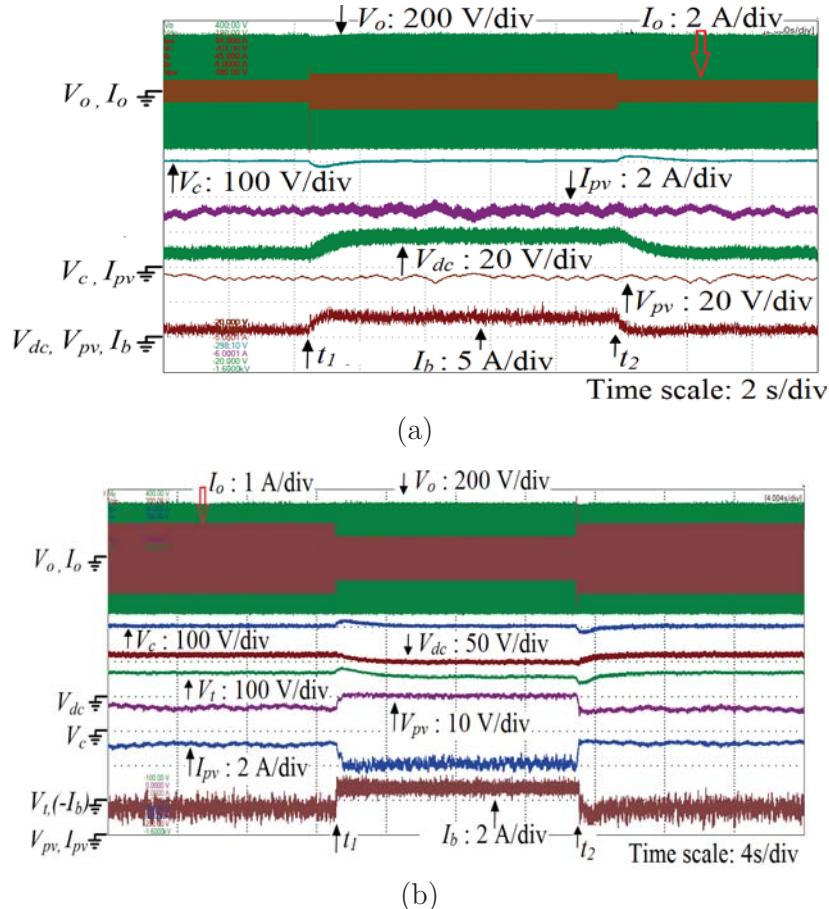


Figure 2.16: Experimental results: (a) response of the system subjected to step changes in load demand while operating in MPP mode and (b) performance of the system during mode transition between MPP and non-MPP mode

The performance of the system during mode transition between MPP and non-MPP mode is shown in Fig. 2.16(b). The maximum allowable charging current for the battery is set at 1 A. The MPP values of the PV array are set at $V_{mpp} = 35$ V and $I_{mpp} = 5$ A. Initially the load demand is set at 160 W and the system operates in MPP mode and it can be observed that the battery is getting discharged during this period. At instant t1, the load demand is reduced to 100 W. As a result surplus power from PV starts charging the battery. As soon as the charging current of the battery reaches 1 A, the system enters into non-MPP mode. This can be confirmed from Fig. 2.16(b) by noting that as and when the charging current of the battery gets restricted to 1 A, the PV operates at a point other than that of its MPP thereby reducing PV output power yield. At instant t2, the load demand is increased to 160 W and the operation of the system gets shifted to MPP mode.

The efficiency curve measured form the laboratory prototype is shown in Fig. 4.25. Following formula is employed to calculate the efficiency,

$$efficiency = \frac{P_{load}}{P_{pv} + P_b}$$

The load power, P_{load} is measured by employing Voltech make single phase power analyzer, PM100 at the load terminal. The PV power, P_{pv} is obtained from the PV simulator display. The battery power, P_b is obtained by measuring battery voltage through a multimeter and the battery current is measured by employing an Ammeter.

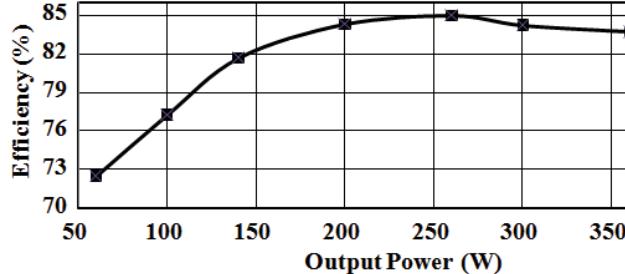


Figure 2.17: Efficiency curve measured form the laboratory prototype

A comparison of the proposed BBIFBI with typical boost type inverters is provided in Table 2.2. From this table it can be concluded that BBIFBI is advantageous in most of the attributes whereas it is comparable with its counterparts in the remaining attributes. A comparison of the proposed stand alone system with typical stand alone systems are presented in Table 2.3. From this comparison it can be inferred that the efficiency of the proposed scheme is comparable with the existing stand alone scheme. However, the proposed scheme requires least number of switches and do not require the service of transformer. Hence it can be considered as a preferable candidate for solar PV based stand alone systems.

Table 2.2: comparison of BBIFBI with typical boost type inverter

Topology	V_{cmin}	n_c	n_L	complexity	n_d
[74]	$(V_{op} + V_{dc})$	2	2	moderate	0
[75]	V_{op}	2	2	complex	1
[76]	V_{op}	1	1	moderate	2
[73]	$(V_{op} + V_{dc})$	-	2	moderate	3
BBIFBI	$(V_{op} - V_{dc})$	1	1	simple	1

V_{cmin} = Minimum voltage stress across dc capacitor, n_c = No. of dc capacitor, n_L = No. of inductors, n_d = number of diodes, V_{op} = peak value of load voltage and V_{dc} = input voltage to the inverter

Table 2.3: Comparison of the proposed scheme with typical stand alone schemes

Scheme	No. of stages	n_S	n_D	n_T	n_L	n_C	Peak efficiency
Chen [18]*	3	9	0	1	5	6	90**
Chen [80]*	3	12	12	1	3	2	91**
Mutoh [84]	4	#	#	1	#	#	#
Chattopadhyay [79]	3	8	2	1	3	6	#
Hu[81]	3	8	4	2	2	4	#
proposed scheme	3	7	2	0	4	4	84.5

n_S = no. of switches, n_D = no. of diodes, n_T = no. of transformer, n_L = no. of inductors, n_C = no. of capacitors, * = as no dc to ac converter is provided a full bridge inverter is added to achieve dc-ac conversion and to maintain uniformity in comparison; # = data inadequate; ** = efficiency obtained in the absence of dc-ac inverter.

2.6 Conclusion

A solar PV based stand alone scheme incorporating a new boost type inverter is presented in this chapter. This new boost inverter is derived by integrating a buck-boost dc-dc converter and a full bridge inverter. The salient features of the proposed inverter as compared to existing boost inverter topologies are: (a) minimum possible requirement in the number of semiconductor devices, (b) minimum requirement for passive elements, (c) reduced voltage stress across dc link capacitor, and (d) reduced voltage gain requirement from the equivalent dc-dc buck-boost converter associated with the inverter. The inclusion of the proposed inverter has led to the development of a three stage stand alone scheme which requires only seven controllable switches. The scheme also allows the use of low voltage levels for the PV array and the battery thereby eliminating concerns pertaining to the use of high voltage levels for them. The control structure of the overall stand alone scheme is presented and is validated through detailed simulation studies. The efficacy of the scheme is ascertained by performing exhaustive experimental validation on a laboratory prototype of the stand alone scheme.

Chapter 3

Transformer Coupled Dual-Input converter based Two Stage Stand alone Scheme

3.1 Introduction

The BBIFBI based stand alone scheme involving three conversion stages which is proposed in the previous Chapter employs a dedicated dc-dc boost converter to achieve maximum power point tracking operation. The presence of this dedicated dc-dc converter leads to the following limitations: (a) this dc-dc converter needs to process the entire PV power as it is placed in the cascaded path thereby reducing the efficiency of the overall system, (b) the utilization of this converter is very poor as it remains idle at least for half a day when there is no PV power, and (c) reduction in battery charging efficiency as two converters are present in the charging path of the battery. In order to eliminate this dc-dc converter along with its allied limitations, the converter configuration presented in [87] - [90] wherein the PV panel is placed in series with the battery seems to be a solution. However, the magnitude of the output voltage of this converter is equal to the sum of the voltages of PV panel and the battery, and this voltage is generally designed to be low. To boost this voltage to the desired level service of another dc-dc converter becomes necessary. The involvement of this additional converter will increase the device count and will also reduce the efficiency of the overall stand alone scheme. In order to address this issue, a transformer coupled dual input converter (TCDIC) is proposed in this chapter. The unique feature of TCDIC is that it can ensure MPPT operation, battery charge control and voltage boosting by employing a proper control algorithm. Hence all of the facilities that are achieved in the existing stand alone schemes by involving two or more stages of dc-dc converters, can be obtained by employing the proposed single stage TCDIC. A standard full bridge inverter is employed at the output of TCDIC to achieve

The following papers are published based on the content of this Chapter:

1. D. Debnath and K. Chatterjee, "A Two Stage Solar Photovoltaic based Stand Alone Scheme having Battery as Energy Storage Element for Rural Deployment," *IEEE Trans. on Indus. Electron.*, vol. 62, no. 7, pp. 4148-4157, July 2015.
2. D. Debnath and K. Chatterjee, "Transformer coupled multi-input two stage stand alone solar photovoltaic scheme for rural areas," in *Proc. IEEE Indus. Electron. Society Conf. (IECON)*, pp. 7028- 7033, Nov. 2013.

dc-ac conversion. The stand alone system thus obtained is a two stage one requiring only six controllable switches. The operating principle of TCDIC is presented in the following section. Small signal based mathematical modeling of the TCDIC is presented in Section 3.3. Related design constraints of the TCDIC are discussed at length in Section 3.4. The control strategy devised for the overall stand alone scheme is presented in Section 3.5. Performance features obtained from detailed simulation studies carried out to ascertain the viability of the proposed overall stand alone scheme are presented in Section 3.6. A laboratory prototype for the proposed stand alone scheme is developed and relevant experimental results obtained from the prototype are presented in Section 3.7.

3.2 Operating Principle of TCDIC

The schematic diagram of the TCDIC is depicted in Fig. 3.1. From this figure it can be noted that no dedicated converter is employed for ensuring MPP operation of the PV panel which leads to the improved utilization of the converters involved. Further, only one converter stage is present in the path between the PV panel and the battery thereby improving the charging efficiency of the battery. From Fig. 3.1 it can be observed that the segment of the TCDIC formed by PV, battery, L , S_1 , and S_2 is basically a reconfigured version of a standard buck-boost dc-dc converter. Since both S_1 , and S_2 have bidirectional current carrying capability, this buck-boost converter operates as a bi-directional converter which allows charging as well as discharging of the battery. By controlling charging and discharging of the battery the MPP operation of the PV, and the protection of the battery from being overcharge or over discharge can be carried out. The primary of the transformer is applied with both positive ($V_b + V_{pv}$) and negative dc voltage ($= -V_{c1}$) at switching frequency. Thus at the secondary of the transformer bidirectional voltage will be induced. To achieve a dc voltage output, a rectifier stage is incorporated at the secondary terminal of the transformer. The rectifier employed here is the conventional voltage doubler rectifier which is utilized to achieve high voltage boosting.

In TCDIC, the switches S_1 and S_2 are operated in complementary fashion. The current, i_L flowing through the inductor L is designed to be continuous. All semiconductor devices and passive elements are assumed to be ideal in the following analysis.

3.2.1 Operation of the converter when inductor current is positive

The waveforms of the currents flowing through, and voltages across different key circuit elements of TCDIC, while the current flowing through the inductor, L is positive, are shown in Fig. 3.2(a). The various possible switching modes during this condition are analyzed in this subsection.

(a) Mode I (0 to t1; S_1 and D_3 conducting): when S_1 is turned on, the PV panel voltage, v_{pv} is impressed across L and the inductor current, i_L increases. During this period, the voltage impressed across the primary winding of the transformer is, $v_{pri} = (v_{pv} + v_b - v_{C1})$, wherein v_b is the battery voltage and v_{C1} is the voltage across the capacitor,

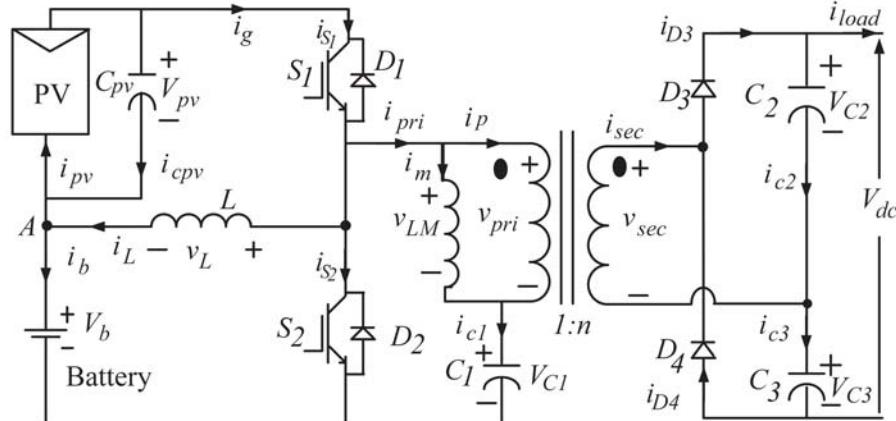


Figure 3.1: Schematic circuit diagram of TCDIC

C_1 . Hence the primary current of the transformer, i_{pri} increases and the capacitor, C_1 gets charged. The current flowing through the secondary winding of the transformer, i_{sec} also increases. The diode, D_3 is forward biased and the capacitor, C_2 gets charged. The voltage across C_2 is given by, $v_{C_2} = n(v_{pv} + v_b - v_{C_1})$, wherein n is the turns ratio of the transformer. The equivalent circuit diagram of TCDIC during this mode is shown in Fig. 3.3.

(b) Mode II (t1 to t2; D_2 and D_4 conducting): This mode begins when S_1 is turned off and S_2 is turned on. At the starting of this mode, i_L is positive and as S_1 is turned off i_{pri} is zero. Since $i_L > i_{pri}$, the diode D_2 starts conducting. The voltage impressed across L is, $v_L = -v_b$ and hence i_L starts decreasing. The voltage impressed across the primary winding of the transformer is, $v_{pri} = -v_{C_1}$ and hence i_{pri} becomes negative and starts decreasing thereby discharging C_1 . The current flowing through the secondary winding of the transformer, i_{sec} reverses and the diode D_4 gets turned on. The capacitor C_3 is getting charged and the voltage across C_3 can be expressed as $v_{C_3} = n(v_{C_1})$. During this mode, $i_L > (-i_{pri})$ and diode D_2 is forward biased. This mode continues till i_L becomes equal to $(-i_{pri})$. The equivalent circuit diagram of TCDIC during this mode is shown in Fig. 3.4(a).

(c) Mode III (t2 to t3; S_2 and D_4 conducting): When i_L becomes smaller than $(-i_{pri})$ the diode D_2 is reverse biased and the switch, S_2 starts conducting. The rest of the operation remains the same as that of mode II. The equivalent circuit diagram of TCDIC during this mode is shown in Fig. 3.4(b).

3.2.2 Operation of the converter when inductor current is negative

The waveforms of the currents flowing through, and voltages across different key circuit elements of TCDIC, while the current flowing through the inductor, L is negative, are shown in Fig. 3.2(b). The various possible switching modes during this condition are analyzed in this subsection.

(a) Mode I (0 to t1; D_1 and D_3 conducting): This mode begins when S_1 is turned on

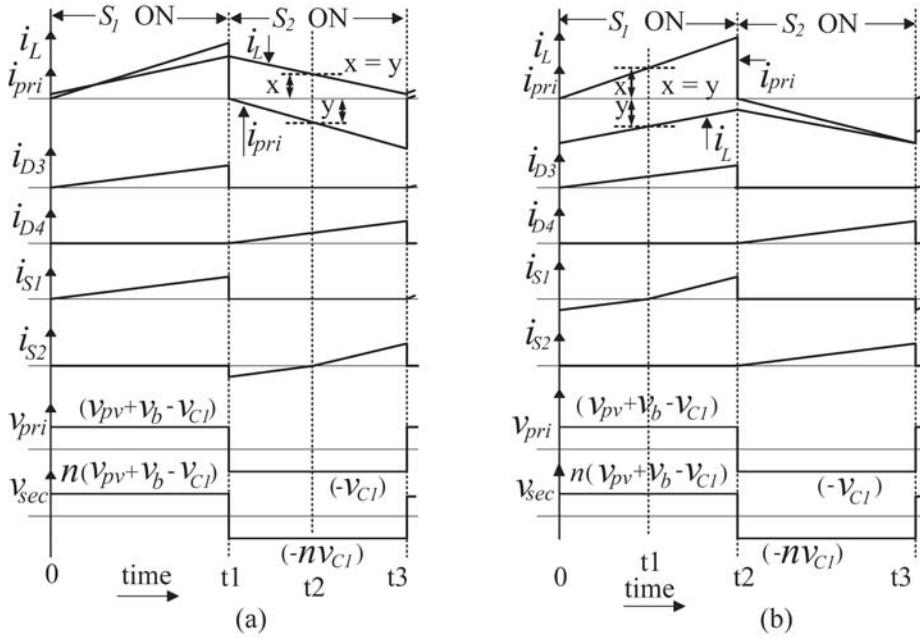


Figure 3.2: Waveforms of currents flowing through and voltage across different key circuit elements of TCDIC when: a) i_L is positive and b) i_L is negative

and S_2 is turned off. At the starting of this mode, i_L is negative and i_{pri} is zero. Hence the diode D_1 starts conducting. The rest of the operation is same as that of mode I discussed in the previous subsection. This mode continues till i_{pri} becomes equal to $(-i_L)$. The equivalent circuit diagram of TCDIC during this mode is shown in Fig. 3.5(a).

(b) Mode II (t1 to t2; S_1 and D_3 conducting): When i_{pri} becomes greater than $-i_L$ the diode D_1 is reverse biased and the switch, S_1 starts conducting. The rest of the operation is same as that of mode I discussed in the previous subsection. The equivalent circuit diagram of TCDIC during this mode is shown in Fig. 3.5(b).

(c) Mode III (t2 to t3; S_2 and D_4 conducting): This mode begins when S_1 is turned off and S_2 is turned on. During this mode, both i_L and i_{pri} are negative and the switch S_2 conducts. The negative current in the primary winding of the transformer results in negative current in the secondary winding of the transformer. Hence the diode D_4 is forward biased and the capacitor C_3 gets charged. During operation in this mode, $v_L = -v_b$, $v_{pri} = -v_{Cl}$ and $v_{C3} = nv_{Cl}$. The equivalent circuit diagram of TCDIC during this mode is same as that shown in Fig. 3.4(b) except that the direction of i_L is reversed.

From Fig. 3.1, the voltage, v_L across the inductor, L can be expressed as,

$$\begin{aligned} v_L &= v_{pv}, \text{ when } S_1 \text{ is on} \\ v_L &= -v_b, \text{ when } S_2 \text{ is on} \end{aligned} \quad (3.1)$$

Therefore, the average voltage drop across the inductor is,

$$V_L = dV_{pv} - (1-d)V_b$$

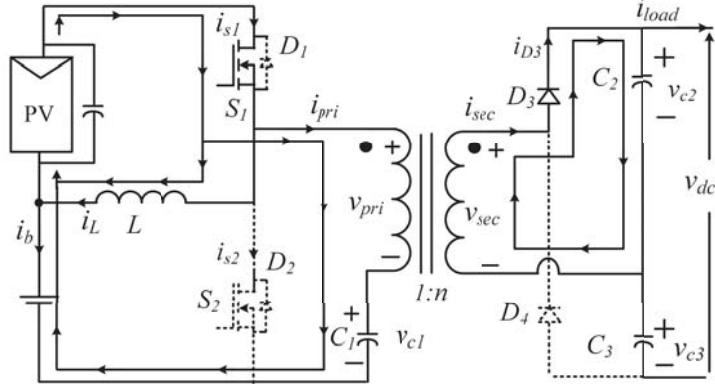


Figure 3.3: Equivalent circuit diagram of TCDIC when operating in mode I and inductor current is positive

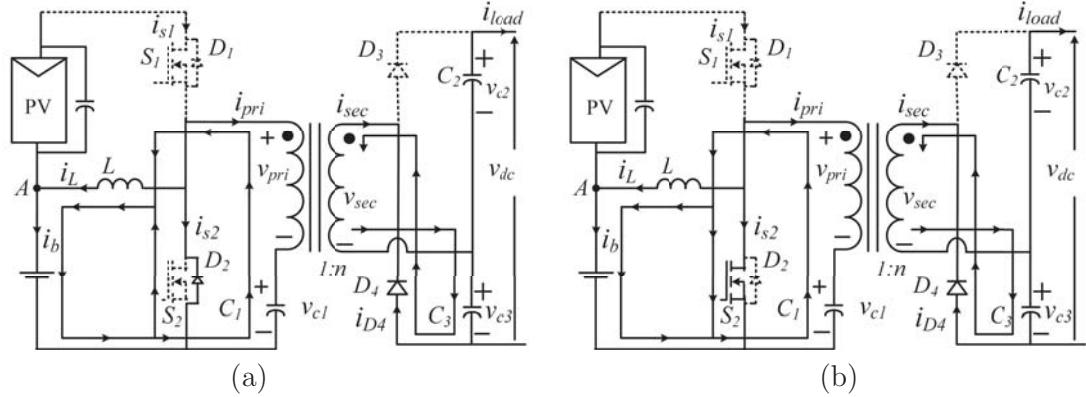


Figure 3.4: Equivalent circuit diagrams of TCDIC when inductor current is positive: a) mode II, and b) mode III

wherein d is the duty ratio of the switch S_1 . Equating average voltage drop across the inductor to zero,

$$V_{pv} = [(1 - d)/d]V_b \quad (3.2)$$

From (3.2) it can be inferred that the PV voltage can be controlled by manipulating d as battery voltage v_b can be assumed to be a stiff source. Therefore, MPPT operation of PV panel can be achieved through a proper manipulation of d .

The average output voltage of the TCDIC, V_{dc} is given by,

$$\begin{aligned} V_{dc} &= (V_{C_2} + V_{C_3}) \\ &= [n(V_b + V_{pv} - V_{C_1}) + nV_{C_1}] \\ &= n(V_b + V_{pv}) \end{aligned} \quad (3.3)$$

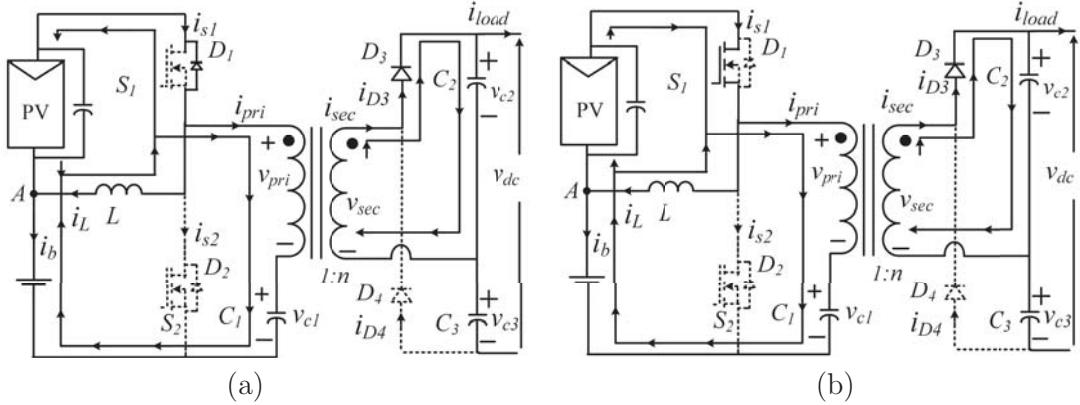


Figure 3.5: Equivalent circuit diagrams of TCDIC when inductor current is negative: a) mode I, and b) mode II

Applying KCL at point A of Fig. 3.1,

$$i_L + i_{cpv} = i_b + i_{pv} \quad (3.4)$$

Considering the average values of i_L , i_{cpv} , i_b , and i_{pv} over a switching cycle and noting that $\bar{i}_{cpv} = 0$, (3.4) transforms to

$$\bar{I}_b = \bar{I}_L - \bar{I}_{pv} \quad (3.5)$$

From (3.5) it can be noted that for $\bar{I}_L > \bar{I}_{pv}$, the battery is charged and for $\bar{I}_L < \bar{I}_{pv}$, the battery is discharged. Therefore, by controlling I_L , for a given I_{pv} , battery charging and discharging can be controlled. The details of the control strategy devised for TCDIC is discussed in section V.

3.3 Small Signal based Mathematical Model of TCDIC

A small signal mathematical model of the TCDIC is derived so that it can be utilized to design the closed loop controllers [95]. Following notations are used for developing the model: \bar{x} is average value of variable x over a switching cycle while X is its steady state value, and \hat{x} represents small signal perturbation of x around its steady state value X . The equations describing the steady state behaviour of the system are:

$$\begin{aligned} \bar{v}_L &= d\bar{v}_{pv} - (1-d)\bar{v}_b \\ \bar{i}_{Cpv} &= \bar{i}_{pv} - \bar{i}_g = \bar{i}_{pv} - d(\bar{i}_L + \bar{i}_{pri}) \\ \bar{v}_{LM} &= (\bar{v}_b + \bar{v}_{pv} - \bar{v}_{C1})d - \bar{v}_{C1}(1-d) \\ \bar{i}_{C1} &= \bar{i}_{pri} = \bar{i}_m + \bar{i}_p \\ \bar{i}_{C2} &= \frac{\bar{i}_p}{n}d - \bar{i}_{load} \end{aligned}$$

$$\begin{aligned}
\bar{i}_{C3} &= -\bar{i}_{Load} = (1-d)\left(\frac{\bar{i}_p}{n}\right) \\
\bar{i}_{C2} + \bar{i}_{C3} &= \frac{\bar{i}_p}{n} - 2\bar{i}_{load} \\
&= C_2 \frac{d\bar{v}_{C2}}{dt} + C_3 \frac{d\bar{v}_{C3}}{dt}
\end{aligned}$$

Since $[C_2 = C_3 = C]$,

$$\begin{aligned}
C \frac{d(\bar{v}_{C2} + \bar{v}_{C3})}{dt} &= \frac{\bar{i}_p}{n} - 2\bar{i}_{load} \\
C \frac{d\bar{v}_{dc}}{dt} &= \frac{\bar{i}_p}{n} - 2\bar{i}_{load}
\end{aligned}$$

In order to linearize the system, a small perturbation is applied around a steady state point so that all the following variables, d , v_{pv} , i_{pv} , i_L , i_{pri} , i_m , i_p , i_{load} , i_{c1} , i_{c2} , i_{c3} , and v_{dc} get perturbed in the following form:

$$x = X + \hat{x}$$

wherein $\hat{x} \ll X$. The linearised system equations are as follows:

$$Ls\hat{i}_L = D\hat{v}_{pv} + (v_{pv} + v_b)\hat{d} \quad (3.6)$$

$$\hat{v}_{pv}[sC_{pv} + \frac{1}{R_{pv}}] = -\hat{d}(I_L + I_{pri}) - D(\hat{i}_L + \hat{i}_{pri}) \quad (3.7)$$

$$sL_m \frac{d\hat{i}_m}{dt} = (v_b + v_{pv})\hat{d} + \hat{v}_{pv}D - \hat{v}_{c1} \quad (3.8)$$

$$\hat{i}_{c1} = \hat{i}_m + \hat{i}_p \quad (3.9)$$

$$sC_2\hat{v}_{c2} = \hat{i}_{c2} = \frac{1}{n}[D\hat{i}_p + I_p\hat{d}] - \hat{i}_{Load} \quad (3.10)$$

$$sC_3\hat{v}_{c3} = \hat{i}_{c3} = \frac{1}{n}[(1-D)\hat{i}_p - \hat{d}I_p] \quad (3.11)$$

$$\hat{v}_{dc}[Cs + \frac{2}{R}] = \frac{1}{n}\hat{i}_p \quad (3.12)$$

wherein, $R = V_{dc}/I_{load}$ and $R_{pv} = -(V_{pv}/I_{pv})$. The required transfer functions are obtained by solving equations (3.6)-(3.12) and are provided below:

$$\begin{aligned}
\frac{\hat{v}_{pv}}{\hat{d}}|_{\hat{v}_0=0} &= -\frac{LCL_m I_L s^3 + CD(v_{pv} + v_b)(L_m + L)s^2 + LI_L s + D(v_{pv} + v_b)}{C_{pv} CL_m s^4 + \frac{LCL_m}{R_{pv}} s^3 + [C_{pv} LR_{pv} + D^2 CL_m + CD^2] + \frac{L}{R_{pv}} s + D^2} \\
\frac{\hat{i}_L}{\hat{d}}|_{\hat{v}_0=0} &= \frac{(CL_m s^2 + 1)[(v_b + v_{pv} - I_L DR_{pv}) + (v_{pv} + v_b)sR_{pv}C_{pv}]}{R_{pv}CC_{pv}LL_m s^4 + LCL_m s^3 + R_{pv}[LC_{pv} + D^2 C(L_m + L)]s^2 + Ls + D^2 R_{pv}}
\end{aligned}$$

3.4 Design Constraints of TCDIC

It has been shown in the previous section that the output voltage of the TCDIC depends on V_{pv} , V_b and n as per (3.3). Out of these three variables, n is constant for a

given transformer, V_b is an independent variable which varies depending on the charge level of the battery and V_{pv} depends on environmental condition. However, there is only one degree of freedom available for controlling the TCDIC and that is the duty ratio of the switch S_1 . As power extraction from the PV panel is required to be maximized, PV voltage needs to be controlled at a level corresponding to its MPP value and this is achieved by manipulating the duty ratio of the switch, S_1 . This implies that the control of the output voltage of the TCDIC, V_{dc} and the MPP operation of the PV panel cannot be accomplished simultaneously. When PV power is not available, the voltage across the PV capacitor, V_{pv} can be controlled to control V_{dc} at a desired value as per (3.3). However, the variation in PV voltage over wide range of variation in environmental conditions is limited within a small range [91]-[92]. Further, variation of battery voltage is also limited over its entire charge-discharge cycle. Therefore, the variation in V_{dc} is also small. The TCDIC is followed by a full bridge inverter as shown in Fig. 3.6 which performs dc-ac conversion while maintaining the required voltage level at the load terminal. Hence, irrespective of the variation of V_{dc} , the inverter controls and maintains a proper voltage level as required by the load. However, in order to maintain the standard (Indian) single phase ac output voltage of 230 V, a full bridge inverter requires a minimum of 350 V to be applied at its dc link to operate in the linear modulation range.

For design purpose, the ‘BP 4175T’ model from BP Solar [93] is considered as a reference model for PV modules. This model provides 175 W under standard test condition with panel voltage at this maximum power level, V_{mpp} as 35.4 V. The variation of this V_{mpp} with variation in environmental condition is approximately ± 5 V as provided in [93]. The voltage level of the battery is chosen as 36 V and three 12 V batteries are connected in series to form the battery bank. Considering the variation in the level of state of charge (SOC) of the battery around 40-100 %, the variation in the battery voltage is assumed as ± 5 V. Thus an overall variation of ± 10 V on $(V_b + V_{pv})$ is considered for the design purpose. With this consideration the variation in $(V_b + V_{pv})$ is allowed to be in the range, 62- 82 V approximately. As the dc-ac converter requires a minimum 350 V as its input dc link voltage, the turns ratio of the transformer is chosen to be 5.6 (i.e. 350/62). With this chosen turns ratio for the transformer, the variation in the dc link voltage, V_{dc} is (350-460) V thereby limiting the voltage stress of the semiconductor devices and passive elements to 460 V.

3.5 Control Structure of the Stand Alone Scheme Incorporating TCDIC

The controller of a stand alone system is required to perform the following tasks: (a) extraction of maximum power from the PV panel, (b) manipulation of the battery usage without violating the limits of overcharge and over discharge, and (c) dc-ac conversion while maintaining the load voltage at the prescribed level. A controller is devised for manipulating the TCDIC to realize the first two aforementioned objectives. The third objective is achieved by employing a conventional proportional integral (PI) based closed loop control strategy to control the output voltage of the full bridge inverter at the

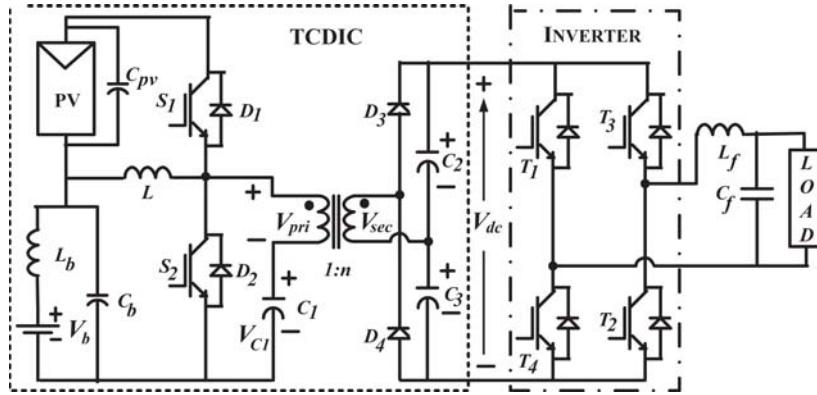


Figure 3.6: Schematic of the complete stand alone scheme

prescribed level. The unipolar sinusoidal pulse width modulation strategy is employed to derive gating pulses for the four switches of the inverter. As conventional control scheme is employed for controlling the output voltage of the inverter, its design issues are not discussed in this chapter. The details of control algorithm devised for TCDIC is presented in this section.

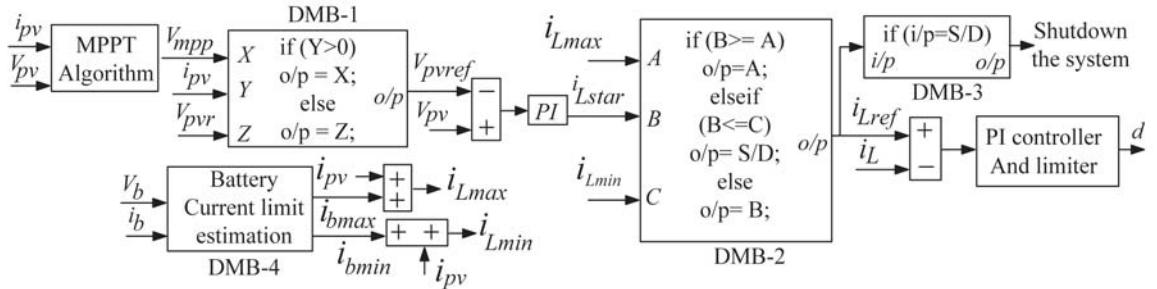


Figure 3.7: Control structure for the proposed TCDIC

In order to achieve the aforementioned two objectives, TCDIC is required to operate in one of the following modes: MPPT mode, non-MPPT mode, shutdown mode, and battery-only (BO) mode. The detailed definition of these modes and their selection criterions are discussed in Section 1.2.2. The control algorithm devised to select proper mode of operation for the TCDIC is shown in Fig. 3.7. The proper mode selection is done by four logical decision making blocks (DMB).

The control block, DMB-1 sets the reference for PV panel voltage, v_{pvref} . It also decides whether the system will operate in BO mode or in MPPT mode. When it is found that $i_{pv} > 0$, thereby indicating the availability of PV power, MPPT mode of operation is selected and the output of the MPPT algorithm block (i.e. v_{mpp}) sets v_{pvref} . When the PV power is not available, BO mode is selected and v_{pvref} is taken as v_{pvr} wherein v_{pvr} is selected so as to maintain the output voltage v_{dc} within the desired range

of 350-460 V as per (3.3). The error between v_{pvref} and v_{PV} is processed through a PI controller to set the required reference for the inductor current, i_{Lstar} . An upper limit, i_{Lmax} and a lower limit, i_{Lmin} is imposed on i_{Lstar} based on the relationship given in (3.5) to prevent over charging and over discharging of the battery respectively. These two limits are derived as follows:

$$i_{Lmax} = i_{bmax} + i_{pv} \quad (3.13)$$

$$i_{Lmin} = i_{bmin} + i_{pv} \quad (3.14)$$

wherein i_{bmax} and i_{bmin} are maximum permissible charging and discharging current of the battery respectively. These two limits are set based on the SOC level and the allowable depth of discharge of the battery [94]. The block, DMB-4 is employed to carry out the aforementioned functions. The block, DMB-2 sets the reference level for the inductor current, i_{Lref} after resolving the constraints imposed by i_{Lmax} and i_{Lmin} . When i_{Lref} remains within its prescribed limit, the system operates either in MPPT mode (for $i_{pv} > 0$) or in battery only-mode (for $i_{pv} \leq 0$). When i_{Lref} hits its lower limit thereby indicating that the over discharge limit of the battery is reached, DMB-3 withdraws gating pulses from all the switches and shuts down the system (shutdown mode). When the battery over charging limit is attained, i_{Lref} hits its upper limit. This situation arises only when the system is operating in MPPT mode with $p_{mpp} > p_{load}$ and the surplus power is more than p_{bmax} . In this condition, i_{Lref} is limited to i_{Lmax} to limit the battery charging current to i_{bmax} and the MPPT function is bypassed (as i_{Lref} does not follow i_{Lstar}). As the battery charging current is limited to i_{bmax} , power consumed by the battery gets restricted to p_{bmax} . This makes the available PV power more than $(p_{load} + p_{bmax})$. This extra PV power starts charging the PV capacitor, and its voltage increases beyond v_{mpp} . This shifts the PV operating point towards right side of the MPP point and the power extracted from the PV panel reduces. This process continues till the power drawn from the PV panel becomes equal to $(p_{load} + p_{bmax})$. Hence during operation of the system in non-MPPT mode, PV panel is operated at a point on the right side of its true MPP and hence $p_{pv} < p_{mpp}$. If there is a decrement in load demand while operating in non-MPPT mode, power drawn from the PV panel becomes more than $(p_{load} + p_{bmax})$ and this excess power drawn starts charging PV capacitor thereby shifting the operating point of the PV further towards right side of its previous operating point. In case of increment in the load demand, the power drawn from the PV panel falls short of supplying the load demand and the dc link capacitors and PV capacitor starts discharging. As the voltage of the PV capacitor falls, the operating point of the PV panel shifts towards left side from its previous operating point. This leads to an increment in the power drawn from the PV panel and this process continues till the power balance is restored. In case the load demand increases to an extent such that the PV power available at its MPP falls short to supply this load, battery will come out of its charging mode and i_{Lref} will become less than i_{Lmax} and the system operates in MPPT mode.

3.6 Simulated Performance

The system shown in Fig. 3.6 is simulated on Matlab/Simulink platform and the simulated responses obtained under different operating conditions are presented in this section. Different parameters/elements used in the simulation model are provided in Table 3.1.

Table 3.1: Parameters/elements used for stand alone system

Parameter	Value
power rating	500 VA
Transformer turns ratio, n	6
Capacitors	$C_{pv}=2000 \mu\text{F}$, $C_b = 1000 \mu\text{F}$ $C_f = 4 \mu\text{F}$, $C_1 = 470 \mu\text{F}$, $C_2 = C_3 = 1000 \mu\text{F}$
Inductors	$L_b=1 \text{ mH}$, $L = 3 \text{ mH}$, $L_f = 2.5 \text{ mH}$
Switching frequency, F_s	15 kHz
MPPT algorithm	Incremental conductance
PI controller gains	For PI-1: $K_p=0.068$, $K_i=.25$ For PI-2: $K_p=0.03$, $K_i=1$

The steady state response of the system while operating in MPPT mode is shown in Fig. 3.8. The level of insolation is chosen to be $1\text{kW}/m^2$ with corresponding I_{mpp} , V_{mpp} and P_{mpp} as 14.8 A, 35.4 V and 525 W respectively. Load demand is kept at 450 W which is less than P_{mpp} . It can be inferred from Fig. 3.8(a) that v_{pv} and i_{pv} is at their respective MPP values whereas i_b is positive indicating battery is charged to consume the surplus power. The load voltage which is being maintained at 230 V and the dc link voltage profile are shown in Fig. 3.8(b).

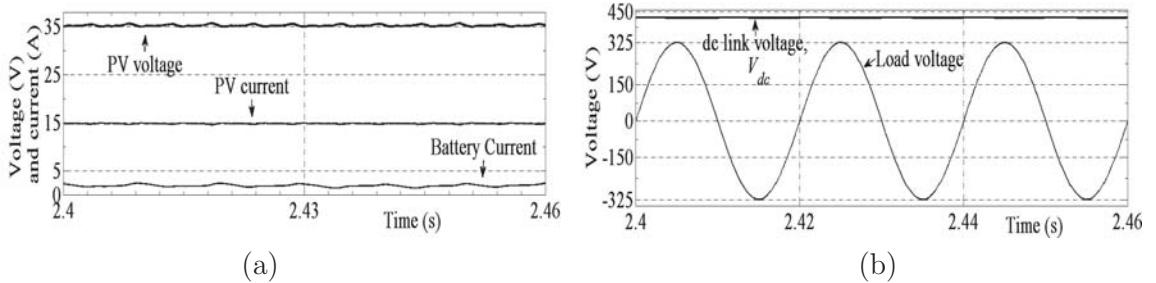


Figure 3.8: Simulated response of the system under steady state operation in MPPT mode. (a) v_{pv} , i_{pv} and i_b , (b) v_{dc} and load voltage

Simulated response of the system subjected to step changes in load demand and insolation level while operating in MPPT mode is shown in Fig. 3.9. Initially the insolation level is set at $0.75 \text{ kW}/m^2$ ($I_{mpp} = 11 \text{ A}$, $V_{mpp} = 35 \text{ V}$). At 1.4 s, the insolation level is changed to $1 \text{ kW}/m^2$ ($I_{mpp} = 14.8 \text{ A}$, $V_{mpp} = 35.4 \text{ V}$). The profile of the load demand to be negotiated is kept as follows: 450 W from 0-2.6 s, 350 W from 2.6 - 3.8 s, and 450 W

from 3.8 s onward. It can be inferred from Fig. 3.9(a) that v_{pv} and i_{pv} remain at their respective MPP values irrespective of changes in load or insolation level whereas i_b gets adjusted to maintain the operation at MPPT mode. The dc link voltage, v_{dc} and load voltage is shown in Fig. 3.9(b).

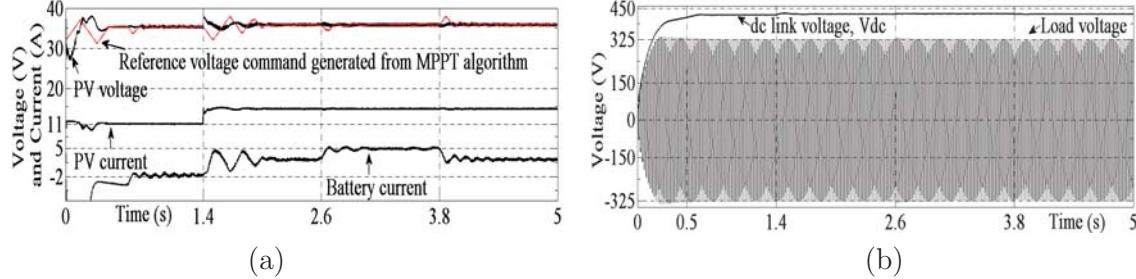


Figure 3.9: Simulated response of the system under changes in load and insolation level while operating in MPPT mode.(a) v_{pv} , i_{pv} and i_b , (b) v_{dc} and load voltage

Simulated response of the system during mode transition between MPPT and non-MPPT and the effect of step change in load demand while the operation is in non-MPPT mode, is shown in Fig. 3.10. The insolation level is kept fixed at 0.75 kW/m^2 ($I_{mpp} = 11 \text{ A}$, $V_{mpp} = 35 \text{ V}$, $P_{mpp} = 385 \text{ W}$). The I_{bmax} is set at 1 A which sets P_{bmax} at 36 W. Initially the load demand is kept at 450 W which is more than P_{mpp} . As a result, battery is discharged and the system operates in MPPT mode. At 1.2 s, load is reduced to 250 W which is less than P_{mpp} , and hence, the surplus power from PV starts charging the battery. Once the battery current reaches 1 A it gets restricted around this limit and the system enters into non-MPPT mode of operation. It can be noted from Fig. 3.10(a) that in non-MPPT mode, PV voltage settles at a value higher than its value at MPP i.e. PV operating point gets shifted to right side of its MPP. At 2.2 s, load is increased to 300 W. In order to supply this increased load demand, PV operating point shifts towards left of the previous operating point but remains on the right hand side of the MPP. At 3.3 s, the load demand is reduced to 250 W and the operating point of the PV shifts towards right hand side of MPP. At 4.2 s, load demand is increased to 450 W which is more than P_{mpp} . As a consequence battery starts discharging. This restores the system operation back to MPPT mode. It can be noted from Fig. 3.10(b) that v_{dc} changes when v_{pv} changes as per (3.3). However, value of v_{dc} remains within desired range of 350-460 V and hence load voltage is conveniently controlled at 230 V irrespective of changes in v_{dc} .

Simulated response of the system during mode transition between MPPT and BO mode is shown in Fig. 3.11. Load demand is kept fixed at 200 W. The insolation level is kept at 0.2 kW/m^2 ($I_{mpp} = 3 \text{ A}$, $V_{mpp} = 33 \text{ V}$) till 2 s. During this time interval the system operates in MPPT mode. At 2 s, insolation level is reduced to zero. This reduces PV current to zero and the system enters into BO mode. The PV voltage reference for BO mode is kept at 35 V. At 4.5 s, insolation is increased to 0.2 kW/m^2 . It can be observed from Fig. 3.11(a) that the PV voltage is controlled at its MPP value when system operates in MPPT mode while it is maintained at 35 V when the system operates in battery

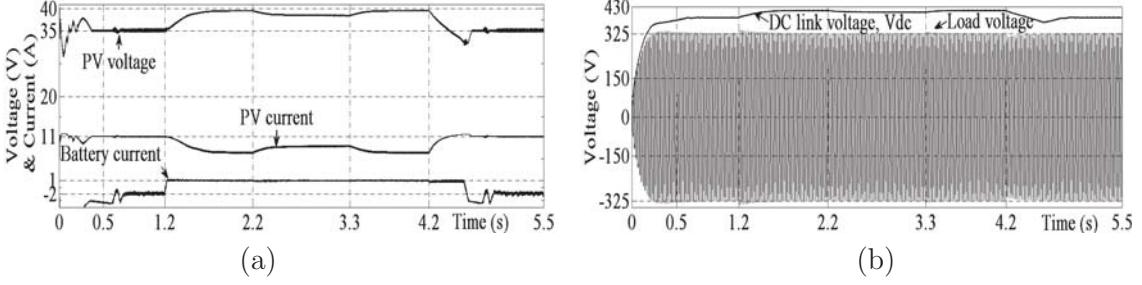


Figure 3.10: Simulated response of the system under mode transition between MPPT and non-MPPT mode and affect of load change in non-MPPT mode. (a) v_{pv} , i_{pv} and i_b , (b) v_{dc} and load voltage

only mode. The dc link voltage, v_{dc} and load voltage is shown in Fig. 3.11(b).

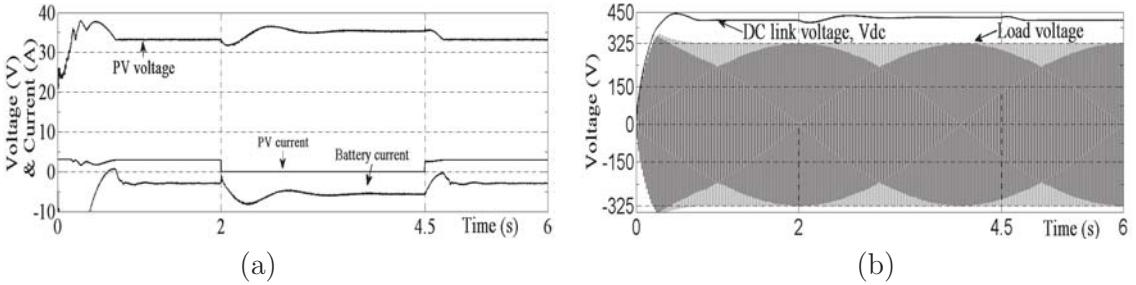


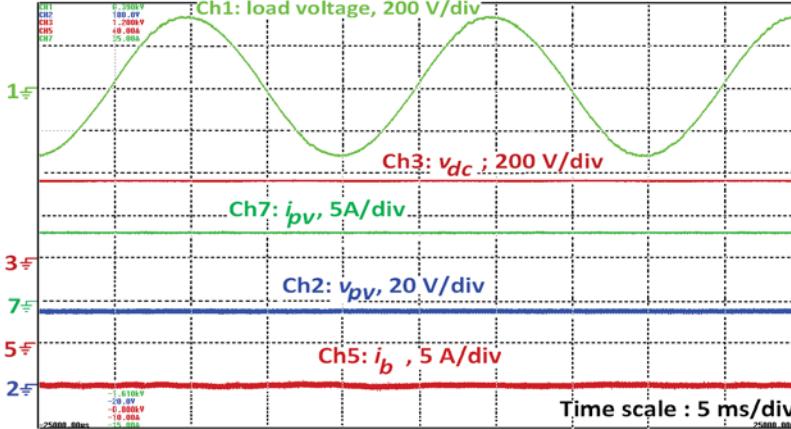
Figure 3.11: Response of the simulated system during mode transition between MPPT and BO mode. (a) v_{pv} , i_{pv} and i_b , (b) v_{dc} and load voltage

3.7 Experimental Validation

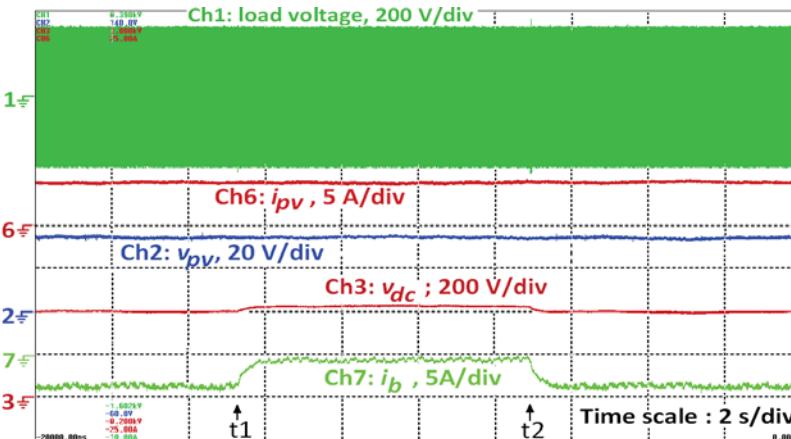
In order to demonstrate the viability of the proposed scheme a laboratory prototype is developed. The PV panel is realized by involving Agilent make solar panel simulator, E4360A. Three 12 V, 7 Ah valve regulated lead acid batteries are connected in series to form the 36 V battery bank. The RMS and peak values of currents and voltages to be handled by various semiconductor devices in the worst cases are provided in Table 3.2. Considering safety factor, device loss, and availability, the semiconductor devices chosen are as follows: (a) S_1 and S_2 : IRFP4668PbF (MOSFET, 200 V, 90 A), (b) D_3 and D_4 : STTH6010 (1000 V, 60 A), and (c) T_1 - T_4 : IRG7PH35UD1PbF (IGBT, 1200 V, 20 A). The controller is realized by employing Texas Instruments floating-point DSP, TMS320F28335. Other relevant parameters/elements used to realize the prototype remains the same as those used for carrying out simulation study, and provided in Table 3.1.

The steady state response of the system while operating in MPPT mode is shown in Fig. 3.12(a). The load demand is kept at 400 W. The values for V_{mpp} and I_{mpp} are set as 34 V and 8 A respectively. The battery voltage is measured using a multimeter as 33 V.

From Fig. 3.12(a) it can be inferred that v_{pv} (ch2) and i_{pv} (ch7) attains their respective prescribed values required for MPP operation. The dc link voltage, v_{dc} is around 385 V (ch3) which is approximately the expected value as per (3.3). The AC load voltage which is controlled at 230 V RMS, is shown in ch1. The battery current (ch5) is negative indicating battery is getting discharged.



(a)



(b)

Figure 3.12: Experimental result: (a) steady state response of the system while operating in MPPT mode and (b) response of the system under step changes in load demand during operation in MPPT mode

The system response under step changes in load demand while operating in MPPT

Table 3.2: Maximum current and voltage stress to be handled by various semiconductor devices at worst condition

Devices	RMS current	peak voltage
S_1 and S_2	26 A	82 V
D_3 and D_4	2.5 A	460 V
$T_1 - T_4$	3 A	460 V

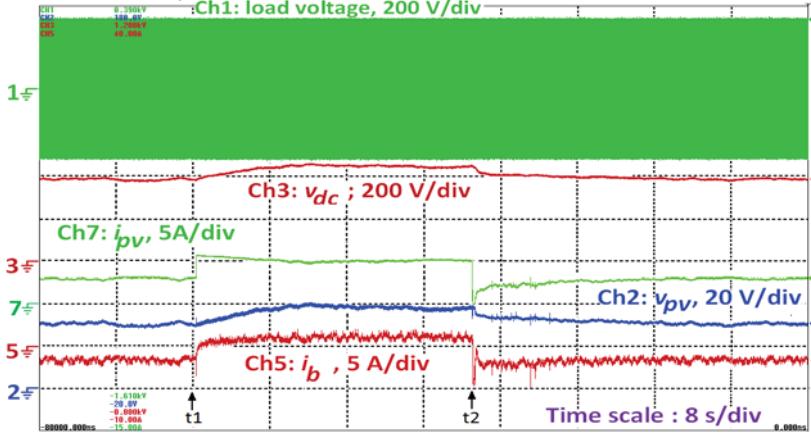
mode is shown in Fig. 3.12(b). The values of V_{mpp} and I_{mpp} are set as 35 V and 5 A respectively. The step changes in load demand are made at instants t1, from 260 W to 160 W, and at instant t2, from 160 W to 260 W. From Fig. 3.12(b) it can be inferred that the battery current (discharging)(ch7) has increased when the load demand has increased and it has decreased when the load demand has reduced however, v_{pv} and i_{pv} are maintained at their respective MPP values. It can be noted that v_{dc} (ch3) has reduced slightly when the load is increased. This is due to the fact that the voltage drop across switches and passive elements of TCDIC increases slightly when the current flowing through them has increased due to increment in the load demand. The load voltage (ch1) is maintained at 230 V and variation in load demand has negligible effect on it as closed loop control is employed to control the load voltage.

The system response to step changes in insolation level while operating in MPPT mode is shown in Fig. 3.13(a). The load demand is maintained at 120 W. The changes in insolation level is emulated by changing V_{mpp} and I_{mpp} values in the solar panel simulator. The values of V_{mpp} and I_{mpp} are set as follows: 30 V and 3 A till the instant t1; 38 V and 5 A during the interval t1 to t2; and 30 V and 3 A beyond t2. From Fig. 3.13(a) it can be inferred that the system tracks MPP satisfactorily irrespective of abrupt changes in insolation level.

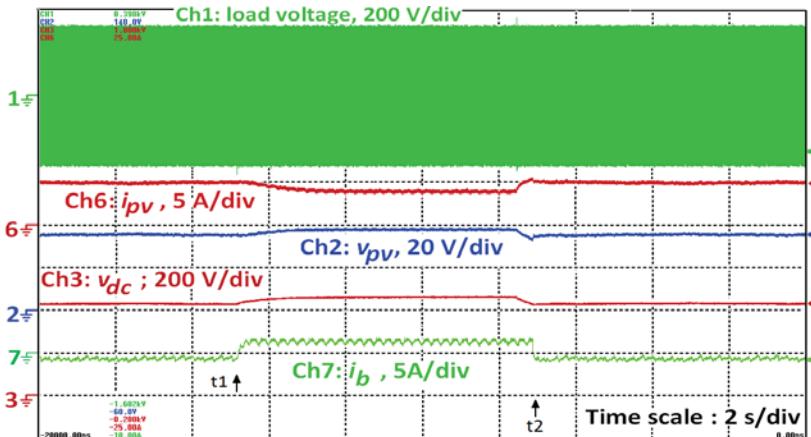
The response of the system during transition of mode between MPPT and non-MPPT is shown in Fig. 3.13(b). The I_{bmax} is set at 1.5 A. PV voltage and current at MPP are set at 35 V and 5 A respectively. Initially the load demand is set at 170 W. The battery is being discharged and the system operates in MPPT mode. At instant t1, the load is reduced to 60 W. This reduction in load forces the battery to go into charging mode in order to maintain operation at MPPT mode. As battery current reaches 1.5 A, it gets restricted around this limit and the system enters into non-MPPT mode of operation. Once the system enters to non-MPPT mode, MPPT algorithm gets deactivated and PV starts operating at a point on the right side of its MPP. This can be inferred from Fig. 3.13(b) that when the system enters into non-MPPT mode, the PV voltage(ch2) has become higher and the PV current (ch6) has become lower compared to their values at MPP. Due to an increment in the PV voltage, the dc link voltage has also increased as per (3.3). At the instant t2, the load demand is changed back to the previous value of 170 W and the operation of the system shifts from non-MPPT to MPPT.

The performance of the system during step changes in load demand while operating in non-MPPT mode is shown in Fig. 3.14(a). Initially the system is operating in MPPT mode with $V_{mpp} = 32$ V, $I_{mpp} = 6$ A while negotiating a load demand of 200 W. At the instant t1, the load is reduced to 60 W and the system operation is shifted to non-MPPT mode with I_{bmax} being set to 1.5 A. At the instant t2, the load demand is reduced to 0 W. As a result of further load reduction PV operating point shifts further towards right side of its MPP point and the power extracted from PV is reduced. This can be inferred from Fig. 3.14(a) as there is a further increase in PV voltage from its previous value. At the instant t3, load demand is changed back to 60 W.

The response of the system during transition of mode between MPPT and BO mode is shown in Fig. 3.14(b). The reference for the PV voltage during operation in the BO mode,



(a)



(b)

Figure 3.13: Experimental result: (a) response of the system subjected to step changes in insolation level during operation in MPPT mode and (b) performance of the system during mode transition between MPPT and non-MPPT mode

V_{pvr} is set at 35 V. The load demand is kept at 100 W. Initially the system operates in MPPT mode with $V_{mpp} = 30$ V, $I_{mpp} = 3$ A. At the instant t_1 , PV panel is disconnected from the system. As a result the PV current becomes zero and the system enters into BO mode. At the instant t_2 , PV panel is brought into the system and the system operation gets changed to MPPT from BO mode. From Fig. 3.14(b) it can be noted that the PV voltage is controlled at its MPP value when the system operates in MPPT mode whereas it is maintained at 35 V when the system operates in BO mode.

The measured efficiency curves for the proposed stand alone system for different operating conditions are shown in Fig. 3.15. A peak efficiency of 93.9% is obtained when both the PV panel and the battery are simultaneously feeding a load demand of around 300 W. A comparison of the proposed scheme with typical stand alone schemes is shown in Table 3.3. From this Table it can be concluded that the proposed scheme is advantageous in most of the attributes while it is comparable in the remaining attributes with respect to a given existing stand alone scheme.

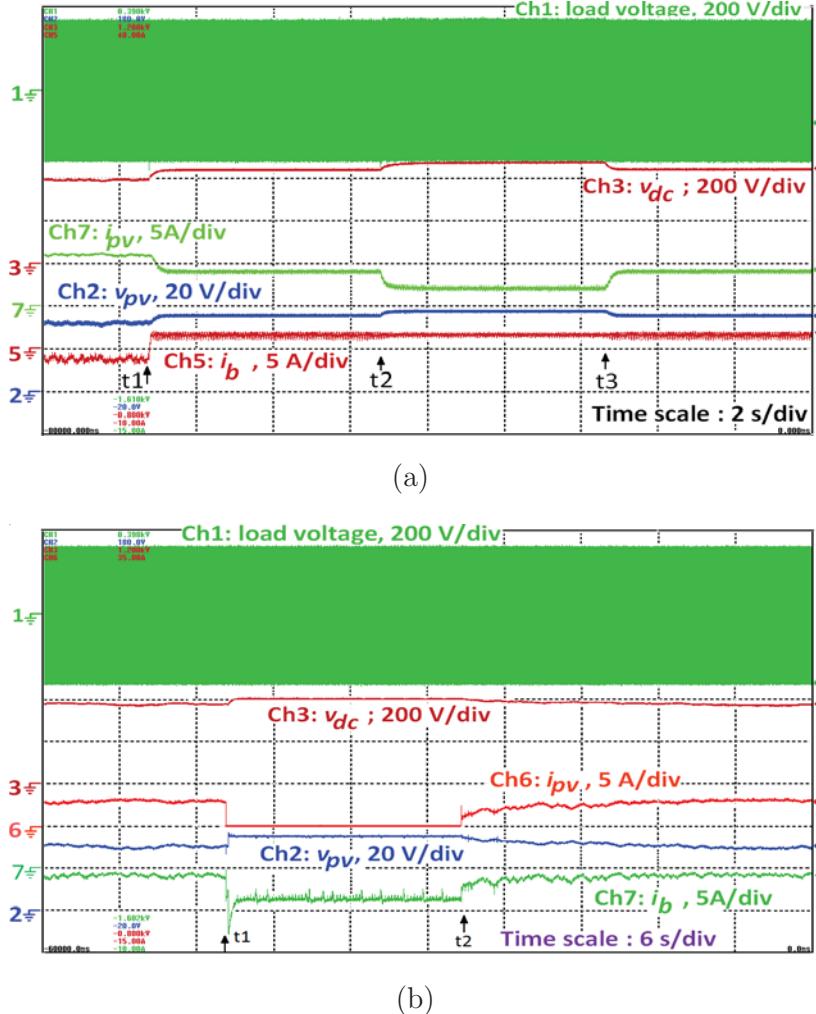


Figure 3.14: Experimental result: (a) response of the system under step changes in load demand during operation in non-MPPT mode and (b) response of the system during mode transition between MPPT and BO mode

3.8 Conclusion

A solar PV based stand alone power generation scheme is proposed in this chapter. It is realized by involving a new transformer coupled dual-input converter (TCDIC) followed

Table 3.3: Comparison of the proposed scheme with typical stand alone schemes

scheme	no. of stages	n_s	n_d	n_t	n_l	n_c	peak efficiency	dedicated conv. for MPPT	no. of conv. in battery charging path
Chen [19]*	3	9	0	1	5	6	90**	yes	2
Wang [14]	4	7	5	0	4	4	94.1	yes	1
Chen [80]*	3	12	12	1	3	2	91**	yes	2
Mutoh [84]	4	#	#	1	#	#	#	yes	2
Debnath [86]	3	7	2	0	4	4	#	yes	2
proposed	2	6	2	1	3	6	93.9	no	1

n_s = no. of switches, n_d = no. of diodes, n_t = no. of transformer, n_l = no. of inductors, n_c = no. of capacitors, * = as no dc-ac converter is provided a full bridge inverter is added to achieve dc-ac conversion and to maintain uniformity in comparison; # = data inadequate; ** = efficiency obtained in the absence of dc-ac inverter

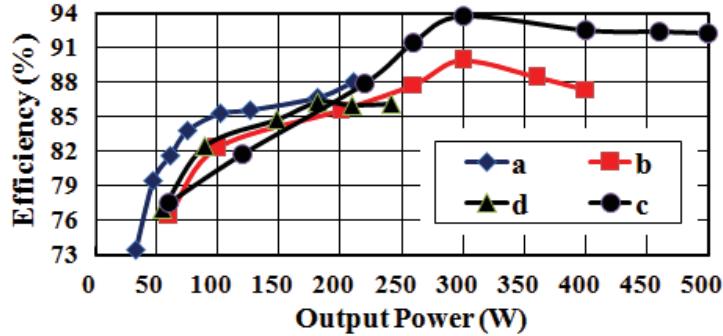


Figure 3.15: Measured efficiency curves obtained from the laboratory prototype: a) PV feeding power to battery under no load condition, b) battery feeding power to load when PV power is zero, c) both PV and battery simultaneously feeding power to the load, and d) PV feeding power simultaneously to the battery and the load

by a conventional full bridge dc-ac inverter. The salient features of the proposed scheme includes: (a) MPP tracking of PV panel, charge control of the battery, and boosting of the dc voltage are accomplished in a single converter, (b) enhancement of utilization of power converters as use of dedicated converter for ensuring MPP operation of the PV panel is eliminated, (c) enhancement in battery charging efficiency as a single converter is present in the battery charging path, (d) lesser component count as only two power conversion stages are required, (e) isolation is provided between input sources and load, and (f) simple and efficient control structure ensuring proper operating mode selection and smooth transition between different possible operating modes. The efficacy of the scheme is verified by performing detailed simulation studies. The viability of the scheme is confirmed through detailed experimental studies. A comparison of the proposed scheme with typical stand alone schemes indicate that the proposed scheme is advantageous in most of the attributes while it is comparable in the remaining attributes with respect to a given existing stand alone scheme. Thus it can be concluded that the proposed scheme is a deserving candidate for solar PV based stand alone scheme.

Chapter 4

Transformer-Less Decentralized Grid Connected Systems

4.1 Introduction

In order to conform to the aspiration of Jawaharlal Nehru National Solar Mission (JNNSM), grid connected solar photovoltaic schemes have been considered as one of the topics of investigation of the thesis. As a consequence a decentralized transformerless grid connected neutral point clamped inverter and its various mode of applications are proposed in this Chapter. Decentralized schemes are generally designed for low power ratings (<5 kW) and a single phase inverter is employed to form the interfacing link between the PV panel and the distribution grid. Though several converter topologies exist for realizing single-phase grid connected inverter, the transformerless inverter topologies have become popular due to their advantages such as low weight, less volume, high efficiency, low cost, etc [25]. However, the existing transformerless inverter schemes have one or more of the following drawbacks: (a) requirement of high voltage level for the PV panel owing to buck nature of the inverter, (b) inability to support wide variation in PV panel voltage, (c) inability to ensure flow of leakage current within permissible limit as it depends on the parasitic capacitances (including junction capacitance of switches) present in the leakage current loop, their location and grid voltage magnitude, (d) not tolerant to shoot through fault problem, (e) requirement of service of an additional dc-dc converter, and (f) requirement of two separate PV panels to be operated at the same conditions. The aforementioned limitations of transformerless grid connected inverter topologies reported in the literature can be overcome by resorting to the inverter proposed in this Chapter. This inverter having a neutral point clamped (NPC) structure can operate in buck-boost mode. This unique combination of NPC structure along with the ability of the inverter to operate in buck-boost mode bestows the scheme with the following advantages:

The following papers are published based on the content of this Chapter:

1. D. Debnath and K. Chatterjee, “A Neutral Point Clamped Transformer-less Grid Connected Inverter having Voltage Buck-boost Capability for Solar Photovoltaic Systems,” accepted for publication in IET Power Electronics
2. D. Debnath and K. Chatterjee, “A Transformerless Grid Connected Inverter for Solar Photovoltaic Systems Having Capability to Negotiate DC Loads,” in Proc. IEEE Int. Conf. on Indus. Tech. (ICIT), pp. 2835- 2840, March, 2015.

1. PV voltage level can be chosen independent of the grid voltage owing to the buck-boost nature of the inverter which facilitates to assign the designed voltage of the PV panel to be low. As PV voltage can be designed to be low, the scheme is less prone to suffer from low power yield while the individual PV modules are subjected to mismatched operating conditions.
2. the neutral point clamped based structure of the inverter leads to elimination of leakage current problem as PV parasitic capacitors will be impressed with either zero or constant dc voltage.
3. the inverter is tolerant to shoot-through fault.
4. the scheme requires six switches out of which four switches operate at grid frequency whereas only two switches operate at high frequency. Further, only two switches conduct at a given time.
5. grid current is not required to be sensed.

The principle of operation of the proposed scheme is presented in Subsection 4.2.1. The control strategy devised for the scheme is illustrated in Subsection 4.2.2. Design of various passive elements are provided in section Subsection 4.2.3. Detailed simulation results are presented in Subsection 4.2.4 to ascertain viability of the scheme. A scaled down laboratory prototype is developed and exhaustive experimental results obtained from the prototype are presented in Subsection 4.2.5. After confirming the efficacy of the proposed inverter, it has been modified to operate two PV panels at their respective MPPs while they are subjected to mismatched meteorological conditions. The motivation of this application, principle of operation, control philosophy, simulation and experimental studies are presented in Section 4.3. In addition to this, the proposed inverter can be made to feed PV power to the ac grid and at the same time can feed dc power to dc loads or to a dc microgrid. This application of the inverter has been presented in detail along with detailed simulation studies in Section 4.4.

4.2 Decentralized Grid Connected Neutral Point Clamped (NPC) Inverter

4.2.1 Principle of Operation

The schematic circuit diagram of the proposed inverter is shown in Fig. 4.1. As shown in the figure, a combination of two serially placed capacitors is connected across the PV panel. The midpoint of these two capacitors is connected to the neutral/ground terminal of the grid. This ensures that constant dc voltage is impressed across the parasitic capacitors which exists between the PV panel and the ground. These parasitic capacitors are represented by C_{pv1} and C_{pv2} in Fig. 4.1. Being impressed with constant dc voltage the flow of leakage current through these capacitors gets eliminated.

The inverter topology can be visualized as a combination two dc-dc buck-boost converters namely, CON1 and CON2. The converter, CON1 comprises of inductor, L_1 and

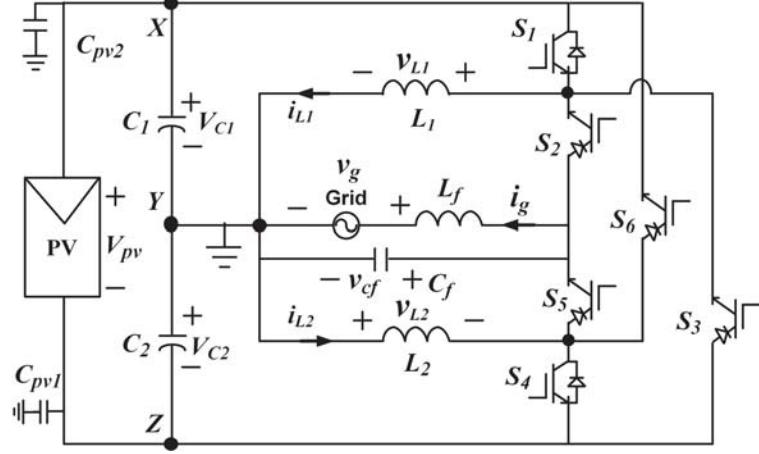


Figure 4.1: Schematic circuit diagram of the proposed inverter

switches, S_1 , S_2 , and S_3 . The other converter, CON2 is comprising of inductor, L_2 and switches, S_4 , S_5 , and S_6 . The switches, S_2 , S_3 , S_5 , and S_6 are required to have reverse voltage and reverse current blocking capability. Hence these switches can be realized either by employing reverse-blocking IGBTs (RB-IGBT) or a series combination of diode and IGBT/MOSFET. In this thesis work reverse blocking IGBTs are employed as they are compact and has less conduction loss as compared to the series combination of a diode and IGBT/MOSFET. On the contrary, switches, S_1 , and S_4 , can carry current in forward direction only owing to the structure and operating principle of the inverter. Further, they need not have reverse voltage blocking capability. Hence they can be realized by employing IGBT/MOSFET with or without having anti-parallel body diode. The combination of inductor, L_f and capacitor, C_f is employed to filter the current being injected to the grid. The converter is made to operate in discontinuous conduction mode (DCM). The operation of the inverter is explained as follows:

A. Operation in positive half cycle (PHC) of the grid voltage

I. Operation of CON1

The switch, S_2 is kept off and the switch S_3 is kept on while the duty ratio, d_1 of switch, S_1 is controlled to maintain voltage across C_1 , v_{C1} at half of v_{mpp} , wherein v_{mpp} is the PV panel voltage at its MPP. When S_1 is turned on, the current, i_{L1} flowing through L_1 , increases and hence L_1 stores energy received from the capacitor C_1 . When S_1 is turned off, the stored energy in L_1 is supplied to the capacitor, C_2 , through S_3 , and i_{L1} decreases. Therefore, CON1 works as a buck-boost dc-dc converter in PHC having C_1 at its input and C_2 at its output. As series combination two equal valued capacitor is connected across the PV panel, each of these capacitors receives half of the PV panel energy at any given time. However, all the energy received by C_1 is transferred to C_2 via CON1 as voltage across C_1 is maintained at a given value. Thus all the energy from PV panel is transferred to capacitor, C_2 ; half directly from the PV panel and remaining half

from C_1 via CON1. Hence, the average amount of power processed by CON1 during PHC is, $P_{CON1pos} = P_{pv}/2$ wherein P_{pv} is the magnitude of power being extracted from the PV panel.

II. Operation of CON2

The switch S_6 is kept off and switch S_5 is kept on while duty ratio, d_4 of switch, S_4 is controlled to maintain voltage across C_2 , v_{C2} at half of v_{mpp} . When S_4 is turned on, inductor L_2 stores energy from C_2 and its current i_{L2} increases. When S_4 is turned off the stored energy in L_2 is supplied to the grid through switch, S_5 , and i_{L2} decreases. As the voltage across C_2 is maintained at a constant voltage, the amount of energy it receives in a switching cycle from the PV panel gets transferred to the grid in the same switching cycle. Since C_2 receives the entire energy from the PV panel in a switching cycle, the grid is fed with total power extracted from the PV panel. Hence, the average amount of power processed by CON2 during PHC is, $P_{CON2pos} = P_{pv}$.

The power flow diagram during PHC is depicted in Fig. 4.2(a).

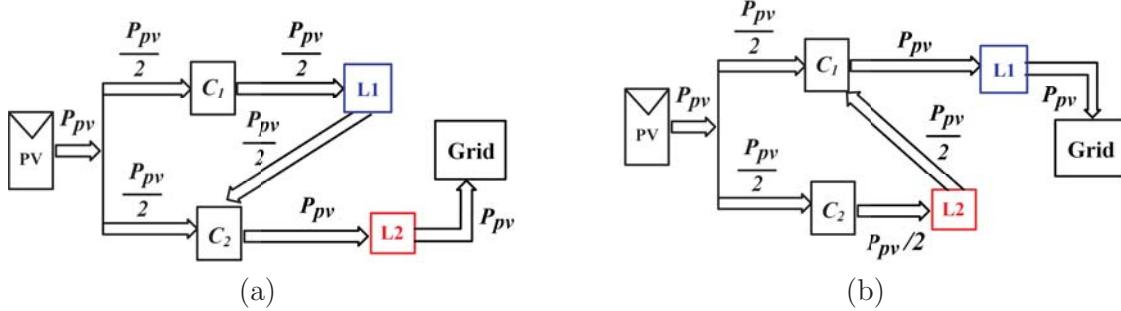


Figure 4.2: Operation of the proposed NPC inverter: (a) power flow diagram during positive half cycle, and (b) power flow diagram during negative half cycle

B. Operation in negative half cycle (NHC) of the grid voltage

I. Operation of CON1

The switch S_3 is kept off and S_2 is kept on while duty ratio of S_1 is controlled to maintain v_{C1} at half of v_{mpp} . In this half, C_1 is charged with total energy received from the PV panels (similar to charging of C_2 in positive half of grid voltage). When S_1 is turned on, inductor L_1 stores energy from C_1 and its current i_{L1} increases. When S_1 is turned off the stored energy in L_1 is supplied to the grid through switch, S_2 , and i_{L1} decreases. Thus, during NHC of grid voltage, CON1 supplies total power extracted from the PV panel to the grid. Hence, the average amount of power processed by CON1 during NHC is, $P_{CON1neg} = P_{pv}$.

II. Operation of CON2

The operation of CON2 in NHC is similar to that of CON1 in PHC. The switch S_6 is

kept on and S_5 is kept off while duty ratio of S_4 is controlled to maintain v_{C2} at half of v_{mfp} . In this half, CON2 transfers energy from C_2 to C_1 . The average amount of power processed by CON2 during NHC is, $P_{CON2pos} = P_{pv}/2$.

The power flow diagram during NHC is depicted in Fig. 4.2(b).

The switching pulses for the six switches are depicted in Fig. 4.3. From this figure it can be noted that out of six switches, two switches are operating at switching frequency and four switches are operating at grid frequency.

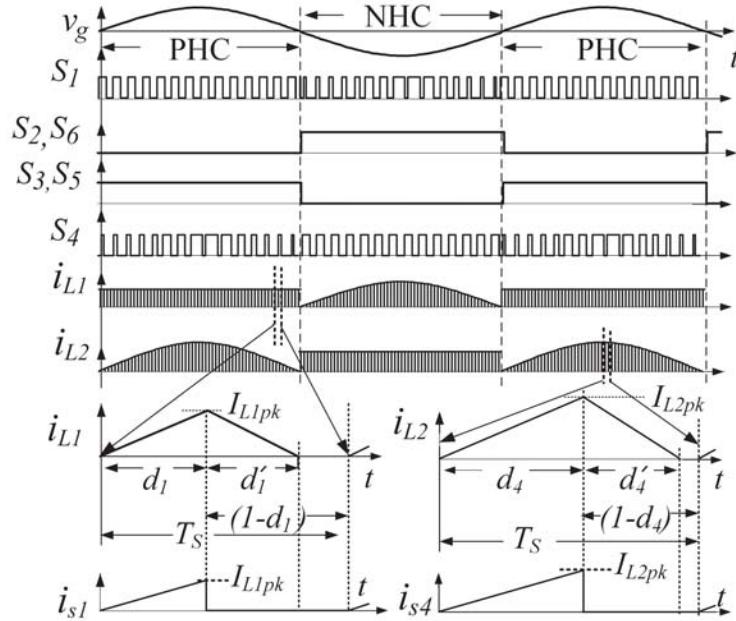


Figure 4.3: Switching pulses for the six switches of the proposed inverter and waveform of the inductor currents, i_{L1} and i_{L2} , along with their magnified views over an arbitrary switching cycle

The waveforms for the inductor currents, i_{L1} and i_{L2} , along with their magnified views over an arbitrary switching cycle are shown in Fig. 4.3.

The voltage impressed across inductor, L_1 is given by,

$$\begin{aligned} v_{L1} &= v_{C1}; \text{ for } 0 < t < d_1 T_s \\ &= v_{cf} k - v_{C2}(1 - k); \text{ for } d_1 T_s < t < (d_1 + d'_1) T_s \\ &= 0; \text{ for } (d_1 + d'_1) T_s < t < T_s \end{aligned}$$

wherein $k = 1$ in NHC and $k = 0$ in PHC. The magnitude of the peak current, i_{L1pk} flowing through the inductor, L_1 , is given by,

$$i_{L1pk} = \frac{v_{C1}}{L_1} d_1 T_s \quad (4.1)$$

The average value of current flowing through the switch, S_1 is, given by,

$$I_{S1avg} = \frac{1}{2} d_1 i_{L1pk} = \frac{V_{C1}}{2L_1} d_1^2 T_s \quad (4.2)$$

The average power received by CON1 during PHC can be expressed as,

$$P_{CON1pos} = V_{C1}I_{S1pos} = \frac{V_{C1}^2}{2L_1}D_{1pos}^2T_s = \frac{P_{pv}}{2} \quad (4.3)$$

wherein, D_{1pos} is the average value of duty cycle of switch S_1 during PHC and I_{S1pos} is the average value of current flowing through switch, S_1 during PHC. The average power received by CON1 during NHC can be expressed as,

$$P_{CON1neg} = V_{C1}I_{S1neg} = \frac{V_{C1}^2}{2L_1}D_{1neg}^2T_s = P_{pv} \quad (4.4)$$

wherein, D_{1neg} is the average value of duty cycle of switch S_1 during NHC and I_{S1neg} is the average value of current flowing through switch, S_1 during NHC.

The voltage impressed across the inductor, L_2 is given by,

$$\begin{aligned} v_{L2} &= v_{C2}; \quad \text{for } 0 < t < d_4 T_s \\ &= -v_{cf}(1 - k) - v_{C1}k; \quad \text{for } d_4 T_s < t < (d_4 + d'_4)T_s \\ &= 0; \quad \text{for } (d_4 + d'_4)T_s < t < T_s \end{aligned} \quad (4.5)$$

The magnitude of peak current, I_{L2pk} flowing through the inductor, L_2 is given by,

$$I_{L2pk} = \frac{v_{C2}}{L_2}d_4 T_s$$

The average value of current flowing through the switch, S_4 is given by,

$$I_{S4avg} = \frac{1}{2}d_4 i_{L2pk} = \frac{V_{C2}}{2L_2}d_4^2 T_s \quad (4.6)$$

The average power received by CON2 during PHC can be expressed as,

$$P_{CON2pos} = V_{C2}I_{S4pos} = \frac{V_{C2}^2}{2L_2}D_{4pos}^2T_s = P_{pv}$$

wherein, D_{4pos} is the average value of duty cycle of switch S_4 during PHC and I_{S4pos} is the average value of current flowing through S_4 during PHC. The average power received by CON2 during NHC can be expressed as,

$$P_{CON2neg} = V_{C2}I_{S4neg} = \frac{V_{C2}^2}{2L_2}D_{4neg}^2T_s = \frac{P_{pv}}{2}$$

wherein, D_{4neg} is the average value of duty cycle of switch S_4 during NHC and I_{S4neg} is the average value of current flowing through switch, S_4 during NHC.

From the above discussion it can be concluded that grid is fed with total PV power in both the half cycles. In both of the half cycles grid is fed from capacitors having same voltage level. Further, the principle by which power is fed to grid from the capacitors is same as that of a buck-boost converter. Thus the proposed inverter can support wide variation in PV voltage as it can be operated in buck as well as boost mode. Also, symmetrical operation in both the half cycles avoid dc current injection into the grid.

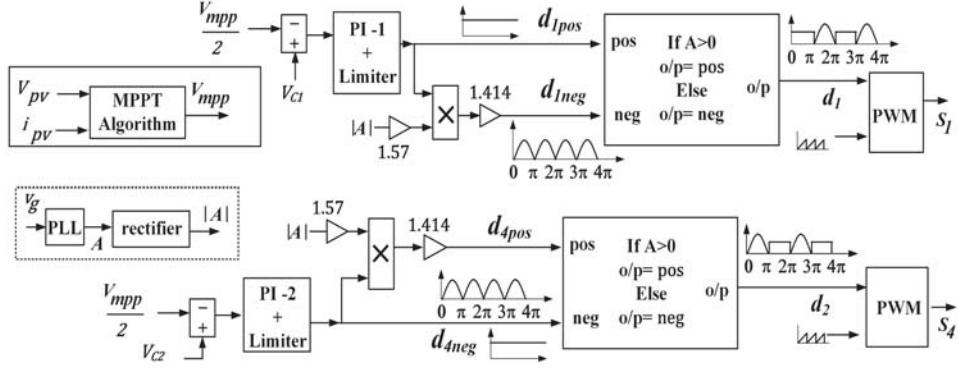


Figure 4.4: Control structure of the proposed inverter servicing single PV panel for operation in DCM

4.2.2 Control Strategy

The control strategy devised for DCM operation of the proposed inverter is shown in Fig. 4.4. A conventional MPPT algorithm is employed to generate reference voltage command for the PV string to operate it at its MPP. This reference voltage command, v_{mpp} is then halved and given as reference voltage commands to control the voltage across capacitors, v_{C1} and v_{C2} . The actual capacitor voltages are then compared with their respective references and the errors obtained are processed and manipulated to generate suitable duty ratios, d_1 for switch S_1 and d_4 for switch S_4 . The manipulation of the duty ratios are carried out with the help of signal ‘ $|A|$ ’. This signal is the rectified version of signal ‘A’ which is a unit amplitude sinusoidal signal phase synchronized with the grid voltage. The signal A is generated by employing a phase locked loop (PLL) algorithm. The steps involved in generation of final duty ratios, d_1 and d_4 , are as follows:

A. Generation of d_1 :

The duty ratio, d_1 needs to be controlled to maintain v_{C1} at its reference value $V_{mpp}/2$. To achieve this the error between reference command and the sensed value of v_{C1} is processed through PI-1 which generates initial/base value for d_1 . This base value is then manipulated to generate final duty ratio as follows:

1. *Generation of d_1 for positive half cycle:* during positive half cycle energy is transferred from C_1 to C_2 through CON1 following same principle of that of a buck-boost dc-dc converter. Hence, the magnitude of d_1 for positive half cycle is kept same as the output of PI-1.

2. *Generation of d_1 for negative half cycle:* As compared to operation in the PHC, the operation of CON1 in NHC is different in the following two aspects:

(i) During NHC energy is transferred from C_1 to the grid through CON1 following same principle of that of a buck-boost dc-dc converter. As the current injected to the grid must be sinusoidal, the profile of d_1 should also be sinusoidal. In order to generate

sinusoidally varying profile for d_1 , the output of PI-1 is multiplied with signal $|A|$ as shown in Fig. 4.4. However, the average magnitude of the resultant product of this multiplication is less than the output of PI-1. This is because the amplitude of the rectified sinusoidal signal, $|A|$ is unity and hence its average value is $\frac{2}{\pi}$ which is less than unity. In order to keep the average duty ratio same after multiplication with $|A|$, the signal $|A|$ is multiplied with $\frac{\pi}{2}$ as shown in Fig. 4.4.

(ii) During negative half cycle the amount of power to be handled by CON1 gets doubled as it has to process the entire PV panel power. Hence the average value of duty ratio for S_1 in NHC, D_{1neg} must be greater than that of its magnitude in PHC, D_{1pos} . The required magnitudes for D_{1pos} and D_{1neg} can be obtained from equations (4.3) and (4.4) respectively as follows,

$$D_{1pos}^2 = \frac{L_1 P_{pv}}{T_s V_{C1}^2} \quad (4.7)$$

$$D_{1neg}^2 = \frac{2L_2 P_{pv}}{T_s V_{C2}^2} \quad (4.8)$$

From (4.7) and (4.8), the required expression for D_{1neg} in terms of D_{1pos} can be written as,

$$D_{1neg} = \sqrt{2} D_{1pos}, \quad \text{as } L_1 = L_2, \text{ and } V_{C1} = V_{C2}$$

This can be inferred from Fig. 4.4 that a factor $1.414 (= \sqrt{2})$ is employed as a gain while generating d_{1neg} so as to account for increased amount of power to be handled by CON1 during NHC.

B. Generation of d_4 :

The duty ratio, d_4 needs to be controlled to maintain v_{C2} at its reference value $V_{mpp}/2$. To achieve this the error between reference command and the sensed value of v_{C2} is processed through PI-2 which generates initial/base value for d_4 . This base value is then manipulated to generate final duty ratio as follows:

i. Generation of d_4 for positive half cycle: during this half cycle energy is transferred from C_2 to the grid through CON2 following the same principle of that of a buck-boost dc-dc converter. As operation of CON2 is PHC is similar to the operation of CON1 in NHC, the final value of d_{4pos} is generated following the similar steps employed for generation of d_{1neg} .

ii. Generation of d_4 for negative half cycle: during positive half cycle energy is transferred from C_2 to C_1 through CON2 following the same principle of that of a buck-boost dc-dc converter. Hence, the magnitude of d_4 for positive half cycle is kept same as the output of PI-2.

4.2.3 Selection Criteria of Various Passive Elements

The selection criterias of various passive elements for operation of the inverter in DCM are as follows:

a. Selection of L_1 and L_2 :

The values of L_1 and L_2 are chosen so that CON1 and CON2 operate under DCM while they are required to negotiate peak power. Following the procedure presented in [47], the critical values of L_1 and L_2 can be expressed as,

$$L_{critical} = \frac{0.25 T_s}{P_{max}} \left[\frac{1}{v_{gm}} + \frac{1}{v_{max}} \right]^{-2} \quad (4.9)$$

wherein, P_{max} is the maximum power output from PV source, v_{max} is the maximum value of PV panel voltage at MPP, v_{gm} is the peak value of grid voltage and T_s is the switching time period. The values of L_1 and L_2 , henceforward referred as L in this chapter, must be less than $L_{critical}$ for operation of the proposed inverter in DCM.

b. Selection of C_1 and C_2 :

The capacitors, C_1 and C_2 , are designed based on guidelines provided in [25] as follows:

$$C_1 = C_2 = \frac{I_{max}}{4\pi f_g \Delta v_{pv}} \quad (4.10)$$

wherein, I_{max} is the maximum value of PV panel current at MPP, Δv_{pv} is the voltage ripple across C_1 and C_2 , and f_g is the grid frequency.

c. Selection of L_f and C_f :

The grid side filters, L_f and C_f are designed based on expressions provided in [47] and are as follows:

$$\begin{aligned} C_f &= \frac{T_s^2}{4L v_{gm} \Delta v} \left[\frac{1}{v_{gm}} + \frac{1}{v_{max}} \right]^{-2} \\ L_f &= \frac{1}{(2\pi f_c)^2 C_f} \end{aligned}$$

wherein, Δv is the ac voltage ripple in C_f , f_c is the cut-off frequency of filter.

4.2.4 Simulated Performance

In order to verify the effectiveness of the proposed scheme, Matlab/Simulink platform is utilized to simulate the scheme. Various components/elements considered for the simulated model are provided in Table 4.1. The insulation level on the PV panel is set as 1000 W/m^2 from 0 - 2 s, 800 W/m^2 from 2 - 3.5 s, and 600 W/m^2 from 3.5 s onwards. The temperature of the PV panel is maintained as 30° C from 0 - 5 s and 20° C from 5 s onwards.

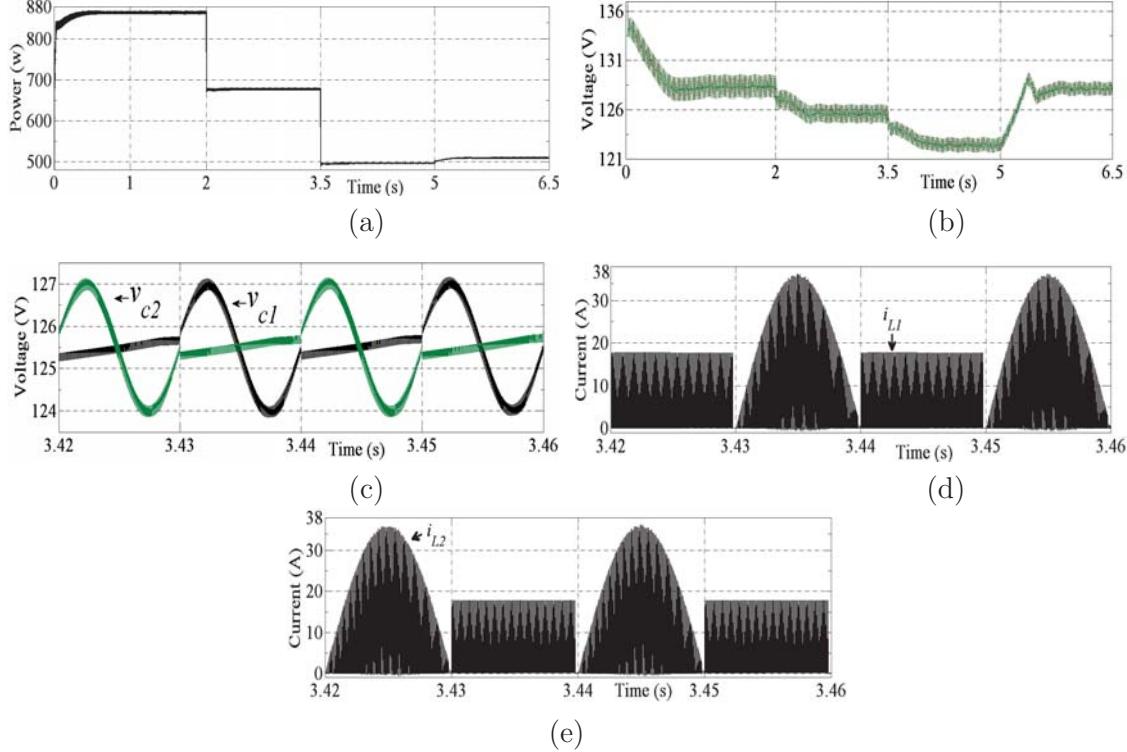


Figure 4.5: Simulated response of the system: a) power output from the PV panel, b) voltage across capacitors, C_1 and C_2 , c) magnified voltage across capacitors, C_1 and C_2 , d) steady state profile of i_{L1} , and e) steady state profile of i_{L2}

The variation in power output from the PV panel with aforementioned values of insolation level and temperature is shown in Fig. 4.5(a). The profiles of voltages across capacitors, C_1 and C_2 , are shown in Fig. 4.5(b). From this figure it can be noted that, with changes in insolation level and temperature, these capacitor voltages also get adjusted to ensure that the system operates at MPP. Further, irrespective of operating conditions of the PV panel, both the capacitor voltages remain to be balanced. The magnified view of voltages across capacitors, C_1 and C_2 , are shown in Fig. 4.5(c) wherein it can be inferred that both of the capacitor voltages has 50 Hz dominant component as they supply power to grid for only one half cycle of the grid voltage. The steady state profiles of inductor

Table 4.1: Parameters/elements considered for the simulation study

Parameter	Value
Grid voltage, V_g	230 V
$L_1 = L_2$	0.1 mH
$C_1 = C_2$	3300 μ F
Grid side filter, C_f & L_f	2 μ F & 5 mH
Switching frequency, F_s	15 kHz
MPPT algorithm	Incremental conductance

currents, i_{L1} and i_{L2} are provided in Fig. 4.5(d) and Fig. 4.5(e) respectively to highlight the operation of the inverter in discontinuous conduction mode (DCM).

The current being fed to the grid is shown in Fig. 4.6(a). The magnified views of the grid voltage and the grid current during steady state operation are shown in Fig. 4.6(b) from where it can be noted that the grid current is fairly sinusoidal and is in phase with the grid voltage. The total harmonic distortion (THD) and dc component in grid current is shown in Fig. 4.6(b) and it can be inferred that the THD is around 3% and that the dc component is almost zero.

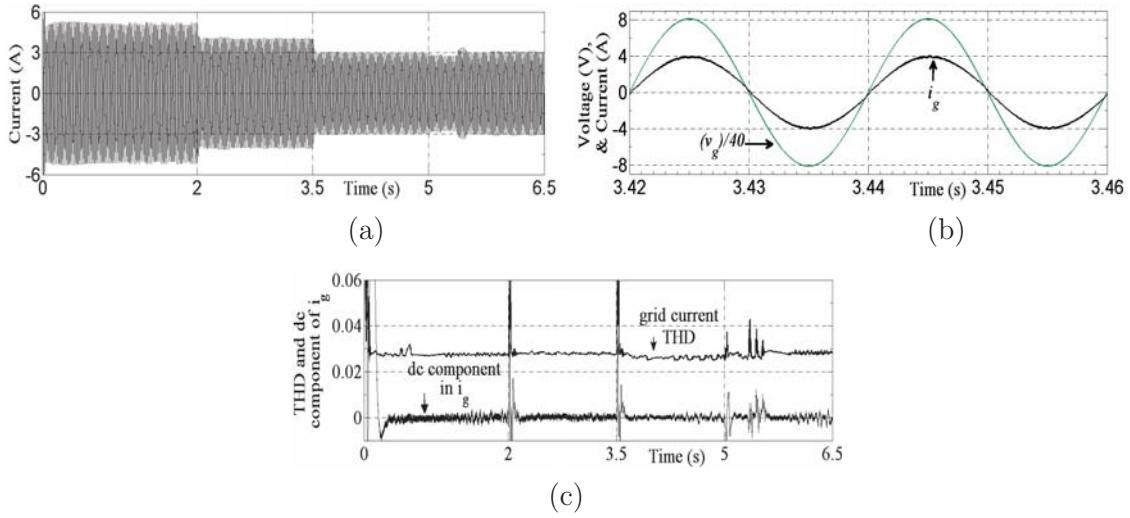


Figure 4.6: Simulated response of the system: a) current flowing into the grid, b) magnified views of grid voltage and current flowing into the grid, and c) profile of THD and dc current component in grid current

4.2.5 Experimental Validation

In order to confirm the viability of the proposed scheme detailed experimental validations have been carried out on a prototype of the scheme developed for the purpose. A single phase autotransformer is utilized to step down the grid voltage to the order of 50-110 V in order to demonstrate the operation of the inverter in both buck and boost mode. The phase information of the grid voltage is obtained by employing enhanced phase lock loop (ePLL) algorithm [96]. The PV panel is realized by Agilent make solar panel simulator, E4360A. This simulator takes input in the form of I_{mpp} , V_{mpp} , I_{sc} , and V_{oc} , wherein I_{sc} is the short circuit current and V_{oc} is the open circuit voltage of the PV panel. By altering these parameters manually, changes in operating condition on the PV panel can be emulated. Other relevant parameters/elements employed to develop the laboratory prototype are given in Table 4.2. A photograph of the experimental setup is shown in Fig. 4.7.

The steady state response of the inverter while it is being operated in buck mode is shown in Fig. 4.8(a). The grid voltage is set at 50 V. The maximum power point values

Table 4.2: Parameters/elements employed to realize the laboratory prototype

Parameter	Value/range
PV Voltage, V_{pv}	50-90 V
PV Current, I_{pv}	0-3 A
Capacitors, C_1 & C_2	3300 μ F
Inverter output filter, C_f & L_f	2 μ F & 4 mH
Inductors, L_1 & L_2	0.1 mH
MPPT algorithm	Incremental conductance
Power rating	200 W
Switch, S_1 & S_4	IRG7PH42UPbF
Switch, S_2 , S_3 , S_5 & S_6	IXRH40N120
Switching frequency for S_1 & S_4	15 kHz
Digital controller	TMS320F28335

for the PV panel are set as, $V_{mpp} = 90$ V and $I_{mpp} = 1.5$ A. From Fig. 4.8(a) it can be inferred that both the capacitor voltages are maintained at 45 V implying that the PV panel is being operated at its maximum power point. The grid current is in phase with the grid voltage and its shape is fairly sinusoidal. A magnified view of Fig. 4.8(b) over few switching cycle is shown in Fig. 4.8(d) to highlight operation of the inverter in DCM. Frequency spectrum of the grid current is shown in Fig. 4.8(c) which shows that the THD of the grid current is around 4 % and the dc component present is around 0.06%.

Steady state response of the system when it is operating in buck-boost mode is shown in Fig. 4.9(a) and 4.9(b). In case of Fig. 4.9(a), the grid voltage is set at 80 V and the maximum power point of the PV panel is set as, $V_{mpp} = 90$ V and $I_{mpp} = 1.5$ A. For the result shown in Fig. 4.9(b), the grid voltage is set at 110 V and the maximum power point of the PV panel is set as, $V_{mpp} = 90$ V and $I_{mpp} = 2$ A. From these measured performances it can be inferred that the system operates satisfactorily in buck-boost mode ensuring MPPT operation while ensuring that sinusoidal current is being injected to the grid. The THD in grid current shown in Fig. 4.9(a) and Fig. 4.9(b) is found to be around 4.3% and 4.38% respectively.

The responses of the system subjected to changes in environmental condition are shown in Fig. 4.10 and Fig. 4.11. The changes in environmental condition is emulated by changing maximum power point values of the PV panel by appropriately changing the input commands of the solar panel simulator, E4360A. The responses of the system subjected to step increment and decrement in MPP values are shown in Fig. 4.10 and Fig. 4.11 respectively. The grid voltage is set at 110 V for both the cases. For the response shown in Fig. 4.10(a), step increment in MPP values are given at the instant, t_1 . Till the instant, t_1 the MPP values of the PV panel are set at $V_{mpp} = 70$ V and $I_{mpp} = 1.5$ A. From Fig. 4.10(a) it can be inferred that the system is operated at its MPP with capacitor voltages being maintained at 35 V. Magnified view of Fig. 4.10(a), while the system is operating at steady state condition with the aforesaid MPP values, is shown in Fig. 4.10(b). At the instant, t_1 the MPP values of the PV panel are changed to $V_{mpp} = 90$ V and $I_{mpp} = 2$ A. It can be inferred from Fig. 4.10(a) that the system tracks the new maximum power point satisfactorily. Magnified view of Fig. 4.10(a) around a point

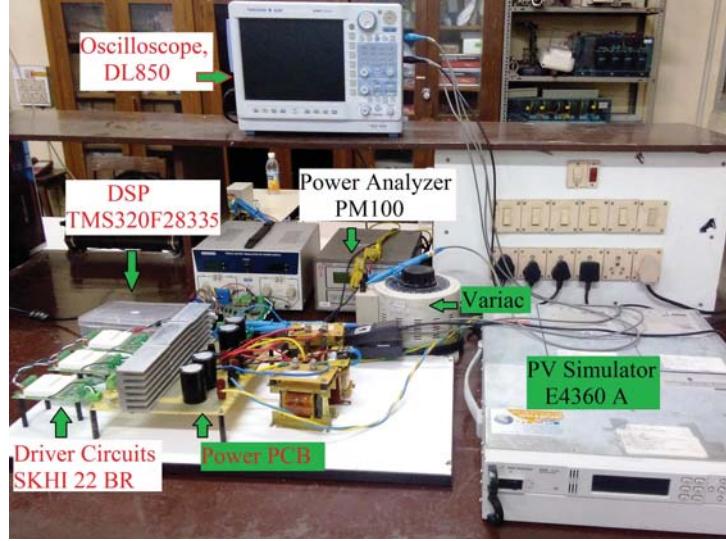


Figure 4.7: Photograph of the experimental setup

where the system is operating at steady state condition with these new set of MPP values is shown in Fig. 4.10(c). For the response shown in Fig. 4.11(a), step decrement in MPP values are given at instant, t_2 . Till the instant, t_2 the MPP values are set at $V_{mpp} = 80$ V and $I_{mpp} = 2$ A. At the instant, t_2 the MPP values are changed to $V_{mpp} = 70$ V and $I_{mpp} = 1.5$ A. From Fig. 4.11(a) it can be inferred that the inverter is capable of tracking MPP satisfactorily irrespective of step decrement in MPP values. The magnified views of Fig. 4.11(a) around a point when the system is operating at steady state before and after the MPP values being changed are shown in Fig. 4.11(b) and Fig. 4.11(c) respectively.

In order to measure the efficiency of the laboratory prototype the following procedure has been pursued. The PV panel voltage is maintained at the maximum power point (MPP) of 90 V as the maximum voltage limit of the available solar panel simulator, E4360A employed for the purpose is 90 V. The grid voltage is maintained at 110 V. The power injected to the grid is measured by the power analyzer, PM100 which is then divided by the power output from the PV panel to obtain the overall efficiency of the system. Power output from the PV panel is noted from the display of the solar panel simulator, E4360A. The efficiency thus obtained is the global efficiency of the system including losses incurred in the all the active and passive components of the inverter. The efficiency curves so determined are shown in Fig. 4.12(a). As the output voltage of E4360A is limited to 90 V, in order to obtain the efficiency for the entire range of operation of the proposed inverter, efficiency is estimated for the system by following the procedure presented in [99]-[100]. The estimated efficiency curve of the system while the PV panel voltage is maintained at the MPP of 90 V is also plotted in Fig. 4.12(a). From this figure it can be inferred that the estimated efficiency curve is in close agreement with the measured efficiency curve. Hence it can be concluded that the procedure for determining the estimated efficiency is quite realistic. Subsequently, the overall efficiency curves

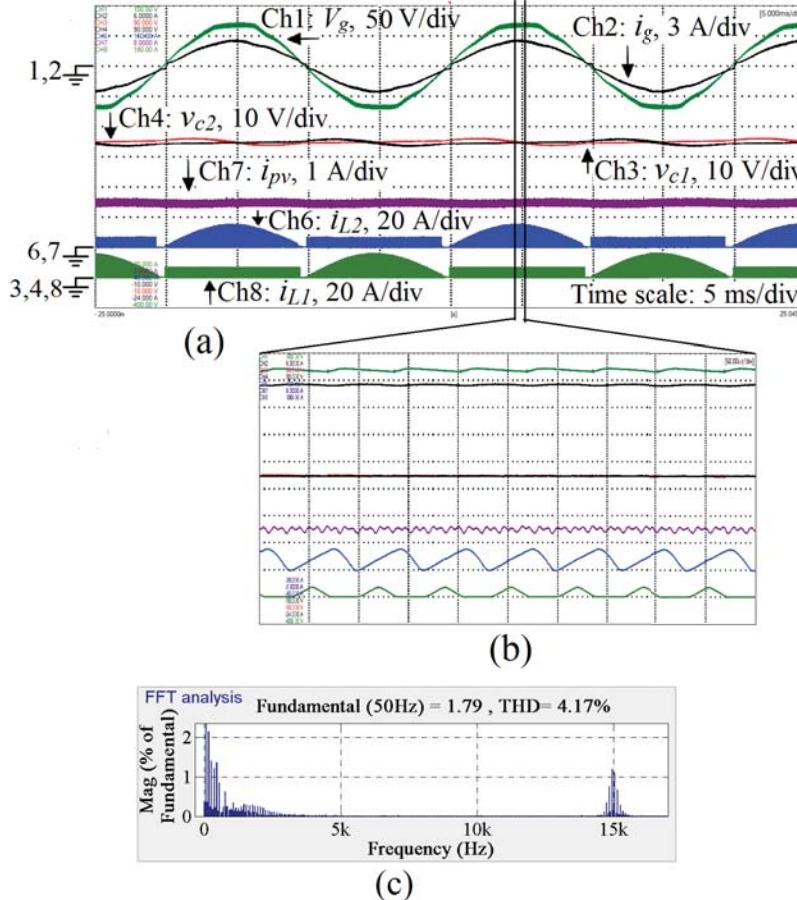


Figure 4.8: Experimental validation: (a) steady state response of the system in buck mode of operation, (b) Magnified view of steady state response over few switching cycle, and (c) Frequency spectrum of the grid current during buck mode of operation

of the system is estimated for the entire range of its operation and they are depicted in Fig. 4.12(b). From this figure it can be observed that the efficiency in the order of 94.5% is achieved from the proposed inverter. A comparison of the circuit losses incurred in the proposed inverter with that of three traditional transformerless inverter schemes is provided in Table 4.3. From this Table and Fig. 4.12(b) it can be observed that the estimated efficiency of the proposed inverter is approximately 3% less as compared to the existing transformerless inverters. However, this marginal decrement in efficiency for the proposed inverter is complemented by its several advantages over its traditional counter parts which are as follows: (a) capability to operate in buck-boost mode thereby allowing wide variation in PV panel voltage, (b) tolerant to shoot through fault thereby improving reliability, (c) elimination of grid current sensor requirement, and (d) elimination of leakage current.

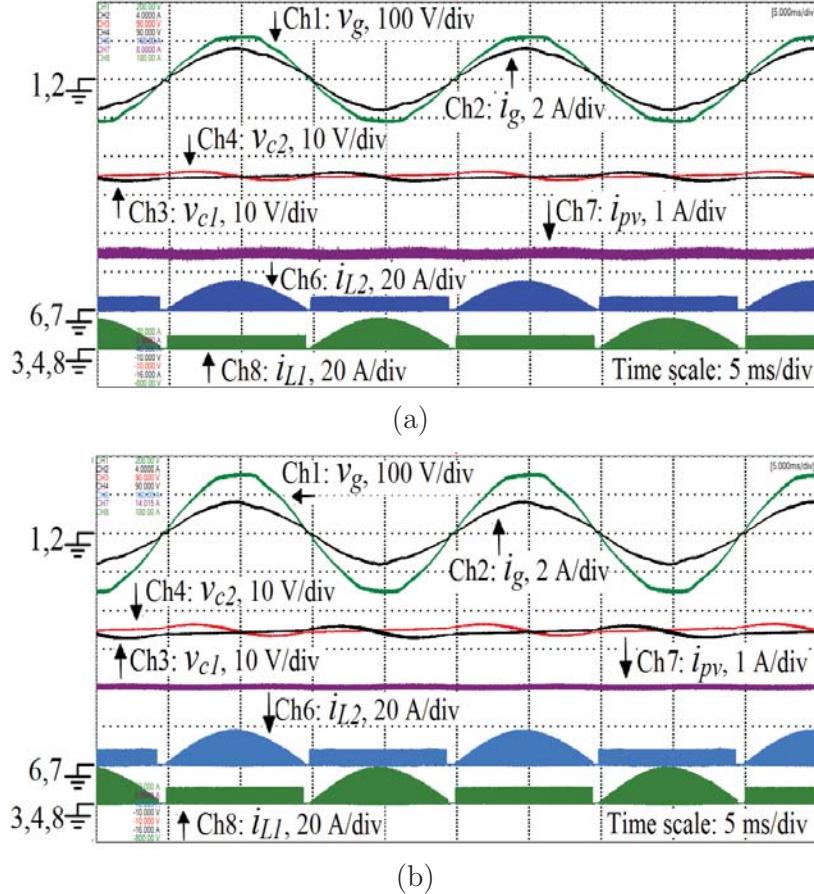


Figure 4.9: Experimental results: (a) steady state response of the system while operating in buck-boost mode with grid voltage set at 80 V, and (b) steady state response of the system while operating in buck-boost mode with grid voltage set at 110 V

A comparison of the proposed inverter with other NPC inverters which can operate in buck-boost mode is provided in Table 4.4. From this table it can be inferred that the proposed scheme is advantageous over other two schemes in terms of input capacitance requirement and assurance of symmetrical operation in both the half cycle of the grid voltage. However, the efficiency of the proposed scheme is slightly less as compared to the other schemes mainly due to its operation in DCM.

4.3 Decentralized Grid Connected NPC Inverter Servicing Two Separate PV Panels

The existing transformerless topologies have a common drawback in that they use a single PV panel as the input to the system. This approach simplifies the design, but results in considerable reduction in power yield when part of the panel is partially shaded or there is a mismatch in operating conditions in the series connected PV modules that form the panel. Few topologies which have the facility to employ two separate PV panels to form

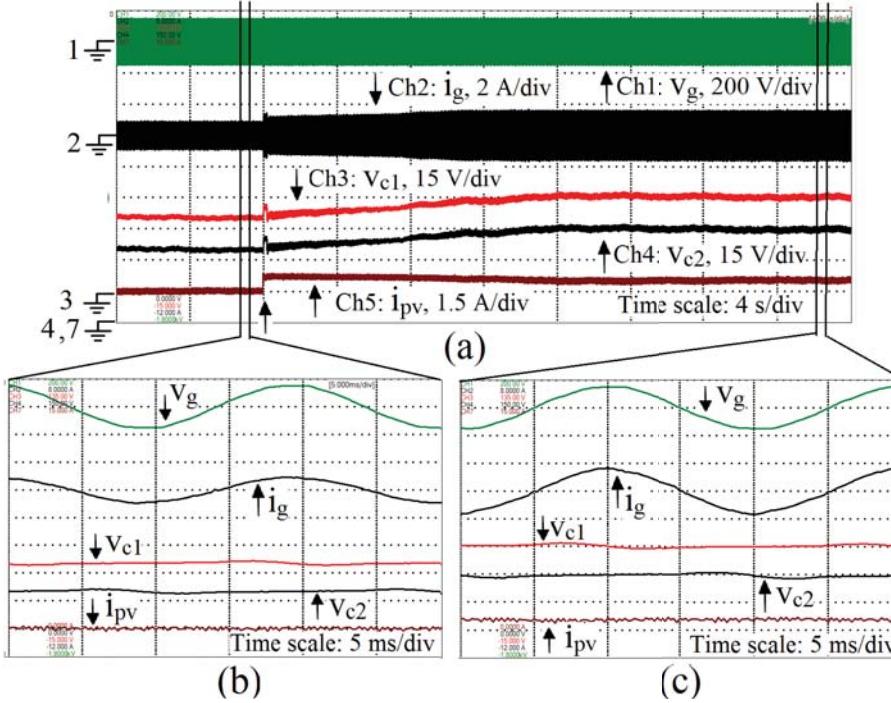


Figure 4.10: Experimental results: (a) response of the system subjected to step increment in MPP voltage and current, b) magnified view of the steady state response of the system before changes in MPP condition were made at instant t_1 , and c) magnified view of the steady state response of the system after changes in MPP condition were made,

Table 4.3: Comparison of estimated/calculated circuit losses

Scheme	loss at 1kW
H5 [33]	27.71 W [34]
HERIC [36]	23.03 W [34]
H6 [38]	25.37 W [34]
Proposed	38 W

the input stage of the inverter have been reported in [51]-[53]. The schemes reported in [51]-[52] can operate satisfactorily if both the PV panels are exposed to similar physical conditions. Further, the energy output from each of the PV panels are required to be stored in a capacitor connected across that PV panel for the duration of a half cycle of the grid voltage. This demands two large capacitors, one across each of the PV panels, to ensure maximum power extraction from both the panels by reducing the magnitude of voltage ripple across the panels. The schemes presented in [53] can extract maximum power from two PV panels but the inverter employed for this scheme is of buck type. This leads to the same limitations mentioned at the beginning of this paragraph.

In order to overcome the aforementioned limitations the proposed NPC base inverter is utilized to operate two PV panels at their respective MPPs thereby resulting in enhancement in power yield. The salient features of the scheme are as follows:

1. Maximum power extraction from two separate PV panels.
2. The inverter being of buck-boost type can support wide variation in both the PV

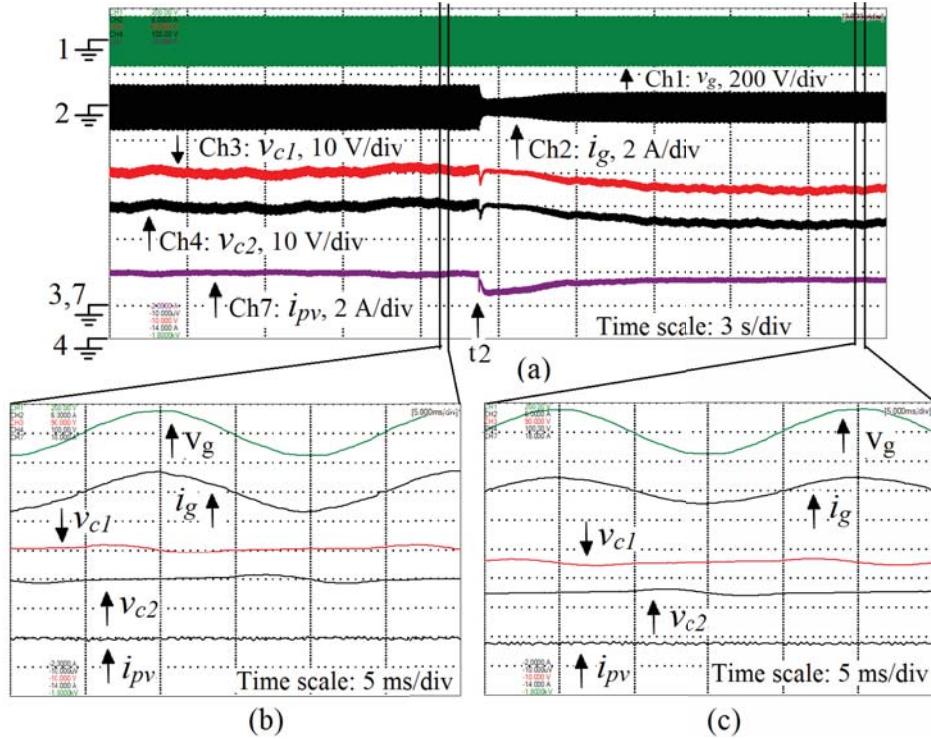


Figure 4.11: Experimental results: (a) response of the system subjected to step decrement in MPP voltage and current, b) magnified view of the steady state response of the system before changes in MPP condition were made at instant t_2 , and c) magnified view of the steady state response of the system after changes in MPP condition were made

panel voltages.

3. The neutral point clamped based structure of the inverter leads to elimination of leakage current problem
4. The inverter is free from shoot-through fault.
5. Out of the six inverter switches, four switches operate at grid frequency and only two switches operate at any given time.
6. Grid current is not required to be sensed.
7. Reduced safety concern as the maximum potential of any point on the input side of the inverter with respect to the ground is equal to the voltage of one PV panel.

The operating principle of the proposed topology is presented in the following Sub-section. The control strategy devised for the scheme is presented in Subsection 4.3.2. Design issues of the proposed topology are provided in Subsection 4.3.3. Detailed simulation results are presented in Subsection 4.3.4 to ascertain effectiveness of the scheme. Experimental results obtained from a laboratory prototype are presented in Subsection 4.3.5 to confirm viability of the scheme.

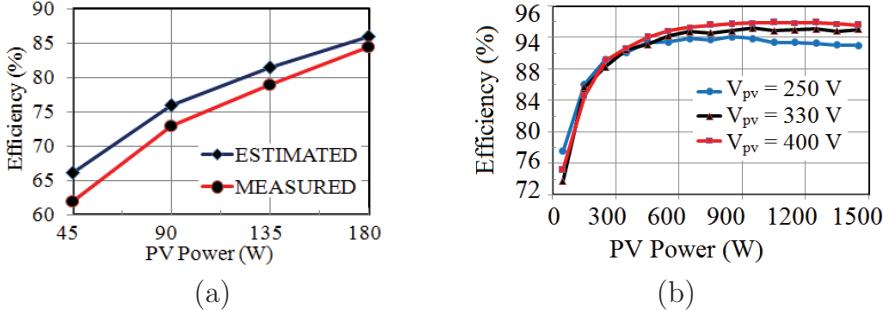


Figure 4.12: Efficiency curves of the proposed inverter: (a) measured and estimated efficiency curves when $V_{pv} = 90$ V and $V_g = 110$ V, and (b) estimated efficiency curves when $V_g = 230$ V and $V_{pv} = 250$ V, 330 V, and 400 V

Table 4.4: Comparison of the proposed inverter with other NPC inverters which can operate in buck-boost

	Aalborg [50]	Kasa [51]	proposed	Remarks
C_{in}	$\frac{1.91P}{2\omega V_c \Delta V_c}$	$\frac{1.91P}{2\omega V_c \Delta V_c}$	$\frac{P}{2\omega V_c \Delta V_c}$	Input capacitance requirement is 1.91 times less in the proposed scheme
O.S.	not guaranteed	not guaranteed	guaranteed	Aalborg and Kasa inverter requires both the PV panels to operate at the same condition which is not practical
η	98.1%	96.5%	95%	Efficiency in the proposed scheme is less, but it can be improved by designing the inverter to operate at CCM

C_{in} = input capacitance requirement, O.S.= operational symmetry in positive and negative half cycle of the grid voltage, η = estimated efficiency at 1 kW, V_c and ΔV_c = Voltage and ripple voltage across input capacitor, $\omega = 2\pi f_g$, f_g = grid frequency, P = total PV power (assuming two PV panels of Aalborg and Kasa inverters are operating at same condition)

4.3.1 Principle of Operation

The schematic circuit diagram of the proposed inverter is shown in Fig. 4.13. As shown in the figure, the inverter has two PV panels at its input. The midpoint of these two PV panels is connected to the neutral/ground terminal of the grid. This ensures either zero or constant voltage across the parasitic capacitances which exists between the PV panel and the ground thereby eliminating the leakage current flow through these capacitors. The inverter topology can be visualized as a combination two dc-dc buck-boost converters namely, CON1 and CON2. The converter, CON1 comprises of inductor, L_1 and switches, S_1 , S_2 , and S_3 . The other converter, CON2 is comprising of inductor, L_2 and switches, S_4 , S_5 , and S_6 . The switches, S_2 , S_3 , S_5 , and S_6 are required to have reverse voltage and reverse current blocking capability. Hence these switches can be realized either by employing reverse-blocking IGBTs (RB-IGBT) or a series combination of diode and IGBT/MOSFET. On the contrary, switches, S_1 , and S_4 , can carry current in forward direction only owing to the structure and operating principle of the inverter. Further, they need not have reverse voltage blocking capability. Hence they can be realized by employing IGBT/MOSFET with or without having anti-parallel body diode. The combination of inductor, L_f and capacitor, C_f is employed to filter the current injected to the grid. The converter is made to operate in discontinuous conduction mode (DCM). The

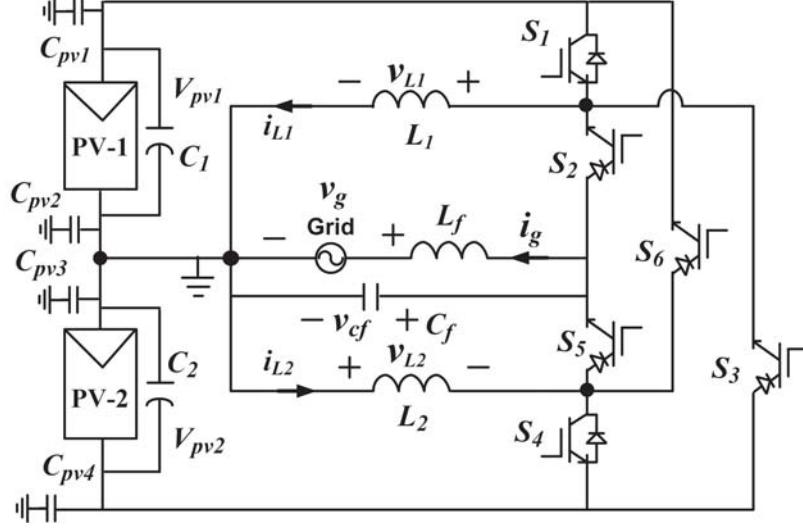


Figure 4.13: Schematic diagram of the proposed NPC inverter servicing two separate PV panels

operation of the inverter is explained as follows:

A. Operation in positive half cycle (PHC) of the grid voltage

I. Operation of CON1

The switch, S_2 is kept off and the switch S_3 is kept on while the duty ratio of switch, S_1 is controlled to maintain PV panel-1 voltage, v_{pv1} at a value corresponding to its maximum power point, v_{mpp1} . When S_1 is turned on, the current, i_{L1} flowing through L_1 , increases and hence L_1 stores energy received from PV panel-1. When S_1 is turned off, the stored energy in L_1 is supplied to the capacitor, C_2 , through S_3 , and i_{L1} decreases. Therefore, CON1 works as a buck-boost dc-dc converter in PHC with PV panel-1 at its input and C_2 at its output.

II. Operation of CON2

The switch S_6 is kept off and switch S_5 is kept on while duty ratio of switch, S_4 is controlled to maintain PV panel-2 voltage, v_{pv2} at a value corresponding to its maximum power point, v_{mpp2} . Since C_2 is connected across PV panel-2 and energy from PV panel-1 is getting transferred to C_2 through CON1, capacitor C_2 receives energy from both the PV panels. When S_4 is turned on, inductor L_2 stores energy from C_2 and its current, i_{L2} increases. When S_4 is turned off the stored energy in L_2 is supplied to the grid through switch, S_5 , and i_{L2} decreases. Therefore, during PHC, CON2 supplies power from both the PV panels to the grid.

The power flow diagram during PHC of the grid voltage is shown in Fig. 4.14(a) wherein P_{pv1} and P_{PV2} are the power output from panel-1 and panel-2 respectively.

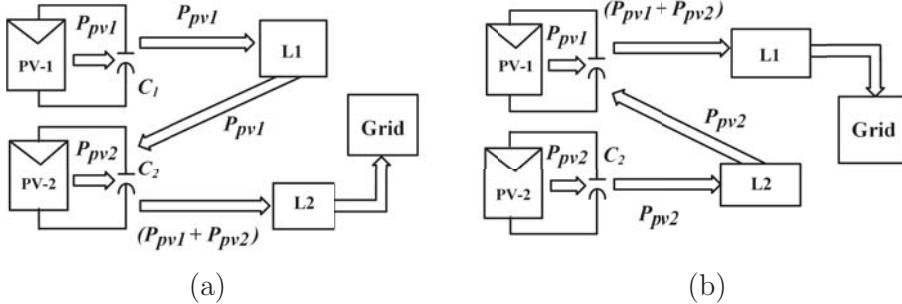


Figure 4.14: Power flow path of the inverter: a) during positive half cycle, and b) during negative half cycle

B. Operation in negative half cycle (NHC) of the grid voltage

I. Operation of CON1

The switch S_3 is kept off and S_2 is kept on while duty ratio of S_1 is controlled to maintain v_{pv1} at v_{mpp1} . In this half, C_1 is charged with energy received from both the PV panels (similar to charging of C_2 in positive half of grid voltage). When S_1 is turned on, inductor L_1 stores energy from C_1 and its current, i_{L1} increases. When S_1 is turned off the stored energy in L_1 is supplied to the grid through switch, S_2 and i_{L1} decreases. Thus, during NHC of grid voltage, CON1 supplies power from both the PV panels to the grid.

II. Operation of CON2

The operation of CON2 in NHC is similar to that of CON1 in PHC. The switch S_6 is kept on and S_5 is kept off while duty ratio of S_4 is controlled to maintain v_{pv2} at v_{mpp2} . In this half CON2 transfers energy from PV panel-2 to C_1 .

The power flow diagram during NHC of the grid voltage is shown in Fig. 4.14(b). The switching pulses for the six switches are depicted in Fig. 4.15. From this figure it can be noted that out of six switches, two switches are operating at switching frequency and four switches are operating at grid frequency.

The waveforms for the inductor currents, i_{L1} and i_{L2} along with their magnified views over an arbitrary switching cycle are shown in Fig. 4.15.

The voltage impressed across inductor, L_1 is given by,

$$\begin{aligned}
 v_{L1} &= v_{pv1} ; \text{ for } 0 < t < d_1 T_s \\
 &= v_{cfk} - v_{pv2}(1 - k) ; \text{ for } d_1 T_s < t < (d_1 + d'_1) T_s \\
 &= 0 ; \text{ for } (d_1 + d'_1) T_s < t < T_s
 \end{aligned}$$

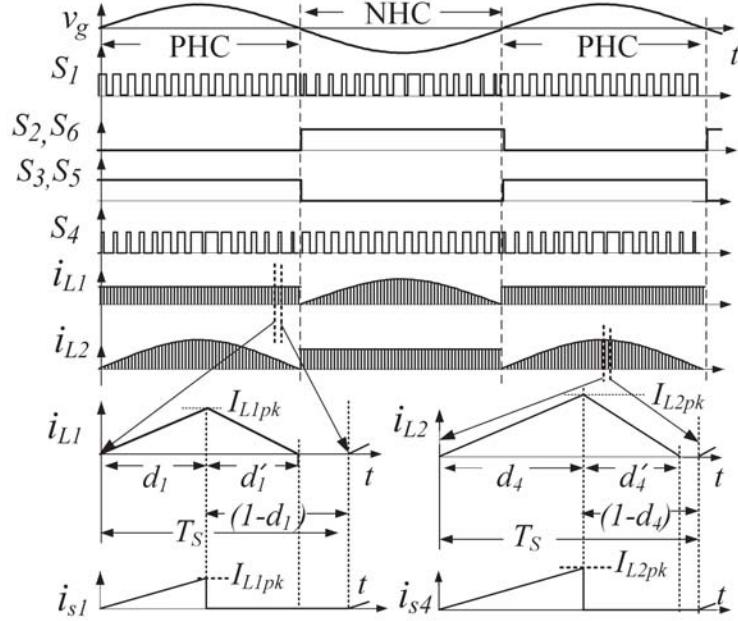


Figure 4.15: Switching pulses for the six switches of the proposed inverter and waveform of the inductor currents, i_{L1} and i_{L2} and their magnified view for an arbitrary switching cycle

wherein $k = 1$ in NHC and $k = 0$ in PHC. The magnitude of the peak current, i_{L1pk} flowing through the inductor, L_1 , is given by,

$$i_{L1pk} = \frac{V_{pv1}}{L_1} d_1 T_s \quad (4.11)$$

The average value of current flowing through the switch, S_1 is, given by,

$$I_{S1avg} = \frac{1}{2} d_1 i_{L1pk} = \frac{V_{pv1}}{2L_1} d_1^2 T_s \quad (4.12)$$

The average power received by CON1 during PHC can be expressed as,

$$P_{CON1pos} = P_{PV1} = V_{pv1} I_{S1pos} = \frac{V_{pv1}^2}{2L_1} D_{1pos}^2 T_s ; \quad [\text{using}(4.12)] \quad (4.13)$$

wherein, D_{1pos} is the average value of duty cycle of switch S_1 during PHC and I_{S1pos} is the average value of current flowing through switch, S_1 during PHC. The average power received by CON1 during NHC can be expressed as,

$$P_{CON1neg} = P_{PV1} + P_{PV2} = V_{pv1} I_{S1neg} = \frac{V_{pv1}^2}{2L_1} D_{1neg}^2 T_s \quad (4.14)$$

wherein, D_{1neg} is the average value of duty cycle of switch S_1 during NHC and I_{S1neg} is the average value of current flowing through switch, S_1 during NHC. The voltage impressed

across the inductor, L_2 is given by,

$$\begin{aligned} v_{L2} &= v_{pv2} ; \text{ for } 0 < t < d_4 T_s \\ &= -v_{cf}(1-k) - v_{pv1}k ; \text{ for } d_4 T_s < t < (d_4 + d'_4)T_s \\ &= 0 ; \text{ for } (d_4 + d'_4)T_s < t < T_s \end{aligned} \quad (4.15)$$

The magnitude of peak current, i_{L2pk} flowing through the inductor, L_2 is given by,

$$i_{L2pk} = \frac{v_{pv2}}{L_2} d_4 T_s$$

The average value of current flowing through the switch, S_4 is given by,

$$I_{S4avg} = \frac{1}{2} d_4 i_{L2pk} = \frac{V_{pv2}}{2L_2} d_4^2 T_s \quad (4.16)$$

The average power received by CON2 during PHC can be expressed as,

$$P_{CON2pos} = P_{PV1} + P_{PV2} = V_{pv2} I_{S4pos} = \frac{V_{pv2}^2}{2L_2} D_{4pos}^2 T_s$$

wherein, D_{4pos} is the average value of duty cycle of switch S_4 during PHC and I_{S4pos} is the average value of current flowing through S_4 during PHC. The average power received by CON2 during NHC can be expressed as,

$$P_{CON2neg} = P_{PV2} = V_{pv2} I_{S4neg} = \frac{V_{pv2}^2}{2L_2} D_{4neg}^2 T_s$$

wherein, D_{4neg} is the average value of duty cycle of switch S_4 during NHC and I_{S4neg} is the average value of current flowing through switch, S_4 during NHC.

From the above discussion it can be concluded that as voltages of the two PV panels can be controlled in a decoupled manner, each of the PV panel can be operated at its maximum power point. Hence this scheme can deliver the sum of the maximum powers extracted from the individual panels while they experience different operating conditions.

4.3.2 Control Strategy

The control strategy devised for the proposed inverter is shown in Fig. 4.16. Two dedicated MPP trackers are employed to generate reference voltage commands for each of the PV panels so as to operate them at their respective maximum power points. The sensed PV panel voltages are compared with their respective reference voltage commands and the errors are processed through proportional integral (PI) controllers and subsequently manipulated to generate required duty ratios, d_1 for switch, S_1 and d_4 for switch, S_4 . The duty ratio, d_1 (or d_4) is derived directly from the output of the PI-1 (or PI-2) when CON1 (or CON2) is feeding power to C_2 (or C_1). However, d_1 (or d_4) is made a sinusoidally varying function in that half cycle of the grid voltage when CON1 (or CON2) is feeding power to the grid in order to make the injected current to the grid sinusoidal. A unit sinusoidal function synchronized to the grid voltage is obtained by employing a phase locked loop (PLL) algorithm. This function is then rectified and multiplied with

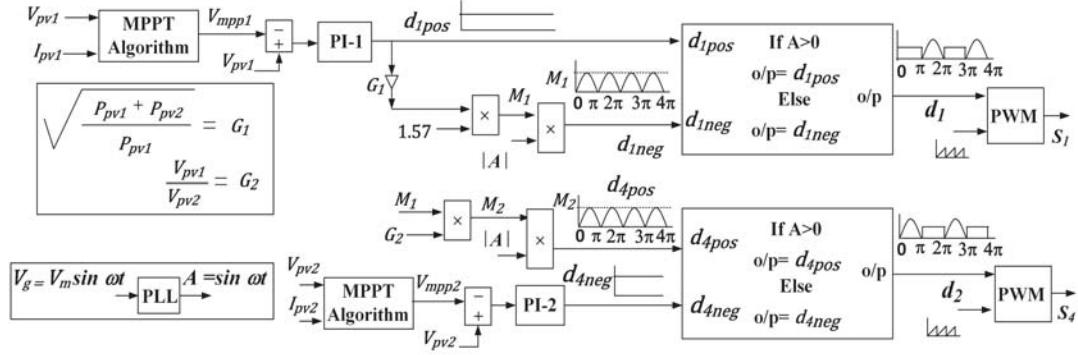


Figure 4.16: Control structure of the proposed inverter for operation in DCM

the output of PI-1 (or PI-2) to generate the sinusoidally varying d_1 (or d_4) in the required half cycle of the grid. In addition to these, the sinusoidally varying part of the duty ratios, d_1 and d_4 are multiplied with gains, G_1 and G_2 respectively, the significance of which are explained below.

a. Design and Significance of G_1

During PHC of the grid voltage, CON1 processes the power of PV panel-1, P_{PV1} and hence the average value of current, I_{S1pos} flowing through switch, S_1 in this half cycle can be expressed as,

$$I_{S1pos} = \frac{P_{PV1}}{V_{pv1}} \quad (4.17)$$

From (4.12), I_{S1pos} can also be expressed as,

$$I_{S1pos} = \frac{V_{pv1}}{2L_1} D_{1pos}^2 T_s \quad (4.18)$$

From (4.17) and (4.18),

$$D_{1pos}^2 = \frac{2L_1 P_{PV1}}{V_{pv1}^2 T_s} \quad (4.19)$$

During NHC of grid voltage CON1 has to process powers available from both the PV panels. Following the similar treatment employed for derivation of D_{1pos} , the average value of duty ratio of S_1 for the NHC, D_{1neg} can be expressed as,

$$D_{1neg}^2 = \frac{2L_1(P_{PV1} + P_{PV2})}{V_{pv1}^2 T_s} \quad (4.20)$$

From (4.19) and (4.20),

$$D_{1neg} = D_{1pos} \sqrt{\frac{P_{PV1} + P_{PV2}}{P_{PV1}}} \quad (4.21)$$

or, $D_{1neg} = G_1 D_{1pos}$

wherein $G_1 = \sqrt{\frac{P_{PV1}+P_{PV2}}{P_{PV1}}}$. Therefore, the incremental power to be processed by CON1 in NHC is being estimated beforehand through the inclusion of G_1 and thereby generating D_{1neg} . A half sinusoid having its average value as D_{1neg} is generated to obtain sinusoidally varied duty ratio for S_1 during NHC and the amplitude of this half sinusoid is given by,

$$M_1 = \frac{\pi}{2}D_{1neg} = 1.57D_{1neg} \quad (4.22)$$

The shape of d_{1pos} , d_{1neg} and d_1 is also shown in Fig. 4.16.

b. Design and Significance of G_2

Since both the PV panels are controlled at their respective MPPs, V_{pv1} and V_{pv2} may or may not be equal. As the inverter is operated in DCM, dc current injection into the grid can be avoided if the peak current profile through L_1 in the NHC is kept equal to peak current profile through L_2 in the positive half. The peak current, $i_{L1pkneg}$ flowing through the inductor L_1 in a switching cycle in the NHC of the grid voltage, and the peak current, $i_{L2pkpos}$ flowing through the inductor, L_2 in the PHC of the grid voltage can be expressed as,

$$i_{L1pkneg} = \frac{v_{pv1}}{L_1} M_1 |\sin \omega t| T_s, \quad (4.23)$$

$$i_{L2pkpos} = \frac{v_{pv2}}{L_2} M_2 |\sin \omega t| T_s \quad (4.24)$$

wherein M_2 is amplitude of the duty ratio of switch, S_4 in the PHC of the grid voltage. In order to ensure required profiles for $i_{L1pkneg}$ and $i_{L2pkpos}$ so as to prevent dc current injection into the grid, the desirable relationship between M_1 and M_2 , from (4.23) and (4.24) is,

$$M_2 = \frac{V_{pv1}}{V_{pv2}} M_1 = G_2 M_1, \quad [\text{as } L_1 = L_2] \quad (4.25)$$

wherein, $G_2 = \frac{V_{pv1}}{V_{pv2}}$.

c. Effect of G_2 on the amount of power processed by CON2 in the PHC

The average value of duty ratio, D_{4pos} of S_4 in the PHC can be expressed as,

$$D_{4pos} = \frac{2}{\pi} M_2 \quad (4.26)$$

From (4.26), (4.25) and (4.22),

$$D_{4pos} = \frac{V_{pv1}}{V_{pv2}} D_{1neg} \quad (4.27)$$

From Fig. 4.15, the average value of current, I_{S4pos} flowing through the switch, S_4 in the

PHC can be expressed as,

$$\begin{aligned}
I_{S4pos} &= \frac{V_{pv2}}{2L_2} D_{4pos}^2 T_s \\
I_{S4pos} &= \frac{V_{pv2}}{2L_2} \left[\frac{V_{pv1}}{V_{pv2}} D_{1neg} \right]^2 T_s, \text{ using (4.27)} \\
I_{S4pos} &= \frac{V_{pv2}}{2L_2} \left[\frac{V_{pv1}}{V_{pv2}} \right]^2 \frac{2L_1 I_{S1neg}}{V_{pv1}}, \text{ using (4.12)} \\
I_{S4pos} &= \frac{V_{pv1} I_{S1neg}}{V_{pv2}}, [\text{as } L_1 = L_2] \\
I_{S4pos} V_{pv2} &= V_{pv1} I_{S1neg}
\end{aligned} \tag{4.28}$$

From (4.28) it can be inferred that the average power received by CON1 in the NHC of the grid voltage is same as that of received by CON2 in the PHC. Therefore it can be concluded that in each of its half cycle the grid is fed with same power even though power extracted from the two PV panels may be different.

4.3.3 Selection Criteria of Various Passive Elements

The selection criteria of various passive elements for operation of the proposed inverter in DCM is as follows:

a. Selection of L_1 and L_2

The values of L_1 and L_2 are chosen so that CON1 and CON2 operate under DCM while they are required to negotiate peak power. Following the procedure presented in [47], the critical values of L_1 and L_2 can be expressed as,

$$L_{critical} = \frac{0.25}{P_{max}} \frac{T_s}{v_{gm}} \left[\frac{1}{v_{gm}} + \frac{1}{v_{max}} \right]^{-2} \tag{4.29}$$

wherein, P_{max} is the summation of individual peak powers extracted from both the PV panels, v_{max} is the expected peak voltage of PV panels at MPP, v_{gm} is the peak value of grid voltage and T_s is the switching time period. The values of L_1 and L_2 , henceforward referred as L in this chapter, must be less than $L_{critical}$ for operation of the proposed inverter in DCM.

b. Selection of C_1 and C_2

The capacitors connected in parallel with the PV panels, C_1 and C_2 are designed, as per guidelines provided in [25], as follows:

$$C_1 = C_2 = \frac{I_{max}}{4\pi f_g \Delta v_{pv}} \tag{4.30}$$

wherein, I_{max} is the maximum value of PV panels current at MPP, Δv_{pv} is the ripple across PV panel voltages and f_g is the grid frequency.

c. Selection of L_f and C_f

The grid side filters, L_f and C_f are designed based on expressions provided in [47] and are as follows:

$$C_f = \frac{T_s^2}{4Lv_{gm}\Delta v} \left[\frac{1}{v_{gm}} + \frac{1}{v_{max}} \right]^{-2}$$

$$L_f = \frac{1}{(2\pi f_c)^2 C_f}$$

wherein, Δv is the ac voltage ripple in C_f , f_c is the cut-off frequency of filter.

4.3.4 Simulated Performance

In order to confirm the efficacy of the proposed scheme, detailed simulation studies are carried out on Matlab/Simulink platform. Various components/elements considered for the simulation study are provided in Table 4.5.

Table 4.5: Parameters/elements considered for simulation studies

Parameter	Value
grid voltage, V_g	230 V, 50 Hz
$L_1 = L_2$	0.1 mH
$C_1 = C_2$	3300 μ F
grid side filter, C_f & L_f	2 μ F & 5 mH
Switching frequency, F_s	15 kHz
MPPT algorithm	Incremental conductance

Test 1: The objective of this test is to evaluate the performance of the inverter when difference in output voltage of the two PV panels is small but difference in the magnitude of powers extracted from them are considerable. This situation is similar to the condition wherein the two PV panels are operating at same temperature but experiencing different insolation (S) levels. The temperature for both the panels is maintained at 25° C. The insolation level for PV panel-1 is kept fixed at 850 W/m^2 . The insolation level for PV panel-2 is varied with time and it is chosen as follows: 1000 W/m^2 from 0 - 2 s, 850 W/m^2 from 2 - 3.5 s and 700 W/m^2 from 3.5 s onwards. The output powers of the two PV panels are shown in Fig. 4.17(a). The voltage across each of the PV panels and their magnified views at a given steady state condition are shown in Fig. 4.17(b) and Fig. 4.17(c) respectively. From Fig. 4.17(c) it can be noted that PV panel voltages has a 50 Hz dominant ripple component as compared to 100 Hz ripple component generally experienced while power from a PV panel is processed through a single phase inverter. This phenomenon is observed in the proposed scheme as a PV panel feeds power to the grid only for one half cycle of the grid voltage.

The steady state profile of inductor currents, i_{L1} and i_{L2} , are shown in Fig. 4.18(a) and Fig. 4.18(b) respectively. From Fig. 4.18 it can be noted that profile of peak current

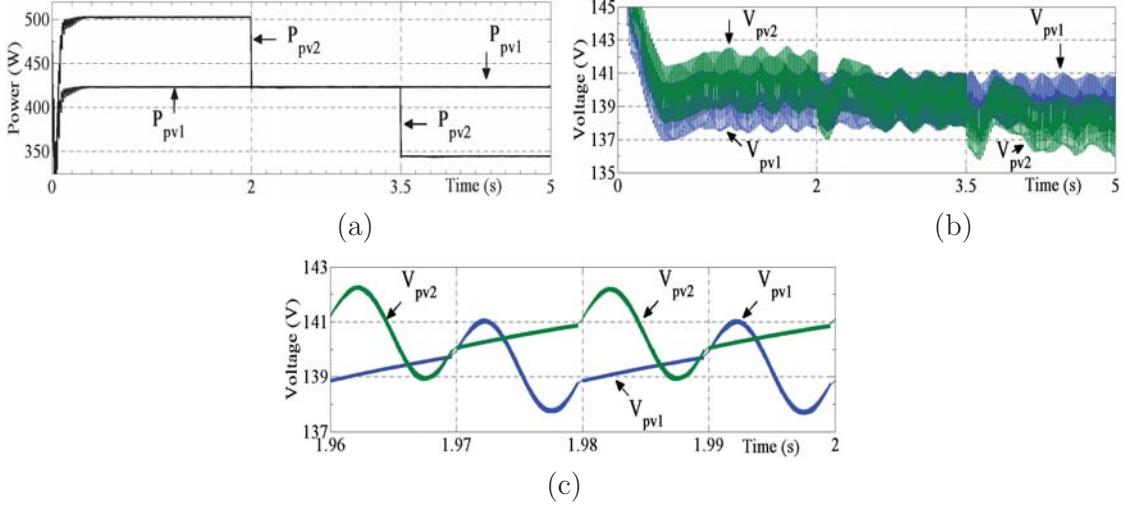


Figure 4.17: Simulated response for conditions pertaining to test1: (a) power output from the individual PV panels, (b) voltages across the PV panels, and (c) magnified views of voltages across the PV panels

flowing through L_2 in the PHC of the grid voltage is identical to the profile of peak current flowing through L_1 in the NHC.

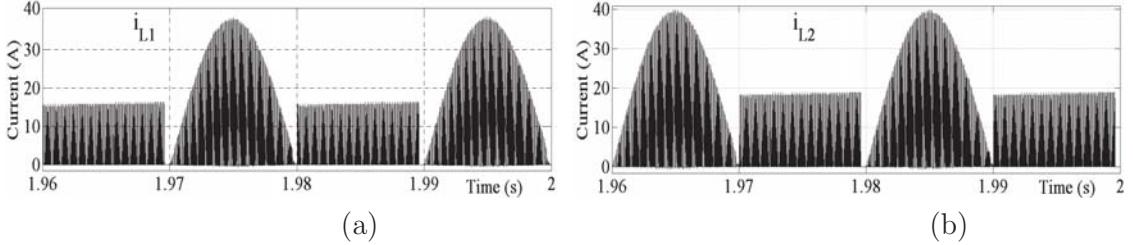


Figure 4.18: Simulation results showing current flowing through the inductors, a) i_{L1} , and b) i_{L2} at a given steady state condition during test1

The current that is fed to the grid and its magnified version along with the grid voltage at a steady state operating condition is shown in Fig. 4.19(a) and Fig. 4.19(b) respectively. From Fig. 4.19(b) it can be inferred that the grid current is in phase with the grid voltage. The plot showing total harmonic distortion (THD) of the grid current is shown in Fig. 4.19(c) which confirms that the THD of the grid current is lower than maximum allowable limit of 5% [25]. The magnitude of dc current injected to the grid is approximately 0.05%.

Test 2: The objective of this test is to examine the performance of the inverter while difference in output voltages of the two PV panels as well as difference in the magnitude of powers extracted from the PV panels are considerable. This condition emulates the situation wherein both the PV panels are experiencing large difference in temperature

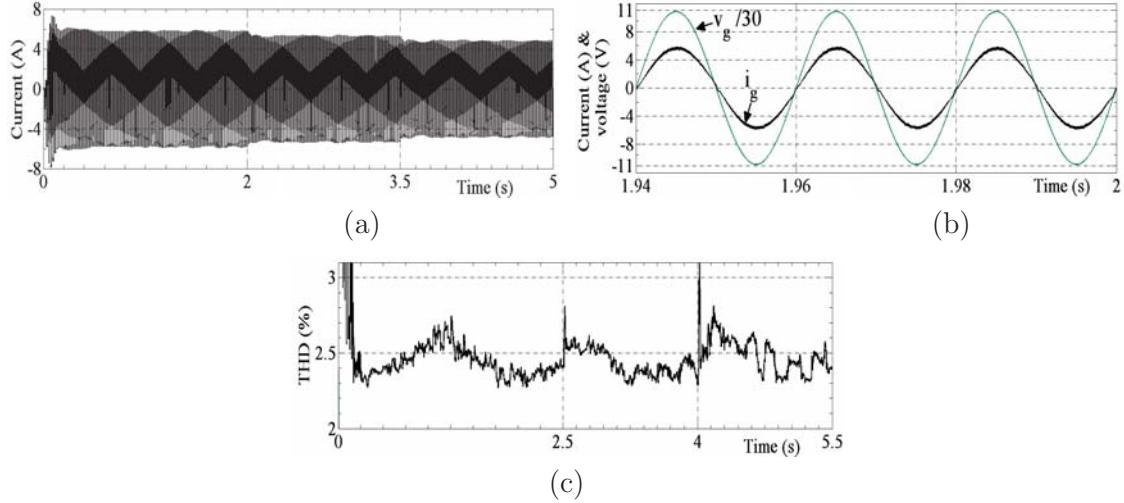


Figure 4.19: Simulated response for conditions pertaining to test1: a) current injected to the grid, b) magnified view of grid voltage and current injected to the grid, and c) THD plot of the grid current

and insolation levels. The temperature for PV panel-1 and PV panel-2 are maintained at 40^0 C and 25^0 C respectively. The insolation level for PV panel-1 is kept fixed at 800 W/m^2 . The insolation level for PV panel-2 is varied with time and it is chosen as follows: 1000 W/m^2 from $0 - 2.5\text{ s}$, 900 W/m^2 from $2.5 - 4\text{ s}$ and 700 W/m^2 from 4 s onwards. The output powers of the two PV panels are shown in Fig. 4.20(a). The voltage across each of the PV panels is shown in Fig. 4.20(b).

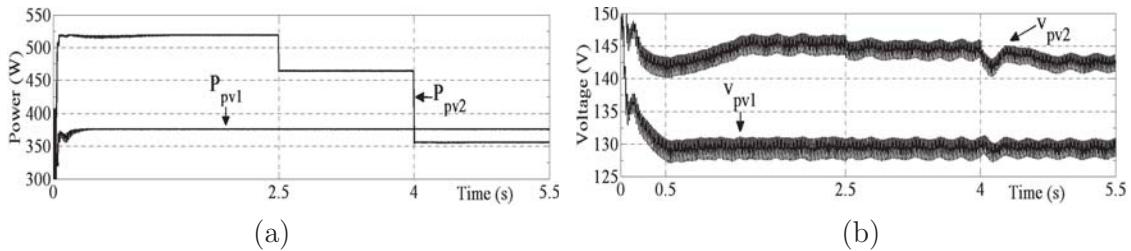


Figure 4.20: Simulated response for conditions pertaining to test2: a) power output from the individual PV panels, and b) voltages across the PV panels

The current that is fed to the grid and its magnified version along with the grid voltage at a steady state operating condition are shown in Fig. 4.21(a) and Fig. 4.21(b) respectively. The plot showing total harmonic distortion (THD) of the grid current is provided in Fig. 4.21(c). The steady state profile of currents, i_{L1} and i_{L2} are shown in Fig. 4.21(d) wherein it can be noted that profile of peak current flowing through L_2 in the PHC of the grid voltage is identical to the profile of peak current flowing through L_1 in the NHC.

From the above two tests it can be concluded that the proposed inverter can work satisfactorily under wide range of differences in operating conditions on the two PV panels.

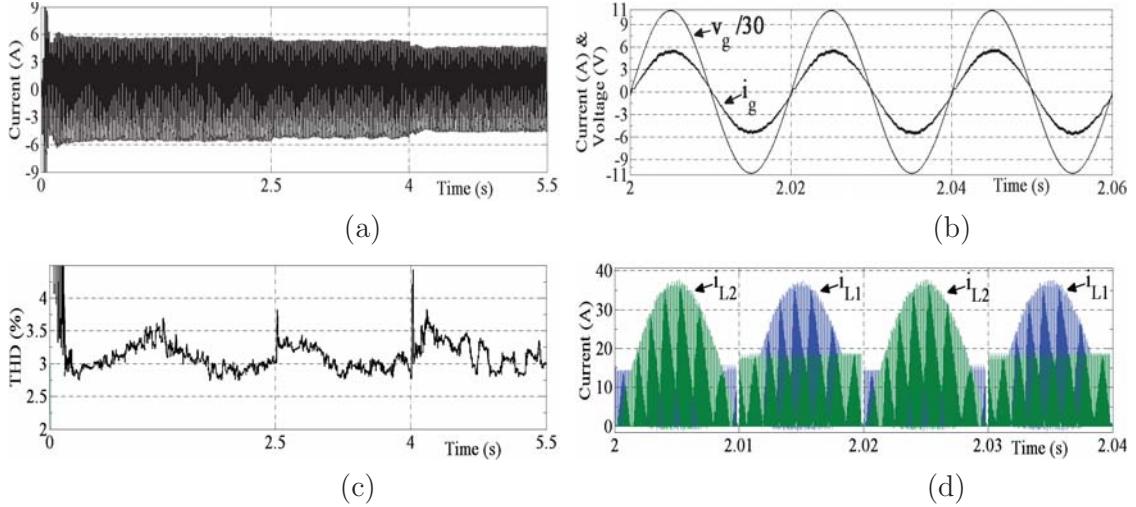


Figure 4.21: Simulated response for conditions pertaining to test2: a) current injected to the grid, b) magnified view of grid voltage and current injected to the grid, c) THD plot of the grid current, and d) current flowing through inductors, L_1 and L_2 .

4.3.5 Experimental Results

In order to ascertain the viability of the proposed inverter a scaled down laboratory prototype is developed. Two independent modules of Agilent make solar panel simulator, E4360A is employed to realize PV panel-1 and PV panel-2. This simulator generates PV characteristic curves for each of the modules based on four input signals viz. V_{mp} , I_{mp} , V_{oc} and I_{sc} . Texas Instruments make floating-point DSP, TMS320F28335 is employed to realize the controller. Enhanced phase lock loop (ePLL) is employed to obtain phase information of the grid voltage [96]. Relevant parameters/elements used to realize the laboratory prototype are provided in Table 4.6.

Table 4.6: Parameters/elements employed in laboratory prototype

Parameter	Value/range
Gird Voltage, v_g	110 V
PV Voltages, V_{pv1} & V_{pv2}	50-88 V
PV Currents, I_{pv1} & I_{pv2}	0-3 A
C_{pv1} , C_{pv1} , C_f , L_f , L_1 , L_2	as given in Table 4.5
MPPT algorithm	Incremental conductance
Switch, S_1 & S_4	IRG7PH42UPbF
Switch, S_2 , S_3 , S_5 & S_6	IXRH40N120
Switching frequency for S_1 & S_4	15 kHz

The steady state response of the system when both the PV panels are operating under the same condition is shown in Fig. 4.22. The MPP voltages and MPP currents are set as 70 V and 2 A respectively for both the PV panels. From Fig. 4.22(a) it can be observed that both the PV panel voltages are 70 V and both the PV panel currents are 2 A. Hence both the PV panels are operating at their respective MPPs. Further, it can be noted that the grid current is in phase with the grid voltage and it is fairly sinusoidal. The frequency

spectrum of the grid current is shown in Fig. 4.22(b) wherein the THD in grid current is observed to be 4.18%. The magnitude of dc component in grid current is 0.1%.

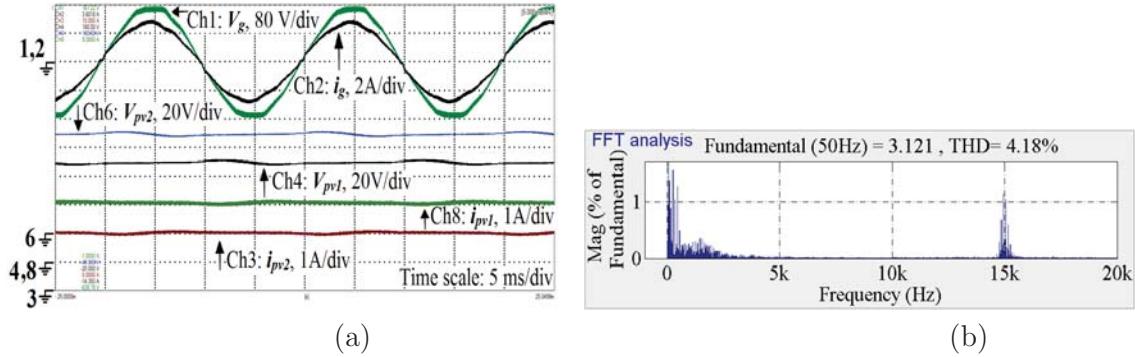


Figure 4.22: Experimental result showing response of the system when both the PV panels are operating under same condition. a) steady state response and b) Frequency spectrum of the grid current

The steady state response of the scheme when the PV panels are operating under mismatched conditions is shown in Fig. 4.23. The MPP values for PV panel-1 are set as: $V_{mpp1} = 70 \text{ V}$ and $I_{mpp1} = 2 \text{ A}$. The MPP values for PV panel-2 are set as: $V_{mpp2} = 60 \text{ V}$ and $I_{mpp2} = 1.5 \text{ A}$. From Fig. 4.23 it can be inferred that PV panel-1 voltage and current are 70 V and 2 A respectively while voltage and current of the PV panel-2 are 60 V and 1.5 A respectively. Hence it is objectively shown that both the PV panels are operating at their respective MPPs. The magnified view of Fig. 4.23(a) is shown in Fig. 4.23(b) to highlight the dominant 50 Hz ripple components present in voltages and currents of the PV panels. It can also be noted that the grid current is in phase with the grid voltage and it is fairly sinusoidal. The frequency spectrum of the grid current is shown in Fig. 4.23(c) wherein the THD in grid current is observed to be 4.29%. The magnitude of dc component in grid current is 0.12%.

The response of the system when PV panels are subjected to changes in operating conditions is shown in Fig. 4.24(a). The variation in operating condition is effected by changing MPP values manually in the solar panel simulator for PV panel-1 as follows: $V_{mpp1} = 60 \text{ V}$, $I_{mpp1} = 1.5 \text{ A}$ till instant t_1 , $V_{mpp1} = 70 \text{ V}$, $I_{mpp1} = 2 \text{ A}$ from instant t_1 to t_2 , and $V_{mpp1} = 60 \text{ V}$, $I_{mpp1} = 1.5 \text{ A}$ from instant t_2 onwards. The MPP values for PV panel-2 are kept to be fixed at $V_{mpp2} = 60 \text{ V}$ and $I_{mpp2} = 1.5 \text{ A}$. From Fig. 4.24(a) it can be noted that PV panel-2 voltage and current are maintained at 60 V and 1.5 A respectively while the PV panel-1 voltage and current gets adjusted corresponding to their MPP values set for the given time slot. This confirms capability of the inverter to track MPP of each of the PV panels when subjected to changes in operating conditions.

The steady state profile of currents, i_{L1} and i_{L2} flowing through the inductors, L_1 and L_2 along with the grid voltage and grid current are shown in Fig. 4.24(b). From this figure it can be inferred that the profile of peak current flowing through L_2 in the PHC of the grid voltage is identical to the profile of peak current flowing through L_1 in the NHC.

In order to measure efficiency of the scaled down laboratory prototype following procedure is adopted. The voltages of two PV panels are maintained at 90 V which is the

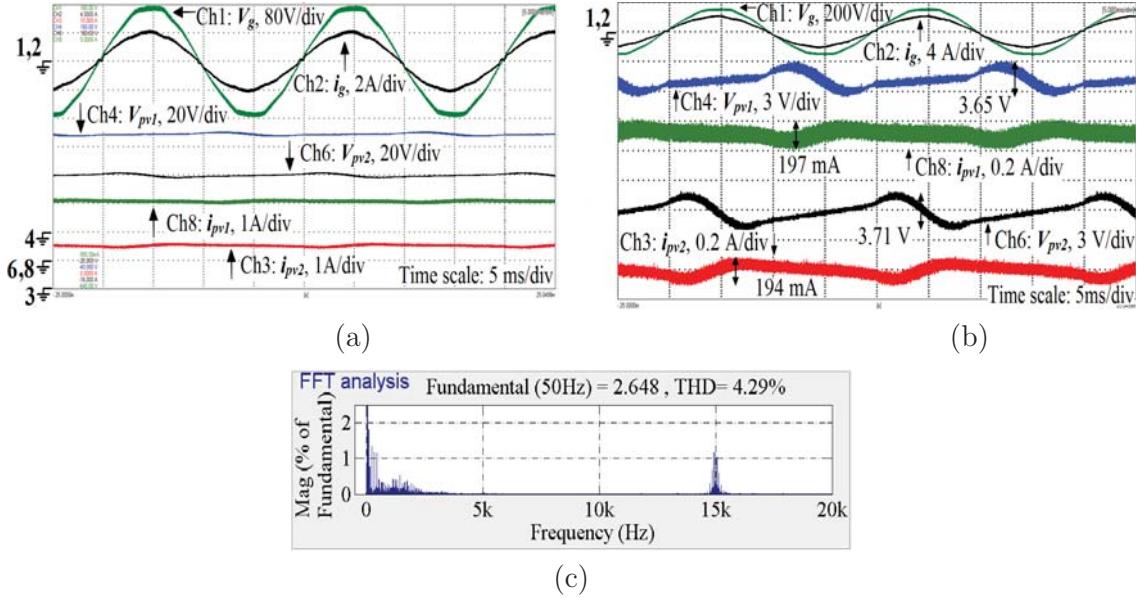


Figure 4.23: Experimental result showing steady state response of the system when PV panels are operating under mismatched condition. a) steady state response, b) magnified view of the steady state response, and c) frequency spectrum of the grid current

maximum voltage level of the solar simulator, E4360A employed for experimental study. The PV panel currents are increased in steps and the PV power outputs from both the panels are noted from the display of E4360A. The grid voltage is maintained at 110 V. The power fed to the grid is measured utilizing the power analyzer, PM100. The grid power thus obtained is then divided by the total power from both the PV panels to obtain efficiency curve of the proposed inverter which is depicted in Fig. 4.25. The efficiency curve so obtained is the global efficiency of the inverter which includes losses incurred in all the active and passive elements of the inverter. From this figure it can be noted that the efficiency of the inverter is low. However, the measured efficiency of the experimental set-up happens to be low as the PV panel voltages are kept low due to the constraint imposed by E4360 (which leads to more current and hence more conduction losses), and the inverter is operated in part loading condition. In order to obtain efficiency curve of the proposed inverter for its desired range of operation, estimation of the efficiency is carried out following the loss calculation of various passive and active elements as reported in [99]-[100]. The efficiency is calculated as (PV power - total loss)/PV power. At first, the estimation is carried out for PV panel voltage of 90 V which is same as that of the voltage employed for the experimental study. This is done to check the accuracy of the estimation procedure employed. The estimated efficiency curve while the PV panel voltage is maintained at 90 V is also depicted in Fig. 4.25. From this figure it can be inferred that the estimated efficiency curve is in close agreement with the measured efficiency curve. Hence it can be concluded that the procedure for estimating the efficiency of the system following the procedure presented in [99]-[100], is quite realistic. Subsequently, the overall efficiency curve of the system is estimated for the entire range of its operation and is

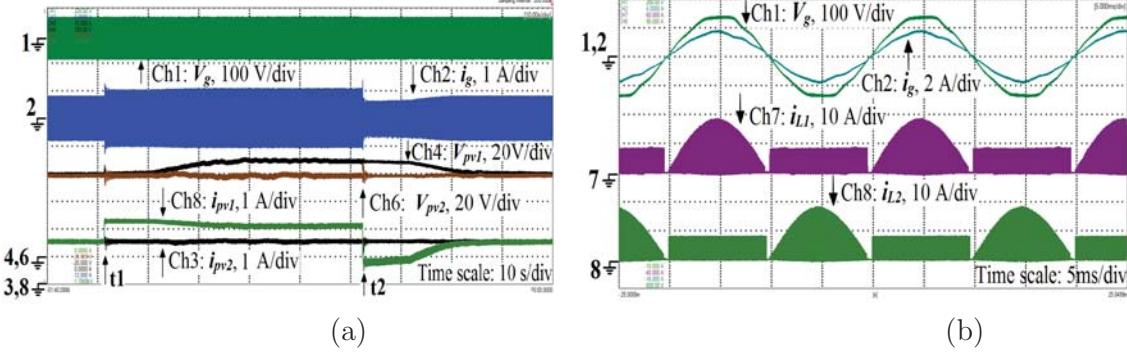


Figure 4.24: Experimental result: (a) response of the system when subjected to changes in operating condition and (b) steady state profile of inductor currents, i_{L1} and i_{L2} along with grid voltage and current being fed to the grid

depicted in Fig. 4.25. From this figure it can be observed that the efficiency in the order of 94.8% is achieved from the proposed inverter.

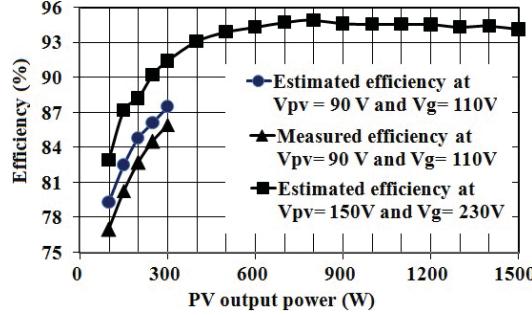


Figure 4.25: Efficiency curves of the proposed inverter: Measured and estimated efficiency curve with $V_{pv1} = V_{pv2} = 90\text{ V}$ and $V_g = 110\text{ V}$; and estimated efficiency curve with $V_{pv1} = V_{pv2} = 150\text{ V}$ and $V_g = 230\text{ V}$

Comparison of the proposed inverter with existing transformerless buck type inverters: The efficiency of the standard transformerless H-bridge or NPC based buck type inverters is around 97-98%. Hence, the efficiency of the proposed inverter is approximately 2.5% less as compared to these inverters. However, the amount of power that can be extracted from the PV panel(s) is more in case of the proposed scheme as the two PV panels can be operated at their respective MPPs irrespective of the prevailing operating conditions being experienced by each of them. In order to estimate the amount of power gain in the proposed scheme with respect to a standard scheme which employs a single PV panel of 400 V, following procedure is employed. The scheme presented in [37] is considered as a reference scheme for the purpose of comparison. First, a 400 V PV panel having capability to generate 1500 W power at standard test condition (STC) is taken and then it is divided into two panels, P-A and P-B connected in series. Each of these panels is having a voltage level of 200 V and power generation capability of 750 W

at STC. The insolation level and temperature of P-A is kept fixed at 1 kW/m^2 and 25°C respectively which corresponds to STC. The temperature on the P-B is maintained at 25°C , however, its insolation level is varied in steps from 1 kW/m^2 to 0.5 kW/m^2 . These variation in insolation level is purposefully applied to emulate the condition of shading in one of the panels (considered to be P-B in the present case). In order to define the extent of shading, a factor SF (shading factor) is introduced which is defined as, $\text{SF} = \text{S}_1/\text{S}_2$, wherein S1 and S2 are the insolation levels of P-A and P-B respectively. Two bypass diodes are connected across both the panels to take care of shading. This results in the existence of two MPPs in the P-V characteristics of the overall system and out of these two, the point which corresponds to the maximum power is termed as global MPP (GMPP) in the literature. It is assumed that the scheme presented in [37] is made to operate at the GMPP. The overall power extracted from the panels is estimated, as SF is varied from 1 to 2. This is then multiplied by the efficiency of the reference inverter ([37]) at the respective operating points to obtain the amount of power being fed to the grid. The same procedure is followed for the inverter proposed in this paper. However, the voltage level for each of the two PV panels is maintained at 150 V as the proposed inverter is operated in buck-boost mode. The grid voltage and power output from the panels at STC are kept same as that of the case which is considered for the reference inverter. The detailed results so obtained for the two cases are presented in Table 4.7. From this table it can be inferred that though the efficiency of the proposed inverter is marginally less, the amount of power it can inject into the grid in case of shading (or mismatched operating condition) is much higher than that of a standard scheme. The results obtained from the aforementioned table is plotted in Fig. 4.26 which depicts the additional amount of power that can be fed to the grid by utilizing the proposed scheme in comparison to that of a standard scheme. From this figure it can be inferred that an additional 280 W of power is fed to the grid in the proposed scheme when SF is 2. In addition, the proposed inverter has several advantages over transformerless buck type inverters which are as follows: (a) capability to operate in buck-boost mode thereby allowing wide variation in PV panel voltage, (b) tolerant to shoot through fault thereby improving reliability, (c) elimination of grid current sensor requirement, and (d) reduced safety concern as voltage level at any point on the PV side with respect to ground is the voltage of one PV panel which is around 150 V while in traditional scheme it is more than 400 V.

Comparison of the proposed inverter with existing transformerless buck-boost inverters: A comparison of the proposed inverter with existing transformerless inverters which operate in buck-boost principle is presented in Table 4.8. From this Table it can be inferred that the efficiency of the proposed inverter is similar to those of existing buck-boost inverters. However, the proposed inverter is the only buck boost inverter which is having the capability of extracting maximum power form two separate PV panels. Hence the amount of power extracted from the PV is more in case of the proposed scheme while the panels are operating under mismatched operating conditions. As the amount of extracted power is more and efficiency remains the same as those of existing buck-boost inverters, the amount of power injected to the grid is more in case of

Table 4.7: Comparison of performance of the proposed inverter with a standard inverter for different shading conditions

S1	S2	SF =S1/S2	P_c [W]	P_p [W]	η_c	η_p	G_c , [W] = $P_c * \eta_c$	G_p , [W] = $P_p * \eta_p$	P_g , [W] = $G_p - G_c$
1	1	1	1500	1500=(750+750)	0.97	0.945	1455	1418	-37
1	0.9	1.11	1391	1418=(750+668)	0.97	0.946	1349	1341	-8
1	0.8	1.25	1252	1336=(750+586)	0.971	0.946	1216	1264	48
1	0.7	1.43	1102	1257=(750+507)	0.972	0.947	1071	1190	119
1	0.6	1.67	948	1179=(750+429)	0.97	0.948	920	1118	198
1	0.5	2	790	1102=(750+352)	0.97	0.948	766	1046	280

S1 and S2 are the insolation levels of P-A and P-B respectively (in kW/m^2); SF is the shading factor; P_c and P_p = power output from the PV panels in case of the reference scheme (RS) and the proposed scheme (PS) respectively; η_c and η_p are the efficiencies of RS and PS respectively; G_c and G_p are the powers fed to the grid in case of RS and PS respectively; P_g is the amount of power gained in case of the proposed scheme

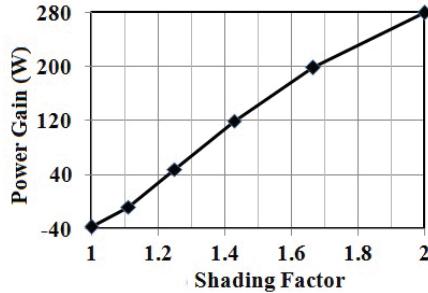


Figure 4.26: Amount of power gain in case of the proposed inverter as compared to that of a standard transformerless inverter [37]

the proposed scheme under mismatched operating conditions.

Comparison of the proposed inverter with existing micro-inverters: The efficiency of the existing micro-inverters is slightly higher/comparable to that of the proposed inverter. However, the power rating for which the micro-inverters can be designed (typically 300-500 W) is considerably less while the proposed scheme can be designed for power rating in excess of 3 kW [97]. This leads to increased cost and size requirement if micro-inverter based topology is adopted for a given power rating.

4.4 Decentralized Grid Connected NPC Inverter Capable of Negotiating dc Loads

The decentralized grid connected systems are generally installed in residential and commercial premises. It is projected that in near future residential dc microgrid will become a reality [101] - [103]. This dc microgrid will be fed from the locally installed renewable sources like solar PV and as well as by the ac grid. However, the interconnection

Table 4.8: Comparison of the proposed scheme with transformerless grid connected schemes based on buck-boost principle

Scheme	N_s	N_d	N_L	N_c	S_s		S_g	S_c		η	T	$N_{pv} = 2?$
					pos	neg		pos	neg			
[46]	4	2	2	3	1	1	2	2	2	#	#	No
[47]	5	3	2	2	2	1	3	2	2	86%	4.9%	No
[51]	4	2	3	3	1	1	2	2	2	#	#	No
[52]	6	6	3	3	1	1	2	2	2	#	#	No
[97]	4	2	3	2	1	1	2	1	1	80%	6%	No
Proposed *	6	4	3	3	2	2	4	2	2	85.7 %	4.3%	Yes

N_s = No. of switch, N_d = No. of diode, N_L = No. of inductor, N_c = No. of capacitors, S_+ = No. of switches operating at switching frequency, S_- = No. of switches operating at grid frequency,

S_c = No. of switches conducting at a time, η and T= measured efficiency and THD of grid current when PV power is around 200W to 300 W, pos= PHC of grid, neg= NHC of grid, and N_{pv} =No. of individually controllable PV panel. * To maintain uniformity in comparison, the four switches, S_2 , S_3 , S_5 , and S_6 in the proposed inverter are considered to be composed of a combination of a power switch in series with a diode. # = data inadequate.

of the dc microgrid with the PV panel and the ac grid requires two separate converters. The presence of this additional converter increases cost while reducing efficiency of the overall system. This issue can be addressed by utilizing a single converter which can negotiate dc loads and/or feed a dc mircrogrid while feeding power from PV panel to the ac grid or can feed power from the ac grid to the dc load when power from the PV panel is not available.

Converters capable of simultaneously negotiating ac and dc loads have been presented in [104]-[106] for stand alone or off-grid applications. However, these converters have the following limitations: (a) they cannot be employed to realize transformerless grid connected scheme as they are prone to problems arising out of the leakage current flow caused by the presence of the PV panels parasitic capacitance [26]-[27], (b) being stand alone systems they are not designed for power flow from ac side to dc loads, (c) the dc load voltage has to be greater than the amplitude of the ac load/gird voltage, and (d) can not operate under zero dc load condition. The NPC inverter presented Section 4.1 is modified appropriately to overcome the aforementioned limitations. The salient features of the proposed scheme are as follows:

1. Capable of supplying PV power to the grid, and to the dc load/dc microgrid simultaneously. Further the same inverter is utilized to feed dc load/dc microgrid from the ac grid when PV power is not sufficient.
2. Buck-boost operation in inverting mode (PV to grid) as well as in rectifying mode (grid to dc load) of conversion
3. Possessing Shoot-through fault tolerant capability
4. Elimination of leakage current problem that exists in a transformerless grid connected inverters for PV application

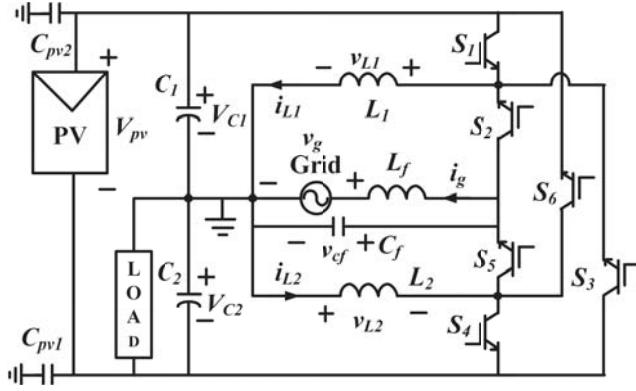


Figure 4.27: The schematic power circuit of the proposed NPC converter servicing single PV panel while negotiating dc loads

5. The scheme comprises of six switches out of which only two switches conduct at a given time.
6. Sensing of grid current is not required.
7. Seamless transition between inverting and rectifying mode of operation.

The operating principle of the converter is presented in the next Subsection. Control structure devised for the scheme to ensure it to operate it in inverting mode as well as in rectifying mode is presented in Subsection 4.4.2. The validation of the scheme is carried out through detailed simulation studies and relevant results are provided in Subsection 4.4.3.

4.4.1 Principle of Operation

The schematic circuit diagram of the proposed scheme is shown in Fig. 4.27. The dc loads/dc microgrid is connected across the capacitor, C_2 . However, instead of C_2 it can be connected across C_1 , and the principle of operation remains the same. The system requires six switches having reverse voltage as well as reverse current blocking capability. The combination of L_f and C_f is employed to filter out the distortions present in the current fed to the grid. Depending on the difference between the available PV power and the dc load power demand, the converter operates either in inverting mode or in rectifying mode of operation. The converter is operated in discontinuous conduction mode (DCM) to achieve seamless transition between these two modes.

A. Inverting mode of operation

When the maximum extractable power from the PV panel, P_{mpp} is more than the dc load power demand, P_{load} , the converter operates in inverting mode. The surplus power from PV, $P_{mpp} - P_{load}$, is fed to the grid. The switching pulses for six switches for operation

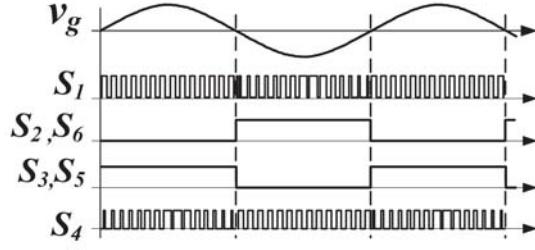


Figure 4.28: Switching pulses during inverting mode of operation

in inverting mode are depicted in Fig. 4.28. The operation of the converter in this mode is explained as follows:

(I) *Operation during positive half cycle:* During this half cycle, S_2 and S_6 are kept off while S_3 and S_5 are kept on as shown in Fig. 4.28. The duty ratio, d_1 for switch S_1 , is controlled to maintain voltage across C_1 at $V_{mpp} - V_{dcref}$ wherein V_{mpp} is the voltage of the PV panel at its maximum power point (MPP) and V_{dcref} is the desired dc load voltage. When S_1 is on, inductor L_1 stores energy from C_1 and when S_1 is off stored energy in L_1 gets transferred to C_2 through S_3 . As the voltage across C_1 is controlled to be constant, the entire energy received by C_1 in a switching cycle gets transferred to C_2 in the same switching cycle. Thus the overall energy extracted from the PV panel in a switching cycle is transferred to capacitor, C_2 ; some part of this energy is directly received from the PV panel while the remaining portion is drawn via C_1 , S_1 , L_1 and S_3 .

The duty ratio, d_4 for switch S_4 , is controlled to maintain the voltage across C_2 to be V_{dcref} . When S_4 is on, the inductor, L_2 stores energy from C_2 and when S_4 is off, the energy stored in L_2 gets transferred to the grid through S_5 . As grid current has to be sinusoidal, the profile of d_4 is maintained sinusoidal. The equivalent circuit diagram of the converter during positive half cycle is depicted in Fig. 4.29(a). As gating pulses for S_3 and S_5 are provided for the entire half cycle they are represented by equivalent diodes, D_3 and D_5 respectively.

(II) *Operation during negative half cycle:* Operation of the converter in this half cycle is similar to the operation in positive half cycle except that the grid is now fed from C_1 instead of C_2 . The profile of duty ratio, d_1 is now maintained sinusoidal to ensure sinusoidal current flow to the grid. The equivalent circuit diagram for this half cycle is shown in Fig. 4.29(b).

The profiles of current flowing through L_1 and L_2 along with their magnified views over an arbitrary switching cycle for operation in DCM are shown in Fig. 4.30.

The voltage impressed across the inductor, L_1 is given by,

$$\begin{aligned}
 v_{L1} &= v_{c1}; \text{ for, } 0 < t < d_1 T_s \\
 &= v_{cf} K - v_{c2}(1 - K); \text{ for, } d_1 T_s < t < (d_1 + d'_1) T_s \\
 &= 0; \text{ for, } (d_1 + d'_1) T_s < t < T_s
 \end{aligned}$$

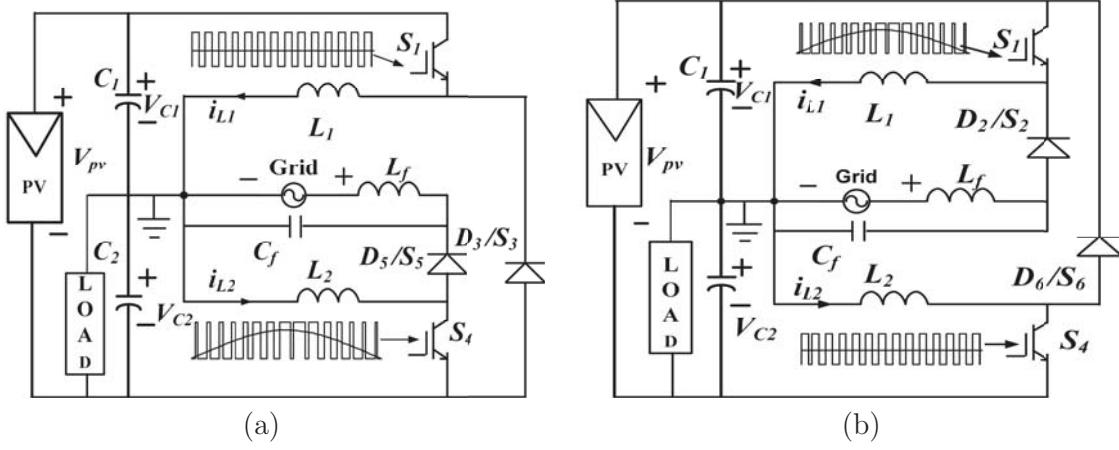


Figure 4.29: Equivalent circuit diagram of the converter while operating in inverting mode during, (a) positive half cycle, and b) negative half cycle

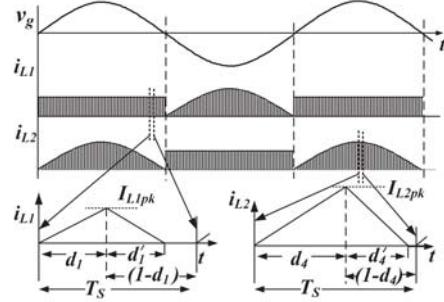


Figure 4.30: Waveform of the inductor currents, i_{L1} and i_{L2} for operation in DCM, and their magnified views for an arbitrary switching cycle in inverting mode of operation

wherein $K = 1$ in the negative half cycle and $K = 0$ in the positive half cycle. The magnitude of the peak current, i_{L1pk} flowing through the inductor, L_1 , is given by,

$$i_{L1pk} = \frac{v_{c1}}{L_1} d_1 T_s \quad (4.31)$$

The voltage impressed across the inductor, L_2 is given by,

$$\begin{aligned} v_{L2} &= v_{c2}; \text{ for, } 0 < t < d_4 T_s \\ &= -v_{cf}(1 - k) - v_{c1}k; \text{ for, } d_4 T_s < t < (d_4 + d'_4) T_s \\ &= 0; \text{ for, } (d_4 + d'_4) T_s < t < T_s \end{aligned}$$

The magnitude of the peak current, i_{L2pk} flowing through the inductor, L_2 , is given by,

$$I_{L2pk} = \frac{v_{c2}}{L_2} d_4 T_s$$

B. Rectifying mode of operation

When $P_{mpp} < P_{load}$, the converter operates in rectifying mode. The dc load is fed with power from PV panel as well as the grid. The switching pulses for the six switches for this mode of operation are depicted in Fig. 4.31.

The operation of the converter for this mode is described as follows:

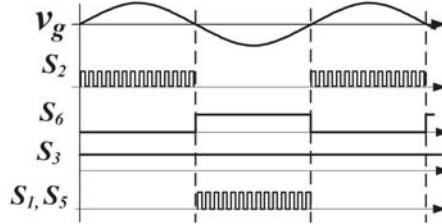


Figure 4.31: Switching pulses during rectifying mode of operation

(I) *Operation during positive half cycle:* During positive half cycle, S_3 is kept on while duty ratio, d_2 of switch S_2 is controlled to extract the required power from the grid. This is achieved by controlling d_2 so as to maintain V_{c2} at V_{dcref} . The other switches are kept off. The equivalent circuit diagram for this half cycle is shown in Fig. 4.32(a).

(II) *Operation during negative half cycle:* During this half cycle the difference between the power demanded by the load to that of supplied by the PV panel is transferred from the grid to C_2 via C_1 . Power from the grid is transferred to C_1 through S_5 , L_2 and S_6 . When S_5 is on, L_2 stores energy from the grid and when S_5 is off energy stored in L_2 is transferred to C_1 through S_6 . The power from C_1 is transferred to C_2 through S_1 , L_1 and S_3 . The equivalent circuit diagram for operation during this half cycle is shown in Fig. 4.32(b).

C. Operation as dc-dc converter

The equivalent circuit formed by S_1 , L_1 , S_3 resembles a buck-boost dc-dc converter having C_1 at its input and C_2 at its output. Power transferred from the PV panel to the dc load is realized by this buck-boost dc-dc converter action of the topology. This dc-dc converter action is inherent in both the inverting as well as rectifying mode. As the dc load is connected across one of the split capacitors of the PV panel (C_2 in the present case), some part of the power supplied by the PV panel gets directly transferred to the load. The remaining part of the power is transferred to the load via the other capacitor (C_1 in the present case). The power transferred from C_1 to C_2 takes place through S_1 , L_1 and S_3 .

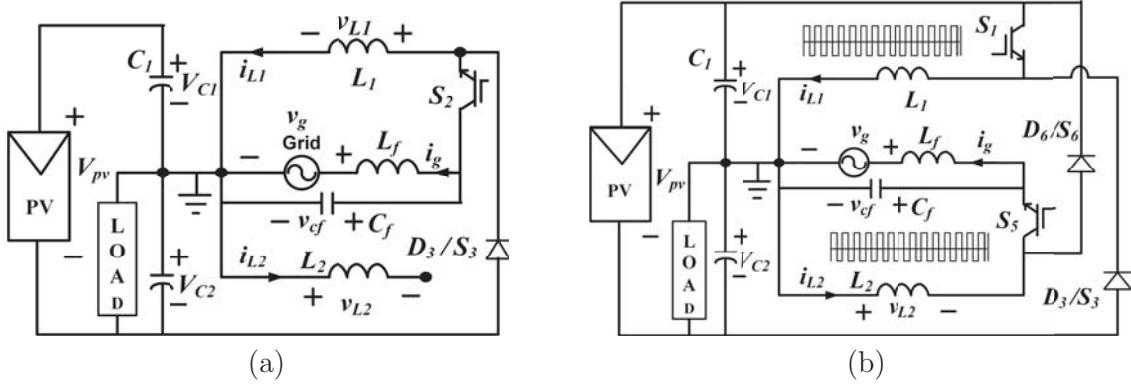


Figure 4.32: Equivalent circuit diagram of the converter while operating in rectifying mode during, (a) positive half cycle, and b) negative half cycle

D. Selection of L_1 and L_2 for DCM

To ensure operation in DCM throughout the ac power cycle, the selection for critical values of L_1 and L_2 must be obtained for a condition when maximum power is required to be processed. Due to unity power factor operation of the inverter, these two inductors process maximum power when grid voltage is at its peak. Further, the maximum power involved with these two inductors is same due to the existing symmetry in the operation of the converter over a power cycle. Following the procedure presented in [47] the critical value for L_1 and L_2 can be derived as,

$$L_{1critical} = L_{2critical} = L_{critical} = \frac{0.25T_s}{QP_{pvm} + (1-Q)P_{lm}} \left[\frac{1}{V_{cmax}} + \frac{1}{V_{gm}} \right]^{-2} \quad (4.32)$$

wherein T_s is the switching time period, P_{pvm} is maximum PV power, P_{lm} is the maximum load demand, V_{cmax} is the maximum voltage of either V_{c1} or V_{c2} , V_{gm} is the maximum grid voltage, and Q is a constant whose value is 1 for inverting mode of operation and zero for rectifying mode respectively.

4.4.2 Control Structure

A. Inverting mode

The control strategy employed for inverting mode of operation is shown in Fig. 4.33. A conventional MPPT algorithm is employed to generate the reference voltage command (v_{mpp}) for the PV panel to operate it at its MPP. In order to control the actual PV voltage, v_{pv} at v_{mpp} , the voltage across C_1 is controlled to be v_{c1ref} where $v_{c1ref} = v_{mpp} - v_{c2}$. The error between v_{c1ref} and v_{c1} is then processed through PI-1 and subsequently manipulated to generate the desired duty ratio, d_1 for switch S_1 . The duty ratio, d_1 is directly derived from the output of PI-1 during the positive half cycle as power is transferred from C_1 to C_2 through S_1 , L_1 and S_3 . During the negative half cycle power is transferred to the grid from C_1 through S_1 , L_1 and S_2 . As the grid current has to be sinusoidal and in phase

with the grid voltage to achieve unity power factor operation, the profile of d_1 during the negative half cycle is made sinusoidal by multiplying the output of PI-1 with the signal, $|p|$. The signal, $|p|$ is the rectified version of the unit amplitude sinusoidal signal p which is in synchronism with the grid voltage. The signal p is generated through a phase locked loop (PLL) algorithm [96]. The output of PI-1 is also multiplied with a factor ‘1.57’ (has been discussed in Section 4.4 of this Chapter) to ensure that the average magnitude of d_1 remains the same as that of the output of PI-1 after multiplication with $|p|$.

The dc load voltage, v_{c2} is controlled at a desired reference magnitude, V_{dcref} . The error between V_{dcref} and v_{c2} is processed through PI-2 to generate desired duty ratio, d_4 for the switch, S_4 . The duty ratio, d_4 is directly derived from the output of PI-2 during negative half cycle as power is transferred to C_1 from C_2 through S_4 , L_2 and S_6 . During the positive half cycle, power is transferred to the grid from C_2 through S_4 , L_2 and S_5 . As the grid current has to be sinusoidal and in phase with the grid voltage to achieve unity power factor operation, the profile of d_4 has to be sinusoidal. Further, d_4 must be generated in such a way so that the dc current injection into the grid is restricted within permissible limit. In the present scheme, the voltages across C_1 and C_2 will be different which may lead to dc current injection into the grid. As the inverter is operated in DCM, dc current injection to the grid can be avoided if profile of the discontinuous current peaks through L_1 in the negative half cycle is kept equal to that of the profile of the discontinuous current peaks through L_2 in the positive half cycle. The peak current, $i_{L1pkneg}$ flowing through the inductor L_1 in a switching cycle in the negative half of the grid voltage, and the peak current, $i_{L2pkpos}$ flowing through the inductor, L_2 in the positive half cycle of the grid voltage can be expressed as,

$$i_{L1pkneg} = \frac{v_{c1}}{L_1} M_1 |\sin \omega t| T_s, \quad (4.33)$$

$$i_{L2pkpos} = \frac{v_{c2}}{L_2} M_2 |\sin \omega t| T_s \quad (4.34)$$

wherein M_1 is the amplitude of the duty ratio of the switch, S_1 in the negative half cycle of the grid voltage and M_2 is the amplitude of the duty ratio of the switch, S_4 in the positive half cycle of the grid voltage. In order to prevent dc current injection into the grid the desirable relationship between M_1 and M_2 , can be obtained by equating (4.33) and (4.34) which is as follows,

$$M_2 = \frac{V_{c1}}{V_{c2}} M_1 = G_2 M_1, \quad [\text{as } L_1 = L_2] \quad (4.35)$$

wherein, $G_2 = \frac{V_{c1}}{V_{c2}}$.

B. Rectifying mode

The schematic control block diagram employed for the rectifying mode of operation is shown in Fig. 4.34. The reference voltage commands for capacitors, C_1 and C_2 , are kept same as those of inverting mode of operation. The voltage across C_1 is controlled to be v_{c1ref} wherein $v_{c1ref} = v_{mpp} - v_{c2}$, by generating suitable duty ratio for S_1 with the

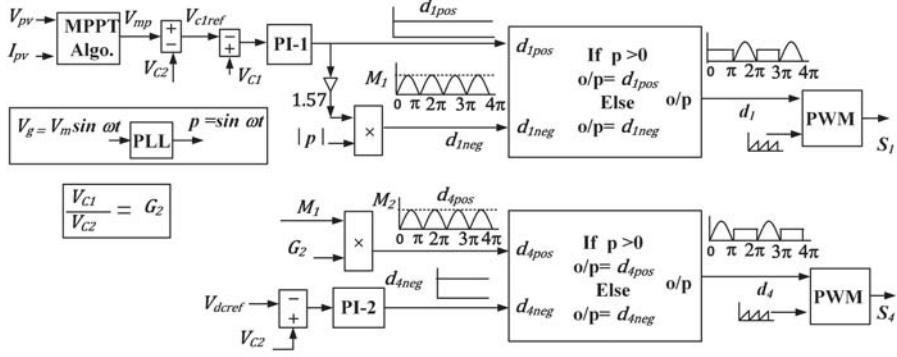


Figure 4.33: Control strategy for inverting mode of operation

help of PI-1 as shown in Fig. 4.34. To maintain v_{c2} at V_{dcref} and to ensure symmetrical grid current flow over a grid cycle, one line-cycle regulation approach (OLCRA) [107] is employed for rectifying mode of operation. The error between V_{dcref} and v_{c2} is processed through PI-2. The output of PI-2 is then fed to a sample and hold (S&H) circuit. This S&H circuit samples the output of PI-2 at the positive going zero crossing instants of the grid voltage and holds this sampled value for entire duration of the grid cycle. Thus the output of the S&H circuit remains the same for entire duration of a grid cycle. During positive half cycle of the grid voltage, the output of the S&H circuit is taken as the duty ratio for switch S_2 . When S_2 is on, the grid voltage is applied across L_1 and it stores energy from the grid. When S_2 is turned off, the energy stored in L_1 is transferred to C_2 via S_3 (S_3 is kept on for the entire duration of the positive half cycle). Since duty ratio for switch S_2 is kept constant for the entire positive half cycle and sinusoidal grid voltage is applied across L_1 when S_2 is on, the grid current is rendered to be sinusoidal and further it is synchronised with the grid voltage.

During the negative half cycle, S_2 is kept off and the duty ratio of the switch, S_5 is generated from the output of the S&H circuit. When S_5 is on the grid voltage is applied across L_2 and it stores energy from the grid. When S_5 is turned off, the energy stored in L_2 is transferred to C_1 via S_6 . Being taken from the output of the same S&H circuit, the duty ratio of S_5 in the negative half cycle is same as that of the switch, S_2 in positive half cycle. This ensures symmetrical grid current flow having zero dc current offset.

C. Mode transition

(I) Transition from inverting to rectifying mode: While operating in inverting mode if P_{pv} becomes less than P_{load} , the dc load voltage, v_{c2} starts falling as grid cannot supply power to the dc load during inverting mode. Once v_{c2} hits a prescribed lower limit, the mode of operation is shifted to rectifying mode wherein both the PV panel and the grid supplies power to the dc load and v_{c2} is restored back to its reference value, V_{dcref} .

(II) Transition from rectifying to inverting mode: While operating in rectifying mode if P_{pv} becomes greater than P_{load} , the dc load voltage, v_{c2} starts increasing as grid cannot consume power during rectifying mode. Once v_{c2} hits a prescribed upper limit, the mode

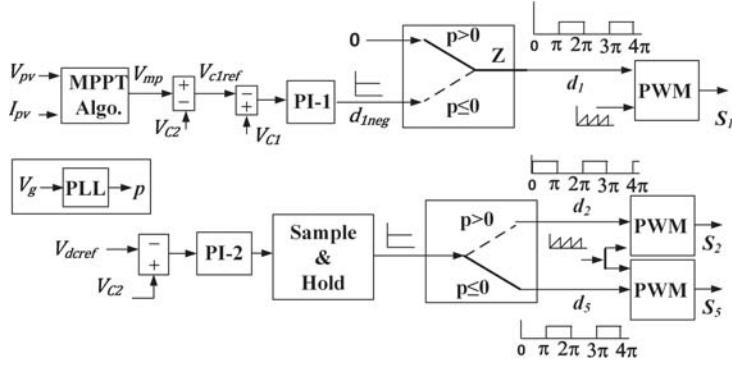


Figure 4.34: Control strategy for rectifying mode of operation

of operation is shifted to inverting mode wherein surplus power from the PV panel is fed to grid and the v_{c2} is restored back to its reference value, V_{deref} .

4.4.3 Simulated Performance

In order to ascertain efficacy of the proposed scheme detailed simulation studies are carried out on Matlab/Simulink platform. Various parameters considered in the simulated model of the scheme are provided in Table 4.9.

Case a. Inverting mode of operation:

The simulated performance of the scheme while operating in inverting mode is shown in Fig. 4.35. The dc load demand is set as follows: 100 W from 0 - 2.5 s, 200 W from 2.5 - 3.5 s, and 100 W from 3.5 s onwards. The temperature of the PV module is kept fixed at 25°C . The insolation level of the PV panel is set as: 800 W/m^2 (corresponding $P_{mpp}=485 \text{ W}$) till 1.5 s and 1000 W/m^2 (corresponding $P_{mpp}=595 \text{ W}$) from 1.5 s onwards.

The variation in PV power and PV voltage with the aforementioned changes in insolation level are shown in Fig 4.35(a) and 4.35(b) respectively. The dc load voltage and the voltage across C_1 are shown in Fig 4.35(c). From this figure it can be inferred that the load voltage is maintained at 120 V and the voltage across C_1 is manipulated to operate the PV panel at its MPP. The profile of the grid current is shown in Fig. 4.35(d) wherein

Table 4.9: Parameters/elements considered for the simulation study

Parameter	Value
Grid voltage, V_g	230 V, 50 Hz
PV voltage, V_{pv}	240-280 V
DC load voltage, V_{deref}	120 V
$L_1 = L_2$	0.1 mH
$C_1 = C_2$	$3300 \mu\text{F}$
Grid side filter, C_f & L_f	$2 \mu\text{F}$ & 4 mH
Switching frequency, F_s	15 kHz
MPPT algorithm	Incremental conductance

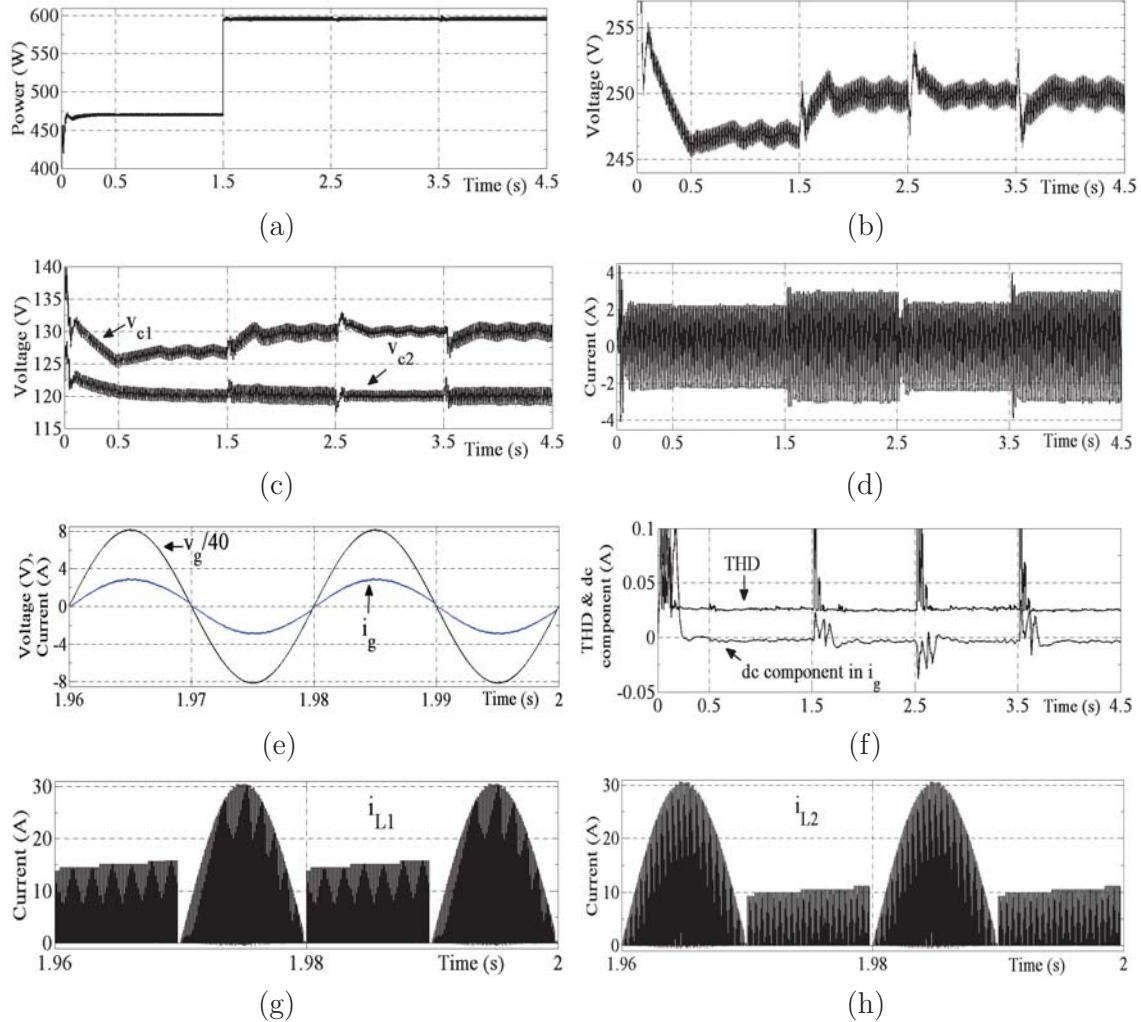


Figure 4.35: Simulated performance in inverting mode of operation: a) p_{pv} , b) v_{pv} , c) V_{c1} and V_{c2} , d) i_g , e) magnified view of i_g and v_g in steady state, f) THD and dc component in i_g , g) i_{L1} in steady state, and h) i_{L2} in steady state.

it can be observed that the magnitude of the grid current is adjusted in accordance to the variation in insolation level and the load demand. Magnified view of the grid current along with the grid voltage at a given steady state condition is shown in Fig. 4.35(e). From this figure it can be noted that the grid current is fairly sinusoidal and is in phase with the grid voltage thereby implying that power is being fed to the grid at unity power factor. The levels of total harmonic distortion (THD) and the dc component present in the grid current are shown in Fig. 4.35(f). From this figure it is observed that the THD is around 2.8% whereas dc component is almost zero. Magnified views of current flowing through the inductors, L_1 and L_2 at a given steady state condition are shown in Fig. 4.35(g) and 4.35(f) respectively to show that the converter is operated in DCM.

Case b. Rectifying mode of operation:

The simulated performance of the scheme while operating in rectifying mode is shown in Fig. 4.36. The dc load demand is set as follows: 500 W from 0 - 1 s, 600 W from 1 - 3 s, and 500 W from 3 s onwards. The temperature of the PV module is kept fixed at $25^{\circ}C$. The insolation level of the PV panel is set as follows: 300 W/m^2 (corresponding $P_{mpp}=165 \text{ W}$) till 2 s and 400 W/m^2 (corresponding $P_{mpp}=225 \text{ W}$) from 2 s onwards. The variation in PV power and PV voltage with the aforementioned changes in insolation level is shown in Fig 4.36(a) and 4.36(b) respectively. The dc load voltage and the voltage across C_1 are shown in Fig 4.36(c). From this figure it can be inferred that the load voltage is maintained at 120 V and the voltage across C_1 is manipulated to operate the PV panel at its MPP. The profile of grid current is shown in Fig. 4.36(d) wherein it can be observed that the magnitude of the grid current is adjusted in accordance to the variation in insolation level and the load demand. Magnified view of the grid current along with the grid voltage at a given steady state condition is shown in Fig. 4.36(e). From this figure it can be noted that the grid current is fairly sinusoidal and is 180° out of phase with the grid voltage thereby implying that power is being absorbed from the grid at unity power factor. The level of THD and the dc component present in grid current is shown in Fig. 4.36(f). From this figure it can be noted that the THD is around 3% whereas dc component is almost zero.

Case c. Mode transition:

The simulated performance of the scheme during mode transition between inverting and rectifying mode is shown in Fig. 4.37. Here the insolation level and the temperature of the PV panel are kept fixed at 700 W/m^2 and $35^{\circ}C$ respectively (corresponding $P_{mpp}=400 \text{ W}$). The PV power and PV voltage is shown in Fig. 4.37(a). Till 1.5 s the load demand is set at 80 W which is less than the P_{pv} and hence the system operates in inverting mode. At 1.5 s, the load demand is increased to 580 W which is more than the P_{pv} , and hence, the load voltage starts decreasing as shown in Fig 4.37(b). Once the load voltage reaches 108 V (prescribed lower limit), the operation is shifted to rectifying mode. Once the system enters into the rectifying mode, the grid current reverses, and the load voltage is brought back to 120 V as shown in Fig 4.37(b). The magnified view of i_g and v_g during mode transition from inverting mode to rectifying mode is shown in Fig. 4.37(d). From this figure it can be observed that the polarity of the grid current reverses when mode of operation gets shifted from inverting to rectifying and that the mode transition is seamless. At 3 s, while the system is operating in the rectifying mode, the load demand is reduced to 80 W which is less than P_{pv} . As a consequence, the load voltage starts increasing as shown in Fig 4.37(b). Once this load voltage reaches 132 V (prescribed upper limit), the mode of operation is shifted back to inverting mode of operation. The magnified view of i_g and v_g during mode transition from rectifying to inverting mode is shown in Fig. 4.37(e). From this figure it can be observed that the polarity of the grid current reverses when mode of operation gets shifted from rectifying to inverting and that

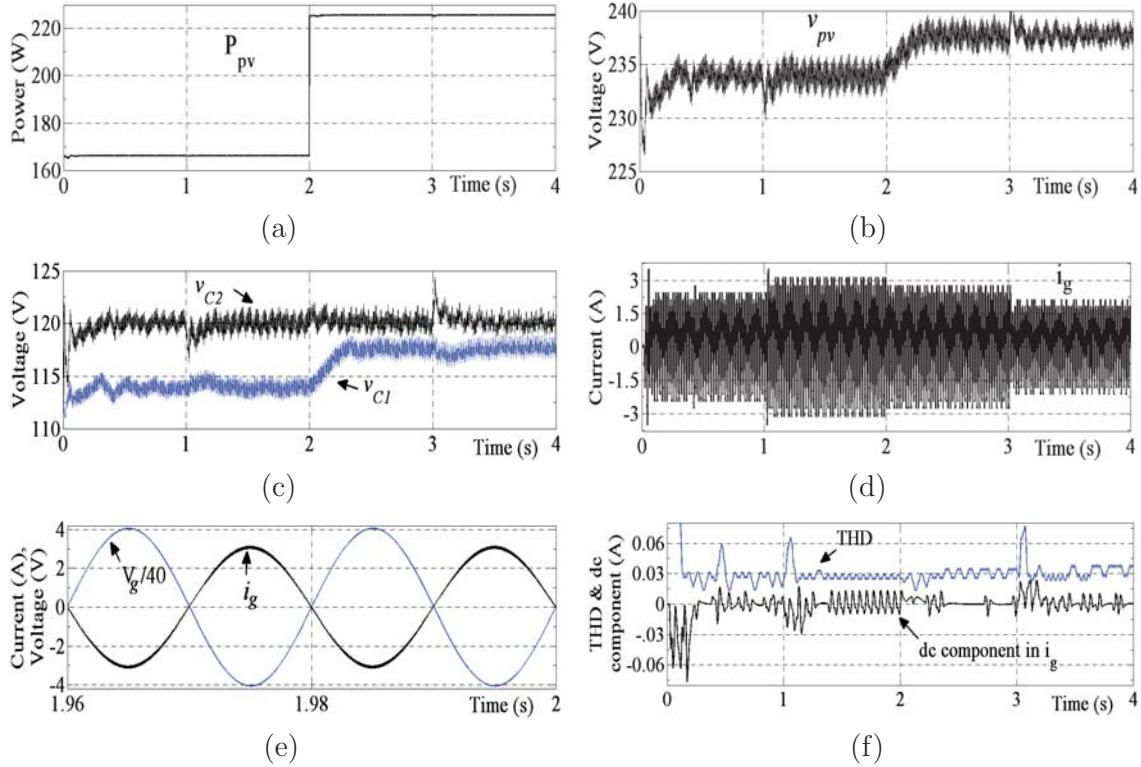


Figure 4.36: Simulated performance in rectifying mode of operation: a) p_{pv} , b) v_{pv} , c) V_{c1} and V_{c2} , d) i_g , e) THD and dc component in i_g , and (f) magnified view of i_g and v_g in steady state.

the mode transition is seamless.

4.5 Conclusion

A multi-purpose transformerless grid connected inverter scheme is proposed in this chapter. This inverter is based on neutral point clamped inverter structure and has the voltage buck-boost capability. It can be utilized to extract maximum power from a single as well as two separate PV panels. While extracting maximum power from a single PV panel the same converter can be utilized to negotiate dc loads simultaneously. The aforementioned dc loads can be supplied from the PV panel and/or the grid. Thus the proposed converter can serve as dc-ac inverter (PV to grid), dc-dc converter (PV to dc load), and ac-dc converter (grid to dc load). The other advantages of the proposed scheme includes, (a) elimination of concerns pertaining to the leakage current issue in grid connected solar PV systems, (b) elimination of grid current sensor requirement, and (c) elimination of shoot-through problem. The control structures devised for the aforementioned applications of the proposed scheme is presented. The effectiveness of the proposed scheme for all of the aforementioned applications have been ascertained through detailed simulation studies. A laboratory prototype for the scheme is developed and experimental validation is carried out for the scheme when it is employed to extract

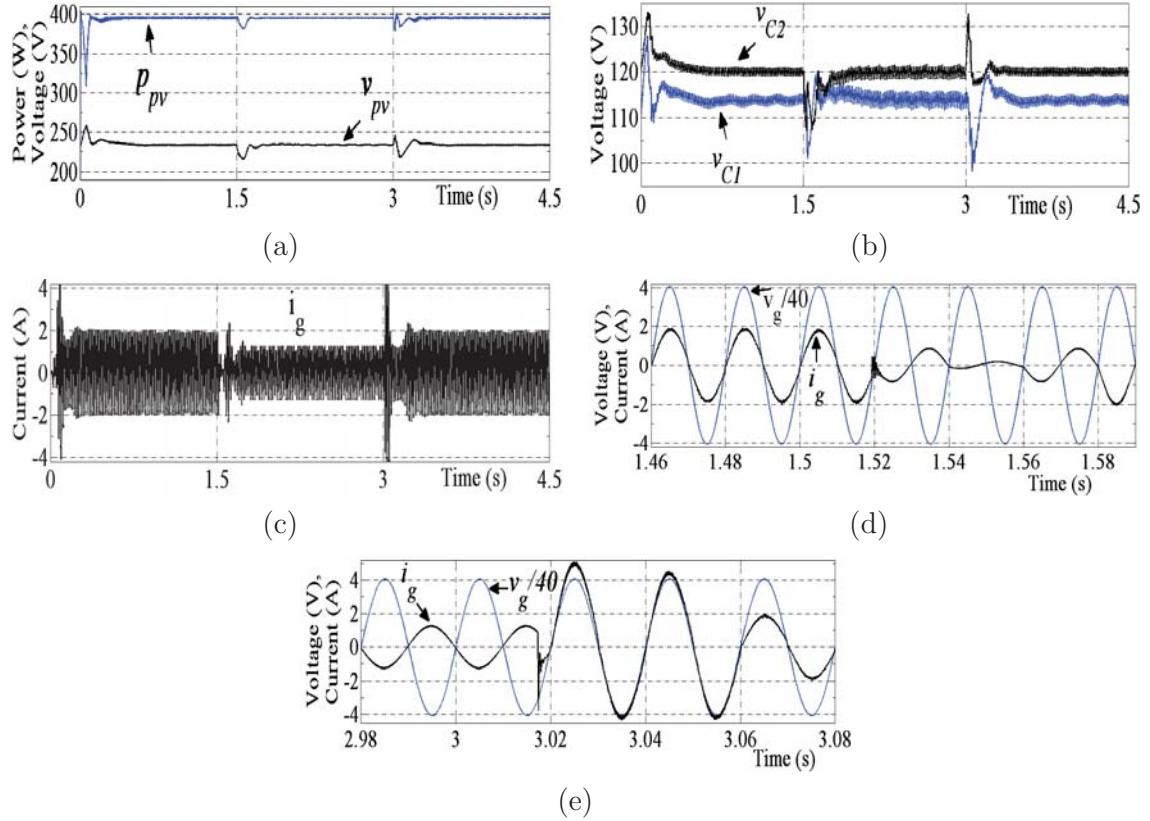


Figure 4.37: Simulated performance during mode transition: a) p_{pv} and v_{pv} , b) V_{c1} and V_{c2} , c) i_g , d) magnified view of i_g and v_g during mode transition from inverting to rectifying mode, and e) magnified view of i_g and v_g during mode transition from rectifying to inverting mode.

maximum power from single as well as two separate PV panels.

Chapter 5

A Simple Distributed Maximum Power Point Tracking Scheme

5.1 Introduction

The solar photovoltaic based systems discussed in the previous three Chapters of the thesis deal with low power level. As a result the voltage level of the PV array for these schemes remain to be low. As the power level of the systems increase, the PV voltage level has also to be increased by connecting several PV modules in series to form a PV string in order to reduce losses in the system. Solar photovoltaic (PV) strings formed by series combination of several PV modules suffer from considerable reduction in power yield when subjected to mismatched operating conditions. In order to address this issue several schemes have been reported in the literature. Out of these the group of schemes based on compensating power-dedicated dc-dc converter based distributed maximum power point tracking (CPDC-DMPPT) seem to be the most promising ones. However, the existing CPDC-DMPPT schemes have one or more of the following drawbacks: (a) requirement of insulation level and temperature sensing [66]-[67], (b) requirement of module level power sensing thereby requiring more number of sensors [68] - [70], (c) requirement of communication link between local dc-dc converters [71], (d) operation of PV modules at their approximate (and not exact) MPP [56]-[65], and (e) requirement of executing N numbers of MPPT algorithm simultaneously thereby increasing the burden on the processor [71] (N is the number of series connected modules). In order to overcome the aforementioned drawbacks a scheme is proposed in [56]. It employs multistage chopper circuit to realize local dc-dc converters and requires a single voltage and a single current sensor. In this case, the duty ratios of $(N - 1)$ local converters are kept fixed, and the duty ratio of the remaining local converter is varied to maximize the string output power. After a certain interval, duty ratio of the next local converter is varied to maximize the power yield whereas duty ratios of remaining $(N - 1)$ converter are kept fixed at their previous updated values. This process is repeated cyclically. However, this scheme has the following constraints:

The following paper is based on the content of this Chapter:

1. D. Debnath, P. De, and K. Chatterjee, “A Simple Scheme to Extract Maximum Power from Series Connected PV Modules Experiencing Mismatched Operating Conditions,” accepted for publication in IET Power Electronics

1. With the increment in number of series connected modules the ON time of the switches of the local converters for a given switching switching frequency increases considerably which makes the scheme impractical for strings with higher number of series connected modules
2. Model of the scheme has been derived ignoring the parasitic elements of the converter which might be crucial for practical implementation as the local converters are operated in open loop fashion
3. It is not tolerant to shoot through fault and the effect of dead band on the performance of the scheme has not been investigated
4. This strategy cannot be applied for schemes which employ isolated local converters. The reason for this is as follows: the input voltage of the local converters in isolated converter based schemes is the PV string voltage itself [68]. This string voltage gets changed with perturbation in duty ratio of any local converter. As the duty ratio of remaining ($N - 1$) local converters are kept the same at a given time, the voltage level at their output, i.e, voltage across each PV module (and hence their power yield) also changes with changes in the input/string voltage. Under this scenario, the variation in the string output power is not solely dependant on the variation of the duty ratio of the N th converter. This violates the basic principle of operation of the scheme.

In order to address these issues, this chapter proposes a simple method to extract maximum power from PV string having number of series connected PV modules. This scheme is an improved version of the scheme presented in [56] and seeks to eliminate drawbacks associated with the same. The salient features of the proposed scheme are as follows:

1. Reduced burden on the processor as only one conventional MPPT algorithm needs to be executed at a given time
2. Communication link among the local dc-dc converters is not required
3. Requirement of reduced number of current sensors as the scheme does not require information of power derived by each of the modules. It requires only $(N+1)$ voltage sensors and only one current sensor for its operation.
4. This scheme, simultaneously, has the effectiveness of the true/exact MPP schemes and the simplicity of implementation similar to that of the voltage equalization based schemes

The operating principle of the scheme is presented in the following Section. The implementation of the proposed control algorithm is explained in Section 5.3. The simulated performance of the scheme is presented in Section 5.4 to verify its efficacy. Experimental validation of the scheme is carried out by utilizing a scaled down laboratory prototype and relevant results are presented in Section 5.5.

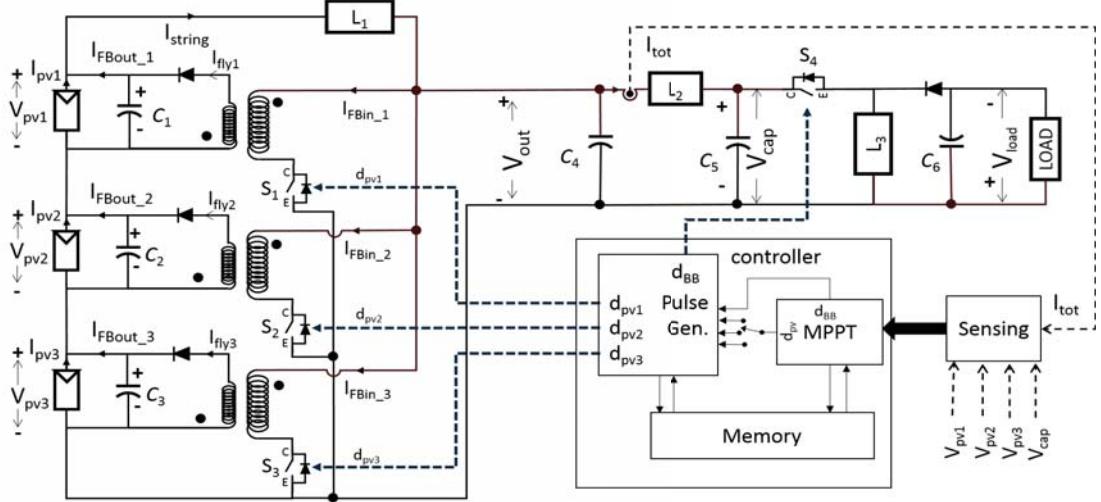


Figure 5.1: Schematic circuit diagram of flyback converter based DMPPT scheme adopted for demonstration of the proposed DMPPT strategy [57], [68]

5.2 Principle of Operation

The power circuit configuration of Fig. 5.1 which is reported in [57], [68], is utilized to demonstrate the proposed DMPPT strategy. It is to be noted that the proposed DMPPT strategy can be applied for any solar PV based system wherein voltage of each of the PV module is controlled by their individual local dc to dc converters. Here the system considered is having three solar modules connected in series however, the proposed DMPPT algorithm can be extended to N number of such serially connected modules. The power circuit configuration of the scheme is shown in Fig. 5.1 and is having separate flyback converters to operate each of the PV modules at their respective MPPs. The string current, i_{string} is equal to the magnitude of the current of that module which sources the maximum current among all the modules present in the string. The difference between the string current and the current generated by individual PV module is termed as the balance current. Each of the flyback converters has to supply the required balance current to ensure that the corresponding PV module operates at its MPP. All the flyback converters are connected in parallel to the output terminals of the string. The terminals of the string is subsequently connected to the input terminals of a buck-boost converter which serves as the central converter to feed the net power extracted from the string to the effective load connected across the capacitor, C_6 . In this particular case the load is considered to be a stand alone dc load however, it can be modified to feed a stand alone ac load or an ac grid, and for this the buck-boost dc to dc converter is to be replaced by a suitable dc to ac inverter.

Under steady state conditions, the output voltage of the i th flyback converter operating in continuous conduction mode is expressed as:

$$V_{pv_i} = nV_{out} \frac{d_{pv_i}}{(1 - d_{pv_i})}$$

wherein i is an integer which ranges from 0 to N , V_{pv_i} is the voltage across the i th PV

module, n is the turns ratio of the transformer of the flyback converter from output (PV side) to input side, and d_{pv_i} is the duty ratio of the switch of the i th flyback converter. Thus V_{pv_i} can be controlled by manipulating d_{pv_i} .

Considering a situation wherein the current generation capability of module-1, I_{pv1} is more than the other two modules, the string current is,

$$I_{string} = I_{pv1} \quad (5.1)$$

Therefore, the balance current required from the flyback converter-1 is,

$$I_{FBout_1} = I_{string} - I_{pv1} = 0 \quad (5.2)$$

Neglecting the voltage drops across L_1 and L_2 (which are used to filter the current ripples), the voltage at the input terminal of buck-boost converter is given as,

$$V_{cap} = V_{out} = V_{pv1} + V_{pv2} + V_{pv3} \quad (5.3)$$

The expressions for the power output from the three flyback converters are,

$$P_{outFB_1} = V_{pv1} \times I_{FBout_1} = 0 \quad (5.4)$$

$$P_{outFB_2} = V_{pv2} \times I_{FBout_2} = V_{pv2}(I_{string} - I_{pv2}) \quad (5.5)$$

$$P_{outFB_3} = V_{pv3} \times I_{FBout_3} = V_{pv3}(I_{string} - I_{pv3}) \quad (5.6)$$

Assuming the flyback converters to be lossless,

$$P_{outFB_i} = P_{inFB_i} = I_{inFB_i}V_{out} \quad (5.7)$$

wherein P_{inFB_i} is the input power of the i th flyback converter, and I_{inFB_i} is the input current to the i th flyback converter. From (5.4)-(5.7), the input currents to the three flyback converters are,

$$I_{FBin_1} = 0 \quad (5.8)$$

$$I_{FBin_2} = V_{pv2} \frac{(I_{string} - I_{pv2})}{V_{out}} \quad (5.9)$$

$$I_{FBin_3} = V_{pv3} \frac{(I_{string} - I_{pv3})}{V_{out}} \quad (5.10)$$

From Fig. 5.1, considering the average current flowing through the capacitor, C_4 to be zero over a switching cycle,

$$\begin{aligned} I_{tot} &= I_{string} - (I_{FBin_1} + I_{FBin_2} + I_{FBin_3}) \\ &= I_{string} - [0 + V_{pv2} \frac{(I_{string} - I_{pv2})}{V_{out}} + V_{pv3} \frac{(I_{string} - I_{pv3})}{V_{out}}], \text{ using (5.8)-(5.10)} \\ &= I_{string} \left(1 - \frac{V_{pv2}}{V_{out}} - \frac{V_{pv3}}{V_{out}}\right) + V_{pv2} \frac{I_{pv2}}{V_{out}} + V_{pv3} \frac{I_{pv3}}{V_{out}} \end{aligned} \quad (5.11)$$

Using (5.1), (5.3), and (5.11),

$$\begin{aligned} I_{tot} &= I_{string} \frac{V_{pv1}}{V_{out}} + I_{pv2} \frac{V_{pv2}}{V_{out}} + I_{pv3} \frac{V_{pv3}}{V_{out}} \\ \text{or, } I_{tot}V_{out} &= V_{pv1}I_{pv1} + V_{pv2}I_{pv2} + V_{pv3}I_{pv3} \end{aligned}$$

wherein ' $I_{tot}V_{out} = P_{tot}$ ' is the power input to the buck-boost dc-dc converter. From the above equation it can be noted that the net output power from all the PV modules is fed to the input of buck-boost converter. As there is no constraint on the voltages and currents of the PV modules, they can operate at their respective MPP points. Thus maximum power of each of the modules is extracted from the system.

It can be noted that if a PV module is operated at a given voltage (any voltage between 0 and its open circuit voltage, V_{oc}) its output power remains constant for this particular voltage for a given operating condition. Therefore, if each of the ($N - 1$) modules is operated at a voltage fixed by their individual local converters, their total output power remains constant for a given operating condition. Hence the overall output power of the string which is given by, $P_{tot} = V_{out}I_{tot}$, is modulated by the variation of power generated in the i^{th} module of the string whose voltage is being modulated at the current instant. Therefore the reference voltage commands of ($N - 1$) modules are kept fixed at their respective previous updated values. The voltage reference for the i^{th} module is adjusted such that P_{tot} and hence the output power of the i^{th} module is ascertained to be maximum. This process is repeated for all the modules in a successive manner. The control algorithms to realize the aforementioned process is presented in the following Section.

5.3 Control Structure

The control algorithm can be implemented in two ways based on the method employed for adjustment of voltage reference for individual modules. The first approach is based on periodic search algorithm wherein voltage reference for each module is adjusted for a fixed duration of time. This fixed time interval, T_s , is the time period of the periodic search algorithm. As three modules are being considered, the reference for two modules is kept fixed for T_s and the reference voltage command for the remaining module is adjusted to get maximum total output power, P_{tot} . The flowchart diagram of this approach is shown in Fig. 5.2. At the beginning, the voltage references, v_{m1} , v_{m2} , and v_{m3} for the three modules respectively are initialized at a value, X . Although ' X ' can be any value lying between 0 to V_{oc} , however it is preferable to keep it close to the MPP of the module in question at standard test condition (STC)(as provided in the datasheet for that particular module). The integer variables j and k are initialized to zero. The variable Vr is the output provided by the MPPT algorithm. In the present case MPP routine based on P & O algorithm is used however any MPP routine can be utilized. The variable, Vr is also initialized to the value X . The MPPT algorithm will update this Vr continuously utilizing the information of V_{out} and I_{tot} in order to maximize the string output power. Thus Vr is the reference voltage for every module being serviced for $ITER_MAX$ number of iterations wherein $ITER_MAX$ corresponds to time period of the periodic search algorithm, T_s . The variable k is incremented by one at the end of the time interval corresponding to $ITER_MAX$ iterations and is reset when it reaches its maximum value N ($N=3$ in the present case). For the very first set of iteration of j , i.e. for j lying between 0 and $ITER_MAX$, k is zero and the reference for module 1, v_{m1} is

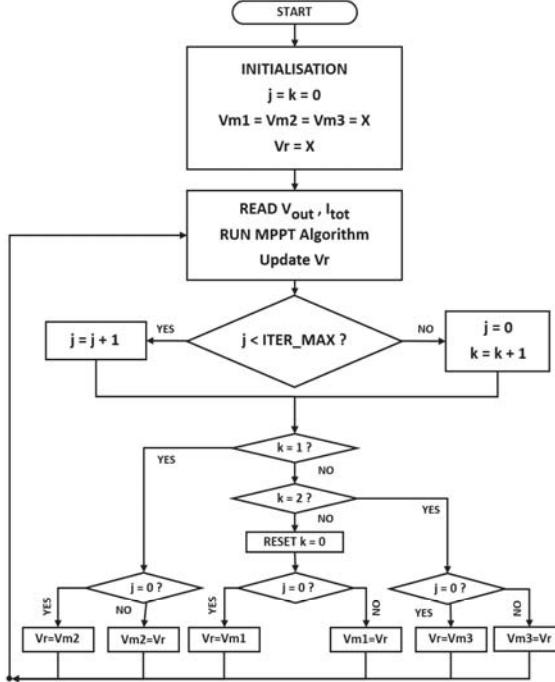


Figure 5.2: Flowchart showing control structure to generate reference voltage commands for three modules being serviced at fixed interval of time

updated with V_r . The references, v_{m2} and v_{m3} , are kept at their initialized values. Once j reaches its set limit, i.e. $ITER_MAX$, j is reset to zero and k is increased to 1 which marks the start of the second time interval where module-2 is serviced. The previous value of v_{m2} is now loaded to V_r (for condition $k=1$ and $j=0$ as shown in Fig. 5.2). This step is necessary to start updating v_{m2} from its previous value. The value of v_{m2} is updated till j again reaches its set value, $ITER_MAX$. During this interval v_{m1} and v_{m3} are kept fixed at their previous updated values. Once j again reaches $ITER_MAX$, j is reset to zero and k is increased to 2 which marks the start of the third time interval where module-3 is serviced. Similar to the previous time interval, at the beginning of this interval, previous value of v_{m3} is made to be the initial value for V_r and v_{m3} is updated till j reaches $ITER_MAX$. After j reaches $ITER_MAX$, fourth interval starts and k is reset to 0. During this time interval, v_{m1} starts getting updated while v_{m2} and v_{m3} are kept at their previous updated values and this process is repeated.

In the second approach the reference voltage command for each module is adjusted till it reaches its MPP. Once MPP is reached for a given module its reference voltage command is frozen at that value and the reference voltage command for the next module is updated. This process continues in a cyclic order. This is realized by slightly modifying the way the variable j is updated as compared to the previous approach. The variable, j is now binary in nature which shows whether a module, being serviced, is in MPP or not. When that module is not in MPP its reference continues to get adjusted. On the other hand if MPP of that module is attained the present voltage reference is frozen and consequently the next module is being serviced. The implementation of this approach is shown in Fig.5.3.

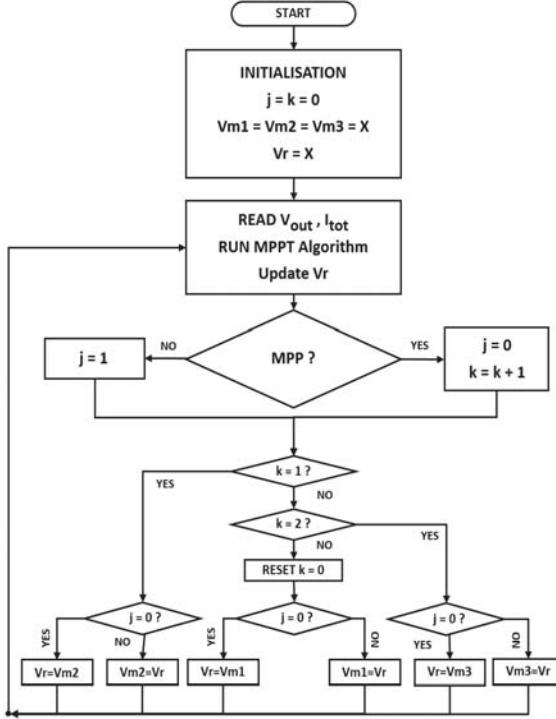


Figure 5.3: Flowchart showing control structure to generate reference voltage commands for three modules with each module being serviced till it attains its MPP

From the above discussion it can be inferred that implementation of the first approach is easier compared to that of the second approach as a decision making process is required in the second approach to determine whether the MPP has attained or not. However, in case of the first approach, the waiting period (the duration of time elapsed between two successive servicing) of a module becomes considerable if the number of modules present in the string is large. Thus the first approach is suitable for schemes having less number of modules. In case of the second approach the time required to reach MPP for each of the modules for the first time may be considerable but then once MPP for the modules are attained or in other words steady state is reached, time required to service a module becomes less. Hence a change in operating condition in a module can be addressed quickly if the second approach is followed. The second approach is suitable for schemes having large number of serially connected modules.

The sensed PV module voltages are compared with their respective reference voltage commands and the error is processed through proportional integral (PI) controller which generates suitable duty ratio for the respective flyback converter.

The reference voltage command for the string is sum of the reference voltage commands for each of the serially connected modules and is given by,

$$V_{outref} = v_{m1} + v_{m2} + v_{m3}$$

The sensed string voltage is made to follow its reference voltage command, V_{outref} by

employing a PI controller which generates suitable duty ratio for the controllable switch of the central converter. Thus, no separate MPPT algorithm is required for the central converter.

5.4 Simulated Performance

In order to ascertain the viability of the proposed scheme the system shown in Fig. 5.1 is simulated in Matlab/Simulink platform. Three modules having similar electrical characteristics to that of ‘BP4175T’ module from BP solar is considered for the simulation study [93]. The electrical characteristics of such a module under standard test condition (STC) is given in Table 5.1. The control strategy as shown in Fig. 5.2 is implemented to generate reference voltage command for the three modules. The flyback converters are designed to operate in discontinuous conduction mode (DCM). The central converter is realized by a buck-boost dc-dc converter. Conventional perturb and observe (*P&O*) algorithm is employed to track MPP of the string. Different parameters considered for simulating the system are provided in Table 5.2.

Table 5.1: Electrical characteristics of BP4175T module at STC

Parameter	value at STC
P_{mpp}	175 W
Voltage at P_{mpp} , V_{mpp}	35.4 V
Current at P_{mpp} , I_{mpp}	4.94 A
Open circuit voltage, V_{oc}	43.6 V
Short circuit current, I_{sc}	5.45 A

Table 5.2: Parameters considered for the simulation study

Parameter	value
L_1 and L_2	0.1 mH
C_{pv}	100 μ F
C_{out}	500 μ F
Magnetizing inductance (flyback)	0.14 mH
Input voltage range of flyback (PV string voltage)	80-126 V
Output voltage range of flyback (voltage across each PV module)	25-40 V
Max. duty ratio (flyback)	0.45
Switching frequency	20 kHz

Simulated performance of the scheme has been obtained for both the approaches shown in Fig. 5.2 and Fig.5.3. Insolation levels for three modules were set at different values while maintaining a constant temperature of 25^0 C for each of the module for both the approaches. Relevant electrical parameters of these modules along with their set insolation levels are provided in Table 5.3.

Table 5.3: Relevant details of three PV modules considered for simulation study

Module	S (kW/m^2)	V_{mpp} (V)	I_{mpp} (A)	P_{mpp} (W)
Mod 1	0.8	34.8	3.97	138
Mod 2	0.6	34	3.03	103
Mod 3	1	35.4	4.94	175
$\sum = 104.2$			$\sum = 416$	

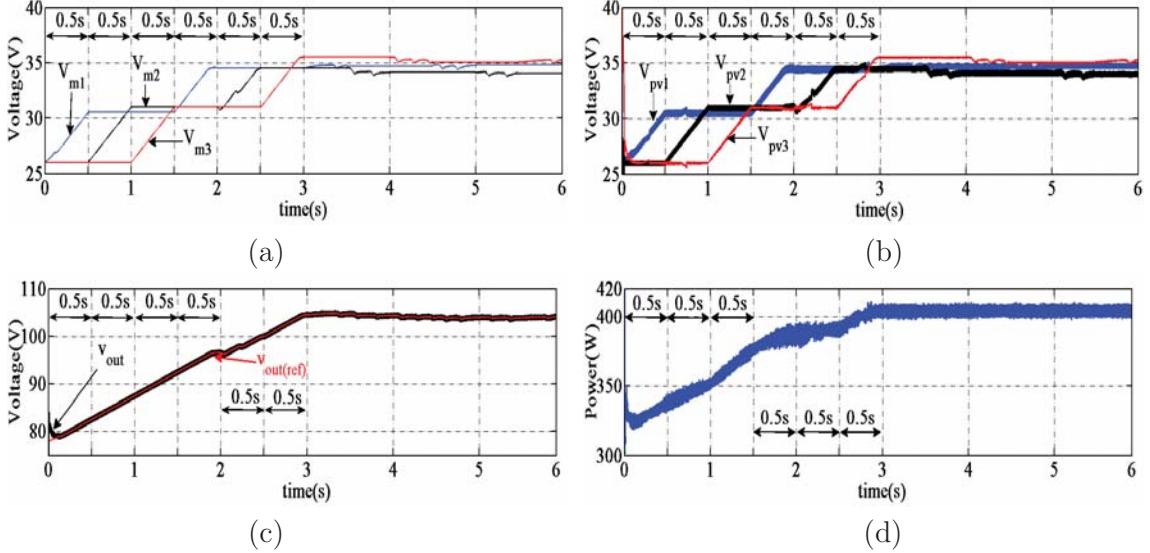


Figure 5.4: Simulated response of the system (Fixed time approach): a) reference voltage commands generated for three PV modules, b) actual voltage across three PV modules, c) reference command and actual voltage across the string, and d) total power output from the string

5.4.1 Fixed time iteration approach

The fixed time interval for which each module is serviced periodically (the corresponding upper limit of j as shown in Fig. 5.2) has been chosen as 0.5 s. The initial voltage references for each module is set at 26 V.

The voltage references generated for each module (V_{m1} , V_{m2} and V_{m3}) are shown in Fig. 5.4(a). From this figure it can be inferred that, during first slot of 0.5 s, V_{m1} is adjusted whereas V_{m2} and V_{m3} are kept at their initialized values, i.e. 26 V. During the second slot of 0.5 s, V_{m2} is adjusted whereas V_{m1} is frozen at its previous updated value. The value of V_{m3} is also kept constant to its previous value during this period. For third slot of 0.5 s, V_{m3} is varied whereas V_{m1} and V_{m2} are kept constant at their previous updated values and this sequence of events is continued. When the references, V_{m1} , V_{m2} and V_{m3} reached their desired values (as provided in Table 5.3), they are maintained around these values as dictated by the P & O algorithm. The PV module voltages are shown in Fig. 5.4(b) wherein it can be noted that they follow their respective references shown in Fig. 5.4(a). The voltage reference command for the string and the actual string voltage are shown in Fig. 5.4(c) wherein the string voltage is observed to follow its reference. The net output

power from the string, P_{tot} is shown in Fig. 5.4(d). From this figure it can be inferred that the string output power is almost equal to the expected maximum power from the string as provided in Table 5.3.

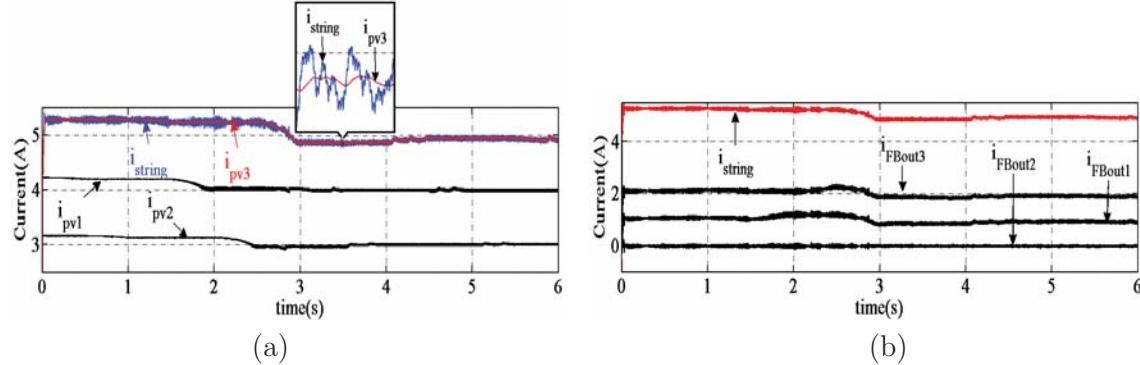


Figure 5.5: Simulated response of the system (Fixed time approach): a) the string current and the currents flowing through three modules, and b) the string current and three balancing currents provided by the flyback converters

The string current, i_{string} and currents flowing through each module are shown in Fig. 5.5 (a). Since magnitude of the current at MPP is highest for module-3 as compared to other modules (Table 5.3), the string current and the current flowing through module-3 has to be equal. This can be inferred from Fig. 5.5 (a) wherein i_{string} and i_{pv3} are observed to be equal. Further, the currents flowing through all the three modules attain their prescribed values implying successful tracking of MPP of each module. The three balancing currents provided by the flyback converters and the string current, i_{string} are shown in Fig. 5.5(b). From this figure it can be inferred that the balancing current provided by the flyback converter connected across module-3 is zero as i_{pv3} is equal to i_{string} . Therefore this flyback converter does not process any power. The flyback converter connected to module-2 provides a balance current given by, $i_{FBout2} = i_{string} - i_{pv2} = 1.91A$ and hence the magnitude of power being processed by it is given by, $i_{FBout2} v_{pv3} = 65W$. The flyback converter connected to module-1 provides a balance current given by, $i_{FBout1} = i_{string} - i_{pv1} = 0.97A$ and hence the magnitude of power being processed by it is given by, $i_{FBout1} v_{pv1} = 33.8W$.

5.4.2 Variable time iteration/Service until MPP approach

The time for which each module is serviced (see Fig. 5.3) is not fixed and depends upon the time duration that a given module takes to reach MPP from its current state. For the sake of fair comparison with fixed time approach, the initial voltage references for each module is set at 26 V.

The voltage references generated for each module (V_{m1} , V_{m2} and V_{m3}) are shown in Fig. 5.6(a). From this figure it can be inferred that at the beginning of execution of the program, module-1 is serviced and its reference voltage V_{m1} is adjusted till it reaches its MPP. The reference voltage commands, V_{m2} and V_{m3} are kept at their initialized values,

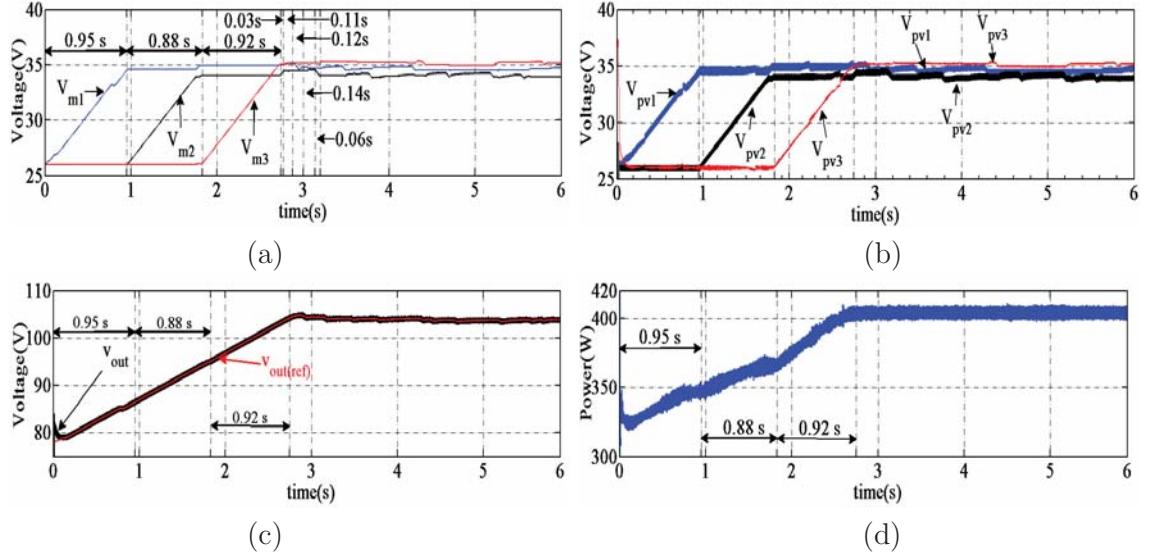


Figure 5.6: Simulated response of the system (Variable time approach): a) reference voltage commands generated for three PV modules, b) actual voltage across three PV modules, c) reference command and actual voltage across the string, and d) total power output from the string

i.e. 26 V while module-1 is serviced. From Fig. 5.6(a) it can be observed that at around 0.95 s the MPP of module-1 is attained. Once it is ensured that the MPP of the module-1 is reached, the controller starts servicing module-2. While servicing module-2, V_{m1} is kept fixed at its previous updated value. The value of V_{m3} is also kept constant to its previous value during this period. The controller services module-2 till it reaches its MPP which takes about 0.88s which can be inferred from Fig. 5.6(a). Once it is ensured that the MPP of the module-2 is reached, the controller starts servicing the module-3. Module-3 is serviced till it reaches its MPP which takes around 0.92s as shown in Fig. 5.6(a). While V_{m3} is varied v_{m1} and V_{m2} are kept constant at their previous updated values. Once MPP of module-3 is reached, the controller starts servicing module-1 again, and this process continues. The reference voltage command for the three modules, V_{m1} , V_{m2} and V_{m3} are provided in Table 5.3. From the Fig. 5.6(a), it can be inferred that once the MPP of each module is reached, the duration of time elapsed between two successive servicing of a module becomes less as all the modules are already being operated at their respective MPPs. Hence any change in operating condition on a module can be addressed within a short period. The PV module voltages are shown in Fig. 5.6(b) wherein it can be noted that they follow their respective references shown in Fig. 5.6(a). The command for the voltage reference of the string and the actual string voltage are shown in Fig. 5.6(c) wherein the string voltage is observed to be following its reference. The net output power from the string, P_{tot} is shown in Fig. 5.6(d). From this figure it can be inferred that the string output power is almost equal to the expected maximum power from the string as provided in Table 5.3.

5.5 Experimental Validation

Experimental validation of the proposed DMPPT strategy is carried on a scaled down laboratory prototype having the circuit configuration of Fig. 5.1. Different components/parameters utilized for developing the laboratory prototype are kept same as those employed for simulation studies. The details of the semiconductor devices employed in the scheme are as follows: (a) switches, $S_1 - S_4$: IXTQ88N30P (MOSFET- 300 V, 88 A), (b) diodes for flyback converters: FFPF30UP20STTU (200 V, 30 A), and (c) diode for buck-boost converter: ISL9R3060G2 (600 V, 30 A). The three PV modules are realized by employing three modules of Agilent make solar array simulator, E4360 A. These modules emulate PV characteristics of a module based on four input parameters, V_{oc} , V_{mpp} , I_{sc} , and I_{mpp} . The aforementioned three modules of the solar array simulator are independently configurable.

The transient response of the system during tracking of MPPs of three modules is shown in Fig. 5.7(a). To simulate the different weather conditions, the MPP set points of the solar array simulator are set as (20.0 V, 0.8 A), (15.0 V, 1.5 A) and (15.0 V, 0.8 A) for PV1, PV2 and PV3 respectively. The open circuit voltage settings are $V_{oc1} = 25$ V, $V_{oc2} = 22$ V and $V_{oc3} = 20$ V for PV1, PV2 and PV3 respectively. The execution of the program is started at time $t = T_{start}$. It can be seen, for $t < T_{start}$, that the electrical parameters of the three PV modules correspond to their open circuit conditions. The $V_{out}(OC) = 66$ V, as expected, is approximately the summation of the three PV voltages while the current sourced by all the PV modules and the output power is practically nil. As soon as the system is started at $t = T_{start}$, the program services each module for 7.5 s to track their respective MPP points. The measured quantities once steady state is reached are as follows: $V_{pv1} = 20$ V, $I_{pv1} = 0.8$ A, $V_{pv2} = 17.5$ V, $I_{pv2} = 1.56$ A, $V_{pv3} = 15$ V, $I_{pv3} = 0.85$ A. This confirms that all of the three modules are operating at their respective MPPs.

Fig. 5.7(b) shows the response of the system when there is a sudden change in the operating condition of one of the PV-modules. The initial MPP set points are maintained to be (20.0 V, 1.5 A), (15.0 V, 1.2 A) and (15.0 V, 1.0 A) for PV1, PV2, and PV3 respectively. At the instant, T_{step} MPP voltage and current of PV3 are increased to 20 V and 2.0 A respectively to emulate sudden change in operating condition on PV3. It can be observed from Fig. 5.7(b) that the system tracks the new MPP of PV3 satisfactorily irrespective of the aforementioned sudden change in operating condition.

The steady state performance of the system demonstrating the function of one the flyback converters is shown in Fig. 5.8(a). The MPP set-points maintained are 20.0 V and 2.0 A for PV-1; 20.0 V and 2.0 A for PV-2, and 15.0 V and 1.0 A for PV-3. From these aforementioned settings it can be inferred that the string current has to be 2 A as the maximum current that can be generated by any of the three PV modules is 2 A. This can be confirmed from Fig. 5.8(a) wherein it is observed that the string current is 2 A. As the current at MPP for PV-3 is 1 A, the flyback converter connected across it has to provide a balance current of 1 A to operate PV-3 at its MPP. From Fig. 5.8(a) it can be observed that the current sourced by the flyback converter-3, I_{FBout3} is 1 A. The current flowing through the secondary winding of the flyback transformer-3, I_{fly3} is also shown in

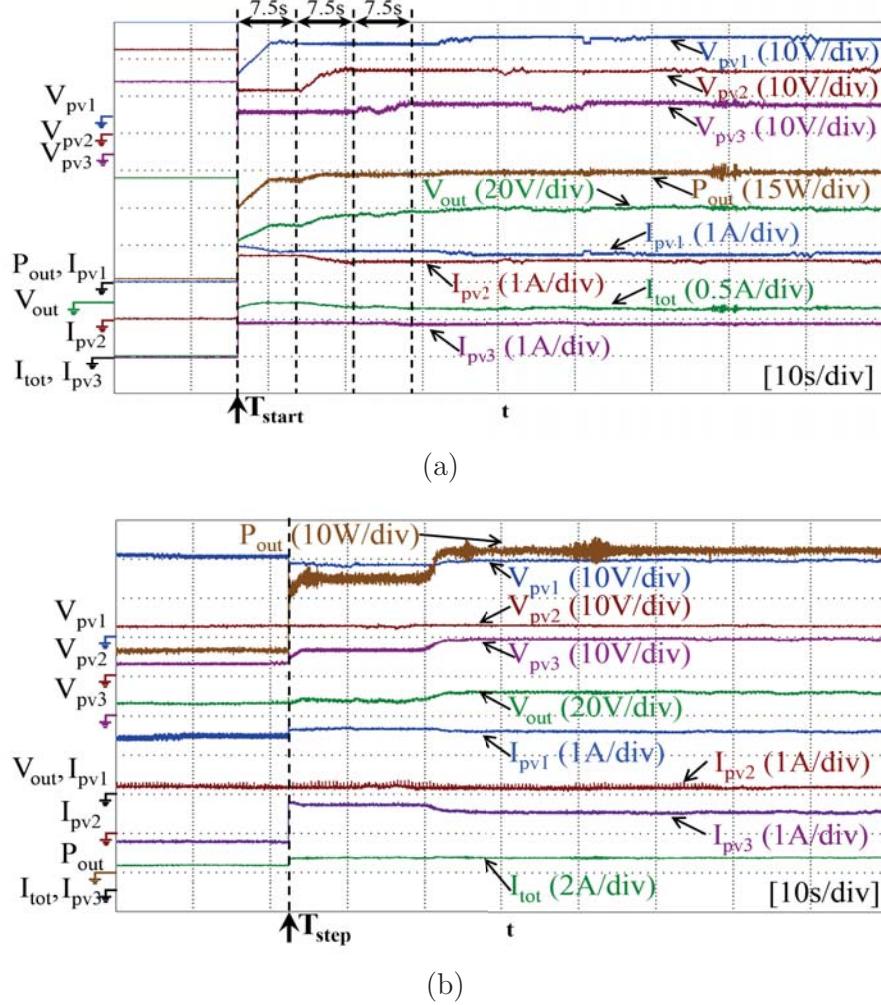


Figure 5.7: Experimental results: (a) performance of the system during MPP tracking from starting of the execution of the proposed DMPPT strategy and (b) performance of the system subjected to step change in insolation level in module-3

Fig. 5.8(a) which confirms the operation of the flyback converter in DCM.

The steady state response of the system showing the output current, I_{tot} along with voltages and currents of three PV modules are provided in Fig. 5.8(b). The MPP set-points are as follows: 20.0 V and 2.0 A for PV-1; 20.0 V and 2.0 A for PV-2, and 15.0 V and 1.0 A for PV-3. From this figure it can be noted that all the PV modules are operating at their respective MPPs. Thus it shows that the scheme is capable of tracking the true maximum power point of each module independently.

A comparison of the proposed scheme with some typical DMPPT schemes reported in the literature is presented in Table 5.4. From this table it can be inferred that the proposed scheme is the only scheme which can extract true maximum power from each of the serially connected modules while facilitating simple implementation, minimal burden on the processor, and reduction in sensor requirement.

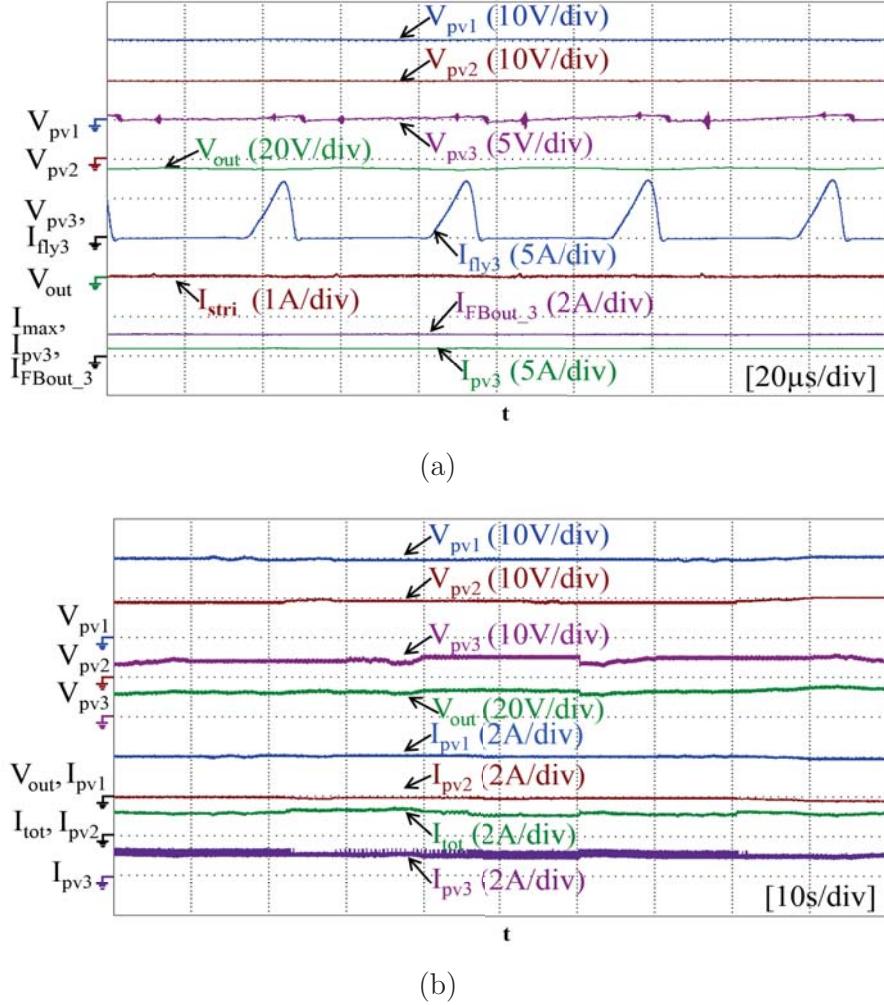


Figure 5.8: Experimental results: (a) the steady state performance of the system demonstrating functioning of one of the flyback converters, and (b) steady state response of the system showing the output current, I_{tot} along with voltages and currents of three PV modules

5.6 Conclusion

This chapter presents a simple distributed maximum power point tracking scheme capable of extracting exact maximum power from serially connected PV modules experiencing mismatched operating conditions. The main advantages of this scheme are: (a) reduced burden on the processor as only one conventional MPPT algorithm is required to be executed at a given time, (b) elimination of communication requirement between local dc-dc converters leading to improved reliability and reduction in cost, (c) elimination of requirement of module level power measurement leading to reduction in current sensor requirement, and (d) simple implementation. The implementation issues and the control philosophy of the proposed scheme is discussed utilizing the power circuit configuration of the existing flyback-converter based standard DMPPT scheme. The efficacy of the scheme is ascertained through detailed simulated performance. The experimental validation of

Table 5.4: Comparison of the proposed scheme with typical DMPPT schemes sans the central converter

Scheme	n_{mpp}	n_{cs}	n_{vs}	True MPP ?	Remarks
[56]	-	1	1	Yes	Difficult to implement for schemes with higher N
[64]	1	1	1	No	Simple to implement but can not extract true MPP from each module
[65]	1	1	N	No	Simple to implement but can not extract true MPP from each module
[66]	N	0	N	No	Needs temperature and insolation sensing
[67]	N	0	N	No	Needs temperature and insolation sensing
[68]	N	$N + 1$	$N + 1$	Yes	Needs extra switch per module, PV string has to be disconnected from central converter periodically
[69]	N	$N + 1$	$N + 1$	Yes	Needs power measurement for every series connected module
[70]	-	$N + 1$	$N + 1$	Yes	Needs more current sensor, complex in control
[71]	$N + 1$	1	$N + 1$	Yes	Complex in control, needs communication between local converters
proposed	1	1	$N + 1$	Yes	simple to implement, reduced burden on processor, exact MPPT scheme

n_{mpp} = number of MPP tracker required to be executed, n_{cs} = no. of current sensor, n_{vs} = no. of voltage sensors, and N = number of series connected module

the scheme is carried out on a scaled down laboratory prototype and the results are found to be satisfactory.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The work carried out in this thesis is focused on designing power electronic interface and associated control philosophy for solar PV based stand alone and grid connected systems. The major contributions of the thesis are as follows:

(1) This thesis proposes a new boost type inverter for application in solar PV based stand alone systems. The proposed inverter operates as a combination of buck-boost dc-dc converter and a full bridge dc-ac inverter. The salient features of the proposed inverter are: (a) minimum requirement in the number of semiconductor devices, (b) minimum requirement of passive elements, (c) reduced voltage stress across dc link capacitor, and (d) reduced voltage gain requirement from the equivalent dc-dc buck-boost converter incorporated inside the inverter. The inclusion of the proposed inverter has led to the development of a three stage stand alone scheme which requires only seven controllable switches. The control structure of the overall stand alone scheme is presented and its efficacy is ascertained by performing detailed simulation studies. The validity of the scheme is ascertained by performing exhaustive experimental validation on a laboratory prototype of the stand alone scheme.

(2) A high frequency transformer coupled dual-input dc-dc converter (TCDIC) is proposed for application in solar PV based stand alone schemes. The unique feature of TCDIC is that it can be made to perform MPPT operation, battery charge control and voltage boosting by employing a proper control algorithm. Hence all of the facilities that are present in the stand alone schemes reported in the literature by involving two or more stages of dc-dc converters, can be obtained by employing the proposed single stage TCDIC. A standard full bridge inverter is employed at the output of the TCDIC to achieve dc-ac conversion. Thus the resultant stand alone scheme comprises of only two power conversion stages as opposed to the existing stand alone schemes which require a minimum number of three power conversion stages. The salient features of the proposed stand alone scheme are: (a) MPP tracking of PV array, charge control of the battery, and boosting of the dc voltage are accomplished through a single converter, (b) enhancement of utilization of power converters as requirement of a dedicated converter for ensuring MPP operation of the PV array is eliminated, (c) enhancement in battery charging efficiency as a single converter is present in the battery charging path, (d) lesser component count as only two power conversion stages are required, (e) the load is galvanically isolated from the PV panel and the battery, and (f) simple and efficient control structure ensuring proper operating mode

selection and smooth transition between different possible operating modes. The efficacy of the scheme is verified by performing detailed simulation studies. The viability of the scheme is confirmed by performing detailed experimental studies.

(3) A multi-purpose transformerless inverter scheme is proposed for application in PV based decentralized grid connected systems. This inverter has the voltage buck-boost capability and can be utilized to extract maximum power from a single as well as two separate PV arrays. While extracting maximum power from a single PV array the same converter can be utilized to negotiate dc loads as well. The aforementioned dc loads can be supplied from the PV array and/or the grid depending on the availability of power from the PV source. Thus the proposed converter can serve as a dc to ac inverter (PV to grid), dc to dc converter (PV to dc load), and ac to dc converter (grid to dc load). The other advantages of the proposed scheme includes, (a) elimination of concerns pertaining to the flow of leakage current in transformerless grid connected solar PV systems, (b) elimination of grid current sensor requirement, and (c) elimination of shoot-through problem. The control structures devised for the aforementioned applications of the proposed scheme are presented. The effectiveness of the proposed scheme for all of the aforementioned applications have been ascertained through detailed simulation studies. A laboratory prototype for the scheme is developed and experimental validation is carried out for the scheme when it is employed to extract maximum power from single as well as two separate PV arrays.

(4) In order to extract maximum power from serially connected PV modules experiencing mismatched operating conditions, a simple distributed maximum power point tracking (DMPPT) scheme is proposed. The main advantages of this scheme are as follows: (a) reduced burden on the processor as only one conventional MPPT algorithm is required to be executed, (b) elimination of communication requirement between local dc-dc converters leading to improved reliability and reduction in cost, (c) elimination of requirement of module level power measurement leading to reduction in current sensor requirement, and (d) simple implementation. The implementation issues and the control philosophy of the proposed scheme is discussed utilizing the power circuit configuration of the existing flyback-converter based standard DMPPT scheme. The efficacy of the scheme is ascertained through detailed simulated performance. The experimental validation of the scheme is carried out on a scaled down laboratory prototype and the results are found to be satisfactory.

6.2 Scope of Future Work

Two schemes for stand alone systems are proposed in this thesis. An attempt can be made to improve these schemes through further reduction in component count, employment of soft switching technique, etc. Further, the application of these schemes can be extended to areas where grid is present but the availability of power is not consistent. In such scenario attempts can be made to design the stand alone schemes such that the battery can be charged from the grid as well as PV. This will improve the availability of power to the household appliances in case of grid outage as well as unavailability of PV

power. Further, integration of the proposed stand alone scheme to other renewable or conventional energy sources can be carried out.

The inverter proposed for decentralized grid connected scheme are designed to operate under discontinuous conduction mode (DCM). This leads to reduction in efficiency owing to the flow of considerable RMS current through the switches and the inductors. Efforts can be made to design the converter to operate under continuous conduction mode so as to improve the efficiency of the inverter.

For medium and high power PV systems, DMPPT schemes are going to play a major role. Most of the existing DMPPT schemes are designed for PV strings having number of series connected PV modules. These schemes are commonly termed as shunt compensation schemes as they connect dc-dc converters across PV modules to provide required compensating current/power so as to operate each PV module at their respective MPPs. The same concept can be extended for compensating PV modules which are connected in parallel by means of series compensation. Though there are few schemes which address this issues, more involved research work can be carried out on this topic. Further, a combination of both series and shunt compensation may be investigated for application in large power plants where PV modules/strings are required to be connected in series as well as in parallel.

List of Publications

Journal Publications:

A. Published:

1. D. Debnath and K. Chatterjee, “A Two Stage Solar Photovoltaic based Stand Alone Scheme having Battery as Energy Storage Element for Rural Deployment,” *IEEE transaction on Industrial Electronics*, vol. 62, no. 7, pp. 4148-4157, July 2015

B. Accepted:

1. D. Debnath and K. Chatterjee, “Neutral point clamped transformerless grid connected inverter having voltage buck boost capability for solar photovoltaic systems,” accepted for publication in IET Power Electronics. (doi: 10.1049/iet-pel.2014.0873)
2. D. Debnath, P. De, and K. Chatterjee, “Simple scheme to extract maximum power from series connected photovoltaic modules experiencing mismatched operating conditions,” accepted for publication in IET Power Electronics. (doi: 10.1049/iet-pel.2015.0068)
3. D. Debnath and K. Chatterjee, “Solar photovoltaic-based stand-alone scheme incorporating a new boost inverter,” accepted for publication in IET Power Electronics. (doi: 10.1049/iet-pel.2015.0112)

C. Provisionally Accepted:

1. D. Debnath and K. Chatterjee, “Maximizing Power Yield in a Transformerless Single Phase Grid Connected Inverter Servicing Two Separate PV Panels,” provisionally accepted subjected to major revision in IET Renewable Power Generation.

Patent Filed:

1. D. Debnath and K. Chatterjee, “Transformer-less grid connected inverter with two separate PV arrays while minimizing leakage current,” Indian patent, Appl. No. 1873/MUM/201 5 (filed on 12-5-2015)

Conference Publications:

1. D. Debnath and K. Chatterjee, "A buck-boost integrated full bridge inverter for solar photovoltaic based stand alone system," *in Proc. IEEE Photovoltaic Specialists conf. (PVSC)*, pp: 2867- 2872, June 2013.
2. D. Debnath and K. Chatterjee, "Transformer coupled multi-input two stage stand alone solar photovoltaic scheme for rural areas," *in Proc. IEEE Indus. Electron. Society Conf. (IECON)*, pp. 7028- 7033, Nov. 2013.
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