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Solar photovoltaic-based stand-alone scheme incorporating a new boost inverter

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Abstract: This study considers the design of a solar photovoltaic (PV)-based stand-alone system using a battery for energy storage. Its main feature is a new boost inverter, derived by integrating a dc–dc buck–boost converter and a full bridge dc–ac inverter, which can perform simultaneous voltage boosting and dc–ac conversion. Inclusion of this inverter has led to the development of a three stage stand-alone scheme which can operate with low voltage level(s) for the PV and the battery. The logical evolution and operating principles of this inverter are presented, followed by an overview of the entire stand-alone scheme and its control structure. The complete scheme is validated both by detailed simulation studies and exhaustive experimental studies on a laboratory prototype.

1 Introduction

Rural electrification being a promising measure to improve the quality of living standards and to enhance the economic growth in rural areas, has become an emerging topic of interest in developing countries. The solar photovoltaic (PV)-based systems are increasingly being adopted as the source of electricity in such schemes [1]. This paper deals with the design of a solar PV-based stand-alone scheme for rural areas where power grid is not available. In addition to the solar PV modules/arrays, stand-alone systems also require the service of, (a) energy storage element typically being realised by battery bank to compensate for the intermittent nature of the PV power [2], and (b) power electronic converters to form the interfacing link between PV, battery, and the ac load.

A typical stand-alone scheme for rural house hold application is required to be designed for a power rating in the range of 250 – 500 VA. The voltage levels for the PV array and the battery are generally chosen to be in the range of 24 – 36 V. To avoid drawbacks associated with the choice of higher voltage levels for the battery and the PV array are as follows: (a) safety concern pertaining to high voltage [3], (b) requirement of complex maximum power point tracking (MPPT) algorithm or additional arrangement/converters to extract maximum power from series connected PV module system experiencing mismatched operating conditions [4–6], and (c) increased size and cost for series connected battery bank. Further, most of the stand-alone systems employ a full-bridge inverter for dc–ac conversion [7–11]. This full-bridge inverter being a buck type inverter requires at its input a dc bus voltage >350 V to maintain 230 V, 50 Hz (Indian standard) at the load terminal. To achieve such a high dc bus voltage the gain requirement from the intermediate dc–dc converters which interface the PV array and the battery to the input dc bus of the inverter becomes high and lie in the range of 9–15. Such a high gain can be achieved by employing three dc–dc converters [10]. However, this approach results in low efficiency and less reliability as four converters are involved in the scheme. High gain can also be realised by employing two high gain transformer coupled dc–dc converters [11–13]. However, this approach requires minimum number of six controllable switches to realise two dc–dc converters and four switches to realise the inverter. A possible solution to realise high gain is to employ a boost inverter instead of a conventional buck type full-bridge inverter. However, the existing inverter topologies which can be used as boost type inverter have the following drawbacks: (a) high switch count (≥ 5) [14–18], (b) high-voltage stress across dc-link capacitor [19–21], (c) higher number of passive elements [19, 20], and (d) complex control [20, 21]. To overcome the aforementioned drawbacks of these inverters, this paper proposes a new topology of a boost inverter. Since this new topology is derived by integrating a dc–dc buck–boost converter with a full-bridge inverter, the proposed inverter is termed as buck–boost integrated full-bridge inverter (BBIFBI). The proposed BBIFBI requires only four controllable switches, one diode, one dc-link capacitor, and one inductor. The stress across the dc-link capacitor is considerably less than that of other boost type inverter topologies. The stand-alone scheme formed by incorporating BBIFBI is a three stage one consisting of two dc–dc converters and the BBIFBI. The proposed scheme requires only seven controllable switches. The basic concept of the aforementioned scheme incorporating BBIFBI and its very preliminary study has been presented in [22]. The new contributions made in this paper as compared with [22] are as follows: identifying the evolution process involved in BBIFBI, inclusion of a detailed discussion on its gain profile, presenting the overall control algorithm of the entire scheme while highlighting issues concerning its implementation, exhaustive experimental validation of the stand-alone scheme, objective comparison of the BBIFBI with other boost type inverters, and comparison of the proposed stand-alone scheme with other stand-alone systems. This paper is organised as follows: the operating principle of BBIFBI is explained in Section 2. The control algorithm for the overall stand-alone scheme is presented in Section 3. The simulated performance of the scheme obtained through the MATLAB/SIMULINK platform is provided in Section 4. The measured performance of the scheme obtained by performing detailed experimental studies on a laboratory prototype of the scheme, is presented in Section 5.

2 Principle of operation of BBIFBI

In this section, the process of derivation of BBIFBI from a combination of a buck–boost dc–dc converter and a full-bridge dc–ac inverter is first elaborated. Subsequently the operating principle of BBIFBI is explained. The combination of a buck–boost dc–dc converter and a full-bridge dc–ac inverter is depicted in Fig. 1*a*. The buck–boost converter of Fig 1*a* is a reconfigured version of the standard buck–boost converter having its input

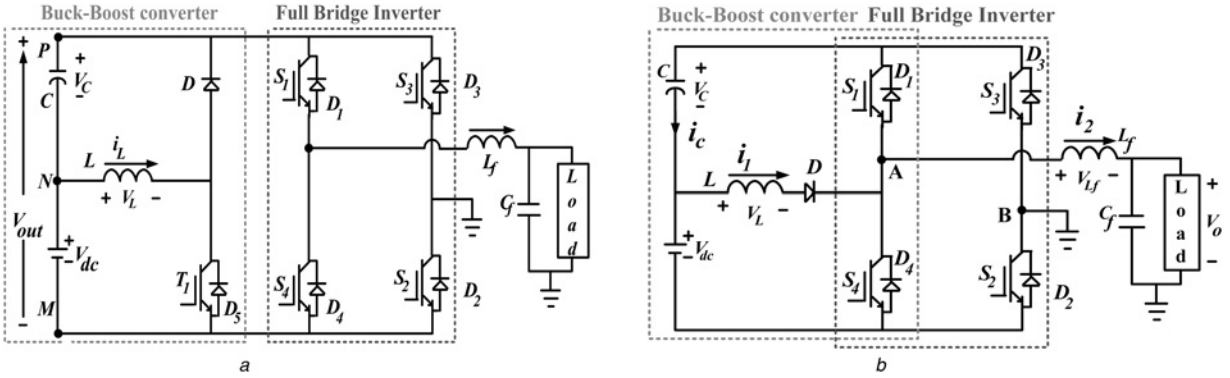

Fig. 1 *Schematic circuit diagrams depicting*

a Combination of a buck–boost converter and a full bridge inverter
b Structure of the proposed BBIFBI

terminals as N and M, and having its output terminals as P and N [23]. When the switch T_1 is on, the inductor, L stores energy from the input source, V_{dc}. When T_1 is turned off the energy stored in L is transferred to the output capacitor C through the diode D. The voltage across L, v_L can be expressed as

$$v_L = V_{dc}, \quad \text{when } T_1 \text{ is on}$$
$$v_L = -V_c, \quad \text{when } T_1 \text{ is off}$$

Assuming continuous conduction mode (CCM) of operation and equating average voltage drop across the inductor, L to be zero, voltage across the capacitor, C can be expressed as

$$V_c = [d/(1-d)]V_{dc} \tag{1}$$

wherein d is the duty ratio of the switch T_1. The voltage across the terminals, P and M, V_{out} can be expressed as

$$\begin{aligned} V_{out} &= (V_c + V_{dc}) \\ &= [(d/(1-d)]V_{dc} + V_{dc} \\ &= [1/(1-d)]V_{dc} \end{aligned} \tag{2}$$

This expression for V_{out} is similar to the expression of output voltage of a boost converter operating under CCM having V_{dc} as its input. Therefore, if M and P are considered to be output terminals, the operation of the buck–boost converter shown in Fig. 1*a* resembles to that of a boost converter. The advantages of this configuration of the buck–boost converter over the conventional configuration of boost/buck–boost converter are as follows: (a) the voltage gain requirement from the buck–boost converter is less as gain requirement in this case is $(V_{out} - V_{dc})/V_{dc}$ as compared with (V_{out}/V_{dc}) in case of the conventional topology, (b) the voltage stress across capacitor C is less by an amount V_{dc}, and (c) voltage stress across T_1 and D is V_{out} as compared with $(V_{out} + V_{dc})$ for the conventional buck–boost converter. Considering Fig. 1*a*, the full-bridge inverter formed by four switches S_1–S_4 and having P and M as input terminals 'sees' a boost converter with respect to input voltage V_{dc}. Thus the scheme shown in Fig. 1*a* can be visualised as a combination of full-bridge inverter following a boost converter, having input source connected between terminals, N and M.

The process of combination of the two converters shown in Fig. 1*a* leads to the evolution of a new converter which is shown in Fig. 1*b*. In this converter, the switches S_1 and S_4 are shared by both buck–boost converter and the full-bridge inverter. The diode D is employed to ensure that the power flow through the buck–boost converter segment is unidirectional. The proposed converter reduces the switch count by one as compared with the scheme shown in Fig. 1 while preserving all its advantages. The switches of the BBIFBI are controlled in a similar fashion to that of the conventional full-bridge inverter employing unipolar sinusoidal pulse-width modulation (SPWM) scheme for deriving gating pulses for the switches, $S_1 - S_4$. For simplicity, unity power factor operation is considered for describing the operation of the BBIFBI. However, it is to be noted that the operation of the BBIFBI is not restricted only for unity power factor operation.

2.1 Operation of BBIFBI in positive half cycle (PHC)

In unipolar SPWM technique, the gating pulses for the four switches of the inverter are provided in the following sequence for PHC of the load voltage: (a) state 1: gating pulses are provided for S_1 and S_2, (b) state 2: gating pulses are provided for S_4 and S_2, (c) state 3: gating pulses are provided for S_1 and S_2, and (d) state 4: gating pulses are provided for S_1 and S_3. This switching sequence is repeated in every switching cycle.

2.1.1 Operation in CCM: When the BBIFBI operates in CCM, the current, i_1 flowing through the inductor, L is continuous and positive. Further, the current, i_2 flowing through the filter inductor, L_f is also positive in PHC as unity power factor operation is considered for the analysis. The operation of BBIFBI for the aforementioned four switching states depend on the difference between i_1 and i_2.

Case 1: When $i_1 > i_2$: The operation of BBIFBI for this case is as follows:

(a) *State 1:* In this state, the gating pulses for the switches, S_1 and S_2 are provided. As i_2 is positive, the switch S_2 conducts to provide a path for i_2 while its anti-parallel diode, D_2 remains idle. However, as $i_1 > i_2$, the diode D_1 conducts (though gating pulse for S_1 is provided). Since $i_1 > i_2$, the capacitor, C, gets charged. Thus, the switch, S_2 and the diode, D_1 conducts in this state. The current, i_1 decreases as '$-V_c$' is impressed across L while i_2 increases as $(V_c + V_{dc} - V_o)$ which is positive, is impressed across L_f. The current flowing through different components of BBIFBI in this state is depicted in Fig. 2*a*. This state continues till gating pulse of S_1 is withdrawn and simultaneously gating pulse for S_4 is released.

(b) *State 2:* In this state, the gating pulses for the switches, S_4 and S_2 are provided. As $i_1 > i_2$, S_4 conducts. The switch, S_2 also conducts as i_2 is positive. The current, i_1 increases as '$+V_{dc}$' is impressed across L while i_2 decreases as '$-V_o$' is impressed across L_f. The current flowing through different components of BBIFBI in this state is depicted in Fig. 2*b*. This state continues till gating pulse of S_4 is withdrawn and simultaneously gating pulse for S_1 is released.

(c) *State 3:* The situation remains the same as that of state 1. This state continues till gating pulse of S_2 is withdrawn and simultaneously gating pulse for S_3 is released.

(d) *State 4:* In this state, the gating pulses for the switches, S_1 and S_3 are provided. As i_2 is positive, the diode, D_3 conducts though gating

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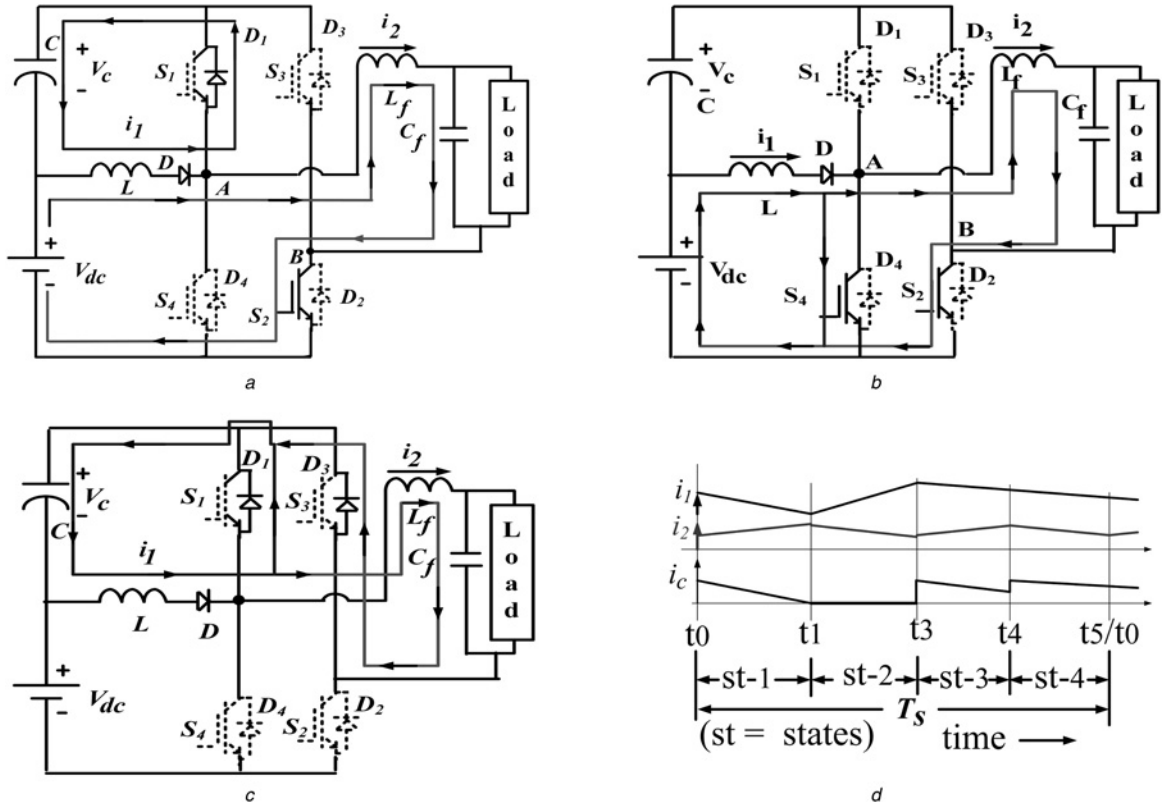

Fig. 2 *BBIFBI in PHC while operating in CCM under case 1*

a Current path in state 1
b Current path in state 2
c Current path in state 4
d Waveforms of i_1, i_2, and i_c

pulses for S_3 is provided. Further, as $i_1 > i_2$ the diode, D_1 conducts (though gating pulse for S_1 is provided) and C gets charged. The current, i_1 decreases as '$-V_c$' is impressed across L while i_2 also decreases as '$-V_o$' is impressed across L_f. The current flowing through different components of BBIFBI in this state is depicted in Fig. 2*c*. This state continues till gating pulse of S_3 is withdrawn and simultaneously gating pulse for S_2 is released, and then state 1 follows.

The waveforms of i_1, i_2, and i_c for the aforementioned four states for the condition $i_1 > i_2$ are depicted in Fig. 2*d*.

Case 2: When $i_1 < i_2$: The operation of BBIFBI for this case is as follows:

(a) *State 1:* As i_2 is positive, the switch, S_2 conducts. However, as $i_1 < i_2$ the switch, S_1 conducts (its anti-parallel diode, D_1 remains idle). Thus switches, S_1 and S_2 conduct in this state. Since $i_1 < i_2$, the capacitor, C is discharged. The current, i_1 decreases as '$-V_c$' is impressed across L while i_2 increases as $(V_c + V_{dc} - V_o)$ which is positive, is impressed across L_f. The current flowing through different components of BBIFBI in this state is depicted in Fig. 3*a*.
(b) *State 2:* As $i_1 < i_2$, D_4 conducts (though gating pulse for S_4 is provided). The switch S_2 also conducts as i_2 is positive. The current, i_1 increases as '$+V_{dc}$' is impressed across L while i_2 decreases as '$-V_o$' is impressed across L_f. The current flowing through different components of BBIFBI in this state is depicted in Fig. 3*b*.
(c) *State 3:* The situation remains the same as that of state 1 of case 2.
(d) *State 4:* As i_2 is positive, the diode, D_3 conducts though gating pulse for S_3 is provided. Further, as $i_1 < i_2$ the switch, S_1 conducts and C gets charged as i_1 completes its path through C. The current, i_1 decreases as '$-V_c$' is impressed across L while i_2 also decreases as '$-V_o$' is impressed across L_f. The current flowing through different components of BBIFBI in this state is depicted in Fig. 3*c*.

The waveforms of i_1, i_2, and i_c for the aforementioned four states for the condition $i_1 > i_2$ are depicted in Fig. 3*d*.

2.1.2 Operation in discontinuous conduction mode (DCM): When the converter operates in DCM, the current, i_1 flowing through, L is greater than zero for some portion and is zero for the remaining portion in a given switching time period. The switching sequences are same as that of the case of CCM. However, out of the four switching states, i_1 can increase only in state 2. Since the operation in DCM is being considered, i_1 becomes zero before the initiation of state 2, and i_1 starts increasing from zero in this state. Hence, the operation of BBIFBI in DCM is described starting from state 2 for ease of understanding.

(a) *State 2:* At the starting of this state $i_1 > i_2$ (end point of the previous state, $t2$) and hence D_1 and S_2 conducts. As S_1 is turned on, '$-V_c$' is impressed across L and as a consequence i_1 starts decreasing. The current, i_2 increases as $(V_c + V_{dc} - V_o)$ which is positive is impressed across L_f. This continues till i_2 becomes equal to i_1. The time interval corresponding to this case is $t2$and $t3$ as shown in Fig. 4. When i_2 exceeds i_1 switches, S_1 and S_2 conduct for $t3$and $t4$ as shown in Fig. 4. This state continues till gating pulse of S_2 is withdrawn and simultaneously gating pulse for S_3 is released.
(b) *State 3:* At the starting of this state $i_1 < i_2$ (end point of the previous state, $t4$) and hence S_1 conducts. As i_2 is positive, the diode, D_3 conducts though gating pulses for S_3 is provided. In this state, both i_1 and i_2 decrease (as voltage across L is $-V_c$ and voltage across L_f is $-V_o$). Since $i_1 < i_2$, S_1 and D_3 conduct entirely in this state having corresponding time interval $t4$ and $t5$ as shown

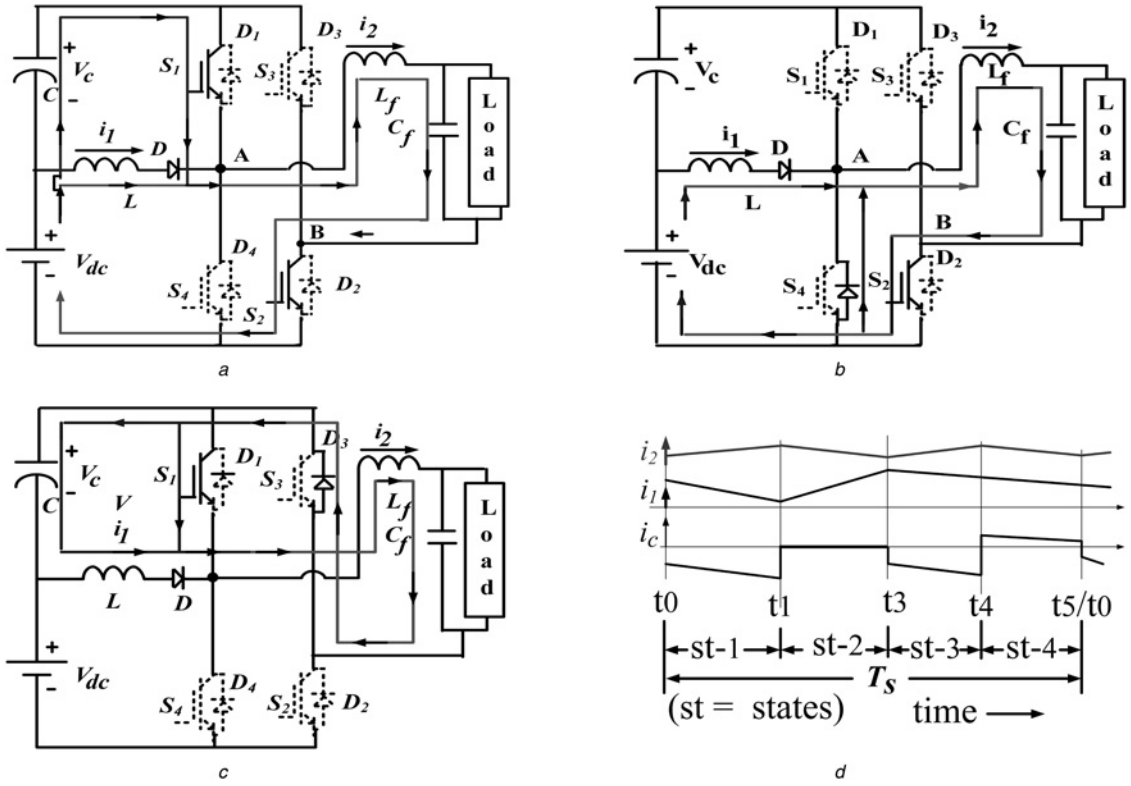

Fig. 3 *BBIFBI in PHC while operating in CCM under case 2*

a Current path in state 1
b Current path in state 2
c Current path in state 4
d Waveforms of i_1, i_2, and i_c

in Fig. 4. This state continues till gating pulse of S_3 is withdrawn and simultaneously gating pulse for S_2 is released.

(c) *State 4:* When S_2 is turned on, i_2 increases as $(V_c + V_{dc} - V_o)$ which is positive is impressed across L_f. However, i_1 continues to decrease as '$-V_c$' is impressed across L. This situation continues till i_1 becomes zero (DCM operation). The time interval corresponding to this case is $t5$ and $t6$ as shown in Fig. 4. When i_1 reaches zero it gets clamped to this value (i_1 cannot become negative due to the presence of D) while i_2 continues to increase till the end of this state. The time interval corresponding to this case is $t6$ and $t7$ as shown in Fig. 4. This state continues till gating pulse for S_1 is withdrawn while gating pulse for S_4 is released which marks the beginning of state 2 and this process continues.

(d) *State 1*: In this state, the gating pulses for the switches, S_4 and S_2 are provided. The initial value of i_1 at the starting of this state is zero. However, i_1 starts increasing as '$+V_{dc}$' is impressed across L. The current, i_2 is positive and it decreases as '$-V_o$' is impressed across L_f.

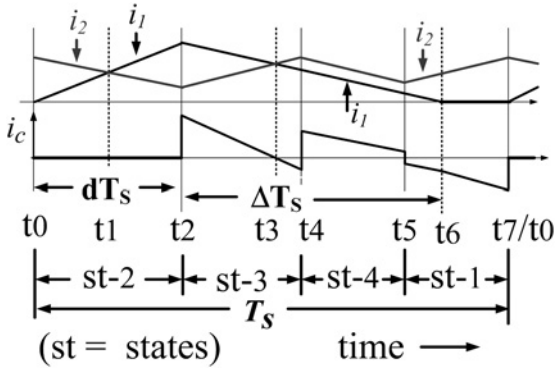

Fig. 4 *Waveforms of* i_1, i_2, *and* i_c *while operating in DCM*

At the starting of state 2, $i_1 < i_2$ and hence S_2 and D_4 conduct. This process continues till i_1 becomes equal to i_2. The time interval corresponding to this case is $t0$ and $t1$ as shown in Fig. 4. When i_1 becomes more than i_2 switches S_2 and S_4 conduct for the time interval $t1$ and $t2$ as shown in Fig. 4. This state continues till gating pulse of S_4 is withdrawn and simultaneously gating pulse for S_1 is released.

2.2 Operation of BBIFBI in negative half cycle

The switching sequence is divided into four switching states, and is described as follows:

(a) State 1 ($S_3 - S_4$ ON): When S_3 and S_4 are ON, current flowing through L increases and the capacitor, C gets discharged.
(b) State 2 ($S_2 - S_4$ ON): The situation remains the same as that of state 2 of the PHC.
(c) State 3 ($S_3 - S_4$ ON): The situation remains the same as that of state 1 of the negative half cycle.
(d) State 4 ($S_3 - S_1$ ON): The situation remains the same as that of state 4 of the PHC.

In CCM, the expression for V_c can be obtained by equating the average voltage across the inductor, L to zero which leads to

$$V_c = (d/1-d)V_{dc} \tag{3}$$

wherein d is the duty ratio of the switch, S_4 and is given by

$$d = \frac{1 - M\sin wt}{2} \tag{4}$$

wherein M is the modulation index for unipolar SPWM scheme.

From Figs. 1*b* and 4, the expression for the inductor voltage in DCM mode is given by

$$\begin{aligned} v_L &= V_{dc} \quad \text{for } 0 < t < dT_s \\ &= -V_{dc} \quad \text{for } dT_s < t < (d+\Delta)T_s \\ &= 0 \quad \text{for } (d+\Delta)T_s < t < dT_s \end{aligned}$$

The peak value of inductor current is given by

$$I_{peak} = \frac{V_{dc}}{L} dT_s$$

Equating average voltage across the inductor over a switching cycle to be zero

$$\Delta = \frac{dV_{dc}}{V_c}$$

The average charging current of C over a switching cycle, T_s (time interval $t2$–$t6$ in Fig. 4) is given by

$$I_{chsc} = \frac{I_{peak}}{2T_s}\Delta T_s = \frac{V_{dc}^2 d^2 T_s}{2LV_c} \tag{5}$$

Hence the average charging current of the capacitor, C over a power cycle is given by

$$I_{chpc} = \frac{1}{2\Pi}\int_0^{2\Pi} I_{chsc} d(\omega t) = \frac{V_{dc}^2}{8LF_sV_c}\left(1 + \frac{M^2}{2}\right) \tag{6}$$

wherein $F_s(=1/T_s)$ is the switching frequency. Now, assuming the inverter to be lossless

$$(V_c + V_{dc})I_{dc} = P_l \tag{7}$$

wherein I_{dc} is the average discharging current of the capacitor over a power cycle and P_l is the load power. Now, under steady-state condition both the average charging and discharging currents of the capacitor are same so as to make the average capacitor current to be zero. Therefore, in steady state

$$I_{dc} = I_{chpc} \tag{8}$$

Combining (6)–(8)

$$V_c = \frac{V_{dc}^3\left(1 + \left(M^2/2\right)\right)}{8P_lLF_s - V_{dc}^2\left(1 + \left(M^2/2\right)\right)} \tag{9}$$

From (9), the capacitor voltage, V_c increases with increment in V_{dc} and M, and decreases with increment in P_l, L and F_s when the system operates in DCM. As per (4), the average value of the duty ratio for the switch, S_4 is 0.5. Therefore, if the buck–boost segment of the converter operates in CCM, the gain of this segment is 2 when the input voltage is V_{dc} and the output voltage is V_{out} as per (2) and (3). If the buck–boost segment of the converter operates in DCM, the gain of this segment is more than 2 as gain obtained in DCM mode is higher than that of CCM mode. However, from (4) it can be noted that duty ratio for switch S_4 varies over a wide range under unipolar SPWM switching scheme and hence a large value of L is required to ensure that the converter operates in CCM whereas a very small value of inductance is required to ascertain its operation in DCM. To have operation in CCM the size and weight of the inductor becomes considerable. However, as DCM operation requires a lower value of inductance, the current rating of the switches, S_1 and S_4 and that of the inductor itself becomes considerable. Therefore, the inverter is intended to operate partly in CCM and partly in DCM over a power cycle. As a result, the overall voltage gain obtained from the buck–boost converter segment is >2. As the duration for which the converter operates in CCM or DCM depends on several parameters, the voltage gain from the buck–boost converter portion is variable and is also difficult to find a closed form expression for it. To obtain the rough estimate of the aforementioned gain, the converter is simulated on MATLAB/SIMULINK platform. The variation in gain with respect to different parameters is shown in Figs. 5*a* and *b*.

Selection of C: The capacitor, C designed as per the guidelines provided in [24], is presented as follows:

$$C = \frac{2.4P_l}{f\Delta V_c(V_c + V_{vc})} \tag{10}$$

wherein f is the frequency of the load voltage and ΔV_c is the voltage ripple across C.

3 Stand-alone scheme and its control structure

Fig. 5*c* depicts the schematic circuit diagram for the proposed stand-alone scheme. In addition to the BBIFBI, it houses a conventional boost converter to perform MPPT for the PV array and a conventional bidirectional dc–dc converter for charge/discharge control of the battery. The power rating of the system is 500 VA and the voltage level for PV array (at standard test condition) and the battery is chosen to be 36 V.

3.1 Control of BBIFBI

The inverter segment of the proposed BBIFBI is controlled in a manner similar to that of a conventional full-bridge inverter employing proportional–integral-based closed-loop control. Unipolar SPWM scheme is employed for deriving gating pulses for four switches of BBIFBI. However, the input voltage seen by the inverter segment is $(V_c + V_{dc})$ as shown in Fig. 1*b*. Also this voltage has to be more than the peak of sinusoidal load voltage. Since the amplitude of the voltage to be maintained at the load terminal is 325 V ($=230*\sqrt{2}$), the minimum value for $(V_c + V_{dc})$ is set at 350 V to account for the voltage drops across the filter inductor and semiconductor devices of BBIFBI. The maximum value for $(V_c + V_{dc})$ is chosen as 400 V so that the voltage stress on the semiconductor devices is also limited to 400 V. Since input voltage of the BBIFBI, V_{dc} is connected at the output terminals of the boost converter, V_{dc} must be greater than V_{pv}. To accommodate the variation in V_{pv} with variation in environmental conditions, the minimum value for V_{dc} is chosen as 50 V. The output voltage of the buck–boost converter segment, V_c is controlled by controlling the input voltage, V_{dc}. A plot depicting the values of V_{dc} required to control V_c at three desired values for different loading conditions is shown in Fig. 5*d*. The aforementioned plot is obtained by simulating the BBIFBI on a MATLAB/SIMULINK platform utilising the parameters provided in Table 3. These three values are chosen based on the gain profiles are shown in Fig. 5. From Fig. 5*d*, it can be observed that if V_c is maintained at 335 V for $P_l < 50$ W, at 325 V for $50 < P_l < 150$ W, and at 300 V for $150 < P_l < 500$ W then $(V_c + V_{dc})$ can be maintained in the desired range of 350–400 V and V_{dc} can be maintained at a level higher than 50 V. Neglecting losses in the system, the load power demand can be estimated from the following power balance equation:

$$P_l = P_{pv} - P_b \tag{11}$$

wherein P_{pv} and P_b are the PV and battery power, respectively.

The control structure employed to control the capacitor voltage, V_c at the desired value is marked by the dotted rectangle in Fig. 6. From this figure, it can be noted that V_c is controlled by manipulating V_{dc}.

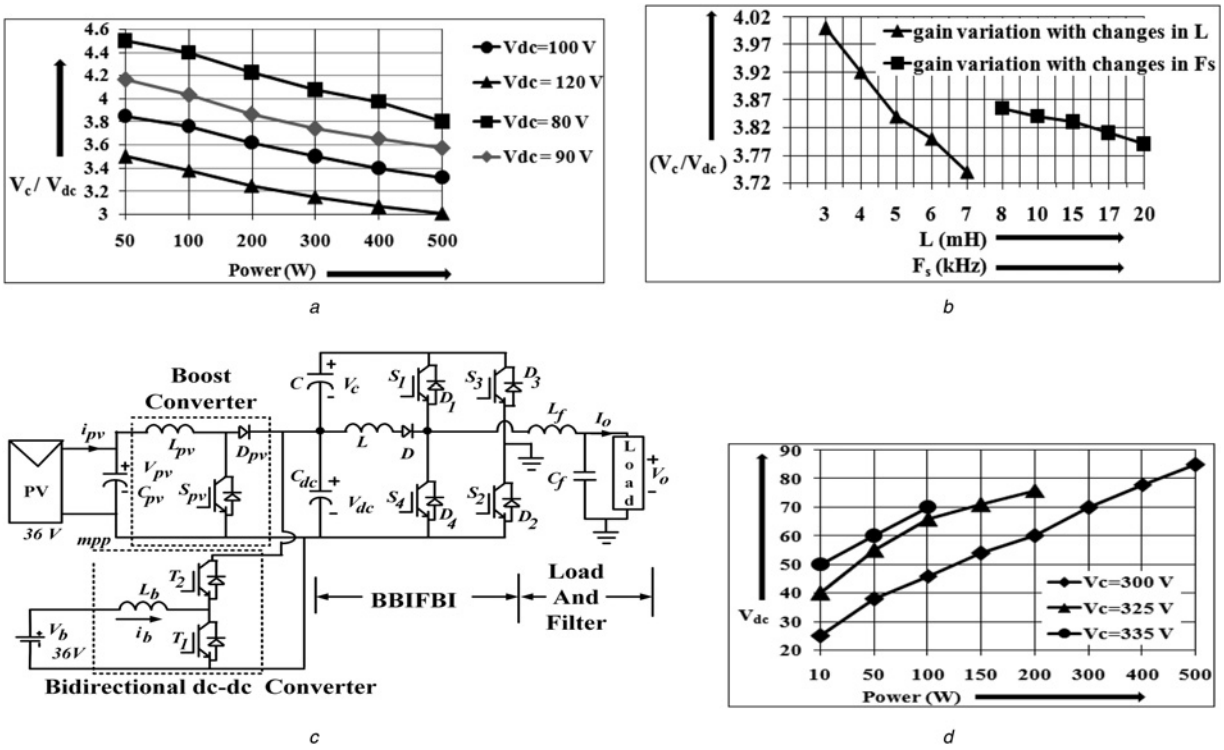

Fig. 5 *Voltage gain profile of the buck–boost converter segment of the BBIFBI, and schematic diagram of the overall stand alone scheme*

a Variation of voltage gain of the buck-boost converter segment with respect to V_{dc} and P_l with $L = 6$ mH, $F_s = 20$ kHz
b Variation of voltage gain of the buck-boost converter segment with respect to L and F_s with $V_{dc} = 90$ V, $P_l = 250$ W
c Schematic circuit diagram of the overall stand-alone system incorporating BBIFBI
d Plot showing required values of V_{dc} to maintain V_c at three desired values for different loading conditions

3.2 Control of boost and bidirectional dc–dc converter

The schematic diagram of the controller used for the dc–dc converters of the stand-alone scheme is shown in Fig. 6*a*. The role of these two converters depends on the mode of operation of the stand-alone scheme. Typically a stand-alone scheme operates in one of the following modes: maximum power point (MPP) mode, non-MPP mode, battery-only (BO) mode, and shutdown (SD) mode [22, 25]. The mode selection criteria's are provided in Table 1. The selection of a proper mode and shifting of operation among various modes are carried out by the algorithm depicted in Fig. 6*b*. This algorithm generates two mode selection signals MP and non-MP, having magnitude either zero or one. The values of these two signals for different modes are: (a) MPP mode: MP = 1, non-MP = 0, (b) non-MPP: MP = 0, non-MP = 1, (c) SD mode: MP = non-MP = 0, and (d) BO mode: MP = 1, non-MP = 0.

When the system operates either in BO mode or in MPP mode with $p_{mpp} < p_l$, battery has to discharge to satisfy the load demand. While discharging if the battery current becomes greater than its allowable discharge limit, I_{bmin} the system operation is changed to SD mode wherein gating pulses for all the switches are withdrawn to prevent over discharging of the battery.

When the system operates in MPP mode and $p_{mpp} > p_l$, battery is charged with the surplus power ($p_{mpp} - p_l$). In order to prevent damage of the battery due to overcharging, the charging current of the battery needs to be restricted below its maximum allowable limit, I_{bmax}. Therefore, when the reference current of the battery, i_{bref} tries to exceed I_{bmax}, the system operation is shifted to non-MPP mode by setting MP = 0 and non-MP = 1 as shown in Fig. 6*b*. In non-MPP mode battery is charged with I_{bmax} and V_{dc} is controlled by the boost converter thus bypassing the MPPT algorithm. In non-MPP mode, power extracted from PV array is $P_{pv} = (V_b * I_{bmax}) + P_l$ which is less than p_{mpp}. When the load demand changes during this mode, the PV power gets adjusted accordingly in order to maintain V_{dc} at the required value. If the load demand increases so that PV power falls short of supplying this load demand, the capacitors C and C_{dc} start discharging to meet the load demand and hence both V_c and V_{dc} start reducing. Once $(V_c + V_{dc})$ reaches minimum permissible value of 350 V, the system operation is shifted to MPP mode by setting MP = 1 and non-MP = 0. Once the system enters MPP mode, battery converter starts controlling V_{dc} (and hence V_c) whereas boost converter operates to achieve MPP operation of the PV array.

The operation in MPP and BO modes is similar except that the boost converter remains idle in BO mode whereas it is controlled to achieve MPP operation in the MPP mode.

The root mean square (RMS) and peak values of currents and voltages to be handled by the four switches of the BBIFBI for load power demand of 500 W are provided in Table 2.

4 Simulated performance

To verify the performance of the proposed scheme, detailed simulation study has been carried out on MATLAB/SIMULINK platform. Various system parameters considered for the simulation study are provided in Table 3.

The simulated steady-state response of the system while it is operating in MPP mode and is negotiating 300 W load is shown in Figs. 7*a* and *b*. The insolation level is set at 0.4 kW/m^2 ($I_{mpp} = 5.8$ A, $V_{mpp} = 35$ V, and $P_{mpp} = 200$ W). From Fig. 7*a*, it can be noted that the PV array voltage and current attain their respective MPP values confirming that the operation is in MPP mode. From Fig. 7*b*, it can be observed that the capacitor voltage, V_c is maintained at 300 V by controlling V_{dc}. Further, the ac load voltage is controlled at 230 V and is sinusoidal. The battery is discharged to meet the load demand.

The simulated performance of the system while it is being subjected to step changes in insolation level and in load demand while operating in MPP mode is shown in Figs. 7*c* and *d*. The profile of the load demand is set as follows: 300 W till 1.5 s and 400 W from 1.5 s onwards. The profile of the insolation level is

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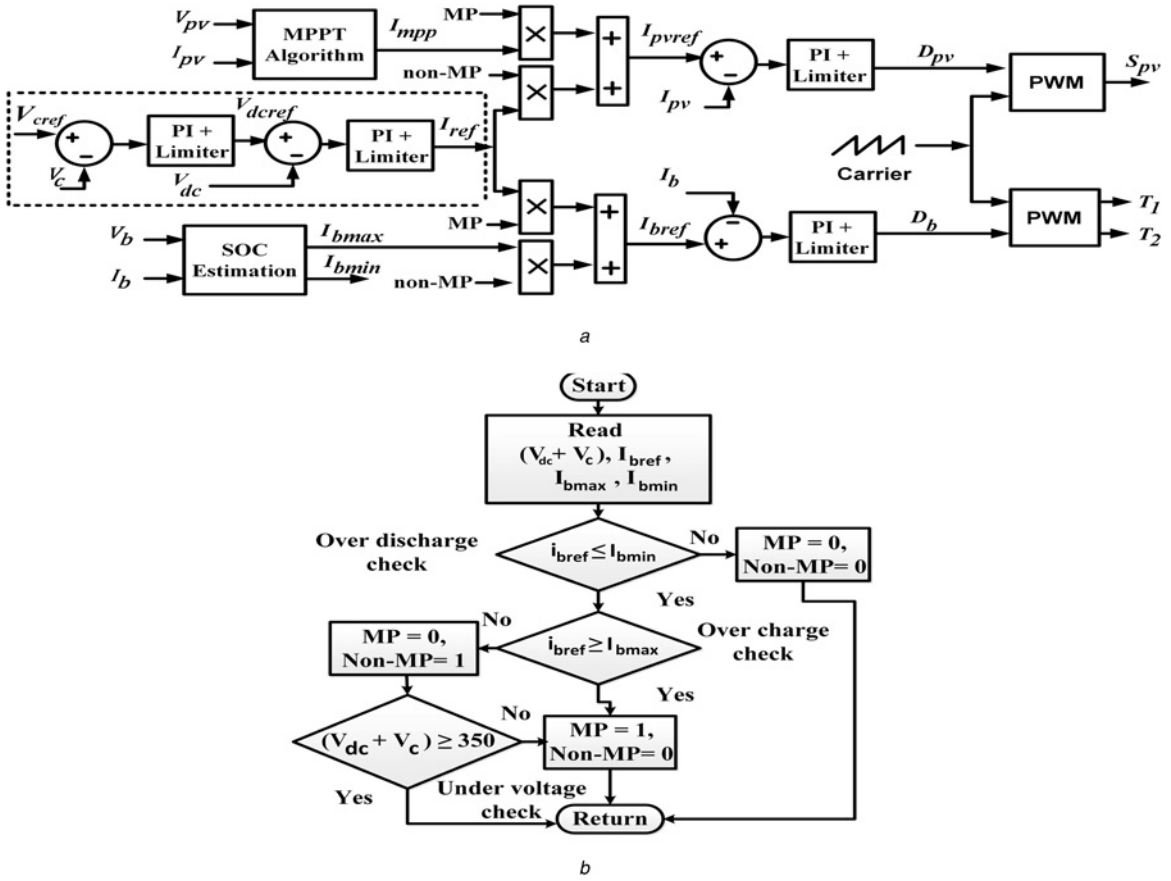

Fig. 6 *Control of boost and bidirectional dc–dc converter*

a Control strategy for the dc–dc converters of the stand-alone scheme
b Algorithm employed for generating mode selection signals MP and non-MP

Table 1 Mode selection criterion for a typical stand-alone system

Condition	Mode
i. $p_{mpp} \geq p_l$ and battery can consume ($p_{mpp} - p_l$), or ii. $p_{mpp} < p_l$ and battery can supply ($p_l - p_{mpp}$)	MPP
$p_{mpp} > p_l$ and battery cannot consume ($p_{mpp} - p_l$)	non-MPP
$p_{mpp} < p_l$ and battery cannot supply ($p_l - p_{mpp}$)	SD
$p_{mpp} = 0$ and battery can supply p_l	BO

p_{mpp} =PV power at MPP, p_l =load power demand.

Table 2 Maximum current and voltage stress of four switches of BBIFBI for load power demand of 500 W

Switches	RMS current, A	Peak current,A	Voltage stress, V
S_2 and S_3	1.6	+3.7 and −3.5	430
S_1	6	+3.8 and −24	430
S_4	12	+3.8 and −24	430

'+' indicates the current flowing through a switch whereas '−' sign indicates the current flowing through anti-parallel body diode of that switch.

set as follows: 0.4 kW/m^2 (I_{mpp} = 5.8 A, V_{mpp} = 35 V) till 2.5 s and 0.5 kW/m^2 (I_{mpp} = 7.2 A, V_{mpp} = 35.5 V) from 2.5 s onwards. From Fig. 7*c*, it can be inferred that irrespective of step changes in the insolation level and in load demand, the PV array operates at its MPP. The battery current gets adjusted to operate the system at MPP mode. From Fig. 7*d*, it can be observed that V_c is maintained at 300 V by controlling V_{dc}.

The simulated performance of the system during mode transition between MPP and non-MPP modes of operation is shown in Fig. 8.

Table 3 Parameters/elements used in simulation study

Parameter	Value
L	6 mH
C, C_{pv}	2000 μF
L_f, L_b, L_{pv}	2 mH
C_f	5 μF
switching frequency, F_s	15 kHz
C_{dc}	2700 μF
MPPT algorithm	incremental conductance
temperature of PV array	25 °C
battery voltage	36 V

The insolation level on the PV array is kept at 1 kW/m^2 (I_{mpp} = 15 A, V_{mpp} = 36.5 V, P_{mpp} = 550 W). The limit on maximum charging current for the battery, I_{bmax} is set at 5 A. Initially, the load demand is set at 500 W which is 50 W less than P_{mpp}. Hence battery is charged with about 1 A of current. At 1.8 s, the load demand is reduced by 200 W. As a result battery charging current starts increasing to consume the surplus power from the PV array. As soon as the charging current of the battery reaches 5 A (equal to set I_{bmax}), it gets restricted there to protect the battery from overcharge. At this point, the system operation gets shifted to non-MPP mode as discussed in the previous section. At 3.5 s, the load demand is increased to 500 W and the system operation gets shifted to MPP mode.

5 Experimental validation

The experimental validation of the scheme is carried out by utilising a laboratory prototype developed for the purpose. The battery bank is

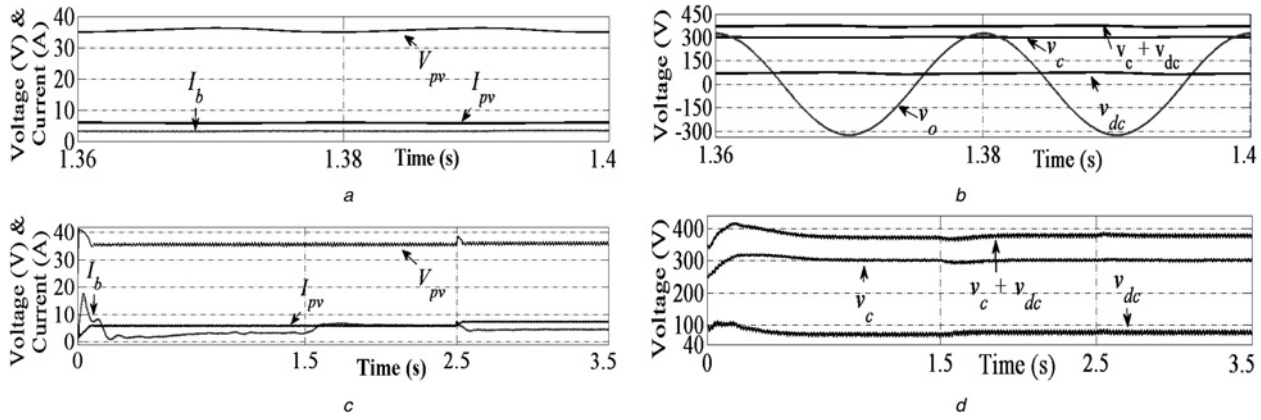

Fig. 7 *Simulated performance of the system while operating in MPPT mode*

a Steady-state response showing, v_{pv}, i_{pv}, and i_b
b Steady-state response showing, v_{dc}, v_c, $v_t = (v_{dc} + v_c)$, and v_o
c Response of the system subjected to step changes in insolation level and in load demand showing, v_{pv}, i_{pv}, and i_b
d Response of the system subjected to step changes in insolation level and in load demand showing, v_{dc}, v_c, and $v_t = (v_{dc} + v_c)$

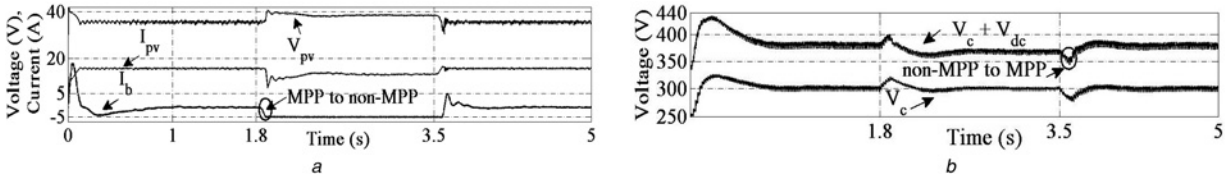

Fig. 8 *Simulated performance of the system during mode transition between MPP and non-MPP modes of operation*

a v_{pv}, i_{pv}, and i_b
b v_{dc}, v_c, and $v_t = (v_{dc} + v_c)$

formed by connecting three 12 V, 7 Ah batteries in series. Agilent make solar array simulator, E4360A is employed to emulate the solar array. This simulator generates *I–V* characteristics for the PV array based on four input command, viz. V_{mpp}, V_{oc}, I_{mpp}, and I_{sc}, wherein V_{oc} and I_{sc} are the open-circuit voltage and short-circuit current of the PV module, respectively. The ac loads at the inverter output are realised by employing incandescent bulbs of different ratings. The digital control platform required to implement the

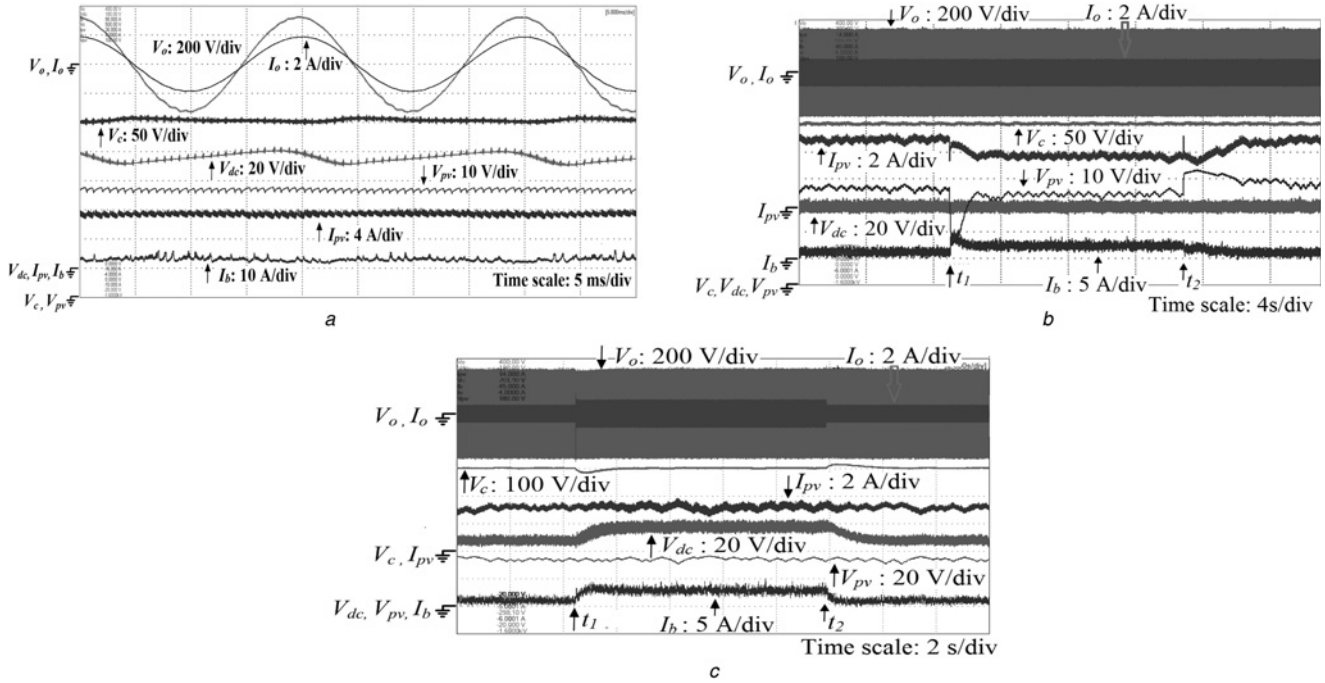

Fig. 9 *Experimental results while operating in MPPT mode*

a Steady-state response of the system
b Response of the system subjected to changes in PV operating condition
c Response of the system subjected to step changes in load demand

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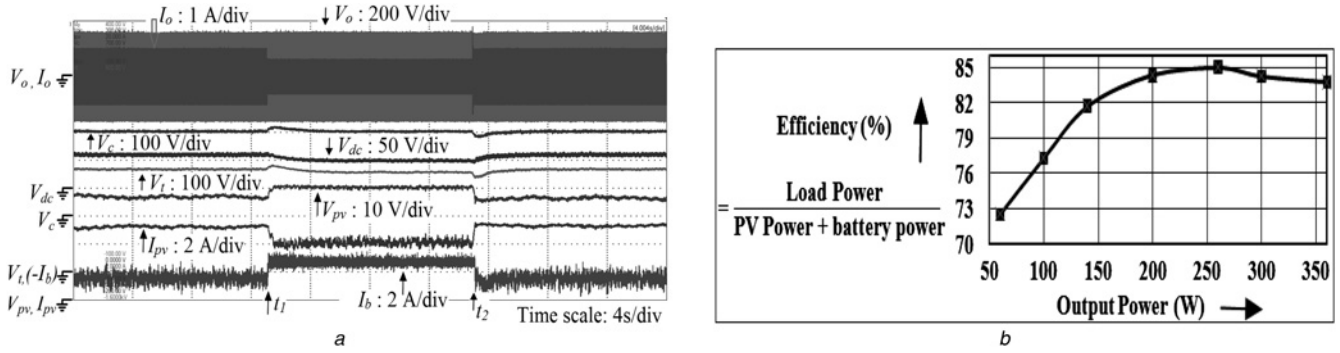

Fig. 10 *Experimental result*

a Performance of the system during mode transition between MPP and non-MPP modes
b Efficiency curve measured from the laboratory prototype

control structure of the proposed scheme is realised by employing Texas Instruments floating-point DSP, TMS320F28335. The semiconductor devices employed in the prototype are as follows: (a) switches, S_{pv}, T_1, and T_2: IRFP4668PbF (MOSFET), (b) diode, D_{pv}: DSEI60-02a, (c) diode, D: STTH6010, and (d) $S_1 - S_4$: BSM75GB120DN2 (IGBT). Other relevant parameters/elements used to realise the prototype remain the same as those used for carrying out simulation study, and are provided in Table 3.

The steady-state response of the system while operating in MPP mode and negotiating 300 W load is shown in Fig. 9*a*. The MPP values for the PV array are set at $V_{mpp} = 36$ V and $I_{mpp} = 7$ A. From Fig. 9*a*, it can be inferred that the PV voltage and current attain values which are equal to the set values at MPP. Further, the capacitor voltage V_c is maintained at 300 V as V_{dc} is being maintained at 76 V. The ac load voltage is controlled at 230 V and is sinusoidal. The battery is discharged to meet the load demand.

The response of the system subjected to changes in PV operating condition while operating in MPP mode is shown in Fig. 9*b*. The load demand is kept fixed at 160 W. The changes in PV operating condition are realised by providing step changes in the MPP values, V_{mpp} and I_{mpp} of the solar array simulator. The values of V_{mpp} and I_{mpp} are set as follows: 36 V and 5 A till the instant $t1$, 34 V and 4 A during the interval $t1$ and $t2$, and 36 V and 5 A beyond $t2$. From Fig. 9*b*, it can be observed that the system tracks new set point of the MPP satisfactorily.

The response of the system subjected to step changes in load demand while operating in MPP mode is shown in Fig. 9*c*. The MPP values for the PV array are kept fixed at $V_{mpp} = 34$ V and $I_{mpp} = 3$ A. The changes in load demand are done as follows: 100 W till instant $t1$, 160 W during the interval $t1$ and $t2$, and 100 W beyond $t2$. From Fig. 9*c*, it can be noted that the PV operating points are maintained at their respective MPP points irrespective of step changes in the load demand. The battery current gets adjusted to accommodate the load demand. The capacitor voltage, V_c is maintained at 300 V as V_{dc} is being properly adjusted.

The performance of the system during mode transition between MPP and non-MPP modes is shown in Fig. 10*a*. The maximum allowable charging current for the battery is set at 1 A. The MPP values of the PV array are set at $V_{mpp} = 35$ V and $I_{mpp} = 5$ A. Initially, the load demand is set at 160 W and the system operates in MPP mode while the battery is discharged. At instant $t1$, load demand is reduced to 100 W. As a result, surplus power from PV starts charging the battery. As soon as the charging current of the battery reaches 1 A, the system enters into non-MPP mode. This can be confirmed from Fig. 10*a* by noting that as and when the charging current of the battery gets restricted to 1 A, the PV operates at a point other than that of its MPP thereby reducing PV output power yield. At instant $t2$, the load demand is increased to 160 W and the operation of the system gets shifted to MPP mode.

The efficiency curve measured form the laboratory prototype is shown in Fig. 10*b*. The load power is measured by employing power analyser, PM100 at the load terminal. The PV power is obtained from the PV simulator display. The battery power is obtained by measuring battery voltage and current through a multimeter and an ammeter, respectively.

Table 4 Comparison of BBIFBI with typical boost inverters

Topology	V_{cmin}	n_c	n_L	control complexity	n_d
[19]	$(V_{op} + V_{dc})$	2	2	moderate	0
[20]	V_{op}	2	2	complex	1
[21]	V_{op}	1	1	moderate	2
[14]	$(V_{op} + V_{dc})$	-	2	moderate	3
BBIFBI	$(V_{op} - V_{dc})$	1	1	simple	1

V_{cmin} is the minimum voltage stress across dc capacitor, n_c is the number of dc capacitors, n_L is the number of inductors, n_d is the number of diodes, V_{op} peak value of load voltage, and V_{dc} is the input voltage to the inverter.

Table 5 Comparison of the proposed scheme with typical stand-alone schemes

Scheme	Number of stages	n_S	n_D	n_T	n_L	n_C	Peak efficiency
[7][a]	3	9	0	1	5	6	90[b]
[11][a]	3	12	12	1	3	2	91[b]
[8]	4	#	#	1	#	#	#
[9]	3	8	2	1	3	6	#
[25]	2	6	2	1	3	6	#
[12]	3	8	4	2	2	4	#
proposed	3	7	2	0	4	4	85

n_S is the number of switches, n_D is the number of diodes, n_T is the number of transformers, n_L is the number of inductors, and n_C is the number of capacitors.
[a]As no dc to ac converter is provided a full-bridge inverter is added to achieve dc–ac conversion and to maintain uniformity in comparison; and # = data inadequate.
[b]Efficiency obtained in the absence of dc–ac inverter.

A comparison of the proposed BBIFBI with typical boost type inverters is provided in Table 4. From this table, it can be concluded that BBIFBI is advantageous in most of the attributes whereas it is comparable with its counterparts in the remaining attributes. A comparison of the proposed stand-alone system with typical stand-alone systems is presented in Table 5. From this comparison, it can be inferred that as compared with the existing schemes the proposed scheme has comparable efficiency while having additional advantages like requirement of reduced number of switches and elimination in the requirement of a transformer. Hence it can be considered as a preferable candidate for solar PV-based stand-alone systems.

6 Conclusion

A solar PV-based stand-alone scheme incorporating a new boost type inverter is presented in this paper. This new boost inverter is

derived by integrating a buck–boost dc–dc converter and a full-bridge inverter. The salient features of the proposed inverter are (a) minimum requirement in the number of semiconductor devices, (b) minimum requirement for passive elements, (c) reduced voltage stress across dc-link capacitor, (d) reduced voltage gain requirement from the equivalent dc–dc buck–boost converter incorporated inside the inverter, and (e) simple control structure. The inclusion of the proposed inverter has led to the development of a three stage stand-alone scheme which requires only seven controllable switches. The scheme also allows the use of low voltage levels for the PV array and the battery thereby eliminating concerns pertaining to the use of high voltage levels for them. The control structure of the overall stand-alone scheme is presented and is validated through detailed simulation studies. The efficacy of the overall scheme is ascertained by performing exhaustive experimental validation on a laboratory prototype.

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