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High step-up converters based on quadratic boost converter for micro-inverter

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ABSTRACT

This paper proposes two DC–DC converters namely semi-tapped and fully-tapped quadratic boost converter based on the quadratic boost converter topology for high step-up applications such as micro-inverter. The proposed converters integrate the step-up capabilities of the quadratic boost converter and the tapped-inductor based converter due to which high step-up voltage gain can be achieved at lower duty ratio. Further, the proposed converters also have feature of low voltage stress on active switch. This paper presents detailed steady state analysis of proposed converters which include voltage gain and efficiency analysis with the presence of parasitic components. The theoretical analysis of proposed converters is verified by simulation and experimental results.

1. Introduction

Distributed generation systems based on non-conventional energy sources are becoming increasingly important and prevalent in power generation scenario. The non-conventional energy sources such as photovoltaic (PV) and fuel cell are low voltage energy sources; therefore, it is necessary to increase a voltage level for further processing and to make it compatible for AC load or to feed power to grid. The PV modules can be connected in series to get sufficient dc voltage, but in such cases shadow effect reduces energy generation significantly. The other way is to provide micro-inverter to each PV module [1]. The micro-inverter processes the available power in two stages as shown in Fig. 1. The first stage employs the high step-up DC–DC converter to meet the voltage demand of the second stage and also track maximum power point in order to get maximum power from the PV module. The second stage is a DC to AC inverter to meet the load demand. Sometimes the voltage requirements are such that the conventional boost converter with extremely high duty ratio has to be used in this stage. However, the use of high voltage rating switch operating at high duty ratio may result in reverse-recovery problem, which not only causes low efficiency but also creates electromagnetic interference (EMI) problem [2].

Many high step-up DC–DC converters have been proposed for interfacing the source and inverter [1–14]. In [3,4], switched capacitor technique is used for high step-up operation. Voltage-lift technique is used to obtain high step-up in [5–7]. Coupled inductor based converters also proposed for high step-up voltage gain in [9–12]. However, the leakage energy induces high voltage stress and increased switching losses and also create EMI problem. An active clamp circuit can be used to minimize these problems in coupled inductor based converters. Two cascade boost converters can achieve high step-up voltage gain but using two switches reduces the efficiency. In comparison with cascaded boost converter, quadratic boost converter is more reliable because of single driver circuit [13,14] though these topologies are structurally similar. With a quadratic voltage conversion ratio, one can get a wide conversion range. Many researchers have used tapped-inductor based boost converters for high gain operation [15–18]. The tapped-inductor boost converter faces the problem of highly pulsating input current especially when turns-ratio is higher or current is larger. However it is observed that switch voltage stress in tapped-boost converter is lower compared to the boost converter for the same output voltage. To achieve a high step-up gain, two different topologies which are combination of quadratic boost converter and tapped inductor boost converter are proposed in this paper. To the best of author's knowledge, these topologies along with its detailed performance analysis are not yet reported in the literature. Fig. 2(a) shows a tapped-inductor quadratic boost converter which can be called as semi-tapped quadratic boost converter. Fig. 3(a) is another possible combination of tapped-inductor

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Nomenclature

V_{in}	input DC voltage
V_0	output voltage
V_{C_1}	quiescent voltage of C_1 capacitor
V_{C_2}	quiescent voltage of C_2 capacitor
v_{C_1}	C_1 capacitor voltage
v_{C_2}	C_2 capacitor voltage
I_{L_1}	steady state value of L_1 inductor current
I_{L_2}	steady state value of L_2 inductor current
i_{L_1}	L_1 inductor current
i_{L_2}	L_2 inductor current
Φ_1, Φ_2	steady state value of flux through L_1, L_2
n_1	turns ratio (N_{12}/N_{11}) of tapped inductor L_1
k	coupling coefficient
D	steady state value of duty ratio
d	averaged value of duty ratio
r_{L_1}	resistance of inductor L_1
r_{L_2}	resistance of inductor L_2
D_1, D_2, D_3	diodes
n_2	turns ratio (N_{22}/N_{21}) of tapped inductor L_2
φ_1, φ_2	flux through inductor core L_1, L_2
R	load resistance
L_1	inductor 1
L_2	inductor 2
L_{11}	first part of tapped inductor L_1
L_{12}	second part of tapped inductor L_1
L_{21}	first part of tapped inductor L_2
L_{22}	second part of tapped inductor L_2
N_{11}	number of turns of L_{11}
N_{12}	number of turns of L_{12}
N_{21}	number of turns of L_{21}
N_{22}	number of turns of L_{22}
$r_{L_{11}}$	resistance of inductor L_{11}
$r_{L_{12}}$	resistance of inductor L_{12}
$r_{L_{21}}$	resistance of inductor L_{21}
$r_{L_{22}}$	resistance of inductor L_{22}
r_{C_1}	resistance of C_1 capacitor
r_{C_2}	resistance of C_2 capacitor

and quadratic boost converter which can be called as fully tapped quadratic boost converter. The detailed steady state performance analysis of semi-tapped and fully tapped quadratic boost is presented in this paper.

The organization of the paper is as follows. Section 2 provides the operation and steady state analysis of proposed converters. The voltage gain and efficiency analysis for non-ideal converters are presented in Section 3. Section 4 shows a performance comparison of both the proposed converters considering voltage gain, efficiency and voltage stress as key features. Section 5 gives the experimental results which verify analysis and simulation. Conclusions are given in Section 6.

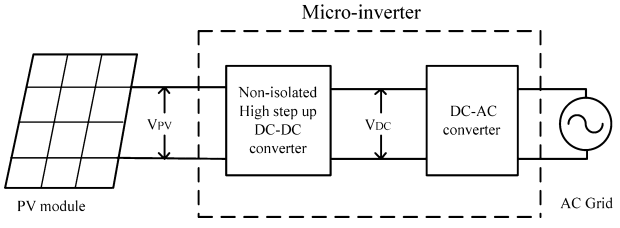

Fig. 1. Block diagram of AC module connected to grid.

2. Principle of operation and steady state analysis

To simplify the analysis the following conditions are assumed: (1) capacitors are large enough, thus the voltage across them can be considered as constant in one switching period, (2) the components of the converters are ideal, (3) the coupling coefficient is equal to one, and (4) converters are operating in Continuous Conduction Mode (CCM).

2.1. Semi-tapped quadratic boost converter

Fig. 2(a) shows the semi-tapped quadratic boost converter with untapped inductor L_1 and tapped-inductor L_2. Tapping divides inductor L_2 in two parts L_{21} and L_{22} with number of turns N_{21} and N_{22} respectively. Fig. 2(b) shows the circuit when switch S is ON. Diodes D_1 and D_3 are reverse biased and diode D_2 conducts. During switch-on period, voltage across inductor L_1 is the input voltage and voltage across inductor L_{21} is same as capacitor voltage V_{C_1}. Fig. 2(c) shows the circuit when switch S is OFF. Diode D_1 and D_3 conducts and diode D_2 gets reverse biased. In this mode inductor supplies stored energy to the load and capacitors similar to quadratic boost converter.

For the analysis, inductor current i_{L_1}, capacitor voltage v_{C_1} and v_{C_2} are chosen as state variables. For the tapped inductor, core flux φ_2 is chosen as a state variable instead of current. Though the flux is not directly measurable, current measurement can confirm the analysis. The steady state expressions for semi-tapped quadratic boost converter will now be derived.

When the switch is ON, the equivalent circuit of the converter is as shown in Fig. 2(b). The state equations for switch-ON duration can be written as:

$$L_1\dot{i}_{L_1} = V_{in}, \quad N_{21}\dot{\varphi}_2 = v_{C_1}, \quad C_1\dot{v}_{C_1} = \varphi_2\frac{N_{21}}{L_{21}}, \quad C_2\dot{v}_{C_2} = \frac{v_{C_2}}{R} \tag{1}$$

For the equivalent circuit of the converter during switch-OFF state as shown in Fig. 2(c), the state equations can be written as:

$$L_1\dot{i}_{L_1} = V_{in} - v_{C_1}, \quad (N_{21}+N_{22})\dot{\varphi}_2 = v_{C_1} - v_{C_2},$$
$$C_1\dot{v}_{C_1} = i_{L_1} - \frac{(N_{21}+N_{22})}{L_2}\varphi_2, \quad C_2\dot{v}_{C_2} = \frac{(N_{21}+N_{22})}{L_2}\varphi_2 - \frac{v_{C_2}}{R} \tag{2}$$

The steady state expressions for flux through the core of tapped-inductor L_2, inductor current I_{L_1} and capacitor voltages V_{C_1}, V_{C_2} can be derived by using averaging method [19]. The steady state expressions for semi-tapped quadratic boost converter are given as

$$\Phi_2 = \frac{I_0 L_2}{(1-D)(N_{21}+N_{22})}, \quad I_{L_2\,ON} = \frac{N_{21}\Phi_2}{L_{21}},$$
$$I_{L_2\,OFF} = \frac{(N_{21}+N_{22})\Phi_2}{L_2} \tag{3}$$

$$I_{L_1} = I_{in} = \frac{V_{in}(1+n_2D)^2}{R(1-D)^4} = \frac{V_0(1+n_2D)}{R(1-D)^2} \tag{4}$$

$$V_{C_1} = \frac{V_{in}}{(1-D)}, \quad V_0 = V_{C_2} = \frac{V_{in}(1+n_2D)}{(1-D)^2} \tag{5}$$

where n_2, turns ratio of tapped-inductor can be defined as $n_2 = N_{22}/N_{21}$ and D is duty ratio. It can be observed that output voltage is also a function of turns ratio n_2, which can substantially step up the output voltage. Also, one advantage of this converter is the continuous input current since the input inductor is not tapped.

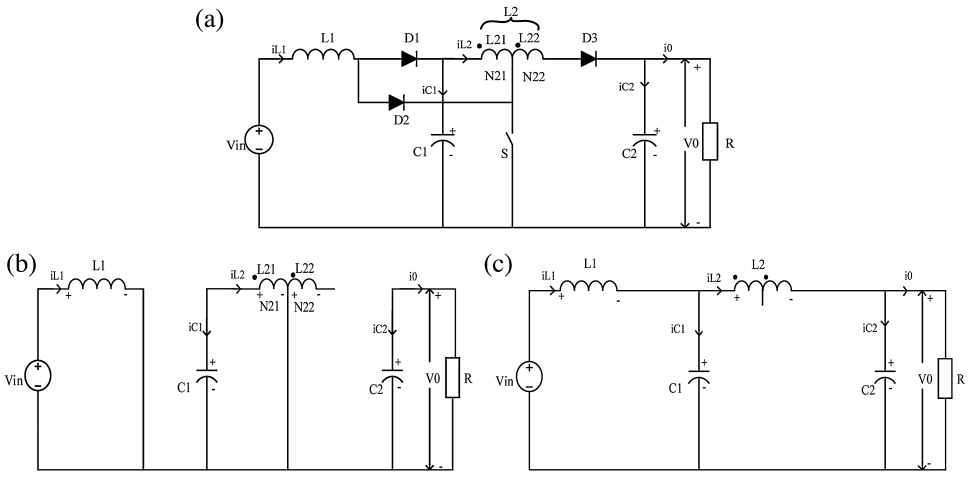

Fig. 2. (a) Semi-tapped quadratic boost converter. (b) Equivalent circuit of semi-tapped quadratic boost converter for switch-ON. (c) Equivalent circuit of semi-tapped quadratic boost converter for switch-OFF.

2.2. Fully-tapped quadratic boost converter

Fig. 3(a) shows fully tapped quadratic boost converter with both the inductor tapped. Inductor L_1 is divided into two parts L_{11} and L_{12} having number of turns N_{11} and N_{12} respectively. Similarly inductor L_2 is also in two parts L_{21} and L_{22}, and having number of turns N_{21} and N_{22} respectively. When the switch S is ON, diodes D_1 and D_3 gets reverse biased and diode D_2 conducts. During switch-ON period voltage across inductor L_{11} is equals to input voltage V_{in} and voltage across inductor L_{21} is equals to capacitor voltage V_{C_1}. Due to coupling effect voltage induced across inductors L_{12} and L_{22}. When switch S is OFF, diodes D_1 and D_3 conduct and diode D_2 gets reverse bias. In this duration, inductor stored energy supplied to load and capacitors. The steady state expressions for converter are derived as given below.

The equivalent circuit for switch-ON period of fully-tapped quadratic boost converter is as shown in Fig. 3(b), and the state equation for this duration can be written as:

$$N_{11}\dot{\varphi} = V_{in}, \quad N_{21}\dot{\varphi}_2 = v_{C_1}, \quad C_1\dot{v}_{C_1} = -\varphi_2\frac{N_{21}}{L_{21}}, \quad C_2\dot{v}_{C_2} = -\frac{v_{C_2}}{R} \tag{6}$$

For switch-OFF period equivalent circuit of the converter shown in Fig. 3(c), the state equations are as:

$$(N_{11}+N_{12})\dot{\varphi}_1 = V_{in} - v_{C_1}, \quad (N_{21}+N_{22})\dot{\varphi}_2 = v_{C_1} - v_{C_2},$$
$$C_1\dot{v}_{C_1} = \frac{\varphi_1(N_{11}+N_{12})}{L_1} - \frac{\varphi_2(N_{21}+N_{22})}{L_2},$$
$$C_2\dot{v}_{C_2} = \frac{\varphi_2(N_{21}+N_{22})}{L_2} - \frac{v_{C_2}}{R} \tag{7}$$

By using (6) and (7), the steady state expressions [19] for flux through the core of tapped-inductors L_1, L_2 and capacitor voltages V_{C_1}, V_{C_2} can be found as:

$$\Phi_1 = \frac{DI_0L_1}{DN_{11}(1+n_1)^2 + (1-D)(N_{11}+N_{12})}, \quad I_{L_1\,\mathrm{ON}} = \frac{\Phi_1 N_{11}}{L_{11}},$$
$$I_{L_2\,\mathrm{OFF}} = \frac{\Phi_1 N_1}{L_1} \tag{8}$$

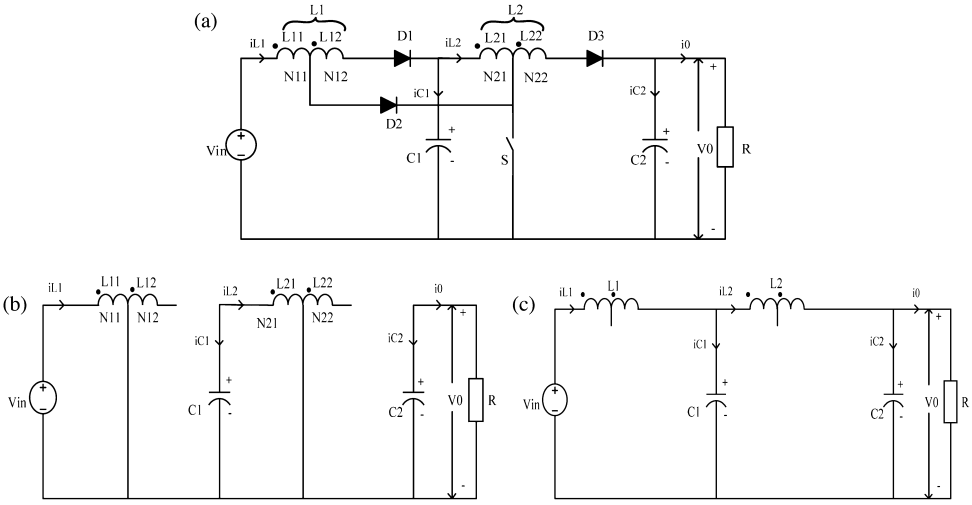

Fig. 3. (a) Fully tapped quadratic boost converter. (b) Equivalent circuit of fully-tapped quadratic boost converter for switch-ON. (c) Equivalent circuit of fully-tapped quadratic boost converter for switch-OFF.

$$\Phi_2 = \frac{DI_0L_2}{(1-D)(N_{21}+N_{22})}, \quad I_{L_2\,\mathrm{ON}} = \frac{\Phi_2 N_{21}}{L_{21}}, \quad I_{L_2\,\mathrm{OFF}} = \frac{\Phi_2 N_2}{L_2} \tag{9}$$

$$V_{C_1} = \frac{V_{\mathrm{in}}(1+n_1D)}{(1-D)}, \quad V_0 = V_{C_2} = V_{\mathrm{in}}\left\{\frac{(1+n_1D)(1+n_2D)}{(1-D)^2}\right\} \tag{10}$$

where $n_1 = N_{12}/N_{11}$ and $n_2 = N_{22}/N_{21}$ are turns ratio of tapped-inductors L_1 and L_2 respectively. This converter provides more flexibility in obtaining a high gain with the help of turns ratio. Unlike semi-tapped quadratic boost converter, the input current is of pulsating nature since input inductor is also tapped.

3. Voltage gain and efficiency of converters

In order to evaluate the performance parameters like voltage gain and efficiency, one has to consider the non-idealities of various components. Effects of non-idealities on voltage gain and efficiency is studied in this section. The performance is evaluated for semi-tapped and fully tapped quadratic boost converter. Inductors and capacitors are modeled with series resistance and the power MOSFET during ON-state is modeled as ideal switch with series resistance. Also diodes in conduction state can be modeled as forward voltage source in series with resistance. The circuit parameters of all three converters used for performance evaluation are listed in Table 1.

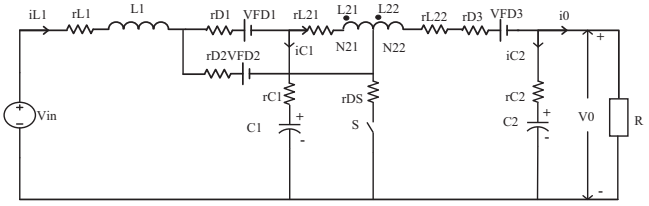

Fig. 4. Semi-tapped quadratic boost converter with parasitic parameters.

3.1. Voltage gain and efficiency for semi-tapped quadratic boost converter

Fig. 4 is the semi-tapped quadratic boost converter with non-idealities. In this figure, $r_{L_{21}}$ and $r_{L_{22}}$ are the Equivalent Series Resistance (ESR) of tapped inductor L_{21} and L_{22}. The state space averaged model of this converter is given by Eqs. (A1)–(A4). Considering the same state variables, the current through tapped inductor during switch-ON and switch-OFF duration is given by (3). In steady state, by taking LHS terms as zero for Eqs. (A1)–(A4), the voltage gain of the semi-tapped quadratic boost converter can be derived as:

$$\frac{V_0}{V_{\mathrm{in}}} = \frac{((1-D'V_{FD_1}/V_{\mathrm{in}} - DV_{FD_2}/V_{\mathrm{in}})(D'^2/L_2)((D(N_{21}+N_{22})/N_{21})+D')) + (-D'V_{FD_3}/(V_{\mathrm{in}}(N_{21}+N_{22})))(D'^3((N_{21}+N_{22})/L_2))}{X} \tag{11}$$

The current through inductor L_1 is the input current and is derived as:

$$I_{L_1} = I_{\mathrm{in}} = \frac{\begin{array}{l}(V_{\mathrm{in}} - D'V_{FD_1} - DV_{FD_2})\left\{(1/(R+r_{C_2}))((N_{21}D/L_{21}) + ((N_{21}+N_{22})D'/L_2))((D/N_{21}) + (D'/(N_{21}+N_{22})))\right\} \\ +(-D'V_{FD_3}/(N_{21}+N_{22}))\{(1/(R+r_{C_2}))((N_{21}D/L_{21}) + ((N_{21}+N_{22})D'/L_2))\}\end{array}}{X} \tag{12}$$

where X is

$$\begin{aligned} X = D'^2 &\left[\frac{-RD'^2}{(R+r_{C_2})L_2} - \frac{1}{(R+r_{C_2})}\left\{\frac{(r_{L_{21}}+r_{C_1}+r_S)D}{N_{21}} + \frac{D'r_{C_1}}{L_2} + \frac{D'(r_{L_{22}}+r_{L_{21}}+r_{D_3})}{L_2}\right\}\right] - \frac{1}{(R+r_{C_2})}\left[\left\{\left(\frac{-N_{21}D}{L_1} - \frac{(N_{21}+N_{22})D'}{L_2}\right)\left(\frac{D}{N_{21}} + \frac{D'}{N_{21}+N_{22}}\right)(-r_{L_1} - D(r_{D_2}+r_S) - D'(r_{D_1}+r_{C_1}))\right\} + \left\{\left(\frac{D'^2r_{C_1}}{N_{21}+N_{22}}\right)\left(-\frac{N_{21}D}{L_1} - \frac{(N_{21}+N_{22})D'}{L_2}\right)\right\} - \left\{\left(\frac{D'^2r_{C_1}(N_{21}+N_{22})}{L_2}\right) \times \left(\frac{D}{N_{21}} + \frac{D'}{N_{21}+N_{22}}\right)\right\}\right] \end{aligned}$$

The efficiency of the converter can be found as:

$$\eta = \frac{V_0{}^2/R}{V_{\mathrm{in}}I_{\mathrm{in}}} \tag{13}$$

Fig. 5 shows the variation of voltage gain with variation in duty ratio for different load resistances using (11). The efficiency (6) plot as shown in Fig. 6 can be derived using (11) and (12) for different loads. It can be observed that higher the value of load resistance,

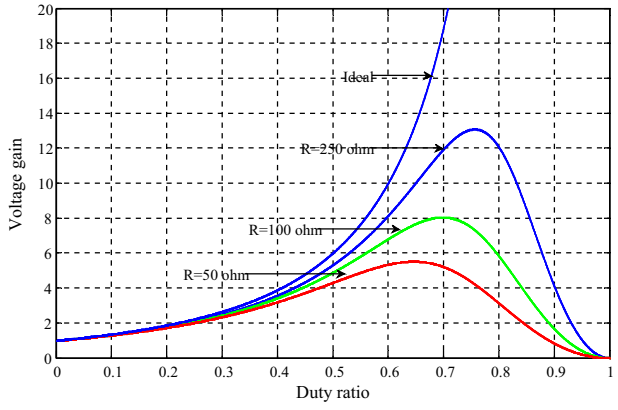

Fig. 5. Voltage gain of semi-tapped converter ($n_2 = 1$).

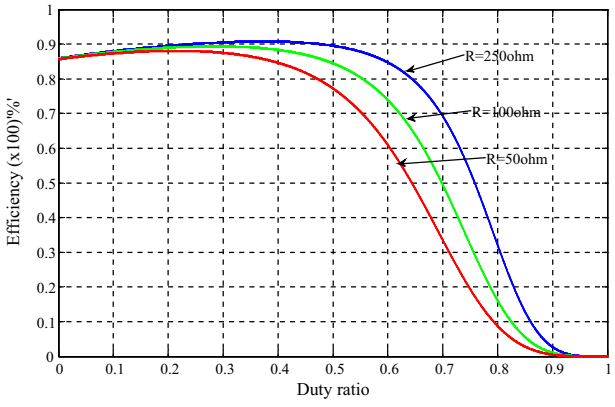

Fig. 6. Efficiency of semi-tapped converter ($n_2 = 1$).

Table 1
Parameters of converters.

S. no.	Parameters	Value
1.	Input voltage	15 V
2.	Inductor L_1, L_2	1.1 mH, 2.6 mH
3.	Inductor L_{11}, L_{12}, L_{21}, L_{22} ($n_1 = n_2 = 1$)	L_{11} = 278.9 μH, L_{12} = 284.3 μH, L_{21} = 666.8 μH, L_{22} = 673.8 μH
4.	Inductor L_{11}, L_{12}, L_{21}, L_{22} ($n_1 = n_2 = 1.5$)	L_{11} = 180 μH, L_{12} = 408.6 μH, L_{21} = 426 μH, L_{22} = 702 μH
5.	Capacitor C_1, C_2	88.6 μF, 180 μF
6.	r_{L_1}, r_{L_2}	0.114 Ω, 0.196 Ω
7.	$r_{L_{11}}$, $r_{L_{12}}$, $r_{L_{21}}$, $r_{L_{22}}$ ($n_1 = n_2 = 1$)	$r_{L_{11}} = r_{L_{12}} = 0.057\,\Omega$, $r_{L_{21}} = r_{L_{22}} = 0.098\,\Omega$
8.	$r_{L_{11}}$, $r_{L_{12}}$, $r_{L_{21}}$, $r_{L_{22}}$ ($n_1 = n_2 = 1.5$)	$r_{L_{11}} = 0.456\,\Omega$, $r_{L_{12}} = 0.0684\,\Omega$, $r_{L_{21}} = 0.0784\,\Omega$, $r_{L_{22}} = 0.1176\,\Omega$
9.	r_{C_1}, r_{C_2}	0.152 Ω, 0.076 Ω
10.	V_{FD_1}, V_{FD_2}, V_{FD_3} (maximum)	1.05 V each
11.	Load resistance R	50 Ω, 100 Ω, 250 Ω
12.	Switch resistance rDS (maximum)	0.18 Ω

one can get higher voltage gains and efficiency for lower duty ratios. This can be explained on the fact that as load resistance decreases, current increases which increases the drop in parasitic resistances. The values taken for this analysis are given in Table 1. The tapped inductor used for the semi-tapped converters is tightly coupled and the measured value of coupling coefficient 'k' is 0.9875 but for calculation it is assumed as $k = 1$.

3.2. Voltage gain and efficiency of fully tapped quadratic boost converter

Fig. 7 shows the equivalent circuit of fully-tapped quadratic boost converter with non-idealities. The averaged model of fully-tapped inductor quadratic boost converter is given by Eqs. (A5)–(A8).

The steady state voltage gain of fully-tapped inductor quadratic boost converter can be derived by solving (A5)–(A8) and can be given as:

$$\frac{V_0}{V_{in}} = \frac{\{((D/N_{11}) + (D'/(N_{11}+N_{12}))) - (D'V_{FD_1}/V_{in}(N_{11}+N_{12})) - (DV_{FD_2}/V_{in}N_{11})\}(-e\cdot h\cdot j) + (-D'V_{FD_3}/(V_{in}(N_{21}+N_{22})))(c\cdot h\cdot j)}{Y} \quad (14)$$

From (A5)–(A8), the steady state value of flux through the core of inductor L_1 is given as:

$$\Phi_1 = \frac{\{((V_{in}D/N_{11}) + (V_{in}D'/(N_{11}+N_{12}))) - (D'V_{FD_1}/(N_{11}+N_{12})) - (DV_{FD_2}/N_{11})\}(-e\cdot i\cdot m) + (-D'V_{FD_3}/(N_{21}+N_{22}))(c\cdot i\cdot m)}{Y} \quad (15)$$

where details of Y and other coefficients are given in Appendix.

The steady state value of inductor L_1 current can be derived as

$$I_{L_1} = I_{in} = \left\{\frac{DN_{11}}{L_{11}} + \frac{D'(N_{11}+N_{12})}{L_1}\right\}\Phi_1 \quad (16)$$

Fig. 8 shows the plot of variation in voltage gain with variation in duty ratio for different load resistance using (14). The plot of variation in efficiency with duty ratio is shown in Fig. 9 and it is derived by using (13), (14) and (16). It can be observed that significant voltage gain can be achieved even for lower load resistances.

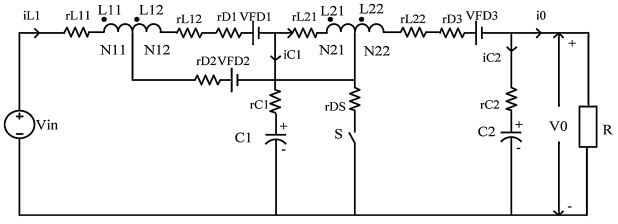

Fig. 7. Fully tapped inductor quadratic boost converter with parasitic parameters.

4. Comparison between quadratic boost, semi-tapped quadratic boost and fully-tapped quadratic boost converter

4.1. Comparison of voltage gain and efficiency

The proposed converters are derived from quadratic boost converter which has same number of elements as proposed converter and similar quadratic conversion ratio. Hence, it would be apt to compare the proposed converters with the quadratic boost converter. The steady state performance equations for quadratic boost converter are given in [14]. Similarly Eqs. (11)–(14) and (16) are used to evaluate the performance of the proposed converters. Figs. 10 and 11, show variation in efficiency and voltage gain against variation in duty ratio for converters. The load resistance and other parameters are same for comparison. At higher duty ratios, gain reduces due to higher voltage drops. The voltage gain of fully tapped inductor quadratic boost converter is highest and gain of semi-tapped inductor is higher than quadratic boost converter as shown in Fig. 11. It can be observed from Figs. 10 and 11 that for a given voltage gain, the efficiency of fully-tapped converter is higher than the other two converters.

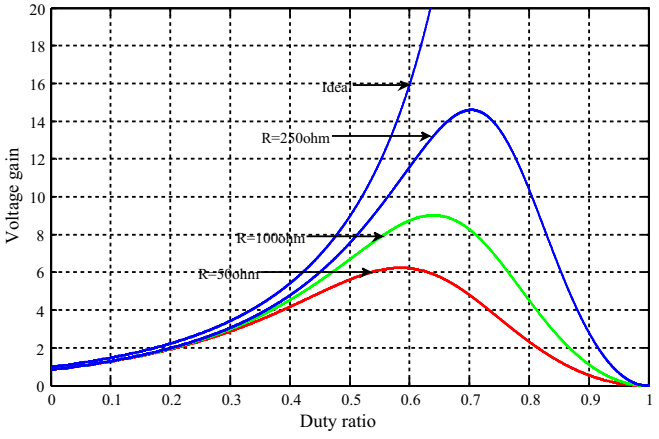

Fig. 8. Voltage gain of fully tapped converter ($n_1 = n_2 = 1$).

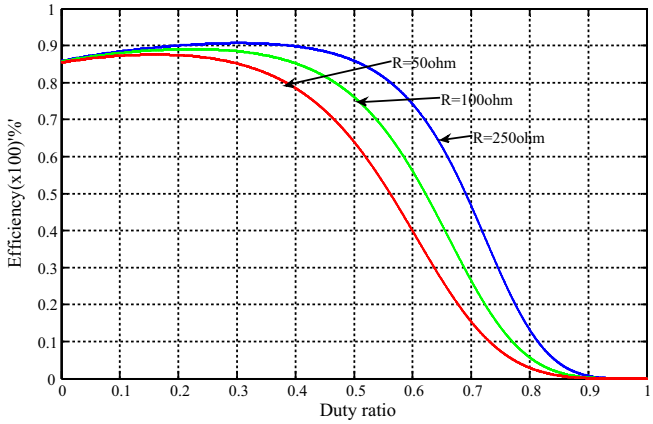

Fig. 9. Efficiency of fully tapped inductor converter ($n_1 = n_2 = 1$).

4.2. Comparison for voltage stress on active and passive switches

Comparison on the basis of voltage stress on the switch and diodes without parasitic components is given in Table 2. From Table 2 it can be concluded that stress over switch S is reduced in case of semi-tapped and fully-tapped quadratic boost converter for same output voltage in comparison to quadratic boost converter and it will reduce further as turn ratio increases for same output voltage. Similarly for diode D_2, voltage stress of semi-tapped quadratic boost converter is reduced as compared to quadratic boost converter and it is lowest in case of fully-tapped quadratic boost converter. For diode D_1 voltage stress in fully-tapped quadratic boost converter is more in comparison to the rest of two converters. The voltage stress for diode D_3 is higher in case of semi-tapped and fully-tapped quadratic boost converter.

5. Simulation and experimental results

The performance of the proposed converters in terms of voltage stress, efficiency and voltage gain is tested by using the laboratory prototypes. The experimental setup has the same specifications listed in Table 1 and TL494 is used to generate gate pulse in open loop configuration at switching frequency of 20 kHz. In a prototype circuit, MOSFET IRF640 is used as active switch and diode MUR460 is used as a passive switch. The inductor current is measured using Tektronix current probe A622. Fig. 12 shows a picture of experimental setup. Also using the same parameters listed in Table 1, the proposed converters are simulated in PLEXIM-PLECS simulation tool.

Fig. 13 (a) shows a simulation result for semi-tapped converter for $D = 0.4$ and $R = 248\ \Omega$ and turns ratio $n_2 = 1.5$. Simulation result shows switch voltage and current through tapped inductor L_2. Fig. 13(b) shows experimental results of semi-tapped quadratic boost converter's switch voltage and current through tapped inductor L_2 for the same duty ratio, resistance and turns ratio as in simulation. One can observe the pulsating current in tapped inductor L_2 from the simulation as well as experimental results.

Similarly Fig. 14 shows simulation and experimental results for fully tapped inductor converter for $D = 0.4$, $R = 248$ and $n_1 = n_2 = 1.5$. The waveform shows current of tapped inductor L_1 and switch voltage. It can be seen from Figs. 13 and 14 that simulation and experimental waveforms matches considerably. For example in Fig. 13, peak of the inductor current in both is almost equal (near 1.5 A) while switch voltage is also near 40 V in both. Further, one can

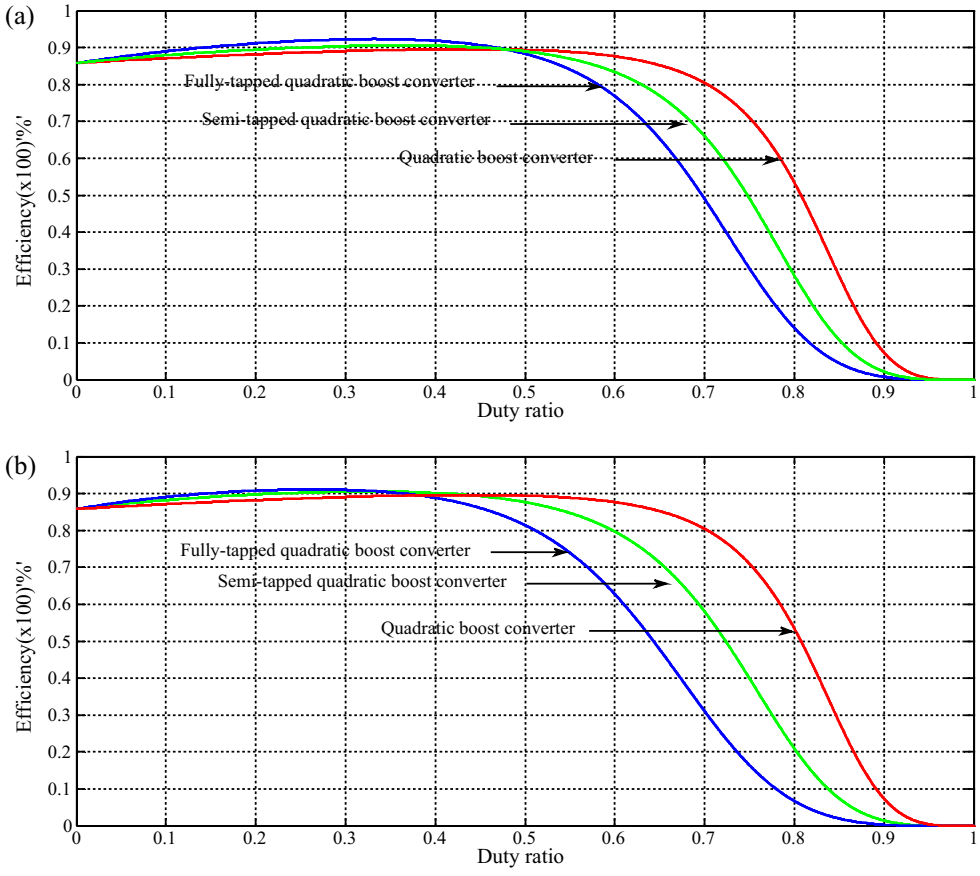

Fig. 10. (a) Comparison of efficiency for $n_1 = n_2 = 1$. (b) Comparison of efficiency for $n_1 = n_2 = 1.5$.

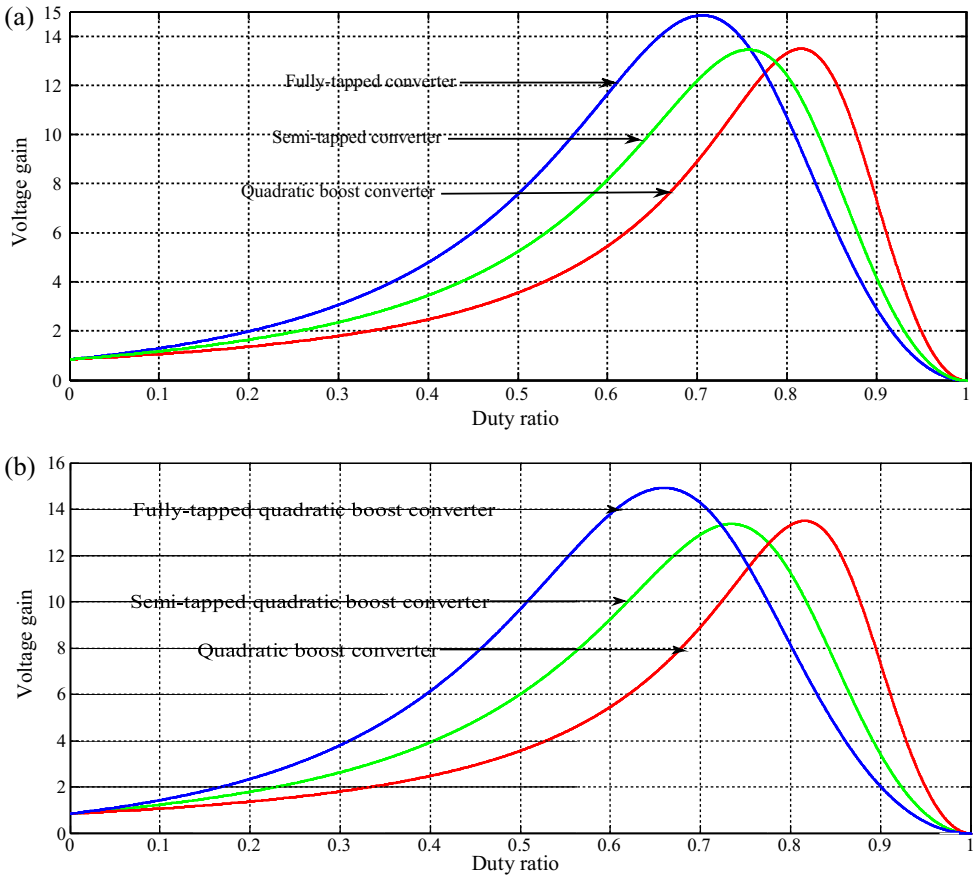

Fig. 11. (a) Comparison of voltage gain for $n_1 = n_2 = 1$. (b) Comparison of voltage gain for $n_1 = n_2 = 1.5$.

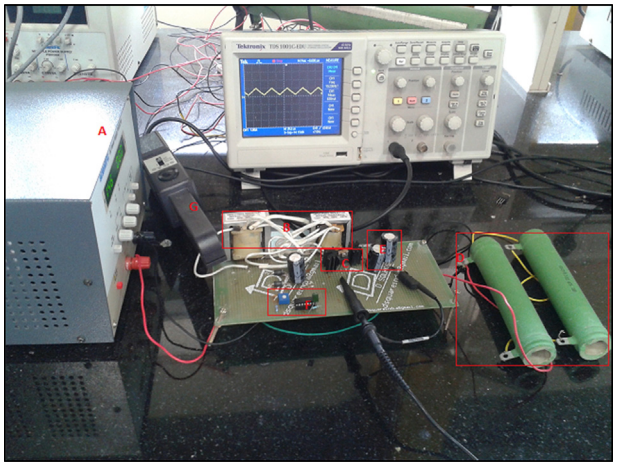

Fig. 12. Experimental setup. A: Power supply, B: tapped-inductors, C: MOSFET, D: resistive load, E: output capacitor, F: PWM circuit and G: current probe.

observe spikes in switch voltages and inductor currents in experimental waveforms. These spikes are due to the leakage inductance (imperfect coupling) which is not considered in above performance analysis and simulation results.

Fig. 15(a) and (b), shows the measured voltage gain of quadratic boost, semi-tapped quadratic boost and fully tapped quadratic boost converters, for tapped-inductor turn ratio is 1 and 1.5 respectively. Measured values of voltage gain for quadratic boost converter, semi-tapped and fully tapped converters are also listed in Tables 3–5. The inductor details are same as mentioned in above performance analysis. Fig. 15 reveals that, for same duty ratio, voltage gain of fully tapped quadratic boost converter is highest among all the three converters and by increasing turn ratio gain can be further increased. Experimental results of Fig. 15 are in good agreement with the performance analysis results of Fig. 11. Further, for fully tapped converter, Fig. 16 (a) shows the calculated and measured voltage gain plot for the turns ratio $n_1 = 1$ and $n_2 = 1.5$. Fig. 16 (b) shows voltage gain plot for $n_1 = 1.5$ and $n_2 = 1$. As stated above, fully tapped converter has pulsating input current which will increase as turns ratio increases. Therefore for fully tapped converter, input tapped inductor can be designed with less turns ratio

Table 2
Comparison of voltage stress for active and passive switches.

Component	Quadratic boost	Semi-tapped quadratic boost	Fully-tapped quadratic boost converter
Switch S	V_0	$V_0\left\{1-(Dn_2/(1+n_2D))\right\}$	$V_0\{1-(Dn_2/(1+n_2D))\}$
Diode D_1	V_{C_1}	V_{C_1}	$V_{in}(1+2n_1D)/(1-D)$
Diode D_2	$V_0 - V_{C_1}$	$V_0\{1-(n_2D/(1+n_2D))\} - V_{C_1}$	$V_0\{1-(n_2D/(1+n_2D))\} - V_{C_1} - (V_{in}Dn_1/(1-D))$
Diode D_3	V_0	$V_0\{1+(Dn/(1+nD))\}$	$V_0\{1+(n_2D/(1+n_2D))\}$

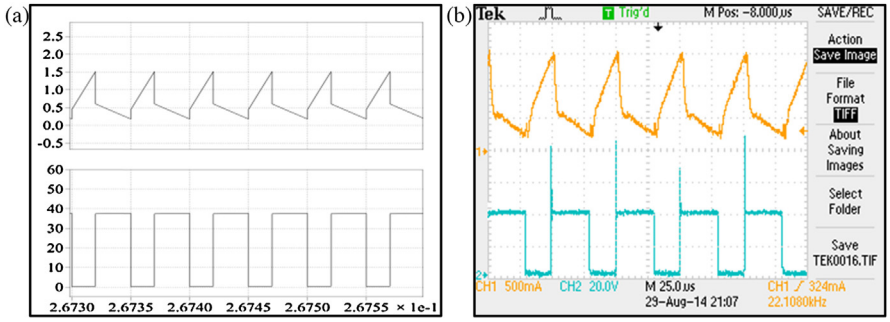

Fig. 13. (a) Simulation results of switch voltage and inductor L_2 current of semi-tapped converter for $D = 0.4$ and $n_2 = 1.5$. (b) Experimental results of switch voltage and inductor L_2 current of semi-tapped converter for $D = 0.4$ and $n_2 = 1.5$.

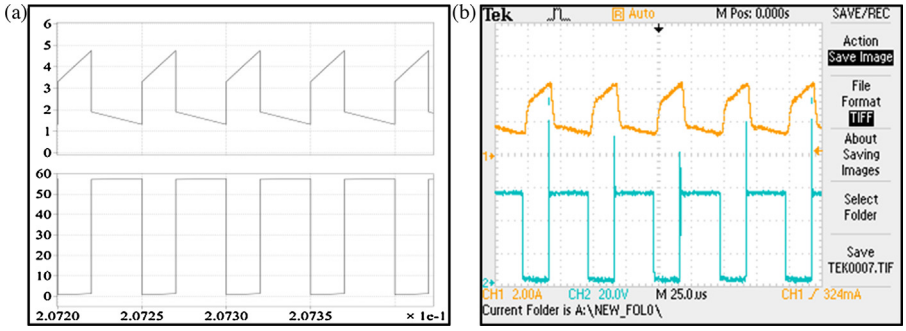

Fig. 14. (a) Simulation results of switch voltage and inductor L_1 current of fully-tapped converter for $D = 0.4$ and $n_1 = n_2 = 1.5$. (b) Experimental results of switch voltage and inductor L_1 current of fully-tapped converter for $D = 0.4$ and $n_1 = n_2 = 1.5$.

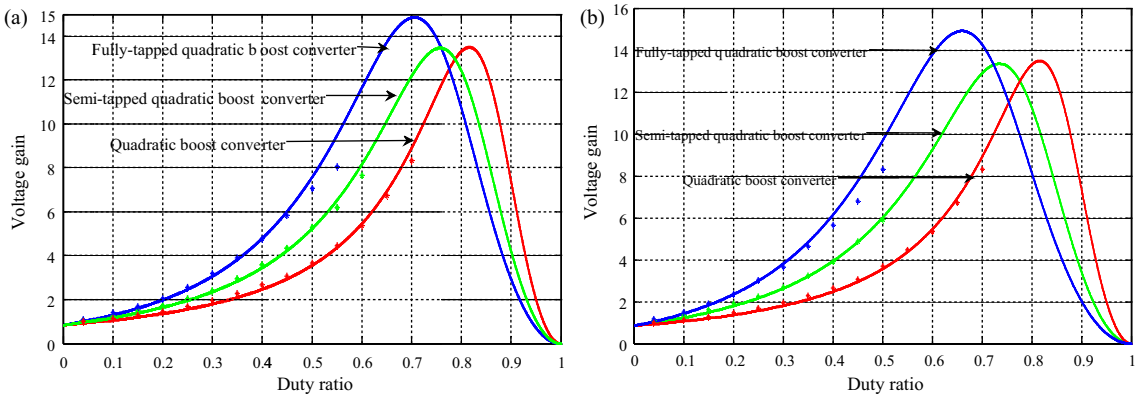

Fig. 15. (a) Measured and calculated voltage gain against duty ratio for $n_1 = n_2 = 1$. (b) Measured and calculated voltage gain against duty ratio for $n_1 = n_2 = 1.5$.

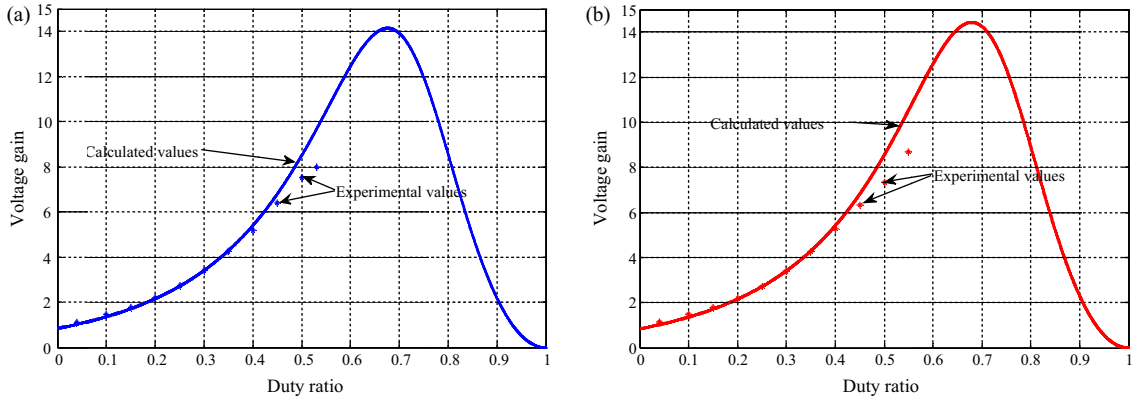

Fig. 16. (a) Measured and calculated voltage gain against duty ratio for $n_1 = 1$, $n_2 = 1.5$. (b) Measured and calculated voltage gain against duty ratio for $n_1 = 1.5$, $n_2 = 1$.

Table 3
Measured values of voltage gain for quadratic boost converter.

Duty ratio (%)	Quadratic boost measured gain
4	0.993
10	1.146
15	1.293
20	1.46
25	1.67
30	1.953
35	2.26
40	2.653
45	3.050
50	3.673
55	4.467
60	5.367
65	6.73
70	8.33

Table 4
Measured values for $n_1 = n_2 = 1$.

Duty ratio (%)	Semi-tapped measured gain	Fully-tapped measured gain
4	1.033	1.093
10	1.253	1.4
15	1.473	1.673
20	1.74	2.053
25	2.053	2.533
30	2.406	3.173
35	2.966	3.906
40	3.58	4.78
45	4.346	5.846
50	5.273	7.06
55	6.193	8.07

Table 5
Measured values for $n_1 = n_2 = 1.5$.

Duty ratio (%)	Semi-tapped measured gain	Fully-tapped measured gain
4	1.086	1.16
10	1.346	1.513
15	1.6	1.893
20	1.9	2.366
25	2.24	3.013
30	2.68	3.646
35	3.233	4.666
40	3.913	5.666
45	4.853	6.8
50	5.9	8.33

to reduce the pulsating current or one has to use input filter to avoid pulsating current which is drawn from the input source.

6. Conclusions

The semi-tapped quadratic boost converter and the fully-tapped quadratic boost converter are proposed in this paper to obtain a higher voltage gain at lower duty ratios. Performance of these converters and quadratic boost converter is analyzed under steady state conditions. The analysis shows that for same duty ratio, the voltage gain of fully-tapped quadratic boost converter is highest among the three converter followed by semi-tapped quadratic and quadratic boost converter. The voltage gain and voltage stress over the switch of semi-tapped and fully-tapped converters is a function of duty ratio and turns ratio of tapped inductor. The comparison of voltage stress on active and passive switches reveals that the voltage stress on the active switch is least in case of fully-tapped quadratic boost converter in comparison to other two converters for same output voltage. As the voltage stress over main switch reduces for both tapped-inductor based converters, thus low voltage rating and low on-state resistance switch can be used to decrease the power loss in switch. The proposed converters are simulated in PLEXIM-PLECS and the prototype of proposed converters and quadratic boost converter is implemented in the laboratory and the experimental results verify the theoretical analysis and simulation results of the converters.

Appendix A.

Semi-tapped quadratic boost

$$\dot{i}_{L_1}(t) = \frac{1}{L_1}\Big\{V_{\text{in}} - d(V_{FD_2} + i_{L_1}(r_{L_1} + r_{D_2} + r_S)) - (1-d) \times \left(V_{FD_1} + i_{L_1}(r_{L_1} + r_{D_1}) + r_{C_1}\left(i_{L_1} - \varphi_2\left(\frac{N_{21}+N_{22}}{L_2}\right)\right) + v_{C_1}\right)\Big\} \tag{A1}$$

$$\dot{\phi}_2(t) = \frac{d}{N_{21}}\left(v_{C_1} - \left(\frac{\varphi_2 N_{21}}{L_{21}}(r_{L_2} + r_{C_1} + r_S)\right)\right) + \frac{(1-d)}{N_{21}+N_{22}}\left(v_{C_1} - V_{FD_3} - \frac{\varphi_2(N_{21}+N_{22})}{L_2}(r_{L_2} + r_{D_3}) + r_{C_1}\left(i_{L_1} - \frac{\varphi_2(N_{21}+N_{22})}{L_2}\right) - v_{C_2}\frac{R}{(R+r_{C_2})}\right) \tag{A2}$$

$$\dot{v}_{C_1}(t) = \frac{1}{C_1}\left\{-d\frac{N_{21}\varphi_2}{L_{21}} + (1-d)\left(i_{L_1} - \frac{\varphi_2(N_{21}+N_{22})}{L_2}\right)\right\} \tag{A3}$$

$$\dot{v}_{C_2}(t) = \frac{1}{C_2}\left\{-\frac{v_{C_2}}{R+r_{C_2}} + (1-d)\frac{\varphi_2(N_{21}+N_{22})}{L_2}\right\} \tag{A4}$$

fully-tapped quadratic boost

$$\dot{\phi}_1(t) = \frac{d}{N_{11}}\left\{V_{\text{in}} - V_{FD_2} - \left(\frac{\varphi_1 N_{11}}{L_{11}}(r_{L_{11}} + r_{D_2} + r_S)\right)\right\} + \frac{(1-d)}{N_{11}+N_{12}}\left\{\left(V_{\text{in}} - v_{C_1} - V_{FD_1} - \frac{\varphi_1(N_{11}+N_{12})}{L_1}(r_{L_{11}} + r_{L_{12}} + r_{D_1}) - r_{C_1}\left(\frac{\varphi_1(N_{11}+N_{12})}{L_1} - \frac{\varphi_2(N_{21}+N_{22})}{L_2}\right)\right)\right\} \tag{A5}$$

$$\dot{\phi}_2(t) = \frac{d}{N_{21}}\left\{v_{C_1} - \left(\frac{\varphi_2 N_{21}}{L_{21}}(r_{L_{21}} + r_{C_1} + r_S)\right)\right\} + \frac{(1-d)}{N_{21}+N_{22}}\left\{\left(v_{C_1} - V_{FD_3} - \frac{v_{C_2}R}{(R+r_{C_2})} - \frac{\varphi_2(N_{21}+N_{22})}{L_2}(r_{L_{21}} + r_{L_{22}} + r_{D_3}) + r_{C_1}\left(\frac{\varphi_1(N_{11}+N_{12})}{L_1} - \frac{\varphi_2(N_{21}+N_{22})}{L_2}\right)\right)\right\} \tag{A6}$$

$$\dot{v}_{C_1}(t) = \frac{1}{C_1}\left\{-d\frac{N_{21}\varphi_2}{L_{21}} + (1-d)\left(\frac{\varphi_1(N_{11}+N_{12})}{L_1} - \frac{\varphi_2(N_{21}+N_{22})}{L_2}\right)\right\} \tag{A7}$$

$$\dot{v}_{C_2}(t) = \frac{1}{C_2}\left\{-\frac{v_{C_2}}{R+r_{C_2}} + (1-d)\frac{\varphi_2(N_{21}+N_{22})}{L_2}\right\} \tag{A8}$$

In Eqs. (14) and (15), $Y = b \cdot e \cdot h \cdot m - a \cdot e \cdot i \cdot m + c \cdot l \cdot i \cdot m - c \cdot f \cdot h \cdot m + c \cdot g \cdot h \cdot j$where

$$a = -\left\{ \frac{D(r_{L_{11}} + r_{D_2} + r_S)}{L_{11}} + \frac{D'(r_{L_{11}} + r_{D_1} + r_{L_{12}})}{L_1} + \frac{D' r_{C_1}}{L_1} \right\},$$

$$b = \frac{D' r_{C_1}(N_{21} + N_{22})}{L_2(N_{11} + N_{12})}$$

$$c = \frac{-D'}{(N_{11} + N_{12})} \quad e = \left\{ \frac{D}{N_{21}} + \frac{D'}{(N_{21} + N_{22})} \right\}$$

$$f = -\left\{ \frac{D(r_{L_{21}} + r_{C_1} + r_S)}{L_{21}} + \frac{D'(r_{L_{21}} + r_{D_3} + r_{L_{22}})}{L_2} + \frac{D' r_{C_1}}{L_2} \right\},$$

$$g = \frac{-RD'}{(N_{21} + N_{22})(R + r_{C_2})}$$

$$h = \frac{D'(N_{11} + N_{12})}{L_1}, \quad i = -\left\{ \frac{DN_{21}}{L_{21}} + \frac{D'(N_{21} + N_{22})}{L_2} \right\}$$

$$j = \frac{D'(N_{21} + N_{22})}{L_2}, \quad m = \frac{-1}{R + r_{C_2}}, \quad l = \frac{D' r_{C_1}(N_{11} + N_{12})}{(N_{21} + N_{22})}$$

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