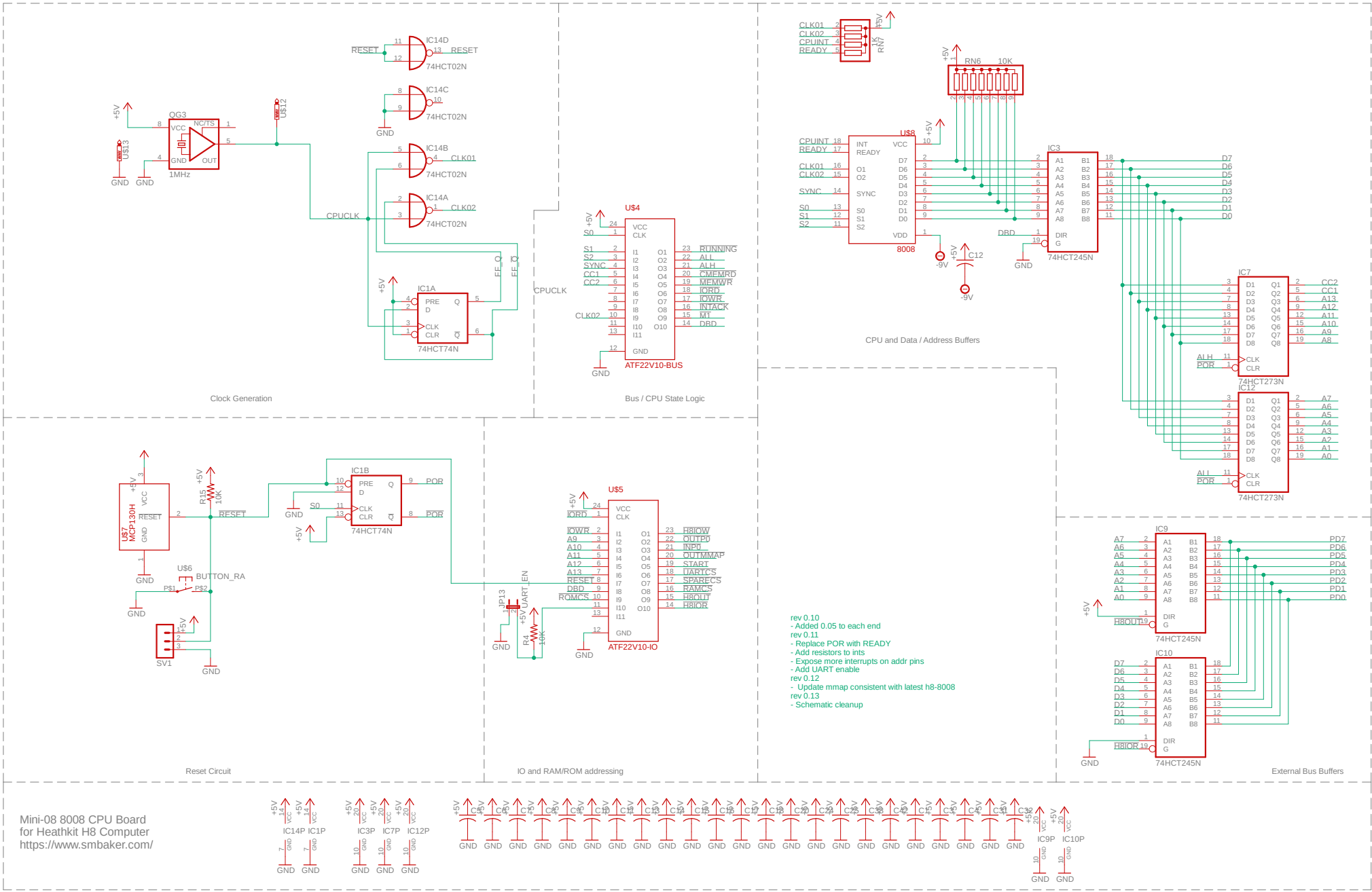
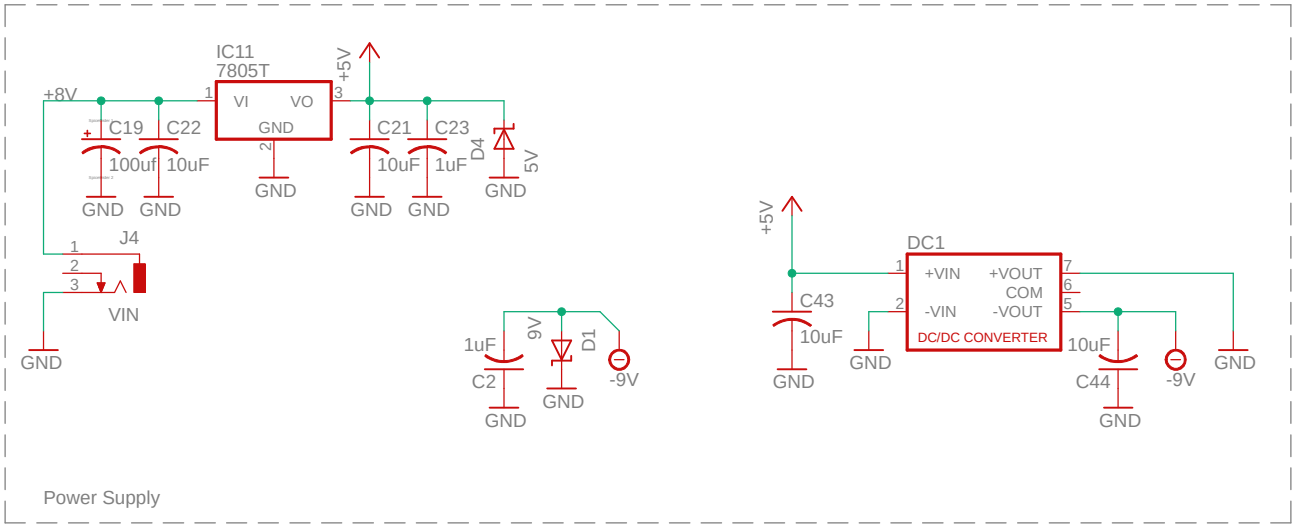
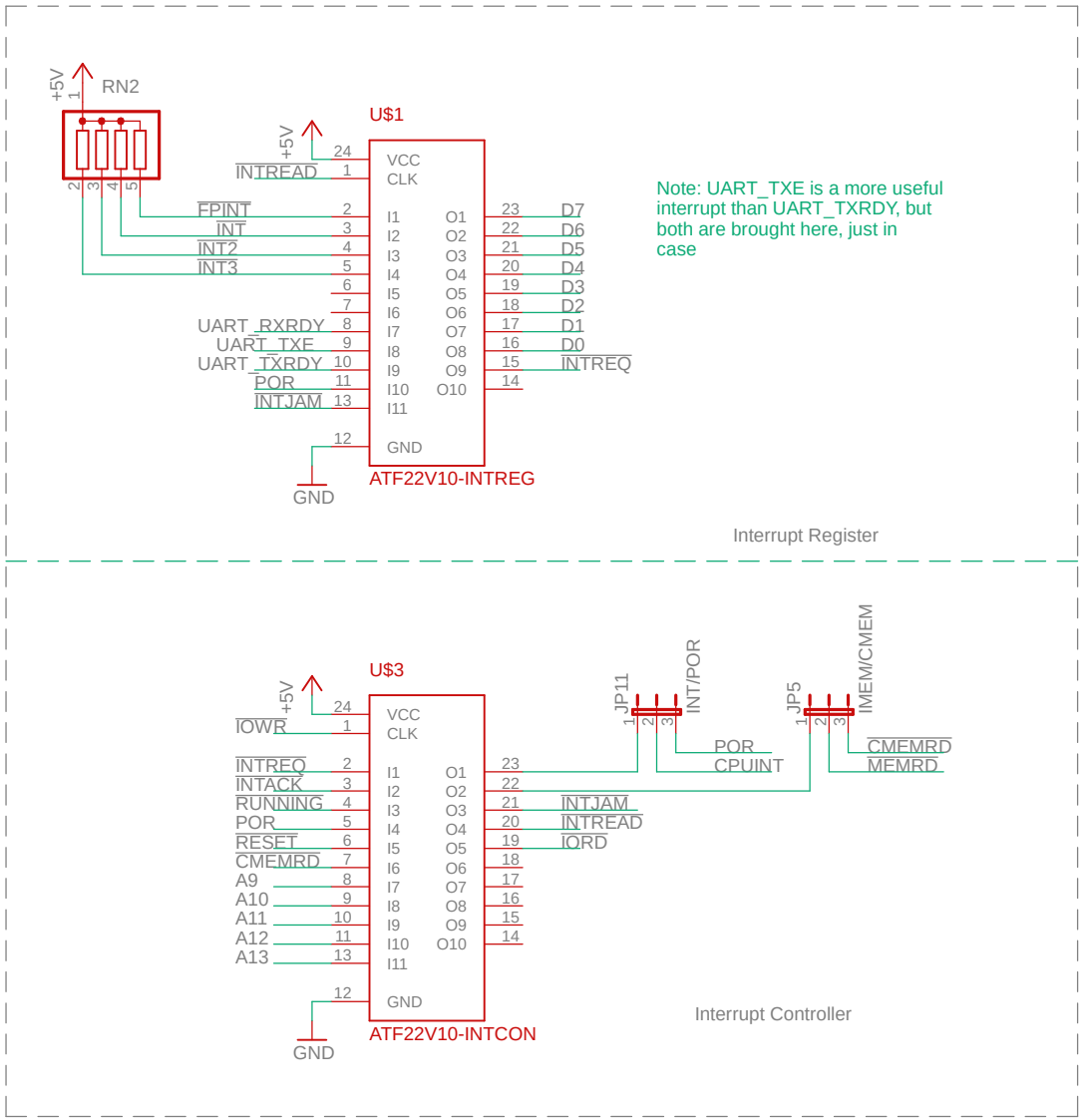
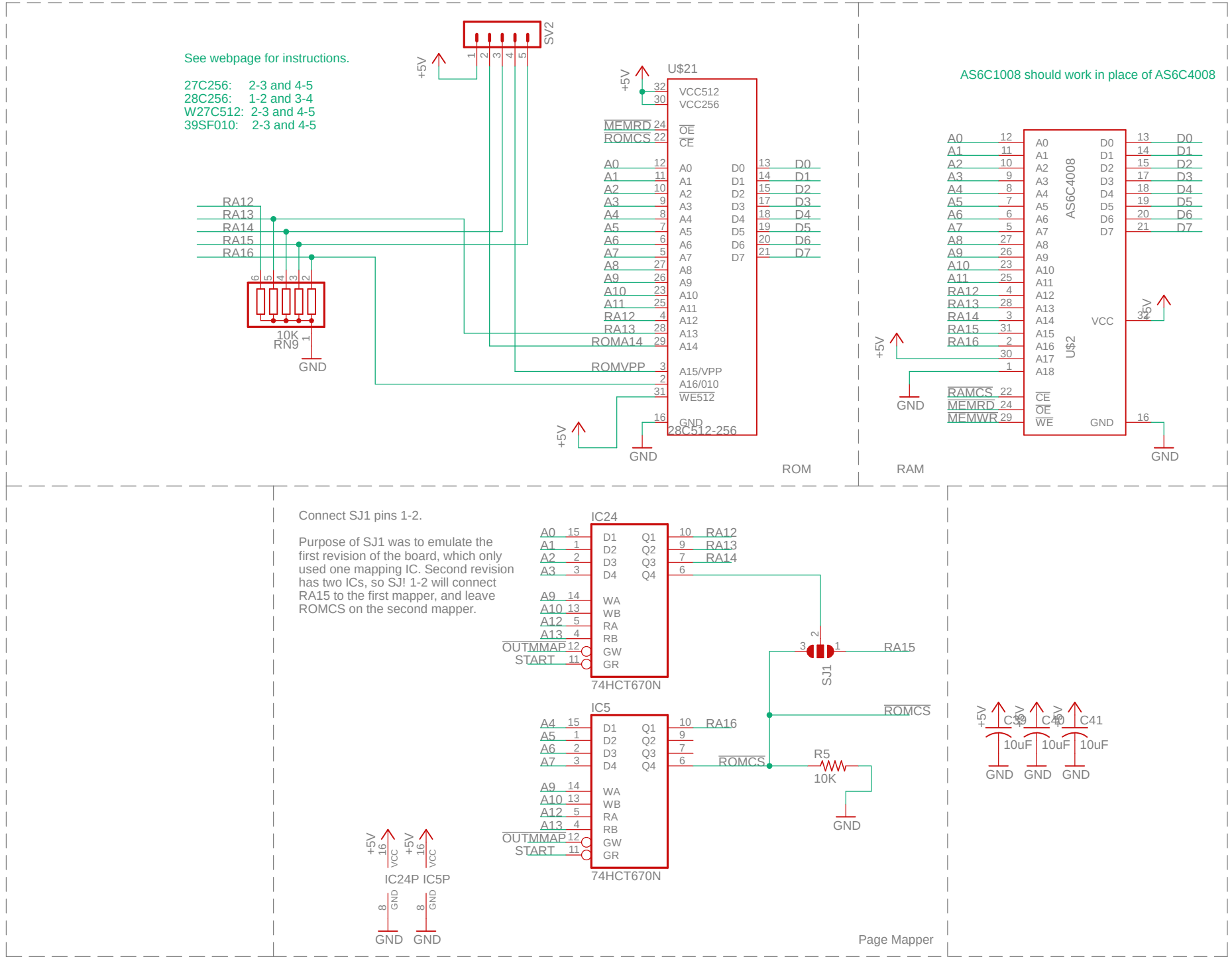
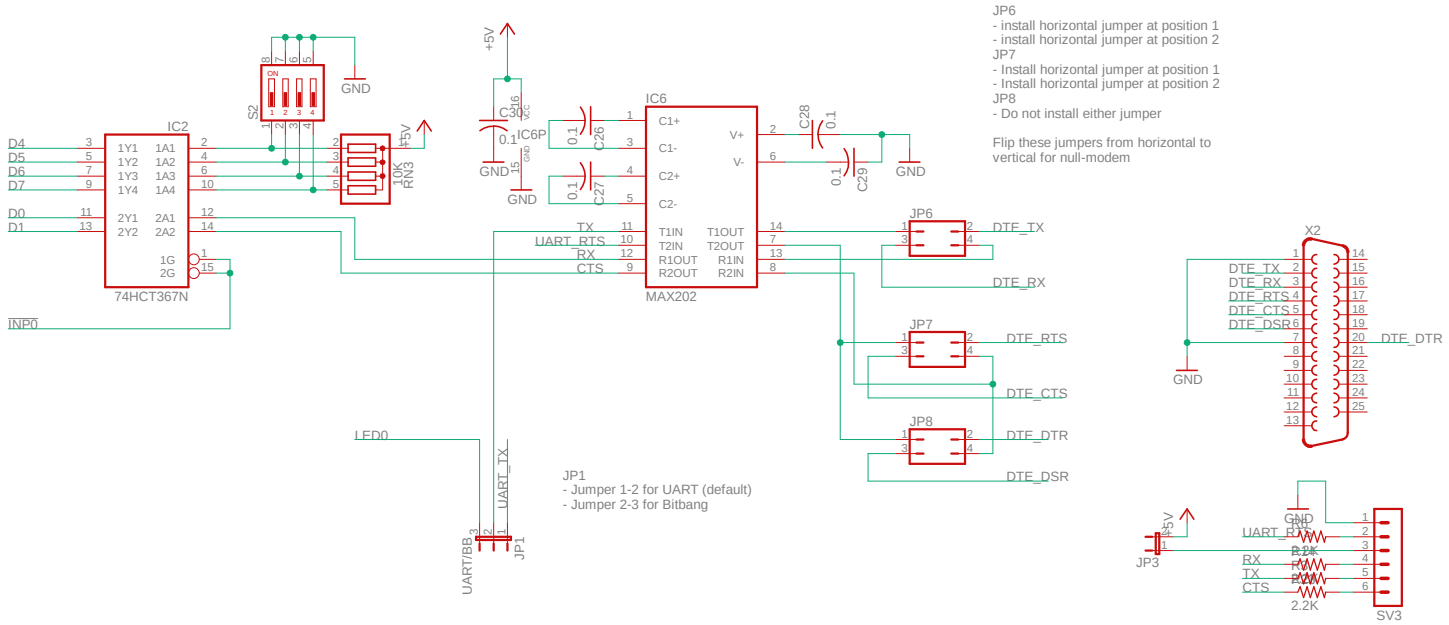
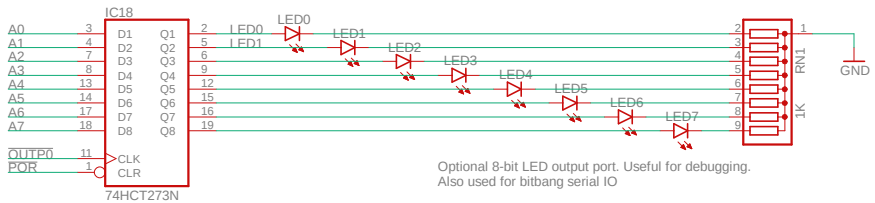

Clock Generation
Bus / CPU State Logic
CPU and Data / Address Buffers
Reset Circuit
IO and RAM/ROM addressing
External Bus Buffers
rev 0.10
- Added 0.05 to each end
rev 0.11
- Replace POR with READY
- Add resistors to ints
- Expose more interrupts on addr pins
- Add UART enable
rev 0.12
- Update mmap consistent with latest h8-8008
rev 0.13
- Schematic cleanup
Mini-08 8008 CPU Board
for Heathkit H8 Computer
https://www.smbaker.com/

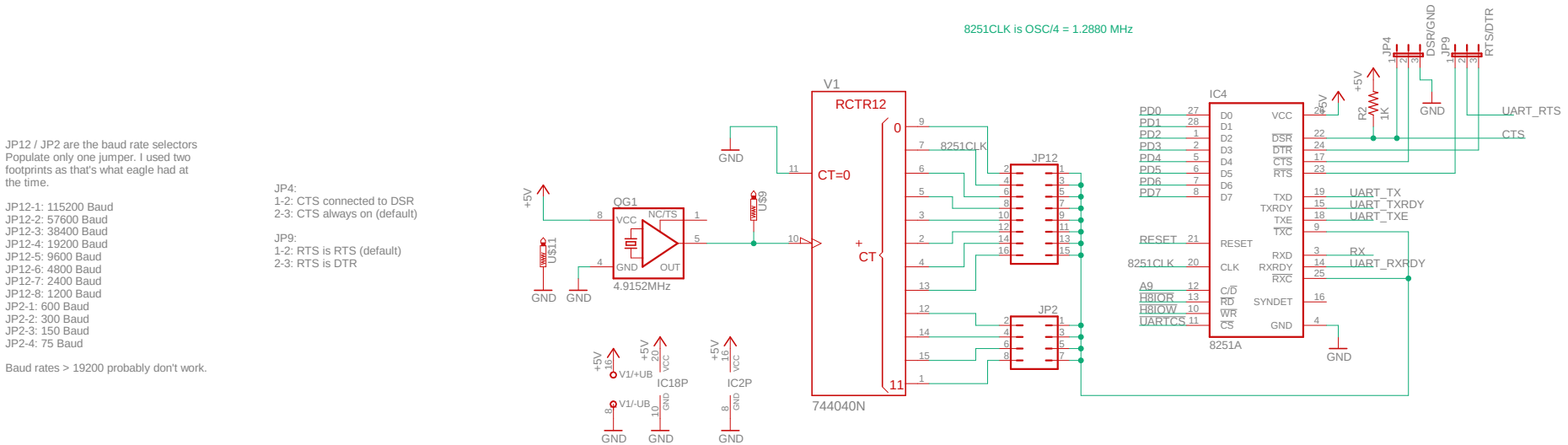

IC11
7805T
+8V
VI
VO
GND
+5V
C19
C22
C21
C23
100uf
10uF
10uF
1uF
D4
5V
GND
J4
VIN
1uF
C2
9V
D1
-9V
+5V
DC1
+VIN
+VOUT
COM
-VIN
-VOUT
DC/DC CONVERTER
C43
10uF
C44
10uF
-9V
Power Supply

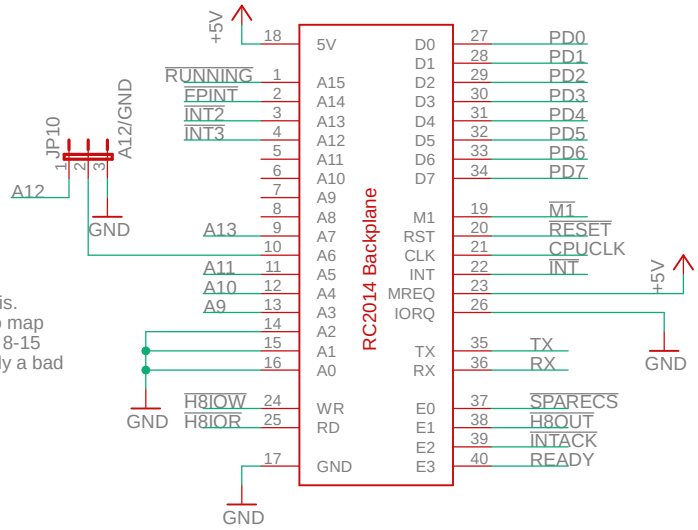

RN2
+5V
1
2
3
4
5
U$1
+5V
24
VCC
INTREAD
1
CLK
FPINT
2
INT
3
INT2
4
INT3
5
6
7
UART_RXRDY
8
UART_TXE
9
UART_TXRDY
10
POR
11
INTJAM
13
12
GND
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
O1
O2
O3
O4
O5
O6
O7
O8
O9
O10
23
22
21
20
19
18
17
16
15
14
D7
D6
D5
D4
D3
D2
D1
D0
INTREQ
GND
ATF22V10-INTREG
Note: UART_TXE is a more useful interrupt than UART_TXRDY, but both are brought here, just in case
Interrupt Register
U$3
+5V
24
VCC
IOWR
1
CLK
INTREQ
2
INTACK
3
RUNNING
4
POR
5
RESET
6
CMEMRD
7
A9
8
A10
9
A11
10
A12
11
A13
13
12
GND
ATF22V10-INTCON
JP11
1
2
3
INT/POR
POR
CPUINT
JP5
1
2
3
IMEM/CMEM
CMEMRD
MEMRD
INTJAM
INTREAD
IORD
Interrupt Controller


See webpage for instructions.
27C256: 2-3 and 4-5
28C256: 1-2 and 3-4
W27C512: 2-3 and 4-5
39SF010: 2-3 and 4-5
SV2
+5V
U$21
VCC512
VCC256
MEMRD
ROMCS
OE
CE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
RA12
RA13
ROMA14
ROMVPP
A15/VPP
A16/010
WE512
GND
28C512-256
D0
D1
D2
D3
D4
D5
D6
D7
RA12
RA13
RA14
RA15
RA16
10K
RN9
ROM
AS6C1008 should work in place of AS6C4008
AS6C4008
U$2
VCC
RAMCS
MEMRD
MEMWR
RAM
Connect SJ1 pins 1-2.
Purpose of SJ1 was to emulate the first revision of the board, which only used one mapping IC. Second revision has two ICs, so SJ! 1-2 will connect RA15 to the first mapper, and leave ROMCS on the second mapper.
IC24
74HCT670N
D1
D2
D3
D4
Q1
Q2
Q3
Q4
WA
WB
RA
RB
GW
GR
OUTMMAP
START
SJ1
IC5
ROMCS
R5
10K
IC24P
IC5P
Page Mapper
C39
C40
C41
10uF


JP6
- install horizontal jumper at position 1
- install horizontal jumper at position 2
JP7
- Install horizontal jumper at position 1
- Install horizontal jumper at position 2
JP8
- Do not install either jumper
Flip these jumpers from horizontal to vertical for null-modem
IC2
74HCT367N
IC6
MAX202
JP6
JP7
JP8
DTE_TX
DTE_RX
DTE_RTS
DTE_CTS
DTE_DTR
DTE_DSR
X2
SV3
JP3
JP1
- Jumper 1-2 for UART (default)
- Jumper 2-3 for Bitbang
"The Real Deal" DB25 RS232 connector


IC18
74HCT273N
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
RN1
Optional 8-bit LED output port. Useful for debugging.
Also used for bitbang serial IO
LED8
R1
1K


8251CLK is OSC/4 = 1.2880 MHz
JP12 / JP2 are the baud rate selectors
Populate only one jumper. I used two
footprints as that's what eagle had at
the time.
JP12-1: 115200 Baud
JP12-2: 57600 Baud
JP12-3: 38400 Baud
JP12-4: 19200 Baud
JP12-5: 9600 Baud
JP12-6: 4800 Baud
JP12-7: 2400 Baud
JP12-8: 1200 Baud
JP2-1: 600 Baud
JP2-2: 300 Baud
JP2-3: 150 Baud
JP2-4: 75 Baud
Baud rates > 19200 probably don't work.
JP4:
1-2: CTS connected to DSR
2-3: CTS always on (default)
JP9:
1-2: RTS is RTS (default)
2-3: RTS is DTR
V1
RCTR12
744040N
CT=0
CT
8251CLK
JP12
JP2
QG1
4.9152MHz
IC4
8251A
RESET
UART_RTS
CTS
UART_TX
UART_TXRDY
UART_TXE
RX
UART_RXRDY
DSR/GND
RTS/DTR



JP10:
1-2: A6 is A12 (default)
2-3: A6 is GND. I forget why I did this. Something to do with wanting to map input ports 0-8 and output ports 8-15 to the same addresses. Probably a bad idea.

External Bus Connector
Mostly RC2014 Compatible

The 8008 only has 5-bits of IO port address space, so they're mapped to the high address bits on the RC2014 bus (A3-A7). RC2014 address bits A0-A2 are always low.

MREQ is forced high. Memory never goes to this bus.

IOREQ is forced low. All Reads and Writers to this bus are IO (not memory).

Address bits A12-A15 are repurposed to hold some useful 8008 signals.