

# ECSE 421 – Embedded Systems System Design Document

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# Contents

<b>Introduction</b>	<b>3</b>
<b>1 Overview</b>	<b>4</b>
<b>2 Hardware</b>	<b>5</b>
2.1 Controller: Microchip PIC32MX695F512H . . . . .	5
2.1.1 Hardware Peripheral Support . . . . .	5
2.1.2 Programming . . . . .	7
2.2 Amplifier A – Cirrus CS4245 . . . . .	7
2.2.1 ADC . . . . .	7
2.2.2 Output . . . . .	8
2.2.3 Communications . . . . .	9
2.2.4 DSP . . . . .	9
2.2.5 Power . . . . .	9
2.3 Amplifier B – Cirrus CS4412 . . . . .	9
2.4 EEPROM – Microchip 24FC1025 . . . . .	10
2.5 LCD – Hitachi HD44780 . . . . .	10
2.6 Buttons . . . . .	11
2.7 Continuous Rotary Switch . . . . .	11
2.8 Power Regulation . . . . .	11
2.9 Circuit Board . . . . .	12
<b>3 Software</b>	<b>13</b>

# List of Figures

2.1	Schematic – Microcontroller . . . . .	6
2.2	Schematic – Analog Input Filtering . . . . .	8
2.3	Schematic – Amplifier Output Filters . . . . .	8
2.4	Schematic – CS4525 Amplifier . . . . .	9
2.5	Schematic – Cirrus CS4412 . . . . .	10
2.6	Power Regulation . . . . .	11
2.7	PCB Layout . . . . .	12

# Introduction

# Chapter 1

## Overview

## Chapter 2

# Hardware

### 2.1 Controller: Microchip PIC32MX695F512H

The core of the system is the powerful Microchip PIC32MX695F512H controller, which directly interfaces with each of the system's peripherals. This controller was chosen due to the high processing speed, low cost, and abundant peripherals. It operates at 3.3V with an instruction clock of 80MHz, referenced to an 8MHz crystal for improved stability with the extreme temperature fluctuations provided by the amplifiers. The controller is based on a MIPS32 M4K 32-bit core, featuring a 5-stage pipeline, 512kB of flash program memory (with an additional 12kB available for a bootloader), and 128kB of RAM. The chip uses a 64-pin TQFP package.

#### 2.1.1 Hardware Peripheral Support

The PIC32MX695F512H Its abundant hardware peripherals include:

- 4 I<sup>2</sup>C channels
- 3 SPI channels
- 16 channel 10-bit ADC
- 2 analog comparators
- 10/100Mbit ethernet controller
- USB 2.0 transceiver with On-The-Go (OTG) and full-speed capabilities
- 6 UART channels
- 5 16-bit timers
- 5 Output Compare modules
- 5 Input Capture modules
- Up to 53 general purpose I/Os, many of which are 5V tolerant.



- Weak pull-ups for inputs to eliminate the need for external resistors
- Generate interrupt on selectable edge
- Select complementary or open-drain to allow driving voltages higher than  $V_{DD}$

## Output Compare

The output compare modules compare the value of a timer to one or two fixed values and with output connected to an I/O pin. For our applications, this allows the ability to output a PWM signal using a timer that is continuously looping past a single comparison value.

## Input Capture

Input capture allows timer values to be captured upon external events. This is useful in a wide array of applications where pulses need to be detected and characterized. Our system uses it to take input from a PWM signal.

### 2.1.2 Programming

Microchip offers a free C compiler, MPLAB C32, for educational use. Compiled code can be loaded to the chip using the **In-Circuit Serial Programming (ICSP)** header on the board and a PICKit2, which is a small USB programming device. Programming may also be done directly over USB to the controller by incorporating Microchip's USB bootloader into our code.

## 2.2 Amplifier A – Cirrus CS4245

The Cirrus CS4245 is a 4-channel Class-D (digital) amplifier with an integrated stereo ADC and audio signal processing capabilities.

### 2.2.1 ADC

The 24-bit 48kHz SAR ADC connects to the output of the input bandpass filter. This bandpass filter eliminates higher frequency noise as well as isolating the  $V_{DD}/2$  DC bias applied internally to center the input in the ADC range. This high-frequency noise is particularly dangerous, as it can include high voltage spikes that can damage the ADC. Additionally, it is detrimental to audio fidelity to sample at above the Nyquist frequency ( $f_s/2 = 24\text{kHz}$ ), as components above that frequency will appear as if they were folded over the Nyquist frequency.



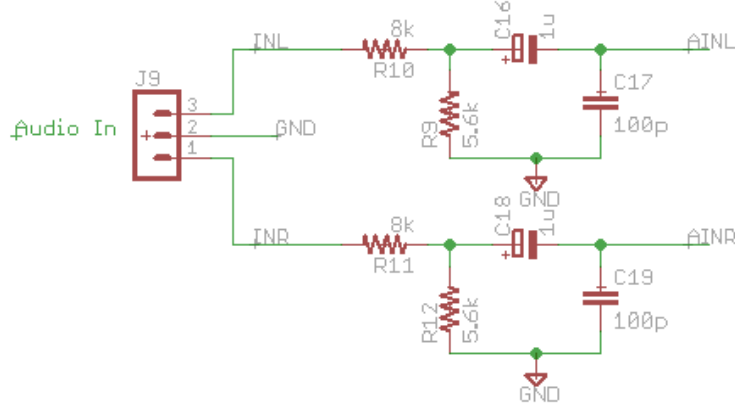


Figure 2.2: Schematic of the amplifier input filters

## 2.2.2 Output

The output of a digital amplifier is a PWM signal which must be filtered through an analog network to reproduce the input signal. The frequency of this signal is configurable on the amplifier (to reduce AM interference) and is normally in the range of 300 to 400kHz. Logic-level outputs are also provided to allow the signals to be passed to another amplifier. The CS4525 can be configured to mix a subwoofer channel as well, using one of these logic-level outputs.

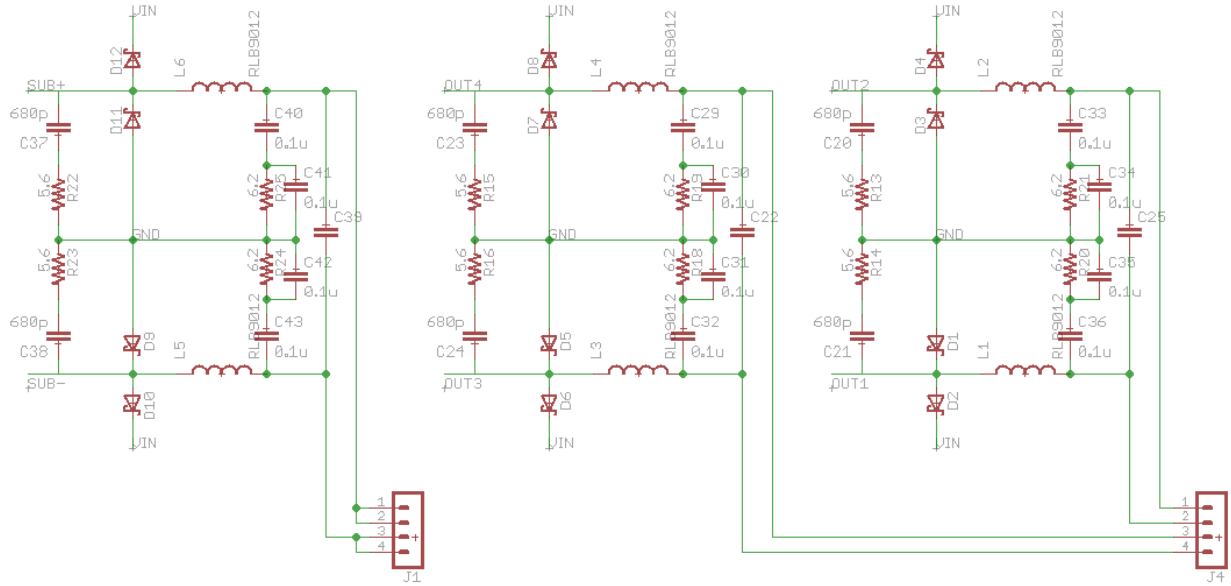


Figure 2.3: Schematic of the output filters for the subwoofer, left, and right channels

Though there are 4 single-ended outputs, we use them in a stereo **Bridge-Tied Load** (BTL, also known as *H-Bridge*) configuration which uses two single-ended outputs, one inverted from the other, for each channel. The difference between each pair is taken as the output for each channel, providing a maximum voltage swing

of  $2V_{IN}$ . For a fixed load impedance, this is an 4-fold increase in power over a single-ended configuration.

### 2.2.3 Communications

The CS4525 is controlled over I<sup>2</sup>C in addition to asynchronous interrupt (output) and reset (input) lines. The LSB of the slave address of the device is configured in hardware by tying a pin to either  $V_{CC}$  or ground. The amplifier cannot report errors solely using I<sup>2</sup>C, since it is required that the master initialize each communication. The asynchronous interrupt line is therefore used to signal to the controller that it must read the *Interrupt Status* register in order to determine the nature of the error.

### 2.2.4 DSP

### 2.2.5 Power

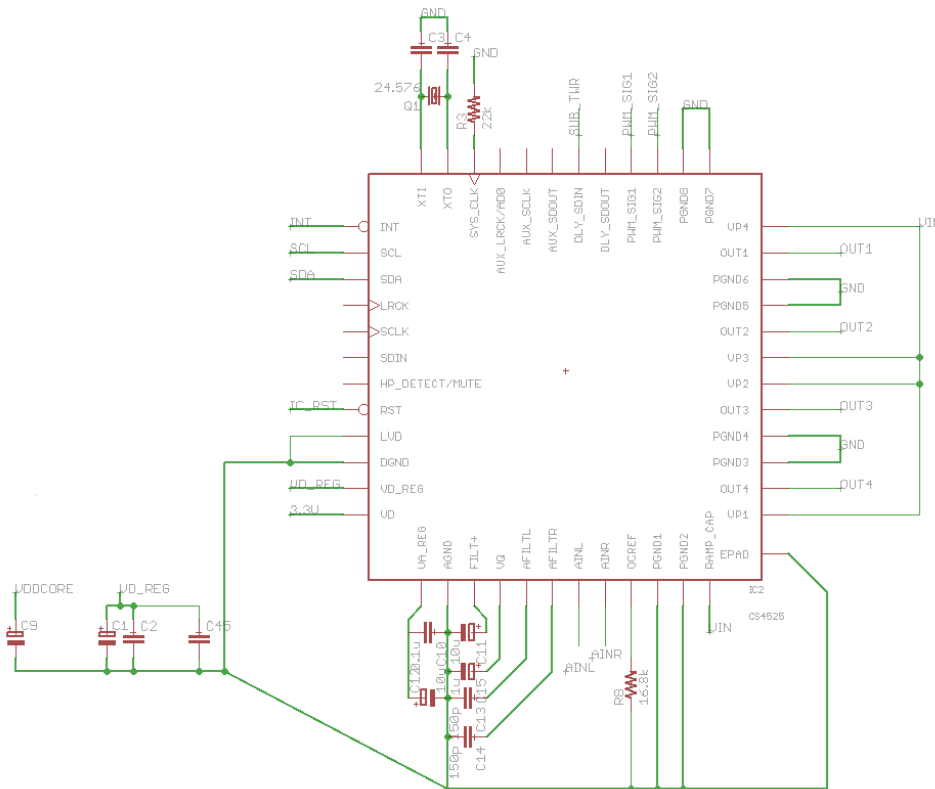


Figure 2.4: Schematic of the CS4525 and its connectivity

## 2.3 Amplifier B – Cirrus CS4412

The Cirrus CS4412 contains the same amplifier circuitry as the CS4525 but without the ADC and signal processing features. It is therefore well suited as a peripheral to the CS4525, amplifying an additional channel. It uses a remixed, processed, logic-level signal from the CS4525 for input and is connected in a mono BTL configuration to a lower impedance subwoofer. As this amplifier is not capable of any bus communications, any errors are caught by the interrupts on the PIC32. For thermal conditions that would not warrant an error but do require notification of the amplifier for the application of thermal foldback, there is an additional line to notify the CS4525 of this state.



## 2.6 Buttons

## 2.7 Continuous Rotary Switch

## 2.8 Power Regulation

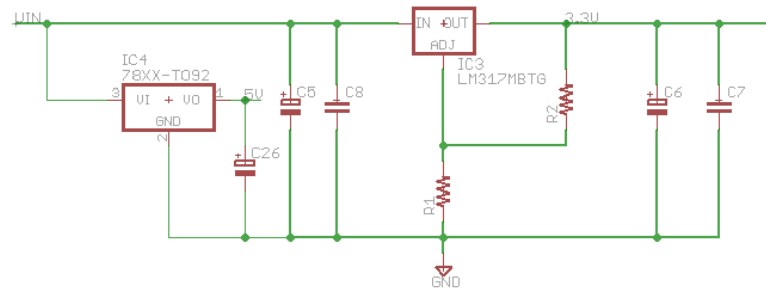


Figure 2.6: Schematic of the power regulator circuitry

## 2.9 Circuit Board

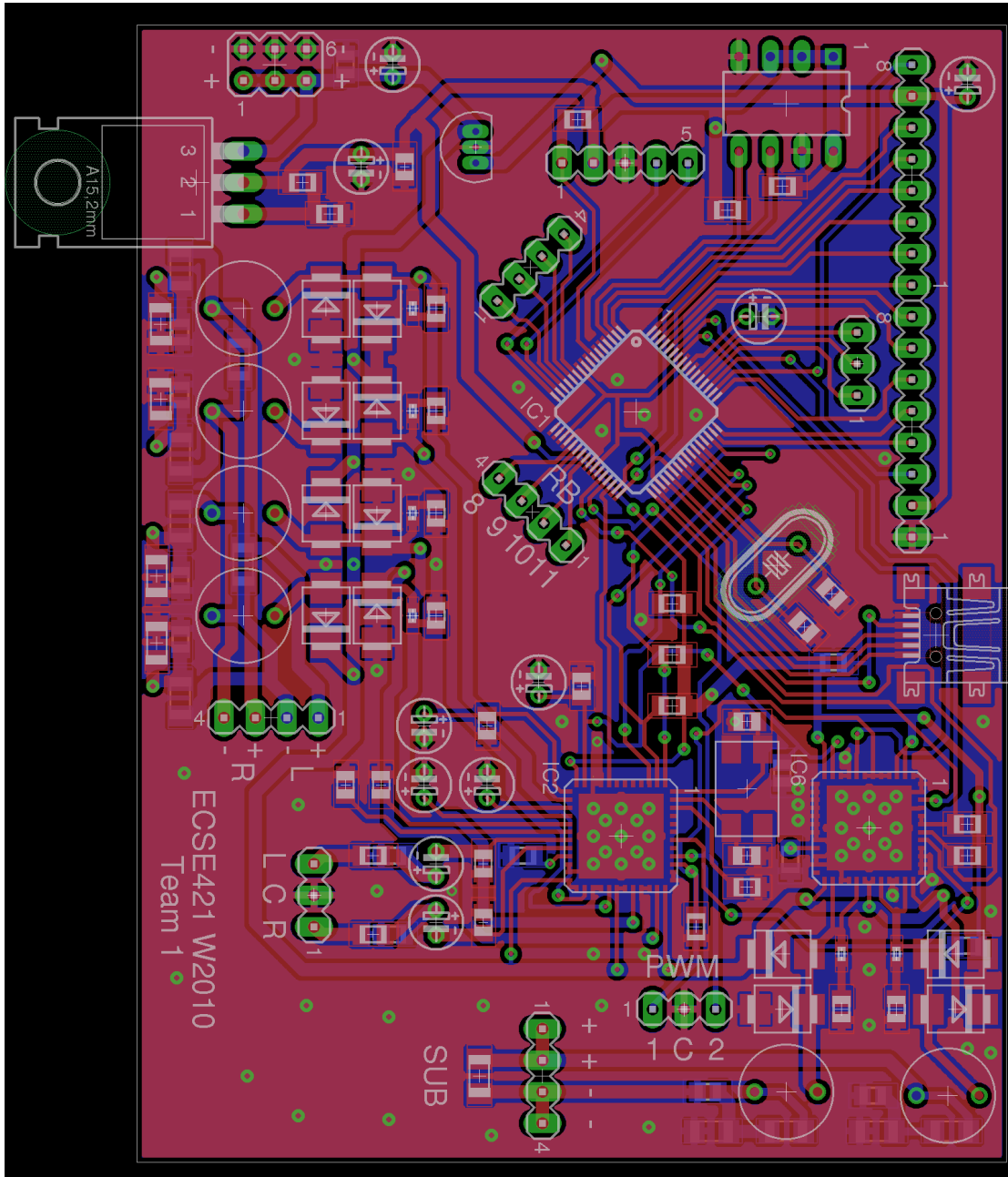


Figure 2.7: Printed circuit board layout

# Chapter 3

## Software