STM32F3 DAC

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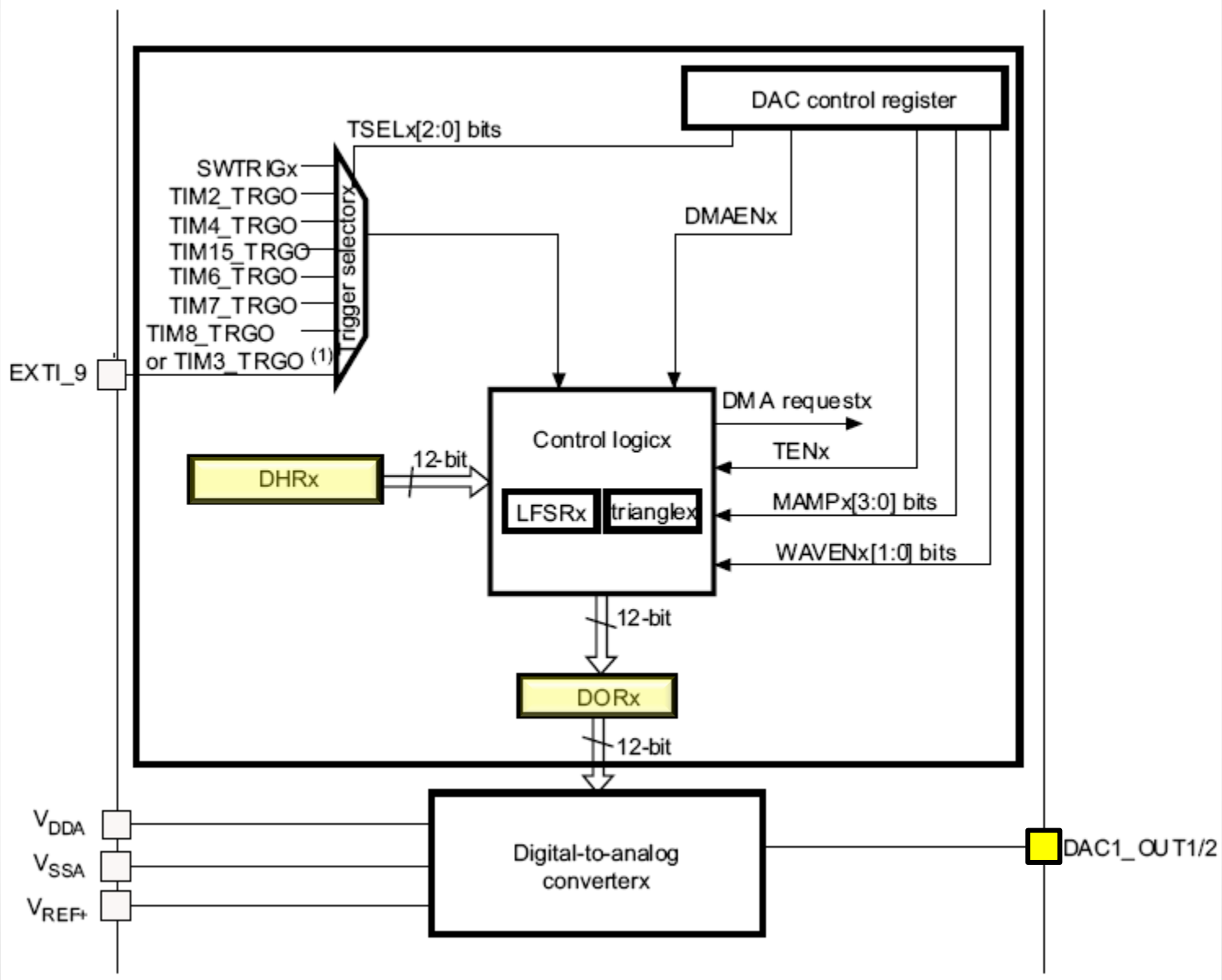
DAC1 Introduction

- The DAC module is a 12-bit, voltage output digital-to-analog converter.
- The DAC can be configured in 8- or 12-bit mode and may be used in conjunction with the DMA controller.
- In 12-bit mode, the data could be left- or right-aligned. An input reference voltage, VREF+ (shared with ADC) is available.
- The output can optionally be buffered for higher current drive.
- The devices features one DAC, DAC1, with two 12-bit channels:
  - DAC1 channel output 1, DAC1_OUT1
  - DAC1 channel output 2, DAC1_OUT2
- The two channels can be used independently or simultaneously when both channels are grouped together for synchronous update operations (dual mode).

DAC1 main features

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Independent or simultaneous conversions (dual mode only)
- DMA capability for each channel
- DMA underrun error detection
- External triggers for conversion
- Programmable internal buffer
- Input voltage reference, VREF+

Block Diagram



DAC1 pins

Name	Signal type	Remarks
V_{REF+}	Input, analog reference positive	The higher/positive reference voltage for the DAC, 1.8 V ≤ V_{REF+} ≤ V_{DDA}
V_{DDA}	Input, analog supply	Analog power supply
V_{SSA}	Input, analog supply ground	Ground for analog power supply
DAC1_OUT1/ DAC1_OUT2	Analog output signal	DAC1 channelx analog output

- Once DAC1 channelx is enabled, the corresponding GPIO pin (**PA4** or **PA5**) is automatically connected to the analog converter output (DAC1_OUTx).
- In order to avoid parasitic consumption, the PA4 or PA5 pin should first be configured to analog (AIN).

DAC registers

Off		
00	**DAC_CR**	**DAC control register**
04	DAC_SWTRIGR	DAC software trigger register
08	**DAC_DHR12R1**	**DAC channel1 12-bit right-aligned data holding register**
0C	DAC_DHR12L1	DAC channel1 12-bit left aligned data holding register
10	DAC_DHR8R1	DAC channel1 8-bit right aligned data holding register
14	**DAC_DHR12R2**	**DAC channel2 12-bit right-aligned data holding register**
18	DAC_DHR12L2	DAC channel2 12-bit left aligned data holding register
1C	DAC_DHR8R2	DAC channel2 8-bit right aligned data holding register
20	DAC_DHR12RD	Dual DAC 12-bit right-aligned data holding register
24	DAC_DHR12LD	DUAL DAC 12-bit left aligned data holding register
28	DAC_DHR8RD	DUAL DAC 8-bit right aligned data holding register
2C	DAC_DOR1	DAC channel1 data output register
30	DAC_DOR2	DAC channel2 data output register
34	DAC_SR	DAC status register

DAC Registers

Address offset	Register name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	DAC_CR	Res.	Res.	DMAUDRIE2	DMA EN2	MAMP2[3:0]				WAVE2[1:0]		TSEL2[1:0]		TSEL20	TEN2	BOFF2	EN2	Res.	Res.	DMAUDRIE1	DMAEN1	MAMP1[3:0]				WAVE[1:0]1		TSEL1[2:0]			TEN1	BOFF1	EN1
	Reset value			0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	DAC_ SWTRIGR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	SWTRIG2	SWTRIG1
	Reset value																														0	0
0x08	DAC_DHR12R1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC1DHR[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x0C	DAC_DHR12L1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC1DHR[11:0]												Res.	Res.	Res.	Res.
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0				
0x10	DAC_DHR8R1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC1DHR[7:0]							
	Reset value																									0	0	0	0	0	0	0	0
0x14	DAC_DHR12R2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC2DHR[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x18	DAC_DHR12L2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC2DHR[11:0]												Res.	Res.	Res.	Res.
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0				
0x1C	DAC_DHR8R2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC2DHR[7:0]							
	Reset value																									0	0	0	0	0	0	0	0
0x20	DAC_DHR12RD	Res.	Res.	Res.	Res.	DACC2DHR[11:0]												Res.	Res.	Res.	Res.	DACC1DHR[11:0]											
	Reset value					0	0	0	0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0	0	0	0
0x24	DAC_DHR12LD	DACC2DHR[11:0]												Res.	Res.	Res.	Res.	DACC1DHR[11:0]												Res.	Res.	Res.	Res.
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0	0	0	0				
0x28	DAC_DHR8RD	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC2DHR[7:0]				DACC1DHR[7:0]											
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x2C	DAC_DOR1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC1DOR[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x30	DAC_DOR2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DACC2DOR[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x34	DAC_SR	Res.	Res.	DMAUDR2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DMAUDR1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
	Reset value			0																0													

DAC Control Register: main bits

Name	Description	Operation
WAVEx[1:0]	DAC channelx noise/triangle wave generation enable	00: Wave generation disabled 01: Noise wave generation enabled 1x: Triangle wave generation enabled
BOFFx	DAC channelx output buffer disable	0: DAC channelx output buffer enabled 1: DAC channel1 output buffer disabled
ENx	DAC channel1 enable	0: DAC channel1 disabled 1: DAC channel1 enabled

DAC conversion

- The DAC channelx data output register (DAC_DORx) cannot be written directly.
- Any data transfer to the DAC channelx must be performed by loading the DAC_DHRx register (write to DAC_DHR8Rx, DAC_DHR12Lx, DAC_DHR12Rx).
- Data stored in the DAC_DHRx register are automatically transferred to the DAC_DORx register after one APB1 clock cycle, if no hardware trigger is selected (TENx bit in DAC_CR register is reset).

DAC output voltage

- Digital inputs are converted to output voltages on a linear conversion between 0 and VDDA.
- The analog output voltages on each DAC channel pin are determined by the following equation:

$$DAC\ output = \mathrm{V_{DD}}\ \frac{\mathrm{DOR}}{4095}$$