

Where to get Firmware, and how to reverse engineering it.

Travis Goodspeed, Dartmouth College, 2022.01.23

What is Firmware?

- Many formats:
 - .BIN -- Flat binary image, lacking a loading address.
 - .DFU -- USB Device Firmware Update
 - .ELF -- Contains everything you'd want. Rather rare.
 - .EXE -- Custom updaters for Windows. Gotta reverse engineer it first!
 - .??? -- Custom file format, lots of variety.

Where to get firmware?

- Download an updater from the manufacturer's website.
- Read the code out of a physical device:
 - Memory chip reader, JTAG.
 - Memory corruption exploit, voltage glitching.
 - Microscopes. (Not joking.)

Firmware Updates



The image shows the XIEGU X6100 HF/50MHz Transceiver. The radio is black with a large digital display showing '01.808.000' and '07.050.000'. It has various buttons and knobs, and a microphone is attached to the top. The model name 'X6100 HF/50MHz TRANSCEIVER' is printed on the front.

XIEGU
ALL MODE PORTABLE SDR TRANSCEIVER

Built-in Battery / ATU / Mic / SWR Scanner
Voice Call | Preset Message
Digital Noise Reduction | Data Modem | IQ Signal Output

Icons for WiFi, Bluetooth, USB, and other connectivity options.

2022.01.17 Upgrade Log | [CLICK HERE](#) to download.

APP : V1.1.2 Jan 17 2022,16:31:45

BASE : V1.1.2 Jan 17 2022,15:44:18

Note: This upgrade is important. Please read the following details carefully.

Firmware Updates

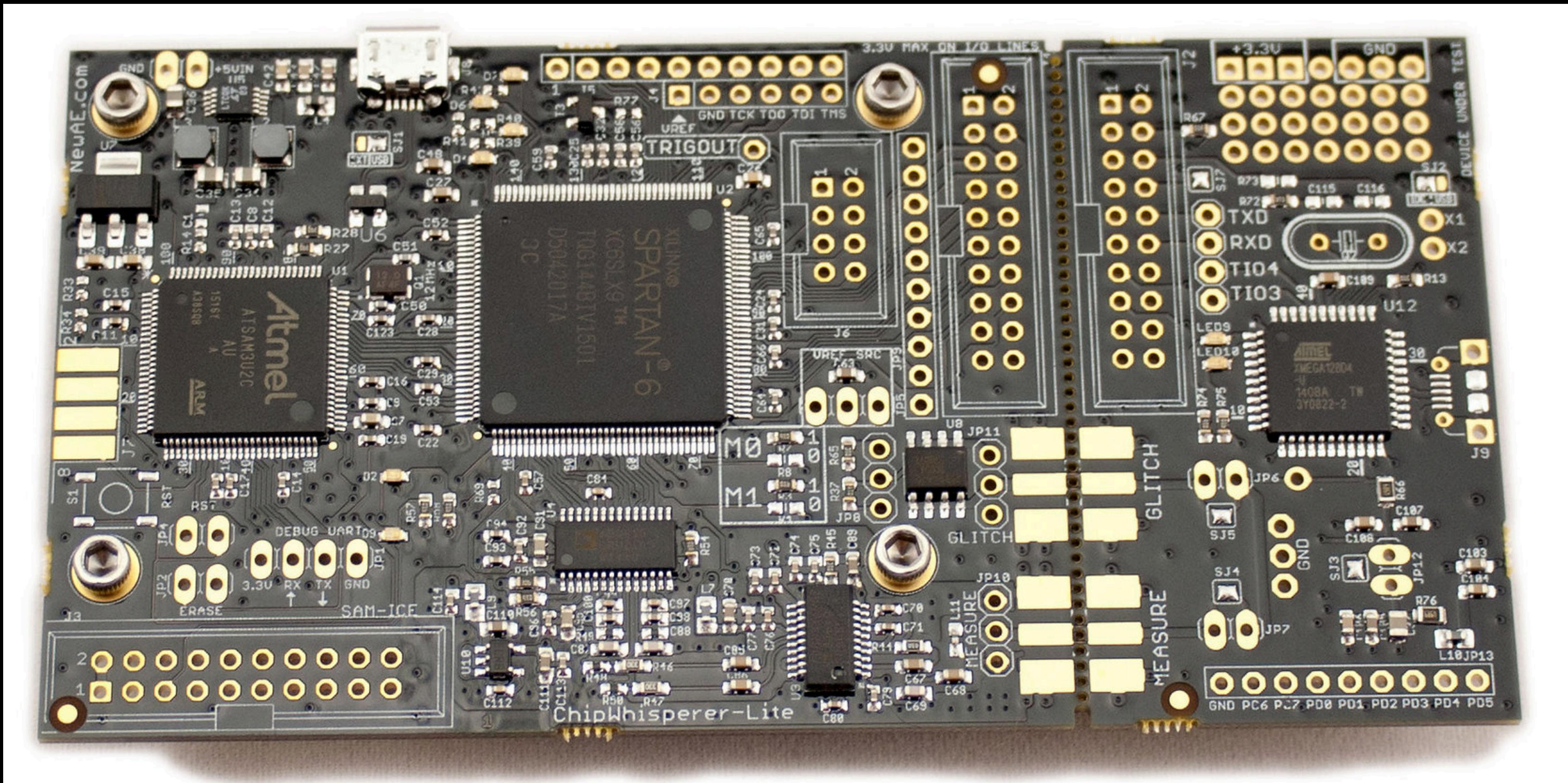
- Often encrypted:
 - Tytera MD380 radio uses XOR with a random block.
 - How can we crack that?
- Often wrapped:
 - USB Device Firmware Update protocol in a Windows .EXE.
 - You'll reverse engineer the wrapper first, to get the firmware.

Memory Chip Readers / JTAG

- Unique to reach memory type:
 - Parallel ROM, SPI Flash
 - Compact Flash, Secure Digital
- JTAG
 - Testing protocol for manufacturing.
 - Also does debugging.
 - Sometimes disabled

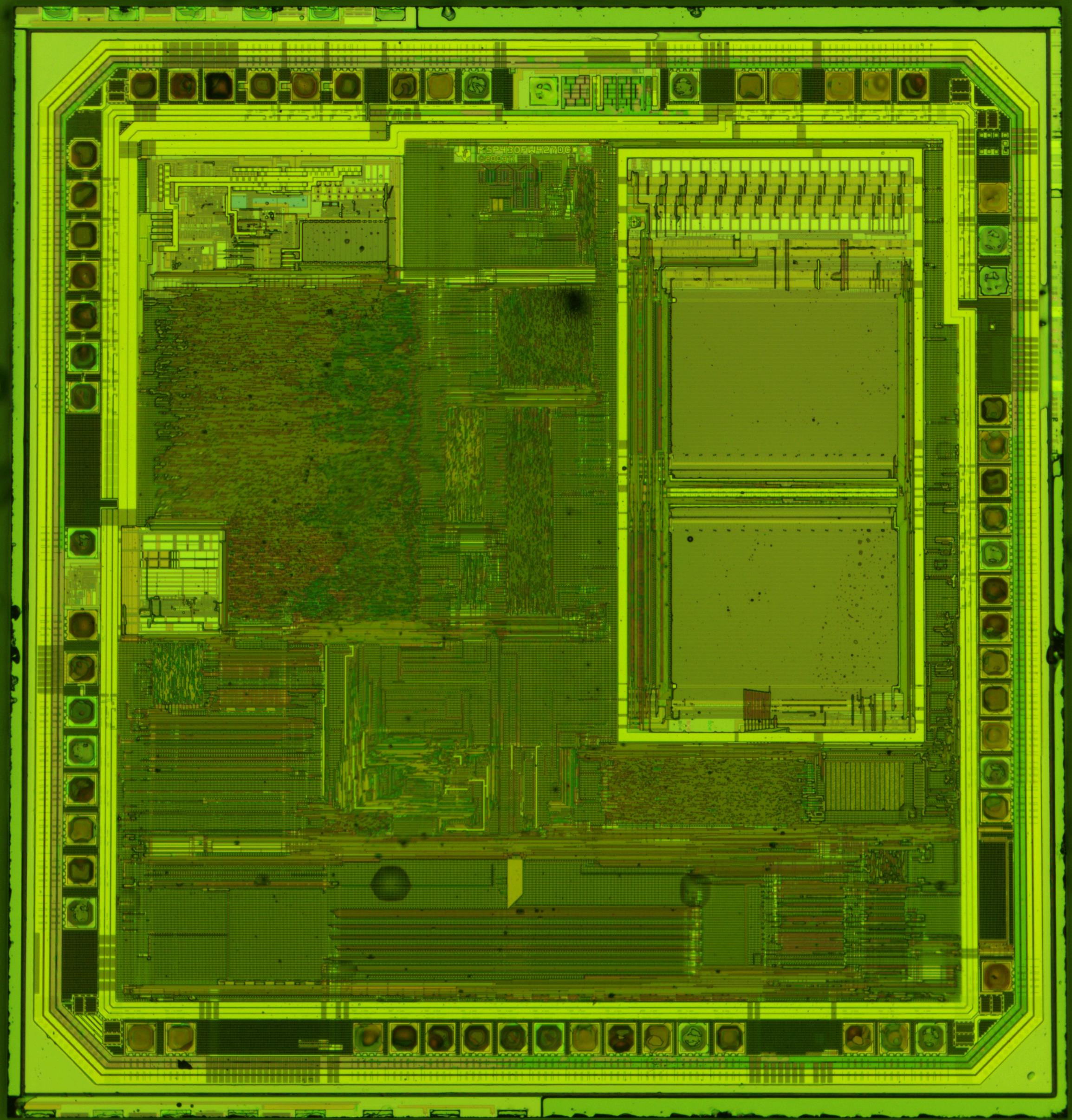


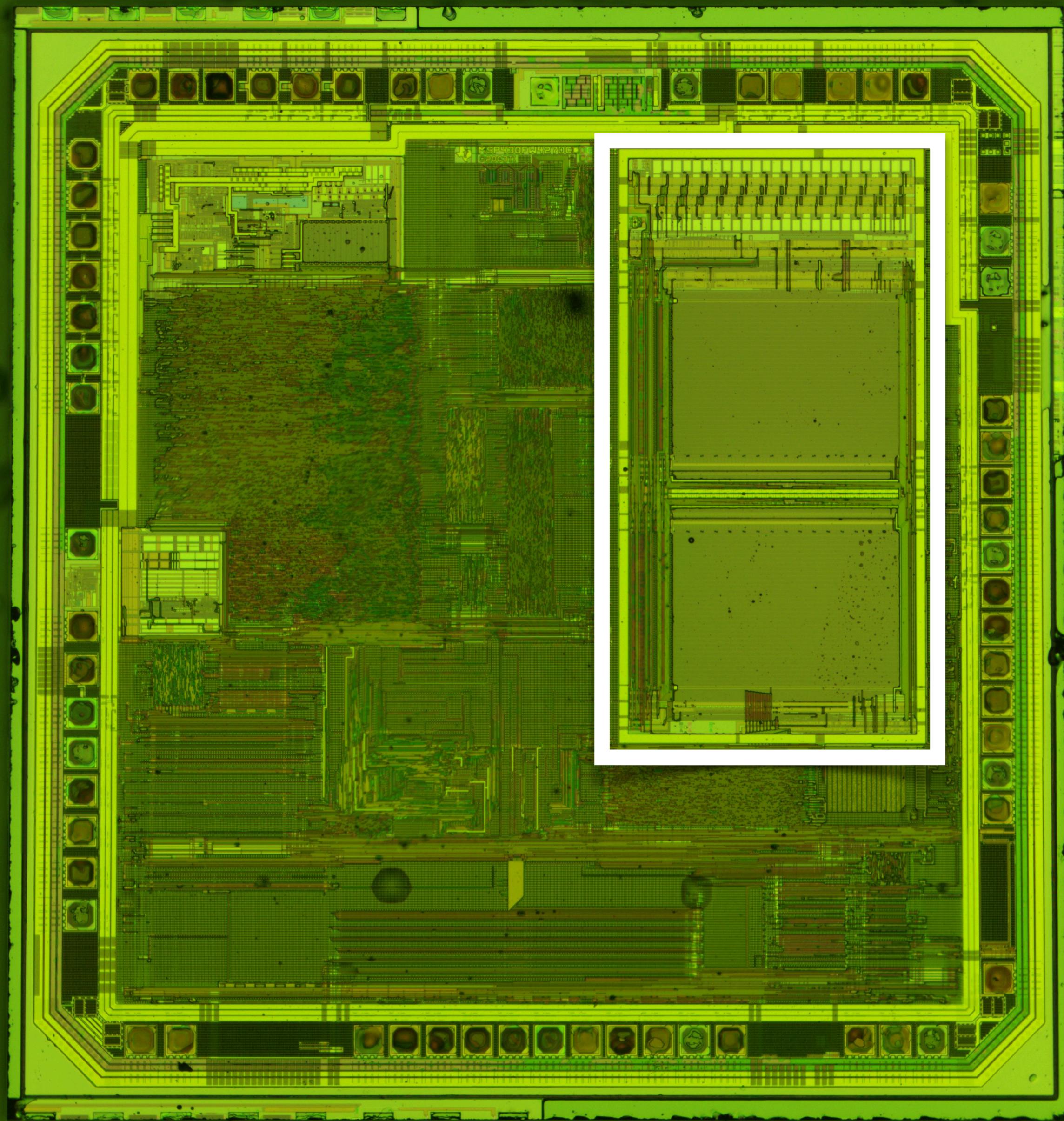
Exploiting the Device to Get the Firmware

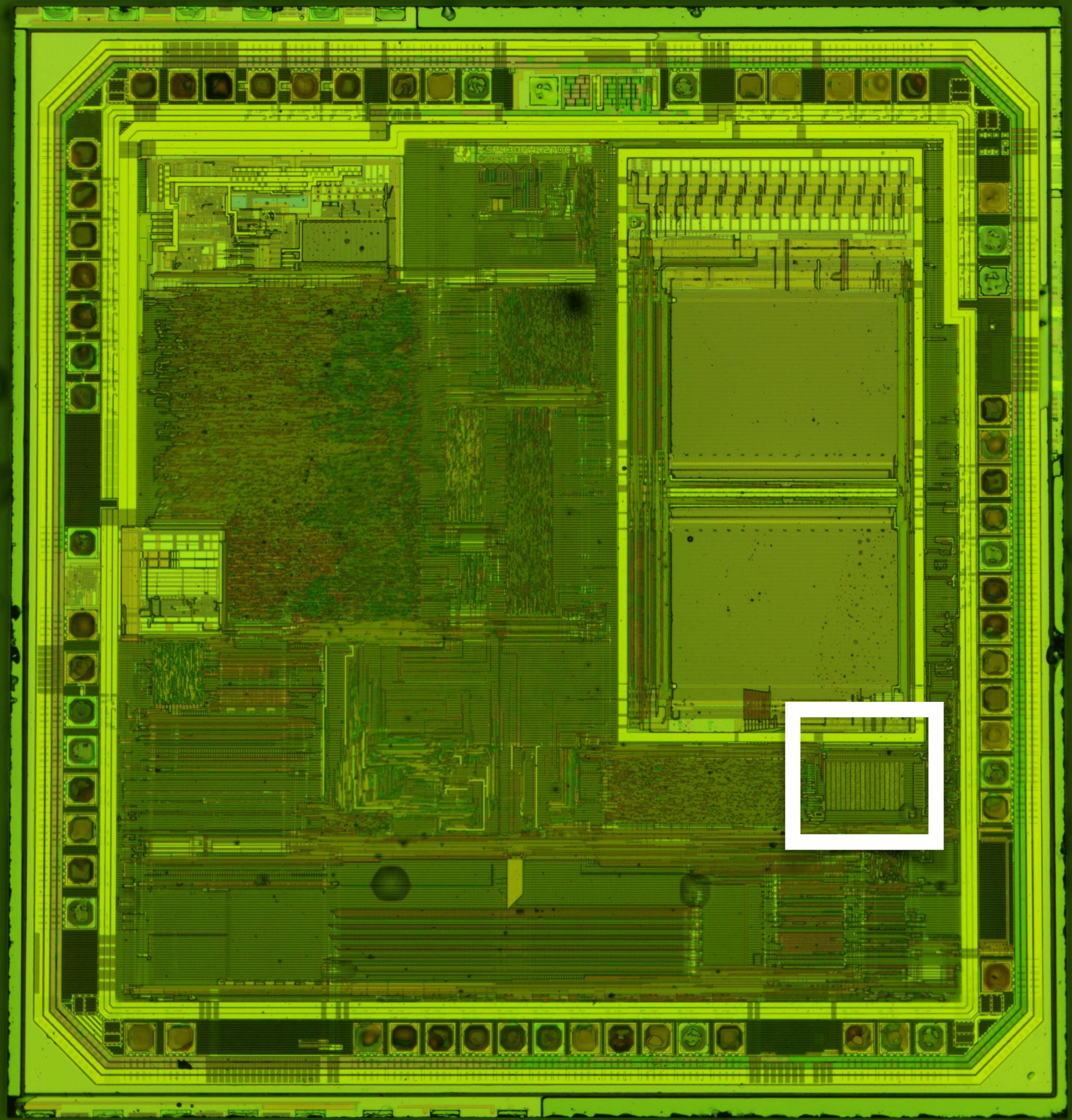


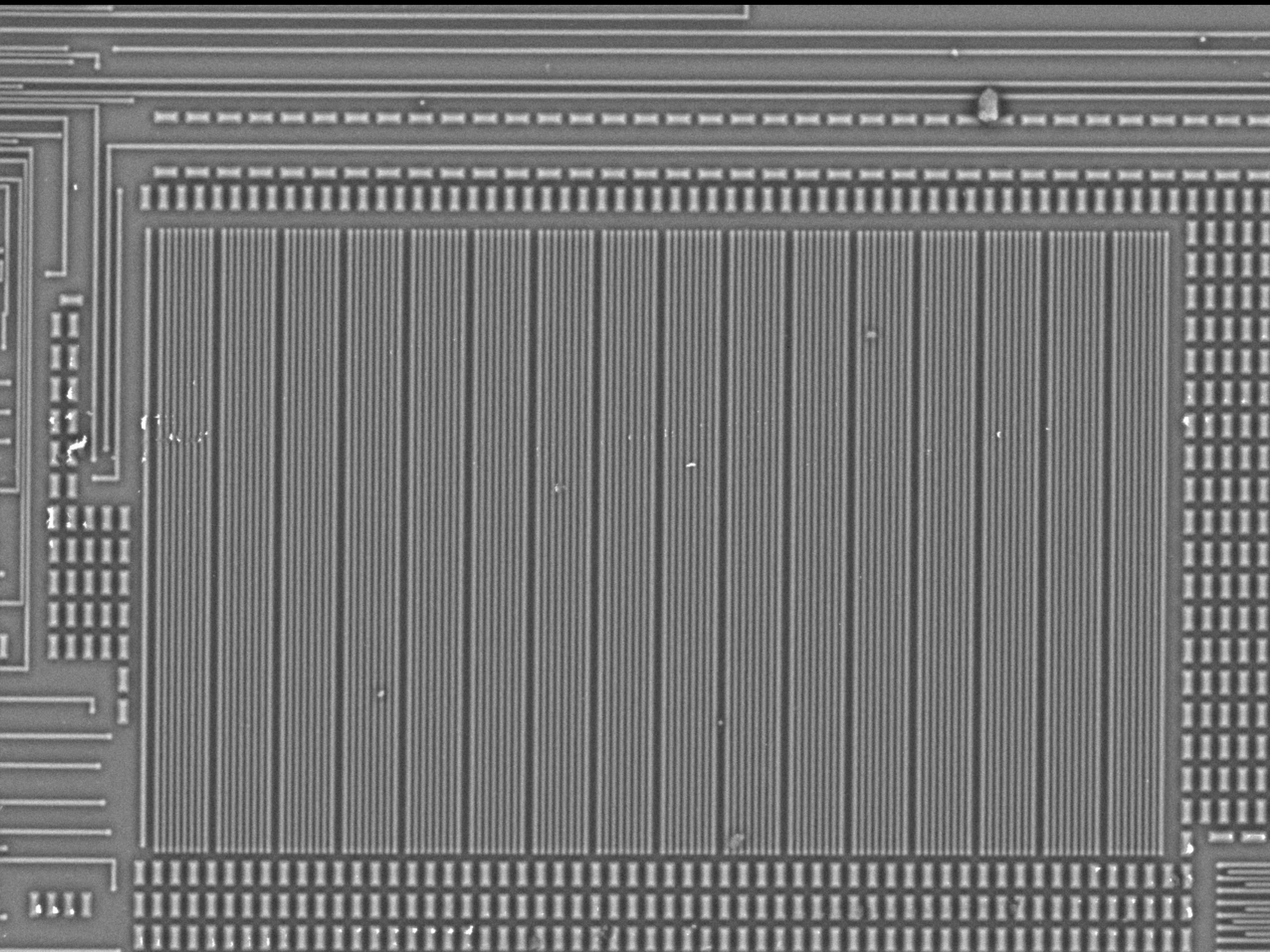
ROM Microscopy

- Mask ROM uses a custom mask layer in chip manufacturing to encode the bits. Different customers can have all other masks the same, and only change the mask that encodes the ROM bits.
- Implant ROM uses a mask with a hole for each bit, then selectively fires a laser at the mask to encode the bits.



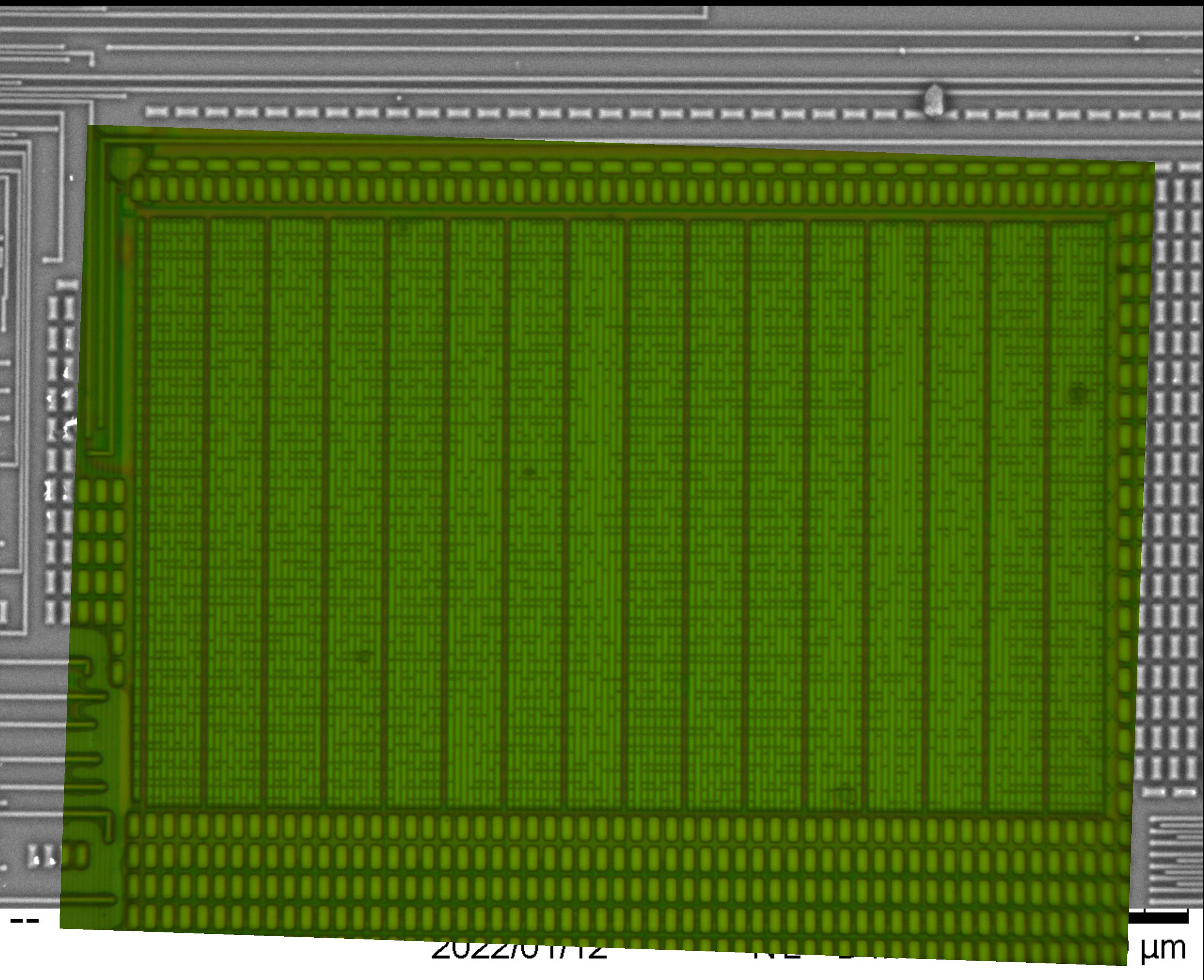






2022/01/12

NL D4.7 x600 100 μ m



Firmware Reverse Engineering

Languages and Loading Addresses

- Much wider variety of architectures than a PC.
 - AARCH32 and Thumb2 in ARM
 - MIPS and MIPS16
 - PowerPC and PPC16/VLE
 - MSP430, AVR, U8/100, Risc V, PIC16, 8051, 6502
- Many chips have two instructions sets: A long and a short one.

Firmware Reverse Engineering

Languages and Loading Addresses

- Where does the code sit?
 - AVR begins at 0x0000, MSP430 *ends* at 0xFFFF.
 - ARM Cortex M3 begins code at 0x0000.0000 or 0x0800.0000.
- Different methods of locating it:
 - Microcontroller datasheet, or SDK's linking scripts.
 - Look for some absolute address, then move the code until they match.
 - Guess until things look right.

Firmware Reverse Engineering

Getting our Bearings

- After loading the code, we don't know any function names.
 - Firmware is statically linked, there are no standard libraries.
 - There are no system calls.
- But we're not helpless:
 - I/O Addresses
 - Interrupt Vector Table

Firmware Reverse Engineering

- Hardware Peripherals have I/O Addresses
 - Standard prefix (0x4000.0000 in ARM)
 - Addressed by a "volatile" pointer.
- These are defined in header files:
 - P1REN is 0x0206
 - P1DIR is 0x0204
 - P1OUT is 0x0202
 - P1IN is 0x0200

```
//! Activate the side button.  
void sidebutton_init(){  
    //Set mode to I/O, direction to input.  
    P1SEL&=~BIT5;  
    P1DIR&=~BIT5;  
    //Pull up with internal resistor.  
    P1REN|=BIT5;  
    P1OUT|=BIT5;  
}  
  
//! Test the side button.  
int sidebutton_pressed(){  
    //Easily accessible side button.  
    if(!(P1IN&BIT5))  
        return 1;  
    return 0;  
}
```

Firmware Reverse Engineering

Interrupt Vector Table and Handlers

- Interrupt Vector Table is a list interrupt handlers.
 - "Vector" just means "function pointer."
 - Some architectures have instructions, instead of addresses.
- Continuing our button press example,
 - PORT1_VECTOR is 0xFFE2
 - Instead of polling that pin, the firmware might have an interrupt handler's function pointer at 0xFFE2.

Firmware Reverse Engineering

Recovering Functions from Standard Libraries

- Many functions come from static libraries.
 - Shipped in commercial C compilers and vendor SDKs.
 - Free trials of these compilers are available!
 - License is enforced in the Linker, not the Libraries.
- We can fingerprint these libraries!
 - IDA Pro FLIRT Signatures
 - symgrate.com

CodeBrowser: thd74/thd74-110

File Edit Analysis Navigation Search Select Tools Window Help

Program Trees

e0000000.bin

ram

Listing: thd74-110

*thd74-110

c00b32f2 70 47 bx lr

***** FUNCTION *****

undefined FUN_c00b32f4()

assume LRset = 0x0
assume TMode = 0x1

r0:1 <RETURN>

FUN_c00b32f4

c00b32f4 00 28 cmp r0,#0x0
c00b32f6 02 d0 beq LAB_c00b32fe
c00b32f8 41 65 str r1,[r0,#0x54]
c00b32fa c2 64 str r2,[r0,#0x4c]
c00b32fc 03 65 str r3,[r0,#0x50]

c00b32fe 70 47 LAB_c00b32fe bx lr

c00b3300 4c 69 62 s_Libpng_jmp_buf_still_allocated_c00b3300 ds "Libpng jmp_buf still allocated"

Decompile: setjmp - (thd74-110)

```
1 undefined4 setjmp(undefined4 *param_1)
2
3 {
4     undefined4 unaff_r4;
5     undefined4 unaff_r5;
6     undefined4 unaff_r6;
7     undefined4 unaff_r7;
8     undefined4 unaff_r8;
9     undefined4 unaff_r9;
10    undefined4 unaff_r10;
11    undefined4 unaff_r11;
12    undefined4 in_lr;
13
14    *param_1 = unaff_r4;
15    param_1[1] = unaff_r5;
16    param_1[2] = unaff_r6;
17    param_1[3] = unaff_r7;
18    param_1[4] = unaff_r8;
19    param_1[5] = unaff_r9;
20    param_1[6] = unaff_r10;
21    param_1[7] = unaff_r11;
22
23    *(BADSPACEBASE **)(param_1 + 8) = register0x00000054;
```

Console - Scripting

Symgrate2Query.py

28% (3200 of 11229)

Cancel

Data Type Manager

Data Types

- BuiltinTypes
- e0000000.bin
- generic_clib

Console Bookmarks

c00b3344

The screenshot shows the CodeBrowser interface with multiple windows open. The main window displays an assembly listing for the file 'thd74-110' with memory location 'e0000000.bin'. It includes sections for 'Program Trees' (showing 'ram'), 'Symbol Tree' (listing imports, exports, functions, labels, classes, and namespaces), and 'Data Type Manager' (listing various data types like 'BuiltInTypes', 'e0000000.bin', and 'generic_clib'). To the right, a decompiled view of the 'setjmp' function is shown, mapping assembly instructions to C-like pseudocode. A progress bar in a separate window indicates the status of a script named 'Symgrate2Query.py'.

A Tour of the Tower of Babel

So many languages!

- MSP430
 - 16 bit RISC instruction words, optional 16-bit prefix.
 - Von Neumann architecture.
- AVR
 - 16-bit or 32-bit instruction word
 - Harvard architecture.

A Tour of the Tower of Babel

So many languages!

- 8051
 - CISC instruction set, 1 to 3 bytes long.
 - Harvard with multiple memory types:
 - Internal RAM
 - Special Function Registers
 - Program Memory
 - External Data Memory

A Tour of the Tower of Babel

So many languages!

- ARM micros have both AARCH32 and Thumb2 instruction sets:
 - Load/Store Architect
 - Low-bit of PC (IP) chooses instruction set.
- AARCH32 (even)
 - 32-bit RISC instruction words
- Thumb2 (odd)
 - 16-bit instruction words, sometimes 32-bit pairs.

A Tour of the Tower of Babel

So many languages!

- Plenty more languages
 - TMS320 -- Found in DSPs, incompatible between revisions.
 - RiscV -- Open source, common in ASICs.
 - U8/100 -- Casio calculators, Oki LCD controllers.
 - Z80, 68000 -- Texas Instruments calculators
 - SATURN -- HP calculators
- Full custom and manufacturer-specific architectures are common in smaller chips.
- ARM/Thumb2 is semi-standard in larger devices.

How to identify the Instruction Set?

- Interrupt Table
 - MSP430 has 16-bit pointers at the *end* of memory.
 - Thumb2 has one even pointer at the beginning, followed by odd pointers.
 - Z80 uses instructions, instead of addresses.
- Instructions
 - Common entry and exit of functions.
 - "binwalk -A" searches for known patterns.

How to identify the Instruction Set?

Example Interrupt Table

- Interrupt Table is a list of handler addresses for interrupts.
 - In X86, interrupts are usually system calls.
 - In embedded systems, they are signals from I/O devices.
- "Reset Vector" is the entry point for our program, like main().
- "PORT1 Vector" called when something happens on PORT1.

How to identify the Instruction Set?

Example Interrupt Table

- 30 1A 00 20
- 15 56 00 08
- 29 54 00 08
- 2B 54 00 08
- 2D 54 00 08
- 2F 54 00 08

How to identify the Instruction Set?

Example Interrupt Table

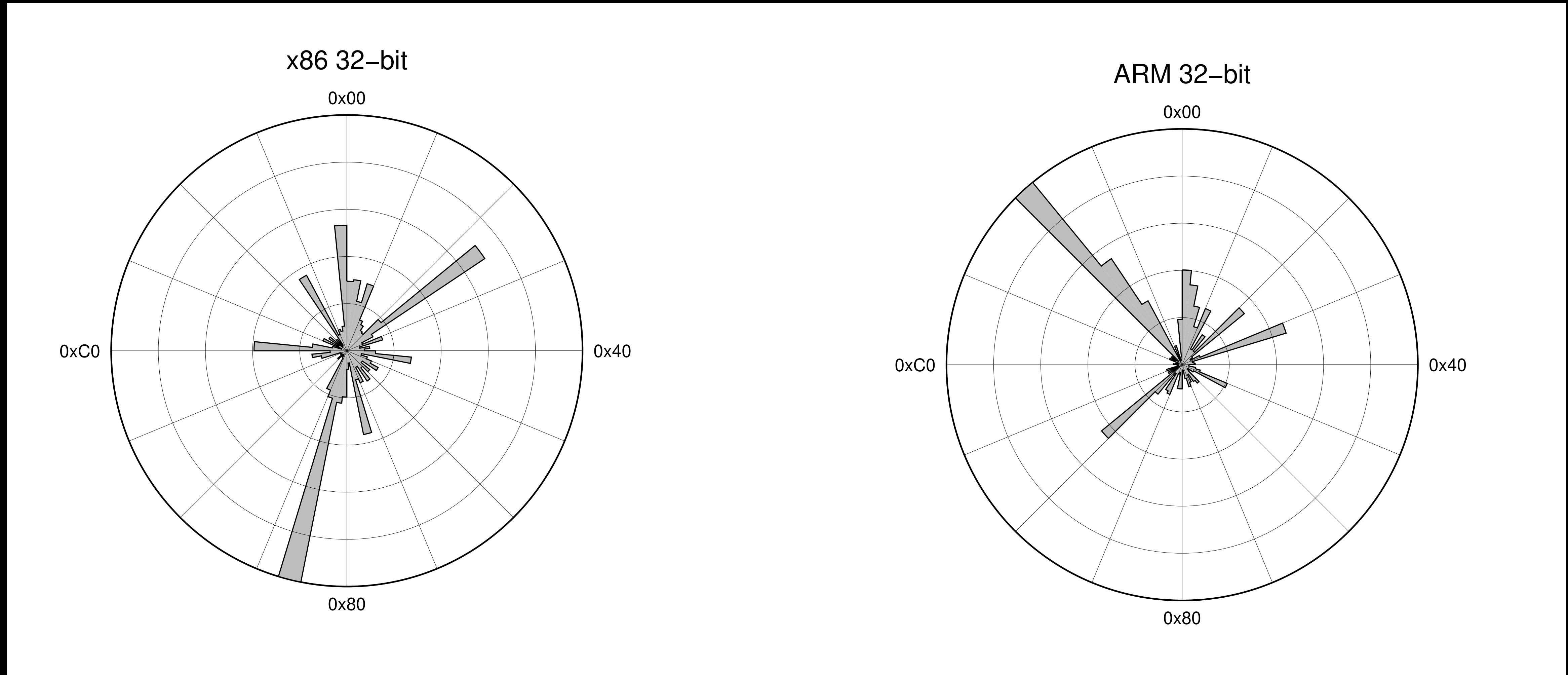
- 30 1A 00 20 = 0x2000.1A30
- 15 56 00 08 = 0x0800.5615
- 29 54 00 08 = 0x0800.5429
- 2B 54 00 08 = 0x0800.542B
- 2D 54 00 08 = 0x0800.542D
- 2F 54 00 08 = 0x0800.542F

How to identify the Instruction Set?

Example Interrupt Table (STM32F405, Thumb2)

- 30 1A 00 20 = 0x2000.1A30 Top of Stack
- 15 56 00 08 = 0x0800.5615 Reset Vector
- 29 54 00 08 = 0x0800.5429 Non-Maskable Interrupt (NMI)
- 2B 54 00 08 = 0x0800.542B Hard Fault
- 2D 54 00 08 = 0x0800.542D Mem Manage
- 2F 54 00 08 = 0x0800.542F Bus Fault
- Page 372 of 1,751 in the STM32F405 Reference Manual.

Identifying by Common Instructions



Identifying by Common Instructions

- ARM/Thumb2
 - Functions begin with "PUSH {.., LR}" and end with "POP {.., PC}".
 - Literal constants sit between functions.
- MSP430
 - Functions end with "RET." (0x4130)
 - "CALL" (0x12B0) is very common.
 - No gaps between functions.

