University of California, Davis

Department of Electrical and Computer Engineering

Lab 4: A Combinational Video Display Circuit

This lab involves the design and implementation of a purely combinational circuit that generates color pixels for a VGA monitor based on inputs from ten switches on the DE10-Lite FPGA board.

I. Prelab

Complete the following and submit your work at the beginning of your lab session.

1. Read the tutorial mentioned in Section II.
2. [10 pts] Perform and document a preliminary design of your lab4.v

II. Monitor Interface Module

A set of three modules as well as supporting "ip" and "synthesis" files have been written for you which serve as the interface to the VGA monitor for this lab.

Details of the module and downloadable code are posted on the EEC 180B lab page, "Tutorial: Displaying to a VGA monitor using a combinational circuit."

Read the tutorial, download and read the code so you are familiar with it.

III. Your Module

Download and unzip the .zip file posted on the tutorial web page. All of your code should be placed inside the file comb_ckt_generator.v which considers the values of input switches and generates the proper output colors when the inputs **`col`** and **`row`** specify pixels.

Your design must implement the operations shown in the table on the following page controlled by the ten DE10-Lite board switches `SW[9:0]`.

Drawn rectangles are 32 pixels by 32 pixels and are displayed in the four areas of the screen as specified. They should be placed in exact locations within the regions that look good to you.

DE10-Lite switches	Parameter	Comments
SW[9]	Rectangle X position	0: left half 1: right half
SW[8]	Rectangle Y position	0: bottom half 1: top half
SW[7]	Rectangle red	0: red off (0000) 1: red on (1111)
SW[6]	Rectangle green	0: green off (0000) 1: green on (1111)
SW[5]	Rectangle blue	0: blue off (0000) 1: blue on (1111)
SW[4]	Rectangle filled	0: rectangle hollow, single pixel line width 1: rectangle drawn filled
SW[3:2]	Screen background color	00: Black, RGB=0000/0000/0000 01: Gray, RGB=1000/1000/1000 10: Aggie blue, RGB=0010/0100/0111 11: UCD gold, RGB=1110/1011/0010
SW[1] and/or SW[0]	Something interesting likely not done by anyone else in the class	-

III. Testing in Simulation

Design and write a new testbench for your module that exercises the functions of all input switches. Suggestion: consider implementing multiple independent tests that are shorter in length and focus on specific features.

Once your design is working correctly, demonstrate it to your TA and have it checked off.

IV. Implementation and Verification on the DE10-Lite

The next step is to test and demonstrate operation on the DE10-Lite board.

Use the modules posted on the course web page in the previously-mentioned tutorial.

Once your design is working correctly, demonstrate it compiling, downloading, and operating to your TA and have it checked off.

Submitted Work [100 pts total]

With the exception of instructor-provided code, all work must be yours alone.

[10 pts] **Prelab**

[80 pts] **Lab Checkoffs**

1) [30 pts] Demonstrate correct operation in simulation using your testbench
2) [50 pts] Demonstrate correct compiling, downloading, and operation on the FPGA board

[10 pts] **Lab Report**

Submit all Verilog hardware and testbench code that you wrote. Do not include any code that you did not write such as files generated by Quartus or IP components.

a) [10 points] Print and submit a paper copy during your lab session.

b) Upload a copy to Canvas by performing the following steps by the end of your lab session—this is essential to receive credit for the entire lab.

1. Make a folder on your computer
2. Copy all verilog files you wrote into the folder—only the ones you wrote
3. "zip" the folder into a single .zip file
4. Log onto Canvas, click Assignments, find the correct lab number
5. Upload the .zip file

2018/05/01 Fixed typo: "sixteen" should be "four"
2018/04/29 Posted