TSPA4C500x

Product Datasheet

- Revision: A_Draft
- Date: 2019-05-14
- Document Number: N/A

Revision History

Revision	Date	Description
A_Draft	2019-05-14	Initial release;

Table of Contents

1 General Description

1.1 Product Concept

TSPA4C500x is compliant with 2.4GHz wireless communication, Bluetooth V5.0 Low Energy. RF analog and baseband digital parts. TSPA4C500x integrates Bluetooth 5 with specification compliant such as 2Mbps high data rate mode as well as the extended advertising capabilities.

1.2 Features

- Compliant with Bluetooth v5.0 Low Energy
  - ✧ High Data Rate supports up to 2Mbps
  - ✧ Advertising Extension support

- RF performance
  - ✧ Max transmit power: +4dBm
  - ✧ Receiver sensitivity: -96 dBm @ 1Mbps
    -94 dBm @ 2Mbps
  - ✧ Tx output 0dBm, 6.5mA, up to +4 dBm，Rx 7mA

- CPU & Memory
  - ✧ ARM Cortex-M4F up to 64MHz with i-cache
  - ✧ 512KB Flash
  - ✧ 64KB SRAM
  - ✧ 1Kb eFuse memory (Manufacturer ID, Security Key storage)
  - ✧ Over-The-Air Update (OTA) support
  - ✧ SWD debug interface

- Peripheral
  - ✧ Up to 24 GPIOs
  - ✧ 2 I2C, master/slave up to 400KHz clock
  - ✧ 2 SPI masters; one is dedicated for external flash memory and the other is w/ multiple SPI slaves supported, up to 16MHz clock
  - ✧ 1 SPI slave, up to 4MHz clock
  - ✧ 2 UART up to 2MHz
  - ✧ 3 dedicated PWMs
  - ✧ 2 PDM mono, 1 stereo with clock range from 160KHz~5.12MHz
  - ✧ ISO7816

- ✧ Keyboard scanner, up to 14 channels
- ✧ 11-bit ADC, 1MS/s, up to 10 channels
- ✧ 4 counters/timers

- Clocks
  - ✧ Build-in 32MHz oscillator for crystal oscillator connection
  - ✧ Build-in 32.768KHz oscillator for crystal oscillator connection

- DMA Controller
  - ✧ Up to 2 concurrent DMA streams with 4 channels each

- Voice over BLE
  - ✧ Build-in 16KHz sampling ADPCM codec, 4:1 compression ratio with 64Kbps mono, 128Kbps stereo

- Power mode
  - ✧ Deep Sleep mode <500nA with 32KHz RC ON
  - ✧ Shutdown mode <20nA

- PMU
  - ✧ Integrated DCDC buck convertor
  - ✧ Input voltage range: 1.8~4.3V

- Packaging
  - ✧ QFN 48 pin 5x5mm 0.35mm pitch, 0.9mm thickness

1.3 Device System Block Diagram

The Figure 1.1 below shows the system block diagram of SoC TSPA4C500x product. And features available on the diagram will vary by part number.

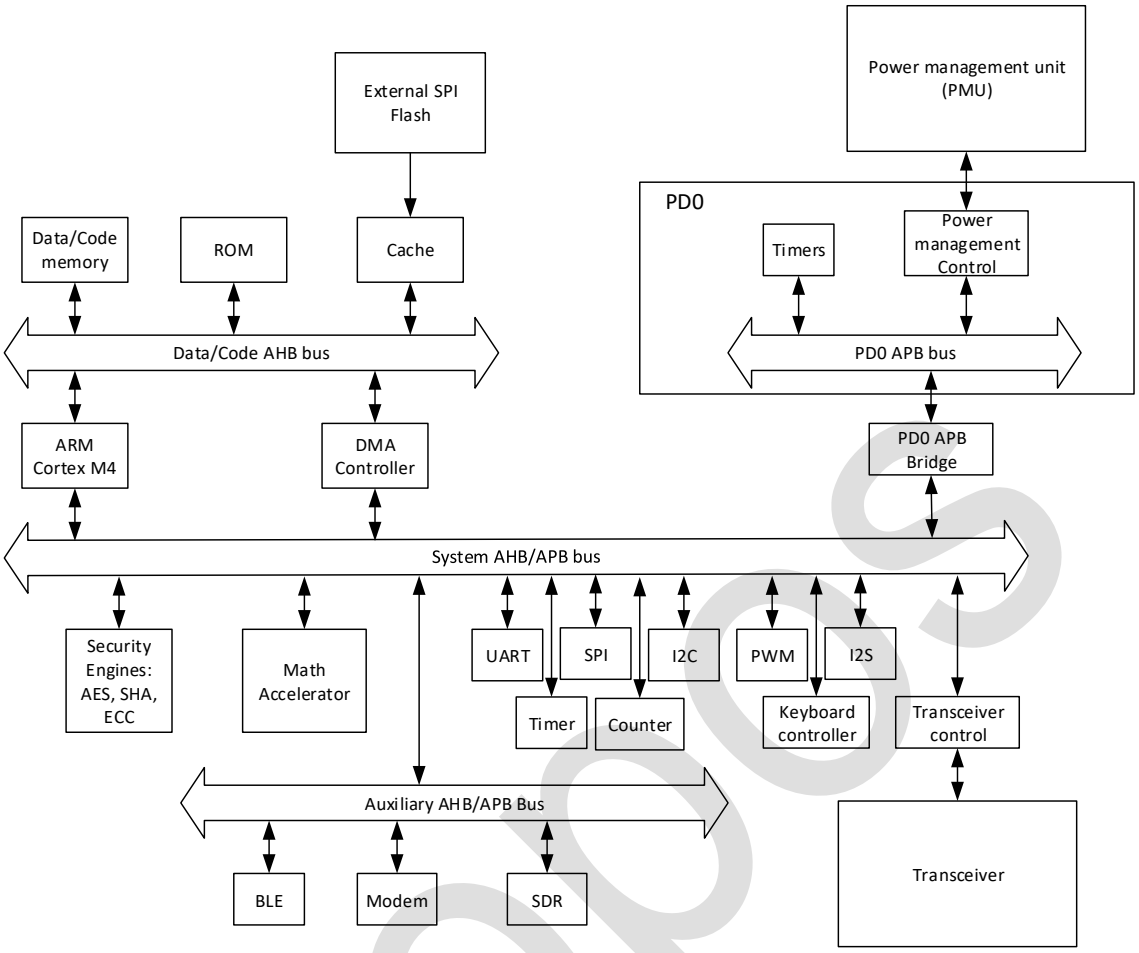


Figure 1.1: Device System Block Diagram (top view)

2 Pin Map Information

2.1 Pin Assignment

The pin assignment (top view) of TSPA4C500A is shown as Figure 2.1.

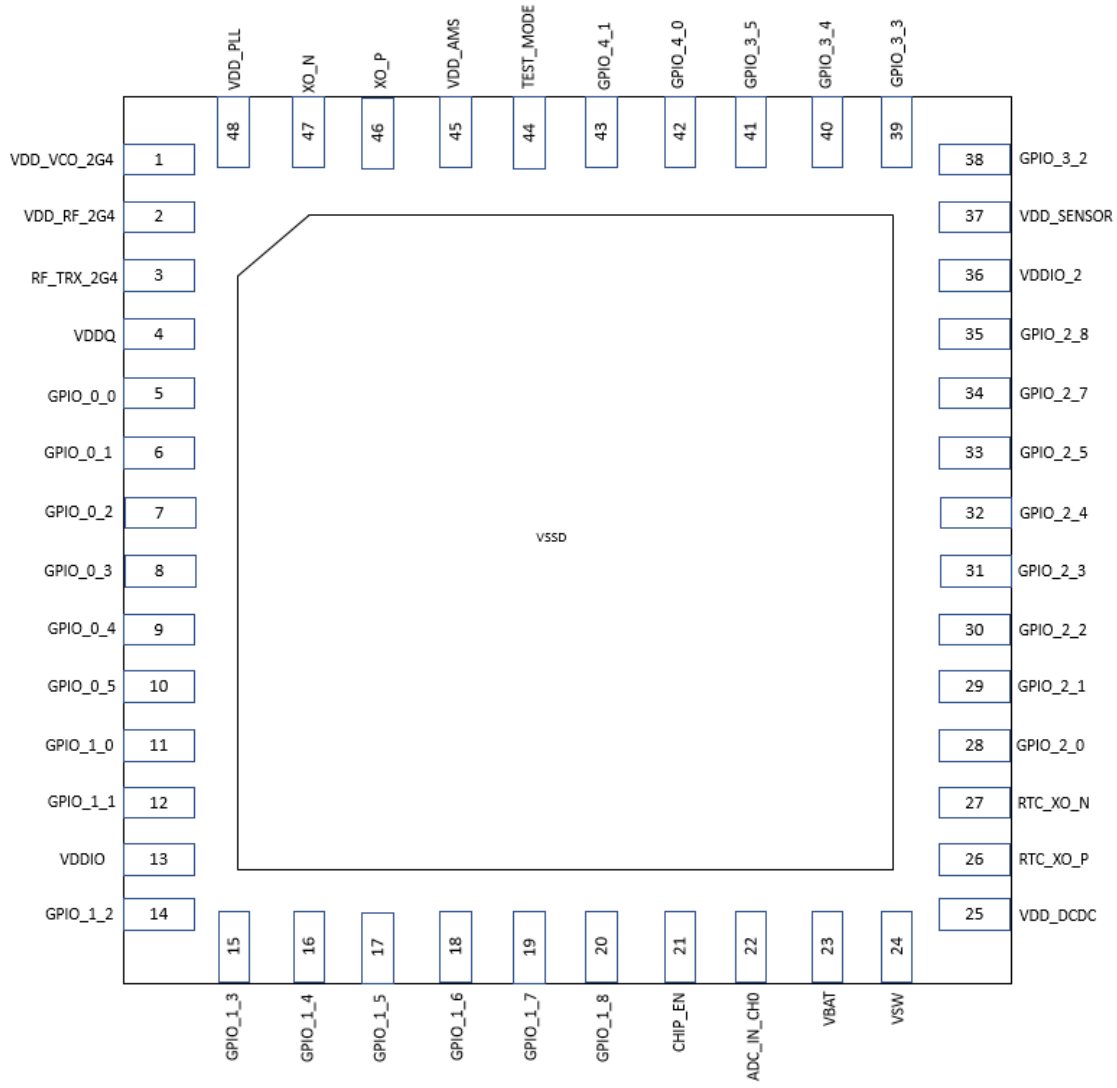


Figure 2.1: Pin assignment (top view)

2.2 Pin Function Descriptions

The attributes, input/output states for operating modes and descriptions for pin functions are shown in Table 2.1.

Pin No.	Pin Name	Pin Type	Functional description
1	VDD_VCO_2G4	Analog/RF	RF VCO Power Supply 1.2V
2	VDD_RF_2G4	Analog/RF	RF Power Supply 1.2V
3	RF_TRX_2G4	Analog/RF	RF Port
4	VDDQ	DIGITAL Input	EFUSE Programming Voltage Supply
5	GPIO_0_0	DIGITAL I/O	Digital Signal GPIO_0_0
6	GPIO_0_1	DIGITAL I/O	Digital Signal GPIO_0_1
7	GPIO_0_2	DIGITAL I/O	Digital Signal GPIO_0_2
8	GPIO_0_3	DIGITAL I/O	Digital Signal GPIO_0_3
9	GPIO_0_4	DIGITAL I/O	Digital Signal GPIO_0_4
10	GPIO_0_5	DIGITAL I/O	Digital Signal GPIO_0_5
11	GPIO_1_0	DIGITAL I/O	Digital Signal GPIO_1_0
12	GPIO_1_1	DIGITAL I/O	Digital Signal GPIO_1_1
13	VDDIO	I/O Power	I/O Voltage Supply for GPIO power domain 1
14	GPIO_1_2	DIGITAL I/O	Digital Signal GPIO_1_2
15	GPIO_1_3	DIGITAL I/O	Digital Signal GPIO_1_3
16	GPIO_1_4	DIGITAL I/O	Digital Signal GPIO_1_4
17	GPIO_1_5	DIGITAL I/O	Digital Signal GPIO_1_5
18	GPIO_1_6	DIGITAL I/O	Digital Signal GPIO_1_6
19	GPIO_1_7	DIGITAL I/O	Digital Signal GPIO_1_7
20	GPIO_1_8	DIGITAL I/O	Digital Signal GPIO_1_8
21	CHIP_EN	PMU	Chip Enable
22	ADC_IN_CH0	PMU	Sensor ADC Input
23	VBAT	PMU	Chip Power Supply
24	VSW	PMU	DCDC Converter Switching Node
25	VDD_DCDC	PMU	DCDC Converter Feedback Node
26	RTC_XO_P	PMU	RTC positive terminal
27	RTC_XO_N	PMU	RTC negative terminal
28	GPIO_2_0	Mixed Signal I/O	Mixed Signal GPIO_2_0
29	GPIO_2_1	Mixed Signal I/O	Mixed Signal GPIO_2_1
30	GPIO_2_2	Mixed Signal I/O	Mixed Signal GPIO_2_2
31	GPIO_2_3	Mixed Signal I/O	Mixed Signal GPIO_2_3
32	GPIO_2_4	Mixed Signal I/O	Mixed Signal GPIO_2_4
33	GPIO_2_5	Mixed Signal I/O	Mixed Signal GPIO_2_5

34	GPIO_2_7	Mixed Signal I/O	Mixed Signal GPIO_2_7
35	GPIO_2_8	Mixed Signal I/O	Mixed Signal GPIO_2_8
36	VDDIO_2	I/O Power	I/O Voltage Supply for GPIO power domain 2
37	VDD_SENSOR	PMU	Power Supply Output
38	GPIO_3_2	Digital I/O	Digital Signal GPIO_3_2
39	GPIO_3_3	Digital I/O	Digital Signal GPIO_3_3
40	GPIO_3_4	Digital I/O	Digital Signal GPIO_3_4
41	GPIO_3_5	Digital I/O	Digital Signal GPIO_3_5
42	GPIO_4_0	Digital I/O	Digital Signal GPIO_4_0
43	GPIO_4_1	Digital I/O	Digital Signal GPIO_4_1
44	TEST_MODE	DIGITAL Input	Test Mode Selection, GND for Normal Operation
45	VDD_AMS	Analog/RF	AMS Supply 1.2V
46	XO_P	Analog/RF	XO positive terminal
47	XO_N	Analog/RF	XO negative terminal
48	VDD_PLL	Analog/RF	RF PLL Power Supply 1.2V

Table 2.1: Pin function

3 Function Block Description

3.1 CPU and Memory Subsystem

The device integrates a powerful ARM Cortex-M4F processor core and their associated busses and memories. The Coretex-M4F processor incorporates a processor core, Nested Vectored Interrupt Controller (NVIC), high performance bus interfaces and a Floating-Point Unit (FPU).

The core processor has 16KB instruction cache. This subsystem also includes two independent DMA controllers with 4 channels each, 64KB of SRAM and 256KB of ROM. The subsystem integrates a hardwired cryptographic engine which is associated with the boot loader system to provide a secure boot implementation. This includes both system integrity check and authentication check of the application software. The advanced architecture design of system buses provides the exclusivity of access to radio communication blocks at the same time the flexibility of access to other peripheral blocks without sacrificing the system performance and stability.

There are two DMA controllers with 4 channels each. They support independent accesses to peripherals using AHB bus to copy data from data/instruction memory to the peripheral memories or vice versa. There is 64KB of SRAM memory, which can be fully retained or retained in increments of user defined blocks as small as 4KB. There is 256KB of ROM memory that contains boot loader and Bluetooth 5 protocol stack. The device also integrates a 512KB flash memory (stacked) for user program and data storage. The device supports XIP (execute-in-place) mode for the flash memory so that user can directly execute the program from flash memory rather than copying it into SRAM to run.

See Figure 3.1 and Figure 3.2 for the memory map in detail.

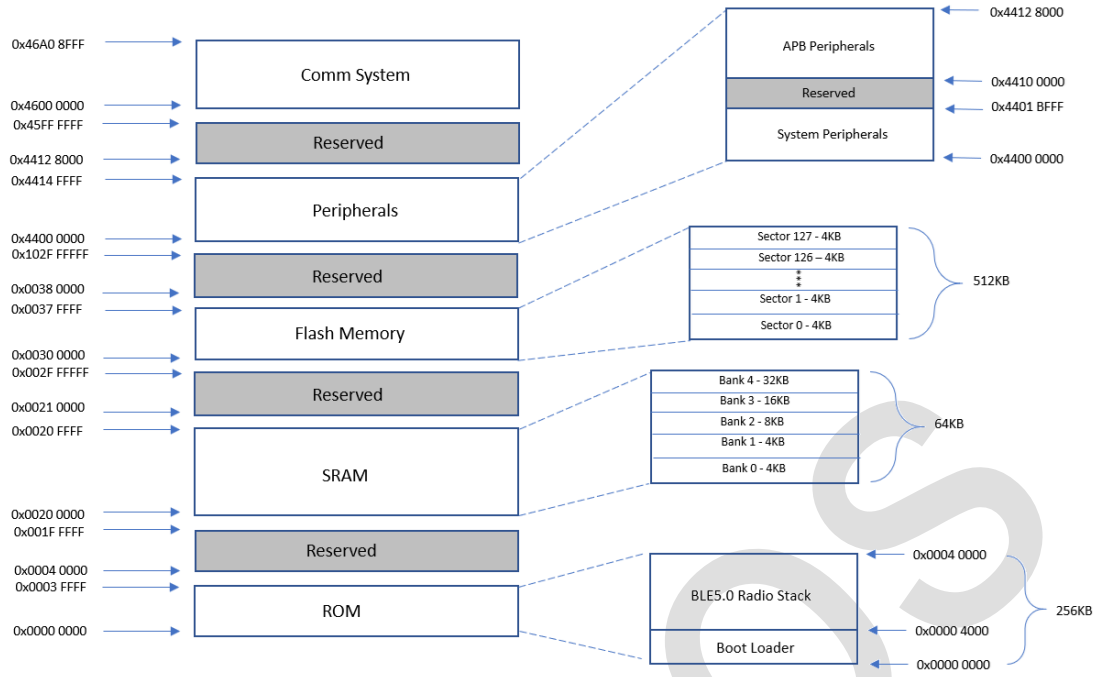


Figure 3.1: Memory Map

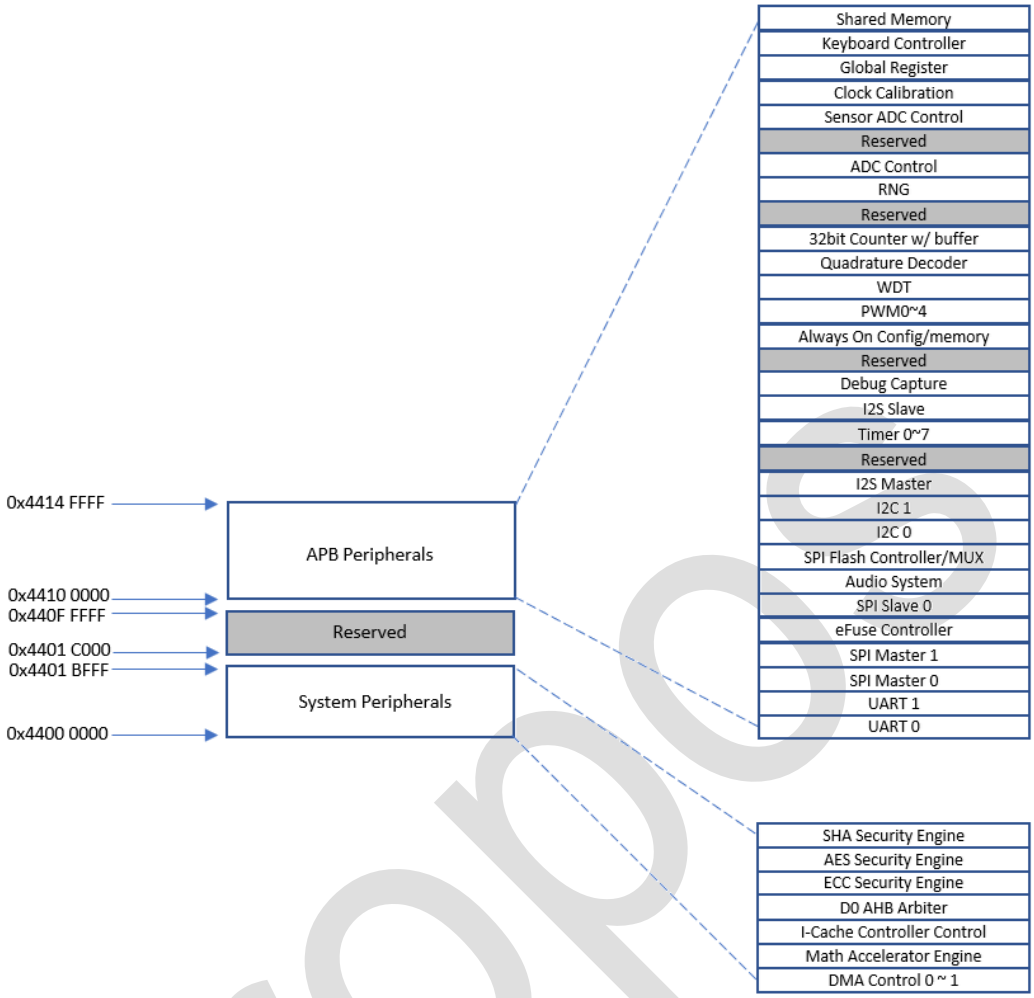


Figure 3.2: Peripheral Memory Map

3.2 Power System and Clock

3.2.1 Power Domains and Power Operation Modes

The power system provides assurance that power supplies for each respective operation mode or blocks are provided with correct timing and voltage.

The device has the following power domains: AONPD (Always-On Power Domain), DOOPD (Dynamic On-off Power Domain) and seven data/instruction memory banks which can be in active mode, retention mode, or power-down mode.

Some power operation modes are listed as followings:

- Chip deep-sleep mode. Only the AONPD domain is on. All the other domains are shut down. In this mode, a sleep timer is running, and the timer decides when to wakeup other domains. This mode can be also waken-up by an external wakeup pin or brown-out detection triggering event.
- Chip sleep modes with memory retention. The AONPD is on, and the content of a certain memory banks is retained. For example, one of such modes is with a 4kB memory bank in retention mode. This is the mode for BLE radio to operate in the most power efficient way during sleep operation for simple task operating such as advertising or with one connection only.
- Chip Active Mode. All the power domains are on.
- Chip Shut Down mode. All blocks are being powered down. The leakage current at this mode is less than 100nA.

3.2.2 Power Supplies

Figure 3.3 shows the power supply architecture for different power domains and blocks. The device has multiple power supplies which including VBAT, VDDIO, and VDDQ. Inside Device, it has a buck DCDC converter, an AONPD LDO, a retention LDO, and two VDDIO switches.

- The AONPD logic is powered by the AONPD LDO.
- The DCDC supplies power for the RF transceiver and the digital core (including CPU, digital portion of the transceiver, efuse, peripherals) through a digital LDO.
- The memory banks are powered by the digital core LDO during active operation mode and by the retention LDO during sleep mode
- The two VDDIO switches (VDDIO SW1 and SW2) provides power supply to external flash memory and external circuity (such as a sensor). During sleep mode, these two switches can be configured to be off in order to reduce leakage power.
- The VDDQ is used to program the efuse memory. It is only needed during efuse programming.

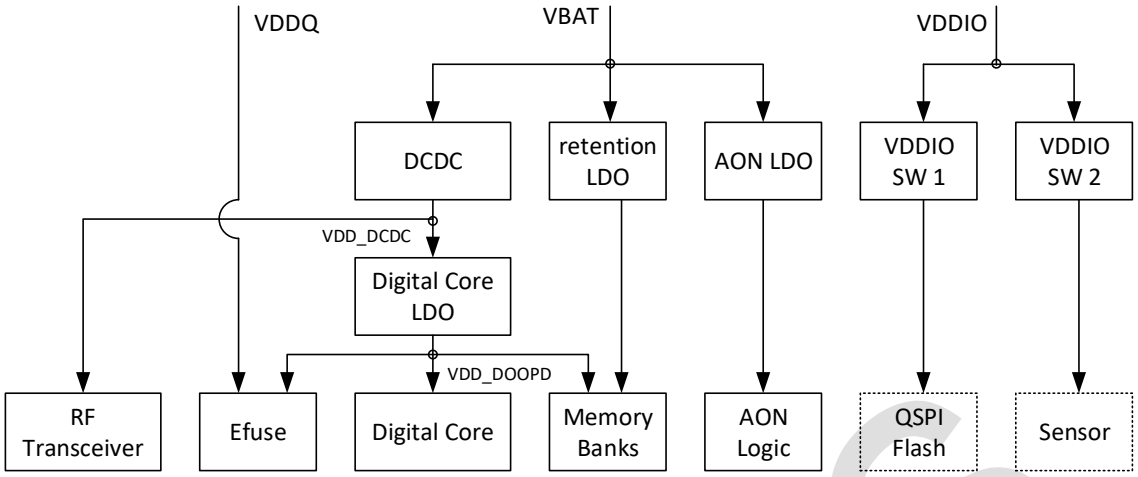


Figure 3.3: Device Power Supplies

DCDC Converter

The buck DCDC converter, as shown in Figure 3.4, efficiently reduces the voltage of the battery to around 1.2V. The 1.2V supply is used to power the radio transceiver directly. In addition, it is used as the input to a LDO that in turn creates the supply for the digital core. Two external components are required for the DCDC converter, an inductor and a capacitor. The recommended values are 4.7uH and 4.7uF, respectively. Other values are permitted; however, they will affect the behavior of the DCDC in terms of efficiency, startup time, and ripple amplitude.

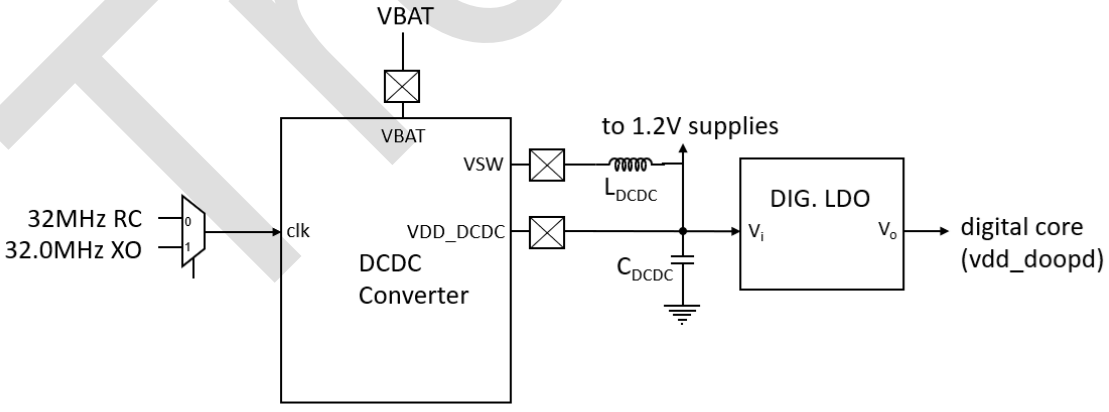


Figure 3.4: DCDC Buck Converter

3.2.3 Clock System

The device's clock system is designed to provide clocks to all subsystems that require clocks and for switching between different clock sources without degrading system performance or power consumption.

There are five types of clock sources. They are RC 32KHz, RTC 32.768KHz, RC 32MHz, XO32/64MHz, and Programmable CLK from the clock PLL. RC 32KHz is the default clock for the AONPD.

3.2.3.1 RC 32KHz

RC32KHz clock is a low frequency clock which is being used for AONPD logic. This clock is the default clock source for AONPD upon cold boot. If the efuse memory configuration indicates an RTC crystal is installed, the boot rom code will switch AONPD clock source to RTC clock.

3.2.3.2 RTC 32.768KHz

During cold boot, the RC 32KHz is the default clock for AONPD. After cold boot, the boot rom code will enable RTC clock and switches to RTC 32.768KHz for AONPD if RTC crystal is installed. Figure 3.5 shows a block diagram of 32.768KHz crystal.

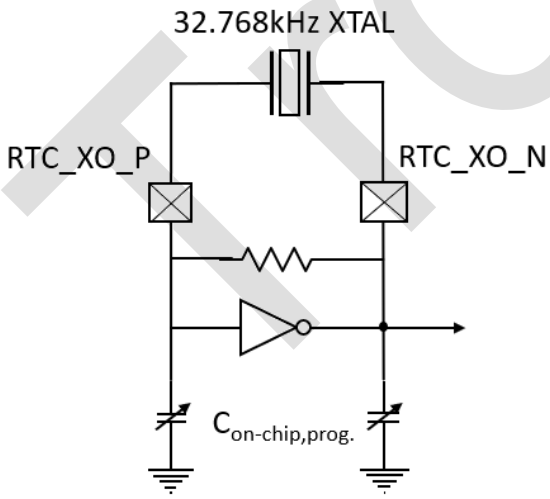


Figure 3.5: 32.768KHz Crystal

The device also supports external 32.768KHz clock source as input as shown in .

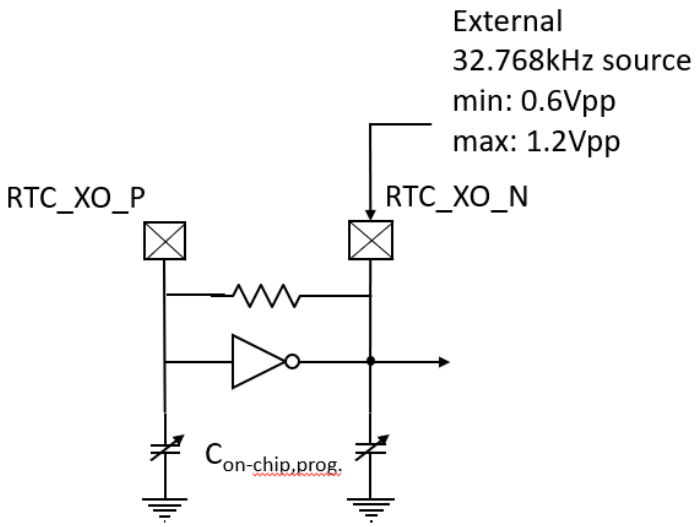


Figure 3.6: External 32.768KHz source

The RTC clock can be muxed out to a GPIO pin that users can use for their applications.

3.2.3.3 RC 32MHz

RC 32MHz is a 32MHz high frequency ring oscillator which provides clock source while the crystal oscillator is starting up. CPU will use RC 32MHz by default after code boot or wake-up from sleep mode and SW may switch to XO clock after XO becomes stable.

3.2.3.4 XO Clock

XO clock is high frequency clock source in 32MHz. XO clock is sourced from an external 32MHz crystal as shown in Figure 3.7. XO is controlled by AONPD and is enabled by default after cold boot. The bootloader should switch between the CPU clock and peripheral clock from RC 32MHz to XO 32MHz. This is important for the bootloader as the bootloader may try to get an image from UART interface which requires a more accurate clock source.

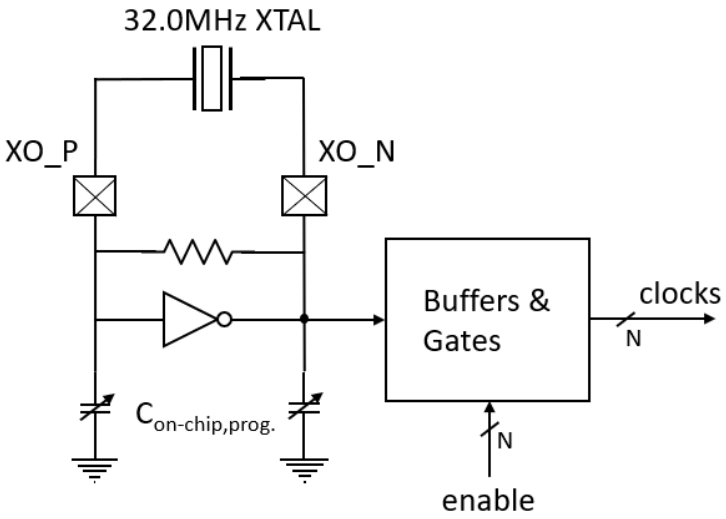


Figure 3.7: XO Clock Source

3.2.3.5 CLK PLL

Clock PLL is designed to provide multiple clock frequencies for different clock requirements for the BLE transceiver on different PHY rate receptions. By default, CLK PLL is automatically controlled by the hardware.

3.3 Bluetooth 5 Radio and Subsystem

The device incorporates a Bluetooth Low Energy subsystem that contains the baseband, PHY and link layer engines with an embedded security engine and is compliant with Bluetooth Core 5 specification including features supported such as extended advertising packet length, higher throughput.

The physical layer has the digital PHY and RF transceiver that transmits and receives GFSK packets at up to 2Mpbs over a 2.4Ghz ISM frequency band.

The baseband controller combines both hardware and software implementation that supports all device classes (Broadcaster, Central, Observer and Peripheral). And all the timing critical functions are implemented in hardware such as encryption/decryption, FEC decoder, CRC, data whitening and access address detection.

Key BLE5.0 features being supported are as followings:

- Bluetooth Low Energy v5.0 Specification compliant
- All packet types support (Broadcasting/Advertising/Data/Control)

- Advertising packet extension, up to 255 bytes
- Encryption/Decryption (AES-CCM) for enhanced security at link layer
- Bit Stream processing (CRC, Whitening)
- All device classes support (Broadcaster, Central, Observer, Peripherals)
- Bluetooth Low Energy v4.0/4.1/4.2 features are fully supported.

The 2.4GHz transceiver has one chip pin, RF_TRX_2G4, for both the transmission and reception of RF signals, as shown in Figure 3.8. An on-board matching network is recommended to get the best RF performance out of the device. It is possible for the matching network to favor the RX path over the TX path or vice-versa, but the recommended matching network in the reference design is a balance of both paths. There are four supply pins for the 2.4GHz transceiver, that are nominally 1.2V. They should normally be connected to the DCDC output, VDD_DCDC. The transceiver needs a 32.0MHz crystal oscillator reference. To reduce BOM cost, the CI for the crystal is integrated on-chip. The on-chip CI can be programmed with registers from 0.5pF to 8pF in 0.5pF steps.

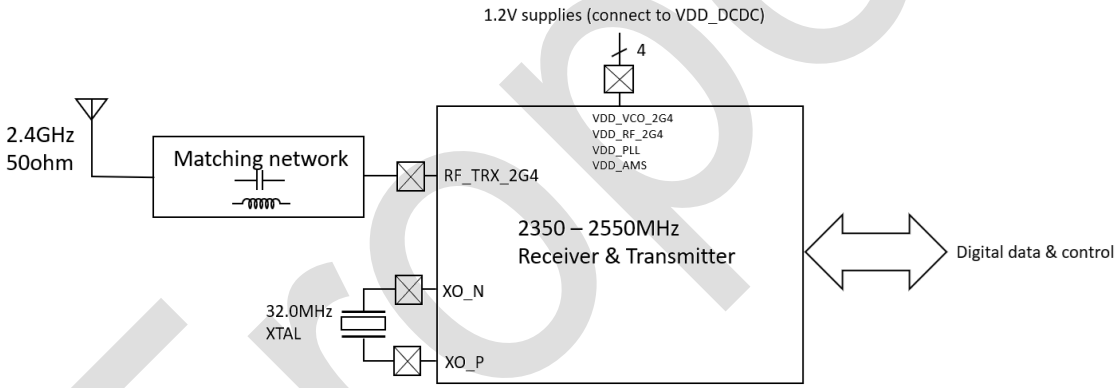


Figure 3.8: 2.4GHz RF Transceiver

3.4 Special Function Blocks

3.4.1 11-bit Sensor ADC

The device has a sensor ADC block as shown in Figure 3.9 which user can use for converting analog signals to digital domain signal for CPU processing.

The Sensor ADC has 11 physical bits and can convert at a maximum of 1MSPS. The actual clock speed and conversion rate are controlled through digital settings. The input to

the ADC is preceded by a multiplexer which enables the user to sample up to 11 different channels (package option dependent). In addition, the ADC can be used to measure the internal VBAT voltage level or the temperature. The digital control system for the ADC gives the user the flexibility to choose which channels are sampled in what order. The required voltage reference (Vref) to the ADC can be selected from multiple sources, including an on-chip 1.0V reference, the VBAT voltage divided by 2, or external channels. The input voltage range to the ADC shall be between 0V and 2*Vref.

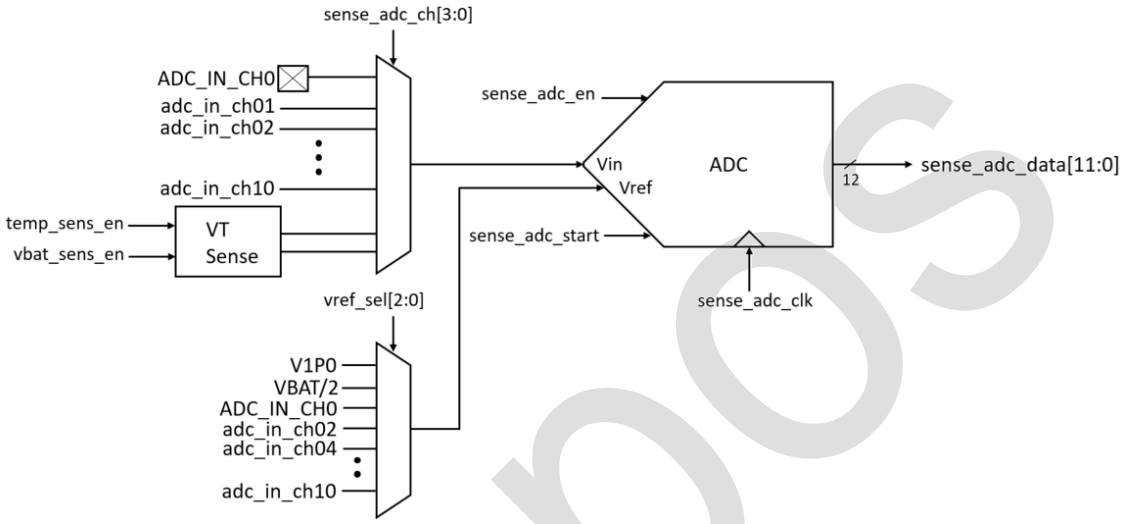


Figure 3.9: Sensor ADC

3.4.2 Hardware Security Engine

The device has two independent sets of cryptographic engines. Each set comprise of hardware accelerator to compute AES, SHA and ECC algorithms. One set of such engine will be used for implementing Bluetooth low energy enhanced security protocol in link layer and the other set can be used by user for application that requires strong security system implementation.

The AES module implements AES encryption and decryption algorithm as defined by the NIST FIPS Publication 197. The features supported by this block are:

- Key length supported are 128b, 192b and 256b and is configurable.
- The authentication modes being supported are XCBC, F8, CMAC, CCM, CBC, CTR and ECB mode.

The SHA module implements hash algorithm and supports SHA-1 and SHA-2.

The ECC module implements ECC encryption and decryption algorithm. The key length supported are 128b, 192b and 256 bits.

3.4.3 Audio ADPCM and Resampling Engines

The device has an ADPCM and audio resampling rate conversion (SRC) engines which can be used to support and develop wireless voice and audio applications.

The audio engine takes the audio data input from either PDM or I2S interfaced microphone then do the ADPCM encoding and wrapper for transmission through radio interface as shown in Figure 3.10.

The received ADPCM coded data through radio interface can also be passed to the ADPCM decoding, and the be played through the Sigma-Delta DAC (SDAC) or I2S as shown in Figure 3.11.

The device's audio SRC can be also to be used for direct PCM sample rate conversion (such as conversion for audio between sampling rate 44.1KHz and 48KHz) as shown in Figure 3.12.

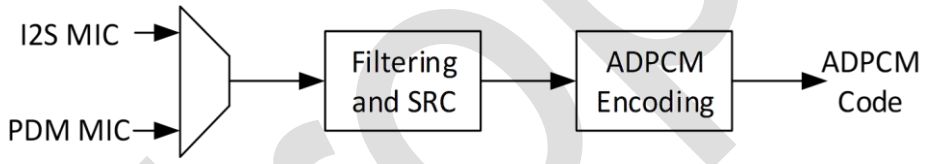


Figure 3.10: ADPCM encoding

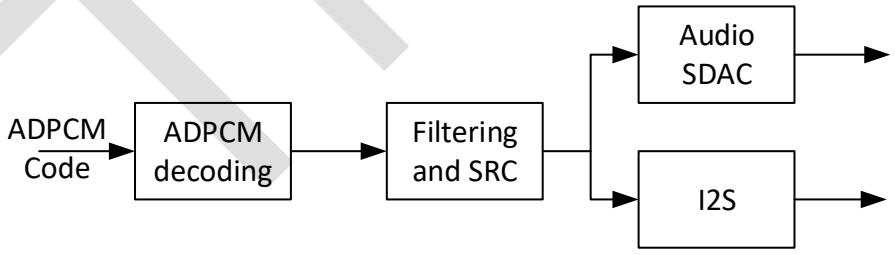


Figure 3.11: ADPCM decoding

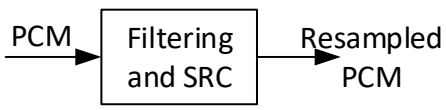


Figure 3.12: Audio SRC

3.4.4 Hardware Math Accelerator Engine

The device has a hardware math accelerator engine (HMAE) which supports various float point (IEEE 754 32-bit single precision) matrix operations. The HMAE includes a floating-point computation unit (FCU), a hardware controller and memory banks associated with the FCU for calculated data/result storage. The FCU comprises a single floating-point operation including addition, multiplication, multiplication-add-accumulate (MAC) and division. The controller can be programmed to use the FCU and dedicated memory banks to perform various matrix math operations and matrix data copying and clearing operations as listed below:

- Matrix addition
- Matrix subtraction
- Matrix multiplication
- Matrix inversion
- Scaling a matrix by a scalar
- Copying a matrix
- Initialize a matrix to zero
- Solving linear equations

The HMAE has an instruction set of 8 instructions to support the above matrix operations. Multiple instructions can be programmed once, and the hardware can perform these instructions sequentially without any software intervention.

The HMAE can have wide applications such as audio compression, audio de-compression and multi-sensor data fusion, for example, the HMAE can be programmed to perform Kalman filtering algorithm which is widely-used for data fusion and processing for Inertial Motion Unit (IMU) sensors.

3.4.5 Keyboard Controller

The device has a keyboard controller module that scan through the columns or rows to identify each key's row/column index. User can define the scan interval and scan through all columns/rows every 0.5, 1, 2 or 4 milliseconds.

Every time after the scan, if any key status has been updated, an interrupt will be generated to notify the CPU. At the same time, following information will be stored in the status registers:

1 bit (press/release)	1 bit (multi-key event)	28 bits (X/Y index) of the key

Table 3.1: Key information register format

The first bit indicates if the key is pressed or released during the scan. The second bit indicates if the multi-key event happens (used to support multiple key pressed/released at the same time). If this bit is asserted, the second status register (same format as the first one) will be populated. If this bit in the second register is also set, the third register will be populated, and so on. At most 4 key status registers will be stored. The last field in the registers is used for column/row index of the key. The number of GPIO's used for columns and rows can be configured through control registers. The number of regular keys and special keys (such as shift, control, alt, home, end, etc.) can be configured through control register and maximal number of supported keys is 108.

Based on the control registers setting, the de-bounce filter can filter out glitches in the range of 0 (debounce feature disabled) to 63 milliseconds (in the step of 1ms). The press and release de-bounce filer can have different glitch filtering time value.

All keyboard interrupt will be listed as parallel I/O ports as a standard interrupt controller (including pulse-to-level conversion, masks, clears features) will be used to combine these interrupts to a single interrupt to CPU. All keyboard control and status registers will be used to convert these signals to control/status registers accessible through APB interface to CPU.

3.4.6 Quadrature Decoder

The device has a Quadrature Decoder with which user can interface the device to a mechanical to electronical rotary device such as servo motor, volume control wheels and PC mice etc. The decoded quadrature signals are used as data input to system to determine the absolute or relative position of the rotary device.

The quadrature decoder comprises of Signal_A, Signal_B and Signal_LED as interface pins to external rotary device. Signal_A and Signal_B are input signals from external quadrature encoder to indicate movement of the rotary device. Signal_LED is an optional output signal to external quadrature encoder and will be asserted a few microseconds (defined through control registers) before the sampling and deasserted immediately after Signal_A, Signal_B values are being sampled by the decoder.

An optional de-bounce filter can be enabled. The Signal_A and Signal_B values are only valid if their values are constants during the de-bounce filter window (which is the same length as the sampling interval). If there is value change in the de-bounce filter

window, the Signal_A/Signal_B value will be ignored and keep the same values as the previous sampling. When the de-bounce filter and Signal_LED are enabled, the Signal_LED will keep asserted during the de-bounce filter window and the Signal_A and Signal_B values are kept being sampled.

3.5 Peripherals

3.5.1 I2C

I2C is a simple two-wire bus with a software defined protocol for system control and peripherals. It has a serial data (SDA) and a serial clock (SCL). The device has two independent I2C interfaces (package dependent). The maximum I2C clock rate being supported is 1MHkz.

I2C can be configured to operate in either master or slave mode. User has the flexibility to determine and program the slave I2C address. It has 7bit addressing. The slave address is transferred in the first byte after the Start condition. The first seven bits of the byte comprise the slave address with the eighth bit indicating R/W flag (“1” for read and “0” for write). It supports bulk transmit mode.

The I2C has access to the DMA Controller and the data can be moved between CPU memory and peripheral buffer through DMA.

3.5.2 SPI

SPI is a four-wire serial peripheral interface bus commonly used to send data between microcontroller and peripherals. It comprises a clock (SCK) and data lines (MOSI, MISO) along with a chip select line (SS).

The device has two SPI interfaces. They both can be configured to operate on either master mode or slave mode. In master operation mode, the maximum clock rate supported is 16MHz. In the master mode, the device can support up to 4 independent slaves using different SS line while sharing the same SCK, MOSI and MISO lines. It may also support dual-SPI and quad-SPI mode operation in the master mode to increase the throughput.

In the slave mode, the device can operate on SCK clock rate of no higher than 4MHz.

SPI has access to DMA Controller and the data can be moved between CPU memory and SPI peripheral buffer through DMA.

3.5.3 UART

The device includes two UART cores which supports universal asynchronous transmitter/receiver function and support programmable baud rate up to 2Mbps. The two UART cores are time-multiplexed to 4 UART interfaces (package dependent).

The UART has built-in 16bytes of transmit and receive data FIFO and support auto flow control.

The UART has access to the DMA Controller and the data can be moved between CPU memory and UART buffer FIFO buffer through DMA.

3.5.4 WDT

The device has a WDT (Watch Dog Timer). User can use it for monitoring of system malfunction by setting a predefined time-out register in the block. It is also possible to output pre-programmed PWM waveform when the WDT expires. The WDT timer may also output a level signal when the timer expires.

3.5.5 Counter/Timer/PWM

The device has one 32bit counter which run on the 32MHz XO clock (or divided version of the 32MHz), one 32KHz 32bit counter, and 4 flexibly configurable counters.

The 4 flexibly configurable counters can be used to capture values (and the time duration) of the external slow signals. They can also be used to send signals out based on the configuration registers. They can be used for Infrared remote control (including learning and transmitting) and ISO-7816 protocol. They can also be used for other features such as frequency estimate of external signals, clock generation, delay timing, etc. They can also be chained together to create more complicated signals.

The device has two Sleep Mode Timers. Both can be used by user for implementing Timer functionality in a lower power fashion without waking up the CPU until Sleep Timer Event expires. The clock source for the Sleep Mode Timer can be either from internal RC 32KHz clock or external RTC 32.768KHz clock.

The device has five Pulse Width Modulators (PWMs) with programmable output frequency and duty cycle.

The clock source can be from 2MHz up to 32MHz which will provide high resolution of output frequency.

3.5.6 PDM

The device has a PDM interface which can convey audio data digitally over a CLK (clock)/PDM (PDM bit stream) pair. The device supports both mono stream and stereo stream of input from an external PDM peripheral with multiple PDM clock rate support from 160KHz to 5.12MHz. The PDM bit stream is clocked at a single edge (selectable) for mono stream or clocked at both edges for stereo stream. After filtering and down-sampling, 16-bit PCM stream will be generated which can be further converted to 4-bit ADPCM format.

3.5.7 I2S

The I2S bus is a simple three-wire serial bus protocol used for connecting digital audio devices together. It has SCK (bit clock), WS (Word Select) and SD (serial multiplexed data line). It supports to operate on either master or slave mode. In master I2S mode, the WS clock rate supported are 7.8125KHz, 8KHz, 15.625KHz, 31.25KHz and 46.875KHz. WS clock rate by default is 15.625KHz. The SCK clock supports from a few hundred KHz to 3.2MHz.

The device has two I2S interface. One is master I2S and the other is slave I2S. Both of the I2S cores support bi-directional data transfer.

The I2S has access to DMA Controller and the data can be moved between CPU memory and I2S data memory through DMA.

3.5.8 GPIO and Analog I/O

The device supports up to 31 GPIOs (package dependent) and a dedicated analog input pin (package dependent). There are two types of GPIOs: mixed signal GPIOs and digital general purpose IOs. A mixed signal GPIO can be configured as a digital GPIO or be configured as an analog signal input pin for Senor ADC.

Each GPIO has a programable pullup or pulldown resistor when it is in digital input mode and has a 2- level programmable output driving strength options.

Each GPIO can be configured as a wakeup pin, and the polarity of each wakeup signal can be programmable to “high” or “low”.

The device supports GPIOs' state retention during sleep.

All GPIOs support asynchronous interrupts. They can be configured as interrupt sources to the ARM core. Multiple of GPIOs' inputs can be grouped together to form a single interrupt. For each GPIO's input, we can configure its polarity, and its mask.

When Chip_En (chip enable) is low, the device is in shutdown mode and all the GPIO(s) are in high Z output state. When the chip is enabled, all the GPIOs are in input mode by default. After boot, the SW may program the GPIOs as appropriate modes (like input/output/high Z state or analog input).

3.5.9 Programing and Debugging Interface

Debug and trace functions are integrated into the device. Serial Wire Debug (SWD) and JTAG (Trace functions) are supported.

Note that SWD and JTAG will be disabled once an efuse bit (the JLINK disable bit) is programmed to be 1, and there will be no access allowed by and from external debugging tools.

3.5.10 User Software Copyright Protection and Secure Boot

Often, for a system with an external flash memory, there are two concerns. The first concern is to how to protect the IPs on the flash. To protect IPs on an external flash, one of popular approaches is to encrypt the code. The second concern is that we need to make sure the image on the flash is an authenticate image. To resolve the second concern, secure booting is required.

The device supports flash encryption and secure booting which can be used to protect user's IP and authenticate the image before it is executed.

3.5.11 User Software Copyright Protection

The device has a dedicated encryption engine to protect user's software intellectual property. It supports secure file transferring from a programmer to the device as shown in Figure 3.13. When a programmer tries to program the device's external flash, the program and the device's boot rom can negotiate a shared secret key through ECDH (Elliptic-curve Diffie-Hellman) key exchange agreement. The secret key can then be used to encrypt the

image file when transferring from the programmer to the device. The encryption is based on AES-256.

TSPA4C500x has dedicated random number generator. Each time it negotiates a key with a programmer, it uses a different random number. Thus, the keys will be different for different devices at different times.

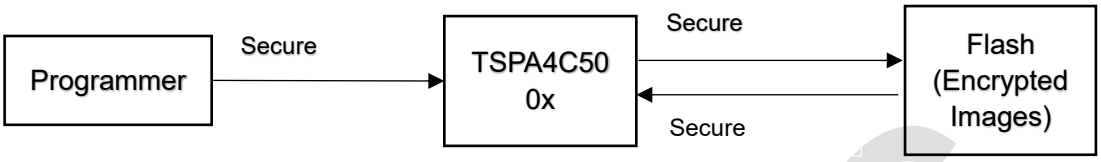


Figure 3.13: Secure Software Copyright Protection

The firmware image file stored on the external flash memory can be configured to be encrypted or unencrypted fashion. If choose to be encrypted, when the device's boot rom gets an encrypted image from the programmer, it first decrypts the image file, and then re-encrypts the image using different key generated through secure programming key generator engine. The newly encrypted image will be programmed to the external flash. Such procedure is being defined as secure programing.

Two types of flash encryption are supported: One is AES-256 encryption. When executing the AES-256 encrypted code, the boot rom will first decrypt the encrypted code using a secret key tied with device's unique ID and put the decrypted code on the device's internal RAM. Another type of encryption is Proprietary Real-Time Encryption (PRTE) which can be decrypted on real-time code execution. An image can be configured to be partly AES-256 encrypted, partly PRTE encrypted, or partly non-encrypted. The encryption keys are tied with the device's unique ID. Thus, the same encrypted code will not be executed on two different devices. We call such code execution on the device secure executing.

3.5.12 Secure Boot

The device supports secure boot based on user's choice. To support secure boot, a firmware image needs to be signed by an encrypted signature (called certificate) attached with that firmware image, as shown in Figure 3.14. During cold boot, the boot rom authenticate the signature. If the authentication fails, the boot rom stops the booting process. TSPA4C500x has dedicated hardware engine and boot rom code to support secure boot.

As shown in Figure 3.14 to support secure boot, a signature must be generated using certain hash engine such as SHA-2. The signature is then encrypted by using ECC (elliptic curve cryptography) encryption. The encrypted signature is a certificate. That certificate will be attached to the image and be programmed into TSPA4C500x's external flash memory. The signature is encrypted by using a private key. The corresponding public key shall be programmed into the TSPA4C500x's internal efuse memory, and the efuse can be configured to lock the public key so that it cannot be modified or altered.

During cold boot, the boot rom hashes the image on the flash memory to calculate its signature. Then, the boot rom uses the ECDSA (Elliptic Curve Digital Algorithm) to authenticate and verify the signature based on the certificate, and the public key. If the verification process passes through, the boot rom will boot the image.

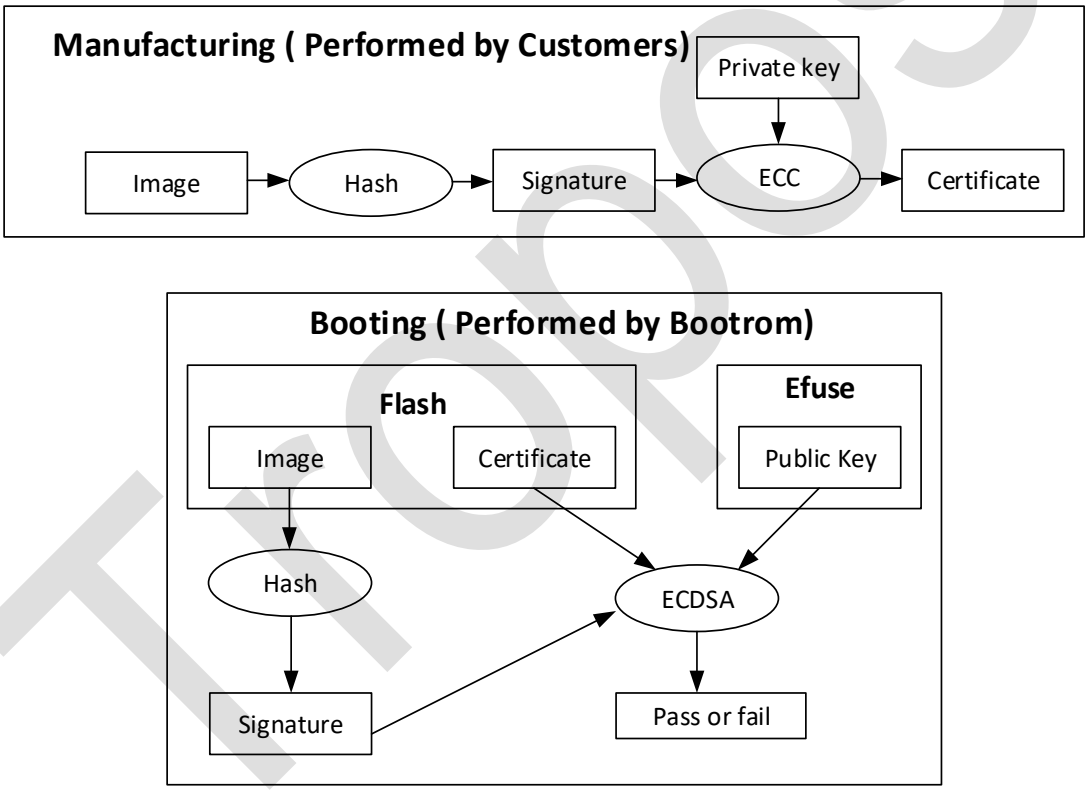


Figure 3.14: Secure Boot

4 Electronical Characteristics

There are voltage ranges where different VDDIO levels apply. The reason for this separation is for the IO drivers whose drive strength is directly proportional to the IO supply voltage. In the TSPA4C500x product, there is a large gap in the IO supply voltage range (1.8 to 3.6v). A guarantee on drive strength across this voltage range would be intolerable to most vendors who only use a subsection of the IO supply range. As such, these voltages are segmented into three manageable sections referenced as VDDIOL, VDDIOM, and VDDIOH in tables listed in this document.

4.1 Absolute Maximum Ratings

The values listed in this section are ratings that can be peaked by the device, but not sustained without causing irreparable damage to the device.

Symbol	Description	Min.	Max.	Unit
VDDIO	I/O Supply Voltage	-0.3	5	V
VBAT	Battery Supply Voltage	-0.3	5	
VIN(1)	All Digital GPIO pins	-0.3	VDDIO	
VAIN1(2)	Analog HV Input Voltage (CHIP_EN, ADC_IN)	-0.3	VBAT	
VAIN2(2)	Analog LV Input Voltage (XO_N, XO_P, RTC_XO_N, RTC_XO_P)	-0.3	2	
VTRX(3)	VDD_RF_2G4, VDD_VCO_2G4, VDD_PLL, VDD_AMS	-0.3	2	
VRF	Input RF Level (RF_TRX_2G4)		+5	dBm
TA	Storage Temperature	-65	150	C

Notes:

1. VIN corresponds to all the digital pins.
2. VAIN corresponds to all the analog pins.
3. VTRX corresponds to all TRX supply voltages

4.2 Recommended Operating Conditions

Symbol	Characteristics	Min.	Typ.	Max.	Unit
VDDIO	I/O Supply Voltage	1.7	3	3.6	V
VBAT	Battery Supply Voltage	1.7	3	3.6	
	Operation Temperature	-40		85	C

Table 4.1: Recommended Operating Conditions

4.3 GPIO PAD Characteristics

Measured at the following condition: Ta = 25C, VBAT=VDDIO=3.V, L=4.7uH, C=4.7uF, unless otherwise noted.

Symbol	Characteristics	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage			0.3*VDDIO	V
V_{IH}	Input High Voltage	0.7*VDDIO			
V_{OL}	Output Low Voltage			0.4V	
V_{OH}	Output High Voltage	VDDIO-0.4V			
I_{OH}	Output High Drive Current		4		mA
I_{OS}	Output Standard Drive Current		4		
t_{LH} / t_{HL} (standard drive)	Rising time/Falling time @standard drive with 12pf load 10%~90%			4	ns
t_{LH} / t_{HL} (high drive)	Rising time/Falling time @high drive with 12pf load 10%~90%			3	ns
R_{PU}	GPIO Pull-up resistance		60K		Ohm
R_{PD}	GPIO Pull-down resistance		60K		Ohm

Table 4.2: DC Characteristics for GPIO Pads

4.4 Buck Converter Characteristics

Measured at the following condition: Ta = 25C, VBAT=VDDIO=3.V, L=4.7uH, C=4.7uF, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output current capacity	0	15	30	mA
	External capacitor range	2	4.7	20	uF
	External inductor range	2	4.7	10	uH
	VBAT Input Range	1.7	3	3.6	V
	Output voltage range	1	1.2	1.4	V
	Efficiency		85		%
	Startup Time		400		us
	Overshoot at startup		0		V

Table 4.3: Buck Converter Characteristics

4.5 11-bit SAR ADC Characteristics

Measured at the following condition: Ta=25C, VBAT=VDDIO=3.0V, VREF=On-chip V1P0, unless otherwise noted.

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Physical bits			11		Bits
ENOB	100Ksps		9.7		Bits
	50Ksps		10.3		Bits
SINAD	100Ksps		60.0		dB
	50Ksps		63.3		dB
Current from VBAT	100Ksps		123		uA
	50Ksps		122		uA
Current from 1.2V VDD	100Ksps		900		nA
	50Ksps		460		nA
Conversion latency		13			Clock cycles
Conversion Rate			50	1000	Ksps
INL		-2		2	LSB
DNL		-1		1	LSB
VREF	Select by register control: External or internal		1.0	VBAT/2	V
Input Voltage range		0		2*VREF	V
Input channels				11	
Input signaling	Single-ended				

Table 4.4: ADC Characteristics

4.6 VBAT Monitoring Characteristics

Measured at the following condition: Ta=25C, VBAT=VDDIO=3.0V, VREF=On-chip V1P0, unless otherwise noted.

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V1P0 as reference		5		mV/LSB
Range	Input to ADC = 0.4*VBAT. Input range of ADC is 0V ~ 2V (FS)	1.7		3.6	V

Table 4.5: VBAT Monitoring Characteristics

4.7 Device Temperature Monitoring Characteristics

Measured at the following condition: Ta=25C, VBAT=VDDIO=3.0V, VREF=On-chip V1P0, unless otherwise noted.

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V1P0 as reference		0.5		C/LSB
Range		-40		125	C

Table 4.6: Device Temperature Monitoring Characteristics

4.8 32KHz RC Oscillator Characteristics

Measured at the following condition: Ta = 25C, VBAT=VDDIO=3.0V, unless otherwise noted.

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	Calibrated with code: osc_32KHz_rc_ibg=TBD, osc_32KHz_rc-ictat=TBD		32		KHz
Temperature coefficient	Calibrated with code: osc_32KHz_rc_ibg=TBD, osc_32KHz_rc-ictat=TBD		TBD		ppm/C

Table 4.7: 32KHz RC Oscillator Characteristics

4.9 32MHz Crystal Oscillator Characteristics

Measured at the following condition: Ta = 25C, VBAT=VDDIO=3.0V, unless otherwise noted.

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Oscillation frequency			32		MHz
Crystal frequency tolerance		-40		40	ppm
ESR (Equivalent Serial Resistor)			60	200	Ohm
Lm (Motional Inductance)			17	35	mH
Cm (Motion Capacitance)			2.2	3	pF
Cl crystal load capacitance	Differential		6	10	pF
C0			0.7	2	pF
On-chip Cl	Differential, programmable in 0.5pF steps	0.5		8	pF
Start-up Time			500	1000	us

Table 4.8: 32MHz Crystal Oscillator Characteristics

4.10 32MHz RC Oscillator Characteristics

Measured at the following condition: Ta = 25C, VBAT=VDDIO=3.0V, unless otherwise noted.

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	Programmable with 1MHz resolution	16	32	48	MHz
Temperature coefficient			TBD		%/C

Table 4.9: 32MHz RC Oscillator Characteristics

4.11 32.768KHz RTC Oscillator Characteristics

Measured at the following condition: Ta = 25C, VBAT=VDDIO=3.0V, unless otherwise noted.

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Oscillation frequency			32.768		KHz
Crystal frequency tolerance	Including aging and temp. drift	-500		500	ppm
ESR (Equivalent Serial Resistor)			30	100	KOhm
On-chip CI	Differential, programmable in 0.5pF steps	0.5		16	pF
CI crystal load capacitance	Differential	4	7	12	pF

Table 4.10: 32.768KHz RTC Oscillator Characteristics

4.12 RF Performance Characteristics

4.12.1 RF Receiver Performance Characteristics

Measured at: BLE RX 1Mbps mode. Ta = 25C, VBAT = VDDIO = 3.0V, fRF = 2440MHz, unless otherwise noted

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Sensitivity with on-chip DC-DC	Measured at SMA connector, BER=1e-3, maximum current settings		-97		dBm

Table 4.11: RF Receiver Characteristics at 1Mbps

Measured at: BLE RX 2Mbps mode. Ta = 25C, VBAT = VDDIO = 3.0V, fRF = 2440MHz, unless otherwise noted

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Sensitivity with on-chip DC-DC	Measured at SMA connector, BER=1e-3, maximum current settings		-94		dBm

Table 4.12: RF Receiver Characteristics at 2Mbps

4.12.2 RF Transmitter Performance Characteristics

Measured at: BLE TX 1Mbps mode. Ta = 25C, VBAT = VDDIO = 3.0V, fRF = 2440MHz, unless otherwise noted

Parameter	Test Condition	Min.	Typ.	Max.	Unit
TX Output Power		-20		+4	dBm

Table 4.13: RF Transmitter Characteristics at 1Mbps

Measured at: BLE TX 2Mbps mode. Ta = 25C, VBAT = VDDIO = 3.0V, fRF = 2440MHz, unless otherwise noted

Parameter	Test Condition	Min.	Typ.	Max.	Unit
TX Output Power		-20		+4	dBm

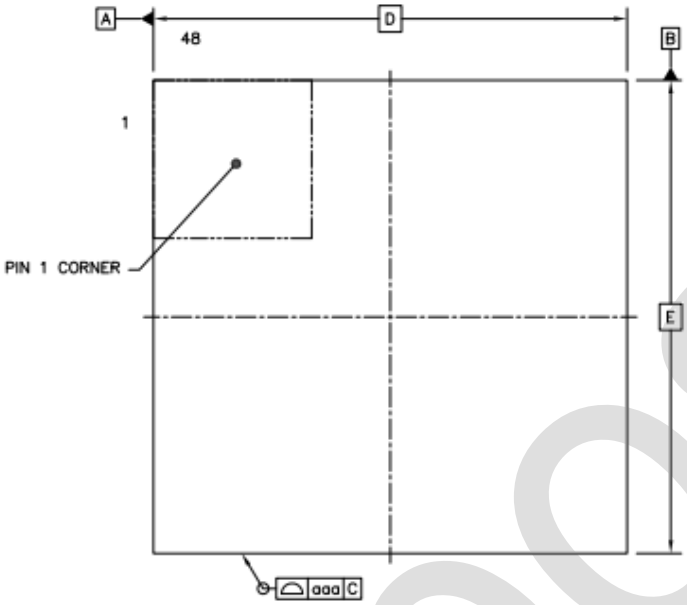
Table 4.14: RF Transmitter Characteristics at 2Mbps

4.13 System Power Consumption

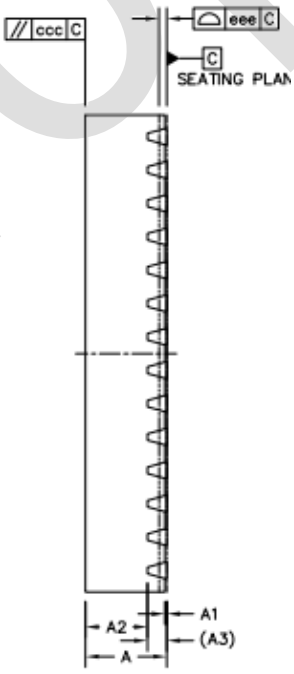
Currents are measured at Ta = 25C, VBAT = VDDIO = 3.0V with internal DC-DC converter enabled, unless otherwise noted.

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
I_VBAT	Battery Current Consumption	Chip disabled, CHIP_EN=0V		20		nA
		Sleep with 32KHz RC and Sleep timer On		500		nA
		Sleep with 32.768KHz RTC, sleep timer on		550		nA
		Sleep with 32.768KHz RTC, sleep timer on, 8KB retention		650		nA
		Sleep with 32.768KHz RTC, sleep timer on, 16KB retention		TBD		
		Sleep with 32.768KHz RTC, sleep timer on, 16KB retention, BOD enabled		TBD		
		Idle; DC-DC powers up core and RAM, 32MHz XO not running		TBD		
		Active; 32MHz running and core running CoreMark		TBD		
I_VDDIO	VDDIO Current Consumption	Chip disabled, CHIP_EN=0V		TBD		
		Chip enabled, CHIP_EN=VDDIO		TBD		

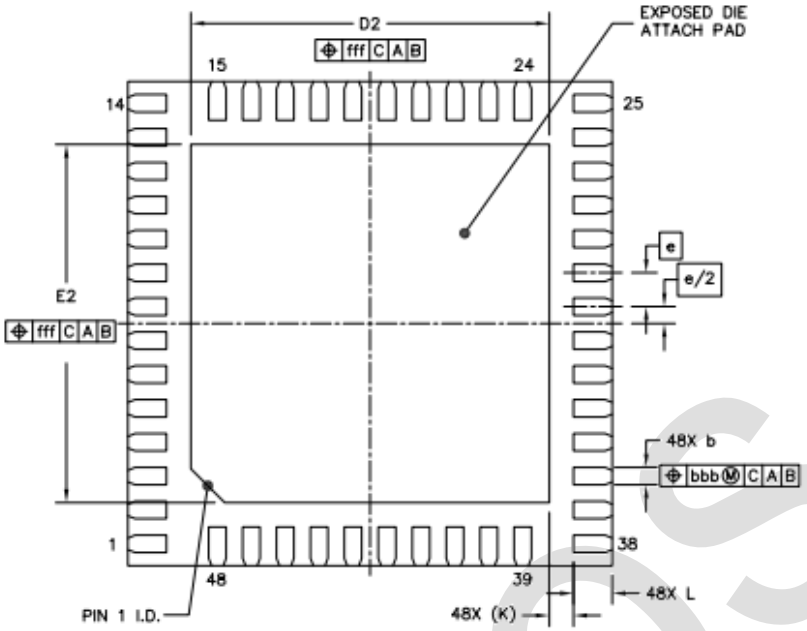
5 Package Outline



TOP VIEW



SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	3.6	3.7	3.8
	Y	E2	3.6	3.7	3.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Figure 5.1: Package outline (QFNWB5×5-48L-J(P0.35T0.85))