HDSC 华大半导体 HUADA SEMICONDUCTOR

32-bit Microcontrollers

Hardware Development Guide for HC 32 F 460 Series

Applicable objects

Series	Product Model
HC32F460	HC32F460JEUA HC32F460JETA HC32F460KEUA HC32F460KETA HC32F460PETB

Table of Contents Table of Contents

1 Abstract

This application note mainly introduces the hardware design based on HC32F460 series chip.

2 Power supply

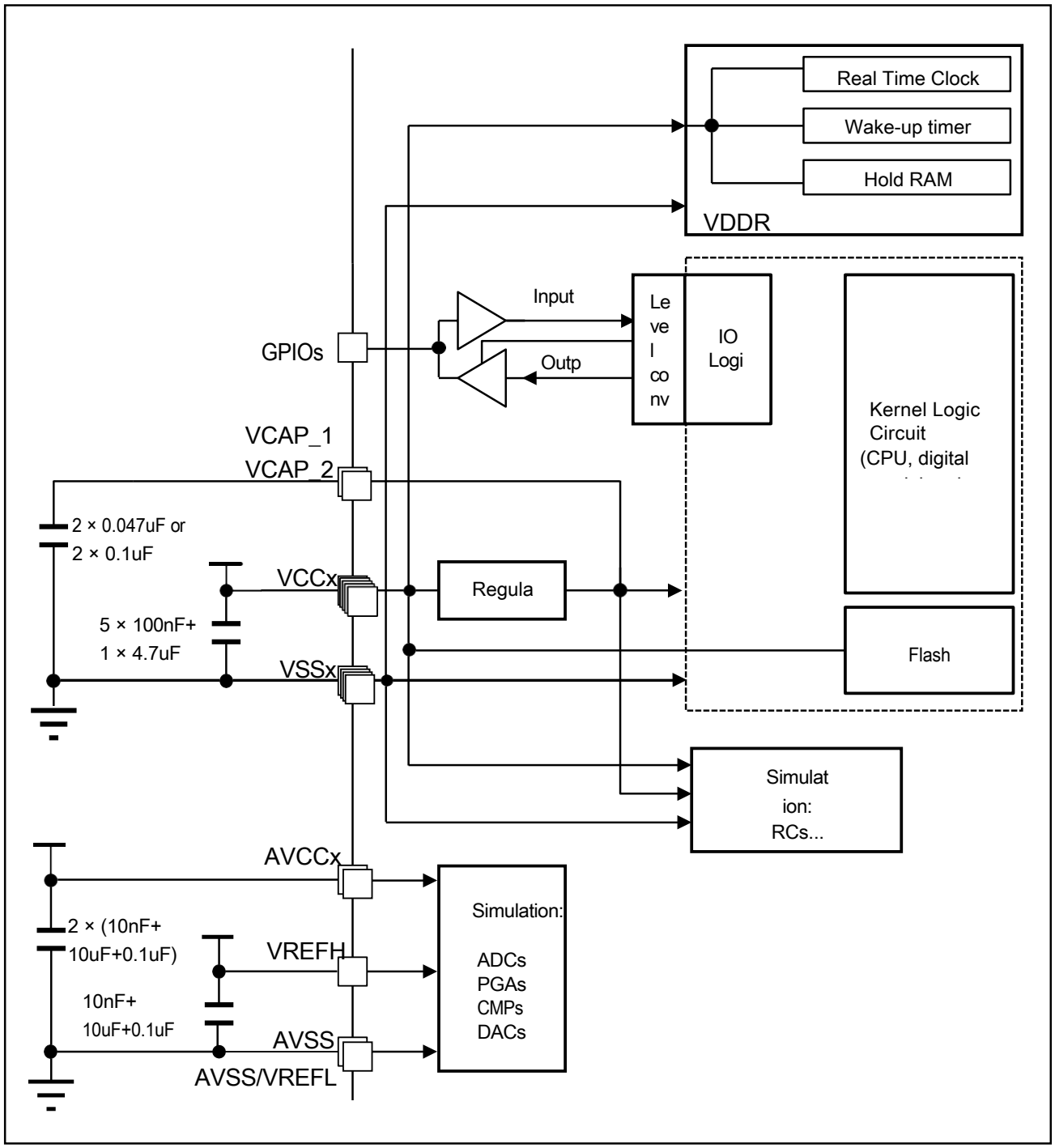


Figure 1 Decoupling Capacitor

* NOTE1: The decoupling capacitor schematic is for 100PIN P/N, for other PIN number P/N, the actual pin configuration is subject to the actual pin configuration.

1. The 4.7uF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS = VSS.
3. Each power pair (e.g. VCC/VSS, AVCC/AVSS ...) must be decoupled using the filtering ceramic capacitors described above. These capacitors must be as close or as low as possible to the appropriate pins under the PCB to ensure proper device operation. It is not recommended to remove the filtering capacitors to reduce PCB size or cost. This may cause the device to operate improperly.
4. The capacitors used in the VCAP_1/VCAP_2 pins of the chip are as follows:
   1) Chips with both VCAP_1 and VCAP_2 pins can use 0.047uF or 0.1uF capacitors per pin (total capacity of 0.094uF or 0.2uF).
   2) Chips with only VCAP_1 pin can use 0.1uF or 0.22uF capacitors.

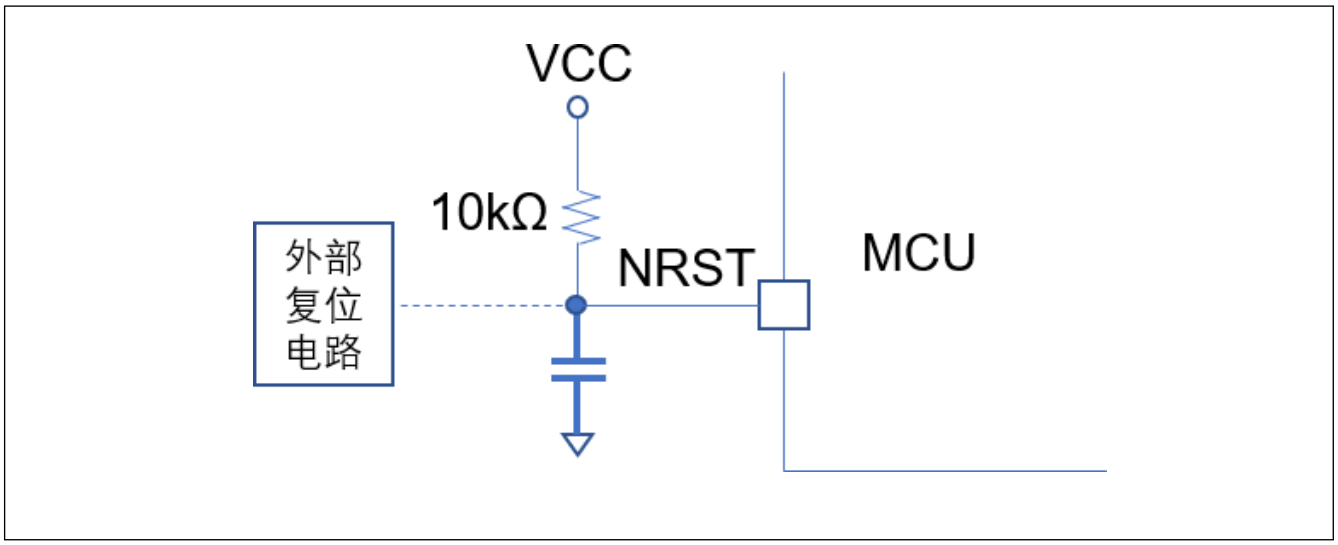
   When waking up from power-down mode, VCAP_1/VCAP_2 needs to be charged during the core voltage build-up. On the one hand, a smaller total VCAP_1/VCAP_2 capacity reduces the charging time and brings fast responsiveness to the application; on the other hand, a larger total VCAP_1/VCAP_2 capacity extends the charging time, but also provides greater electromagnetic compatibility (EMC). The user can choose a larger or smaller capacitance value depending on the EMC and system response speed requirements. The total capacity of VCAP_1/VCAP_2 must match the assignment of the PWR_PWRC3.PDTS bit. If the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, you need to make sure the WR_PWRC3.PDTS bit is cleared before entering the power-down mode.
5. The stability of the main regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin, with the capacitance value CEXT determined according to the stability requirements of the system. The capacitance value CEXT and ESR requirements are as follows:

Table 1 VCAP_1/VCAP_2 Operating Conditions

Symbols	Parameters	Conditions
CEXT	Capacitance value of external capacitor	0.047μF / 0.1μF / 0.22uF

3 Reset

Applications that do not use NRST must pull up NRST to VCC through a resistor (10KΩ recommended). Connecting a capacitor between the NRST pin and



ground (VSS) improves EMC performance with a recommended value of 10nF to 100nF.

Figure 2 NRST Circuit

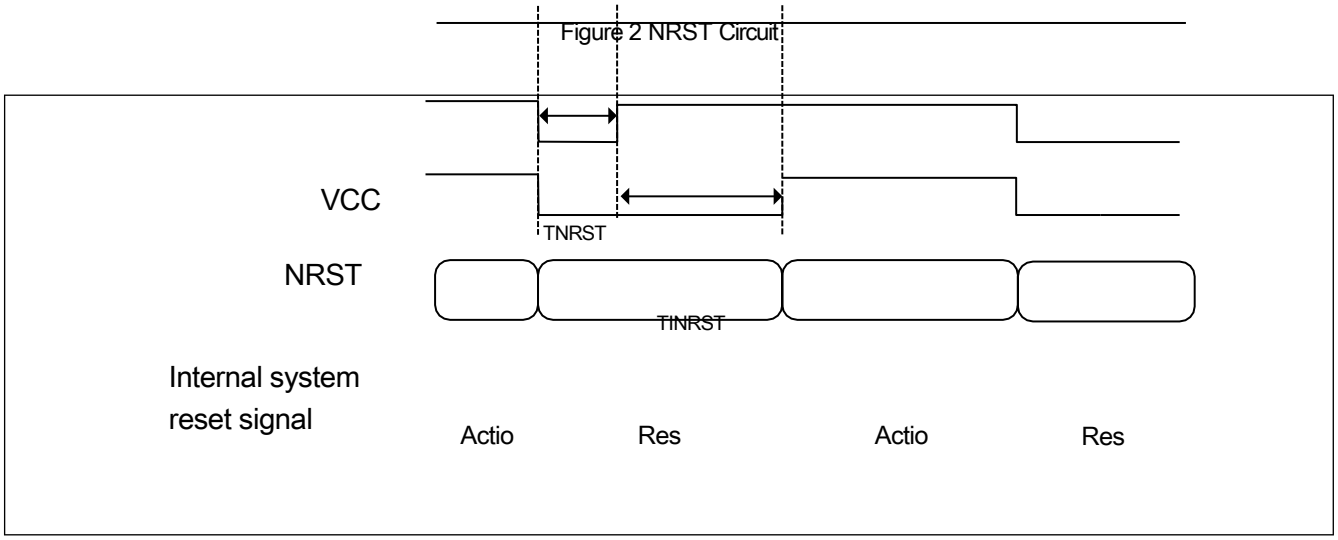


Figure 3 NRST Reset Timing

4 Mode PIN

The mode PIN (PB11/MD) must be pulled up to VCC through a resistor (4.7KΩ recommended).

The PB11/MD user can be used as an input port, but it must remain high while NRST is active (i.e., while NRST is low), otherwise the MCU will mistakenly enter Boot Mode when NRST is released (i.e., when NRST goes high).

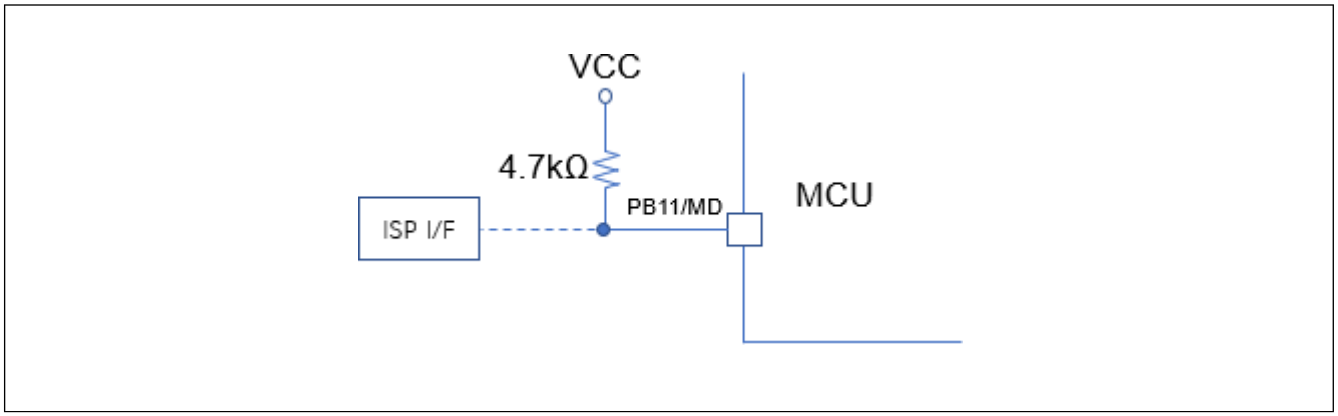


Figure 4 PB11/MD Circuit

5 GPIO

The MCU's GPIO is outputting high through the CMOS PMOS and low through the NMOS. The internal pull-up resistor is also a PMOS, and when the pin is output, the PMOS or NMOS operates in the linear region and its equivalent on-resistance changes with the MCU's VCC. When the MCU operates near the lower voltage limit, the on-resistance changes sharply, and the appearance is that the drive capability drops sharply and the pull-up resistance becomes larger.

5V tolerance means that the MCU's GPIO can accept a maximum level input of 5.5V, not the maximum operating voltage of the chip

The maximum operating voltage of the chip is 3.6V.

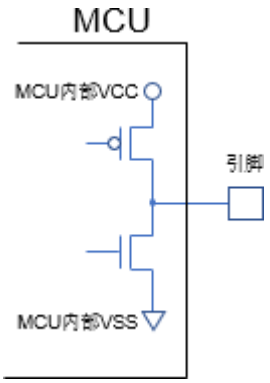


Figure 5 GPIO structure

- The loads that can be driven by the GPIO outputs (individual IO drive current, sigma drive current), as well as the level range of the inputs, must meet the range specified in the Datasheet, otherwise irreversible damage can be caused to the chip.
- When the GPIO output is flipped (L→H, H→L), there will be a short switching current inside the MCU, resulting in noise on VCC and VSS, which will cause the MCU to misunderstand the pin level in a serious situation, so the output load must be within the range specified in the Datasheet.
- When the GPIO outputs with AD analog inputs are flipped, it will cause noise on VCCA, VSSA and affect the accuracy of ADC conversion, so these GPIO outputs should be avoided when ADC conversion is done.
- USB multiplexed GPIOs (PA11/USBFS_DP, PA12/USBFS_DM) do not support 5V tolerance input, 3.6V maximum input.

- The F460 series has a unique countermeasure circuit, refer to the manual register description [General Control Register (PCRxy)].

6 Reference schematic

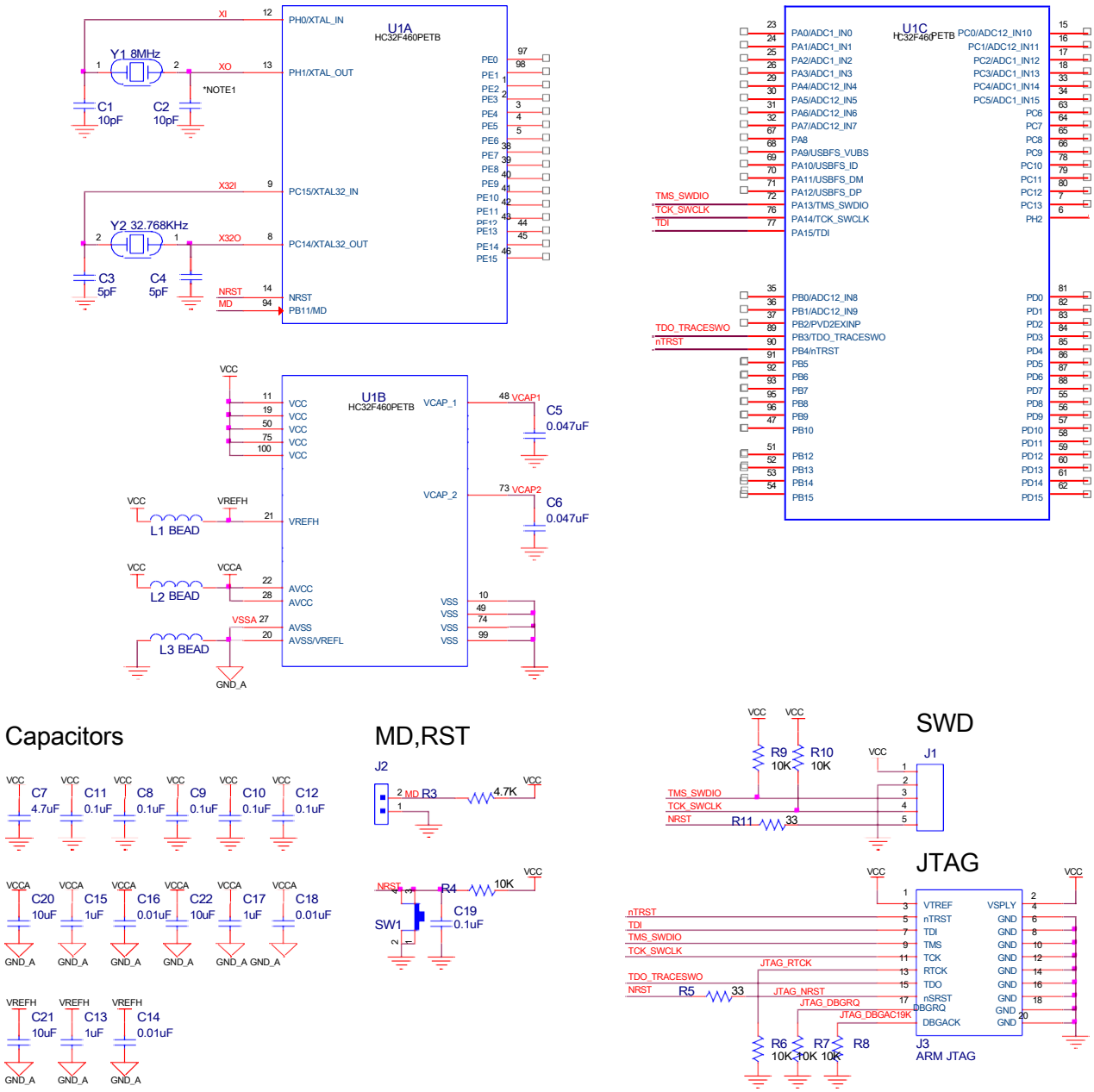


Figure 6 Reference schematic

* NOTE1: The load capacitance of the crystal circuit needs to be adjusted according to the user's system

* NOTE2: The reference schematic is for 100PIN P/N, for other PIN numbers P/N is subject to actual pin configuration.

7 Summary

The above section briefly introduces the hardware related knowledge of HC32F460 series, and explains the application notes of power, reset, mode, GPIO, and provides the reference schematic diagram, which users can design according to the actual needs in the development.

8 Version Information & Contact

Date	Versions	Modify records
2019/2/25	Rev1.0	Initial Release
2019/6/11	Rev1.1	Update of the following information: ①Chapter "Power Supplies" ②Chapter "Reference Schematics

If you have any comments or suggestions in the process of purchase and use, please feel free to contact us.

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