XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32F460 Series

32-bit ARM® Cortex®-M4 microcontrollers

Data Sheet

Rev1.42 September 2022

Product Features

ARM Cortex-M4 32bit MCU+FPU, 250DMIPS, up to 512KB Flash, 192KB SRAM, USB FS (Device/Host), 14 Timers, 2 ADCs, 1 PGA, 3 CMPs, 20 communication interfaces

- **ARMv7-M architecture 32bit Cortex-M4 CPU with integrated FPU, MPU, DSP with SIMD instruction support, and CoreSight standard debug unit. Maximum operating frequency of 200MHz, Flash acceleration unit for 0-wait program execution, and 250DMIPS or 680Coremarks of computing performance**
- **Built-in memory**
  - Maximum 512KByte Flash memory with security protection and data encryption*1
  - Up to 192KByte of SRAM, including 32KByte of 200MHz single-cycle access high-speed RAM, 4KByte of Retention RAM
- **Power, clock, reset management**

  - System power supply (Vcc) 1.8-3.6V
  - 6 independent clock sources: external master clock crystal (4-25MHz), external sub crystal (32.768kHz), internal high speed RC (16/20MHz), internal medium speed RC (8MHz), internal low speed RC (32kHz), internal WDT dedicated RC (10kHz)
  - 14 reset sources including Power On Reset (POR), Low Voltage Detect Reset (LVDR), and Port Reset (PDR), each with individual flag bits
- **Low power operation**
  - Peripheral functions can be turned off or on independently
  - Three low-power modes: Sleep, Stop, and Power down modes
  - Run mode and Sleep mode support switching between super high speed mode, high speed mode and super low speed mode
  - Standby power consumption: Stop mode typ.90uA@25°C, Power down mode down to 1.8uA@25°C
  - Power down mode, supports 16 port wake-up, ultra-low power RTC operation, 4KByte SRAM for data retention
  - Standby fast wake-up, Stop mode wake-up as fast as 2us, Power down mode wake-up as fast as 20us
- **Peripheral operation support system significantly reduces CPU processing load**
  - 8-channel dual host DMAC
  - DMAC for USBFS
  - Data Computing Unit (DCU)
  - Support peripheral event inter-triggering (AOS)
- **High Performance Simulation**
  - 2 independent 12bit 2MSPS ADCs
  - 1 programmable gain amplifier (PGA)
  - 3 independent voltage comparators (CMP), supporting 2 internal reference voltages
  - 1 on-chip temperature sensor (OTS)

- **Timer**
  - 3 multifunctional 16bit PWM timers (Timer6)
  - 3 x 16bit Motor PWM Timer (Timer4)
  - 6 x 16bit general purpose timers (TimerA)
  - 2 16bit base timers (Timer0)
- **Maximum 83 GPIOs**
  - CPU single-cycle access, 100MHz maximum output
  - Maximum 81 5V-tolerant IO
- **Up to 20 communication interfaces**
  - 3 I2C, SMBus protocol support
  - 4 USARTs, supports ISO7816-3 protocol
  - 4 SPI
  - 4 I2S, built-in audio PLL supports audio-level sampling accuracy
  - 2 SDIOs supporting SD/MMC/eMMC formats
  - 1 QSPI with 200Mbps high-speed access (XIP)
  - 1 CAN, supports ISO 11898-1 standard protocol
  - 1 USB 2 .0 FS, built-in PHY, Device/Host support
- **Data encryption function**
  - AES/HASH/TRNG
- **Package form:**

  LQFP100 (14×14mm) VFBGA100 (7×7mm) LQFP64 (10×10mm) QFN60 (7×7mm)
  QFN48 (5×5mm) LQFP48 (7×7mm)

*1: For specific specifications of Flash security protection and data encryption, please consult the sales window.

Supported models:

HC32F460PETB-LQFP100	hc32f460pehb-vfbga100
HC32F460KETA-LQFP64	HC32F460KEUA-QFN60TR
HC32F460JETA-LQFP48	HC32F460JEUA-QFN48TR
HC32F460PCTB-LQFP100	HC32F460KCTA-LQFP64
HC32F460JCTA-LQFP48	

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1 Introduction (Overview)

The HC32F460 series is a high-performance MCU based on the ARM® Cortex®-M4 32-bit RISC CPU operating at up to 200 MHz. The Cortex-M4 core integrates a floating-point unit (FPU) and DSP for single-precision floating-point arithmetic operations, supports all ARM single-precision data processing instructions and data types, and supports the full DSP instruction set. The core integrates the MPU unit and overlays the DMAC dedicated MPU unit for secure system operation.

The HC32F460 series integrates high-speed on-chip memory, including up to 512KB of Flash and up to 192KB of SRAM, and integrates a Flash access acceleration unit to enable single-cycle program execution on Flash by the CPU. The polled bus matrix supports multiple bus hosts for simultaneous access to memory and peripherals to improve operational performance. Bus hosts include CPU, DMA, USB dedicated DMA, etc. In addition to the bus matrix, it supports inter-peripheral data transfer, basic arithmetic operations and event triggering, which can significantly reduce the CPU transaction processing load.

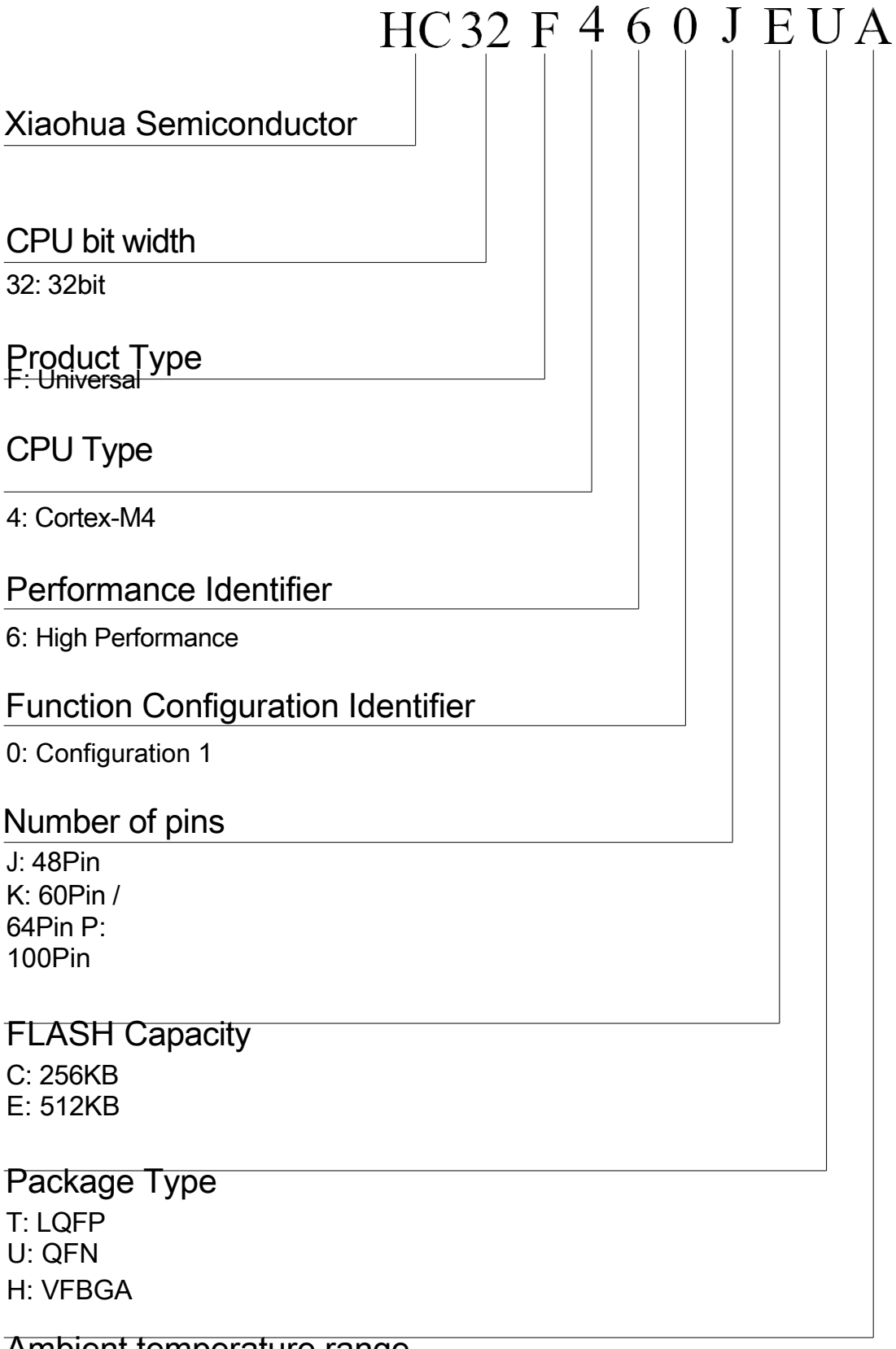
The HC32F460 series integrates a rich set of peripheral functions. It includes two independent 12bit 2MSPS ADCspne gain adjustable PGA, three voltage comparators (CMP) three multi-function 16bit PWM timers (Timer6) supporting 6 complementary PWM outputs, three motor PWM timers (Timer4) supporting 18 complementary PWM outputs, six 16bit general-purpose timers (TimerA) supports three 3-phase quadrature coded inputs and 48 Duty independent configurable PWM outputs, 11 serial communication interfaces
(I2C/UART/SPI)1 QSPI interface, 1 CAN, 4 I2S support audio PLL, 2 SDIO, 1 USB FS Controller with on-chip FS PHY support Device/Host.

The HC32F460 series supports wide voltage range (1.8-3.6V) wide temperature range (-40-105°C) and various low power modes. Run mode and Sleep mode switchable for ultra-high speed mode (≤200MHz) high speed mode (≤168MHz) and ultra-low speed mode
(≤8MHz) Supports fast wake-up in low-power mode, up to 2us for STOP mode and up to 20us for Power Down mode.

Typical Applications

The HC32F460 series is available in 48pin, 64pin, 100pin LQFP packages, 48pin, 60pin QFN packages, and 100pin VFBGA packages for high performance motor inverter control, smart hardware, IoT connectivity modules, etc.

1.1 Model naming rules



1.2 Model Function Comparison Table

Table 1-1 Model Function Comparison Table

Function		Product Model								
		HC32F460PEHB	HC32F460PETB	HC32F460PCTB	HC32F460KETA	HC32F460KCTA	HC32F460JETA	HC32F460JCTA	HC32F460JEUA	HC32F460KEUA
Flash Memory (KB)		512	512	256	512	256	512	256	512	512
Number of pins		100	100	100	64	64	48	48	48	60
Number of GPIOs		83	83	83	52	52	38	38	38	50
Number of 5V Tolerant GPIOs		81	81	81	50	50	36	36	36	48
Package		VFBGA	LQFP						QFN	
Temperature range		-40-105℃			-40-85℃					
Power supply voltage range		1.8 ~ 3.6 V								
OTP (Byte)		960								
SRAM (KB)		192								
DMA		2unit * 4ch								
External port interrupts		EIRQ * 16vec + NMI * 1ch								
Communication Interfaces (The minimum number of IOs required per ch is in parentheses)	UART	4ch (2)								
	SPI	4ch (3)								
	I2C	3ch (2)								
	I2S	4ch (3)								
	CAN	1ch (2)								
	QSPI	1ch (6)								
	SDIO	2ch (3)								
	USB-FS	1ch (2)								
	Timer0	2unit								

	TimerA	6unit		
Timers	Timer4	3unit		
	Timer6	3unit		
	WDT	1ch		
	SWDT	1ch		
	RTC	1ch		
Analog	12bit ADC	2unit, 16ch	2unit, 10ch	2unit.
	PGA	1ch		
	CMP	3ch		

Function	Product Model								
	HC32F460PEHB	HC32F460PETB	HC32F460PCTB	HC32F460KETA	HC32F460KCTA	HC32F460JETA	HC32F460JCTA	HC32F460JEUA	HC32F460KEUA
OTS	√								
AES128	√								
HASH (SHA256)	√								
TRNG	√								
Frequency Monitoring Module (FCM)	√								
Programmable voltage detection function (PVD)	√								
Debugging Interface	SWD								
	JTAG								

1.3 Functional Block Diagram

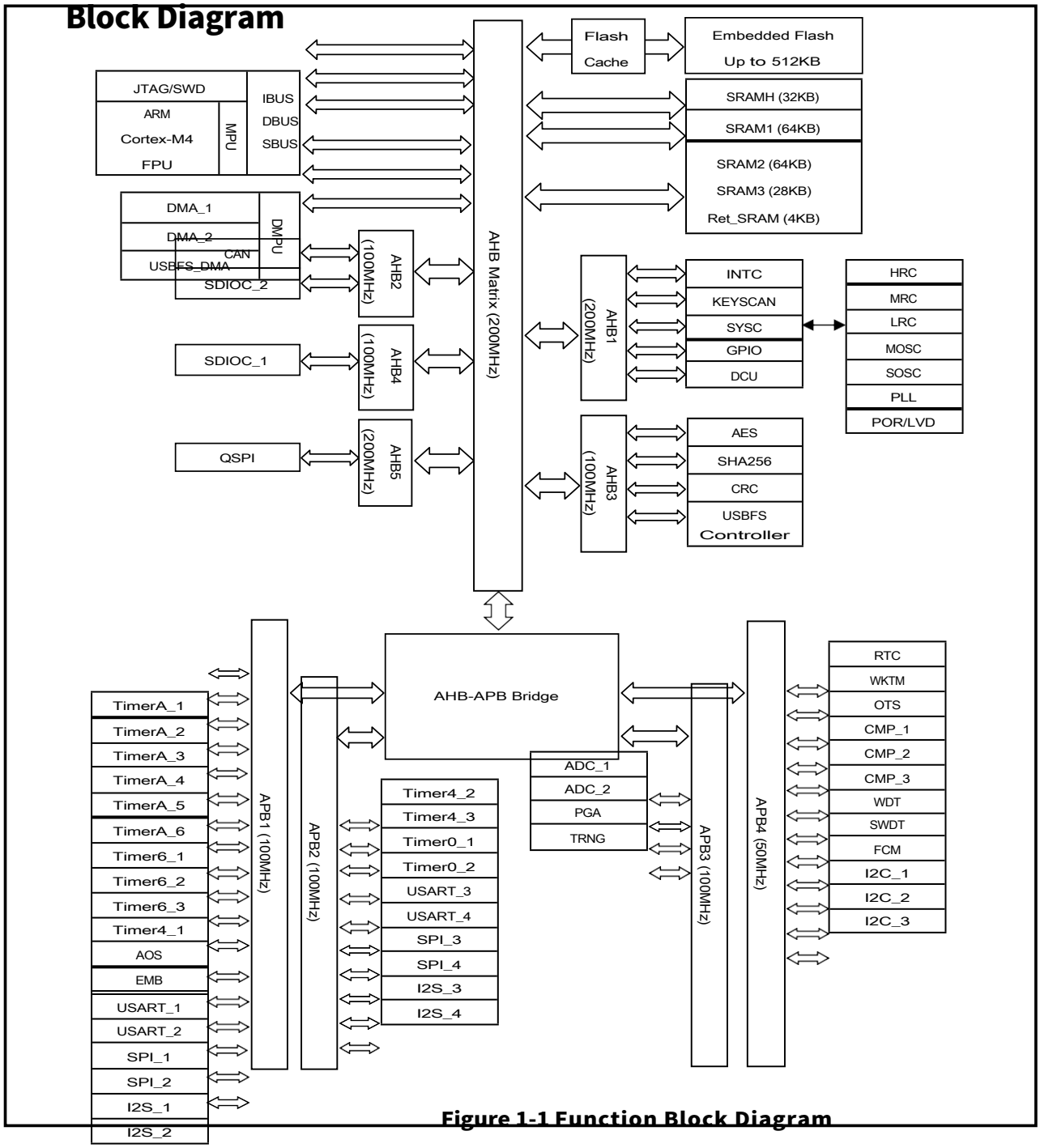


Figure 1-1 Function Block Diagram

1.4 Function Introduction

1.4.1 CPU

The HC32F460 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit lean instruction CPU, providing excellent computing performance and fast interrupt response with low pin count and low power consumption. The CPU supports DSP instructions for efficient signal processing operations and complex algorithms. The single point precision FPU unit avoids instruction saturation and accelerates software development.

1.4.2 Bus Architecture (BUS)

The master system consists of a 32-bit multi-layer AHB bus matrix that

interconnects the following host and slave buses Host Bus

- Cortex-M4F Core CPU-I Bus, CPU-D Bus, CPU-S Bus
- System DMA_1 bus, System DMA_2 bus
- USBFS_DMA Bus

Slave Bus

- Flash ICODE Bus
- Flash DCODE Bus
- Flash MCODE bus (bus for hosts other than the CPU to access Flash)
- SRAMH bus (SRAMH 32kB)
- SRAMA bus (SRAM1 64KB)
- SRAMB bus (SRAM2 64KB, SRAM3 28KB, Ret_SRAM 4KB)
- APB1 Peripheral bus (AOS/EMB/Timers/SPI/USART/I2S)
- APB2 Peripheral Bus (Timers/SPI/USART/I2S)
- APB3 Peripheral Bus (ADC/PGA/TRNG)
- APB4 Peripheral Bus (FCM/WDT/CMP/OTS/RTC/WKTM/I2C)
- AHB1 Peripheral bus (KEYSCAN/INTC/DCU/GPIO/SYSC)
- AHB2 Peripheral Bus (CAN/SDIOC)
- AHB3 Peripheral Bus (AES/HASH/CRC/USB FS)
- AHB4 Peripheral Bus (SDIOC)
- AHB5 Peripheral Bus (QSPI)

With the help of the bus matrix, efficient concurrent access from the host bus to the slave bus is possible.

1.4.3 Reset control (RMU)

The chip is configured with 14 reset methods.

- Power-On Reset (POR)
- NRST Pin Reset (NRST)
- Undervoltage Reset (BOR)
- Programmable Voltage Detect 1 Reset (PVD1R)
- Programmable voltage detection 2 reset (PVD2R)
- Watchdog Reset (WDTR)
- Dedicated watchdog reset (SWDTR)
- Power-down wake-up reset (PDRST)
- Software Reset (SRST)
- MPU Error Reset (MPUR)
- RAM Parity Reset (RAMPR)
- RAMECC reset (RAMECCR)
- Clock abnormal reset (CKFER)
- External high-speed oscillator abnormal stop reset (XTALER)

1.4.4 Clock Control (CMU)

The clock control unit provides clocking functions for a range of frequencies, including: an external high-speed oscillator, an external low-speed oscillator, two PLL clocks, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, a SWDT dedicated internal low-speed oscillator, clock prescaler, clock multiplexing, and clock gating circuitry.

The Clock Control Unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) uses the measurement reference clock to monitor and measure the measurement object clock. An interrupt or reset occurs when the set range is exceeded.

The AHB, APB and Cortex-M4 clocks are all derived from the system clock, which can be sourced from a choice of six clock sources:

1) External high-speed oscillator (XTAL)
2) External low-speed oscillator (XTAL32)
3) MPLL Clock (MPLL)
4) Internal high-speed oscillator (HRC)
5) Internal medium speed oscillator (MRC)
6) Internal low speed oscillator (LRC)

The system clock can run at a maximum clock frequency of 200 MHz. the SWDT has a separate clock source: the SWDT dedicated internal low-speed oscillator (SWDTLRC) The Real Time Clock

(RTC) uses either an external low-speed oscillator or an internal low-speed oscillator as the clock source. 48MHz clock for USB-FS and I2S communication clock can choose system clock, MPLL, UPLL as the clock source.

For each clock source, it can be turned on and off individually. It is recommended to turn off unused clock sources to reduce power consumption.

1.4.5 Power Control (PWC)

The power controller is used to control the power supply, switching, and detection of multiple power domains of the chip in multiple operation modes and low power modes. The power controller consists of a power consumption control logic (PWCL) and a power supply voltage detection unit (PVD).

The chip operates from 1.8 V to 3.6 V. The voltage regulator (LDO) supplies power to the VDD and VDDR domains, and the VDDR voltage regulator (RLDO) supplies power to the VDDR domain during power-down mode. The chip provides three modes of operation: ultra-high-speed, high-speed, and ultra-low-speed, and three low-power modes: sleep, stop, and power-down through the power control logic (PWCL).

The power supply voltage detection unit (PVD) provides power-on reset (POR), power-down reset (PDR), under-voltage reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2), etc. Among them, POR, PDR, BOR control the chip reset action by detecting the VCC voltage. PVD2 generates reset or interrupt by detecting VCC voltage or external input detection voltage, and generates reset or interrupt by register selection.

The VDDR area can maintain power through the RLDO after the chip goes into power-down mode, ensuring that the real-time clock module (RTC), wake-up timer (WKTM) can continue to operate and keep data in the 4KB low-power SRAM (Ret-SRAM). The analog module is equipped with dedicated power supply pins to improve analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip is reset, the hardware circuit will read the FLASH address 0x0000_0400~0x0000_041F (where 0x0000_0408~0x0000_041F is the reserved function address, the 24byte address needs to be set by the user to ensure the chip action is normal) and load the data into the initialization configuration register, the user needs to program or erase the FLASH sector 0 to modify the initialization configuration register. The user needs to program or erase the FLASH sector 0 to modify the initialization configuration register.

1.4.7 Embedded FLASH Interface (EFM)

The FLASH interface provides access to FLASH through the ICODE, DCODE and MCODE buses, which allows programming, sector erase and full erase operations on FLASH; accelerates code execution through instruction prefetch and cache mechanisms.

Main features:

- Maximum 512KByte FLASH space

- I-CODE Bus 16Byte Prefetch
- Shared 64 caches (1Kbyte) on the I-CODE and D-CODE buses
- Provides 960Bbyte One Time Programming Area (OTP)
- Supports low-power read operations
- Support guide exchange function
- Support security protection and data encryption*1

*1: For specific specifications of Flash security protection and data encryption, please consult the sales window.

1.4.8 Internal SRAM (SRAM)

This product comes with 4KB power-down mode hold SRAM (Ret_SRAM) and 188KB system SRAM (SRAMH/SRAM1/SRAM2/SRAM3)

SRAM can be accessed by byte, half-word (16-bit), or full-word (32-bit). Read and write operations are performed at CPU speed, with the possibility of inserting wait cycles.

Ret_SRAM provides 4KB of data retention space in power down mode.

SRAM3 with ECC check (Error Checking and Correcting) ECC check is correcting one and checking two codes, that is, it can correct one error and check two errors; SRAMH/SRAM1/SRAM2/Ret_SRAM with Even- parity check, each byte of data has one check bit per byte of data.

1.4.9 General Purpose IO (GPIO)

GPIO Key Features:

- 16 I/O pins per port group, may be less than 16 depending on actual configuration
- Support pull-up
- Support push-pull, open-drain output mode
- Supports high, medium and low drive modes
- Inputs supporting external interrupts
- Support I/O pin peripheral function multiplexing, up to 16 selectable multiplexed functions per pin, up to 64 selectable functions for some I/Os
- Each I/O pin can be programmed independently
- Each I/O pin can be selected to have 2 functions active at the same time (2 output functions active at the same time are not supported)

1.4.10 Interrupt Control (INTC)

The functions of the Interrupt Controller (INTC) are to select interrupt event requests as interrupt inputs to the NVIC to wake up the WFI, and as event inputs to wake up the WFE. select interrupt event requests as wake-up conditions for low-power modes (sleep mode and stop mode); interrupt control functions for the external pins NMI and EIRQ; and interrupt/event selection functions for software interrupts.

Main specifications:

1) NVIC interrupt vectors: Please refer to the user manual for the actual number of interrupt vectors used (excluding the 16 interrupt lines of the Cortex™-M4F), each interrupt vector can select the corresponding peripheral interrupt event request based on the interrupt select register. For more information on exceptions and NVIC programming, please refer to Chapter 5: Exceptions and Chapter 8: Nested Vector Interrupt Controllers in the ARM

Cortex™-M4F Technical Reference Manual.

2) Programmable priority: 16 programmable priority levels (4-bit interrupt priority used)

3) Non-maskable interrupts: In addition to the NMI pin as a non-maskable interrupt source, multiple system interrupt event requests can be independently selected

As non-maskable interrupts, and each interrupt event request is equipped with independent enable selection, hang, and clear hang registers.

4) Equipped with 16 external pin interrupts.
5) Configure multiple peripheral interrupt event requests, please refer to the interrupt event request sequence number list for details.
6) Equipped with 32 software interrupt event requests.
7) The interrupt can wake up the system in sleep mode and stop mode.

1.4.11 Automatic Operating System (AOS)

Automatic Operation System (AOS) is used to link peripheral hardware circuits without the help of CPU. Events generated by peripheral circuits are used as AOS Source, such as comparison match and timing overflow of timer, period signal of RTC, various states of sending and receiving data of communication module (idle, full receiving data, end of sending data, empty sending data) end of conversion of ADC, etc., to trigger other peripheral circuits to act. The action of the triggered peripheral circuit is called AOS Target.

1.4.12 Keyboard scanning (KEYSCAN)

This product is equipped with a keyboard control module (KEYSCAN) 1 unit. the KEYSCAN module supports keyboard array (row and column) scanning, the columns are driven by independent scan output KEYOUTm (m=0~7), while the row KEYINn (n=0~15) is detected as EIRQn (n=0~15) input. This module implements the key recognition function by the line scan query method.

1.4.13 Storage Protection Unit (MPU)

MPUs can provide protection for memory and can improve system security by

blocking unauthorized access. Four host-specific MPU units and one IP-specific

MPU unit are built into this product.

The ARM MPU provides CPU access control to the entire 4G address space.

The DMA MPU (DMPU) provides DMA_1/DMA_2/USB FS DMA control of read and write access to the full 4G address space. The MPU action can be set to ignore/bus error/non-maskable interrupt/reset when access to the prohibited space occurs.

The IP MPU provides access control to the system IP and security-related IPs when in unprivileged mode.

1.4.14 DMA Controller (DMA)

DMA is used to transfer data between memory and peripheral function modules, enabling data exchange between memory, between memory and peripheral function modules, and between peripheral function modules without CPU involvement.

- The DMA bus is independent of the CPU bus and is transmitted according to the AMBA AHB-Lite bus protocol
- 8 independent channels (4 channels each for DMA_1 and DMA_2) allowing independent operation of different DMA transfer functions
- The start request source for each channel is configured via a separate trigger source selection register
- One block of data is transferred per request
- Data blocks can be as small as 1 data, up to 1024 data

- Each data can be configured as 8bit, 16bit or 32bit
- Up to 65535 transmissions can be configured
- Source and destination addresses can be independently configured as fixed, incremental, decremental, cyclic or jump with specified offsets
- Three types of interrupts can be generated, block transfer completion interrupt, transfer completion interrupt, and transfer error interrupt. Each of these interrupts can be configured to be masked or not. The block transfer completion and transfer completion can be used as event output and as trigger source input for other peripheral modules with hardware trigger function.
- Support chain transfer function, which can transfer multiple data blocks in one request
- Support external events to trigger channel reset
- Can be set to enter module stop state when not in use to reduce power consumption

1.4.15 Voltage Comparator (CMP)

The CMP is a peripheral module that compares two analog voltages, INP and INM, and outputs the result of the comparison.The CMP has 3 independent comparison channels, each with 4 input sources for the analog voltages INP and INM. It is possible to select an INP for a single comparison with an INM or to scan multiple INPs with the same INM. The comparison results can be read from registers, output to external pins, and generate interrupts and events.

1.4.16 Analog-to-digital converters (ADCs)

The 12-bit ADC is an analog-to-digital converter that uses successive approximation. It has a maximum of 16 analog input channels and can convert both external ports and internal analog signals. These channels can be combined in any sequence for successive scan conversion, and the sequence can be converted in a single, or continuous scan. The ADC module is equipped with an analog watchdog function that monitors the conversion results of any given channel and detects if the user-set threshold value is exceeded.

ADC Key Features:

- High Performance
  - Configurable for 12-, 10-, and 8-bit resolution
  - The frequency ratio between the peripheral clock PCLK4 and the A/D converter clock ADCLK can be selected as follows:
    - PCLK4: ADCLK = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4

      -ADCLK can be selected as PLL asynchronous with the system clock HCLK, then the clock source of PCLK4 and ADCLK is fixed as PLL at the same time, and the frequency ratio is 1:1, and the original dividing frequency setting is invalid
  - 2MSPS (PCLK4=ADCLK=60MHz， 12-bit, sampling 17 cycles)

- Independent programming of sampling time for each channel
- Independent data register for each channel
- Data register configurable data alignment
- Continuous multiple conversion averaging function
- Analog watchdog to monitor conversion results

  - The ADC module can be set to stop when not in use
- Analog input channels
  - Up to 16 external analog input channels
  - 1 internal reference voltage
- Conversion start conditions
  - Software Settings Conversion Start
  - Peripheral peripheral synchronization triggers the start of the transition
  - External pins trigger the start of conversion
- Conversion Mode
  - 2 scan sequences A and B, single or multiple channels can be specified at will
  - Sequence A Single Scan
  - Sequence A Continuous Scan
  - Double sequence scanning, sequence A, B independent selection of trigger source, sequence B priority than A
  - Synchronous mode (for devices with two or three ADCs)
- Interrupt and event signal output
  - Sequence A End of Scan Interrupt EOCA_INT and Event EOCA_EVENT
  - Sequence B End of Scan Interrupt EOCB_INT and Event EOCB_EVENT
  - Analog watchdog channel comparison interrupt CHCMP_INT and event CHCMP_EVENT , sequence comparison interrupt SEQCMP_INT and event SEQCMP_EVENT
  - Each of the above 4 events can initiate DMA

1.4.17 Temperature Sensor (OTS)

The OTS can acquire the temperature inside the chip to support reliable operation of the system. After temperature measurement is initiated using software or hardware triggers, the OTS provides a set of temperature-dependent digital quantities that can be calculated using a formula to obtain the temperature value.

1.4.18 Advanced Control Timer (Timer6)

Advanced Control Timer 6 (Timer6) is a 16-bit count width high performance timer that can be used to count different forms of clock waveforms and output for external use. The timer supports both triangle waveform and sawtooth waveform modes and can generate various PWM waveforms; software-synchronous counting and hardware-synchronous counting between units; cache function for each reference value register; 2-phase quadrature encoding and 3-phase quadrature encoding; and EMB control. Timer6 with 3 units is included in this series.

1.4.19 Universal control timer (Timer4)

The Universal Control Timer 4 (Timer4) is a timer module for three-phase motor control, providing a variety of three-phase motor control solutions for different applications. The timer supports both triangle waveform and sawtooth waveform modes, generates various PWM waveforms, supports cache function, and supports EMB control. This series is equipped with 3 units of Timer4.

1.4.20 Emergency Brake Module (EMB)

The emergency brake module is a functional module that notifies the timer when certain conditions are met so that the timer stops outputting PWM signals to the external motor, and the following events are used to generate the notification:

- External port input level change
- PWM output port level occurs in phase (same high or same low)
- Voltage comparator comparison results
- External oscillator stops oscillating
- Write register software control

1.4.21 General purpose timer (TimerA)

Universal Timer A (TimerA) is a timer with 16-bit count width and 8 PWM outputs. The timer supports two waveform modes, triangle waveform and sawtooth waveform, and can generate various PWM waveforms; it supports software synchronous start counting; the comparison reference value register supports cache function; it supports 2-phase quadrature coding counting and 3-phase quadrature coding counting. The series products are equipped with 6 units of TimerA, which can achieve a maximum of 48 PWM outputs.

1.4.22 General purpose timer (Timer0)

Universal Timer 0 (Timer0) is a basic timer that enables both synchronous and asynchronous counting. The timer contains 2 channels and can generate a compare match event during counting. This event can trigger an interrupt or be used as an event output to control other modules, etc. Timer0 with 2 units is installed in this series.

1.4.23 Real Time Clock (RTC)

The Real Time Clock (RTC) is a counter that stores time information in BCD code format. It records the specific calendar time from 00 to 99 years. Both 12/24 hour time systems are supported and the days 28, 29 (leap year) 30 and 31 are automatically calculated based on the month and year.

1.4.24 Watchdog counter (WDT)

There are two watchdog counters, one is a dedicated watchdog counter where the count clock source is a dedicated internal RC (WDTCLK:10KHz)
(SWDT) and the other is a general-purpose watchdog counter (WDT) with count clock source of PCLK3.
The dedicated watchdog and general-purpose watchdog are 16-bit decrementing counters used to monitor software faults resulting from deviations from normal operation of the application due to external disturbances or unforeseen logic conditions.

Both watchdogs support the window function. The window interval can be preset before the count starts, and when the count value is in the window interval, the counter can be refreshed and the count starts again.

1.4.25 Serial communication interface (USART)

This product is equipped with 4 units of serial communication interface module (USART). The USART module allows flexible full-duplex data exchange with external devices; it supports universal asynchronous serial communication interface (UART)， clock synchronous communication interface, and smart card interface (ISO/IEC7816-3). Supports modem operation (CTS/RTS operation)，multi-processor operation.

1.4.26 Integrated Circuit Bus (I2C)

This product is equipped with 3 units of Integrated Circuit Bus (I2C), which is used as an interface between the microcontroller and the I2C serial bus. It provides multi-master mode function and can control all I2C bus protocols and arbitration. Standard mode and fast mode are supported.

1.4.27 Serial Peripheral Interface (SPI)

This product is equipped with a 4-channel serial peripheral interface SPI, which supports high-speed full-duplex serial synchronous transmission for easy data exchange with peripheral devices. Users can set 3-wire/4-wire, master/slave and baud rate range as required.

1.4.28 Four-wire serial peripheral interface (QSPI)

The Quad Wire Serial Peripheral Interface (QSPI) is a memory control module used to communicate with serial ROMs with SPI-compatible interfaces. The targets include serial Flash, serial EEPROM and serial FeRAM.

1.4.29 Integrated circuitry with built-in audio bus (I2S)

I2S(Inter_IC Sound Bus)the integrated circuit built-in audio bus, is dedicated to data transfer between audio devices. This product is equipped with 4 I2S and has the following features.

Function	Main Features
Communication method	- Supports full-duplex and half-duplex communications - Supports master mode or slave mode operation
Data Format	- Selectable channel length: 16/32 bit - Optional transmission data length: 16/24/32 bits - Data shift order: MSB start
Baud rate	- 8-bit programmable linear prescaler for accurate audio sampling frequency - Support sampling frequency 192k, 96k, 48k, 44.1k, 32k, 22.05k, 16k, 8k - Output drive clock to drive external audio components at a fixed rate of 256*Fs (Fs is the audio sampling frequency)
I2S protocol support	- I2S Philips Standard - MSB Alignment Standards - LSB Alignment Standards - PCM Standards
Data buffering	— — Input and output FIFO buffers with 2 words deep and 32 bits wide
Clock source	— Can use internal I2SCLK (UPLLR/UPLLQ/UPLLP/MPLLR/MPLLQ/MPLLP); also available from The external clock on the I2S_EXCK pin provides
Interruptions	- Generate an interrupt when the effective space in the transmit buffer reaches the alarm threshold - Generate an interrupt when the effective space in the receive buffer reaches the alarm threshold - The receive data area is full and there is still a write data request, receive overflow - Sending data area is empty and there are still sending requests, send the next overflow - Send data area is full and still has write data request, send overflow

1.4.30 CAN communication interface (CAN)

This product is equipped with one unit of CAN communication interface module (CAN) and 512Byte of RAM for CAN to store transmit/receive messages. The CAN2.0B protocol according to ISO11898-1 and the TTCAN protocol according to ISO11898-4 are supported.

1.4.31 USB 2.0 Full Speed Module (USB FS)

The USB FS is a dual-role (DRD) controller that supports both slave and host functions. The USB FS

supports both full-speed and low-speed transceivers in master mode, while only full-speed transceivers are supported in slave mode.

The USB FS module on this product can generate SOF events when a SOF token is successfully sent in master mode or received in slave mode.

1.4.32 Cryptographic Coprocessing Module (CPM)

The Cryptographic Co-Processing Module (CPM) consists of three sub-modules: AES Encryption and Decryption Algorithm Processor, HASH Secure Hash Algorithm, and TRNG True Random Number Generator.

The AES encryption and decryption algorithm processor follows standard data encryption and decryption standards and can perform encryption and decryption operations with 128-bit key length.

The HASH secure hash algorithm is the SHA-2 version of the SHA-256 (Secure Hash Algorithm) which complies with the national standard ""FIPS PUB 180-3" published by the National Bureau of Standards and Technology, and can produce 256-bit message digest output for messages up to 2^64 bits in length. message digest output for messages up to 2^64 bits in length.

TRNG True Random Number Generator is a random number generator based on continuous analog noise, providing 64bit random numbers.

1.4.33 Data Computing Unit (DCU)

The Data Computing Unit (DCU) is a module that simply processes data without the help of a CPU. Each DCU unit has 3 data registers, and is capable of adding, subtracting, and comparing the size of 2 data, as well as window comparison functions. This product is equipped with 4 DCU units, each of which can perform its own function independently.

1.4.34 CRC Calculation Unit (CRC)

The CRC algorithm of this module follows the definition of ISO/IEC13239 and uses 32-bit and 16-bit CRC respectively. the polynomial generated by CRC32 is X32+X26+X23+X22+X16+X12+X11+X10+X8+X7+X5+X4+X2+X+1. the polynomial generated by CRC16 is X16+X12+X5+1.

1.4.35 SDIO Controller (SDIOC)

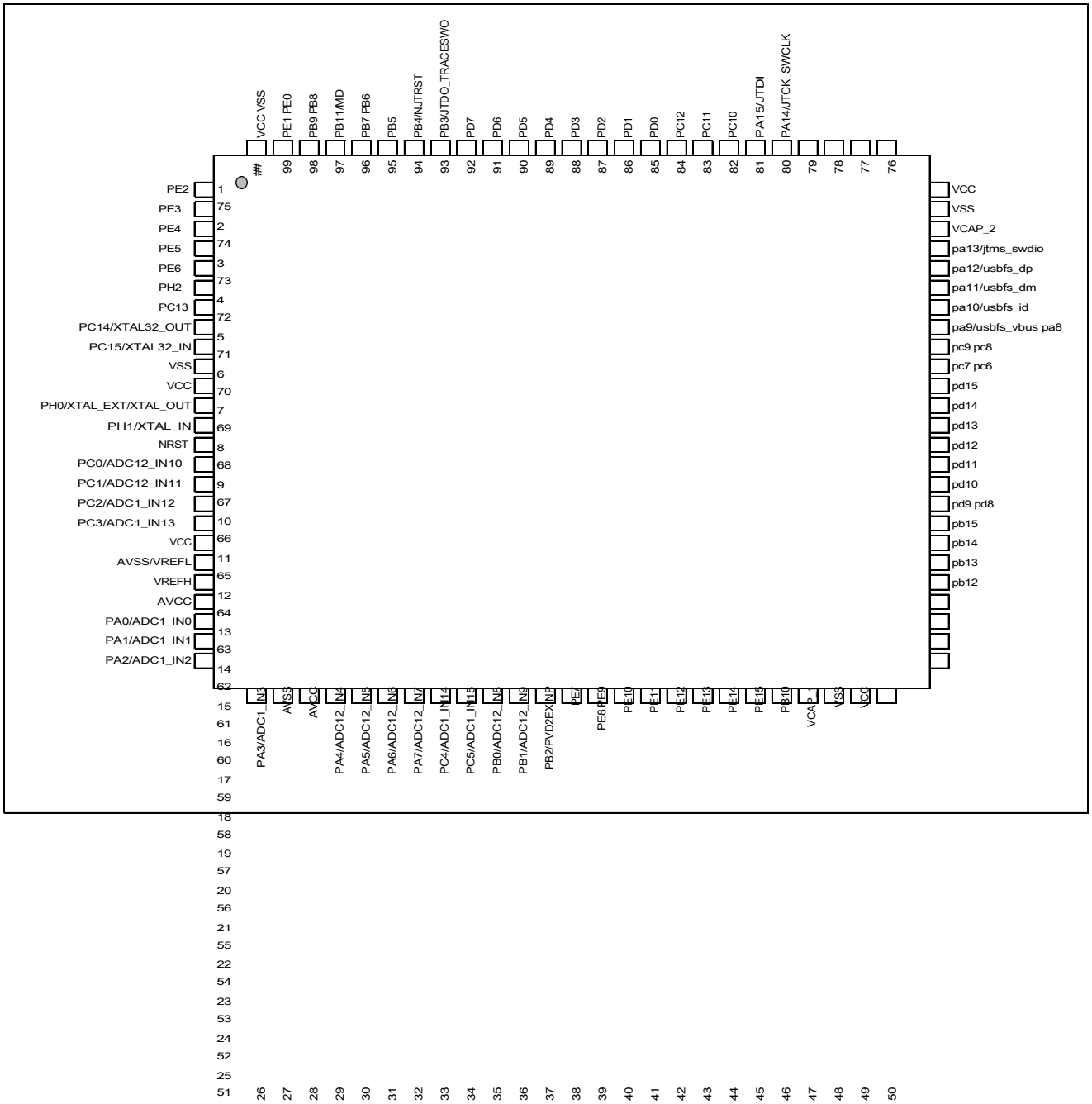
The SDIO controller is the host in the SD/SDIO/MMC communication protocol. This product has 2 SDIO controllers, each providing a host interface for communication with SD cards supporting SD2.0 protocol, SDIO devices and MMC devices supporting eMMC4.51 protocol. SDIOC features are as follows:

- Support SDSC, SDHC, SDXC format SD cards and SDIO devices
- Supports one-wire (1bit) and four-wire (4bit) SD buses
- Supports one-wire (1bit), four-wire (4bit) and eight-wire (8bit) MMC buses
- With card recognition and hardware write protection

2 Pin Configuration and Function (Pinouts)

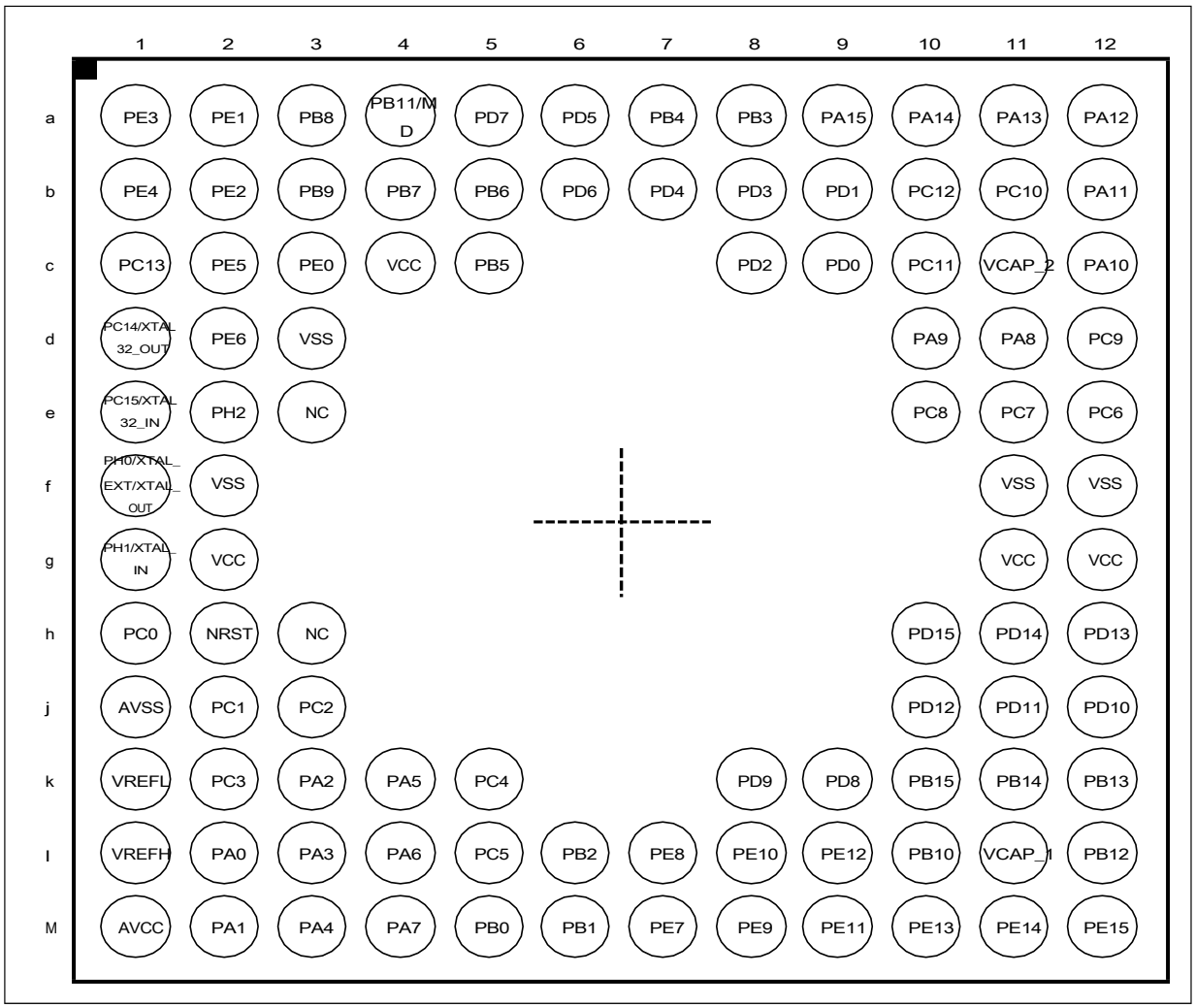
2.1 Pin Configuration Diagram

HC32F460PETB-LQFP100 /HC32F460PCTB-LQFP100



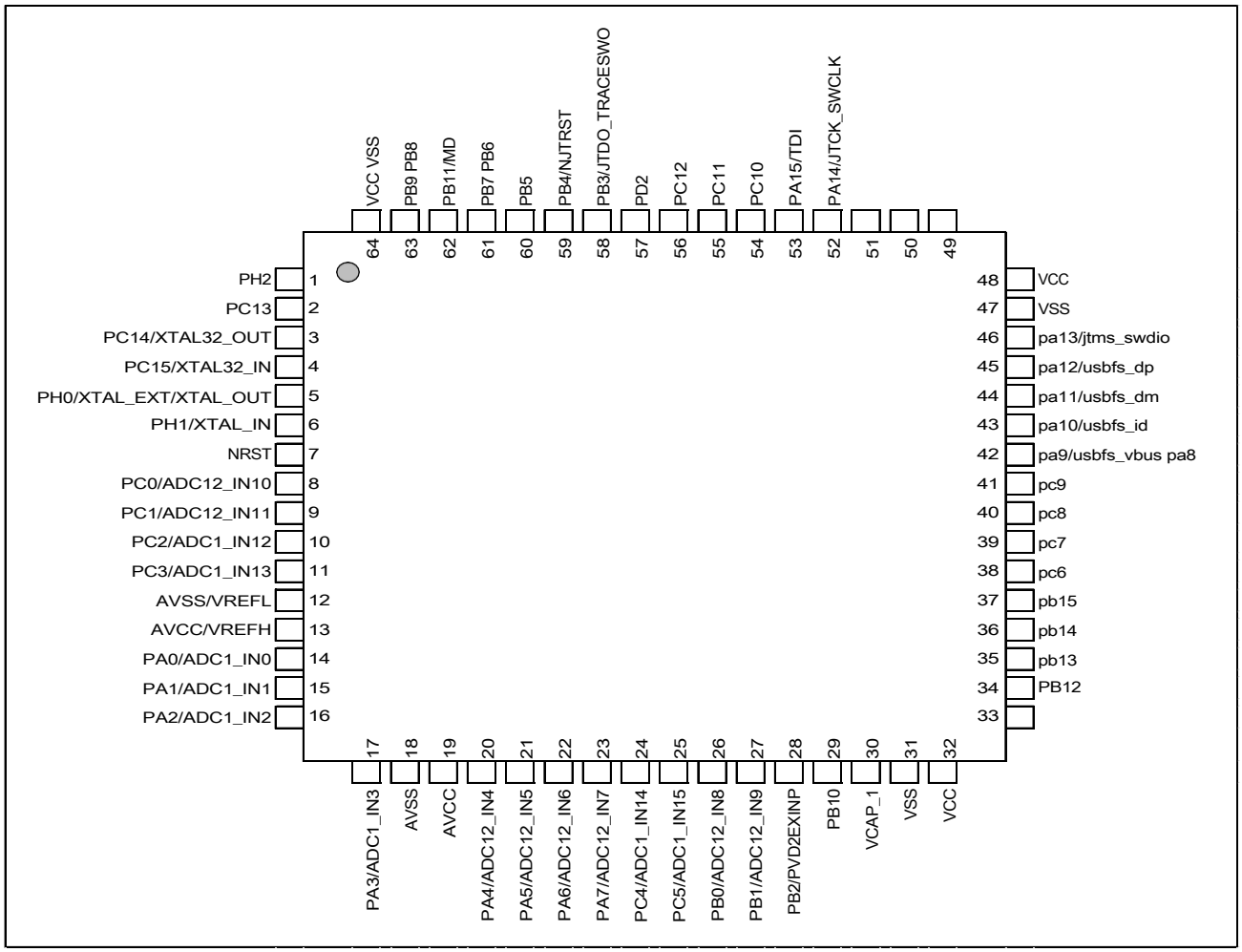
hc32f460pehb-vfbga100

(Top View)

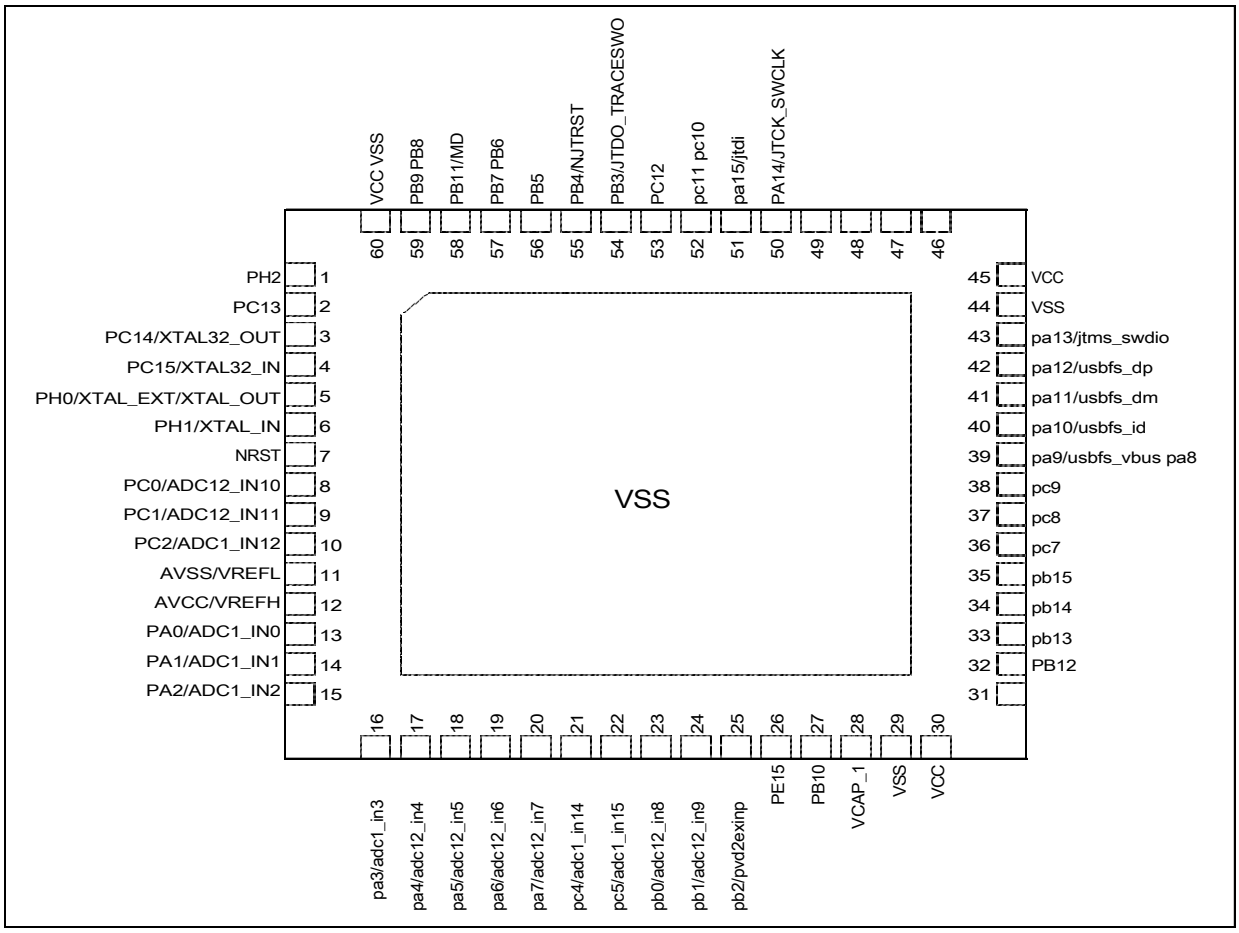


Note: A1 is Pin 1.

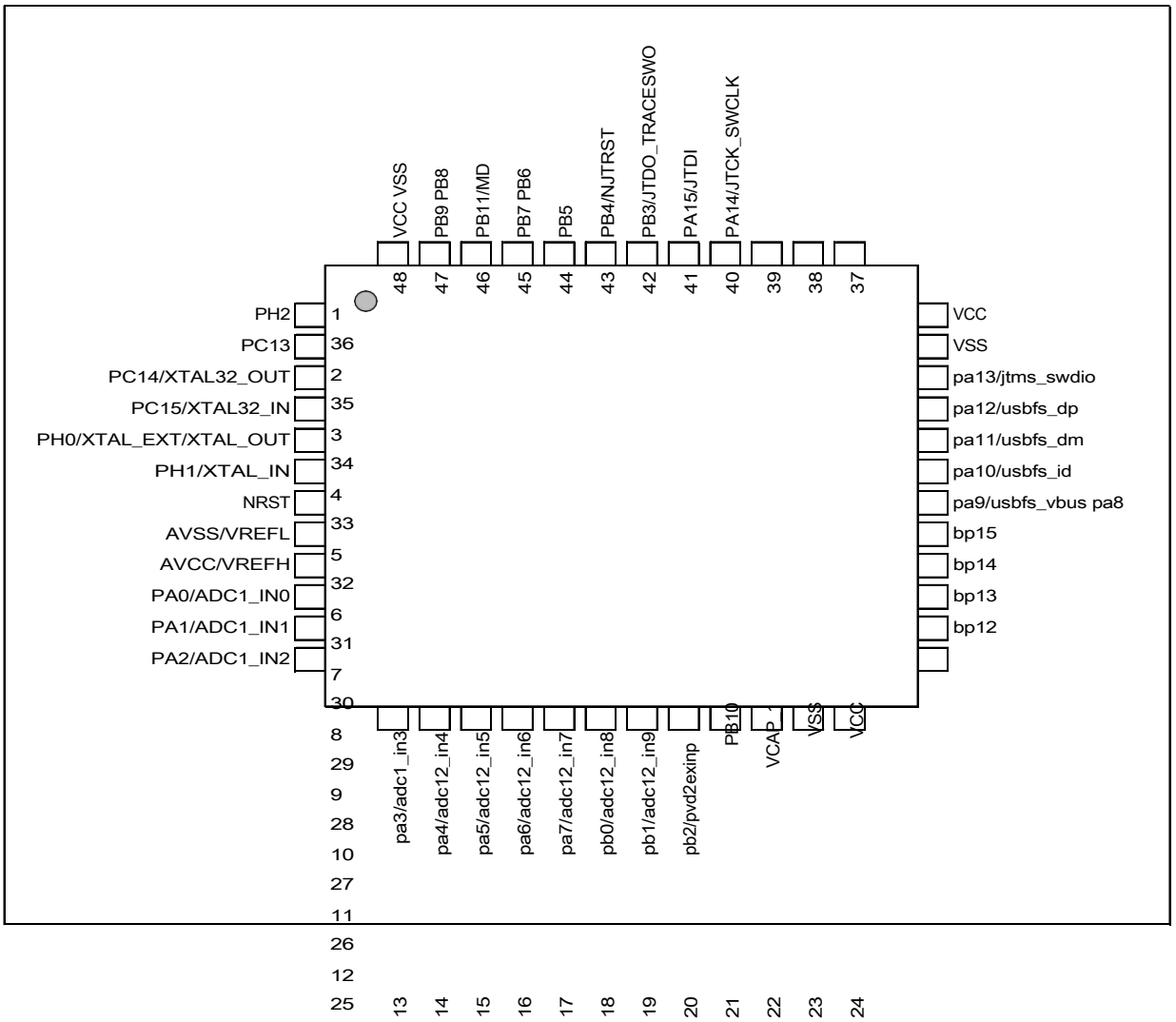
HC32F460KETA-LQFP64/ HC32F460KCTA-LQFP64



HC32F460KEUA-QFN60TR



HC32F460JETA-LQFP48 / HC32F460JCTA-LQFP48



HC32F460JEUA-QFN48TR

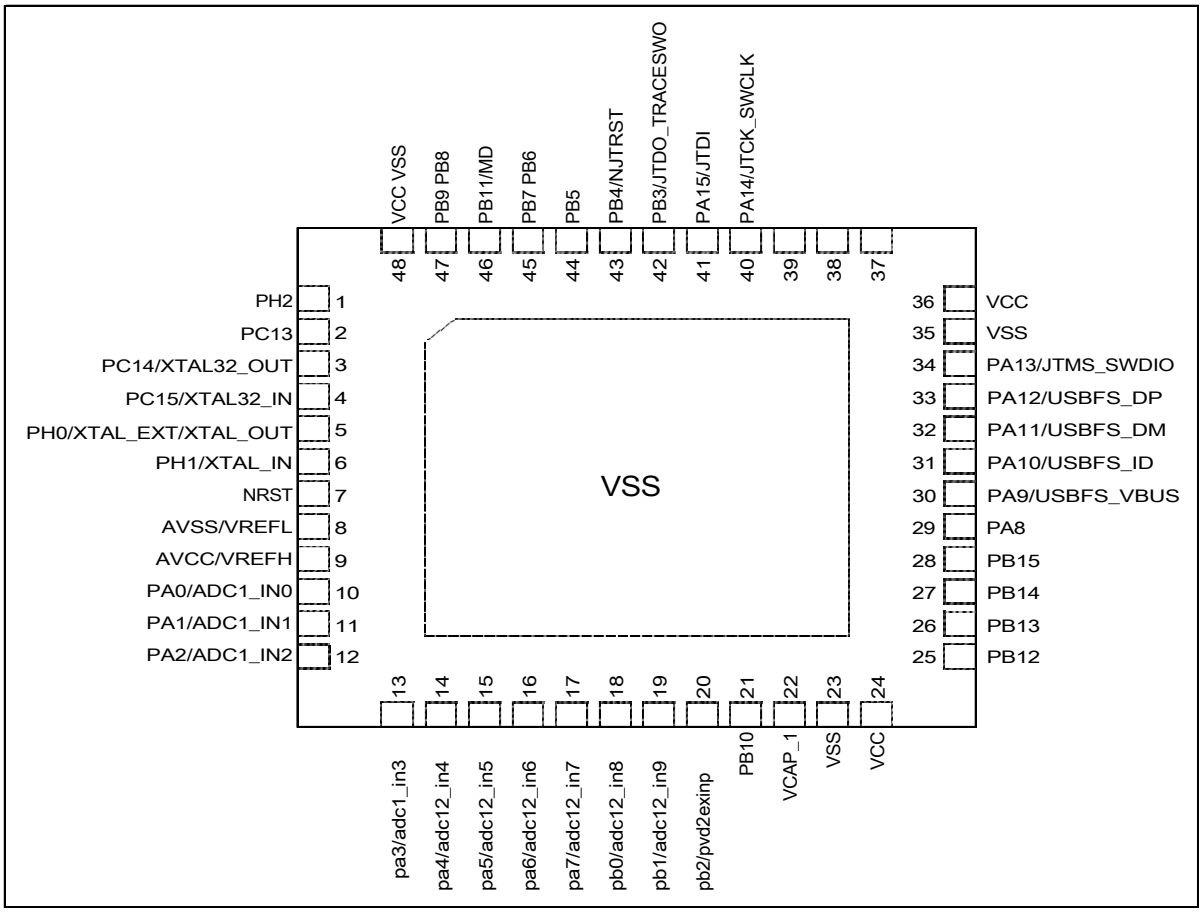


Figure 2-1 Pin Configuration Diagram

2.2 Pin List

Table 2-1 Pin Function Table

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	–	–	–	EVNTPT	EVENTOUT	–	Communication Funcs
1	B2	–	–	–	PE2		EIRQ2	TRACECK	GPO				TIMA_3_PWM5			USART3_CK								EVENTOUT		Func_Grp2
2	A1	–	–	–	PE3		EIRQ3	TRACED0	GPO				TIMA_3_PWM6			USART4_CK								EVENTOUT		Func_Grp2
3	B1	–	–	–	PE4		EIRQ4	TRACED1	GPO				TIMA_3_PWM7											EVENTOUT		Func_Grp2
4	C2	–	–	–	PE5		EIRQ5	TRACED2	GPO				TIMA_3_PWM8											EVENTOUT		Func_Grp2
5	D2	–	–	–	PE6		EIRQ6	TRACED3	GPO															EVENTOUT		Func_Grp2
6	E2	1	1	1	PH2		EIRQ2		GPO	FCMREF	TIM4_2_CLK		TIMA_4_PWM7		EMB_IN4			SDIO2_D4	I2S3_EXCK					EVENTOUT		Func_Grp2
7	C1	2	2	2	PC13		EIRQ13		GPO	RTC_OUT			TIMA_4_PWM8					SDIO2_CK	I2S3_MCK				EVNTP313			Func_Grp2
8	D1	3	3	3	PC14	XTAL32_OUT	EIRQ14		GPO				TIMA_4_PWM5										EVNTP314			
9	E1	4	4	4	PC15	XTAL32_IN	EIRQ15		GPO				TIMA_4_PWM6										EVNTP315			
10	F2	–	–	–	VSS																					
11	G2	–	–	–	VCC																					
12	F1	5	5	5	PH0	XTAL_EXT/XTAL_OUT	EIRQ0		GPO					TIMA_5_PWM3												
13	G1	6	6	6	PH1	XTAL_IN	EIRQ1		GPO					TIMA_5_PWM4												
14	H2	7	7	7	NRST																					
15	H1	8	8	–	PC0	ADC12_IN10/CMP3_INP3	EIRQ0		GPO				TIMA_2_PWM5					SDIO2_D5					EVNTP300	EVENTOUT		Func_Grp1
16	J2	9	9	–	PC1	ADC12_IN11	EIRQ1		GPO				TIMA_2_PWM6					SDIO2_D6					EVNTP301	EVENTOUT		Func_Grp1
17	J3	10	10	–	PC2	ADC1_IN12	EIRQ2		GPO				TIMA_2_PWM7		EMB_IN3			SDIO2_D7					EVNTP302	EVENTOUT		Func_Grp1
18	K2	11	–	–	PC3	ADC1_IN13/CMP1_INM2	EIRQ3		GPO				TIMA_2_PWM8					SDIO1_WP					EVNTP303	EVENTOUT		Func_Grp1
19	–	–	–	–	VCC																					
20	J1	12	11	8	AVSS																					
–	K1	–	–	–	VREFL																					
21	L1	–	–	–	VREFH																					
22	M1	13	12	9	AVCC																					
23	L2	14	13	10	PA0	ADC1_IN0/CMP1_INP1	EIRQ0/WKUP0_0		GPO		TIM4_2_OUH		TIMA_2_PWM1/TIMA_2_CLKA		TIMA_2_TRIG	SPI1_SS1		SDIO2_D4					EVNTP100	EVENTOUT		Func_Grp1
24	M2	15	14	11	PA1	ADC1_IN1/CMP1_INP2	EIRQ1		GPO		TIM4_2_OUL		TIMA_2_PWM2/TIMA_2_CLKB	TIMA_3_TRIG		SPI1_SS2		SDIO2_D5					EVNTP101	EVENTOUT		Func_Grp1
25	K3	16	15	12	PA2	ADC1_IN2/CMP1_INP3	EIRQ2		GPO		TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM1/TIMA_5_CLKA		SPI1_SS3		SDIO2_D6					EVNTP102	EVENTOUT		Func_Grp1
26	L3	17	16	13	PA3	ADC1_IN3/PGAVSS/CMP1_INP4	EIRQ3		GPO		TIM4_2_OVL		TIMA_2_PWM4	TIMA_5_PWM2/TIMA_5_CLKB				SDIO2_D7					EVNTP103	EVENTOUT		Func_Grp1
27	–	18	–	–	AVSS																					
–	E3	–	–	–	NC																					
28	–	19	–	–	AVCC																					
29	M3	20	17	14	PA4	ADC12_IN4/CMP2_INP1/CMP3_INP4	EIRQ4		GPO		TIM4_2_OWH			TIMA_3_PWM5		USART2_CK	KEYOUT0		I2S1_EXCK				EVNTP104	EVENTOUT		Func_Grp1
30	K4	21	18	15	PA5	ADC12_IN5/CMP2_INP2	EIRQ5		GPO		TIM4_2_OWL		TIMA_2_PWM1/TIMA_2_CLKA	TIMA_3_PWM6	TIMA_2_TRIG		KEYOUT1		I2S1_MCK				EVNTP105	EVENTOUT		Func_Grp1
31	L4	22	19	16	PA6	ADC12_IN6/CMP2_INP3	EIRQ6		GPO					TIMA_3_PWM1/TIMA_3_CLKA	EMB_IN2		KEYOUT2	SDIO1_CMD					EVNTP106	EVENTOUT		Func_Grp1
32	M4	23	20	17	PA7	ADC12_IN7/CMP1_INM1/CMP2_INM1/CMP3_INM1	EIRQ7		GPO		TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	TIMA_3_PWM2/TIMA_3_CLKB	EMB_IN3		KEYOUT3	SDIO2_WP					EVNTP107	EVENTOUT		Func_Grp1
33	K5	24	21	–	PC4	ADC1_IN14/CMP2_INM2	EIRQ4		GPO		TIM4_2_OUH			TIMA_3_PWM7		USART1_CK		SDIO2_CD					EVNTP304	EVENTOUT		Func_Grp1
34	L5	25	22	–	PC5	ADC1_IN15/CMP3_INM2	EIRQ5		GPO		TIM4_2_OUL			TIMA_3_PWM8				SDIO2_CMD					EVNTP305	EVENTOUT		Func_Grp1
35	M5	26	23	18	PB0	ADC12_IN8/CMP3_INP1	EIRQ0		GPO		TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	TIMA_3_PWM3		USART4_CK	KEYOUT4	SDIO2_CMD					EVNTP200	EVENTOUT		Func_Grp1
36	M6	27	24	19	PB1	ADC12_IN9/CMP3_INP2	EIRQ1/WKUP0_1		GPO		TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_3_PWM4		QSPI_QSSN	KEYOUT5	SDIO2_D3	I2S2_EXCK				EVNTP201	EVENTOUT		Func_Grp1
37	L6	28	25	20	PB2	PVD2EXINP	EIRQ2/WKUP0_2		GPO	VCOUT123		TIM6_TRIGB	TIMA_1_PWM8		EMB_IN1	QSPI_QSIO3		SDIO2_D2	I2S2_MCK				EVNTP202	EVENTOUT		Func_Grp1
38	M7	–	–	–	PE7		EIRQ7		GPO	ADTRG1		TIM6_TRIGA	TIMA_1_TRIG			USART1_CK								EVENTOUT		
39	L7	–	–	–	PE8		EIRQ8		GPO		TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5											EVENTOUT		
40	M8	–	–	–	PE9		EIRQ9		GPO		TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA											EVENTOUT		
41	L8	–	–	–	PE10		EIRQ10		GPO		TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6											EVENTOUT		
42	M9	–	–	–	PE11		EIRQ11		GPO		TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB											EVENTOUT		
43	L9	–	–	–	PE12		EIRQ12		GPO		TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7			SPI1_SS1								EVENTOUT		Func_Grp2
44	M10	–	–	–	PE13		EIRQ13		GPO		TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3			SPI1_SS2								EVENTOUT		Func_Grp2

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	–	–	–	EVNTPT	EVENTOUT	–	Communication Funcs
45	M11	–	–	–	PE14		EIRQ14		GPO		TIM4_1_CLK		TIMA_1_PWM4			SPI1_SS3		SDIO1_CD						EVENTOUT		Func_Grp2
46	M12	–	26	–	PE15		EIRQ15		GPO				TIMA_1_PWM8	TIMA_5_TRIG	EMB_IN2	USART4_CK		SDIO1_WP						EVENTOUT		Func_Grp2
47	L10	29	27	21	PB10		EIRQ10		GPO	ADTRG2	TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM8		QSPI_QSIO2		SDIO1_D7	I2S3_EXCK				EVNTP210	EVENTOUT		Func_Grp2
48	L11	30	28	22	VCAP_1																					
49	F12	31	29	23	VSS																					
50	G12	32	30	24	VCC																					
51	L12	33	31	25	PB12		EIRQ12		GPO	VCOUT1	TIM4_2_OVL	TIM6_TRIGB	TIMA_1_PWM8		EMB_IN2	QSPI_QSIO1		SDIO2_D1	I2S3_MCK				EVNTP212	EVENTOUT		Func_Grp2
52	K12	34	32	26	PB13		EIRQ13		GPO	VCOUT2	TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5			QSPI_QSIO0		SDIO2_D0					EVNTP213	EVENTOUT		Func_Grp2
53	K11	35	33	27	PB14		EIRQ14		GPO	VCOUT3	TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6			QSPI_QSCK		SDIO1_D6					EVNTP214	EVENTOUT		Func_Grp2
54	K10	36	34	28	PB15		EIRQ15		GPO	RTC_OUT	TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_6_TRIG	EMB_IN4	USART3_CK		SDIO1_CK					EVNTP215	EVENTOUT		Func_Grp2
55	K9	–	–	–	PD8		EIRQ8		GPO		TIM4_3_OUL			TIMA_6_PWM1/TIMA_6_CLKA		QSPI_QSIO0	KEYOUT7						EVNTP408	EVENTOUT		Func_Grp2
56	K8	–	–	–	PD9		EIRQ9		GPO		TIM4_3_OVL			TIMA_6_PWM2/TIMA_6_CLKB		QSPI_QSIO1	KEYOUT6						EVNTP409	EVENTOUT		Func_Grp2
57	J12	–	–	–	PD10		EIRQ10		GPO		TIM4_3_OWL			TIMA_6_PWM3		QSPI_QSIO2	KEYOUT5						EVNTP410	EVENTOUT		Func_Grp2
58	J11	–	–	–	PD11		EIRQ11		GPO		TIM4_3_CLK			TIMA_6_PWM4		QSPI_QSIO3	KEYOUT4						EVNTP411	EVENTOUT		Func_Grp2
59	J10	–	–	–	PD12		EIRQ12		GPO				TIMA_4_PWM1/TIMA_4_CLKA	TIMA_5_PWM5									EVNTP412	EVENTOUT		
60	H12	–	–	–	PD13		EIRQ13		GPO				TIMA_4_PWM2/TIMA_4_CLKB	TIMA_5_PWM6									EVNTP413	EVENTOUT		
61	H11	–	–	–	PD14		EIRQ14		GPO				TIMA_4_PWM3	TIMA_5_PWM7									EVNTP414	EVENTOUT		
62	H10	–	–	–	PD15		EIRQ15		GPO				TIMA_4_PWM4	TIMA_5_PWM8									EVNTP415	EVENTOUT		
63	E12	37	–	–	PC6		EIRQ6		GPO				TIMA_3_PWM1/TIMA_3_CLKA	TIMA_5_PWM8		QSPI_QSCK	KEYOUT3	SDIO1_D6					EVNTP306	EVENTOUT		Func_Grp2
64	E11	38	35	–	PC7		EIRQ7		GPO		TIM4_2_CLK		TIMA_3_PWM2/TIMA_3_CLKB	TIMA_5_PWM7		QSPI_QSSN	KEYOUT2	SDIO1_D7	I2S2_EXCK				EVNTP307	EVENTOUT		Func_Grp2
65	E10	39	36	–	PC8		EIRQ8		GPO		TIM4_2_OWH		TIMA_3_PWM3	TIMA_5_PWM6		USART3_CK	KEYOUT1	SDIO1_D0	I2S2_MCK				EVNTP308	EVENTOUT		Func_Grp2
66	D12	40	37	–	PC9		EIRQ9		GPO	MCO_2	TIM4_2_OWL		TIMA_3_PWM4	TIMA_5_PWM5			KEYOUT0	SDIO1_D1					EVNTP309	EVENTOUT		Func_Grp1
67	D11	41	38	29	PA8		EIRQ8/WKUP2_0		GPO	MCO_1	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA			USART1_CK		SDIO1_D1	USBFS_SOF				EVNTP108	EVENTOUT		Func_Grp1
68	D10	42	39	30	PA9		EIRQ9/WKUP2_1		GPO		TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB					SDIO1_D2	USBFS_VBUS				EVNTP109	EVENTOUT		Func_Grp1
69	C12	43	40	31	PA10		EIRQ10/WKUP2_2		GPO		TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3	TIMA_5_TRIG				SDIO1_CD	USBFS_ID				EVNTP110	EVENTOUT		Func_Grp1
70	B12	44	41	32	PA11		EIRQ11/WKUP2_3		GPO		TIM4_1_CLK		TIMA_1_PWM4		EMB_IN1			SDIO2_CD	USBFS_DM				EVNTP111	EVENTOUT		Func_Grp1
71	A12	45	42	33	PA12		EIRQ12/WKUP3_0		GPO		TIM4_3_OWL	TIM6_TRIGA	TIMA_1_TRIG	TIMA_6_PWM1/TIMA_6_CLKA				SDIO2_WP	USBFS_DP				EVNTP112	EVENTOUT		Func_Grp1
72	A11	46	43	34	PA13		EIRQ13/WKUP3_1	JTMS_SWDIO	GPO				TIMA_2_PWM5	TIMA_6_PWM2/TIMA_6_CLKB		SPI2_SS1		SDIO2_D3					EVNTP113	EVENTOUT		Func_Grp1
73	C11	–	–	–	VCAP_2																					
74	F11	47	44	35	VSS																					
75	G11	48	45	36	VCC																					
76	A10	49	46	37	PA14		EIRQ14/WKUP3_2	JTCK_SWCLK	GPO				TIMA_2_PWM6	TIMA_6_PWM3	TIMA_4_TRIG	SPI2_SS2		SDIO2_D2	I2S1_EXCK				EVNTP114	EVENTOUT		Func_Grp1
77	A9	50	47	38	PA15		EIRQ15/WKUP3_3	JTDI	GPO				TIMA_2_PWM1/TIMA_2_CLKA	TIMA_6_PWM4	TIMA_2_TRIG	SPI2_SS3		SDIO2_D1	I2S1_MCK				EVNTP115	EVENTOUT		Func_Grp1
78	B11	51	48	–	PC10		EIRQ10		GPO		TIM4_3_OUH		TIMA_2_PWM7	TIMA_5_PWM1/TIMA_5_CLKA				SDIO1_D2					EVNTP310	EVENTOUT		Func_Grp1
79	C10	52	49	–	PC11		EIRQ11		GPO		TIM4_3_OVH		TIMA_2_PWM8	TIMA_5_PWM2/TIMA_5_CLKB				SDIO1_D3					EVNTP311	EVENTOUT		Func_Grp1
80	B10	53	50	–	PC12		EIRQ12		GPO		TIM4_3_OWH		TIMA_4_TRIG	TIMA_5_PWM3				SDIO1_CK					EVNTP312	EVENTOUT		Func_Grp1
81	C9	–	–	–	PD0		EIRQ0		GPO	VCOUT123				TIMA_5_PWM4									EVNTP400	EVENTOUT		Func_Grp1
82	B9	–	–	–	PD1		EIRQ1		GPO				TIMA_3_TRIG	TIMA_6_PWM5									EVNTP401	EVENTOUT		Func_Grp1
83	C8	54	–	–	PD2		EIRQ2		GPO				TIMA_2_PWM4	TIMA_6_PWM6				SDIO1_CMD					EVNTP402	EVENTOUT		Func_Grp1
84	B8	–	–	–	PD3		EIRQ3		GPO	VCOUT1				TIMA_6_PWM7									EVNTP403	EVENTOUT		
85	B7	–	–	–	PD4		EIRQ4		GPO	VCOUT2				TIMA_6_PWM8									EVNTP404	EVENTOUT		
86	A6	–	–	–	PD5		EIRQ5		GPO	VCOUT3													EVNTP405	EVENTOUT		
87	B6	–	–	–	PD6		EIRQ6		GPO							USART2_CK							EVNTP406	EVENTOUT		
88	A5	–	–	–	PD7		EIRQ7		GPO							USART2_CK							EVNTP407	EVENTOUT		
89	A8	55	51	39	PB3		EIRQ3/WKUP0_3	JTDO_TRACESWO	GPO	FCMREF	TIM4_3_CLK		TIMA_2_PWM2/TIMA_2_CLKB	TIMA_6_PWM5				SDIO2_D0					EVNTP203	EVENTOUT		Func_Grp2
90	A7	56	52	40	PB4		EIRQ4/WKUP1_0	NJTRST	GPO		TIM4_3_OWL		TIMA_3_PWM1/TIMA_3_CLKA	TIMA_6_PWM6				SDIO1_D0					EVNTP204	EVENTOUT		Func_Grp2
91	C5	57	53	41	PB5		EIRQ5/WKUP1_1		GPO		TIM4_3_OWH		TIMA_3_PWM2/TIMA_3_CLKB	TIMA_6_PWM7				SDIO1_D3	I2S4_EXCK				EVNTP205	EVENTOUT		Func_Grp2
92	B5	58	54	42	PB6		EIRQ6/WKUP1_2		GPO	ADTRG2	TIM4_3_OVL		TIMA_4_PWM1/TIMA_4_CLKA	TIMA_6_PWM8				SDIO2_CK	I2S4_MCK				EVNTP206	EVENTOUT		Func_Grp2
93	B4	59	55	43	PB7		EIRQ7/WKUP1_3		GPO	ADTRG1	TIM4_3_OVH		TIMA_4_PWM2/TIMA_4_CLKB					SDIO1_D0					EVNTP207	EVENTOUT		Func_Grp2
94	A4	60	56	44	PB11/MD		NMI																EVNTP211			
95	A3	61	57	45	PB8		EIRQ8		GPO		TIM4_3_OUL		TIMA_4_PWM3				KEYOUT7	SDIO1_D4	USBFS_DRVVBUS				EVNTP208	EVENTOUT		Func_Grp2

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	–	–	–	EVNTPT	EVENTOUT	–	Communication Funcs
96	B3	62	58	46	PB9		EIRQ9		GPO		TIM4_3_OUH		TIMA_4_PWM4	TIMA_6_TRIG		SPI2_SS1	KEYOUT6	SDIO1_D5					EVNTP209	EVENTOUT		Func_Grp2
97	C3	–	–	–	PE0		EIRQ0		GPO	MCO_1			TIMA_4_TRIG			SPI2_SS2								EVENTOUT		Func_Grp2
98	A2	–	–	–	PE1		EIRQ1		GPO	MCO_2	TIM4_3_CLK					SPI2_SS3								EVENTOUT		Func_Grp2
99	D3	63	59	47	VSS																					
100	C4	64	60	48	VCC																					
–	H3	–	–	–	NC																					

Notes:

-**Func32~63** In the above table, there are 64 pins support Func32~63 function selection, Func32~63 mainly for serial communication function (including USART, SPI, I2C, I2S, CAN) divided into two groups Func_Grp1, Func_Grp2. Please refer to Table 2-2 for details.

Table 2-2 Func32~63

Table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
Func_Grp1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_SS0	SPI1_SCK	SPI2_MOSI	SPI2_MISO	SPI2_SS0	SPI2_SCK
Func_Grp2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_SS0	SPI3_SCK	SPI4_MOSI	SPI4_MISO	SPI4_SS0	SPI4_SCK

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
Func_Grp1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2S1_SD	I2S1_SDIN	I2S1_WS	I2S1_CK	I2S2_SD	I2S2_SDIN	I2S2_WS	I2S2_CK				
Func_Grp2	I2C3_SDA	I2C3_SCL	CAN_TxD	CAN_RxD	I2S3_SD	I2S3_SDIN	I2S3_WS	I2S3_CK	I2S4_SD	I2S4_SDIN	I2S4_WS	I2S4_CK				

Table 2-3 Port Configuration

Package	Port Group	Bits																Pin Count	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Total	
LQFP100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	83
VFBGA100	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	–	–	–	–	–	–	–	–	–	–	–	–	–	o	o	o	3	
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	52
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	–	–	–	–	–	–	–	–	–	–	–	–	–	o	–	–	1	
	PortH	–	–	–	–	–	–	–	–	–	–	–	–	–	o	o	o	3	
QFN60	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	50
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	–	o	o	–	o	o	o	14	
	PortE	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	o	1	
	PortH	–	–	–	–	–	–	–	–	–	–	–	–	–	o	o	o	3	
LQFP48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	38
QFN48	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	–	–	–	–	–	–	–	–	–	–	–	–	–	3	
	PortH	–	–	–	–	–	–	–	–	–	–	–	–	–	o	o	o	3	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Table 2-4 General Function Specifications

Port		Pull up	Open Drain Output	Drive Capability	5V withstand voltage	Remarks
PortA	PA0~PA10 PA13~PA15	Support	Support	Low，Medium，High	Support *	
	PA11, PA12	Support	Support	Low，Medium，High	Not supported	
PortB	PB0~PB10, PB12~PB15	Support	Support	Low，Medium，High	Support *	
	PB11	Support	–	–	Support	Input dedicated
PortC	PC0~PC15	Support	Support	Low，Medium，High	Support *	
PortD	PD0~PD15	Support	Support	Low，Medium，High	Support	
PortE	PE0~PE15	Support	Support	Low，Medium，High	Support	
PortH	PH0~PH2	Support	Support	Low，Medium，High	Support	

Notes:

-When used as an analog function, the input voltage must not be higher than VREFH/AVCC.

2.3 Pin Function Description

Table 2-5 Pin Function Description

Category	Function Name	I/O	Description
Power	VCC	I	Power supply
	VSS	I	Power Ground
	VCAP_1~2	IO	Kernel Voltage
	AVCC	I	Analog Power
	AVSS	I	Analog power ground
	VREFH	I	Analog Reference Voltage
	VREFL	I	Analog Reference Voltage
System	NRST	I	Reset Pin, Low Active
	MD	I	Mode Pins
PVD	PVD2EXINP	I	PVD2 External input comparison voltage
Clock	XTAL_IN	IO	External master clock oscillator interface
	XTAL_EXT/XTAL_OUT	IO	XTAL_EXT External clock input
	XTAL32_IN	I	External sub-clock (32K) oscillator interface
	XTAL32_OUT	O	
	MCO_1~2	O	Internal clock output
GPIO	GPIOxy (x= A~E,H, y=0~15)	IO	General purpose inputs and outputs
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU Event Output
EIRQ	EIRQx (x=0~15)	I	Maskable external interrupts
	WKUPx_y (x,y=0~3)	I	PowerDown mode external wake-up input
	NMI	I	Non-maskable external interrupts
Event Port	EVNTPxy (x=1~4, y=0~15)	IO	Event port input and output function
Key	KEYOUTx(x=0~7)	O	KEYSCAN scan output signal
JTAG/SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECK	O	Track and debug synchronized clock output
	TRACED0~3	O	Trace debug data output
FCM	FCMREF	I	External reference clock input for clock frequency meter measurement
RTC	RTCOUT	O	1Hz clock output

Timer4	TIM4_x_CLK	I	Counting clock port input
(x=1~3)	TIM4_x_OUH	IO	PWM Port U Phase Output

Category	Function Name	I/O	Description
	TIM4_x_OUL	IO	PWM Port U Phase Output
	TIM4_x_OVH	IO	PWM port V-phase output
	TIM4_x_OVL	IO	PWM port V-phase output
	TIM4_x_OWH	IO	PWM Port W Phase Output
	TIM4_x_OWL	IO	PWM Port W Phase Output
Timer6 (x=1~3)	TIM6_TRIGA	I	External event triggers A input
	TIM6_TRIGB	I	External event triggers B input
	TIM6_x_PWMA	IO	External event trigger input or PWM port output
	TIM6_x_PWMB	IO	External event trigger input or PWM port output
TimerA (x=1~6)	TIMA_x_TRIG	I	External event triggered input
	TIMA_x_PWM1/TIMA_x_CLKA	IO	External event trigger input or PWM port output or count clock port input
	TIMA_x_PWM2/TIMA_x_CLKB	IO	External event trigger input or PWM port output or count clock port input
	TIMA_x_PWMy (y=3~8)	IO	External event trigger input or PWM port output
EMB	EMB_INx (x=1~4)	I	Groupx (x=1~4) port input control signal
USARTx (x=1~4)	USARTx_TX	IO	Sending data
	USARTx_RX	IO	Receiving data
	USARTx_CK	IO	Communication Clock
	USARTx_RTS	O	Request to send a signal
	USARTx_CTS	I	Clear send signal
SPIx (x=1~4)	SPIx_MISO	IO	Master input/slave output data transfer pins
	SPIx_MOSI	IO	Master output/slave input data transfer pins
	SPIx_SCK	IO	Transmission Clock
	SPIx_SS0	IO	Slave select input and output pins
	SPIx_SS1~3	O	Slave select output pins
QSPI	QSPI_QSIO0~3	IO	Data Cable
	QSPI_QSCK	O	Clock Output
	QSPI_QSSN	O	Slave Selection
I2Cx (x=1~3)	I2Cx_SCL	IO	Clock Lines
	I2Cx_SDA	IO	Data Cable
I2Sx (x=1~4)	I2Sx_SD	IO	Serial Data
	I2Sx_SDIN	I	Full duplex serial data input
	I2Sx_WS	IO	Word selection
	I2Sx_CK	IO	Serial Clock
	I2Sx_EXCK	I	External clock source
	I2Sx_MCK	O	Master Clock
CAN	CAN_TxD	O	Sending data
	CAN_RxD	I	Receiving data

SDIOx	SDIOx_Dy (y=0~7)	IO	SD data signal

Category	Function Name	I/O	Description
	SDIOx_CK	O	SD clock output signal
	SDIOx_CMD	IO	SD command and reply signals
	SDIOx_CD	I	SD card recognition status signal
	SDIOx_WP	I	SD card write protect status signal
USBFS	USBFS_DM	IO	USBFS on-chip full-speed PHY D-signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+ signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O	USBFS SOF pulse output signal
	USBFS_DRVVBUS	O	USBFS VBUS driver license signal
CMPx (x=1~3)	VCOUT1	O	Analog comparison channel 1 result output
	VCOUT2	O	Analog comparison channel 2 result output
	VCOUT3	O	Analog comparison channel 3 result output
	VCOUT123	O	Analog comparison channel 1~3 Result OR output
	CMPx_INPy	I	Analog comparator channel x positive voltage y input
	CMPx_INMy	I	Analog comparator channel x negative voltage y input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start-up source
	ADC1_INx (x=0~3,12~15)	I	ADC1 external analog input port
	ADC12_INx (x=4~11)	I	ADC1 and ADC2 share an external analog input port
	PGAVSS	I	PGA Ground input

2.4 Pin Usage Instructions

Table 2-6 Pin Usage Description

Pin Name	Instructions for use
VCC	Power supply, connect 1.8V~3.6V voltage and connect decoupling capacitor with VSS pin nearby (refer to electrical characteristics)
VSS	Power ground, connected to 0V
VCAP_1~2	Kernel voltage, connect capacitor to VSS pin nearby to stabilize kernel voltage (refer to electrical characteristics)
AVCC	Analog power supply for analog modules, connected to the same voltage as VCC (refer to electrical characteristics) Shorted to VCC when not using analog modules
AVSS/VREFL	Analog power ground/reference voltage, connected to the same voltage as AVSS (reference electrical characteristics) Shorted to VSS when not using the analog module
VREFH	ADC1, ADC2 analog reference voltage, connected to a voltage not higher than AVCC when not using the ADC, please short with AVCC
PB11/MD	Mode input, fixed to the input state. This pin must be fixed high when the reset pin (NRST) is released (changed from low to high). Recommended connection resistor (4.7KΩ) to VCC (pull-up)
NRST	Reset pin, active low. Connect resistor to VCC (pull-up) when not in use
Pxy, x=A~E,H, y=0~15	General purpose pins. When used as input function, the input voltage should not exceed 5V. when used as analog input, the analog voltage should not exceed VREFH/AVCC Suspend when not in use or connect resistor to VCC (pull-up)/VSS (pull-down)

3 Electrical Characteristics (ECs)

3.1 Parameter Conditions

All voltages are referenced to VSS if not otherwise specified.

3.1.1 Minimum and maximum values

Unless otherwise noted, all device minimum and maximum values are guaranteed by design or characterization testing under worst-case ambient temperature, supply voltage, and clock frequency conditions.

3.1.2 Typical values

Unless otherwise noted, typical data is obtained by design or characterization testing at $_{TA}$ = 25 °C and VCC = 3.3 V.

3.1.3 Typical Curve

Unless otherwise noted, all typical curves are untested and are for design reference only.

3.1.4 Load capacitance

The load conditions used to measure the pin parameters are shown in Figure 3-1 (left).

3.1.5 Pin Input Voltage

The measurement of the input voltage on the device pins is shown in Figure 3-1 (right).

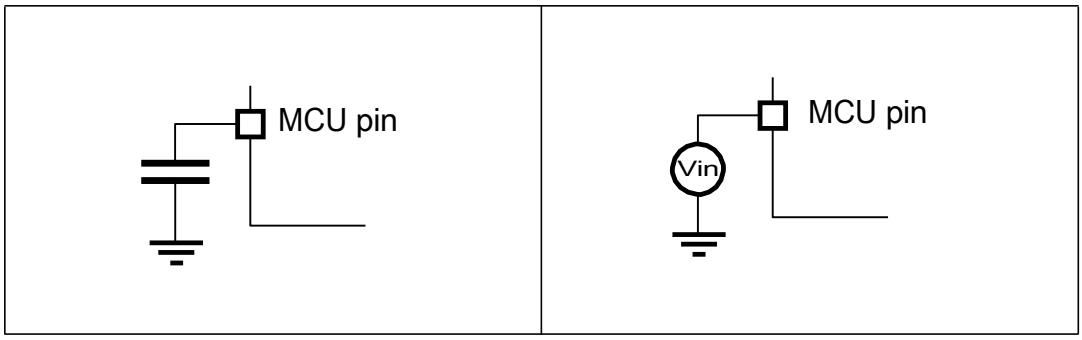


Figure 3-1 Pin load condition (left) and input voltage measurement (right)

3.1.6 Power Solutions

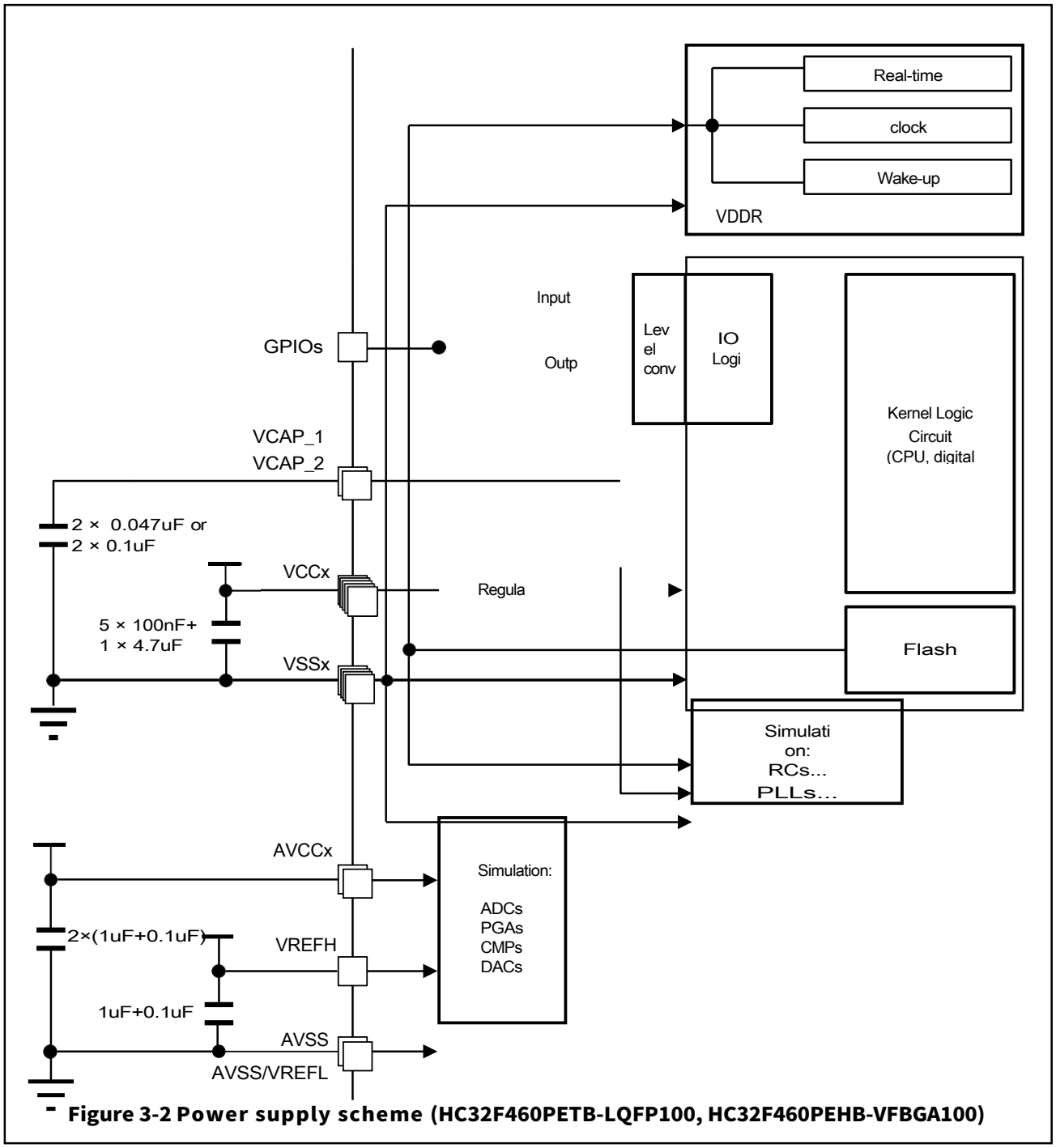


Figure 3-2 Power supply scheme (HC32F460PETB-LQFP100, HC32F460PEHB-VFBGA100)

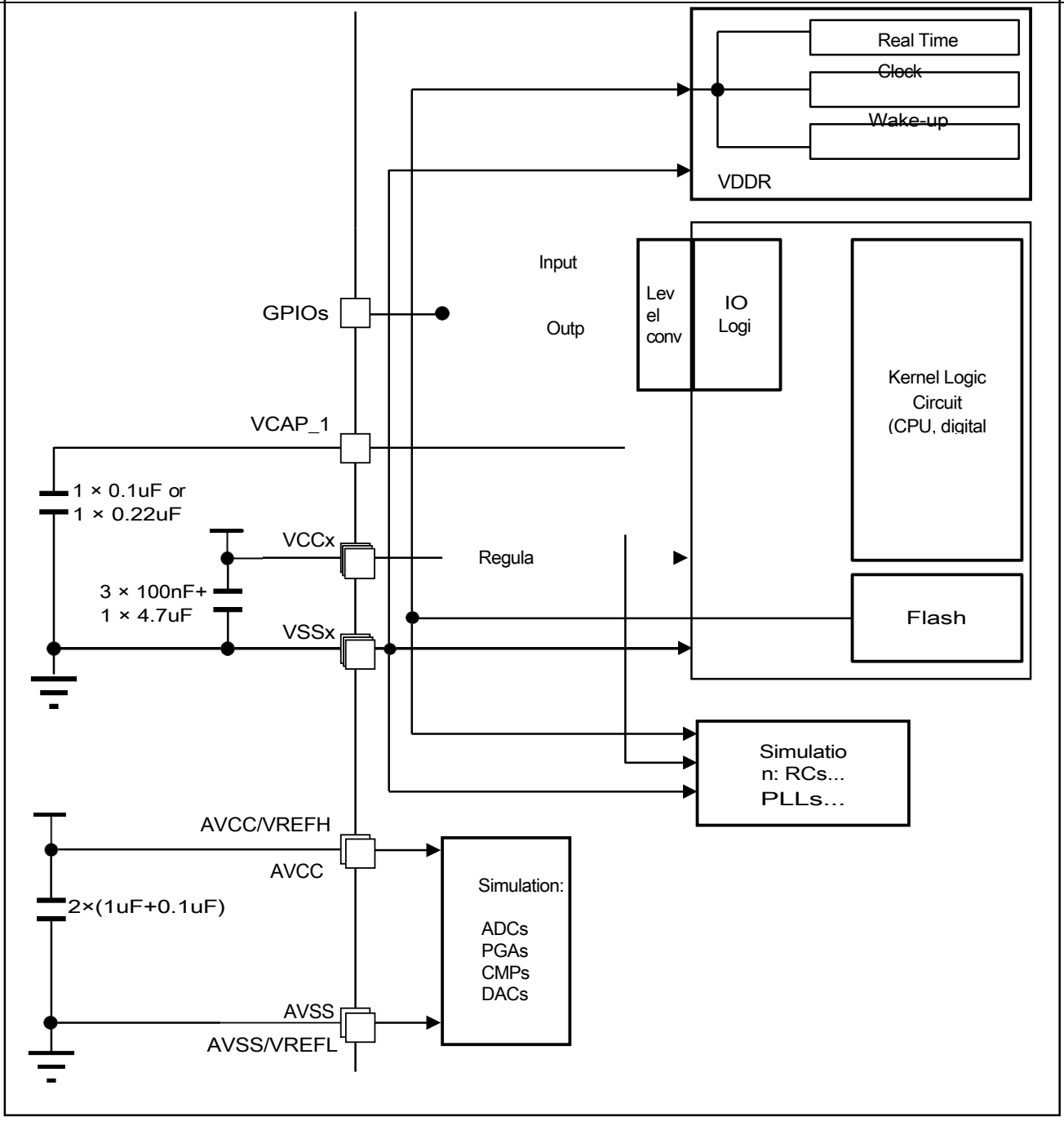


Figure 3-3 Power Supply Solution

(HC32F460KETA-LQFP64)

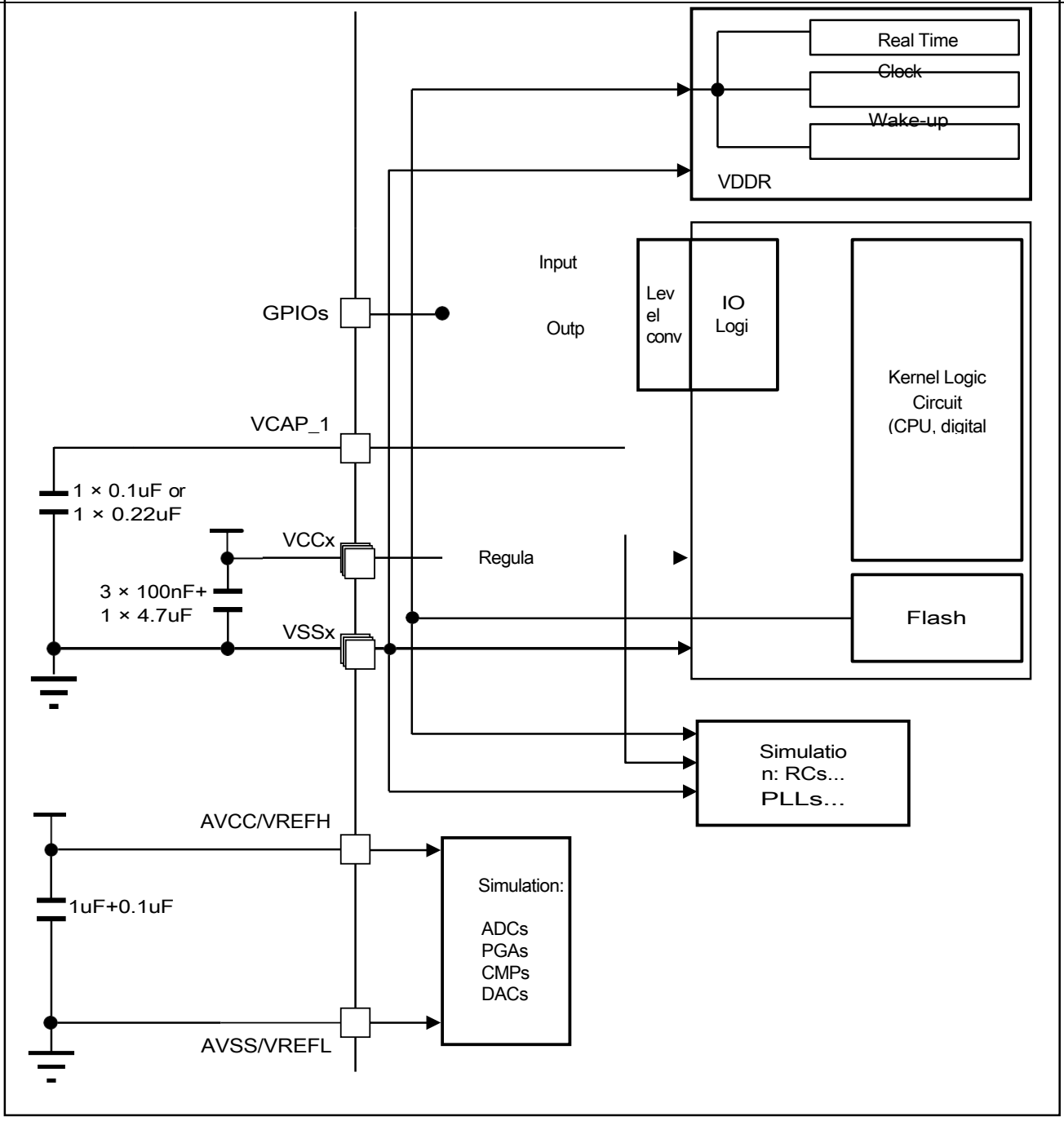


Figure 3-4 Power Supply Solution (HC32F460KEUA-QFN60TR/HC32F460JETA-LQFP48/HC32F460JEUA-QFN48TR)

1. The 4.7μF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS = VSS.
3. Each power pair (e.g. VCC/VSS, AVCC/AVSS ...) must be decoupled using the filtering ceramic capacitors described above. These capacitors must be as close or as low as possible to the appropriate pins below the PCB to ensure proper device operation. Removing the filtering capacitors to reduce PCB size or cost is not recommended. This may cause the device to operate improperly.
4. The capacitors used in the VCAP_1/VCAP_2 pins of the chip are as follows: 1) For chips with both VCAP_1 and VCAP_2 pins, each pin can use 0.047uF or 0.1uF capacitors (total

capacity is 0.094uF or 0.2uF)

(2) For chips with only VCAP_1 pin, 0.1uF or 0.22uF capacitor can be used. When waking up from power-down mode, VCAP_1/VCAP_2 needs to be charged during the core voltage build-up. On the one hand, a smaller total VCAP_1/VCAP_2 capacity reduces the charge time and brings fast response time to the application; on the other hand, a larger total VCAP_1/VCAP_2 capacity extends the charge time, but also provides better electromagnetic compatibility (EMC). The user can choose a larger or smaller capacitance value depending on the EMC and system response speed requirements. The total capacity of VCAP_1/VCAP_2 must match the assignment of PWC_PWRC3.PDTS bit. 0.2uF or 0.22uF for VCAP_1/VCAP_2, make sure the PWC_PWRC3.PDTS bit is cleared before entering power-down mode. If the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, you need to ensure the PWC_PWRC3.PDTS bit is cleared before entering power-down mode.

5. The stability of the main regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin. The capacitance value CEXT is determined according to the stability requirements of the system. The capacitance value CEXT and ESR requirements are as follows:

Table 3-1 VCAP_1/VCAP_2 Operating Conditions

Symbols	Parameters	Conditions
CEXT	Capacitance value of external capacitor	0.047μF / 0.1μF / 0.22uF
ESR	Equivalent series resistance of external capacitor ESR	< 0.3 Ω

3.1.7 Current consumption measurement

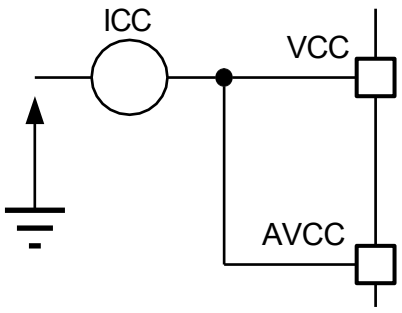


Figure 3-5 Current consumption measurement scheme

3.2 Absolute maximum rating

If the loads applied to the device exceed the absolute maximum ratings listed in Table 3-2 Voltage Characteristics, Table 3-3 Current Characteristics, and Table 3-4 Thermal Characteristics, the device may be permanently damaged. These values are rated stresses only and do not imply that the device functions properly under these conditions. Prolonged operation at maximum rated conditions may affect the reliability of the device.

Table 3-2 Voltage Characteristics

Symbols	Projects	Minimum value	Maximum value	Unit
VCC-VSS	External mains supply voltage (including AVCC, VCC)(1)	-0.3	4.0	V
VIN	Input voltage on 5V withstand voltage pins(2)	VSS-0.3	VCC+4.0 (max. 5.8V)	
	On PA11/USBFS_DM and PA12/USBFS_DP pins The input voltage of	VSS-0.3	4.0	
VESD(HBM)	Electrostatic discharge voltage (human model)	Please refer to 3.3.5 Electrical Sensitivity		–

1. All mains (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the allowed limits.
2. The maximum value of VIN must always be followed. See Table 3-3 for information on the maximum allowable injection current values.

Table 3-3 Current Characteristics

Symbols	Projects	Maximum value	Unit
ΣIVCC	Total current flowing into all VCCx power lines (pull current)(1)	240	mA
ΣIVSS	Total current flowing out of all VSSx grounding lines (potting current) (1)	-240	
IVCC	Maximum current (pull current) flowing into each VCCx power line (1)	100	
IVSS	Maximum current flowing out of each VSSx grounding line (potting current) (1)	-100	
IIO	Output supply current for any I/O and control pins	40	
	Output pull current for arbitrary I/O and control pins	-40	
ΣIIO	Total output supply current on all I/O and control pins	120	
	Total output pull current on all I/O and control pins	-120	

1. All mains (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the allowed limits.

Table 3-4 Thermal Characteristics

Symbols	Projects	Numerical value	Unit
T_{STG}	Storage temperature range	-55 to +125	°C
T_J	Maximum junction temperature	125	°C

3.3 Working conditions

3.3.1 General working conditions

Table 3-5 General working conditions

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
fHCLK	Internal AHB clock frequency	Ultra-high-speed mode [1] PWRC2.DVS=00 PWRC2.DDAS=1111	0	–	200	MHz
		High-speed mode [1] PWRC2.DVS=11 PWRC2.DDAS=1111	0	–	168	
		Ultra low speed mode PWRC2.DVS=10 PWRC2.DDAS=1000	0	–	8	
VCC	Standard working voltage	–	1.8	–	3.6	V
VAVCC(2)	Analog operating voltage	–	1.8	–	3.6	
VIN	Input voltage on 5V withstand voltage pins (3)	2 V ≤ VCC ≤ 3.6 V	-0.3	–	5.5	
		VCC ≤ 2 V	-0.3	–	5.2	
	pa11/usbfs_dm pa12/usbfs_dp Input voltage of the pin		-0.3	–	VCC+0.3	
TJ	Junction temperature range		-40	–	125	°C

1. Mass production test guarantee.
2. If the VREFH pin is present, the following condition must be considered: $V_{AVCC} - V_{REFH} < 1.2$ V.
3. To keep the voltage above VCC+0.3, the internal pull-up/down resistors must be disabled.

3.3.2 Operating conditions at power-up / power-down

TA obeys general working conditions.

Table 3-6 Operating conditions at power-up/power-down

Symbols	Parameters	Minimum value	Maximum value	Unit
tVCC	VCC Rise Time Rate	20	20000	μs/V
	VCC down time rate	20	20000	

3.3.3 Reset and power control module features

Table 3-7 Reset and Power Control Module Characteristics

Symbols	Parameters	Conditions		Minimum value	Typical values	Maximum value	Unit
VBOR	Monitoring voltage of the BOR	Super speed mode	ICG1.BOR_LEV[1:0]=00	1.88	1.99	2.09	V
			ICG1.BOR_LEV [1:0]=01	1.99	2.09	2.20	V
			ICG1.BOR_LEV [1:0]=10	2.09	2.20	2.30	V
			ICG1.BOR_LEV [1:0]=11	2.30	2.40	2.51	V
		High speed mode ultra-low speed mode	ICG1.BOR_LEV[1:0]=00	1.80	1.90	2.00	V
			ICG1.BOR_LEV [1:0]=01	1.90	2.00	2.10	V
			ICG1.BOR_LEV [1:0]=10	2.00	2.10	2.20	V
			ICG1.BOR_LEV [1:0]=11	2.20	2.30	2.40	V
VPVD1	PVD1 monitoring voltage(3)	Super speed mode	PVD1LVL[2:0]=000	1.99	2.09	2.20	V
			PVD1LVL[2:0]=001	2.09	2.20	2.30	V
			PVD1LVL[2:0]=010	2.30	2.40	2.51	V
			PVD1LVL[2:0]=011	2.54	2.67	2.79	V
			PVD1LVL[2:0]=100	2.65	2.77	2.90	V
			PVD1LVL[2:0]=101	2.75	2.88	3.00	V
			PVD1LVL[2:0]=110	2.85	2.98	3.11	V
			PVD1LVL[2:0]=111	2.96	3.08	3.21	V
		High speed mode Ultra low speed mode	PVD1LVL[2:0]=000	1.90	2.00	2.10	V
			PVD1LVL[2:0]=001	2.00	2.10	2.20	V
			PVD1LVL[2:0]=010	2.20	2.30	2.40	V
			PVD1LVL[2:0]=011	2.43	2.55	2.67	V
			PVD1LVL[2:0]=100	2.53	2.65	2.77	V
			PVD1LVL[2:0]=101	2.63	2.75	2.87	V
			PVD1LVL[2:0]=110	2.73	2.85	2.97	V
			PVD1LVL[2:0]=111	2.83	2.95	3.07	V
		Super speed	PVD2LVL[2:0]=000	2.09	2.20	2.30	V

VPVD2	monitoring voltage(3)	mode	PVD2LVL[2:0]=001	2.30	2.40	2.51	V
			PVD2LVL[2:0]=010	2.54	2.67	2.79	V

Symbols	Parameters	Conditions		Minimum value	Typical values	Maximum value	Unit
			PVD2LVL[2:0]=011	2.65	2.77	2.90	V
			PVD2LVL[2:0]=100	2.75	2.88	3.00	V
			PVD2LVL[2:0]=101	2.85	2.98	3.11	V
			PVD2LVL[2:0]=110	2.96	3.08	3.21	V
			PVD2LVL[2:0]=111(2)	1.05	1.15	1.25	V
		High speed mode Ultra low speed mode	PVD2LVL[2:0]=000	2.00	2.10	2.20	V
			PVD2LVL[2:0]=001	2.20	2.30	2.40	V
			PVD2LVL[2:0]=010	2.43	2.55	2.67	V
			PVD2LVL[2:0]=011	2.53	2.65	2.77	V
			PVD2LVL[2:0]=100	2.63	2.75	2.87	V
			PVD2LVL[2:0]=101	2.73	2.85	2.97	V
			PVD2LVL[2:0]=110 (1)	2.83	2.95	3.07	V
			PVD2LVL[2:0]=111(2)	1.00	1.10	1.20	V
Vpvdhyst	PVD1,2 of hysteresis (3)			–	100	–	mV
V_{POR}(1)	Power-up/power-down reset threshold	Rise along VPOR		1.60	1.68	1.76	V
		Descent along the VPDR		1.56	1.64	1.72	V
VPORhyst	POR Hysteresis			–	40	–	mV
IRUSH	Inrush current when the regulator is powered up (POR or from standby call) (wake up)			–	100	150	mA
TNRST	NRST reset minimum width			500	–	–	ns

TIPVD1	PVD1 reset release time		300	380	460	μs
TIPVD2	PVD2 reset release time		300	380	460	μs
TINRST	NRST reset release time		25	35	50	μs
TRIPT	Internal reset time		140	160	200	μs
TRSTBOR	BOR reset release time		440	520	610	μs
TRSTPOR	Power-on reset release time		–	2500	3000	μs

1. Mass production test guarantee.
2. When PVD2LVDL[2:0] = 111, the comparison voltage is the external input comparison voltage of the PVD2EXINP pin.
3. PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops when PVD2LVL[2:0] is set to 111, and PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops when PVD2LVD[2:0] is set to a value other than 111.
4. The hysteresis of PVD1,2 is the difference between the monitoring voltage when VCC is rising and the monitoring voltage when VCC is falling. PVD1 monitoring voltage when VCC is rising = Vpvd1+Vpvdhyst.
   PVD2 monitoring voltage when VCC rises = Vpvd2+Vpvdhyst.

3.3.4 Supply current characteristics

Current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, program location in memory, and the code being run.

The current consumption measurements are described in Figure 3-5 Current consumption measurement scheme. The current consumption measurements for the various modes of operation described in this section are derived from a set of test codes running in FLASH under laboratory conditions.

The specific conditions are as follows:

1) All I/O pins are in input mode with static values (no load)on VCC or VSS.
2) The clock frequency is selected from ultra-high speed mode fHCLK=200MHz, high speed mode fHCLK=168MHz/120MHz/24MHz and ultra-low speed mode fHCLK=8MHz/1MHz.
3) The power consumption modes are: normal operation mode ICC_RUN, sleep mode ICC_SLEEP， stop mode ICC_STP, power-down mode ICC_PD and Dhrystone operation mode ICC_DHRYSTONE.
4) Peripheral clock ON/OFF Please refer to the specific current test items.
5) PLL is on in Super High Speed mode fHCLK=200MHz, High Speed mode fHCLK=168MHz/120MHz.

Table 3-8 Ultra High Speed Mode Current Consumption

Mode	Parameter	Symbol	Conditions	Ta	Product Specifications			Unit
				(°C)	Min	Typ(1)	Max(2)	
Super speed mode	fHCLK= 200MHz	ICC_RUN	while(1),Full module clock OFF	-40	–	16	–	mA
			while(1),full module clock ON	-40	–	29	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	17	–	mA
			CACHE ON	-40	–	19	–	mA
		ICC_SLEEP	Full module clock OFF	-40	–	11	–	mA
			Full modular clock ON	-40	–	24	–	mA
		ICC_RUN	while(1),Full module clock OFF	25	–	16	–	mA
			while(1),full mode Block clock ON	25	–	29	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	17	–	mA
			CACHE ON	25	–	19	–	mA
		ICC_SLEEP	Full module clock OFF	25	–	11	–	mA
			Full modular clock ON	25	–	24	–	mA
		ICC_RUN	while(1),Full module clock OFF	85	–	–	22	mA
			while(1),full mode Block clock ON	85	–	–	35	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	22	mA
			CACHE ON	85	–	–	25	mA
		ICC_SLEEP	Full module clock OFF	85	–	–	17	mA
			Full modular clock ON	85	–	–	30	mA
		ICC_RUN	while(1),full mode Block clock OFF	105	–	–	25	mA

			while(1),full mode Block clock ON	105	–	–	39	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	24	mA
			CACHE ON	105	–	–	29	mA
		ICC_SLEEP	Full module clock OFF	105	–	–	21	mA
			Full modular clock ON	105	–	–	34	mA

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Table 3-9 High-speed

Mode	Parameter	Symbol	Conditions	Ta	Product Specifications			Unit
				(°C)	Min	Typ(1)	Max(2)	
High speed mode	fHCLK= 168MHz	ICC_RUN	while(1),Full module clock OFF	-40	–	13	–	mA
			while(1),full module clock ON	-40	–	23	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	14	–	mA
			CACHE ON	-40	–	15	–	mA
		ICC_SLEEP	Full module clock OFF	-40	–	9	–	mA
			Full modular clock ON	-40	–	19	–	mA
		ICC_RUN	while(1),Full module clock OFF	25	–	13	–	mA
			while(1),full module Clock ON	25	–	23	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	14	–	mA
			CACHE ON	25	–	15	–	mA
		ICC_SLEEP	Full module clock OFF	25	–	9	–	mA
			Full modular clock ON	25	–	19	–	mA
		ICC_RUN	while(1),Full module clock OFF	85	–	–	18	mA
			while(1),full module Clock ON	85	–	–	28	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	18	mA
			CACHE ON	85	–	–	20	mA
		ICC_SLEEP	Full module clock OFF	85	–	–	14	mA
			Full modular clock ON	85	–	–	24	mA
		ICC_RUN	while(1),full module Clock OFF	105	–	–	20	mA
			while(1),full module Clock ON	105	–	–	31	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	19	mA
			CACHE ON	105	–	–	23	mA
		ICC_SLEEP	Full module clock OFF	105	–	–	17	mA
			Full modular clock ON	105	–	–	27	mA

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Table 3-9 High-speed

Table 3-75 High-speed

Mode	Parameter	Symbol	Conditions	Ta	Product Specifications			Unit
				(°C)	Min	Typ(1)	Max(2)	
High speed mode	fHCLK= 120MHz	ICC_RUN	while(1),Full module clock OFF	-40	–	9.5	–	mA
			while(1),full module clock ON	-40	–	16.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	10	–	mA
			CACHE ON	-40	–	11.5	–	mA
		ICC_SLEEP	Full module clock OFF	-40	–	7	–	mA
			Full modular clock ON	-40	–	14.5	–	mA
		ICC_RUN	while(1),Full module clock OFF	25	–	9.5	–	mA
			while(1),when full module ON Chung	25	–	16.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	10	–	mA
			CACHE ON	25	–	11.5	–	mA
		ICC_SLEEP	Full module clock OFF	25	–	7	–	mA
			Full modular clock ON	25	–	14.5	–	mA
		ICC_RUN	while(1),Full module clock OFF	85	–	–	14	mA
			while(1),when full module ON Chung	85	–	–	22	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	14	mA
			CACHE ON	85	–	–	17	mA
		ICC_SLEEP	Full module clock OFF	85	–	–	12	mA
			Full modular clock ON	85	–	–	20	mA
		ICC_RUN	while(1),when full module CHUNG OFF	105	–	–	16	mA
			while(1),when full module ON Chung	105	–	–	25	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	15	mA
			CACHE ON	105	–	–	19	mA
		ICC_SLEEP	Full module clock OFF	105	–	–	15	mA
			Full modular clock ON	105	–	–	22	mA

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Table 3-76 High-speed

Table 3-77 High-speed

Mode	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
High speed mode	fHCLK= 24MHz	ICC_RUN	while(1),Full module clock OFF	-40	–	3	–	mA
			while(1),full module clock ON	-40	–	6	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	3.5	–	mA
		ICC_SLEEP	Full module clock OFF	-40	–	2	–	mA
			Full modular clock ON	-40	–	5.5	–	mA
		ICC_RUN	while(1),full module Clock OFF	25	–	3	–	mA
			while(1),full module Clock ON	25	–	6	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	3.5	–	mA
		ICC_SLEEP	Full module clock OFF	25	–	2	–	mA
			Full modular clock ON	25	–	5.5	–	mA
		ICC_RUN	while(1),Full module clock OFF	85	–	–	8	mA
			while(1),full module Clock ON	85	–	–	12	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	7	mA
		ICC_SLEEP	Full module clock OFF	85	–	–	8	mA
			Full modular clock ON	85	–	–	11	mA
		ICC_RUN	while(1),Full module clock OFF	105	–	–	10	mA
			while(1),full module Clock ON	105	–	–	14	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	8	mA
		ICC_SLEEP	Full module clock OFF	105	–	–	10	mA
			Full modular clock ON	105	–	–	14	mA

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Table 3-12 Ultra-low speed

Mode	Parameter	Symbol	Conditions	Ta	Product Specifications			Unit
				(°C)	Min	Typ(1)	Max(2)	
Ultra low speed mode	fHCLK= 8MHz	ICC_RUN	while(1),Full module clock OFF	-40	–	1	–	mA
			while(1),full module clock ON	-40	–	3.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	1.5	–	mA
		ICC_SLEEP	Full module clock OFF	-40	–	1.2	–	mA
			Full modular clock ON	-40	–	3.2	–	mA
		ICC_RUN	while(1),Full module clock OFF	25	–	1	–	mA
			while(1),all Module Clock ON	25	–	3.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	1.5	–	mA
		ICC_SLEEP	Full module clock OFF	25	–	1.2	–	mA
			Full modular clock ON	25	–	3.2	–	mA
		ICC_RUN	while(1),all Module clock OFF	85	–	–	4	mA
			while(1),full module clock ON	85	–	–	6	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	4	mA
		ICC_SLEEP	Full module clock OFF	85	–	–	3.5	mA
			Full modular clock ON	85	–	–	6	mA
		ICC_RUN	while(1),Full module clock OFF	105	–	–	6	mA
			while(1),all Module Clock ON	105	–	–	7	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	4.5	mA

Table 3-12 Ultra-low speed

		ICC_SLEEP	Full module clock OFF	105	–	–	4	mA
			Full modular clock ON	105	–	–	6.5	mA

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Table 3-13 Ultra-low speed

Mode	Parameter	Symbol	Conditions	Ta	Product Specifications			Unit
				(°C)	Min	Typ(1)	Max(2)	
Ultra low speed mode	fHCLK= 1MHz	ICC_RUN	while(1),Full module clock OFF	-40	–	0.7	–	mA
			while(1),full module clock ON	-40	–	2.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	0.9	–	mA
		ICC_SLEEP	Full module clock OFF	-40	–	0.9	–	mA
			Full modular clock ON	-40	–	2.4	–	mA
		ICC_RUN	while(1),Full module clock OFF	25	–	0.7	–	mA
			while(1),full mode Block clock ON	25	–	2.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	0.9	–	mA
		ICC_SLEEP	Full module clock OFF	25	–	0.9	–	mA
			Full modular clock ON	25	–	2.4	–	mA
		ICC_RUN	while(1),full mode Block clock OFF	85	–	–	4	mA
			while(1),full module clock ON	85	–	–	5	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	3.5	mA
		ICC_SLEEP	Full module clock OFF	85	–	–	3.5	mA
			Full modular clock ON	85	–	–	5	mA
		ICC_RUN	while(1),Full module clock OFF	105	–	–	5	mA
			while(1),full mode Block clock ON	105	–	–	5.5	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	4	mA

Table 3-13 Ultra-low speed

		ICC_SLEEP	Full modular clock OFF	105	–	–	5	mA
			Full modular clock ON	105	–	–	5.5	mA

1. Typ Voltage condition VCC=3.3V
2. Max Voltage condition VCC=1.8~3.6V

Table 3-14 Low Power Mode Current Consumption

Mode	Parameter	Symbol	Conditions (VCC=3.3V)	Ta	Product Specifications			Unit
				(°C)	Min	Typ(1)	Max(2)	
Stop Mode	–	ICC_STP	PWC_PWRC1.STPDAS=00	-40	–	160	–	uA
			PWC_PWRC1.STPDAS=11	-40	–	30	–	uA
			PWC_PWRC1.STPDAS=00	25	–	220	–	uA
			PWC_PWRC1.STPDAS=11	25	–	80	–	uA
			PWC_PWRC1.STPDAS=00	85	–	–	3600	uA
			PWC_PWRC1.STPDAS=11	85	–	–	3400	uA
			PWC_PWRC1.STPDAS=00	105	–	–	4800	uA
			PWC_PWRC1.STPDAS=11(3)	105	–	–	4600	uA
Power down mode	–	ICC_PD	Power down mode 1	-40	–	10	–	uA
			Power down mode 2	-40	–	4	–	uA
			Power down mode 3	-40	–	1.8	–	uA
			Power down mode 4	-40	–	1.8	–	uA
			Power down mode 2+XTAL32+RTC	-40	–	6	–	uA
			Power down mode 2+LRC+RTC	-40	–	9	–	uA
			Power down mode 1	25	–	10	–	uA
			Power down mode 2	25	–	4	–	uA
			Power down mode 3	25	–	1.8	–	uA
			Power down mode 4	25	–	1.8	–	uA
			Power down mode 2+XTAL32+RTC	25	–	6	–	uA
			Power down mode 2+LRC+RTC	25	–	9	–	uA
			Power down mode 1	85	–	–	21	uA
			Power down mode 2	85	–	–	19	uA
			Power down mode 3	85	–	–	19	uA
			Power down mode 4	85	–	–	19	uA

			Power down mode 2+XTAL32+RTC	85	–	–	21	uA
			Power down mode 2+LRC+RTC	85	–	–	21	uA
			Power down mode 1	105	–	–	35	uA

Mode	Parameter	Symbol	Conditions (VCC=3.3V)	Ta	Product Specifications			Unit
				(°C)	Min	Typ(1)	Max(2)	
			Power down mode 2	105	–	–	33	uA
			Power down mode 3	105	–	–	30	uA
			Power-down mode 4 [3]	105	–	–	30	uA
			Power down mode 2+XTAL32+RTC	105	–	–	35	uA
			Power down mode 2+LRC+RTC	105	–	–	35	uA

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V
3. Mass production test guarantee.

Table 3-15 Analog Module Current Consumption

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3V)	Ta	Product Specifications			Unit
				(°C)	Min	Typ	Max	
Module Current	–	ICC_MODULE	XTAL oscillation mode large drive 24MHz	25	–	1.8	–	mA
			Drive 16MHz in oscillation mode	25	–	1	–	mA
			Oscillation mode small drive 10MHz	25	–	0.8	–	mA
			Oscillation mode ultra-small drive 8MHz	25	–	0.6	–	mA
			XTAL 32K	25	–	0.5	–	mA
			HRC	25	–	0.35	–	mA
			PLL (@480MHz)	25	–	2.3	–	mA
			PLL (@240MHz)	25	–	1.4	–	mA
			ADC	25	–	1.2	–	mA
			DAC	25	–	70	–	uA
			CMP	25	–	0.11	–	mA
			PGA	25	–	1	–	mA
			USBFS(1)	25	–	6	–	mA

1. Contains the current when the control section is communicating with the USBPHY.

3.3.5 Electrical sensitivity

Different tests (ESD, LU) are carried out on the chip using specific measurement methods to determine its performance in terms of electrical sensitivity.

3.3.5.1 Electrostatic Discharge (ESD)

An electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with the JESD22-A114/C101 standard.

Table 3-16 ESD Characteristics

Symbols	Parameters	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human model)	T_A = +25 °C according to JESD22-A114	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 °C according to JESD22-C101	1000	

3.3.5.2 Static Latch-up

To evaluate static Latch-up performance, two complementary static Latch-up tests are performed on the chip:

- Apply overvoltage to each power and analog input pin
- Applying current injection to other inputs, outputs and configurable I/O pins these tests comply with the EIA/JESD 78A IC Latch-up standard.

Table 3-17 Static Latch-up Characteristics

Symbols	Parameters	Conditions	Maximum value	Unit
LU	Static Latch-up	T_A = +105 °C, JESD78A compliant	200	mA

3.3.6 Low-power mode wake-up timings

The wake-up time is measured from the wake-up event trigger to the first instruction executed by the CPU:

- For stop or sleep mode: the wakeup event is WFE.
- The WKUP pin is used to wake up from standby, stop, or sleep mode. All timings are tested at ambient temperature and VCC=3.3V.

Table 3-18 Low-power mode wake-up time

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
TSTOP1	Wake up from stop mode	PWC_PWRC1.VHRCSD=1 and PWC_PWRC1.VPLLSD=1, system clock is MRC, program is executed on RAM	2	5	us
TSTOP2	Wake up from stop mode	The system clock is MRC and the program is executed on Flash	8	15	
TPD1(1)	Wake up from power down mode 1	VCAP_1/VCAP_2 total capacity is 0.094uF or 0.1uF	15	25	
		VCAP_1/VCAP_2 total capacity is 0.2uF or 0.22uF	20	30	
TPD2(1)	Wake up from power down mode 2	VCAP_1/VCAP_2 total capacity is 0.094uF or 0.1uF	40	50	
		VCAP_1/VCAP_2 total capacity is 0.2uF or 0.22uF	45	55	
TPD3(1)	Wake up from power down mode 3	VCAP_1/VCAP_2 total capacity is 0.094uF or 0.1uF	2500	3000	
		VCAP_1/VCAP_2 total capacity is 0.2uF or 0.22uF	2500	3000	
TPD4(1)	Wake up from power down mode 4	VCAP_1/VCAP_2 total capacity is 0.094uF or 0.1uF	65	75	
		VCAP_1/VCAP_2 total capacity is 0.2uF or 0.22uF	70	80	

1. The total capacity of VCAP_1/VCAP_2 must match the assignment of PWC_PWRC3.PDTS bit. If the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, make sure the PWC_PWRC3.PDTS bit is cleared before entering power down mode. If the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, make sure the PWC_PWRC3.PDTS bit is cleared before entering power down mode.

3.3.7 I/O Port Features

General input/output characteristics

Table 3-19 I/O Static Characteristics

Symbols	Parameters		Conditions	Minimum value	Typical values	Maximum value	Unit
V_{IL}(1)	Input low level		1.8≤VCC≤3.6	–	–	0.2_{VCC}	V
V_{IH}(1)	Input high level		1.8≤VCC≤3.6	0.8_{VCC}	–	–	V
VHYS	Input hysteresis		1.8≤VCC≤3.6	–	0.2	–	V
I_{LKG}(1)	I/O input leakage current		VSS≤VIN≤VCC	–	–	±1	uA
			VIN = 5.5V(2)	–	–	5	uA
R_{PU}(1)	Weak pull-up equivalent resistance	USBFS_DP, USBFS_DM	–	–	1.5	–	KΩ
		Other input pins except USBFS_DP and USBFS_DM	VIN = VSS	–	30	–	KΩ
CIO	I/O pin capacitance	pa11/usbfs_dm pa12/usbfs_dp	–	–	10	–	pF
		In addition to the PA11/USBFS_DM and PA12/USBFS_DP other inputs In pin	–	–	5	–	pF

1. Mass production test guarantee.
2. To keep the voltage above VCC+0.3 V, the internal pull-up/down resistors must be disabled.

Output Voltage

Table 3-20 Output Voltage Characteristics

Driver settings	Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
Low drive	V_{OL}(1)(2)	Low level output	IIO=±1.5mA, 1.8≤VCC<2.7	–	–	0.4	V
	V_{OH}(1)(3)	High level output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low level output	IIO=±3mA, 2.7≤VCC≤3.6	–	–	0.4	
	V_{OH}(1)(3)	High level output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low level output	IIO=±6mA, 2.7≤VCC≤3.6	–	–	1.3	
	V_{OH}(1)(3)	High level output		VCC-1.3	–	–	
Medium drive	V_{OL}(1)(2)	Low level output	IIO=±3mA, 1.8≤VCC<2.7	–	–	0.4	
	V_{OH}(1)(3)	High level output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low level output	IIO=±5mA, 2.7≤VCC≤3.6	–	–	0.4	
	V_{OH}(1)(3)	High level output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low level output	IIO=±12mA, 2.7≤VCC≤3.6	–	–	1.3	
	V_{OH}(1)(3)	High level output		VCC-1.3	–	–	
High drive	V_{OL}(1)(2)	Low level output	IIO=±6mA, 1.8≤VCC<2.7	–	–	0.4	
	V_{OH}(1)(3)	High level output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low level output	IIO=±8mA, 2.7≤VCC≤3.6	–	–	0.4	
	V_{OH}(1)(3)	High level output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low level output	IIO=±20mA, 2.7 ≤VCC≤3.6	–	–	1.3	
	V_{OH}(1)(3)	High level output		VCC-1.3	–	–	

1. Mass production test guarantee.
2. The I_{IO} supply current of the device must always take into account the absolute maximum rating specified in Table 3-3. The sum of I_{IO} (IO ports and control pins) must

not exceed I_{VSS}.

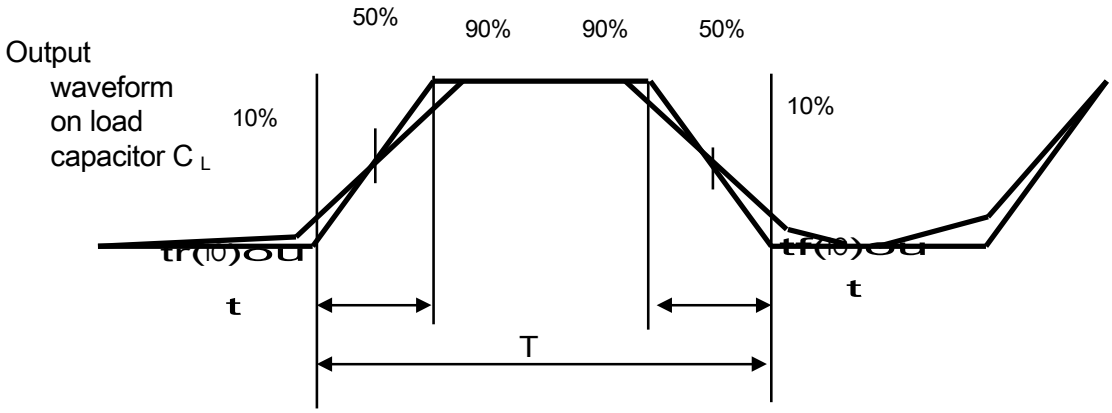
3. The I_{IO} pull current of the device must always follow the absolute maximum ratings listed in Table 3-3, and the sum of the I_{IOs} (I/O ports and control pins) must not exceed I_{VCC}.

Input/output AC characteristics

Table 3-21 I/O AC Characteristics

Driver settings	Symbols	Parameters	Conditions[3]	Minimum value	Typical values	Maximum value	Unit
Low drive	$f_{max(IO)out}$	Maximum frequency[1]	CL=30 pF, VCC≥ 2.7V	–	–	20	MHz
			CL=30 pF, VCC≥1.8V	–	–	10	
			CL=10pF, VCC≥2.7V	–	–	40	
			CL=10pF, VCC≥1.8V	–	–	20	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	–	–	15	ns
			CL=30 pF, VCC≥1.8V	–	–	25	
			CL=10pF, VCC≥2.7V	–	–	7.5	
			CL=10pF, VCC≥1.8V	–	–	15	
Medium drive	$f_{max(IO)out}$	Maximum frequency[1]	CL=30 pF, VCC≥ 2.7V	–	–	45	MHz
			CL=30 pF, VCC≥1.8V	–	–	22.5	
			CL=10pF, VCC≥2.7V	–	–	90	
			CL=10pF, VCC≥1.8V	–	–	45	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	–	–	7.5	ns
			CL=30 pF, VCC≥1.8V	–	–	12	
			CL=10pF, VCC≥2.7V	–	–	4	
			CL=10pF, VCC≥1.8V	–	–	7.5	
High drive	$f_{max(IO)out}$	Maximum frequency[1]	CL=30 pF, VCC≥2.7V	–	–	100	MHz
			CL=30 pF, VCC≥1.8V	–	–	50	
			CL=10pF, VCC≥2.7V	–	–	180	
			CL=10pF, VCC≥1.8V	–	–	100	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	–	–	4	ns
			CL=30 pF, VCC≥1.8V	–	–	6	
			CL=10pF, VCC≥2.7V	–	–	2.5	
			CL=10pF, VCC≥1.8V	–	–	4	

1. The maximum frequency is defined in Figure 3-6.
2. The load capacitance C_L must take into account the capacitance of the PCB and MCU pins (the pin-to-board capacitance can be roughly estimated at 10 pF)



Maximum frequency condition: $(t_r + t_f) \leq (2/3)T$ and Duty cycle= 50%±5%

(Load capacitance C_L is indicated in the "Conditions" column of the "Input/Output AC Characteristics" table)

Figure 3-6 I/O AC Characteristics Definition

3.3.8 USART

Interface Features

Table 3-22 USART AC Timing

Symbols	Parameters		Minimum value	Maximum value	Unit
tcyc	Number of input clock cycles	UART	4	–	tPCLK1
		CSI	6	–	
tCKw	Input Clock Width		0.4	0.6	tScyc
tCKr	Input Clock Rise Time		–	5	ns
tCKf	Input clock down time		–	5	ns
tTD	Sending delay time	CSI	–	28	ns
tRDS	Receive data build time	CSI	15	–	ns
tRDH	Receive data hold time	CSI	5	–	ns

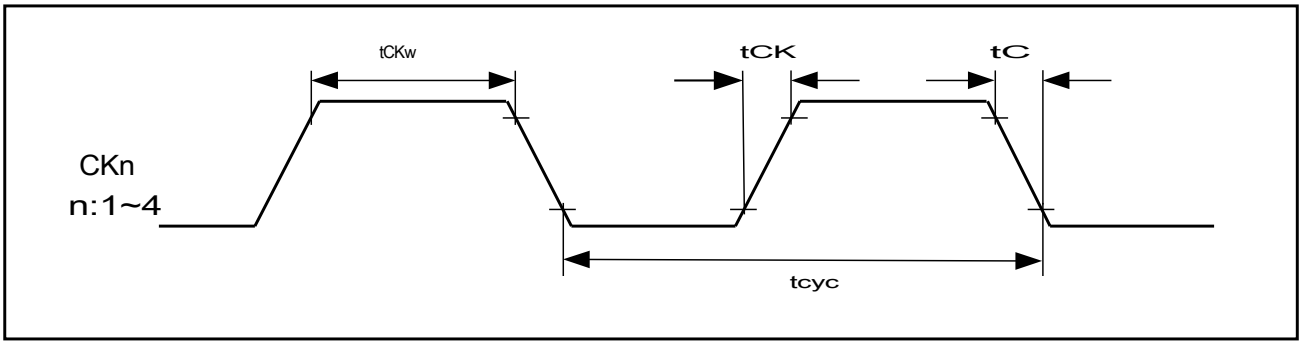


Figure 3-7 USART Clock Timing

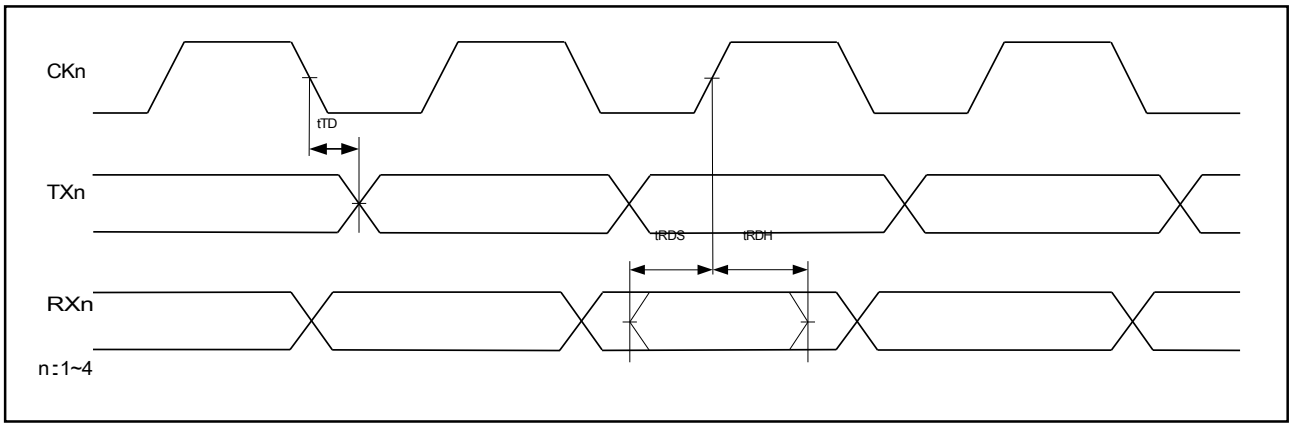


Figure 3-8 USART (CSI) Input and Output Timing

3.3.9 I2S Interface Features

Table 3-23 I2S Electrical Characteristics

Symbols	Performance Indicators	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	–	256*8K	256*Fs	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	20	64*Fs	MHz
		Slave data: 32 bits	–	64*Fs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
t_{v}(WS)	WS valid time	Master mode	0	–	ns
t_{h}(WS)	WS hold time	Master mode	0	–	
t_{su}(WS)	WS setup time	Slave mode	1	–	
t_{h}(WS)	WS hold time	Slave mode	0	–	
t_{su}(SD_MR)	Data input setup time	Master receiver	7.5	–	
t_{su}(SD_SR)		Slave receiver	2	–	
t_{h}(SD_MR)	Data input hold time	Master receiver	0	–	
t_{h}(SD_SR)		Slave receiver	0	–	
t_{v}(SD_ST) t_{h}(SD_ST)	Data output valid time	Slave transmitter(after enable edge)	–	27	
t_{v}(SD_MT)		Master transmitter(after enable edge)	–	20	
t_{h}(SD_MT)	Data output hold time	Master transmitter(after enable edge)	2.5	–	

1. Fs: I2S sampling frequency

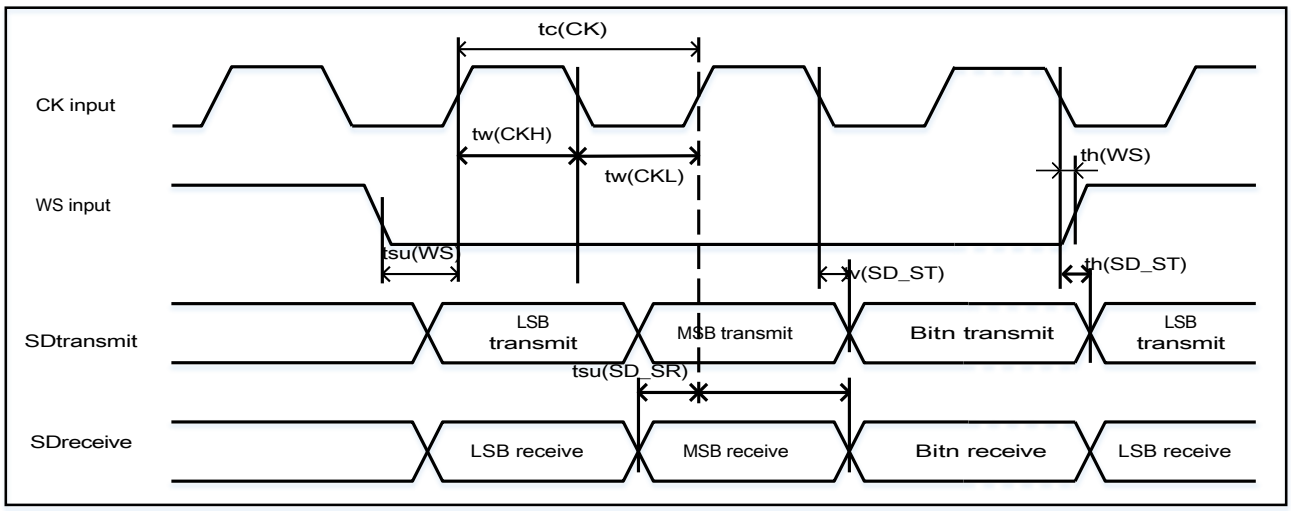


Figure 3-9 I2S Slave Mode Timing (Philips Protocol)

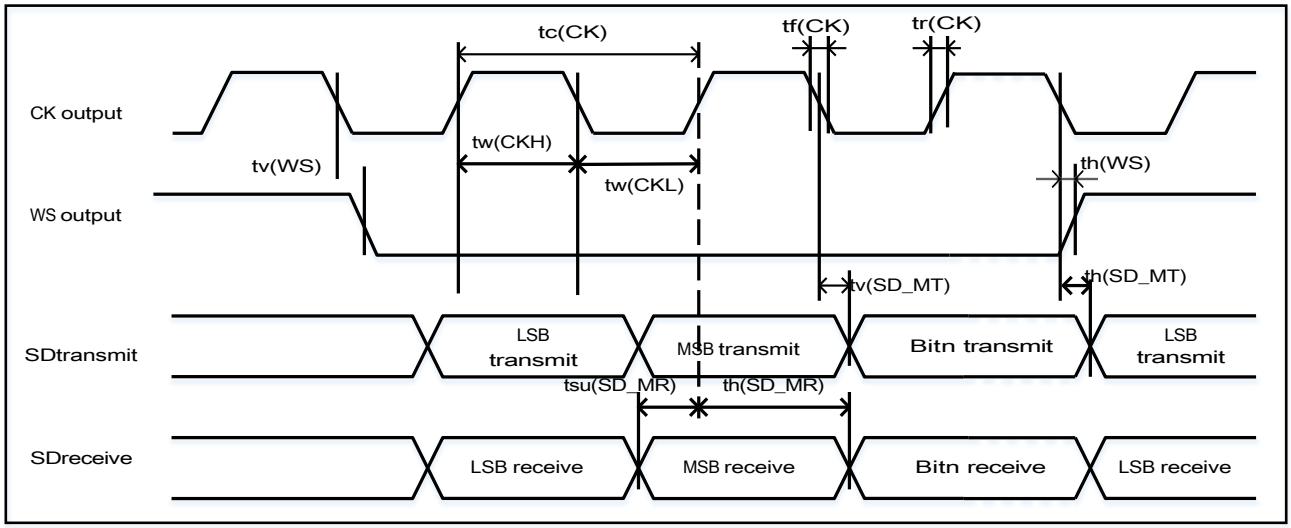


Figure 3-10 I2S Master Mode Timing (Philips Protocol)

3.3.10 I2C Interface Features

Table 3-24 I2C Electrical Characteristics

Symbols	Parameters	Standard Mode (SM)		Fast Mode (FM)		Unit
		Min	Max	Min	Max	
fSCL	SCL Frequency	0	100	0	400	KHz
tHD;STA	Start condition/restart condition Hold	4.0	–	0.6	–	us
tLOW	SCL low	4.7	–	1.3	–	us
tHIGH	SCL high level	4	–	0.6	–	us
tSU;STA	Restart conditionSetup	4.7	–	0.6	–	us
tHD;DAT	Data Hold	0	–	0	–	us
tSU;DAT	DataSetup	50+ tI2C reference clock period	–	50+ tI2C reference clock period	–	ns
tR	Rise time of SCL/SDA	–	1000	6.5	300	ns
tF	SCL/SDA drop time	–	300	6.5	300	ns
tSU;STO	Stop conditionSetup	4	–	0.6	–	us
tBUF	BUS idle time between stop condition and start condition	4.7	–	1.3	–	us
Cb	Load capacitance	–	400	–	400	pF

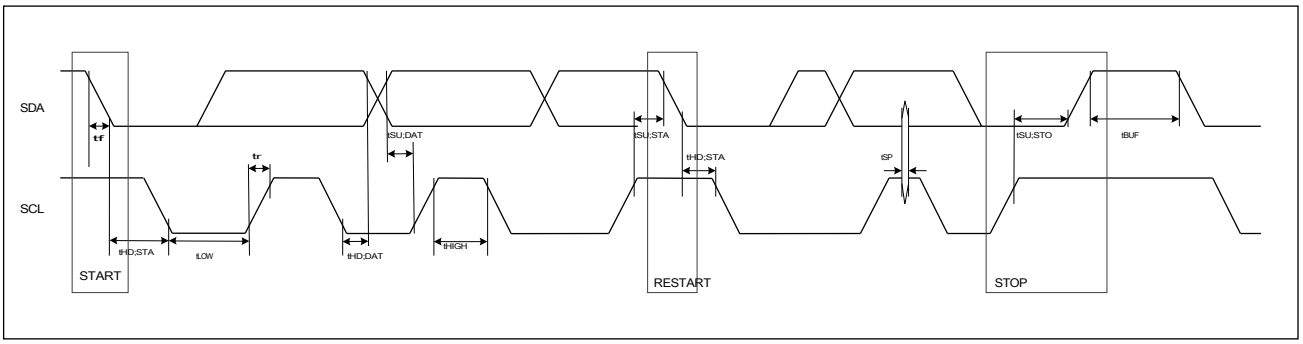


Figure 3-11 I2C Bus Timing Definition

3.3.11 SPI Interface Features

Table 3-25 SPI Electrical Characteristics

Item		Symbol	Min	Max	Unit	Test conditions
SCK clock cycle	Master	tspcyc	2 (pclk ≤60MHz) 4 (pclk ≤60MHz)	4096	tpcyc	Figure 3-12 C=30pF
	Slave		6	4096		
SCK clock rise and fall time	Master	tsckr	–	5	ns	
	Slave	tsckf	–	1	us	
Data input setup time	Master	tsu	4	–	ns	Figure 3-13 C=30pF
	Slave		5	–		
Data input hold time	Master	th	tpcyc	–	ns	
	Slave		20	–		
Data output delay	Master	tod	–	8	ns	
	Slave		–	20		
Data output hold time	Master	toh	0	–	ns	
	Slave		0	–		
MOSI/MISO rise and fall time	Master	tdr	–	5	ns	
	Slave	tdf	–	1	us	
SS rise and fall time	Master	tssr	–	5	ns	
	Slave	tssf	–	1	us	

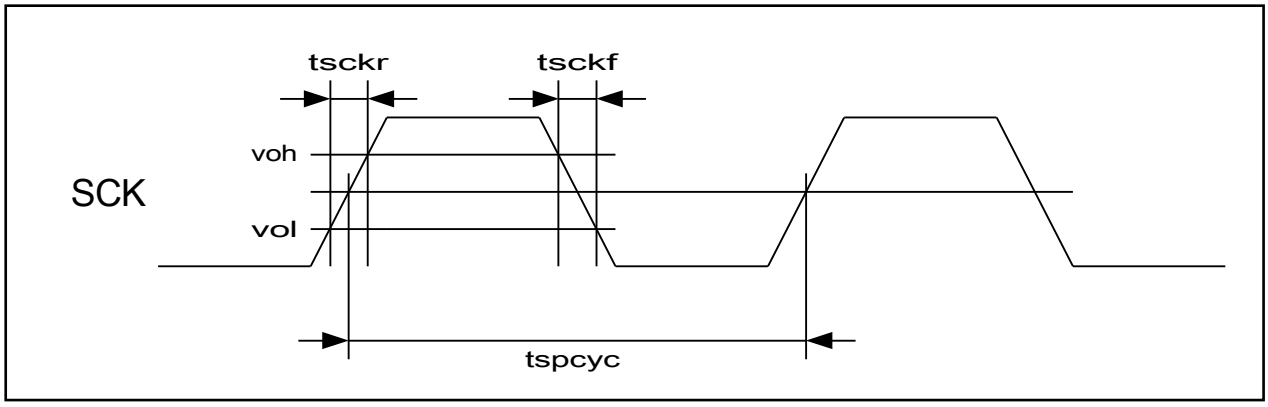


Figure 3-12 SCK Clock Definition

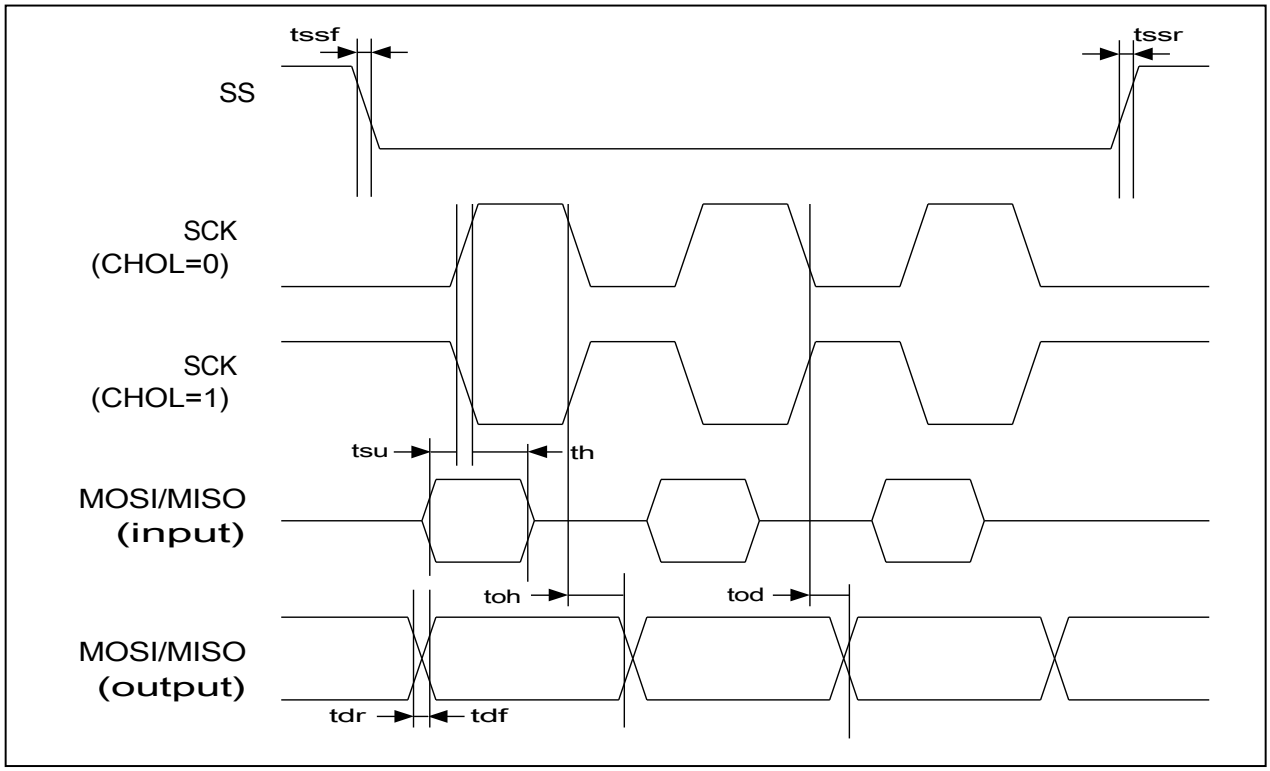


Figure 3-13 SPI Interface Timing Requirements

3.3.12 CAN2.0B Interface Features

For the port characteristics of CANx_TX and CANx_RX, please refer to 3.3.7 I/O Port Characteristics.

3.3.13 USB Interface Features

Table 3-26 USB Full-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input	V_{CC}	Operating Voltage	–	3.0(2)	–	3.6	V
	V_{IL}	Input low level	–	–	–	0.8	V
	V_{IH}	Input high level	–	2.0	–	–	V
	V_{DI}	Differential input sensitivity	–	0.2	–	–	V
	V_{CM}	Differential common mode voltage	–	0.8	–	2.5	V
Output	V_{OL}(3)	Static output low level	RL=1.5kΩ to 3.6V(4)	–	–	0.3	V
	V_{OH}(3)	Static output high level	RL=15kΩ to VSS(4)	2.8	–	3.6	V
	VCRS	Cross-over voltage	CL=50pF	1.3	–	2.0	V
	tR	Rise time	CL=50pF. 10%~90% of |VOH-VOL|	4	–	20	ns
	tF	Descent time	CL=50pF. 10%~90% of |VOH-VOL|	4	–	20	ns
	tRFMA	Rise and fall time ratio tR/tF	CL=50pF	90	–	111.1	%
R_{PD}(3)		Pull Down Resistors	VIN= V_{CC}, in host mode	–	15	–	kΩ
R_{PU}(3)		Pull-up resistors	VIN= V_{SS}, idle state	0.900	1.2	1.575	kΩ
			VIN= V_{SS}. in device mode	1.425	2.3	3.090	kΩ

1. All voltages were measured based on local ground potential.
2. Operating voltage drops to 2.7V still guarantees USB full-speed transceiver functionality, but not full USB full-speed electrical characteristics, which degrade over the V_{CC} voltage range of 2.7 to 3.0V.
3. Mass production test guarantee.
4. R_L is the load connected to the USB full-speed drive.

Table 3-27 USB Low-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input	V_{CC}	Operating Voltage	–	3.0(2)	–	3.6	V
	V_{IL}	Input low level	–	–	–	0.8	V
	V_{IH}	Input high level	–	2.0	–	–	V
	V_{DI}	Differential input sensitivity	–	0.2	–	–	V
	V_{CM}	Differential common mode voltage	–	0.8	–	2.5	V
Output	V_{OL}(3)	Static output low level	RL=1.5kΩ to 3.6V(4)	–	–	0.3	V
	V_{OH}(3)	Static output high level	RL=15kΩ to VSS(4)	2.8	–	3.6	V
	V_{CRS}(3)	Cross-over voltage	CL=200pF~600pF	1.3	–	2.0	V
	t_R(3)	Rise time	CL=200pF~600pF, 10%~90% of |VOH-VOL|	75	–	300	ns
	t_F(3)	Descent time	CL=200pF~600pF, 10%~90% of |VOH-VOL|	75	–	300	ns
	t_{RFMA}(3)	Rise and fall time ratio	CL=200pF~600pF	80	–	125	%
R_{PD}(3)		Pull Down Resistors	VIN= V_{CC}, in host mode	14.25	–	24.80	kΩ

1. All voltages were measured based on local ground potential.
2. The USB low-speed transceiver function is still guaranteed when the operating voltage drops to 2.7V, but the full USB low-speed electrical characteristics are not guaranteed, which deteriorate over the 2.7 to 3.0V V_{CC} voltage range.
3. Mass production test guarantee.
4. R_L is the load connected to the USB low-speed drive.

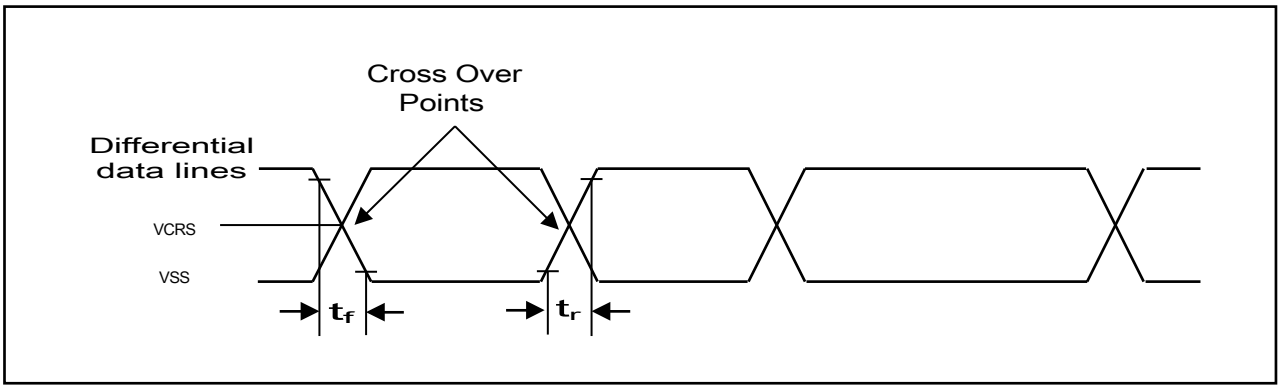


Figure 3-14 USB Rise/Fall Time and Cross Over Voltage Definition

3.3.14 PLL Features

Table 3-28 PLL Key Performance Indicators

Symbols	Parameters	Conditions	Min	Typ	Max	Unit
fPLL_IN	PLL PFD(Phase Frequency Detector) input clock(1)	–	1	–	25	MHz
fPLL_OUT	PLL multiplier output clock	–	15	–	240	MHz
fVCO_OUT	PLL VCO output	–	240	–	480	MHz
JitterPLL	Period Jitter	PLL PFD input clock=8MHz. System clock=120MHz. Peak-to-Peak	–	±100	–	ps
	Cycle-to-Cycle Jitter	PLL PFD input clock=8MHz. System clock=120MHz. Peak-to-Peak	–	±150	–	
tLOCK	PLL lock time	–	–	80	120	μs

1. It is recommended to use a higher input clock to obtain good Jitter characteristics.

3.3.15 JTAG interface features

Table 3-29 JTAG Interface Features

Synbol	Item	Min	Typ	Max	Unit
tTCKcyc	JTCK clock cycle time	50	–	–	ns
tTCKH	JTCK clock high pulse width	20	–	–	ns
tTCKL	JTCK clock low pulse width	20	–	–	ns
tTCKr	JTCK clock rise time	–	–	5	ns
tTCKf	JTCK clock fall time	–	–	5	ns
tTMSs	JTMS setup time	8	–	–	ns
tTMSh	JTMS hold time	8	–	–	ns
tTDIs	JTDI setup time	8	–	–	ns
tTDIh	JTDI hold time	8	–	–	ns
tTDOd	JTDO data delay time	–	–	20	ns

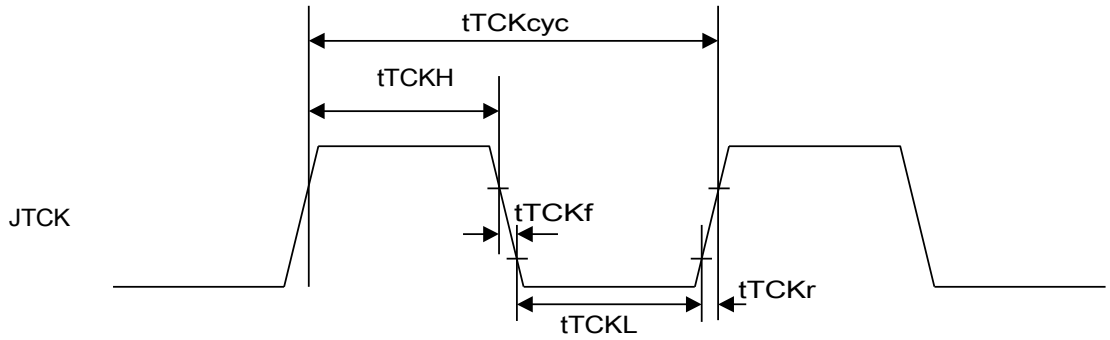


Figure 3-15 JTAG JTCK clock

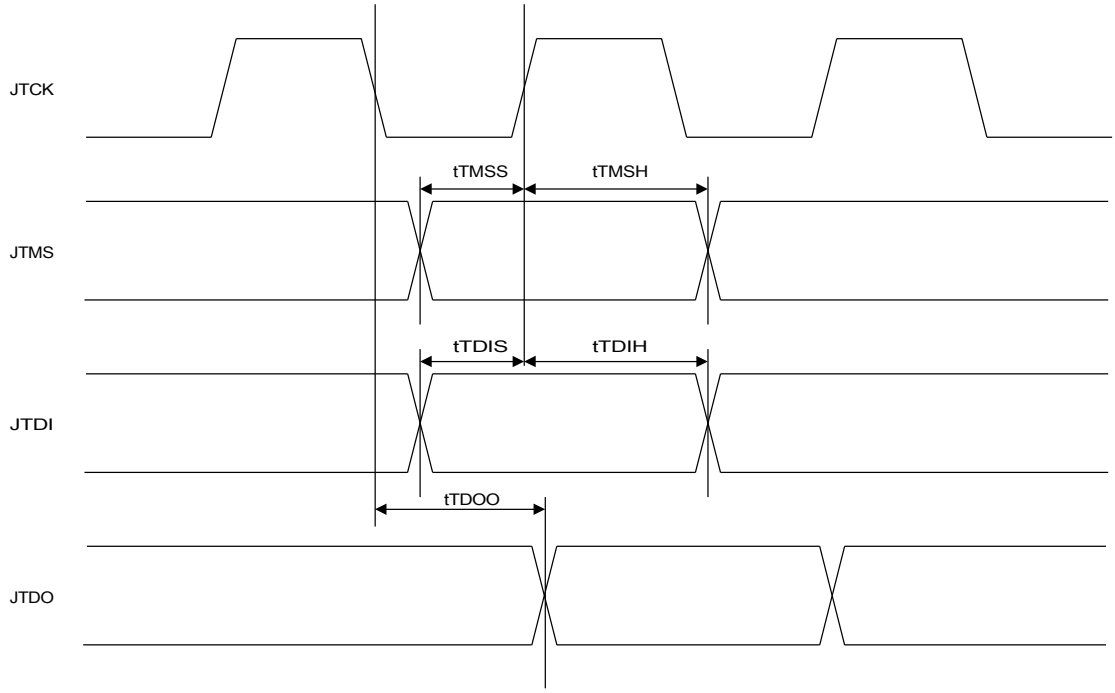


Figure 3-16 JTAG input and output

3.3.16 External clock source characteristics

3.3.16.1 High-speed external user clock generated by external sources

In bypass mode, the XTAL oscillator is off and the input pins are standard I/O. The external clock signal must take into account the static characteristics.

Table 3-30 High-speed external user clock characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{XTAL_EXT}	User external clock source frequency	–	1	–	25	MHz
V_{IH_XTAL}	XTAL_EXT input pin high		$0.8*V_{CC}$	–	V_{CC}	V
V_{IL_XTAL}	XTAL_EXT input pin low		V_{SS}	–	$0.2*V_{CC}$	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_EXT rise or fall time		–	–	5	ns
$Duty_{(XTAL)}$	Duty Cycle	–	40	–	60	%

3.3.16.2 Crystal / Ceramic Resonator Generates High Speed External Clock

A high-speed external (XTAL) clock can be generated using a 4 to 25 MHz crystal/ceramic resonator oscillator. In applications, the resonator and load capacitor must be placed as close to the oscillator pins as possible to minimize output distortion and settling time. For more information on resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-31 XTAL 4-25 MHz Oscillator Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{XTAL_IN}	Oscillator frequency		4	–	25	MHz
R_F(1)	Feedback Resistor		–	300	–	kΩ
A_{XTAL}(2)	XTAL Accuracy	–	-500	–	500	ppm
G_{mmax}	Oscillator G_m	Vibration	4	–	–	mA/V
$t_{SU(XTAL)}$(3)	Start-up time	VCC stable, crystal = 8MHz	–	2.0	–	ms
		VCC stable, crystal = 4MHz	–	4.0	–	ms

1. Mass production test guarantee.
2. This parameter depends on the resonator used in the application.
3. $t_{SU(XTAL)}$ is the start-up time, which is the time measured from the time the XTAL is enabled by software until a stable 8MHz oscillation frequency is obtained. This value is based on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high quality external ceramic capacitors designed for high frequency applications that can meet the requirements of a crystal or resonator (see figure below) C_{L1} and C_{L2} are usually the same size, CL1=CL2=2*(CL-Cs) Cs is the PCB and MCU pins (XTAL_IN, XTAL_OUT) stray capacitance.

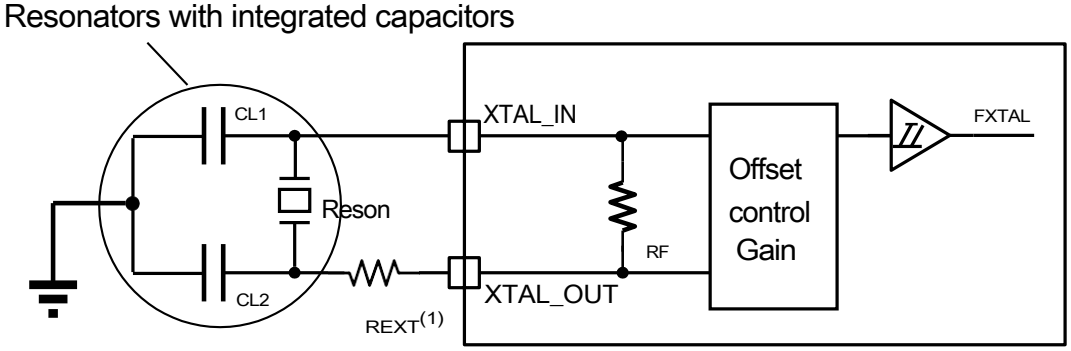


Figure 3-17 Typical Application with 8 MHz Crystal

1. The value of $_{REXT}$ depends on the crystal characteristics.

3.3.16.3 Crystal / Ceramic Resonator Generated Low Speed External Clock

A low-speed external clock can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. In applications, the resonator and load capacitor must be placed as close to the oscillator pins as possible to minimize output distortion and start-up stability time. For more information on resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-32 XTAL32 Oscillator Characteristics

Symbols	Parameters	Conditions	Specification			Unit
			Min	Typ	Max	
F_{XTAL32}	Frequency	–	–	32.768	–	kHz
R_F(1)	Feedback Resistor	–	–	15	–	MΩ
I_{DD_XTAL32}	Power consumption	XTAL32DRV[2:0]=000	–	0.8	–	μA
A_{XTAL32}(2)	XTAL32 Accuracy	–	-500	–	500	ppm
G_{mmax}	Oscillator Gm	–	5.6	–	–	uA/V
$T_{SUXTAL32}$	Start-up time(3)	VCC steady state	–	2	–	s

1. Mass production test guarantee.
2. This parameter depends on the resonator used in the application.
3. $T_{SUXTAL32}$ is the start-up time, which is the time measured from the time XTAL32 is enabled by software until a stable 32.768 kHz oscillation frequency is obtained. This value is based on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high quality external ceramic capacitors (see figure below) C_{L1} and C_{L2} are usually the same size, CL1=CL2=2*(CL-Cs). cs is the PCB and MCU pin (XTAL32_IN, XTAL32_OUT) stray capacitance. if C_{L1} and C_{L2} are larger than 18pF, it is recommended to set XTAL32DRV[2:0]=001 (large drive, power consumption Typical value increases by 0.2uA)

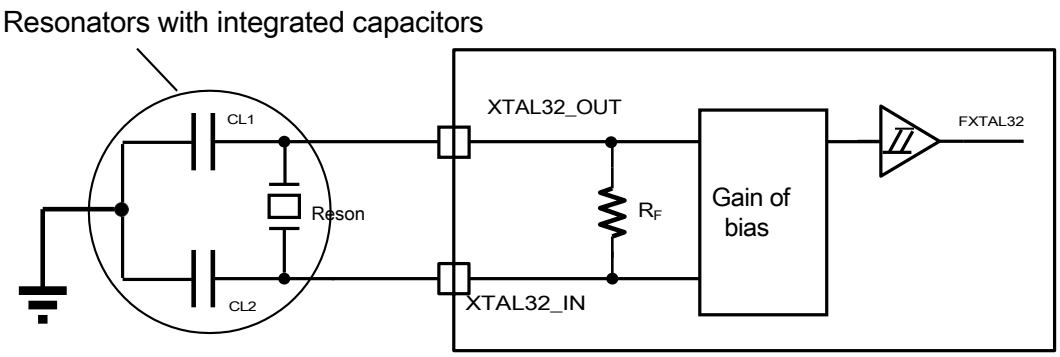


Figure 3-18 Typical Application with 32.768 kHz Crystal

3.3.17 Internal clock source characteristics

3.3.17.1 Internal high speed (HRC) oscillator

Table 3-33 HRC oscillator characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{HRC}	Frequency(1)	Mode 1	–	16	–	MHz
		Mode 2	–	20	–	
	User adjustable scale	–	–	–	0.2	%
	Frequency accuracy(1)	T_A = -40 to 105 °C	-2	–	2	%
		T_A = -20 to 105 °C	-1.5	–	1.5	%
		T_A = 25 °C	-0.5	–	0.5	%
$t_{st(HRC)}$	HRC oscillator oscillation stability time	–	–	–	15	μs

1. Mass production test guarantee.

3.3.17.2 Internal medium speed (MRC) oscillator

Table 3-34 MRC Oscillator Characteristics

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit
f_{MRC}(1)	Frequency	7.2	8	8.8	MHz
$t_{st(MRC)}$	MRC oscillator stabilization time	–	–	3	μs

1. Mass production test guarantee.

3.3.17.3 Internal low speed (LRC) oscillator

Table 3-35 LRC oscillator characteristics

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit
f_{LRC}(1)	Frequency	27.853	32.768	37.683	kHz
$t_{st(LRC)}$	LRC oscillator stabilization time	–	–	36	μs

1. Mass production test guarantee.

3.3.17.4 SWDT dedicated internal low-speed (SWDTLRC) oscillator

Table 3-36 SWDTLRC Oscillator Characteristics

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit
$f_{SWDTLRC}$(1)	Frequency	9	10	11	kHz
tst(SWDTLRC)	SWDTLRC oscillator stabilization time	–	–	57.1	μs

1. Mass production test guarantee.

3.3.18 12-bit ADC

Features

Table 3-37 ADC Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{AVCC}	Power supply	–	1.8	–	3.6	V
V_{REFH}(1)	Positive reference voltage	–	1.8	–	V_{AVCC}	V
f_{ADC}	ADC conversion clock frequency	VAVCC=2.4 ~3.6V in ultra-high speed/high speed action mode	1	–	60	MHz
		VAVCC=1.8 ~2.4V in ultra-high speed/high speed action mode	1	–	30	
		Ultra low speed action mode	1	–	8	
V_{AIN}	Conversion voltage range	–	V_{AVSS}	–	V_{REFH}	V
R_{AIN}	External Input Impedance	See Equation 1 for details	–	–	50	kΩ
R_{ADC}	Sampling switch resistance	–	–	–	6	kΩ
C_{ADC}	Internal sample and hold capacitors	–	–	4	7	pF
t_D	Trigger transition delay	f_{ADC} = 60 MHz	–	–	0.3	μs

Table 3-38 ADC Characteristics (continued)

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
tS	Sampling time	fADC=60MHz	0.183	–	4.266	μs
			11	–	255	1/ fADC
tCONV	Total conversion time per channel (including sampling time)	fADC = 60 MHz 12-bit resolution	0.4	–	–	μs
		fADC = 60 MHz 10-bit resolution	0.36	–	–	μs
		fADC = 60 MHz 8-bit resolution	0.33	–	–	μs
		20 to 268 (sampling time tS+ converging n-bit resolution + 1)				1/fADC
fS	Sampling rate fADC = 60 MHz	12-bit resolution single ADC	–	–	2.5	Msps
		12-bit resolution time-interpolated dual ADC	–	–	4.6	
tST	Power-up time	–	–	1	2	μs

1. VAVCC-VREFH<1.2V

Formula 1: RAIN maximum value formula

$$\square\square\square\square = \frac{k-1}{\square\square\square \times C \times \ln(2^{N+2})} - RADC$$

The above equation (Equation 1) is used to determine the maximum external impedance to bring the error below 1/4 LSB. Where N = 12 (12-bit resolution) and k is the number of sampling periods defined in the ADC_SSTR register.

Table 3-39 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=60MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error	Ultra-high speed/high speed action mode fADC=60MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±4.5	±6	LSB
EO	Offset Error		±3.5	±6	LSB
EG	Gain error		±3.5	±6	LSB
ED	Differential linear error		±1	±2	LSB
EL	Integral linearity error		±1.5	±3	LSB

Table 3-40 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=30MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error	Ultra-high speed/high speed action mode fADC=30MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±4.5	±6	LSB
EO	Offset Error		±3.5	±6	LSB
EG	Gain error		±3.5	±6	LSB
ED(1)	Differential linear error		±1	±2	LSB
EL(1)	Integral linearity error		±1.5	±3	LSB

1. Mass production test guarantee.

Table 3-41 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=30MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error	Ultra-high speed/high speed action mode fADC=30MHz Input source impedance <1kΩ VAVCC=1.8 ~2.4V	±4.5	±6	LSB
EO	Offset Error		±3.5	±6	LSB
EG	Gain error		±3.5	±6	LSB
ED	Differential linear error		±1	±2	LSB
EL	Integral linearity error		±2	±3	LSB

Table 3-42 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=8MHz

Symbo	Par	Con	Typic	Maxi	Unit

ls	ame ters	diti ons	al value s	mum value	
ET	Absolute error	Ultra-low speed action mode fADC=8MHz Input source impedance <1kΩ VAVCC=1.8 ~3.6V	±4.5	±6	LSB
EO	Offset Error		±3.5	±6	LSB
EG	Gain error		±3.5	±6	LSB
ED	Differential linear error		±1	±2	LSB
EL	Integral linearity error		±2	±3	LSB

Table 3-43 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=60MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error	Ultra-high speed/high speed action mode fADC=60MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±5.5	±7	LSB
EO	Offset Error		±4.5	±7	LSB
EG	Gain error		±4.5	±7	LSB
ED	Differential linear error		±1.5	±2	LSB
EL	Integral linearity error		±2.0	±3	LSB

Table 3-44 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=30MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error	Ultra-high speed/high speed action mode fADC=30MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±5.5	±7	LSB
EO	Offset Error		±4.5	±7	LSB
EG	Gain error		±4.5	±7	LSB
E_D(1)	Differential linear error		±1.5	±2	LSB
E_L(1)	Integral linearity error		±2.0	±3	LSB

1. Mass production test guarantee.

Table 3-45 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=30MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error	Ultra-high speed/high speed action mode fADC=30MHz Input source impedance <1kΩ VAVCC=1.8 ~2.4V	±5.5	±7	LSB
EO	Offset Error		±4.5	±7	LSB
EG	Gain error		±4.5	±7	LSB
ED	Differential linear error		±1.5	±2	LSB
EL	Integral linearity error		±2.5	±3	LSB

Table 3-46 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=8MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error		±5.5	±7	LSB

EO	Offset Error	action mode	±4.5	±7	LSB
EG	Gain error	fADC=8MHz	±4.5	±7	LSB
ED	Differential linear error	Input source	±1.5	±2	LSB
EL	Integral linearity error	impedance <1kΩ VAVCC=1.8 ~3.6V	±2.5	±3	LSB

Table 3-47 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy @ fADC=60MHz

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
ENOB	Valid digits	Ultra-high speed/high speed action mode fADC=60MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	10.6	–	Bits
SINAD	Signal-to-noise harmonic ratio		64	–	dB
SNR	Signal-to-noise ratio		66	–	dB
THD	Total Harmonic Distortion		–	-70	dB

Table 3-48 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy @ fADC=30MHz

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
ENOB	Valid digits	Ultra-high speed/high speed action mode fADC=30MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=1.8~2.4V	10.4	–	Bits
SINAD	Signal-to-noise harmonic ratio		62	–	dB
SNR	Signal-to-noise ratio		64	–	dB
THD	Total Harmonic Distortion		–	-67	dB

Table 3-49 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy @ fADC=8MHz

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
ENOB	Valid digits	Ultra-low speed action mode fADC=8MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=1.8~3.6V	10.4	–	Bits
SINAD	Signal-to-noise harmonic ratio		62	–	dB
SNR	Signal-to-noise ratio		64	–	dB
THD	Total Harmonic Distortion		–	-67	dB

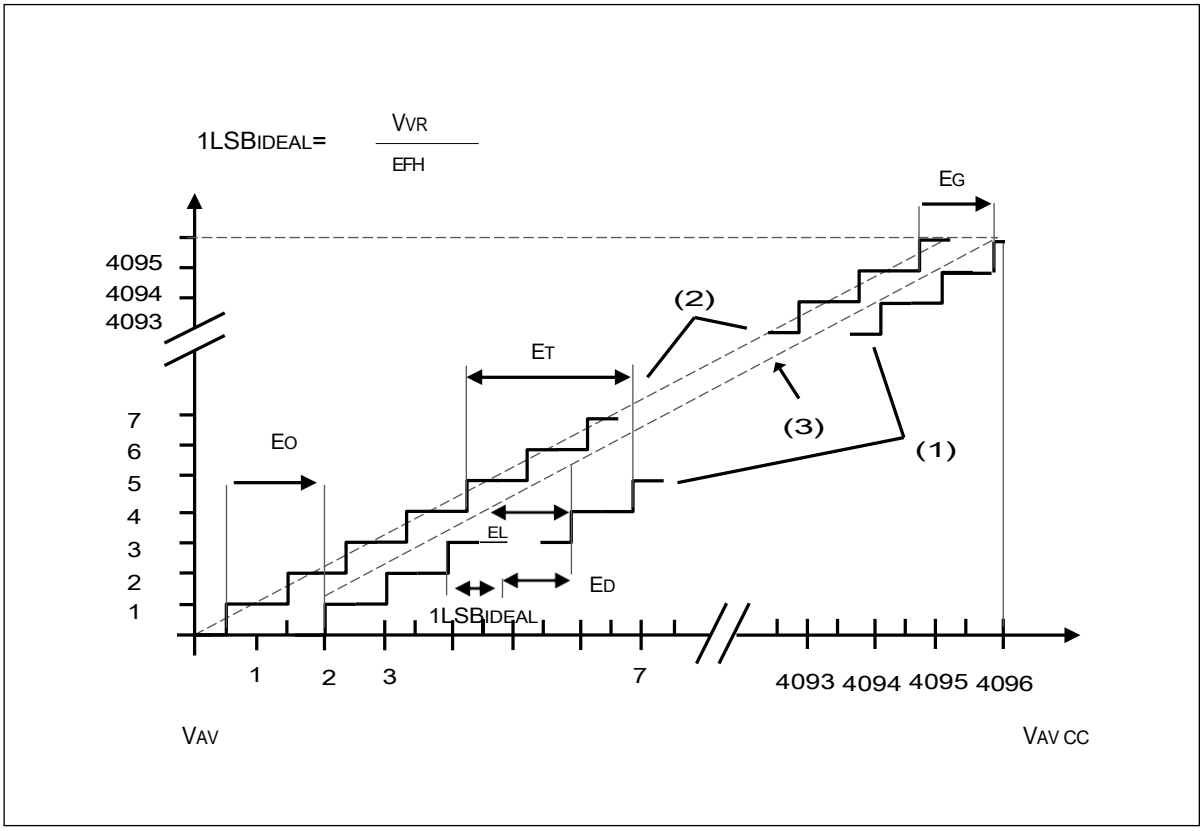


Figure 3-19 ADC Accuracy Characteristics

1. Please also see the table above.
2. Example of actual transmission curve.
3. Ideal transmission curve.
4. Endpoint correlation line.
5. E_T = Total unadjusted error: the maximum deviation between the actual and ideal transfer curves. E_O = Offset Error: The deviation between the first actual and first ideal conversion.

   E_G = Gain error: deviation between the last ideal conversion and the last actual conversion. E_D = Differential linearity error: the maximum deviation between the actual step and the ideal value.

   E_L = Integral linearity error: the maximum deviation between any actual conversion and the endpoint correlation line.

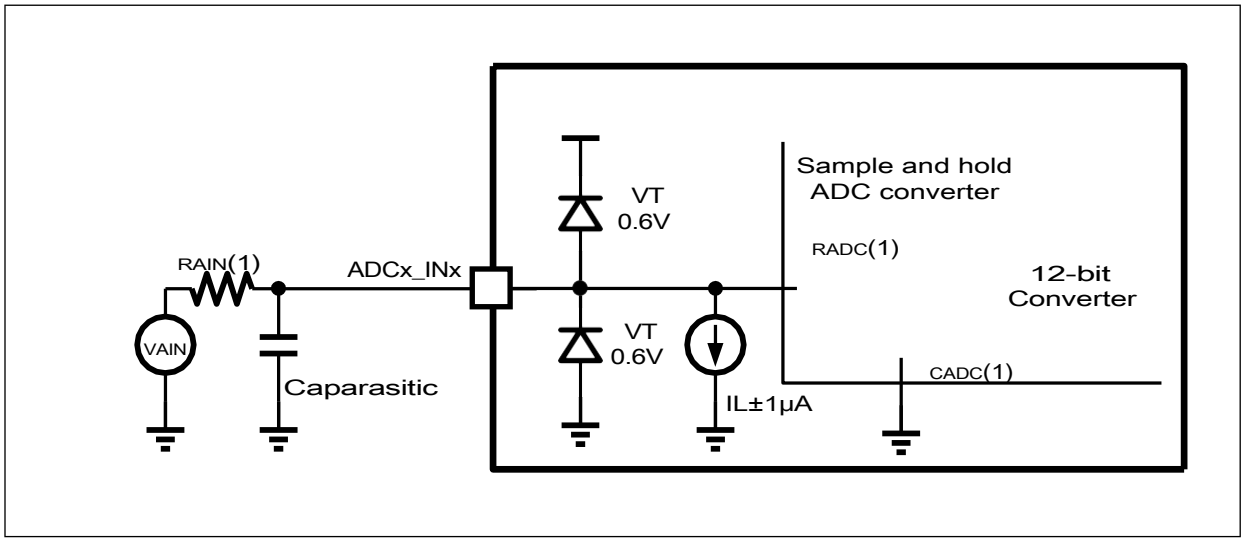


Figure 3-20 Typical Connection Using ADC

1. See Table 3-37 for information on R_{AIN}, R_{ADC}, and C_{ADC} values.
2. $C_{parasitic}$ indicates PCB capacitance (depending on soldering and PCB wiring quality) and pad capacitance (~5 pF). higher Cparasitic values result in lower conversion accuracy. To solve this problem, the f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the following diagram, depending on VREFH is connected to AVCC and the number of AVCC pins. The 0.1μF capacitors should be (high quality) ceramic capacitors. These capacitors should be as close to the chip as possible.

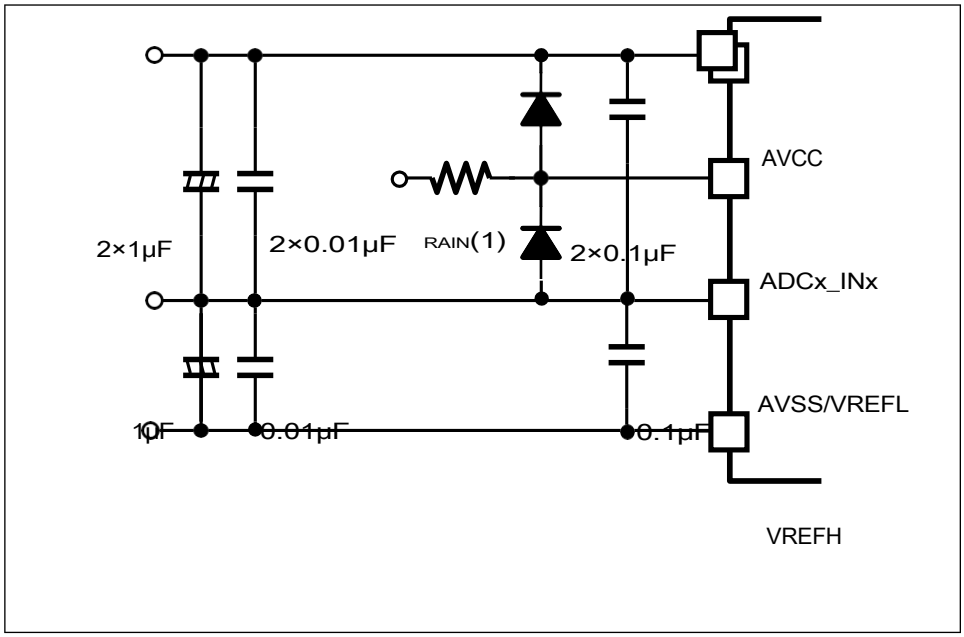


Figure 3-21 Example of decoupling power supply and reference power supply

3.3.19 DAC Characteristics

Table 3-50 DAC Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VAVCC	Analog supply voltage	–	1.8	3.3	3.6	V
DNL	Differential nonlinear error (deviation between two consecutive codes - 1LSB)	–	–	–	±2	LSB
Offset	Offset error (difference between the measured value at code (0x80) and the ideal value VAVCC/2)	–	–	–	±2	LSB
TSETTLING	Build-up time (full scale: applies to the 8-bit input between the lowest input code and the highest input code by the time DA0/DA1 reaches its final value of ±4LSB) (into the code conversion)	–	–	–	8	μs

3.3.20 Comparator Features

Table 3-51 Comparator Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VAVCC	Analog supply voltage	–	1.8	3.3	3.6	V
VI	Input Voltage Range	–	0	–	VAVCC	V
Tcmp	Compare times	Comparator resolution voltage = 100mV	–	50	100	ns
Tset	Input channel switching stability time	–	–	100	200	ns

3.3.21 Gain Adjustable Amplifier Features

Table 3-52 Gain Adjustable Amplifier Characteristics

Symbols	Parameters		Conditions	Minimum value	Typical values	Maximum value	Unit
V_{AVCC}	Analog supply voltage		–	1.8	3.3	3.6	V
V_{OS}(1)	Input derating voltage		–	-8	–	8	mV
V_I	Input Voltage Range		–	0.1*VAVCC/Gain	–	0.9*VAVCC/Gain	V
G_E	Gain error	Using external PGAVSS As PGA Negative phase input	Gain=2(1)	-1	–	1	%
			Gain=2.133	-1	–	1	%
			Gain=2.286	-1	–	1	%
			Gain=2.667	-1	–	1	%
			Gain=2.909	-1	–	1	%
			Gain=3.2	-1.5	–	1.5	%
			Gain=3.556	-1.5	–	1.5	%
			Gain=4.0	-1.5	–	1.5	%
			Gain=4.571	-2	–	2	%
			Gain=5.333	-2	–	2	%
			Gain=6.4	-3.0	–	3.0	%
			Gain=8	-3.0	–	3.0	%
			Gain=10.667	-4.0	–	4.0	%
			Gain=16	-4.0	–	4.0	%
			Gain=32(1)	-7.0	–	7.0	%
		Use internal The simulated ground AVSS as Negative for PGA	Gain=2(1)	-2	–	2	%
			Gain=2.133	-2	–	2	%
			Gain=2.286	-2	–	2	%
			Gain=2.667	-2	–	2	%
			Gain=2.909	-2	–	2	%
			Gain=3.2	-2.5	–	2.5	%
			Gain=3.556	-2.5	–	2.5	%
			Gain=4.0	-2.5	–	2.5	%
			Gain=4.571	-3.0	–	3.0	%

		Phase input	Gain=5.333	-3.0	–	3.0	%
			Gain=6.4	-4.0	–	4.0	%
			Gain=8	-4.0	–	4.0	%
			Gain=10.667	-5.0	–	5.0	%
			Gain=16	-5.0	–	5.0	%
			Gain=32(1)	-8.0	–	8.0	%

1. Mass production test guarantee.

3.3.22 Temperature Sensor

Table 3-53 Temperature Sensor Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
TL	Relative Accuracy	Each chip is individually calibrated according to the user manual	–	–	±5	℃

3.3.23 Memory Features

3.3.23.1 Flash Memory

The flash memory is erased when the device is delivered to the customer.

Table 3-54 Flash Memory Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
IVCC	Supply current	Read mode, VCC=1.8 V~3.6V	–	–	5	mA
		Programming mode, VCC=1.8 V~3.6 V	–	–	10	
		Block erase mode, VCC=1.8 V~3.6V	–	–	10	
		Full erase mode, VCC=1.8 V~3.6V	–	–	10	

Table 3-55 Flash Memory Programming Erase Time

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
T_{prog}(1)	Word programming time	Single Programming Mode	43+2* T_{hclk}(2)	48+4* T_{hclk}(2)	53+6* T_{hclk}(2)	μs
	Word programming time	Continuous programming mode	12+2* T_{hclk}(2)	14+4* T_{hclk}(2)	16+6* T_{hclk}(2)	μs
T_{erase}(1)	Block Erase Time	–	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms
T_{mas}(1)	Full Erase Time	–	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms

1. Mass production test guarantee.
2. T_{hclk} is 1 cycle of the CPU clock.

Table 3-56 Flash memory rewritable times and data retention period

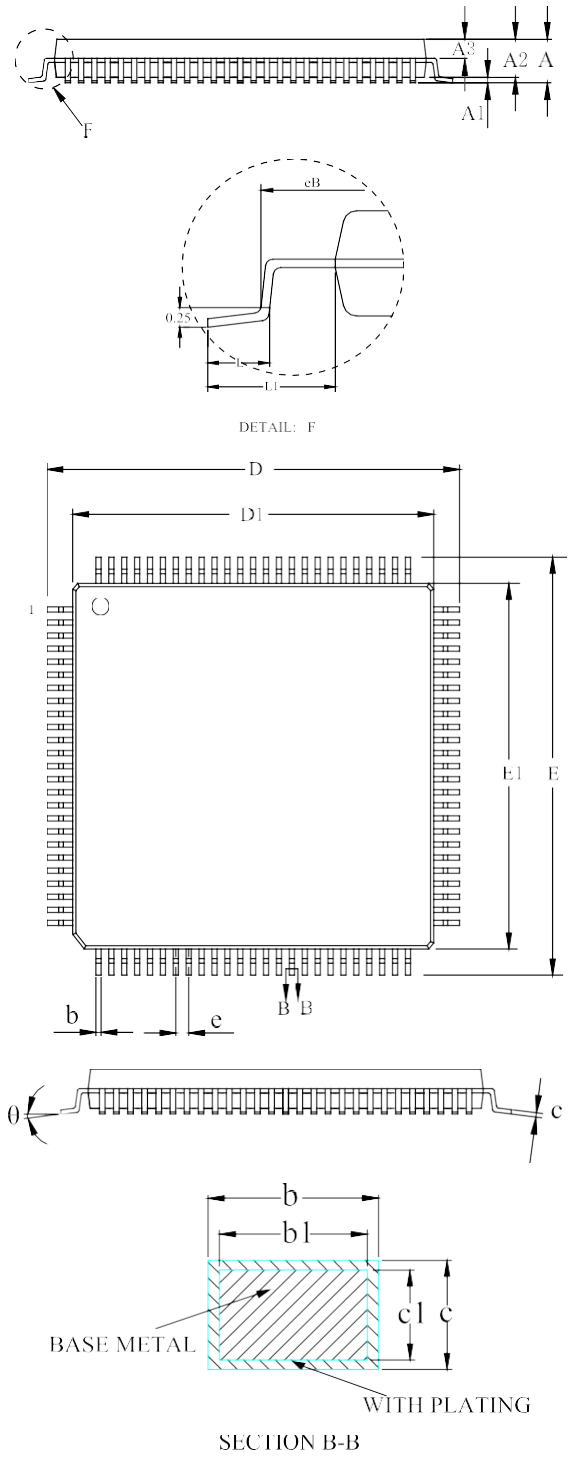
Symbols	Parameters	Conditions	Numerical value	Unit
			Minimum value	
Nend	Programming, block erase times	T_A = 85°C	10	kcycles

Nend	Number of full erasures	T_A = 85°C	10	kcycles
Tret	Data retention period	T_A = 85°C, after 10 kcycles	10	Years

4 Package Information

4.1 Package Size

LQFP100 package



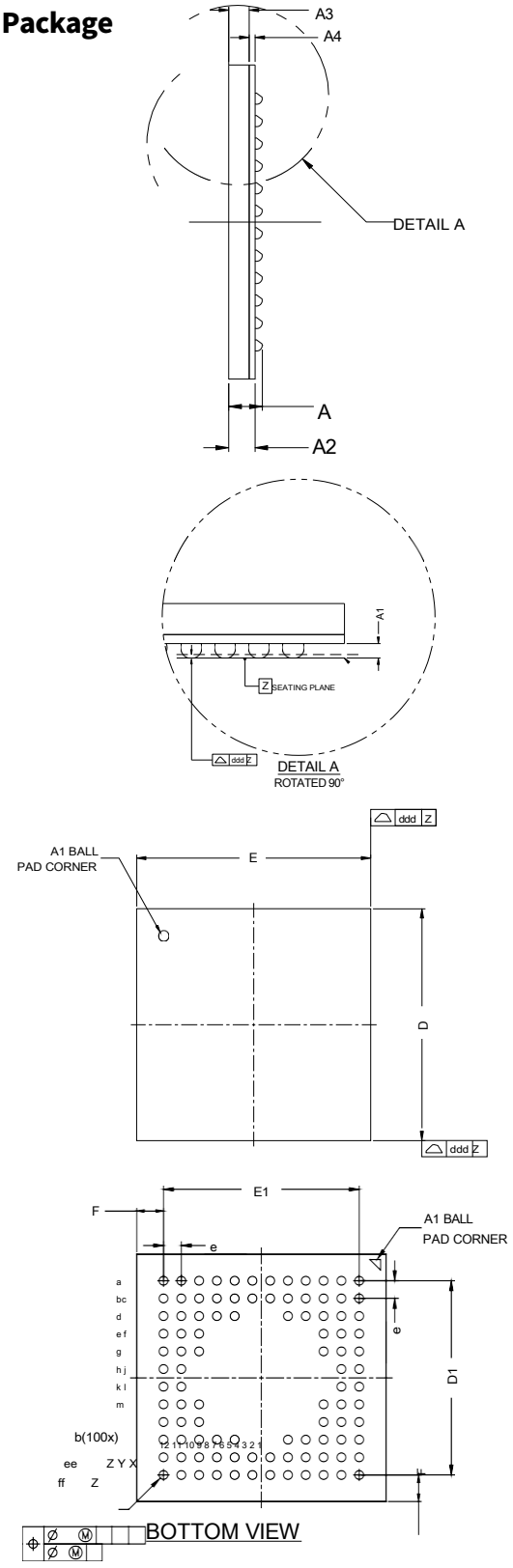
Symbol	14x14 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.27
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

NOTE:

- Dimensions "D1" and "E1" do not include mold flash.

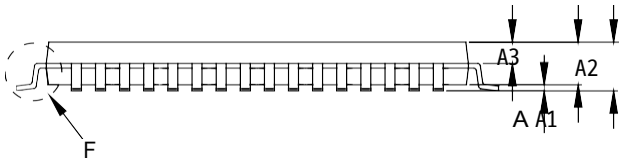
VFBGA100

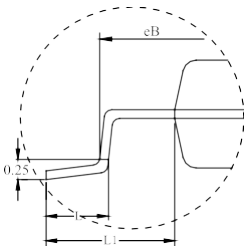
Package



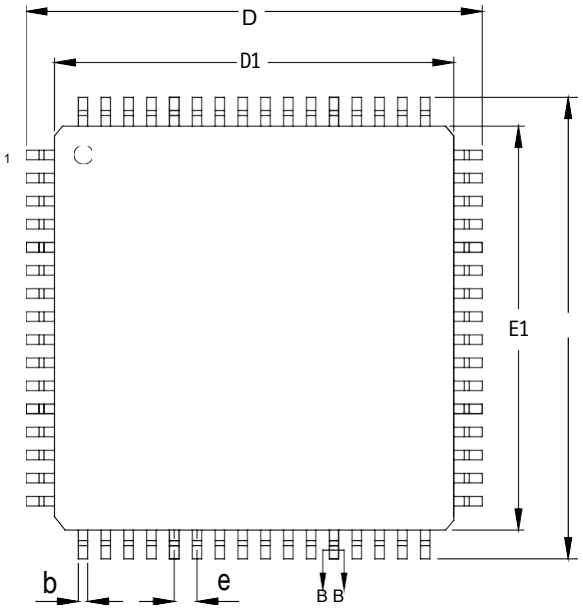
Symbol	7x7 Millimeter		
	Min	Nom	Max
A	0.67	0.74	0.81
A1	0.11	0.16	0.21
A2	0.54	0.58	0.62
A3		0.45REF	
A4		0.13REF	
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D1	--	5.5	--
E	6.90	7.00	7.10
E1	--	5.5	--
e	--	0.5	--
F		0.75REF	
ddd	--	0.10	--
eee	--	0.15	--
fff	--	0.05	--

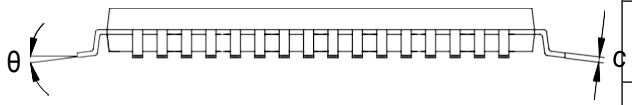
LQFP64

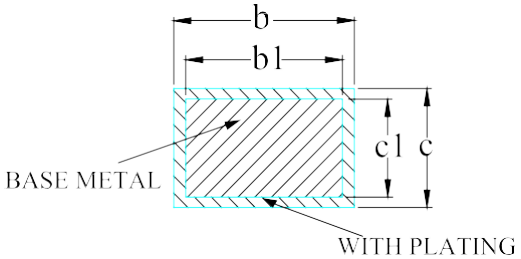




DETAIL: F







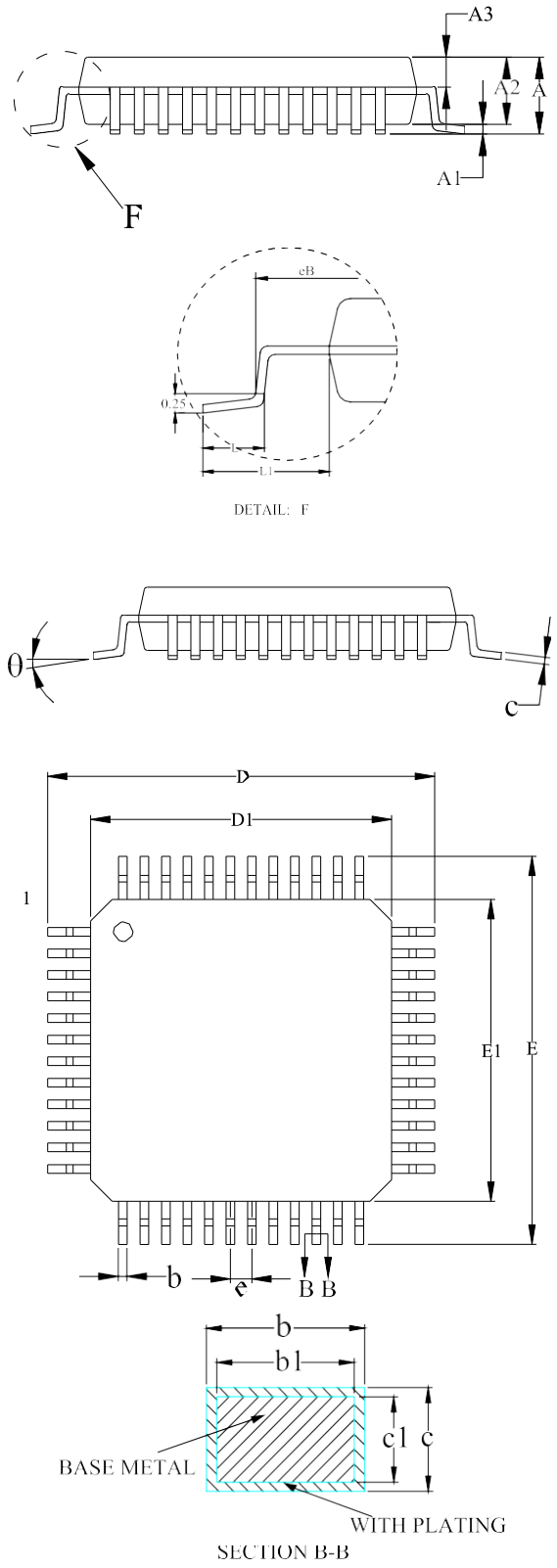
SECTION B-B

Symbol	10x10 Millimeter		
	Min	Nom	Max
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	---	0.27
b1	0.17	0.20	0.23
c	0.13	---	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	---	0.75
L1	1.00REF		
θ	0°	---	7°

NOTE.

- Dimensions "D1" and "E1" do not include mold flash.

LQFP48 package

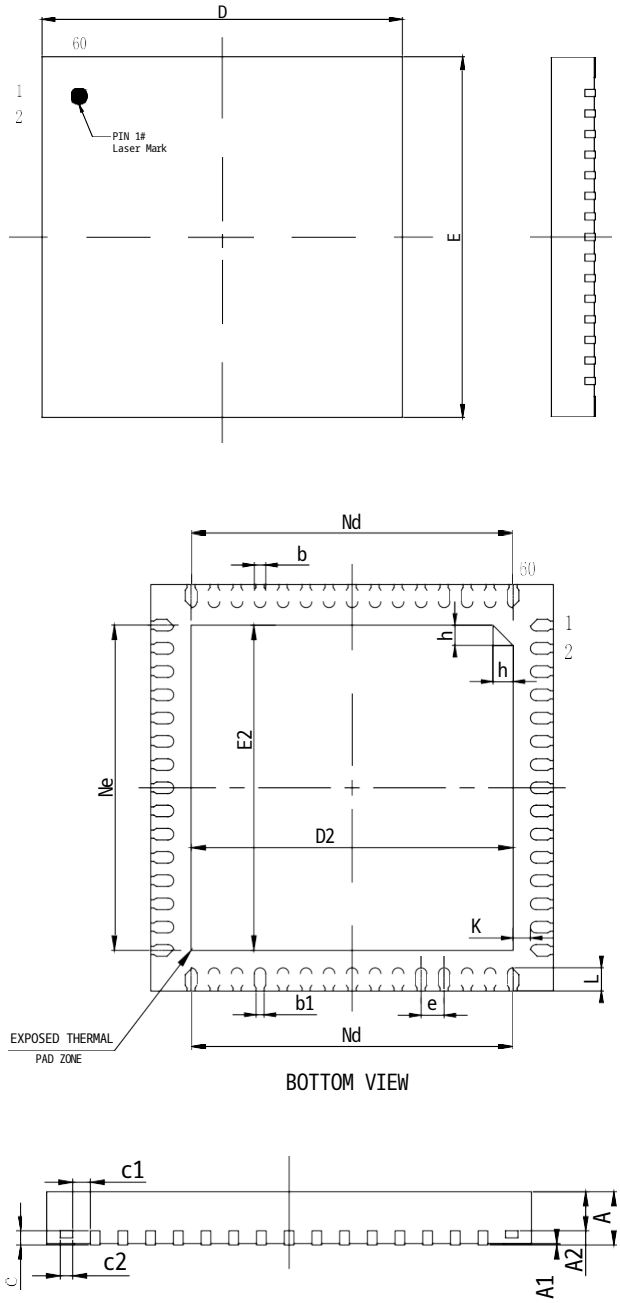


Symbol	7x7 Millimeter		
	Min	Nom	Max
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.27
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.40	--	0.65
L1	1.00REF		
θ	0	--	7°

NOTE.

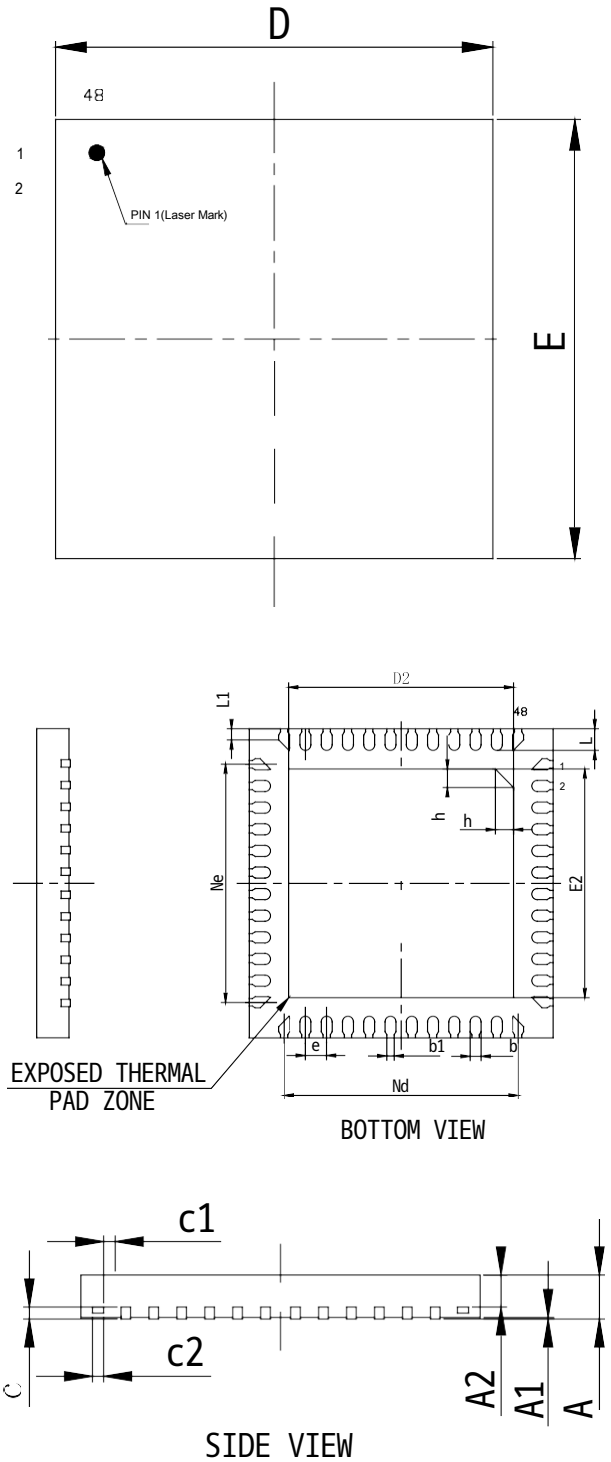
- Dimensions "D1" and "E1" do not include mold flash.

QFN60 Package



Symbol	7x7 Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.547REF	
b	0.15	0.20	0.25
b1		0.14REF	
c		0.20REF	
c1		0.255REF	
c2		0.18REF	
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
Nd		5.60BSC	
e		0.40BSC	
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
Ne		5.60BSC	
L	0.35	0.40	0.45
K	0.25	0.30	0.35
h	0.30	0.35	0.40

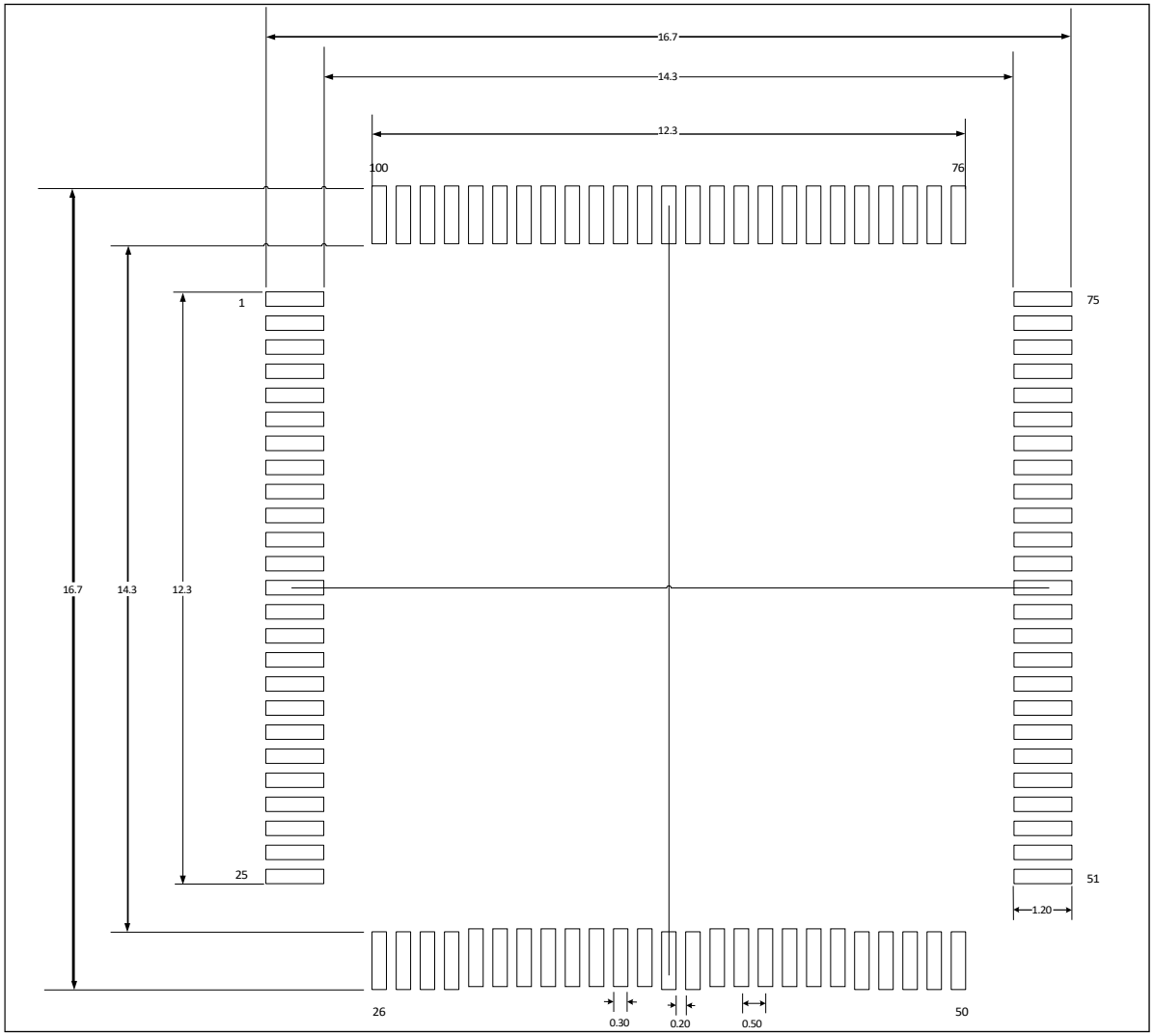
QFN48 Package



Symbol	5x5 Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2		0.40REF	
b	0.13	0.18	0.23
b1		0.12REF	
c	0.10	0.15	0.20
c1		0.145REF	
c2		0.140REF	
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e		0.35BSC	
Ne		3.85BSC	
Nd		3.85BSC	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F Carrier Size		154 x 154	

4.2 Schematic diagram of solder pads

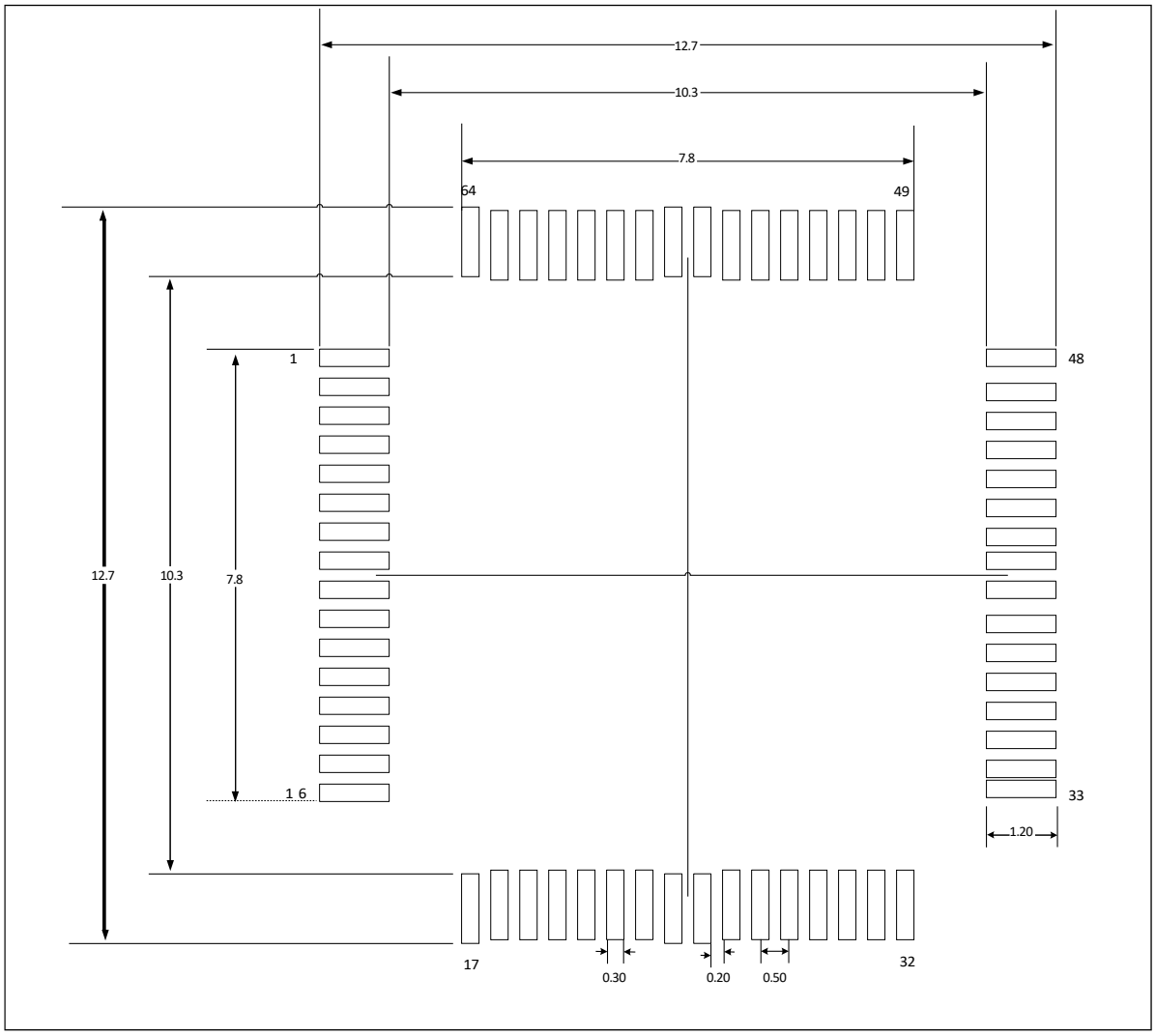
LQFP100 package (14mm x 14mm)



NOTE.

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

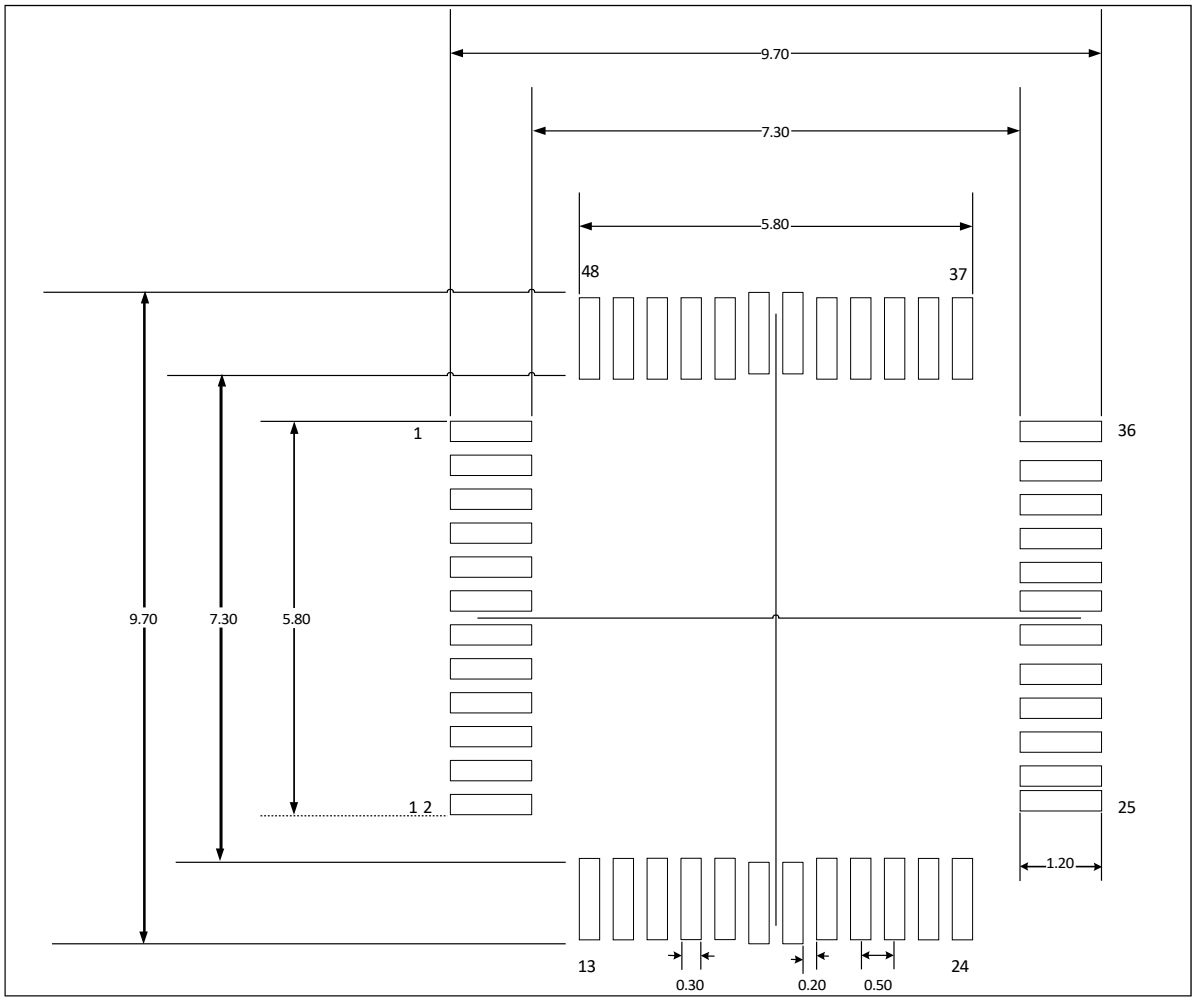
LQFP64 package (10mm x 10mm)



NOTE.

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

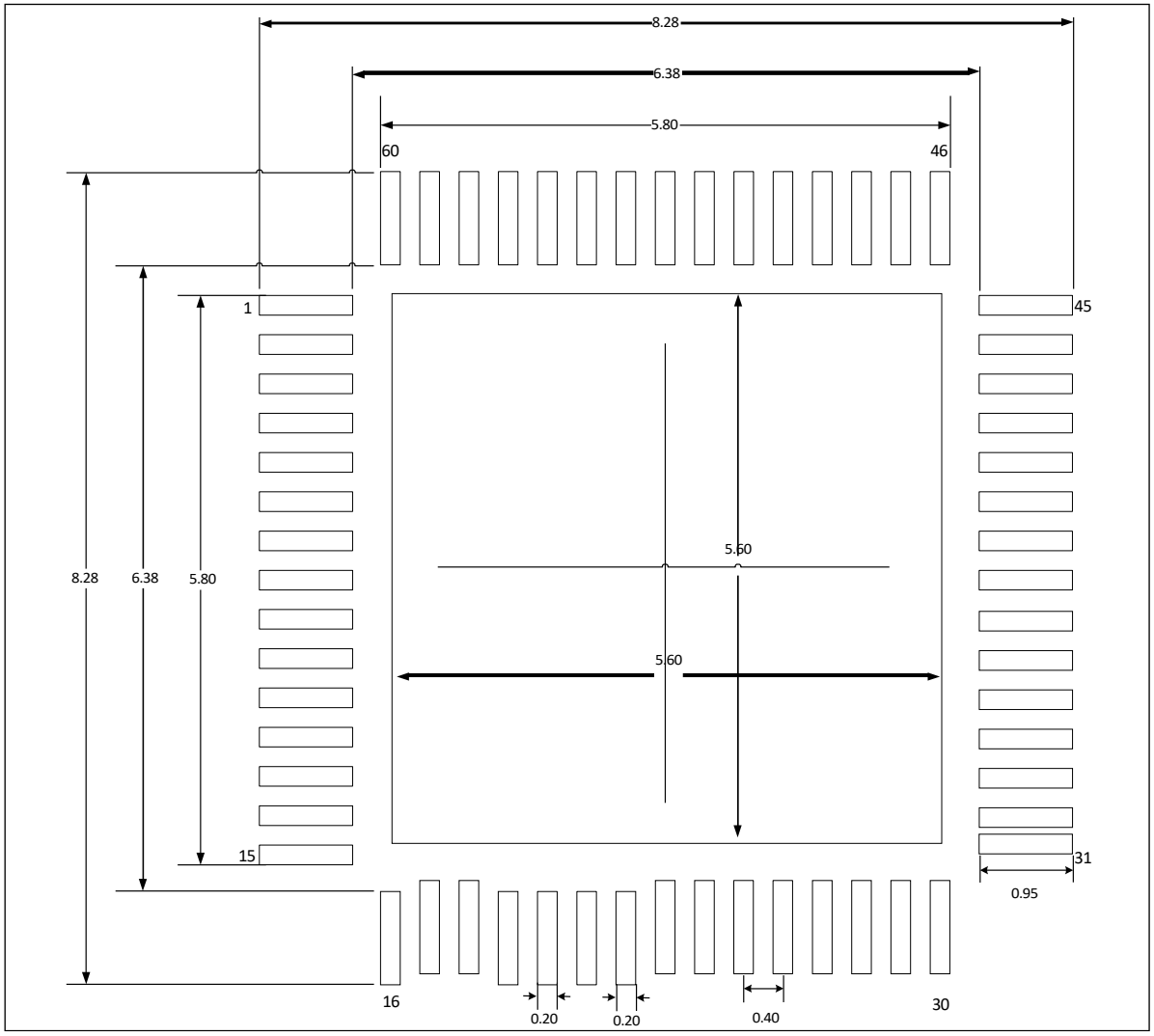
LQFP48 package (7mm x 7mm)



NOTE.

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

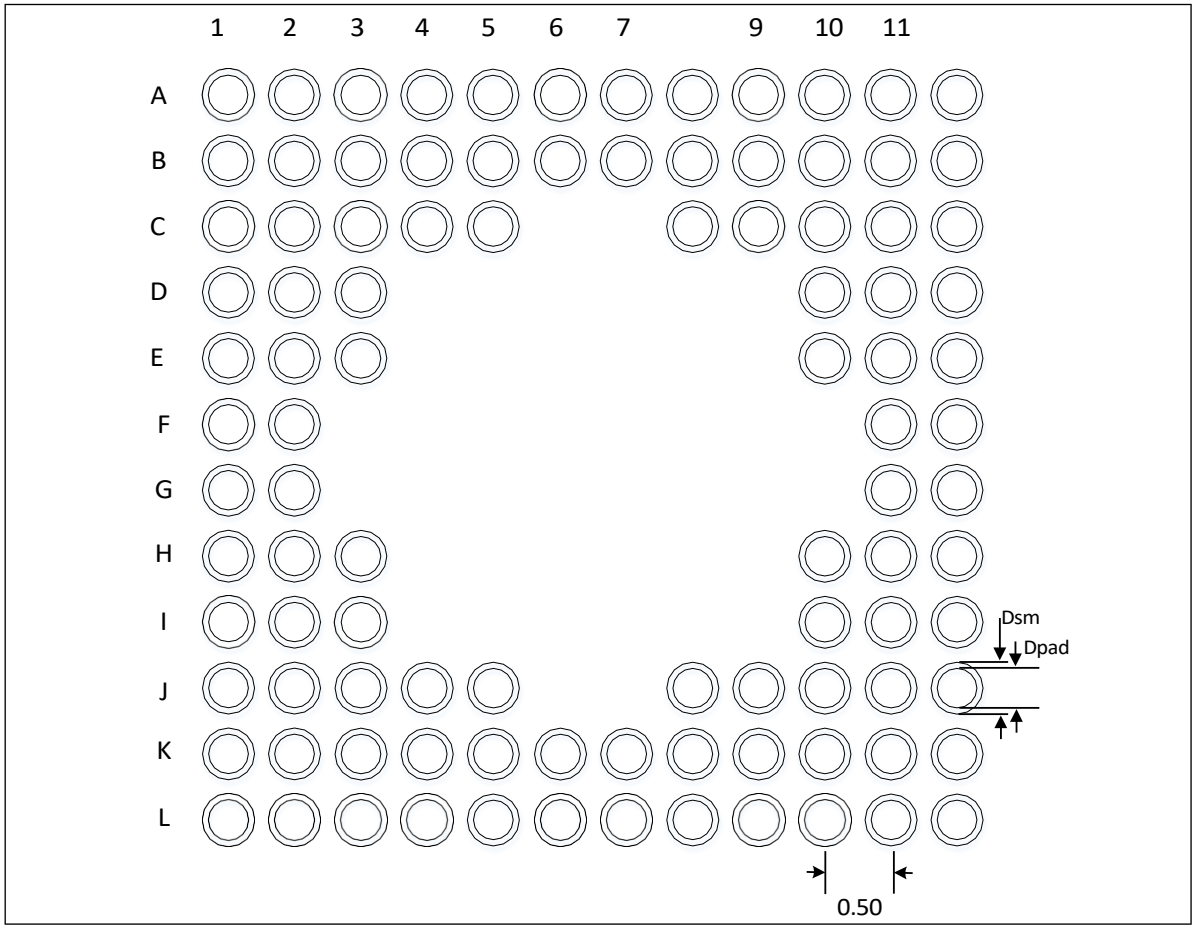
QFN60 package (7mm x 7mm)



NOTE.

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

VFBGA100 package (7mm x 7mm)



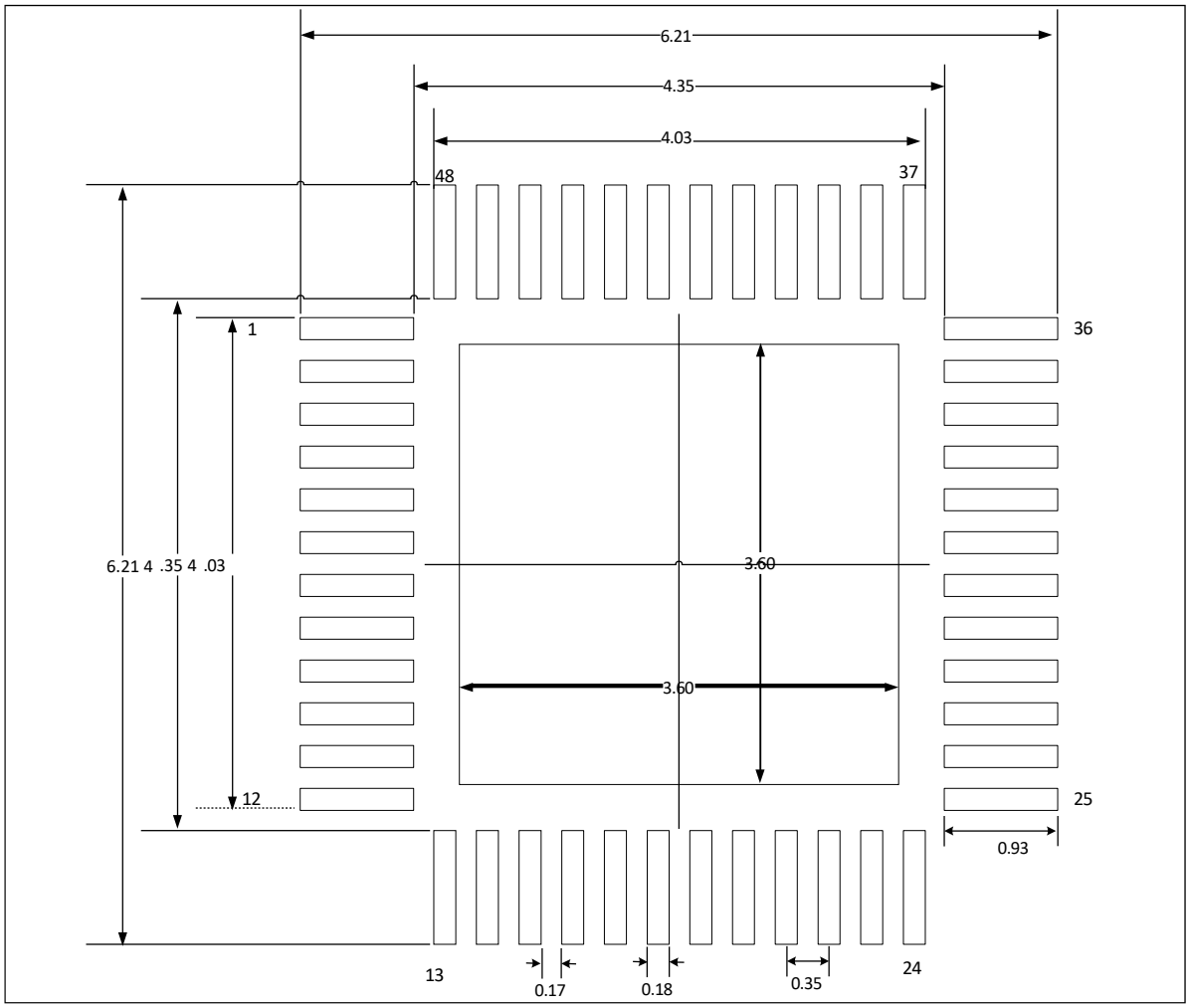
NOTE.

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

VBGA100 recommended PCB design rules(0.5mm pitch)

Dimension	Recommended values
Pitch	0.5mm
Dpad	0.240mm
Dsm	0.340mm typ.(depends) on the soldermask registration tolerance)
Stencil opening	0.240mm
Stencil thickness	Between 0.100mm and 0.125mm

QFN48 package (5mm x 5mm)



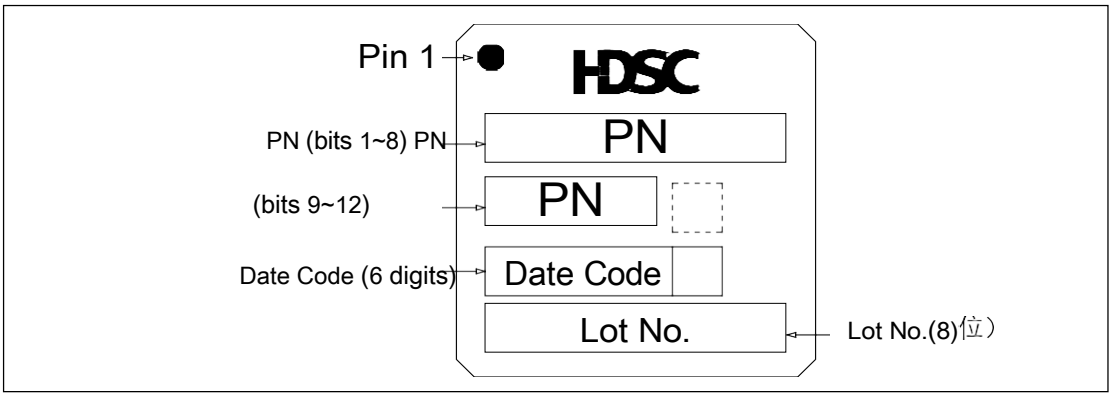
NOTE.

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

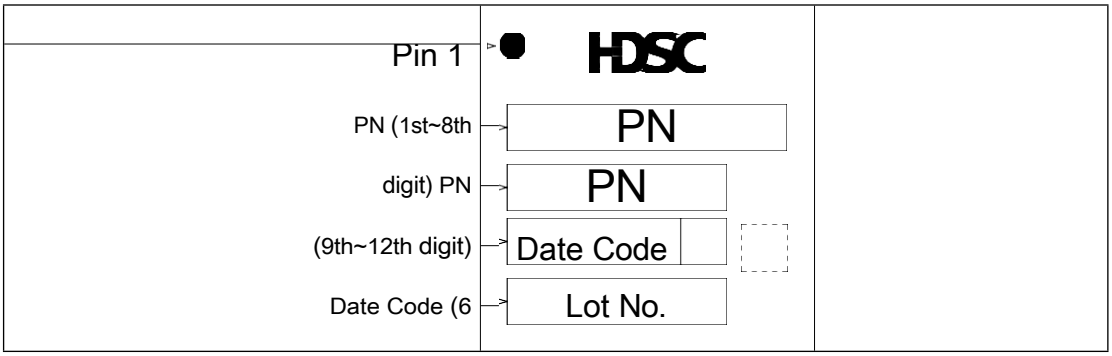
4.3 Silkscreen instructions

The location and information of Pin 1 on the front side of each package is given below.

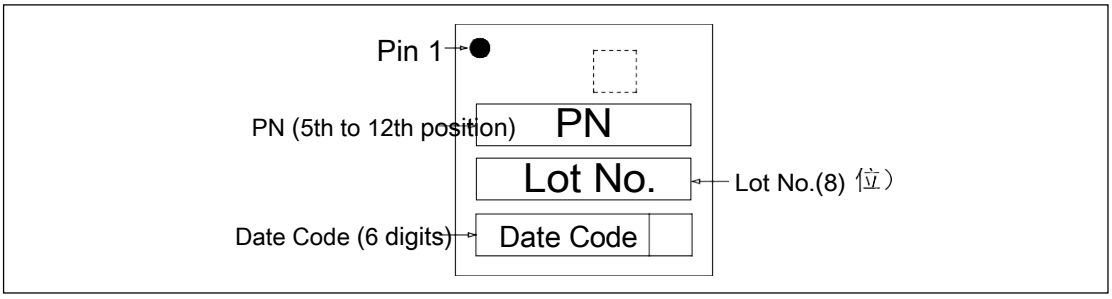
LQFP100 package (14mm x 14mm) / LQFP64 package (10mm x 10mm)
LQFP48 package (7mm x 7mm)



QFN60 package (7mm x 7 m m) / VFBGA100 package (7mm x 7mm)



QFN48 package (5mm x 5mm)



Caution:

- The blank boxes above indicate optional production-related markers that are not described in this section.

4.4 Package thermal resistance coefficient

The junction temperature T_j (°C) on the chip surface when the packaged chip is operated at the specified operating ambient temperature can be calculated according to the following equation:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} is the operating ambient temperature in °C at which the package chip operates;
- θ_{JA} is the thermal resistance coefficient of the package to the operating environment in °C/W;
- P_D is equal to the sum of the chip's internal power consumption and I/O power consumption in W. The chip's internal power consumption is the product's $I_{DD} \times V_{DD}$, and the I/O power consumption refers to the power consumption generated by the I/O pins when the chip is operating, which is usually very small and can be ignored.

The junction temperature T_j on the chip surface when the chip is operating at the specified operating ambient temperature must not exceed the maximum junction temperature T_J that the chip can tolerate.

Table 4-1 Thermal resistance coefficient of each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10%	℃/W
LQFP64 10mm x 10mm / 0.5mm pitch	65 +/- 10%	℃/W
LQFP48 7mm x 7mm / 0.5mm pitch	75 +/- 10%	℃/W
QFN60 7mm x 7mm / 0.4mm pitch	30 +/- 10%	℃/W
QFN48 5mm x 5mm / 0.35mm pitch	42 +/- 10%	℃/W

5 Ordering Information

Product Model	HC32F460JEUA-QFN48TR	HC32F460JETA-LQFP48	HC32F460KEUA-QFN60TR	HC32F460KETA-LQFP64	HC32F460PETB-LQFP100	hc32f460pehb-vfbga100	HC32F460JCTA-LQFP48	HC32F460KCTA-LQFP64	HC32F460PCTB-LQFP100
Main Frequency (MHz)	200	200	200	200	200	200	200	200	200
Kernel	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4
Flash (KB)	512	512	512	512	512	512	256	256	256
RAM (KB)	192	192	192	192	192	192	192	192	192
OTP (B)	960	960	960	960	960	960	960	960	960
Package (mm*mm)	QFN48 (5*5) e=0.35	LQFP48 (7*7) e=0.5	QFN60 (7*7) e=0.4	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5	VFBGA100 (7*7) e=0.5	LQFP48 (7*7) e=0.5	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5
General IO	38	38	50	52	83	83	38	52	83
Minimum operating voltage	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Maximum working voltage	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
16-bit timer	11	11	11	11	11	11	11	11	11
Motor control timer	3	3	3	3	3	3	3	3	3
12-bit ADC conversion unit	2	2	2	2	2	2	2	2	2
Number of 12-bit ADC channels	10	10	15	16	16	16	10	16	16
Comparator	3	3	3	3	3	3	3	3	3
Amplifier PGA	1	1	1	1	1	1	1	1	1
SPI	4	4	4	4	4	4	4	4	4
QUADSPI	1	1	1	1	1	1	1	1	1
I S²	4	4	4	4	4	4	4	4	4
I C²	3	3	3	3	3	3	3	3	3
U(S)ART	4	4	4	4	4	4	4	4	4
CAN	1	1	1	1	1	1	1	1	1
SDIO	2	2	2	2	2	2	2	2	2
Full-speed USB OTG	1	1	1	1	1	1	1	1	1
DMA	8	8	8	8	8	8	8	8	8
DCU	4	4	4	4	4	4	4	4	4
PVD	√	√	√	√	√	√	√	√	√
AES128	√	√	√	√	√	√	√	√	√
SHA256	√	√	√	√	√	√	√	√	√
TRNG	√	√	√	√	√	√	√	√	√
CRC	√	√	√	√	√	√	√	√	√
KEYSCAN	√	√	√	√	√	√	√	√	√
RTC	√	√	√	√	√	√	√	√	√
FLASH Physical Encryption	√	√	√	√	√	√	√	√	√
Shipping method	Tape and Reel	Tray loading	Tape and Reel	Tray loading	Tray loading	Tray loading	Tray loading	Tray loading	Tray loading

Before ordering, please contact the sales window for the latest mass production information.

Version revision record

Version number	Revision Date	Revised content
Rev1.0	2019/11/12	Initial Release
Rev1.1	2020/01/10	1) Add 256KB of product descriptions to the full text; 2) Addition of VFBGA package descriptions throughout the text; 3) Modification of the current max value for 105°C in power-down mode in the electrical characteristics; 4) Update the silkscreen instructions.
Rev1.2	2020/08/26	1) Add ultra-high speed operation mode description, update CoreMark/DMIPS, add ultra-high speed mode description. Updating functional block diagrams; 2) Pin configuration diagram to add 256KB models; 3) Adding pad schematics and package thermal resistance factors; 4) Addition of BOR/PVD characteristics in ultra-high speed mode, current characteristics; 5) Updating the JTAG/SWJ debug port pins;
Rev1.3	2021/12/10	1) Modification of the declaration, addition of A2/c1/c2 size of QFN48/60 to the package size, modification of the data retention period in the flash memory; 2) External master clock crystal: (4-24MHz) to (4-25MHz); 3) Functional block diagram modification: USB_DMA -> USBFS_DMA; I2S_1 -> I2S_2; addition of AOS; 4) 1.4.6 Addresses 0x00000400H~0x0000041FH -> 0x0000_0400~0x0000_041F 0x00000408~0x0000041F -> 0x0000_0408~0x0000_041F 5) Adding the description of "Automatic Operating System (AOS)" profile and updating the description of "Keyboard Scan (KEYSCAN)"; 6) Name correction and description optimization; 7) The recommended configuration of the analog power supply pin bypass capacitor is modified in the power supply scheme diagram by removing the 10nF capacitor and modifying the 10uF capacitor to 1uF; 8) Additional parameters in the reset and power control module characteristics table: TIPVD1/TIPVD2/TINRST/TRSTBOR TRSTTAO->TRSTPOR; 9) 3.3.12 Adding a description of the CAN2.0B interface characteristics; 10) The Max value of f_{PLL_IN} in PLL characteristics is changed from 24MHz to 25MHz, and the Jitter characteristic is added; 11) 3.3.16.1 The maximum value of f_{XTAL_EXT} is changed to 25 MHz; 12) 3.3.16.2 Addition of an external high-speed oscillator XTAL accuracy indicator

		and modification of C_{L1} and C_{L2} related descriptions; 13) 3.3.16.3 Add external low-speed oscillator XTAL32 accuracy indicator and modify C_{L1} and C_{L2} related descriptions.
Rev1.4	2022/03/09	Company logo updated.
Rev1.41	2022/03/29	1) 3.3.13 USB interface characteristics R_{PD} Delete MAX, MIN values and add Typ value 15kΩ; 3.3.16 $t_{SU(XTAL)}$ start time delete maximum value, add typical value 2) 4.1 LQFP100/LQFP64/LQFP48 b MAX value modified to 0.27
Rev1.42	2022/09/14	1) 2.1 PH0/XTAL_IN" is changed to "PH0/XTAL_EXT/XTAL_OUT" and "PH1/XTAL_OUT" in each package pin layout diagram. " Modify change to "PH1/XTAL_IN", QFN60 pin configuration diagram style modification, new QFN48 pin configuration diagram;

Version number	Revision Date	Revised content
		2.2 "PH0/XTAL_IN" is modified to "PH0/XTAL_EXT/XTAL_OUT" and "PH1/XTAL_OUT" is modified to "PH1/XTAL_IN"; 2.3 "XTAL_OUT" is modified to "XTAL_EXT/XTAL_OUT" with the addition of the description "XTAL_EXT external clock input"; 2) 3 .3.16.1 "XTAL_IN" is modified to "XTAL_EXT"; 3.3.16.2 Switching the names of the "XTAL_IN" and "XTAL_OUT" pins in Figure 3-17; 3.3.18 The 10uF capacitance value in Figure 3-21 is modified to 1uF.