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XIAOHUA SEMICONDUCTOR

HC32F460 Series

32-bit ARM® Cortex®-M4 microcontroller

data sheet

Rev1.5 September

2023

Product Characteristics

ARM Cortex-M4 32bit MCU+FPU, 250DMIPS, up to 512KB Flash, 192KB SRAM, USB FS (Device/Host), 14 Timers, 2 ADCs, 1 PGA, 3 CMPs, 20 Communication Interfaces

- **ARMv7-M architecture 32bit Cortex-M4 CPU with integrated FPU, MPU, DSP supporting SIMD instruction, and CoreSight standard debugging unit. Maximum operating frequency 200MHz, Flash acceleration unit for 0-wait program execution, 250DMIPS or 680Coremarks computing performance.**
- **internal memory**
  - Maximum 512KByte Flash memory, support security protection and data encryption*1
  - Up to 192KByte SRAM, including 32KByte 200MHz single-cycle access high-speed RAM, 4KByte Retention RAM
- **Power, Clock, Reset Management**

  - System power supply (Vcc): 1.8-3.6V
  - 6 independent clock sources: external master clock crystal (4-25MHz), external slave crystal (32.768kHz), internal high-speed RC (16/20MHz), internal medium-speed RC (8MHz), internal low-speed RC (32kHz), internal WDT-specific RC (10kHz)
  - 14 reset sources including Power-On Reset (POR), Low Voltage Detect Reset (LVDR), Port Reset (PDR), each with individual flag bits
- **Low power operation**
  - Peripheral functions can be turned off or on independently
  - Three low power modes: Sleep, Stop, and Power down modes.
  - Run mode and Sleep mode support switching between ultra-high speed mode, high speed mode, and ultra-low speed mode.
  - Standby power consumption: Stop mode typ.90uA@25°C, Power down mode down to 1.8uA@25°C
  - Power down mode, supports 16 ports wake-up, supports ultra-low power RTC operation, 4KByte SRAM to hold data
  - Fast wake-up from standby, up to 2us in Stop mode and 20us in Power down mode.
- **Peripheral Runtime Support System significantly reduces CPU processing loads**
  - 8-channel dual host DMAC
  - DMAC for USBFS
  - Data Computing Unit (DCU)
  - Support for mutual triggering of peripheral events (AOS)
- **High Performance Simulation**
  - 2 independent 12bit 2.5MSPS ADCs
  - 1 Programmable Gain Amplifier (PGA)
  - 3 independent voltage comparators (CMPs) supporting 2 internal references
  - 1 on-chip temperature sensor (OTS)

- **Timer**
  - 3 multifunction 16bit PWM timers (Timer6)
  - 3 16bit motor PWM timers (Timer4)
  - 6 16bit Universal Timers (TimerA)
  - 2 16bit base timers (Timer0)
- **Maximum 83 GPIOs**
  - CPU single-cycle access, 100MHz maximum output
  - Maximum 81 5V-tolerant IOs
- **Maximum 20 communication interfaces**
  - 3 I2C, SMBus protocol support
  - 4 USARTs supporting ISO7816-3 protocols
  - 4 SPI
  - 4 I2S, built-in audio PLL for audio grade sampling accuracy
  - 2 SDIOs supporting SD/MMC/eMMC formats
  - 1 QSPI supporting 200Mbps high-speed access (XIP)
  - 1 CAN, supports ISO11898-1 standard protocols
  - 1 USB 2.0 FS with built-in PHY, Device/Host support
- **Data encryption function**
  - AES/HASH/TRNG
- **Encapsulated form:**

LQFP100 (14×14mm)	VFBGA100 (7×7mm)
LQFP64 (10×10mm)	QFN60 (7×7mm)
QFN48 (5×5mm)	LQFP48 (7×7mm)

*1: For specific specifications on Flash security protection and data encryption, please contact the sales window.

Supported Models:

hc32f460petb-lqfp100	hc32f460pehb-vfbga100
hc32f460keta-lqfp64	hc32f460keua-qfn60tr
HC32F460JETA-LQFP48	hc32f460jeua-qfn48tr
HC32F460PCTB-LQFP100	HC32F460KCTA-LQFP64
HC32F460JCTA-LQFP48	

declaration Ming Dynasty (1368-1644)

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table of contents table of contents

table index

map index

1 Introduction (Overview)

The HC32F460 series are high-performance MCUs based on the ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 200 MHz. The Cortex-M4 core integrates a Floating-Point Unit (FPU) and a DSP, realizing single-precision floating-point arithmetic operations, supporting all ARM single-precision data-processing instructions and data types, and supporting the complete DSP instruction set. It supports all ARM single-precision data processing instructions and data types, and the full DSP instruction set. The core integrates an MPU unit and a DMAC dedicated MPU unit to ensure the safety of system operation.

The HC32F460 series integrates high-speed on-chip memories, including up to 512KB of Flash and up to 192KB of SRAM, and a Flash access acceleration unit, which enables the CPU to execute single-cycle programs on Flash. The polled bus matrix supports simultaneous access to memory and peripherals by multiple bus hosts for improved performance. The bus hosts include CPU, DMA, and USB dedicated DMA. In addition to the bus matrix, it supports data transfer between peripherals, basic arithmetic operations, and event triggering, which can significantly reduce the transaction load of the CPU.

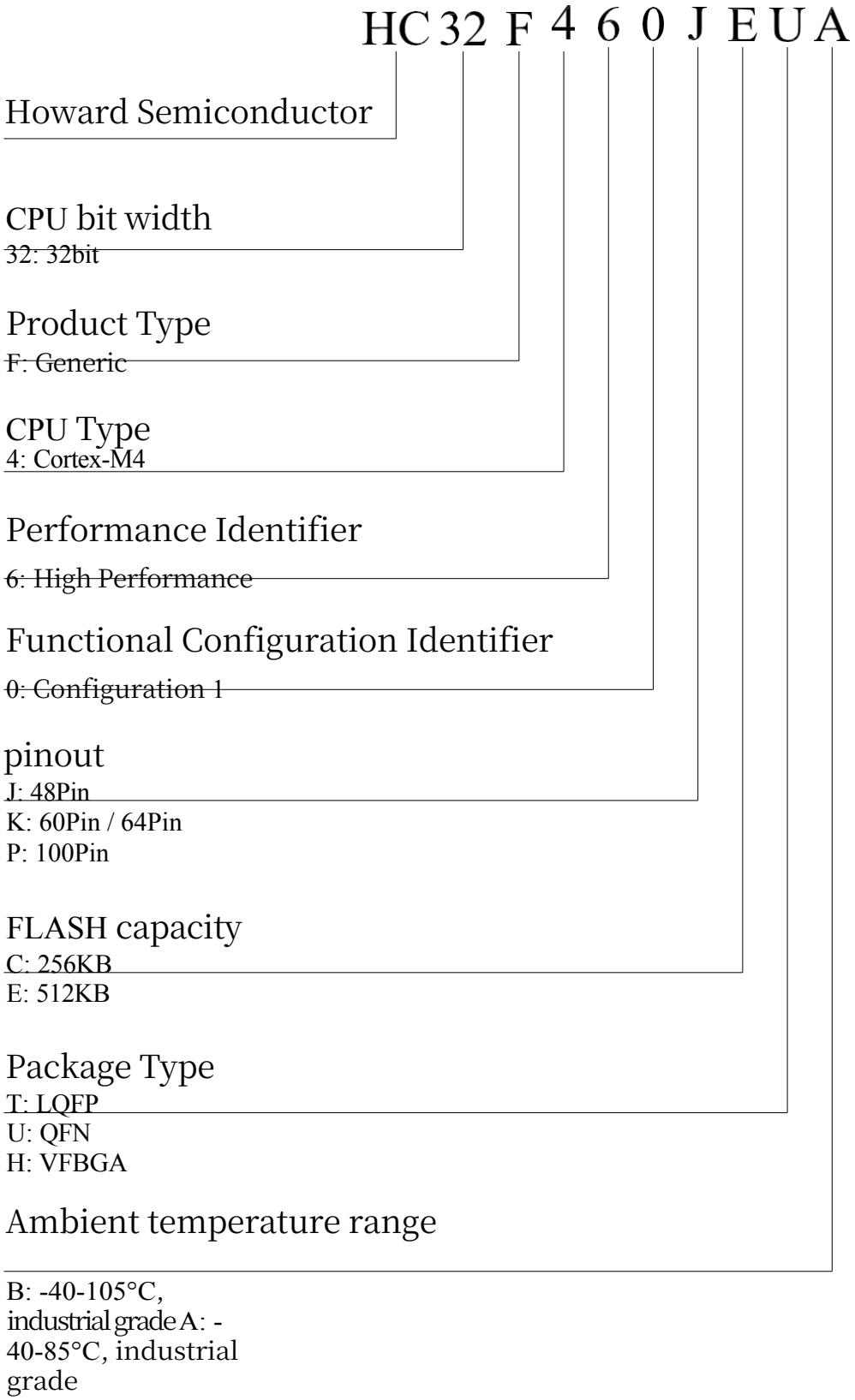
The HC32F460 series integrates a rich set of peripheral functions. These include two independent 12bit 2.5MSPS ADCs, one gain-adjustable PGA, three voltage comparators (CMPs) three multifunctional 16bit PWM timers (Timer6) supporting six complementary PWM outputs, three motor PWM timers (Timer4) supporting 18 complementary PWM outputs, and six 16bit general-purpose Timer
(TimerA) supports 3 3-phase quadrature encoding inputs and 48 Duty independently programmable PWM outputs, 11 serial communication interfaces
(I2C/UART/SPI)1 QSPI interface, 1 CAN, 4 I2S with audio PLL support, 2 SDIO, 1 USB FS Controller with on-chip FS PHY support Device/Host.

The HC32F460 series supports a wide voltage range (1.8-3.6V) a wide temperature range (-40-105°C), and various low-power modes. Ultra-high speed mode (≤200MHz) high speed mode (≤168MHz) and ultra-low speed mode can be switched in Run mode and Sleep mode.
(≤8MHz) Supports fast wake-up in low-power mode, as fast as 2μs in STOP mode and 20μs in Power Down mode.

typical application

The HC32F460 series is available in 48pin, 64pin, and 100pin LQFP packages, 48pin and 60pin QFN packages, and 100pin VFBGA package, which is suitable for high-performance motor inverter control, smart hardware, and IoT connectivity modules.

1.1 Model naming rules



1.2 Model Function Comparison Table

Table 1-1 Model Function Comparison

functionality		Product Model								
		HC32F460 PEHB	HC32F460 PETB	HC32F460 PCTB	HC32F460 KETA	HC32F460 KCTA	HC32F460 JETA	HC32F460 JCTA	HC32F460 JEUA	HC32F460 KEUA
Flash Memory (KB)		512	512	256	512	256	512	256	512	512
pinout		100	100	100	64	64	48	48	48	60
GPIO count		83	83	83	52	52	38	38	38	50
5V Tolerant GPIO count		81	81	81	50	50	36	36	36	48
seal inside		VFBGA	LQFP						QFN	
temperature range		-40-105°C			-40-85°C					
Power supply voltage range		1.8~3.6 V								
OTP (Byte)		960								
SRAM (KB)		192								
DMA		2unit * 4ch								
external port interrupt		EIRQ * 16vec + NMI * 1ch								
Communcation	UART	4ch (2)								
	SPI	4ch (3)								

Interfaces (Minimum number of IOs required per ch in parentheses)	I2C	3ch (2)
	I2S	4ch (3)
	CAN	1ch (2)

functionality		Product Model								
		HC32F460 PEHB	HC32F460 PETB	HC32F460 PCTB	HC32F460 KETA	HC32F460 KCTA	HC32F460 JETA	HC32F460 JCTA	HC32F460 JEUA	HC32F460 KEUA
	QSPI	1ch (6)								
	SDIO	2ch (3)								
	USB-FS	1ch (2)								
Timers	Timer0	2unit								
	TimerA	6unit								
	Timer4	3unit								
	Timer6	3unit								
	WDT	1ch								
	SWDT	1ch								
	RTC	1ch								
Analog	12bit ADC	2unit, 16ch					2unit, 10ch			2unit.
	PGA	1ch								
	CMP	3ch								
	OTS	✓								
AES128		✓								
HASH (SHA256)		✓								
TRNG		✓								
Frequency Monitoring Module (FCM)		✓								

Programmable voltage detection function (PVD)	✓								
functionality	**Product Model**								
	HC32F460 PEHB	**HC32F460 PETB**	**HC32F460 PCTB**	**HC32F460 KETA**	**HC32F460 KCTA**	**HC32F460 JETA**	**HC32F460 JCTA**	**HC32F460 JEUA**	**HC32F460 KEUA**
debugging interface	SWD								
	JTAG								

1.3 functional block diagram

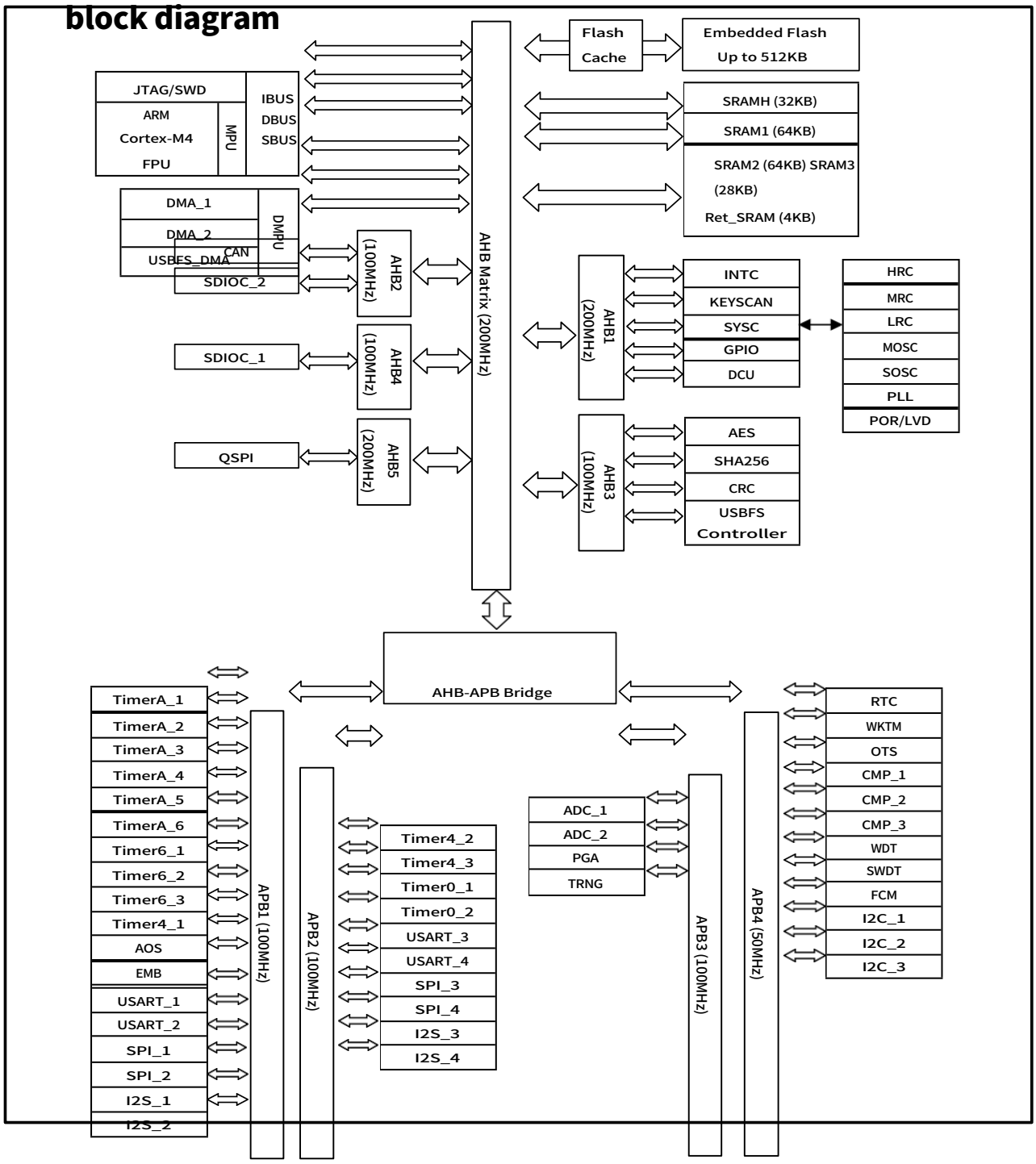


Figure 1-1 Function Block Diagram

1.4 Function Introduction

1.4.1 CPU

The HC32F460 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32-bit Thin Client CPU, which realizes low pin count and low power consumption, while providing excellent computing performance and fast interrupt response. The integrated on-chip memory capacity fully utilizes the excellent instruction efficiency of the ARM® Cortex®-M4 with FPU, and the CPU supports DSP instructions for efficient signal processing operations and complex algorithms. The Floating Point Unit (FPU) avoids instruction saturation and accelerates software development.

1.4.2 Bus Architecture (BUS)

The master system consists of a 32-bit multilayer AHB bus matrix that

interconnects the following host and slave buses. Host Bus

- Cortex-M4F Core CPU-I Bus, CPU-D Bus, CPU-S Bus
- System DMA_1 Bus, System DMA_2 Bus
- USBFS_DMA Bus

Slave Bus

- Flash ICODE Bus
- Flash DCODE Bus
- Flash MCODE bus (bus for hosts other than the CPU to access Flash)
- SRAMH Bus (SRAMH 32kB)
- SRAMA bus (SRAM1 64KB)
- SRAMB Bus (SRAM2 64KB, SRAM3 28KB, Ret_SRAM 4KB)
- APB1 Peripheral Bus (AOS/EMB/Timers/SPI/USART/I2S)
- APB2 Peripheral Bus (Timers/SPI/USART/I2S)
- APB3 Peripheral Bus (ADC/PGA/TRNG)
- APB4 Peripheral Bus (FCM/WDT/CMP/OTS/RTC/WKTM/I2C)
- AHB1 Peripheral bus (KEYSCAN/INTC/DCU/GPIO/SYSC)
- AHB2 Peripheral Bus (CAN/SDIOC)
- AHB3 Peripheral Bus (AES/HASH/CRC/USB FS)
- AHB4 Peripheral Bus (SDIOC)
- AHB5 Peripheral Bus (QSPI)

With the help of the bus matrix, efficient concurrent access from the master bus to the slave bus can be realized.

1.4.3 Reset control (RMU)

The chip is configured with 14 reset methods.

- Power-On Reset (POR)
- NRST Pin Reset (NRST)
- Undervoltage Reset (BOR)
- Programmable Voltage Detection 1 Reset (PVD1R)
- Programmable Voltage Detection 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Specialized Watchdog Reset (SWDTR)
- Power-down wake-up reset (PDRST)
- Software Reset (SRST)
- MPU Error Reset (MPUR)
- RAM Parity Reset (RAMPR)
- RAMECC Reset (RAMECCR)
- Clock Exception Reset (CKFER)
- External high-speed oscillator abnormal stop reset (XTALER)

1.4.4 Clock Control (CMU)

The Clock Control Unit provides clocking functions for a range of frequencies, including: an external high-speed oscillator, an external low-speed oscillator, two PLL clocks, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, an internal low-speed oscillator dedicated to the SWDT, clock prescaler, clock multiplexing, and clock gating circuitry.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the clock of the measurement object using the measurement reference clock. An interrupt or reset occurs when the set range is exceeded.

The AHB, APB and Cortex-M4 clocks are derived from the system clock, which can be sourced from a choice of six clock sources:

1) External High Speed Oscillator (XTAL)
2) External low-speed oscillator (XTAL32)
3) MPLL Clock (MPLL)
4) Internal High Speed Oscillator (HRC)
5) Internal medium-rate oscillator (MRC)
6) Internal low rate oscillator (LRC)

The system clock can run at a maximum clock frequency of 200MHz. the SWDT has a separate

clock source: the SWDT dedicated internal low-speed oscillator (SWDTLRC) the real-time clock (RTC) uses an external low-speed oscillator or an internal low-speed oscillator as clock source. The real-time clock (RTC) uses either an external low-speed oscillator or an internal low-speed oscillator as the clock source.The 48MHz clock of USB-FS and the I2S communication clock can be selected from the system clock, MPLL, and UPLL as the clock source.

For each clock source, it can be turned on and off individually. It is recommended to turn off unused clock sources to reduce power consumption.

1.4.5 Power Control (PWC)

The power controller is used to control the power supply, switching, and detection of multiple power domains of the chip in multiple operation modes and low power modes. The power controller consists of power consumption control logic (PWCL), and a supply voltage detection unit (PVD).

The chip operates from 1.8 V to 3.6 V. The voltage regulator (LDO) supplies power to the VDD domain and VDDR domain, and the VDDR voltage regulator (RLDO) supplies power to the VDDR domain in power-down mode. The chip provides three modes of operation: ultra-high speed, high speed, and ultra-low speed, and three low-power modes: sleep, stop, and power-down through the power consumption control logic (PWCL).

The power supply voltage detection unit (PVD) provides functions such as power-on reset (POR), power-down reset (PDR), undervoltage reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2), etc., of which, POR, PDR, BOR control chip reset by detecting the VCC voltage; PVD1 detects the VCC voltage to generate a reset or interrupt by setting according to the register; PVD2 detects VCC voltage or external input detection voltage to generate a reset or interrupt according to the register; PVD2 detects VCC voltage or external input detection voltage to generate a reset or interrupt by selecting according to the register. PVD1 detects VCC voltage and generates reset or interrupt according to the register setting, while PVD2 detects VCC voltage or external input detection voltage and generates reset or interrupt according to the register setting.

The VDDR area can maintain power through the RLDO after the chip enters power-down mode, which ensures that the real-time clock module (RTC) and wake-up timer (WKTM) can continue to operate and maintain 4KB of low-power SRAM (Ret-SRAM) data. The analog module is equipped with dedicated power supply pins to improve analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x0000_0400~0x0000_041F (of which 0x0000_0408~0x0000_041F is the reserved function address, the 24byte address needs to be set to 1 by the user to ensure that the chip operates correctly) and load the data into the initialization configuration register, and the user needs to program or erase the FLASH sector 0 to modify the initialization configuration register. Users need to program or erase FLASH sector 0 to modify the initialization configuration register.

1.4.7 Embedded FLASH Interface (EFM)

The FLASH interface provides access to FLASH through the ICODE, DCODE and MCODE buses, which allows programming, sector erase and full erase operations on FLASH; and accelerates code execution through instruction prefetching and caching mechanisms.

Key Features:

- Maximum 512KByte FLASH space
- I-CODE Bus 16Byte Prefetched Value
- Shared 64 caches (1Kbyte) on I-CODE and D-CODE buses
- Provides 960Bbyte One Time Programming Area (OTP)
- Supports low-power read operations
- Support for Guided Exchange Function
- Supports security protection and data encryption*1

*1: For specifications on Flash security protection and data encryption, please consult the sales window.

1.4.8 Internal SRAM (SRAM)

This product comes with 4KB of power-down mode retention SRAM (Ret_SRAM) and 188KB of system SRAM (SRAMH/SRAM1/SRAM2/SRAM3)

SRAM can be accessed byte, half-word (16-bit), or full-word (32-bit). Read and write operations are performed at CPU speed and wait cycles can be inserted.

Ret_SRAM provides 4KB of data retention space in power down mode.

SRAM3 with ECC checksum (Error Checking and Correcting) ECC checksum for the correction of one check two code, that is, you can correct one error, check two errors; SRAMH/SRAM1/SRAM2/Ret_SRAM with parity check (Even- parity check) each byte of data with one parity check, with one parity bit per byte of data.

1.4.9 General Purpose IO (GPIO)

GPIO Main Characteristics:

- 16 I/O pins per port group, may be less than 16 depending on actual configuration
- Support for pull-ups
- Supports push-pull, open-drain output modes
- Supports high, medium and low drive modes
- Inputs that support external interrupts
- Supports I/O pin peripheral function multiplexing, up to 16 selectable multiplexing functions per I/O pin, and up to 64 selectable functions for some I/Os.
- Each I/O pin can be programmed independently
- Each I/O pin can be selected to have 2 functions active at the same time (2 output functions active at the same time are not supported).

1.4.10 Interrupt control (INTC)

The functions of the interrupt controller (INTC) are selection of interrupt event requests as interrupt inputs to the NVIC to wake up WFI, and as event inputs to wake up WFE. selection of interrupt event requests as wake-up conditions for low-power modes (sleep and stop modes); interrupt control functions for the external pins NMI and EIRQ; and interrupt/event selection functions for software interrupts.

Key Specifications:

1) NVIC interrupt vectors: Please refer to the user's manual for the actual number of interrupt vectors used (excluding the 16 interrupt lines of the Cortex™-M4F), and each interrupt vector can be selected according to the interrupt selection register to correspond to the peripheral interrupt event request. For more information on

exceptions and NVIC programming, please refer to Chapter 5: Exceptions and Chapter 8: Nested Vector Interrupt Controller in the ARM Cortex™-M4F Technical Reference Manual.

2) Programmable Priority: 16 programmable priorities (4-bit interrupt priority is used)
3) Non-maskable interrupts: In addition to the NMI pin as a non-maskable interrupt source, a variety of system interrupt event requests can be independently selected.

As non-maskable interrupts, and each interrupt event request is equipped with an independent enable selection, hang, and clear the hang register.

4) Equipped with 16 external pin interrupts.
5) Configure multiple peripheral interrupt event requests, refer to the interrupt event request serial number list.
6) Equipped with 32 software interrupt event requests.
7) Interrupts can wake up the system in sleep mode and stop mode.

1.4.11 Automated Operating System (AOS)

The Automatic Operation System (AOS) is used to realize the linkage between peripheral hardware circuits without the aid of the CPU. The events generated by the peripheral circuits are used as AOS sources, such as the comparison match and overflow of the timer, the cycle signal of the RTC, the various states of sending and receiving data of the communication module (idle, full of receiving data, end of sending data, and empty of sending data), and the end of the conversion of the ADC, etc., which trigger the actions of the other peripheral circuits. The triggered peripheral circuit action is called AOS Target.

1.4.12 Keyboard scanning (KEYSCAN)

This product is equipped with one unit of Keyboard Control Module (KEYSCAN). KEYSCAN module supports keyboard array (row and column) scanning, where columns are driven by independent scanning output KEYOUTm (m=0~7) and row KEYINn (n=0~15) is detected as EIRQn (n=0~15) input. This module realizes the key recognition function by line scan query method.

1.4.13 Memory Protection Unit (MPU)

The MPUs can provide protection for the memory and can improve system security by blocking unauthorized access. Four host-specific MPU units and one IP-specific MPU unit are built into this product.

The ARM MPU provides CPU access control to the entire 4G address space.

The DMA MPU (DMPU) provides read/write access control for DMA_1/DMA_2/USB FS DMA to all 4G address space. The MPU action can be set to Ignore/Bus Error/Non-maskable Interrupt/Reset when an access to the prohibited space occurs.

The IP MPU provides access control to system IPs and security-related IPs in unprivileged mode.

1.4.14 DMA Controller (DMA)

DMA is used to transfer data between memories and peripheral function modules, enabling data

exchange between memories, between memories and peripheral function modules, and between peripheral function modules without CPU involvement.

- The DMA bus is independent of the CPU bus and is transmitted according to the AMBA AHB-Lite bus protocol.
- 8 independent channels (4 channels each for DMA_1 and DMA_2) for independent operation of different DMA transfer functions
- The start request source for each channel is configured through a separate trigger source selection register
- Transmit one block of data per request
- The minimum data block is 1 data and the maximum is 1024 data.

- Each data can be configured as 8bit, 16bit or 32bit.
- Up to 65535 transmissions can be configured
- Source and destination addresses can be independently configured as fixed, self-incrementing, self-decrementing, cyclic or jumps with specified offsets
- Three types of interrupts can be generated, block transfer completion interrupt, transfer completion interrupt, and transfer error interrupt. Each interrupt can be configured to be blocked or not. The block transfer completion and transfer completion can be used as event outputs, which can be used as trigger source inputs for other peripheral modules with hardware trigger function.
- Support chain transmission function, can realize one request to transmit multiple data blocks
- Supports external event triggered channel reset
- Can be set to enter the module stop state when not in use to reduce power consumption

1.4.15 Voltage Comparator (CMP)

The CMP is a peripheral module that compares two analog voltages, INP and INM, and outputs the results of the comparison.The CMP has three independent comparison channels, each of which has four inputs for the analog voltages INP and INM. The CMP has three independent comparison channels, each with four inputs for analog voltage INPs and INMs. One INP can be selected for single comparison with one INM, or multiple INPs can be scanned for comparison with the same INM. Comparison results can be read from registers, output to external pins, and generate interrupts and events.

1.4.16 Analog-to-digital converter (ADC)

The 12-bit ADC is an analog-to-digital converter that uses successive approximation. It has a maximum of 16 analog input channels that can convert external port and internal analog signals. These channels can be combined into a sequence for progressive scan conversion, and the sequence can be converted in a single pass, or in a continuous scan. The ADC module also has an analog watchdog function that monitors the conversion results of any given channel to see if it exceeds a user-set threshold.

ADC Main Characteristics:

- high performance
  - Configurable 12-bit, 10-bit and 8-bit resolutions
  - The frequency ratio of the peripheral clock PCLK4 to the A/D conversion clock ADCLK is selectable:
    - PCLK4: ADCLK = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4
      -ADCLK optional PLL asynchronous to the system clock HCLK, in which case the clock sources of PCLK4 and ADCLK are fixed to PLL at the same time,

and the frequency ratio is 1:1, and the original divider setting is invalidated.

- 2.5MSPS (PCLK4=ADCLK=60MHz, 12-bit, 17-cycle sampling)
- Individually programmable sampling time for each channel
- Independent data registers for each channel
- Data registers can be configured for data alignment
- Consecutive multiple conversion averaging function
- Analog watchdog to monitor conversion results

  - The ADC module can be set to stop when not in use.
- Analog Input Channels
  - Up to 16 external analog input channels
  - 1 internal reference voltage
- Conversion start condition
  - Software Setup Conversion Starts
  - Peripheral peripheral synchronization triggers conversion start
  - External pin triggers conversion start
- conversion mode
  - 2 scanning sequences A, B, single or multiple channels can be specified at will
  - Sequence A Single scan
  - Sequence A Continuous Scan
  - Dual sequence scanning, sequence A and B select trigger source independently, sequence B has higher priority than A
  - Synchronized mode (for devices with two or three ADCs)
- Interrupt and event signal output
  - Sequence A End of Scan Interrupt EOCA_INT and Event EOCA_EVENT
  - Sequence B End of Scan Interrupt EOCB_INT and Event EOCB_EVENT
  - Analog Watchdog Channel Compare Interrupt CHCMP_INT and Event CHCMP_EVENT, Sequence Compare Interrupt SEQCMP_INT and Event SEQCMP_EVENT
  - Each of the above 4 events can initiate a DMA

1.4.17 Temperature sensors (OTS)

The OTS can obtain the internal temperature of a chip to support reliable system operation. After initiating temperature measurement using a software or hardware trigger, the OTS provides a set of temperature-dependent digital quantities that can be calculated using a formula to obtain the temperature value.

1.4.18 Advanced Control Timer (Timer6)

The Advanced Control Timer 6 (Timer6) is a 16-bit count width high-performance timer, which can be used to count and generate different forms of clock waveforms for external use. The timer supports triangle and sawtooth waveform modes, and can generate various PWM waveforms; software synchronized counting and hardware synchronized counting can be realized between units; caching function is supported in each reference value register; 2-phase quadrature encoding and 3-phase quadrature encoding are supported; and EMB control is supported. This series of products is equipped with 3 units of Timer6.

1.4.19 Universal Control Timer (Timer4)

The Universal Control Timer 4 (Timer4) is a timer module for three-phase motor control, providing a variety of three-phase motor control solutions for different applications. The timer supports triangular and sawtooth waveform modes, and can generate various PWM waveforms; supports cache function; and supports EMB control. This series of products is equipped with a 3-unit Timer4.

1.4.20 Emergency Brake Module (EMB)

The Emergency Brake Module is a functional module that notifies the timer when certain conditions are met so that the timer stops outputting PWM signals to the external motor, and the following events are used to generate the notification:

- External port input level change
- PWM output port levels are in phase (same high or low)
- Voltage Comparator Comparison Results
- External oscillator stops oscillating
- Write Register Software Control

1.4.21 General-purpose timer (TimerA)

The general-purpose Timer A (TimerA) is a 16-bit count width timer with 8 PWM outputs. The timer supports triangle and sawtooth waveform modes to generate various PWM waveforms, software synchronized start counting, caching of comparison reference value registers, 2-phase orthogonal coded counting and 3-phase orthogonal coded counting. This series of products is equipped with 6 units of TimerA, which can realize 48 PWM outputs at most.

1.4.22 General purpose timer (Timer0)

General purpose Timer 0 (Timer0) is a basic timer that can be used for both synchronous and asynchronous counting. The timer contains 2 channels which can generate a compare match event during the counting period. This event can trigger an interrupt or be used as an event output to control other modules. This series has a 2-unit Timer0.

1.4.23 Real Time Clock (RTC)

The Real Time Clock (RTC) is a counter that stores time information in BCD code format. Records specific calendar times from year 00 to year 99. Supports both 12/24 hour time systems and automatically counts days 28, 29 (leap year) 30, and 31 based on the month and year.

1.4.24 Watchdog Counter (WDT)

There are two types of watchdog counters, one is a dedicated watchdog counter with a dedicated internal RC (WDTCLK:10KHz) as the count clock source.
(SWDT) and the other is a general purpose watchdog counter (WDT) with a count clock source of PCLK3. The Dedicated Watchdog and General Purpose Watchdog are 16-bit decrementing counters that are used to monitor for software failures due to deviations from normal operation of the application program caused by external disturbances or unforeseen logic conditions.

Both watchdogs support the window function. The window interval can be preset before

counting starts. When the count value is located in the window interval, the counter can be refreshed and counting starts again.

1.4.25 Serial communication interface (USART)

This product is equipped with 4 units of Serial Communication Interface Module (USART). The USART enables flexible full-duplex data exchange with external devices; the USART supports universal asynchronous serial communication interface (UART), clock synchronous communication interface, and smart card interface (ISO/IEC7816-3). It supports modem operation (CTS/RTS operation) and multiprocessor operation.

1.4.26 Integrated Circuit Bus (I2C)

This product carries 3 units of Integrated Circuit Bus (I2C).I2C is used as an interface between the microcontroller and the I2C serial bus. Provide multi-master mode function, can control all the I2C bus protocol, arbitration. Support standard mode, fast mode.

1.4.27 Serial Peripheral Interface (SPI)

This product is equipped with a 4-channel serial peripheral interface SPI, which supports high-speed full-duplex serial synchronous transmission and convenient data exchange with peripheral devices. Users can set up 3-wire/4-wire, master/slave and baud rate range as needed.

1.4.28 Four-wire serial peripheral interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) is a memory control module designed to communicate with serial ROMs with SPI-compatible interfaces. The main targets are serial Flash, serial EEPROM and serial FeRAM.

1.4.29 Integrated Circuit Built-in Audio Bus (I2S)

I2S (Inter_IC Sound Bus) an integrated circuit built-in audio bus that specializes in data transfer between audio devices. This product is equipped with 4 I2S and has the following features.

functionality	Main characteristics
communication method	• Supports full-duplex and half-duplex communication • Supports master or slave mode operation
data format	• Selectable channel length: 16/32 bit • Optional transmission data length: 16/24/32 bits • Data shift order: MSB start
baud	• 8-bit programmable linear prescaler for accurate audio sampling frequency • Supported sampling frequency 192k, 96k, 48k, 44.1k, 32k, 22.05k, 16k, 8k • Outputs a drive clock to drive external audio components at a fixed ratio of 256*Fs (Fs is the audio sampling frequency).
Supports I2S protocol	• I2S Philips Standard • MSB Alignment Criteria • LSB Alignment Criteria • PCM Standard
data buffer	Input and output FIFO buffers with 2-word deep, 32-bit wide buffers Input and output FIFO buffers with 2 words deep and 32 bits wide
clock source	– Internal I2SCLK (UPLLR/UPLLQ/UPLLP/MPLLR/MPLLQ/MPLLP); can be used by The external clock on the I2S_EXCK pin provides the
disruptions	• Generate an interrupt when the effective space in the transmit buffer reaches the alarm threshold. • Generate an interrupt when the effective space in the receive buffer reaches the alarm threshold. • Receive data area is full and there is still a write data request, receive overflow • Send data area is empty and there is still a request to send, send underflow • Send data area is full and there is still a request to write data, send overflow

1.4.30 CAN communication interface (CAN)

This product is equipped with a CAN communication interface module (CAN) 1 unit and 512 Bytes of RAM for CAN to store transmit/receive messages. It supports the CAN2.0B protocol specified in ISO11898-1 and the TTCAN protocol specified in ISO11898-4.

1.4.31 USB2.0 Full Speed Module (USB FS)

The USB2.0 Full Speed Module (USB FS) is a 1-unit, on-chip, full-speed PHY. The USB FS is a dual-role (DRD) controller that supports both slave and master functions. In host mode, the USB FS supports both full-speed and low-speed transceivers, while only full-speed transceivers are supported in slave mode.

The USB FS module on this product can generate an SOF event when a SOF token is successfully sent in the host mode or received in the slave mode.

1.4.32 Cryptographic coprocessing module (CPM)

The Cryptographic Co-Processing Module (CPM) consists of three sub-modules: the AES encryption and decryption algorithm processor, the HASH secure hashing algorithm, and the TRNG true random number generator.

The AES encryption and decryption algorithm processor follows standard data encryption and decryption standards and can realize encryption and decryption operations with a 128-bit key length.

The HASH Secure Hash Algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm) which is compliant with the national standard "FIPS PUB 180-3" published by the National Institute of Standards and Technology, and can produce a 256-bit message digest output for messages up to 2^64 bits in length.

The TRNG True Random Number Generator is a random number generator based on continuous analog noise, providing 64bit random numbers.

1.4.33 Data Computing Unit (DCU)

The Data Computing Unit (DCU) is a module that simply processes data without the aid of a CPU. Each DCU unit has 3 data registers and can add or subtract 2 data, compare sizes, and perform window comparison. This product is equipped with 4 DCUs, each of which can perform its own functions independently.

1.4.34 CRC Computation Unit (CRC)

The CRC algorithm in this module follows the definition of ISO/IEC13239 and uses 32-bit and 16-bit CRCs respectively. the generating polynomial for CRC32 is X32+X26+X23+X22+X16+X12+X11+X10+X8+X7+X5+X4+X2+X+1. the generating polynomial for CRC16 is X16+X12+X5+1. the generating polynomial for CRC16 is X16+X12+X5+1. the generating polynomial for CRC16 is X16+X12+X5+1.

1.4.35 SDIO Controller (SDIOC)

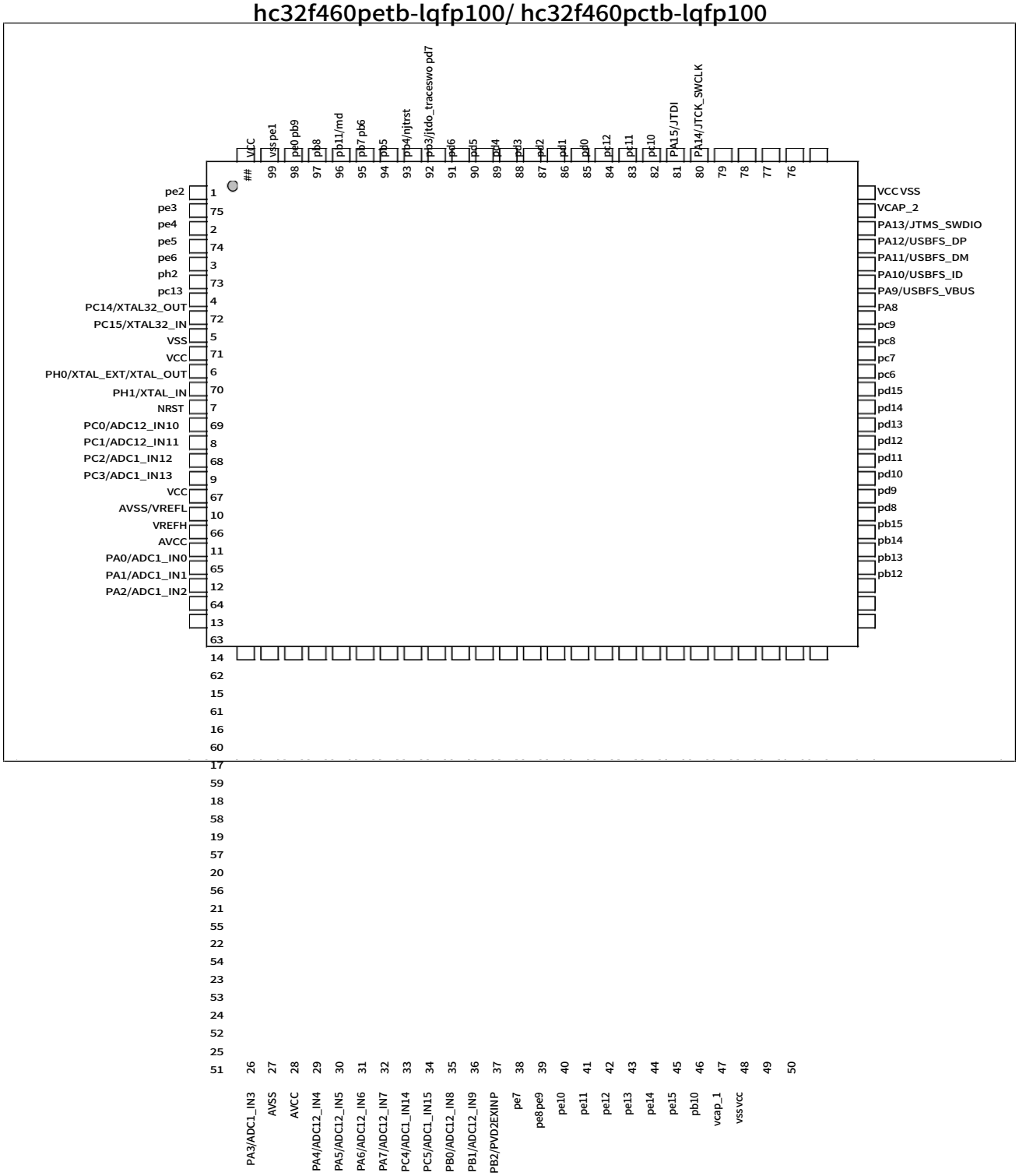
The SDIO controller is the host in the SD/SDIO/MMC communication protocol. This product has two SDIO controllers, each of which provides a host interface for communicating with SD cards that support the SD2.0 protocol, SDIO devices, and MMC devices that support the eMMC4.51 protocol.The SDIOC features are as follows:

- Supports SDSC, SDHC, SDXC format SD cards and SDIO devices.
- Supports 1-wire (1bit) and 4-wire (4bit) SD buses
- Supports 1-wire (1bit), 4-wire (4bit) and 8-wire (8bit) MMC buses
- Card recognition and hardware write protection

2 Pinout and Function (Pinouts)

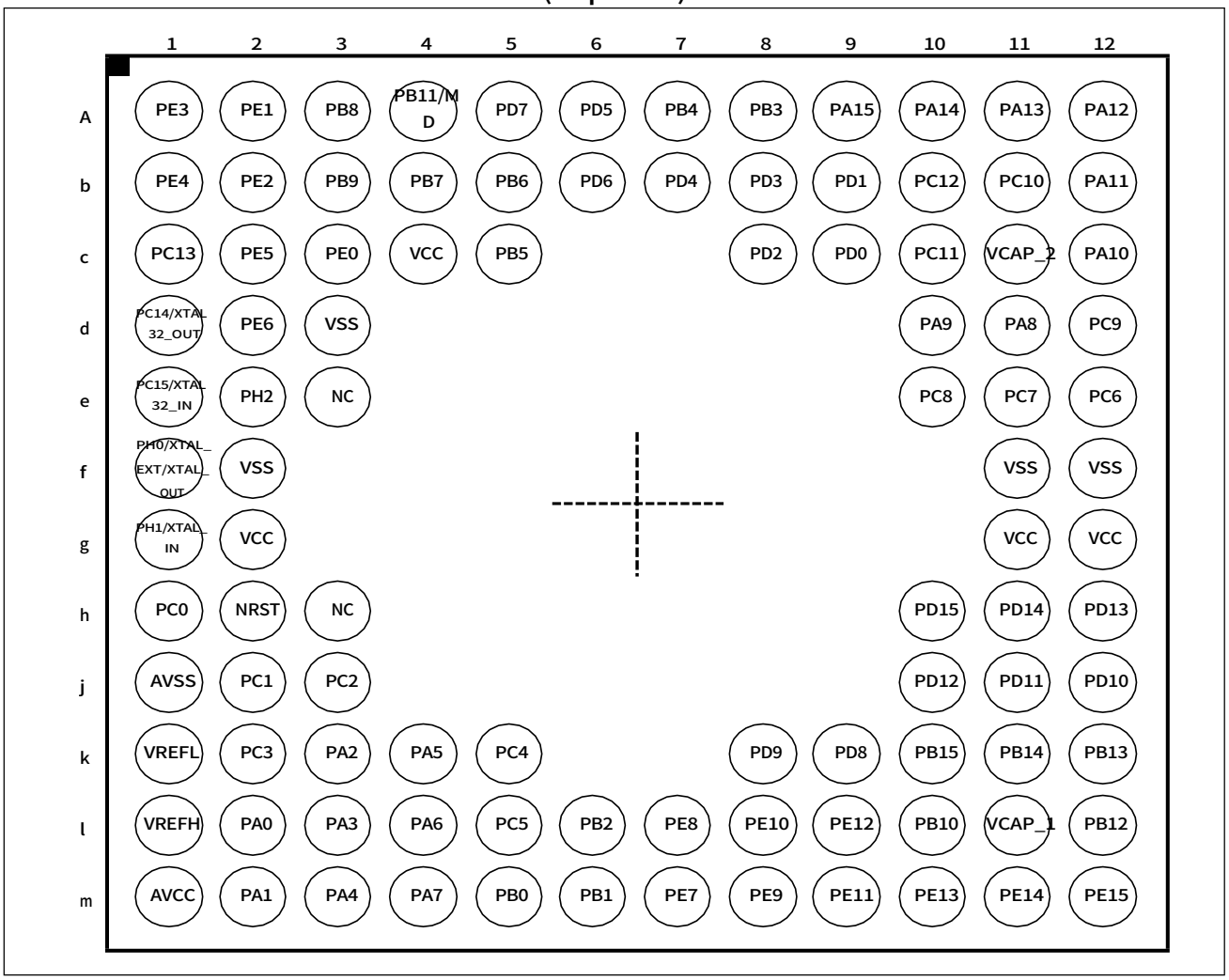
2.1 Pinouts

hc32f460petb-lqfp100/ hc32f460pctb-lqfp100



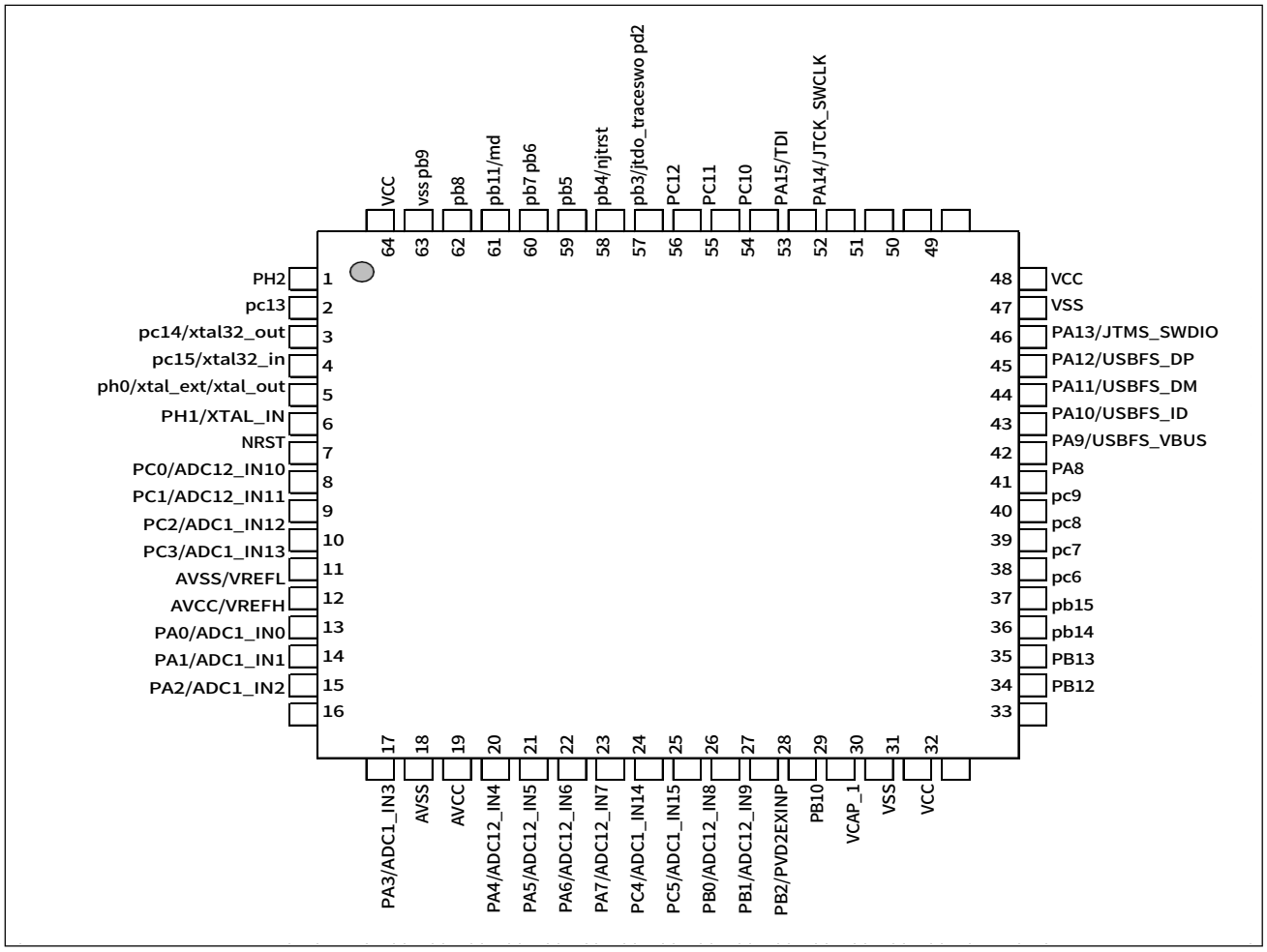
hc32f460pehb-vfbga100

(Top View)

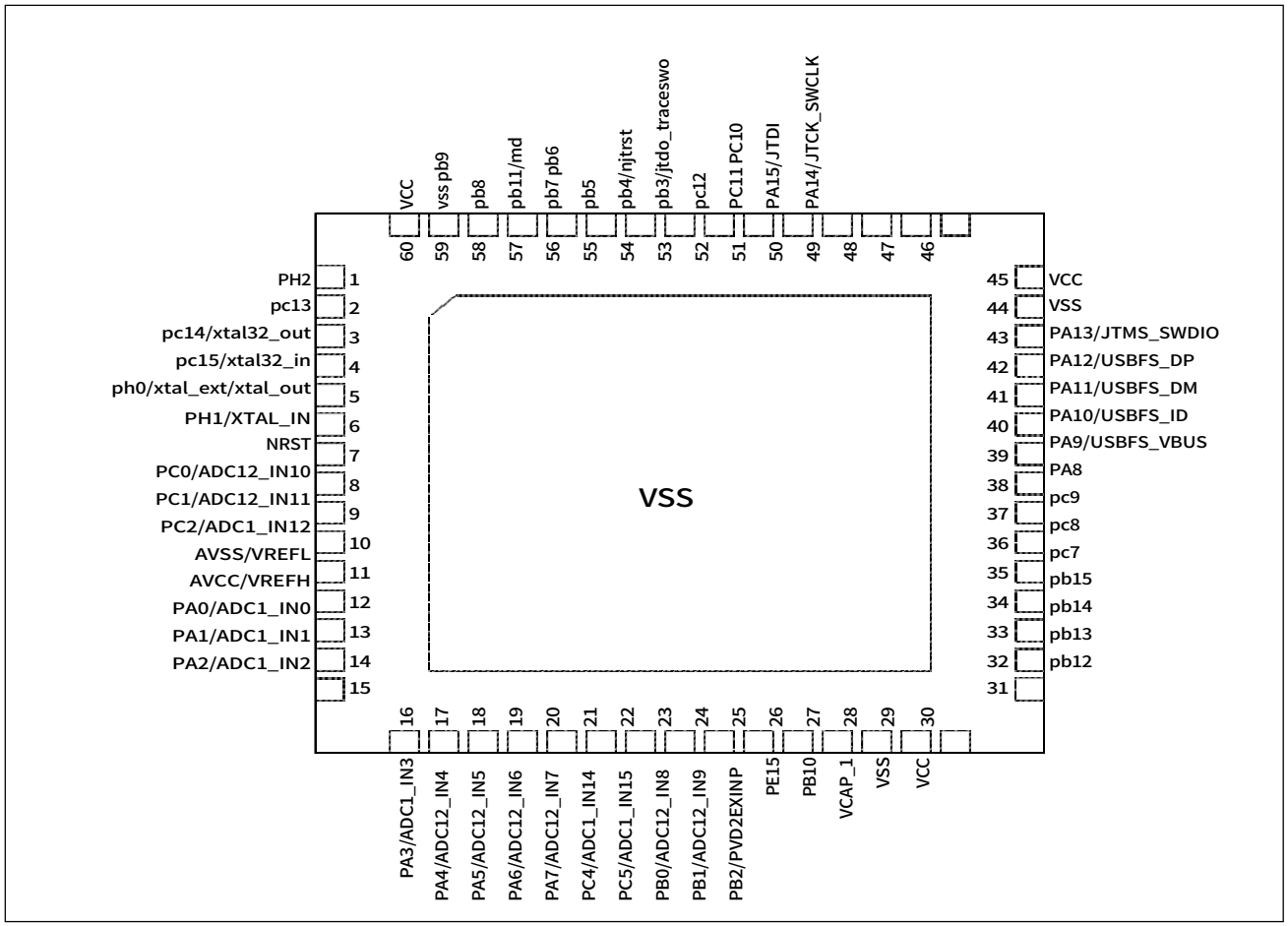


Note: A1 is Pin 1.

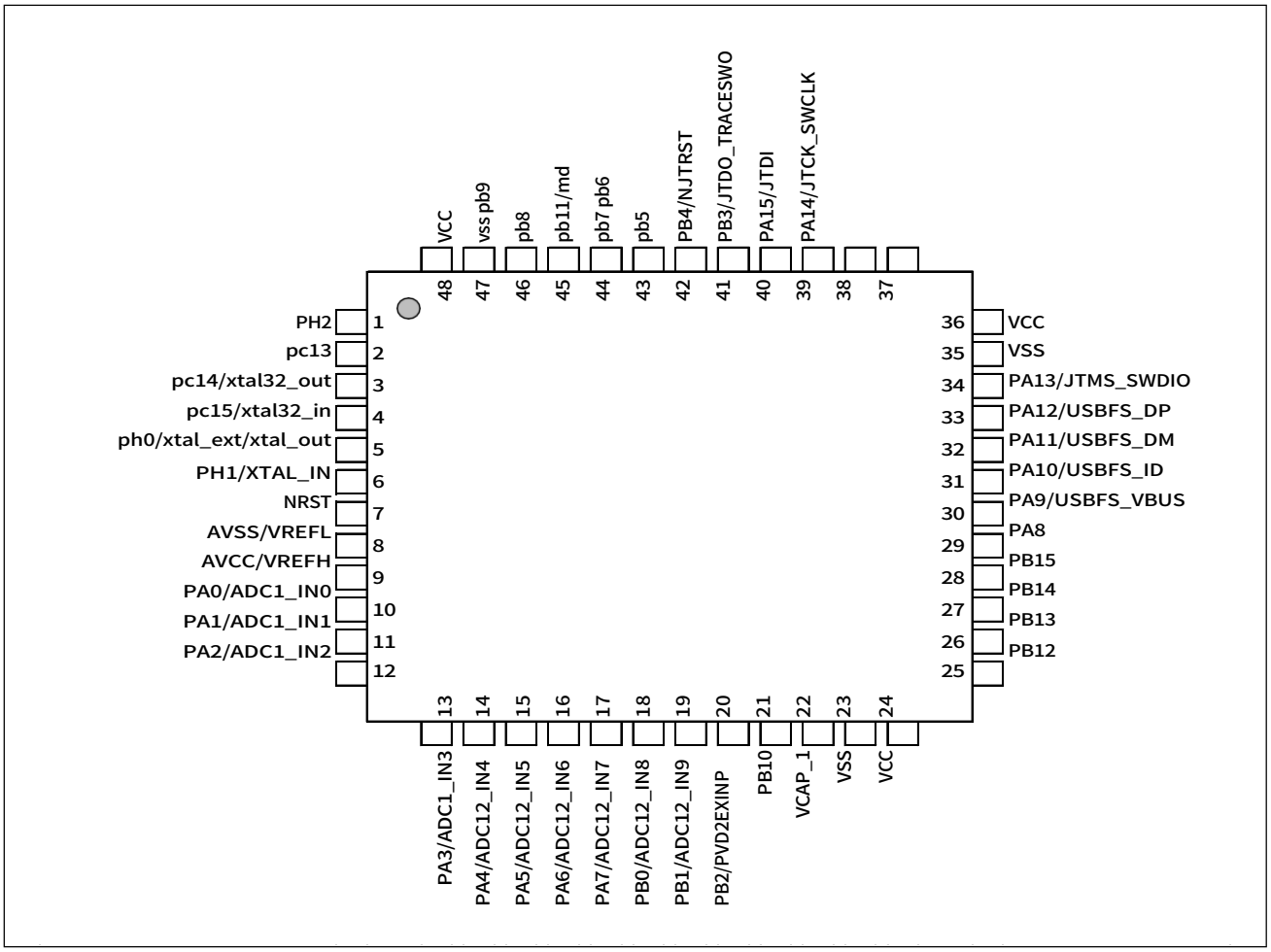
hc32f460keta-lqfp64/ hc32f460kcta-lqfp64



hc32f460keua-qfn60tr



hc32f460jeta-lqfp48/ hc32f460jcta-lqfp48



hc32f460jeua-qfn48tr

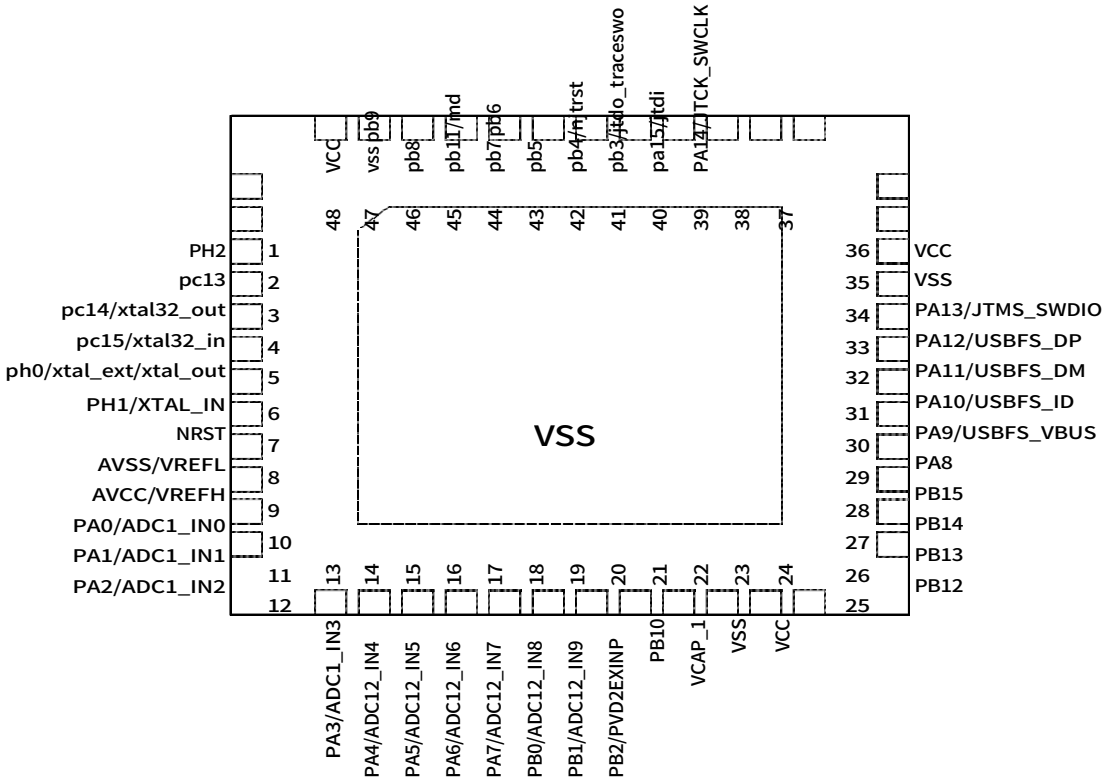


Figure 2-1 Pinout Diagram

2.2 Pin Function Chart

Table 2-1 Pin Function Table

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB, TIMA	USART/SPI/ QSPI	KEY	SDIO	USBFS/I2S	–	–	–	EVNTPT	EVENTOUT	–	Communication Funcs
1	B2	–	–	–	PE2		EIRQ2	TRACECK	GPO				TIMA_3_PWM5			USART3_CK								EVENTOUT		Func_Grp2
2	A1	–	–	–	PE3		EIRQ3	TRACED0	GPO				TIMA_3_PWM6			USART4_CK								EVENTOUT		Func_Grp2
3	B1	–	–	–	PE4		EIRQ4	TRACED1	GPO				TIMA_3_PWM7											EVENTOUT		Func_Grp2
4	C2	–	–	–	PE5		EIRQ5	TRACED2	GPO				TIMA_3_PWM8											EVENTOUT		Func_Grp2
5	D2	–	–	–	PE6		EIRQ6	TRACED3	GPO															EVENTOUT		Func_Grp2
6	E2	1	1	1	PH2		EIRQ2		GPO	FCMREF	TIM4_2_CLK		TIMA_4_PWM7		EMB_IN4			SDIO2_D4	I2S3_EXCK					EVENTOUT		Func_Grp2
7	C1	2	2	2	PC13		EIRQ13		GPO	RTC_OUT			TIMA_4_PWM8					SDIO2_CK	I2S3_MCK				EVNTP313			Func_Grp2
8	D1	3	3	3	PC14	XTAL32_OUT	EIRQ14		GPO				TIMA_4_PWM5										EVNTP314			
9	E1	4	4	4	PC15	XTAL32_IN	EIRQ15		GPO				TIMA_4_PWM6										EVNTP315			
10	F2	–	–	–	VSS																					
11	G2	–	–	–	VCC																					
12	F1	5	5	5	PH0	XTAL_EXT/XTAL_OUT	EIRQ0		GPO					TIMA_5_PWM3												
13	G1	6	6	6	PH1	XTAL_IN	EIRQ1		GPO					TIMA_5_PWM4												
14	H2	7	7	7	NRST																					
15	H1	8	8	–	PC0	ADC12_IN10/CMP3_INP3	EIRQ0		GPO				TIMA_2_PWM5					SDIO2_D5					EVNTP300	EVENTOUT		Func_Grp1
16	J2	9	9	–	PC1	ADC12_IN11	EIRQ1		GPO				TIMA_2_PWM6					SDIO2_D6					EVNTP301	EVENTOUT		Func_Grp1
17	J3	10	10	–	PC2	ADC1_IN12	EIRQ2		GPO				TIMA_2_PWM7		EMB_IN3			SDIO2_D7					EVNTP302	EVENTOUT		Func_Grp1
18	K2	11	–	–	PC3	ADC1_IN13/CMP1_INM2	EIRQ3		GPO				TIMA_2_PWM8					SDIO1_WP					EVNTP303	EVENTOUT		Func_Grp1
19	–	–	–	–	VCC																					
20	J1	12	11	8	AVSS																					
–	K1	–	–	–	VREFL																					
21	L1	–	–	–	VREFH																					
22	M1	13	12	9	AVCC																					
23	L2	14	13	10	PA0	ADC1_IN0/CMP1_INP1	EIRQ0/WKUP0_0		GPO		TIM4_2_OUH		TIMA_2_PWM1/ TIMA_2_CLKA		TIMA_2_TRIG	SPI1_SS1		SDIO2_D4					EVNTP100	EVENTOUT		Func_Grp1
24	M2	15	14	11	PA1	ADC1_IN1/CMP1_INP2	EIRQ1		GPO		TIM4_2_OUL		TIMA_2_PWM2/ TIMA_2_CLKB	TIMA_3_TRIG		SPI1_SS2		SDIO2_D5					EVNTP101	EVENTOUT		Func_Grp1
25	K3	16	15	12	PA2	ADC1_IN2/CMP1_INP3	EIRQ2		GPO		TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM1/ TIMA_5_CLKA		SPI1_SS3		SDIO2_D6					EVNTP102	EVENTOUT		Func_Grp1
26	L3	17	16	13	PA3	ADC1_IN3/PGAVSS/ CMP1_INP4	EIRQ3		GPO		TIM4_2_OVL		TIMA_2_PWM4	TIMA_5_PWM2/ TIMA_5_CLKB				SDIO2_D7					EVNTP103	EVENTOUT		Func_Grp1
27	–	18	–	–	AVSS																					
–	E3	–	–	–	NC																					
28	–	19	–	–	AVCC																					
29	M3	20	17	14	PA4	ADC12_IN4/CMP2_INP1/CMP3_INP4	EIRQ4		GPO		TIM4_2_OWH			TIMA_3_PWM5		USART2_CK	KEYOUT0		I2S1_EXCK				EVNTP104	EVENTOUT		Func_Grp1
30	K4	21	18	15	PA5	ADC12_IN5/CMP2_INP2	EIRQ5		GPO		TIM4_2_OWL		TIMA_2_PWM1/ TIMA_2_CLKA	TIMA_3_PWM6	TIMA_2_TRIG		KEYOUT1		I2S1_MCK				EVNTP105	EVENTOUT		Func_Grp1
31	L4	22	19	16	PA6	ADC12_IN6/CMP2_INP3	EIRQ6		GPO					TIMA_3_PWM1/ TIMA_3_CLKA	EMB_IN2		KEYOUT2	SDIO1_CMD					EVNTP106	EVENTOUT		Func_Grp1

32	M4	23	20	17	PA7	ADC12_IN7/CMP1_INM1/CMP2_INM1/CMP3_INM1	EIRQ7		GPO		TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	TIMA_3_PWM2/TIMA_3_CLKB	EMB_IN3		KEYOUT3	SDIO2_WP				EVNTP107	EVENTOUT		Func_Grp1

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB, TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	–	–	–	EVNTPT	EVENTOUT	–	Communication Funcs
33	K5	24	21	–	PC4	ADC1_IN14/CMP2_INM2	EIRQ4		GPO		TIM4_2_OUH			TIMA_3_PWM7		USART1_CK		SDIO2_CD					EVNTP304	EVENTOUT		Func_Grp1
34	L5	25	22	–	PC5	ADC1_IN15/CMP3_INM2	EIRQ5		GPO		TIM4_2_OUL			TIMA_3_PWM8				SDIO2_CMD					EVNTP305	EVENTOUT		Func_Grp1
35	M5	26	23	18	PB0	ADC12_IN8/CMP3_INP1	EIRQ0		GPO		TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	TIMA_3_PWM3		USART4_CK	KEYOUT4	SDIO2_CMD					EVNTP200	EVENTOUT		Func_Grp1
36	M6	27	24	19	PB1	ADC12_IN9/CMP3_INP2	EIRQ1/WKUP0_1		GPO		TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_3_PWM4		QSPI_QSSN	KEYOUT5	SDIO2_D3	I2S2_EXCK				EVNTP201	EVENTOUT		Func_Grp1
37	L6	28	25	20	PB2	PVD2EXINP	EIRQ2/WKUP0_2		GPO	VCOUT123		TIM6_TRIGB	TIMA_1_PWM8		EMB_IN1	QSPI_QSIO3		SDIO2_D2	I2S2_MCK				EVNTP202	EVENTOUT		Func_Grp1
38	M7	–	–	–	PE7		EIRQ7		GPO	ADTRG1		TIM6_TRIGA	TIMA_1_TRIG			USART1_CK								EVENTOUT		
39	L7	–	–	–	PE8		EIRQ8		GPO		TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5											EVENTOUT		
40	M8	–	–	–	PE9		EIRQ9		GPO		TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA											EVENTOUT		
41	L8	–	–	–	PE10		EIRQ10		GPO		TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6											EVENTOUT		
42	M9	–	–	–	PE11		EIRQ11		GPO		TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB											EVENTOUT		
43	L9	–	–	–	PE12		EIRQ12		GPO		TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7			SPI1_SS1								EVENTOUT		Func_Grp2
44	M10	–	–	–	PE13		EIRQ13		GPO		TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3			SPI1_SS2								EVENTOUT		Func_Grp2
45	M11	–	–	–	PE14		EIRQ14		GPO		TIM4_1_CLK		TIMA_1_PWM4			SPI1_SS3		SDIO1_CD						EVENTOUT		Func_Grp2
46	M12	–	26	–	PE15		EIRQ15		GPO				TIMA_1_PWM8	TIMA_5_TRIG	EMB_IN2	USART4_CK		SDIO1_WP						EVENTOUT		Func_Grp2
47	L10	29	27	21	PB10		EIRQ10		GPO	ADTRG2	TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM8		QSPI_QSIO2		SDIO1_D7	I2S3_EXCK				EVNTP210	EVENTOUT		Func_Grp2
48	L11	30	28	22	VCAP_1																					
49	F12	31	29	23	VSS																					
50	G12	32	30	24	VCC																					
51	L12	33	31	25	PB12		EIRQ12		GPO	VCOUT1	TIM4_2_OVL	TIM6_TRIGB	TIMA_1_PWM8		EMB_IN2	QSPI_QSIO1		SDIO2_D1	I2S3_MCK				EVNTP212	EVENTOUT		Func_Grp2
52	K12	34	32	26	PB13		EIRQ13		GPO	VCOUT2	TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5			QSPI_QSIO0		SDIO2_D0					EVNTP213	EVENTOUT		Func_Grp2
53	K11	35	33	27	PB14		EIRQ14		GPO	VCOUT3	TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6			QSPI_QSCK		SDIO1_D6					EVNTP214	EVENTOUT		Func_Grp2
54	K10	36	34	28	PB15		EIRQ15		GPO	RTC_OUT	TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_6_TRIG	EMB_IN4	USART3_CK		SDIO1_CK					EVNTP215	EVENTOUT		Func_Grp2
55	K9	–	–	–	PD8		EIRQ8		GPO		TIM4_3_OUL			TIMA_6_PWM1/TIMA_6_CLKA		QSPI_QSIO0	KEYOUT7						EVNTP408	EVENTOUT		Func_Grp2
56	K8	–	–	–	PD9		EIRQ9		GPO		TIM4_3_OVL			TIMA_6_PWM2/TIMA_6_CLKB		QSPI_QSIO1	KEYOUT6						EVNTP409	EVENTOUT		Func_Grp2
57	J12	–	–	–	PD10		EIRQ10		GPO		TIM4_3_OWL			TIMA_6_PWM3		QSPI_QSIO2	KEYOUT5						EVNTP410	EVENTOUT		Func_Grp2
58	J11	–	–	–	PD11		EIRQ11		GPO		TIM4_3_CLK			TIMA_6_PWM4		QSPI_QSIO3	KEYOUT4						EVNTP411	EVENTOUT		Func_Grp2
59	J10	–	–	–	PD12		EIRQ12		GPO				TIMA_4_PWM1/TIMA_4_CLKA	TIMA_5_PWM5									EVNTP412	EVENTOUT		
60	H12	–	–	–	PD13		EIRQ13		GPO				TIMA_4_PWM2/TIMA_4_CLKB	TIMA_5_PWM6									EVNTP413	EVENTOUT		
61	H11	–	–	–	PD14		EIRQ14		GPO				TIMA_4_PWM3	TIMA_5_PWM7									EVNTP414	EVENTOUT		
62	H10	–	–	–	PD15		EIRQ15		GPO				TIMA_4_PWM4	TIMA_5_PWM8									EVNTP415	EVENTOUT		
63	E12	37	–	–	PC6		EIRQ6		GPO				TIMA_3_PWM1/TIMA_3_CLKA	TIMA_5_PWM8		QSPI_QSCK	KEYOUT3	SDIO1_D6					EVNTP306	EVENTOUT		Func_Grp2
64	E11	38	35	–	PC7		EIRQ7		GPO		TIM4_2_CLK		TIMA_3_PWM2/TIMA_3_CLKB	TIMA_5_PWM7		QSPI_QSSN	KEYOUT2	SDIO1_D7	I2S2_EXCK				EVNTP307	EVENTOUT		Func_Grp2
65	E10	39	36	–	PC8		EIRQ8		GPO		TIM4_2_OWH		TIMA_3_PWM3	TIMA_5_PWM6		USART3_CK	KEYOUT1	SDIO1_D0	I2S2_MCK				EVNTP308	EVENTOUT		Func_Grp2
66	D12	40	37	–	PC9		EIRQ9		GPO	MCO_2	TIM4_2_OWL		TIMA_3_PWM4	TIMA_5_PWM5			KEYOUT0	SDIO1_D1					EVNTP309	EVENTOUT		Func_Grp1
67	D11	41	38	29	PA8		EIRQ8/WKUP2_0		GPO	MCO_1	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA			USART1_CK		SDIO1_D1	USBFS_SOF				EVNTP108	EVENTOUT		Func_Grp1
68	D10	42	39	30	PA9		EIRQ9/WKUP2_1		GPO		TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB					SDIO1_D2	USBFS_VBUS				EVNTP109	EVENTOUT		Func_Grp1
69	C12	43	40	31	PA10		EIRQ10/WKUP2_2		GPO		TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3	TIMA_5_TRIG				SDIO1_CD	USBFS_ID				EVNTP110	EVENTOUT		Func_Grp1

LQFP100	VFBGA100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
									GPO	other	TIM4	TIM6	TIMA	TIMA	EMB, TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	–	–	–	EVNTPT	EVENTOUT	–	Communication Funcs

70	B12	44	41	32	PA11		EIRQ11/WKUP2_3		GPO		TIM4_1_CLK		TIMA_1_PWM4		EMB_IN1			SDIO2_CD	USBFS_DM				EVNTP111	EVENTOUT		Func_Grp1
71	A12	45	42	33	PA12		EIRQ12/WKUP3_0		GPO		TIM4_3_OWL	TIM6_TRIGA	TIMA_1_TRIG	TIMA_6_PWM1/TIMA_6_CLKA				SDIO2_WP	USBFS_DP				EVNTP112	EVENTOUT		Func_Grp1
72	A11	46	43	34	PA13		EIRQ13/WKUP3_1	JTMS_SWDIO	GPO				TIMA_2_PWM5	TIMA_6_PWM2/TIMA_6_CLKB		SPI2_SS1		SDIO2_D3					EVNTP113	EVENTOUT		Func_Grp1
73	C11	–	–	–	VCAP_2																					
74	F11	47	44	35	VSS																					
75	G11	48	45	36	VCC																					
76	A10	49	46	37	PA14		EIRQ14/WKUP3_2	JTCK_SWCLK	GPO				TIMA_2_PWM6	TIMA_6_PWM3	TIMA_4_TRIG	SPI2_SS2		SDIO2_D2	I2S1_EXCK				EVNTP114	EVENTOUT		Func_Grp1
77	A9	50	47	38	PA15		EIRQ15/WKUP3_3	JTDI	GPO				TIMA_2_PWM1/TIMA_2_CLKA	TIMA_6_PWM4	TIMA_2_TRIG	SPI2_SS3		SDIO2_D1	I2S1_MCK				EVNTP115	EVENTOUT		Func_Grp1
78	B11	51	48	–	PC10		EIRQ10		GPO		TIM4_3_OUH		TIMA_2_PWM7	TIMA_5_PWM1/TIMA_5_CLKA				SDIO1_D2					EVNTP310	EVENTOUT		Func_Grp1
79	C10	52	49	–	PC11		EIRQ11		GPO		TIM4_3_OVH		TIMA_2_PWM8	TIMA_5_PWM2/TIMA_5_CLKB				SDIO1_D3					EVNTP311	EVENTOUT		Func_Grp1
80	B10	53	50	–	PC12		EIRQ12		GPO		TIM4_3_OWH		TIMA_4_TRIG	TIMA_5_PWM3				SDIO1_CK					EVNTP312	EVENTOUT		Func_Grp1
81	C9	–	–	–	PD0		EIRQ0		GPO	VCOUT123				TIMA_5_PWM4									EVNTP400	EVENTOUT		Func_Grp1
82	B9	–	–	–	PD1		EIRQ1		GPO				TIMA_3_TRIG	TIMA_6_PWM5									EVNTP401	EVENTOUT		Func_Grp1
83	C8	54	–	–	PD2		EIRQ2		GPO				TIMA_2_PWM4	TIMA_6_PWM6				SDIO1_CMD					EVNTP402	EVENTOUT		Func_Grp1
84	B8	–	–	–	PD3		EIRQ3		GPO	VCOUT1				TIMA_6_PWM7									EVNTP403	EVENTOUT		
85	B7	–	–	–	PD4		EIRQ4		GPO	VCOUT2				TIMA_6_PWM8									EVNTP404	EVENTOUT		
86	A6	–	–	–	PD5		EIRQ5		GPO	VCOUT3													EVNTP405	EVENTOUT		
87	B6	–	–	–	PD6		EIRQ6		GPO							USART2_CK							EVNTP406	EVENTOUT		
88	A5	–	–	–	PD7		EIRQ7		GPO							USART2_CK							EVNTP407	EVENTOUT		
89	A8	55	51	39	PB3		EIRQ3/WKUP0_3	JTDO_TRACESWO	GPO	FCMREF	TIM4_3_CLK		TIMA_2_PWM2/TIMA_2_CLKB	TIMA_6_PWM5				SDIO2_D0					EVNTP203	EVENTOUT		Func_Grp2
90	A7	56	52	40	PB4		EIRQ4/WKUP1_0	NJTRST	GPO		TIM4_3_OWL		TIMA_3_PWM1/TIMA_3_CLKA	TIMA_6_PWM6				SDIO1_D0					EVNTP204	EVENTOUT		Func_Grp2
91	C5	57	53	41	PB5		EIRQ5/WKUP1_1		GPO		TIM4_3_OWH		TIMA_3_PWM2/TIMA_3_CLKB	TIMA_6_PWM7				SDIO1_D3	I2S4_EXCK				EVNTP205	EVENTOUT		Func_Grp2
92	B5	58	54	42	PB6		EIRQ6/WKUP1_2		GPO	ADTRG2	TIM4_3_OVL		TIMA_4_PWM1/TIMA_4_CLKA	TIMA_6_PWM8				SDIO2_CK	I2S4_MCK				EVNTP206	EVENTOUT		Func_Grp2
93	B4	59	55	43	PB7		EIRQ7/WKUP1_3		GPO	ADTRG1	TIM4_3_OVH		TIMA_4_PWM2/TIMA_4_CLKB					SDIO1_D0					EVNTP207	EVENTOUT		Func_Grp2
94	A4	60	56	44	PB11/MD		NMI																EVNTP211			
95	A3	61	57	45	PB8		EIRQ8		GPO		TIM4_3_OUL		TIMA_4_PWM3				KEYOUT7	SDIO1_D4	USBFS_DRVVBUS				EVNTP208	EVENTOUT		Func_Grp2
96	B3	62	58	46	PB9		EIRQ9		GPO		TIM4_3_OUH		TIMA_4_PWM4	TIMA_6_TRIG		SPI2_SS1	KEYOUT6	SDIO1_D5					EVNTP209	EVENTOUT		Func_Grp2
97	C3	–	–	–	PE0		EIRQ0		GPO	MCO_1			TIMA_4_TRIG			SPI2_SS2								EVENTOUT		Func_Grp2
98	A2	–	–	–	PE1		EIRQ1		GPO	MCO_2	TIM4_3_CLK					SPI2_SS3								EVENTOUT		Func_Grp2
99	D3	63	59	47	VSS																					
100	C4	64	60	48	VCC																					
–	H3	–	–	–	NC																					

Notes:

– In the above table, there are 64 pins supporting Func32~63 function selection, Func32~63 are mainly for serial communication function (including USART, SPI, I2C, I2S, CAN) divided into two groups, Func_Grp1 and Func_Grp2. Please refer to Table 2-2 for details.

Table 2-2 Func32~63

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
Func_Grp1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_SS0	SPI1_SCK	SPI2_MOSI	SPI2_MISO	SPI2_SS0	SPI2_SCK
Func_Grp2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_SS0	SPI3_SCK	SPI4_MOSI	SPI4_MISO	SPI4_SS0	SPI4_SCK

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
Func_Grp1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2S1_SD	I2S1_SDIN	I2S1_WS	I2S1_CK	I2S2_SD	I2S2_SDIN	I2S2_WS	I2S2_CK				
Func_Grp2	I2C3_SDA	I2C3_SCL	CAN_TxD	CAN_RxD	I2S3_SD	I2S3_SDIN	I2S3_WS	I2S3_CK	I2S4_SD	I2S4_SDIN	I2S4_WS	I2S4_CK				

Table 2-3 Port Configuration

Package	Port Group	Bits																Pin Count	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Total	
LQFP100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	83
VFBGA100	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	–	–	–	–	–	–	–	–	–	–	–	–	–	o	o	o	3	
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	52
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	–	–	–	–	–	–	–	–	–	–	–	–	–	o	–	–	1	
	PortH	–	–	–	–	–	–	–	–	–	–	–	–	–	o	o	o	3	
QFN60	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	50
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	–	o	o	–	o	o	o	14	
	PortE	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	o	1	
	PortH	–	–	–	–	–	–	–	–	–	–	–	–	–	o	o	o	3	
LQFP48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	38
QFN48	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	–	–	–	–	–	–	–	–	–	–	–	–	–	3	
	PortH	–	–	–	–	–	–	–	–	–	–	–	–	–	o	o	o	3	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Table 2-4 General Functional Specifications

Port		pull up	open-drain output	driving ability	5V Voltage	note
PortA	PA0~PA10 PA13~PA15	be in favor of	be in favor of	Low，medium，high	Support *	
	PA11, PA12	be in favor of	be in favor of	Low，medium，high	unsupported	
PortB	PB0~PB10, PB12~PB15	be in favor of	be in favor of	Low，medium，high	Support *	
	PB11	be in favor of	–	–	be in favor of	Input Specific
PortC	PC0~PC15	be in favor of	be in favor of	Low，medium，high	Support *	
PortD	PD0~PD15	be in favor of	be in favor of	Low，medium，high	be in favor of	
PortE	PE0~PE15	be in favor of	be in favor of	Low，medium，high	be in favor of	
PortH	PH0~PH2	be in favor of	be in favor of	Low，medium，high	be in favor of	

Notes:

– When used as an analog function, the input voltage must not be higher than VREFH/AVCC.

2.3 Pin Function Description

Table 2-5 Pin Functions

form	functional name	I/O	clarification
Power	VCC	I	electric power source
	VSS	I	POWER GROUND
	VCAP_1~2	IO	Kernel Voltage
	AVCC	I	analog power
	AVSS	I	Analog Power Ground
	VREFH	I	Analog Reference Voltage
	VREFL	I	Analog Reference Voltage
System	NRST	I	Reset Pin, Active Low
	MD	I	Mode Pins
PVD	PVD2EXINP	I	PVD2 External input comparison voltage
Clock	XTAL_IN	IO	External master clock oscillator interface
	XTAL_EXT/XTAL_OUT	IO	XTAL_EXT External clock input
	XTAL32_IN	I	External Subclock (32K) Oscillator Interface
	XTAL32_OUT	o	
	MCO_1~2	o	Internal clock output
GPIO	GPIOxy (x= A~E,H. y=0~15)	IO	General purpose inputs and outputs
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0~15)	I	Maskable external interrupt
	WKUPx_y (x,y=0~3)	I	PowerDown mode external wake-up input
	NMI	I	Non-maskable external interrupt
Event Port	EVNTPxy (x=1~4, y=0~15)	IO	Event Port Input and Output Functions
Key	KEYOUTx(x=0~7)	o	KEYSCAN Scan Output Signal
JTAG/SWD	JTCK_SWCLK	I	online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECK	o	Trace debugging synchronized clock output
	TRACED0~3	o	Trace debug data output
FCM	FCMREF	I	External Reference Clock Input for Clock Frequency Measurement
RTC	RTCOUT	o	1Hz clock output

Timer4	TIM4_x_CLK	I	Counting Clock Port Input
(x=1~3)	TIM4_x_OUH	IO	PWM port U-phase output
form	**functional name**	**I/O**	**clarification**
	TIM4_x_OUL	IO	PWM port U-phase output
	TIM4_x_OVH	IO	PWM Port V-Phase Output
	TIM4_x_OVL	IO	PWM Port V-Phase Output
	TIM4_x_OWH	IO	PWM port W-phase output
	TIM4_x_OWL	IO	PWM port W-phase output
Timer6 (x=1~3)	TIM6_TRIGA	I	External Event Trigger A Input
	TIM6_TRIGB	I	External Event Trigger B Input
	TIM6_x_PWMA	IO	External Event Trigger Input or PWM Port Output
	TIM6_x_PWMB	IO	External Event Trigger Input or PWM Port Output
TimerA (x=1~6)	TIMA_x_TRIG	I	External event-triggered inputs
	TIMA_x_PWM1/TIMA_x_CLKA	IO	External Event Trigger Input or PWM Port Output or Counter Clock Port Input
	TIMA_x_PWM2/TIMA_x_CLKB	IO	External Event Trigger Input or PWM Port Output or Counter Clock Port Input
	TIMA_x_PWMy (y=3~8)	IO	External Event Trigger Input or PWM Port Output
EMB	EMB_INx (x=1~4)	I	Groupx (x=1~4) port input control signal
USARTx (x=1~4)	USARTx_TX	IO	Send data
	USARTx_RX	IO	receive data
	USARTx_CK	IO	communications clock
	USARTx_RTS	o	Request to send a signal
	USARTx_CTS	I	Clears the transmit signal
SPIx (x=1~4)	SPIx_MISO	IO	Master input/slave output data transfer pins
	SPIx_MOSI	IO	Master output/slave input data transfer pins
	SPIx_SCK	IO	transmission clock
	SPIx_SS0	IO	Slave select input and output pins
	SPIx_SS1~3	o	Slave Select Output Pin
QSPI	QSPI_QSIO0~3	IO	data cable
	QSPI_QSCK	o	clock output
	QSPI_QSSN	o	Slave Selection
I2Cx (x=1~3)	I2Cx_SCL	IO	clock line
	I2Cx_SDA	IO	data cable
I2Sx (x=1~4)	I2Sx_SD	IO	serial data
	I2Sx_SDIN	I	Full duplex serial data input
	I2Sx_WS	IO	word choice
	I2Sx_CK	IO	serial clock
	I2Sx_EXCK	I	External Clock Source
	I2Sx_MCK	o	master clock
CAN	CAN_TxD	O	Send data
	CAN_RxD	I	receive data
SDIOx	SDIOx_Dy (y=0~7)	IO	SD Data Signal

form	functional name	I/O	clarification
	SDIOx_CK	o	SD clock output signal
	SDIOx_CMD	IO	SD Command and Response Signal
	SDIOx_CD	I	SD Card Recognition Status Signal
	SDIOx_WP	I	SD card write-protect status signal
USBFS	USBFS_DM	IO	USBFS On-Chip Full Speed PHY D-Signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+ signaling
	USBFS_VBUS	I	USBFS VBUS Signal
	USBFS_ID	I	USBFS ID Signal
	USBFS_SOF	o	USBFS SOF Pulse Output Signal
	USBFS_DRVVBUS	o	USBFS VBUS Driver License Signal
CMPx (x=1~3)	VCOUT1	o	Analog Comparison Channel 1 Result Output
	VCOUT2	O	Analog Comparison Channel 2 Result Output
	VCOUT3	O	Analog Comparison Channel 3 Result Output
	VCOUT123	O	Analog Comparison Channel 1~3 Result OR Output
	CMPx_INPy	I	Analog Comparator Channel x Positive Voltage y Input
	CMPx_INMy	I	Analog Comparator Channel x Negative Voltage y Input
ADC	ADTRG1	I	ADC1 AD conversion external startup source
	ADTRG2	I	ADC2 AD Conversion External Startup Source
	ADC1_INx (x=0~3,12~15)	I	ADC1 External analog input port
	ADC12_INx (x=4~11)	I	ADC1 and ADC2 share common external analog input port
	PGAVSS	I	PGA Ground Input

2.4 Pinouts

Table 2-6 Pin Usage

pinout	Instructions for use
VCC	Power supply, connect 1.8V~3.6V voltage, and connect decoupling capacitor near VSS pin (refer to [Electrical Characteristics (ECs)])
VSS	Power Ground to 0V
VCAP_1~2	Kernel voltage, connect capacitors close to the VSS pin to stabilize the kernel voltage (refer to [Electrical Characteristics (ECs)])
AVCC	Analog power supply, powering the analog module, connected to the same voltage as VCC (refer to Electrical Characteristics (ECs)) When the analog module is not used, short to VCC.
AVSS/VREFL	Analog power ground/reference voltage, connected to the same voltage as AVSS (refer to Electrical Characteristics (ECs)) When the analog module is not used, short out the VSS.
VREFH	Analog reference voltage of ADC1, ADC2, connected to a voltage not higher than AVCC When ADC is not used, short to AVCC.
PB11/MD	Mode input, fixed to the input state. When the reset pin (NRST) is deasserted (changed from low to high), this pin must fix the Set to high level. Recommended connection resistor (4.7KΩ) to VCC (pull-up)
NRST	Reset pin, active low. Connect resistor to VCC when not in use (pull-up)
Pxy, x=A~E, H, y=0~15	General purpose pins. When used as an input, the input voltage should not exceed 5 V. When the input voltage exceeds VCC, the internal pull-up is prohibited, and the input voltage of the pin that does not support 5 V tolerance should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC. Suspend when not in use, or connect resistor to VCC (pull-up)/VSS (pull-down)

3 Electrical Characteristics (ECs)

3.1 parameter condition

All voltages are referenced to VSS unless otherwise noted.

3.1.1 Minimum and maximum values

Unless otherwise noted, all device minimums and maximums are guaranteed by design or characterized under worst case ambient temperature, supply voltage, and clock frequency conditions.

3.1.2 typical value

Typical data are analyzed by design or characterization at T_A = 25 °C, VCC = 3.3 V, unless otherwise noted.

3.1.3 typical curve

Unless otherwise noted, all typical curves are untested and are for design purposes only.

3.1.4 load capacitance

The load conditions used to measure the pin parameters are shown in Figure 3-1 (left).

3.1.5 Pin Input Voltage

The measurement of the input voltage on the device pins is shown in Figure 3-1 (right).

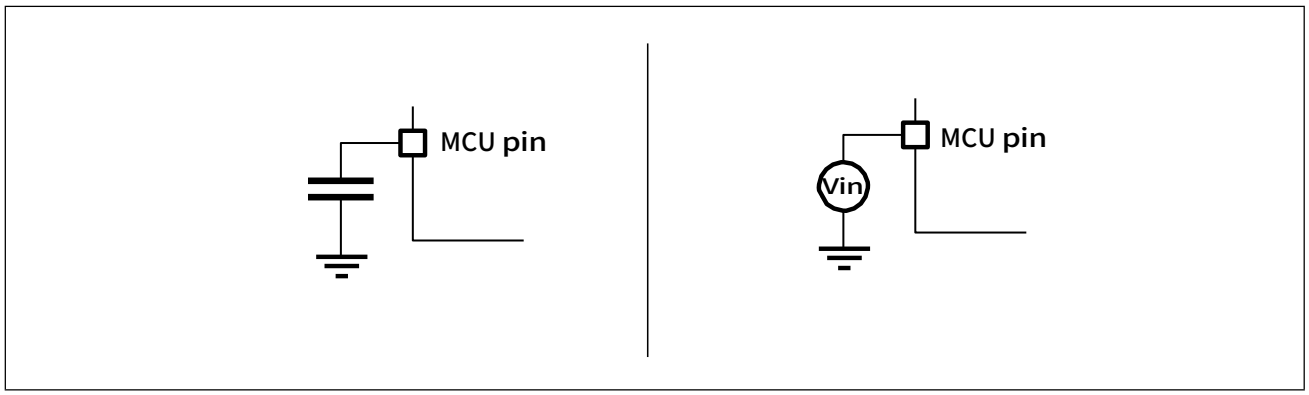


Figure 3-1 Pin Load Conditions (left) and Input Voltage Measurements (right)

3.1.6 Power Solutions

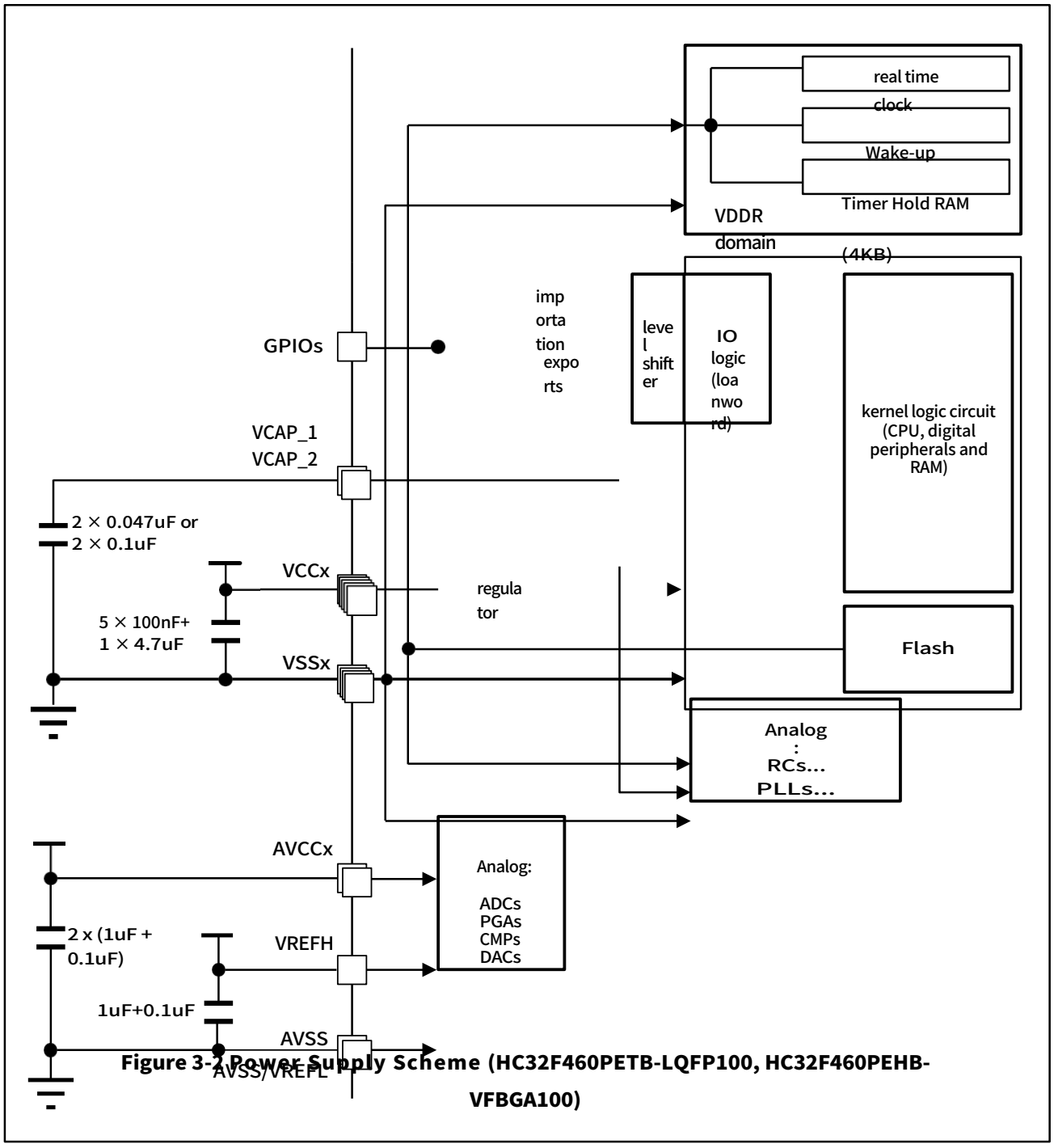


Figure 3-2 Power Supply Scheme (HC32F460PETB-LQFP100, HC32F460PEHB-VFBGA100)

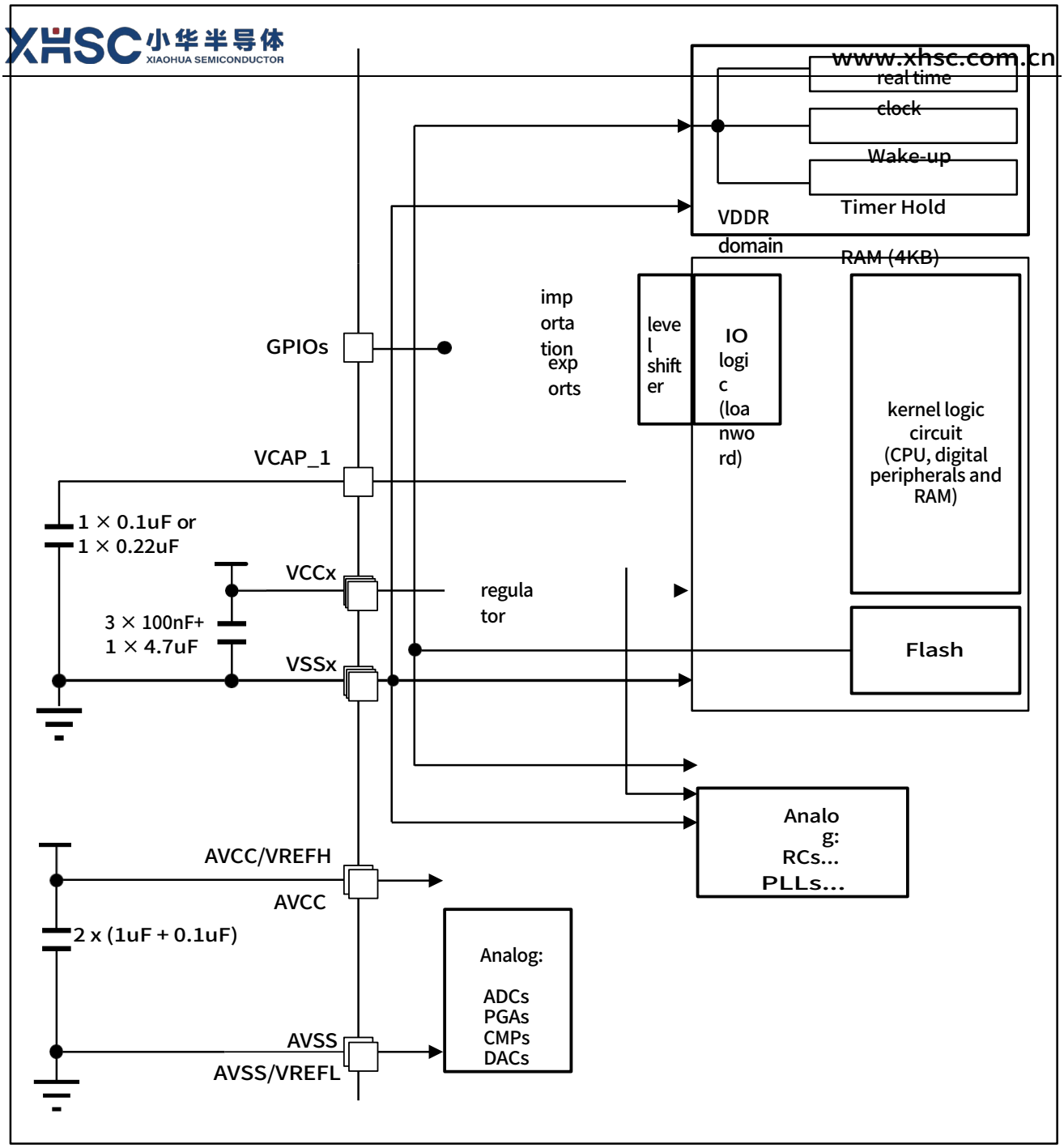


Figure 3-3 Power Supply Scheme (HC32F460KETA-LQFP64)

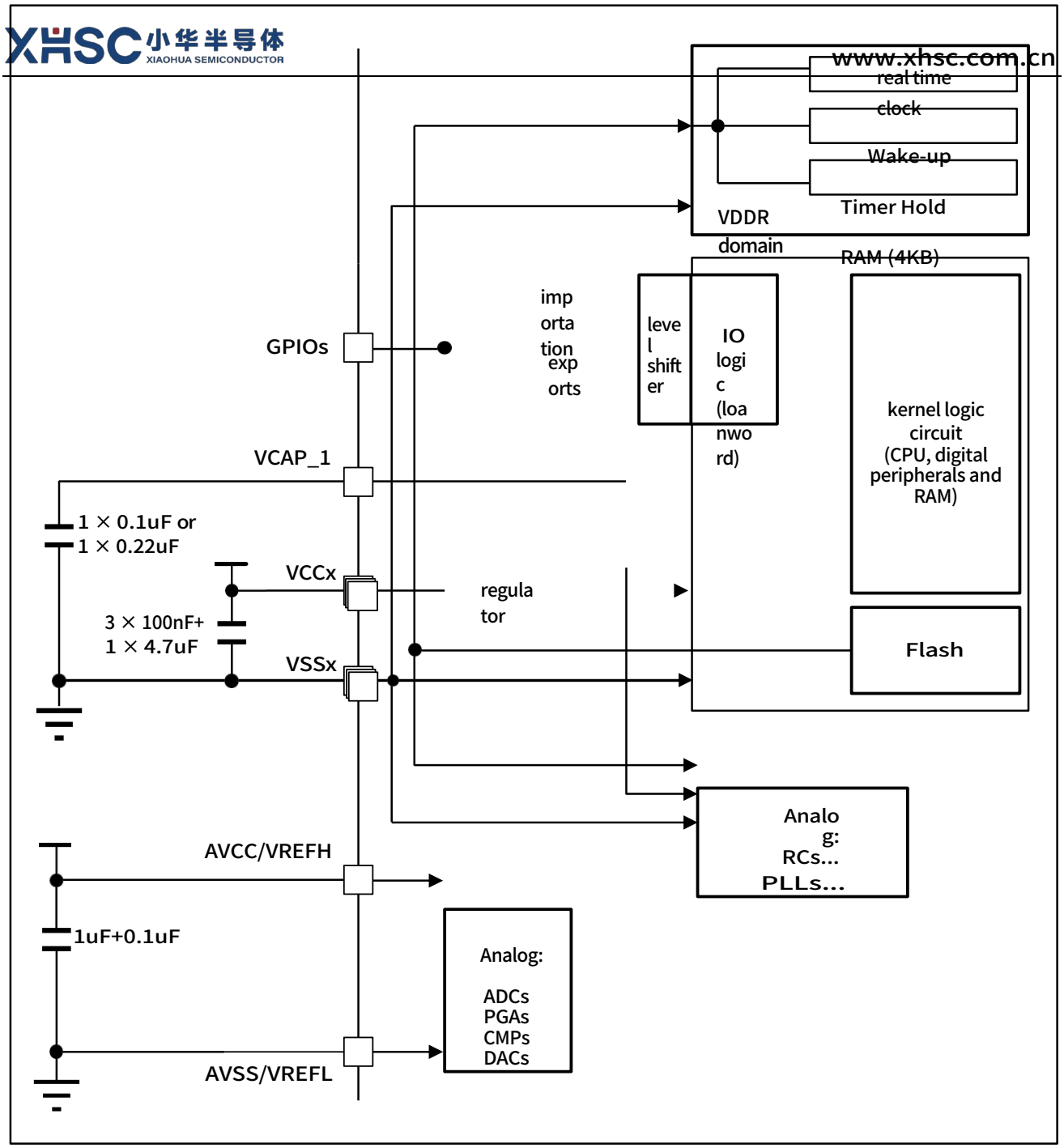


Figure 3-4 Power Supply Scheme (HC32F460KEUA-QFN60TR/ HC32F460JETA-LQFP48/ HC32F460JEUA-QFN48TR)

1. A 4.7μF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS = VSS.
3. Each power pair (e.g. VCC/VSS, AVCC/AVSS ...) must be decoupled using the filtered ceramic capacitors described above. These capacitors must be placed as close as possible to or below the appropriate pins on the underside of the PCB to ensure proper operation of the device. It is not recommended to remove the filter capacitors to reduce PCB size or cost. This may cause the device to operate improperly.
4. The capacitors used on the VCAP_1/VCAP_2 pins of the chip are as follows: 1) For chips with both VCAP_1 and VCAP_2 pins, 0.047uF or 0.1uF capacitors can be used

on each pin (total capacity is 0.094uF or 0.2uF)

(2) For chips with only VCAP_1 pin, 0.1uF or 0.22uF capacitor can be used. When waking up from power-down mode, VCAP_1/VCAP_2 needs to be charged during the kernel voltage establishment process. On the one hand, a smaller total capacity of VCAP_1/VCAP_2 can shorten the charging time and provide fast response time for the application; on the other hand, a larger total capacity of VCAP_1/VCAP_2 will increase the charging time, but also provide better electromagnetic compatibility (EMC). Users can choose a larger or smaller capacitance value depending on EMC and system response speed requirements. The total capacity of VCAP_1/VCAP_2 must match the value assigned to the PWC_PWRC3.PDTS bit. When the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, make sure the PWC_PWRC3.PDTS bit is cleared to zero before entering the power-down mode. If the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, make sure the PWC_PWRC3.PDTS bit is clear before entering the power-down mode.

5. The stability of the main regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin with the capacitance value CEXT determined according to the stability requirements of the system. The capacitance value CEXT and ESR requirements are as follows:

Table 3-1 VCAP_1/ VCAP_2 Operating Conditions

notation	parameters	prerequisite
CEXT	Capacitance value of external capacitor	0.047μF/ 0.1μF/ 0.22uF
ESR	Equivalent series resistance of the external capacitor ESR	< 0.3Ω

3.1.7 Current consumption measurement

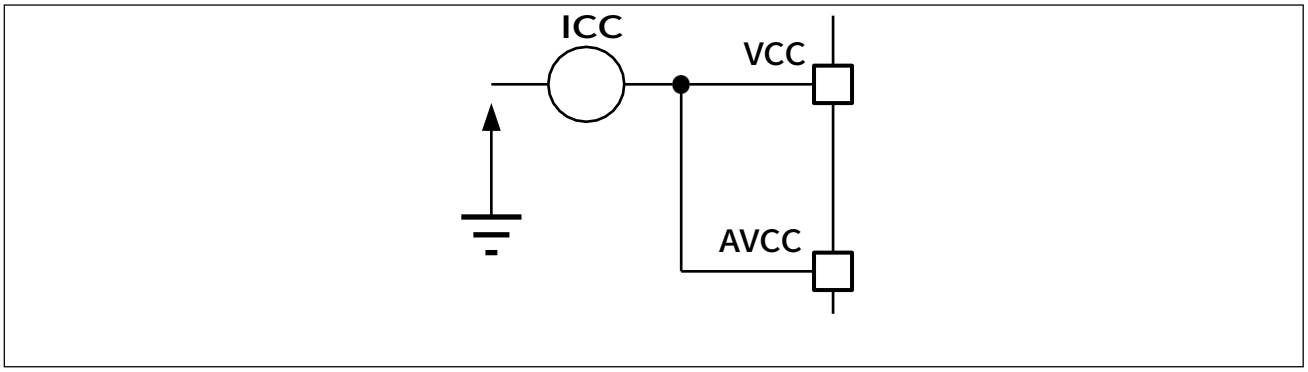


Figure 3-5 Current Consumption Measurement Scheme

3.2 Absolute maximum rating

Loads applied to the device in excess of the absolute maximum ratings listed in Table 3-2, Table 3-3, and Table 3-4 may result in permanent damage to the device. These values are stress ratings only and do not imply that the device functions properly under these conditions. Prolonged operation at the maximum ratings may affect the reliability of the device.

Table 3-2 Voltage Characteristics

notation	sports event	minimum value	maximum values	unit (of measure)
VCC-VSS	External mains voltage (including AVCC, VCC)(1)	-0.3	4.0	V
VIN	Input voltage on 5V withstand pin(2)	VSS-0.3	VCC+4.0 (5.8V max)	
	On the PA11/USBFS_DM and PA12/USBFS_DP pins Input Voltage	VSS-0.3	4.0	
VESD (HBM)	Electrostatic discharge voltage (human model)	Please refer to [Electrical Sensitivity]		–

1. All mains (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the permitted range.
2. The maximum value of V_{IN} must always be followed. See Table 3-3 for information on the maximum allowable injection current values.

Table 3-3 Current Characteristics

notation	sports event	maximum values	unit (of measure)
ΣIVCC	Total current flowing into all V_{CCX} power cords (pull current)(1)	240	mA
ΣIVSS	Total current flowing out of all V_{SSX} ground wires (flood current) (1)	-240	
IVCC	Maximum current flow (pull current) into each V_{CCX} power cord (1)	100	
IVSS	Maximum current flow (sink current) per V_{SSX} ground wire (1)	-100	
IIO	Output sink current for arbitrary I/O and control pins	40	
	Output pull current for arbitrary I/O and control pins	-40	
ΣIIO	Total output sink current on all I/O and control pins	120	
	Total output pull current on all I/O and control pins	-1,120.	

1. All mains (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the permitted range.

Table 3-4 Thermal Characteristics

notation	sports event	numerical value	unit (of measure)
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum Junction Temperature	125	°C

3.3 working conditions

3.3.1 General working conditions

Table 3-5 General Working Conditions

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
fHCLK	Internal AHB clock frequency	Ultra high speed mode [1] PWRC2.DVS=00 PWRC2.DDAS=1111	0	–	200	MHz
		High-speed mode [1] PWRC2.DVS=11 PWRC2.DDAS=1111	0	–	168	
		Ultra low speed mode PWRC2.DVS=10 PWRC2.DDAS=1000	0	–	8	
VCC	Standard Operating Voltage	–	1.8	–	3.6	V
VAVCC(2)	Analog Operating Voltage	–	1.8	–	3.6	
VIN	Input voltage on 5V withstand pin (3)	2 V ≤ VCC ≤ 3.6 V	-0.3	–	5.5	
		VCC ≤ 2 V	-0.3	–	5.2	
	PA11/USBFS_DM PA12/USBFS_DP Pin input voltage		-0.3	–	VCC+0.3	
TJ	Junction temperature range		-40	–	125	°C

1. Mass production testing guaranteed.
2. If the VREFH pin is present, the following condition must be taken into account: $V_{AVCC-VREFH} < 1.2$ V.
3. To keep the voltage above VCC+0.3, the internal pull-up/down resistors must be disabled.

3.3.2 Operating conditions at power-up/power-down

TA Obey general working conditions.

Table 3-6 Operating conditions at power-up/power-down

notation	parameters	minimum value	maximum values	unit (of measure)

tVCC	VCC Rise Time Rate	20	20000	μs/V
	VCC Falling Time Rate	20	20000	

3.3.3 Reset and Power Control Module Features

Table 3-7 Reset and Power Control Module Characteristics

notation	parameters	prerequisite		minimum value	typical value	maximum values	unit (of measure)
VBOR	BOR monitoring voltage	Ultra High Speed Mode	ICG1.BOR_LEV[1:0]=00	1.88	1.99	2.09	V
			ICG1.BOR_LEV [1:0]=01	1.99	2.09	2.20	V
			ICG1.BOR_LEV [1:0]=10	2.09	2.20	2.30	V
			ICG1.BOR_LEV [1:0]=11	2.30	2.40	2.51	V
		High Speed Mode Ultra Low Speed Mode	ICG1.BOR_LEV[1:0]=00	1.80	1.90	2.00	V
			ICG1.BOR_LEV [1:0]=01	1.90	2.00	2.10	V
			ICG1.BOR_LEV [1:0]=10	2.00	2.10	2.20	V
			ICG1.BOR_LEV [1:0]=11	2.20	2.30	2.40	V
VPVD1	PVD1 monitoring voltage (3)	Ultra High Speed Mode	pvd1lvl[2:0]=000	1.99	2.09	2.20	V
			pvd1lvl[2:0]=001	2.09	2.20	2.30	V
			pvd1lvl[2:0]=010	2.30	2.40	2.51	V
			pvd1lvl[2:0]=011	2.54	2.67	2.79	V
			pvd1lvl[2:0]=100	2.65	2.77	2.90	V
			pvd1lvl[2:0]=101	2.75	2.88	3.00	V
			pvd1lvl[2:0]=110	2.85	2.98	3.11	V
			pvd1lvl[2:0]=111	2.96	3.08	3.21	V
		High speed mode Ultra low speed mode	pvd1lvl[2:0]=000	1.90	2.00	2.10	V
			pvd1lvl[2:0]=001	2.00	2.10	2.20	V
			pvd1lvl[2:0]=010	2.20	2.30	2.40	V
			pvd1lvl[2:0]=011	2.43	2.55	2.67	V
			pvd1lvl[2:0]=100	2.53	2.65	2.77	V
			pvd1lvl[2:0]=101	2.63	2.75	2.87	V
			pvd1lvl[2:0]=110	2.73	2.85	2.97	V
			pvd1lvl[2:0]=111	2.83	2.95	3.07	V
		Ultra High	pvd2lvl[2:0]=000	2.09	2.20	2.30	V
			pvd2lvl[2:0]=001	2.30	2.40	2.51	V
			pvd2lvl[2:0]=010	2.54	2.67	2.79	V
			pvd2lvl[2:0]=011	2.65	2.77	2.90	V
			PVD2LVL[2:0]=100	2.75	2.88	3.00	V

VPVD2	PVD2 monitoring voltage (3)	Speed Mode	pvd2lvl[2:0]=101	2.85	2.98	3.11	V
			pvd2lvl[2:0]=110	2.96	3.08	3.21	V
			pvd2lvl[2:0]=111(2)	1.05	1.15	1.25	V
		High speed mode Ultra low speed mode	pvd2lvl[2:0]=000	2.00	2.10	2.20	V
			pvd2lvl[2:0]=001	2.20	2.30	2.40	V
			pvd2lvl[2:0]=010	2.43	2.55	2.67	V

notation	parameters	conditional		minimum value	typical value	maximum values	unit (of measure)
			pvd2lvl[2:0]=011	2.53	2.65	2.77	V
			PVD2LVL[2:0]=100	2.63	2.75	2.87	V
			pvd2lvl[2:0]=101	2.73	2.85	2.97	V
			pvd2lvl[2:0]=110 (1)	2.83	2.95	3.07	V
			pvd2lvl[2:0]=111(2)	1.00	1.10	1.20	V
Vpvdhyst	Late PVD1,2 Stagnation (3)			–	100	–	mV
VPOR(1)	Power-on/power-off reset thresholds	Rise along VPOR		1.60	1.68	1.76	V
		Falling edge VPDR		1.56	1.64	1.72	V
VPORhyst	POR hysteresis			–	40	–	mV
IRUSH	Inrush current at regulator power-up (POR or from standby) (Wake-up call)			–	100	150	mA
TNRST	NRST reset minimum height			500	–	–	ns
TIPVD1	PVD1 reset release timing			300	380	460	μs
TIPVD2	PVD2 reset release			300	380	460	μs

	timing					
TINRST	NRST reset release timing		25	35	50	μs
TRIPT	Internal reset time		140	160	200	μs
TRSTBOR	BOR reset release timing		440	520	610	μs
TRSTPOR	Power-on reset release timing		–	2500	3000	μs

1. Mass production testing guaranteed.
2. When PVD2LVDL[2:0] = 111, the comparison voltage is the external input comparison voltage at the PVD2EXINP pin.
3. The PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; the PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops when PVD2LVL[2:0] is set to 111, and the PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops when PVD2LVD[2:0] is set to a value other than 111.
4. The hysteresis of PVD1,2 is the difference between the monitoring voltage when VCC is rising and the monitoring voltage when VCC is falling. PVD1 monitoring voltage on VCC rise = Vpvd1 + Vpvdhyst.
   PVD2 monitoring voltage at VCC rise = Vpvd2 + Vpvdhyst.

3.3.4 Supply Current Characteristics

Current consumption is affected by a number of parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, program location in memory, and running code. Current consumption measurements are described in Figure 3-5. The current consumption measurements for the various modes of operation described in this section were obtained under laboratory conditions from a set of test codes running on FLASH.

The specific conditions are as follows:

1) All I/O pins are in input mode with static values (no load) on VCC or VSS.
2) Clock frequency selections are ultra-high speed mode fHCLK=200MHz, high speed mode fHCLK=168MHz/120MHz/24MHz and ultra-low speed mode fHCLK=8MHz/1MHz.
3) The power consumption modes are categorized into: normal operation mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, power-down mode ICC_PD and Dhrystone operation mode ICC_DHRYSTONE.
4) Peripheral Clock ON/OFF Refer to the specific current test item.
5) The PLL is turned on in ultra-high speed mode fHCLK=200MHz and high speed mode fHCLK=168MHz/120MHz.

Table 3-8 Ultra High-Speed Mode Current Consumption

para digm	Parameter	Symbol	conditional	Ta (°C)	Product Specification			Unit
					Min	Typ(1)	Max(2)	
Ultra High Speed Mode	fHCLK= 200MHz	ICC_RUN	while(1), full mode Block Clock OFF	-40	–	16	–	mA
			while(1), full mode Block Clock ON	-40	–	29	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	17	–	mA
			CACHE ON	-40	–	19	–	mA
		ICC_SLEEP	Full Module Clock OFF	-40	–	11	–	mA
			Full Module Clock ON	-40	–	24	–	mA
		ICC_RUN	while(1), full mode Block Clock OFF	25	–	16	–	mA
			while(1), full mode Block Clock ON	25	–	29	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	17	–	mA
			CACHE ON	25	–	19	–	mA
		ICC_SLEEP	Full Module Clock OFF	25	–	11	–	mA
			Full Module Clock ON	25	–	24	–	mA
		ICC_RUN	while(1), full mode Block Clock OFF	85	–	–	22	mA
			while(1), full mode Block Clock ON	85	–	–	35	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	22	mA
			CACHE ON	85	–	–	25	mA
		ICC_SLEEP	Full Module Clock OFF	85	–	–	17	mA
			Full Module Clock ON	85	–	–	30	mA
		ICC_RUN	while(1), full mode Block Clock OFF	105	–	–	25	mA

			while(1), full mode Block Clock ON	105	–	–	39	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	24	mA
			CACHE ON	105	–	–	29	mA
		ICC_SLEEP	Full Module Clock OFF	105	–	–	21	mA
			Full Module Clock ON	105	–	–	34	mA

1. Typ Voltage condition VCC=3.3V.
2. Max Voltage condition VCC=1.8~3.6V.

Table 3-9 High-Speed

para digm	Parameter	Symbol	prerequisite	Ta (°C)	Product Specification			Unit
					Min	Typ(1)	Max(2)	
High Speed Mode	fHCLK= 168MHz	ICC_RUN	while(1), full module Clock OFF	-40	–	13	–	mA
			while(1), full module Clock ON	-40	–	23	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	14	–	mA
			CACHE ON	-40	–	15	–	mA
		ICC_SLEEP	Full Module Clock OFF	-40	–	9	–	mA
			Full Module Clock ON	-40	–	19	–	mA
		ICC_RUN	while(1), full module Clock OFF	25	–	13	–	mA
			while(1), full module Clock ON	25	–	23	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	14	–	mA
			CACHE ON	25	–	15	–	mA
		ICC_SLEEP	Full Module Clock OFF	25	–	9	–	mA
			Full Module Clock ON	25	–	19	–	mA
		ICC_RUN	while(1), full module Clock OFF	85	–	–	18	mA
			while(1), full module Clock ON	85	–	–	28	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	18	mA
			CACHE ON	85	–	–	20	mA
		ICC_SLEEP	Full Module Clock OFF	85	–	–	14	mA
			Full Module Clock ON	85	–	–	24	mA
		ICC_RUN	while(1), full module Clock OFF	105	–	–	20	mA
			while(1), full module Clock ON	105	–	–	31	mA

Table 3-9 High-Speed Mode Current Consumption 1

		ICC_DHRYSTONE	CACHE OFF	105	–	–	19	mA
			CACHE ON	105	–	–	23	mA
		ICC_SLEEP	Full Module Clock OFF	105	–	–	17	mA
			Full Module Clock ON	105	–	–	27	mA

1. Typ Voltage condition VCC=3.3V.
2. Max Voltage condition VCC=1.8~3.6V.

Table 3-10 High-Speed

paradigm	Parameter	Symbol	prerequisite	Ta (°C)	Product Specification			Unit
					Min	Typ(1)	Max(2)	
High Speed Mode	fHCLK= 120MHz	ICC_RUN	while(1),full module Bell OFF	-40	–	9.5	–	mA
			while(1),full module Bell ON	-40	–	16.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	10	–	mA
			CACHE ON	-40	–	11.5	–	mA
		ICC_SLEEP	Full Module Clock OFF	-40	–	7	–	mA
			Full Module Clock ON	-40	–	14.5	–	mA
		ICC_RUN	while(1),full module Bell OFF	25	–	9.5	–	mA
			while(1),full module Bell ON	25	–	16.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	10	–	mA
			CACHE ON	25	–	11.5	–	mA
		ICC_SLEEP	Full Module Clock OFF	25	–	7	–	mA
			Full Module Clock ON	25	–	14.5	–	mA
		ICC_RUN	while(1),full module Bell OFF	85	–	–	14	mA
			while(1),full module Bell ON	85	–	–	22	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	14	mA
			CACHE ON	85	–	–	17	mA
		ICC_SLEEP	Full Module Clock OFF	85	–	–	12	mA
			Full Module Clock ON	85	–	–	20	mA
		ICC_RUN	while(1),full module Bell OFF	105	–	–	16	mA
			while(1),full module Bell ON	105	–	–	25	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	15	mA
			CACHE ON	105	–	–	19	mA
		ICC_SLEEP	Full Module Clock OFF	105	–	–	15	mA
			Full Module Clock ON	105	–	–	22	mA

1. Typ Voltage condition VCC=3.3V.
2. Max Voltage condition VCC=1.8~3.6V.

Table 3-11 High-Speed

paradigm	Parameter	Symbol	conditional	Ta (°C)	Product Specification			Unit
					Min	Typ(1)	Max(2)	
High Speed Mode	fHCLK= 24MHz	ICC_RUN	while(1), full module Clock OFF	-40	–	3	–	mA
			while(1), full module Clock ON	-40	–	6	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	3.5	–	mA
		ICC_SLEEP	Full Module Clock OFF	-40	–	2	–	mA
			Full Module Clock ON	-40	–	5.5	–	mA
		ICC_RUN	while(1), full module Clock OFF	25	–	3	–	mA
			while(1), full module Clock ON	25	–	6	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	3.5	–	mA
		ICC_SLEEP	Full Module Clock OFF	25	–	2	–	mA
			Full Module Clock ON	25	–	5.5	–	mA
		ICC_RUN	while(1), full module Clock OFF	85	–	–	8	mA
			while(1), full module Clock ON	85	–	–	12	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	7	mA
		ICC_SLEEP	Full Module Clock OFF	85	–	–	8	mA
			Full Module Clock ON	85	–	–	11	mA
		ICC_RUN	while(1), full module Clock OFF	105	–	–	10	mA
			while(1), full module Clock ON	105	–	–	14	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	8	mA
		ICC_SLEEP	Full Module Clock OFF	105	–	–	10	mA

			Full Module Clock ON	105	–	–	14	mA

Table 3-11 High-Speed Mode Current Consumption 3

1. Typ Voltage condition VCC=3.3V.
2. Max Voltage condition VCC=1.8~3.6V.

Table 3-12 Ultra Low Speed

paradigm	Parameter	Symbol	conditional	Ta (°C)	Product Specification			Unit
					Min	Typ(1)	Max(2)	
Ultra Low Speed Mode	fHCLK= 8MHz	ICC_RUN	while(1),All Module clock OFF	-40	–	1	–	mA
			while(1),All Module Clock ON	-40	–	3.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	1.5	–	mA
		ICC_SLEEP	Full Module Clock OFF	-40	–	1.2	–	mA
			Full Module Clock ON	-40	–	3.2	–	mA
		ICC_RUN	while(1), all Module clock OFF	25	–	1	–	mA
			while(1), all Module clock ON	25	–	3.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	1.5	–	mA
		ICC_SLEEP	Full Module Clock OFF	25	–	1.2	–	mA
			Full Module Clock ON	25	–	3.2	–	mA
		ICC_RUN	while(1), all Module clock OFF	85	–	–	4	mA
			while(1), all Module clock ON	85	–	–	6	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	4	mA
		ICC_SLEEP	Full Module Clock OFF	85	–	–	3.5	mA
			Full Module Clock ON	85	–	–	6	mA
		ICC_RUN	while(1),All Module clock OFF	105	–	–	6	mA
			while(1),All Module clock ON	105	–	–	7	mA
		ICC_DHRYSTONE	CACHE OFF	105	–	–	4.5	mA
		ICC_SLEEP	Full Module Clock OFF	105	–	–	4	mA
			Full Module Clock ON	105	–	–	6.5	mA

1. Typ Voltage condition: VCC=3.3V.
2. Max Voltage condition: VCC=1.8~3.6V.

Table 3-12 Ultra Low Speed Mode Current Consumption 1

Table 3-13 Ultra Low Speed

paradigm	Parameter	Symbol	conditional	Ta (°C)	Product Specification			Unit
					Min	Typ(1)	Max(2)	
Ultra Low Speed Mode	fHCLK= 1MHz	ICC_RUN	while(1), full mode Block Clock OFF	-40	–	0.7	–	mA
			while(1), full mode Block Clock ON	-40	–	2.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	-40	–	0.9	–	mA
		ICC_SLEEP	Full Module Clock OFF	-40	–	0.9	–	mA
			Full Module Clock ON	-40	–	2.4	–	mA
		ICC_RUN	while(1), full mode Block Clock OFF	25	–	0.7	–	mA
			while(1), full mode Block Clock ON	25	–	2.5	–	mA
		ICC_DHRYSTONE	CACHE OFF	25	–	0.9	–	mA
		ICC_SLEEP	Full Module Clock OFF	25	–	0.9	–	mA
			Full Module Clock ON	25	–	2.4	–	mA
		ICC_RUN	while(1), full mode Block Clock OFF	85	–	–	4	mA
			while(1), full mode Block Clock ON	85	–	–	5	mA
		ICC_DHRYSTONE	CACHE OFF	85	–	–	3.5	mA
		ICC_SLEEP	Full Module Clock OFF	85	–	–	3.5	mA
			Full Module Clock ON	85	–	–	5	mA
		ICC_RUN	while(1), full mode Block Clock OFF	105	–	–	5	mA
			while(1), full mode Block Clock ON	105	–	–	5.5	mA

Table 3-13 Ultra Low Speed Mode Current Consumption 2

		ICC_DHRYSTONE	CACHE OFF	105	–	–	4	mA
		ICC_SLEEP	Full Module Clock OFF	105	–	–	5	mA
			Full Module Clock ON	105	–	–	5.5	mA

1. Typ Voltage condition VCC=3.3V.
2. Max Voltage condition VCC=1.8~3.6V.

Table 3-14 Low Power

mold style	Parameter	Symbol	Conditions (VCC=3.3V)	Ta (°C)	Product Specification			Unit
					Min	Typ(1)	Max(2)	
Stop Mode	–	ICC_STP	PWC_PWRC1.STPDAS=00	-40	–	160	–	uA
			PWC_PWRC1.STPDAS=11	-40	–	30	–	uA
			PWC_PWRC1.STPDAS=00	25	–	220	–	uA
			PWC_PWRC1.STPDAS=11	25	–	80	–	uA
			PWC_PWRC1.STPDAS=00	85	–	–	3600	uA
			PWC_PWRC1.STPDAS=11	85	–	–	3400	uA
			PWC_PWRC1.STPDAS=00	105	–	–	4800	uA
			pwc_pwrc1.stpdas=11(3)	105	–	–	4600	uA
power-down mode	–	ICC_PD	Power down mode 1	-40	–	10	–	uA
			Power-down mode 2	-40	–	4	–	uA
			Power-down mode 3	-40	–	1.8	–	uA
			Power-down mode 4	-40	–	1.8	–	uA
			Power-down mode 2 + XTAL32 + RTC	-40	–	6	–	uA
			Power-down mode 2 + LRC + RTC	-40	–	9	–	uA
			Power down mode 1	25	–	10	–	uA
			Power-down mode 2	25	–	4	–	uA
			Power-down mode 3	25	–	1.8	–	uA
			Power-down mode 4	25	–	1.8	–	uA
			Power-down mode 2 + XTAL32 + RTC	25	–	6	–	uA
			Power-down mode 2 + LRC + RTC	25	–	9	–	uA
			Power down mode 1	85	–	–	21	uA
			Power-down mode 2	85	–	–	19	uA
			Power-down mode 3	85	–	–	19	uA
			Power-down mode 4	85	–	–	19	uA
			Power-down mode 2 + XTAL32 + RTC	85	–	–	21	uA
			Power-down mode 2 + LRC + RTC	85	–	–	21	uA
			Power down mode 1	105	–	–	35	uA
			Power-down mode 2	105	–	–	33	uA
			Power-down mode 3	105	–	–	30	uA
			Power-down mode 4 [3]	105	–	–	30	uA
			Power-down mode 2 + XTAL32	105	–	–	35	uA

			+ RTC					
			Power down mode 2 + LRC + RTC	105	–	–	35	uA

Table 3-14 Low Power Mode Current Consumption

1. Typ Voltage condition VCC=3.3V.
2. Max Voltage condition VCC=1.8~3.6V.
3. Mass production testing guaranteed.

Table 3-15 Analog Module Current Consumption

Item	Parameter	Symbol	Conditions (VCC=AVCC=3.3V)	Ta (°C)	Product Specification			Unit
					Min	Typ	Max.	
Module Current	–	ICC_MODULE	XTAL oscillation mode large drive 24MHz	25	–	1.8	–	mA
			Driving 16MHz in oscillation mode	25	–	1	–	mA
			Oscillation mode small drive 10MHz	25	–	0.8	–	mA
			Oscillation mode ultra-small drive 8MHz	25	–	0.6	–	mA
			XTAL 32K	25	–	0.5	–	mA
			HRC	25	–	0.35	–	mA
			PLL (@480MHz)	25	–	2.3	–	mA
			PLL (@240MHz)	25	–	1.4	–	mA
			ADC	25	–	1.2	–	mA
			DAC	25	–	70	–	uA
			CMP	25	–	0.11	–	mA
			PGA	25	–	1	–	mA
			USBFS(1)	25	–	6	–	mA

1. Contains the current when the control section communicates with the USBPHY.

3.3.5 Electrical sensitivity

Different tests (ESD, LU) are performed on the chip using specific measurement methods to determine its performance in terms of electrical sensitivity.

3.3.5.1 Electrostatic Discharge (ESD)

An electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with the JESD22-A114/C101 standard.

Table 3-16 ESD Characteristics

notation	parameters	conditional	maximum values	unit (of measure)
$V_{ESD (HBM)}$	Electrostatic discharge voltage (human model)	T_A = +25 °C according to JESD22-A114	4000	V
$V_{ESD (CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A = +25 °C, JESD22-C101 compliant	1000	

3.3.5.2 Static Latch-up

To evaluate static Latch-up performance, two complementary static Latch-up tests are performed on the chip:

- Apply overvoltage to each power and analog input pin
- Apply current injection to other input, output,

and configurable I/O pins These tests comply with the EIA/JESD 78A IC Latch-up standard.

Table 3-17 Static Latch-up Characteristics

notation	parameters	prerequisite	maximum values	unit (of measure)
LU	Static Latch-up	T_A = +105 °C, JESD78A compliant	200	mA

3.3.6 Low Power Mode Wakeup Timing

Wake-up time is measured from the time the wake-up event is triggered to the first instruction executed by the CPU:

- For stop or sleep mode: the wake-up event is WFE.
- The WKUP pin is used to wake up from standby, stop, and sleep modes. All timings are tested at ambient temperature and VCC=3.3V.

Table 3-18 Low Power Mode Wake-Up Time

notation	parameters	conditional	typical value	maximum values	unit (of measure)
T_{STOP1}	Wake up from stop mode	PWC_PWRC1.VHRCSD=1 and PWC_PWRC1.VPLLSD=1,the system clock is MRC, the program is in the Execution on RAM	2	5	μs
T_{STOP2}	Wake up from stop mode	The system clock is MRC and the program is executed on Flash	8	15	
T_{PD1}(1)	Wake up from power-down mode 1	VCAP_1/VCAP_2 total capacity of 0.094uF or 0.1uF	15	25	
		VCAP_1/VCAP_2 total capacity of 0.2uF or 0.22uF	20	30	
T_{PD2}(1)	Wake up from power-down mode 2	VCAP_1/VCAP_2 total capacity of 0.094uF or 0.1uF	40	50	
		VCAP_1/VCAP_2 total capacity of 0.2uF or 0.22uF	45	55	
T_{PD3}(1)	Wake up from power-down mode 3	VCAP_1/VCAP_2 total capacity of 0.094uF or 0.1uF	2500	3000	
		VCAP_1/VCAP_2 total capacity of 0.2uF or 0.22uF	2500	3000	
T_{PD4}(1)	Wake up from power-down mode 4	VCAP_1/VCAP_2 total capacity of 0.094uF or 0.1uF	65	75	
		VCAP_1/VCAP_2 total capacity of 0.2uF or 0.22uF	70	80	

1. The total capacity of VCAP_1/VCAP_2 must match the value assigned to the PWC_PWRC3.PDTS bit. If the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, make sure the PWC_PWRC3.PDTS bit is cleared to zero before entering power-down mode.If the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, make sure the PWC_PWRC3.PDTS bit is set to 0.094uF or 0.1uF before entering power-down mode.

3.3.7 I/O Port Characteristics

General Input/Output Characteristics

Table 3-19 I/O Static Characteristics

notation	parameters		prerequisite	minimum value	typical value	maximum values	unit (of measure)
V_{IL}(1)	Schmitt input low		1.8≤VCC≤3.6	–	–	0.2_{VCC}	V
V_{IH} (1)	Schmitt input high		1.8≤VCC≤3.6	0.8_{VCC}	–	–	V
V_{HYS}	Schmitt input hysteresis		1.8≤VCC≤3.6	–	0.2	–	V
V_{IL}	CMOS input low level(3)		1.8≤VCC≤3.6	–	–	0.3_{VCC}	V
V_{IH}	CMOS input high(3)		1.8≤VCC≤3.6	0.7_{VCC}	–	–	V
I_{LKG}(1)	I/O Input Leakage Current		$V_{SS}≤V_{IN}≤V_{CC}$	-1	–	1	uA
			V_{IN} = 5.5V(2)	–	–	5	uA
R_{PU}(1)(2)	Weak pull-up equivalent resistance	usbfs_dp, usbfs_dm	–	–	1.5	–	KΩ
		In addition to the USBFS_DP and Other input pins of USBFS_DM	V_{IN} = V_{SS}	–	30	–	KΩ
C_{IO}	I/O Pin Capacitance	PA11/USBFS_DM PA12/USBFS_DP	–	–	10	–	pF
		In addition to PA11/USBFS_DM and PA12/USBFS_DP, the other outputs are inlet pin	–	–	5	–	pF

1. Mass production testing guaranteed.
2. To keep the voltage above VCC+0.3 V, the internal pull-up/down resistors must be disabled.
3. The input type of the pin is CMOS when MOSI/MISO/SCK/NSS0 function of SPI is selected, or SDA/SCL of I2C and SMbus mode is selected, and the input type of the pin is Schmitt when other functions are selected.

output voltage

Table 3-20 Output Voltage Characteristics

Driver settings	notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
low drive	V_{OL}(1)(2)	Low Level Output	IIO=±1.5mA, 1.8≤VCC<2.7	–	–	0.4	V
	V_{OH}(1)(3)	High Level Output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low Level Output	IIO=±3mA, 2.7≤VCC≤3.6	–	–	0.4	
	V_{OH}(1)(3)	High Level Output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low Level Output	IIO=±6mA, 2.7≤VCC≤3.6	–	–	1.3	
	V_{OH}(1)(3)	High Level Output		VCC-1.3	–	–	
medium driver	V_{OL}(1)(2)	Low Level Output	IIO=±3mA, 1.8≤VCC<2.7	–	–	0.4	
	V_{OH}(1)(3)	High Level Output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low Level Output	IIO=±5mA, 2.7≤VCC≤3.6	–	–	0.4	
	V_{OH}(1)(3)	High Level Output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low Level Output	IIO=±12mA, 2.7≤VCC≤3.6	–	–	1.3	
	V_{OH}(1)(3)	High Level Output		VCC-1.3	–	–	
high drive	V_{OL}(1)(2)	Low Level Output	IIO=±6mA, 1.8≤VCC<2.7	–	–	0.4	
	V_{OH}(1)(3)	High Level Output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low Level Output	IIO=±8mA, 2.7≤VCC≤3.6	–	–	0.4	
	V_{OH}(1)(3)	High Level Output		VCC-0.4	–	–	
	V_{OL}(1)(2)	Low Level Output	IIO=±20mA, 2.7 ≤VCC≤3.6	–	–	1.3	
	V_{OH}(1)(3)	High Level Output		VCC-1.3	–	–	

1. Mass production testing guaranteed.
2. The I_{IO} sink current of the device must always take into account the absolute

maximum ratings specified in Table 3-3. the sum of the I_{IOs} (I/O ports and control pins) must not exceed I_{VSS}.

3. The I_{IO} pull current of the device must always follow the absolute maximum ratings listed in Table 3-3, and the sum of the I_{IOs} (I/O ports and control pins) must not exceed I_{VCC}.

Input/Output AC Characteristics

Table 3-21 I/O AC Characteristics

Driver settings	notation	parameters	Conditions (3)	minimum value	typical value	maximum values	unit (of measure)
low drive	$f_{max}(IO)out$	Maximum frequency(1)	CL=30 pF, VCC≥ 2.7V	–	–	20	MHz
			CL=30 pF, VCC≥1.8V	–	–	10	
			CL=10pF, VCC≥2.7V	–	–	40	
			CL=10pF, VCC≥1.8V	–	–	20	
	$t_f(IO)out$ $t_r(IO)out$	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	–	–	15	ns
			CL=30 pF, VCC≥1.8V	–	–	25	
			CL=10pF, VCC≥2.7V	–	–	7.5	
			CL=10pF, VCC≥1.8V	–	–	15	
medium driver	$f_{max}(IO)out$	Maximum frequency(1)	CL=30 pF, VCC≥ 2.7V	–	–	45	MHz
			CL=30 pF, VCC≥1.8V	–	–	22.5	
			CL=10pF, VCC≥2.7V	–	–	90	
			CL=10pF, VCC≥1.8V	–	–	45	
	$t_f(IO)out$ $t_r(IO)out$	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	–	–	7.5	ns
			CL=30 pF, VCC≥1.8V	–	–	12	
			CL=10pF, VCC≥2.7V	–	–	4	
			CL=10pF, VCC≥1.8V	–	–	7.5	
high drive	$f_{max}(IO)out$	Maximum frequency (1)	CL=30 pF, VCC≥2.7V	–	–	100	MHz
			CL=30 pF, VCC≥1.8V	–	–	50	
			CL=10pF, VCC≥2.7V	–	–	180	
			CL=10pF, VCC≥1.8V	–	–	100	
	$t_f(IO)out$ $t_r(IO)out$	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	–	–	4	ns
			CL=30 pF, VCC≥1.8V	–	–	6	
			CL=10pF, VCC≥2.7V	–	–	2.5	
			CL=10pF, VCC≥1.8V	–	–	4	

1. The maximum frequency is defined in Figure 3-6.
2. Load capacitance C_L The capacitance of the PCB and MCU pins must be taken into account (the capacitance of the pins to the board can be roughly estimated at 10pF)

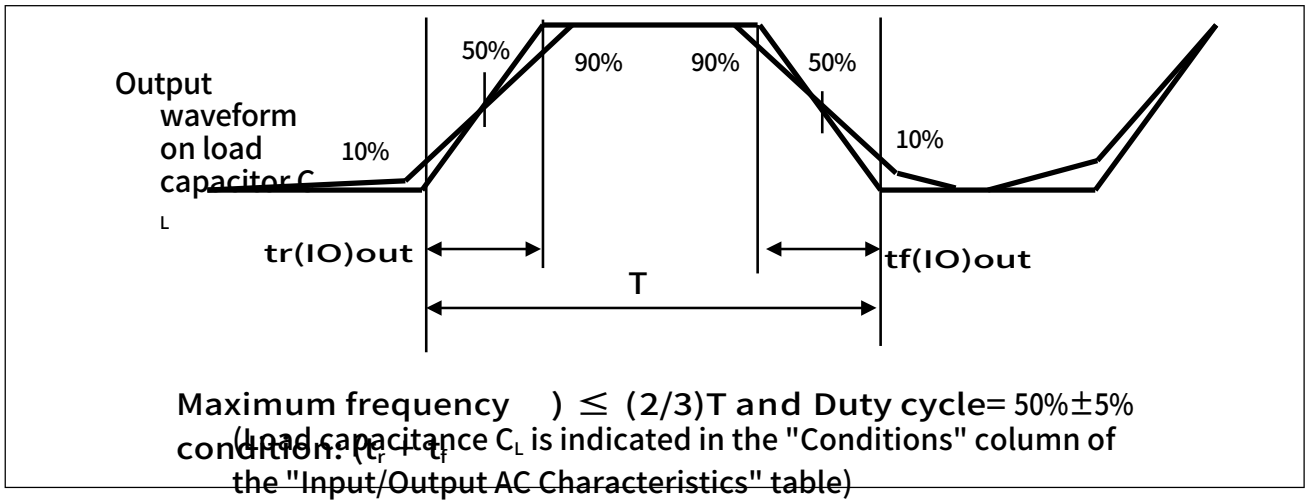


Figure 3-6 I/O AC Characteristics Definition

3.3.8 USART

Interface Features

Table 3-22 USART AC Timing

notation	parameters		minimum value	maximum values	unit (of measure)
tcyc	Number of input clock cycles	UART	4	–	tPCLK1
		CSI	6	–	
tCKw	Input Clock Width		0.4	0.6	tScyc
tCKr	Input clock rise time		–	5	ns
tCKf	Input clock fall time		–	5	ns
tTD	Transmission delay time	CSI	–	28	ns
tRDS	Receive data setup time	CSI	15	–	ns
tRDH	Receive Data Hold Time	CSI	5	–	ns

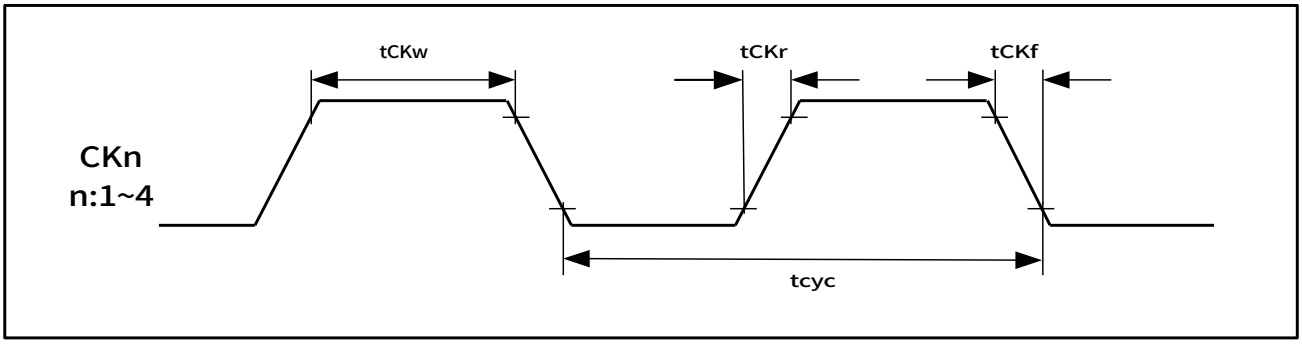


Figure 3-7 USART Clock Timing

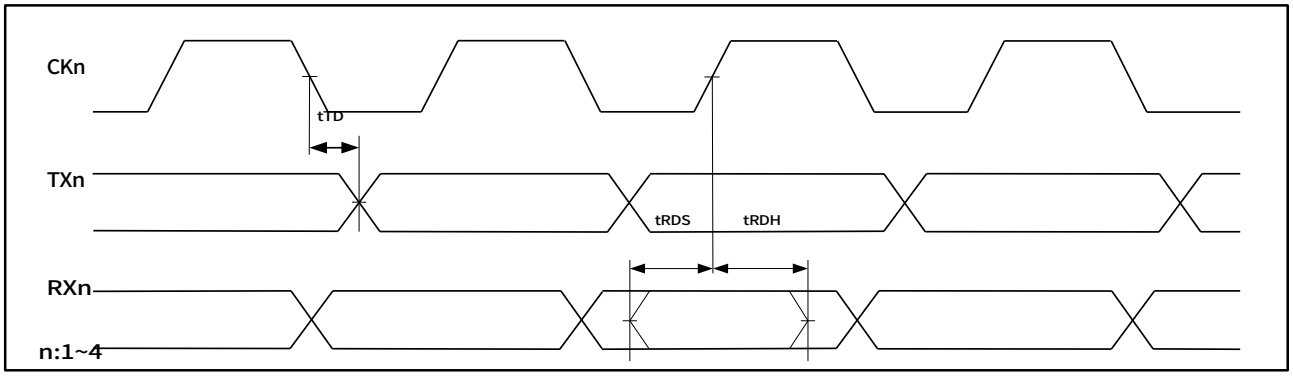


Figure 3-8 USART (CSI) Input/Output Timing

3.3.9 I2S Interface Features

Table 3-23 I2S Electrical Characteristics

notation	Performance indicators	prerequisite	Min	Max.	Unit
f_{MCK}	I2S main clock output	–	256*8K	256*Fs	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	20	64*Fs	MHz
		Slave data: 32 bits	–	64*Fs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
t_{v}(WS)	WS valid time	Master mode	0	–	ns
t_{h}(WS)	WS hold time	Master mode	0	–	
t_{su}(WS)	WS setup time	Slave mode	1	–	
t_{h}(WS)	WS hold time	Slave mode	0	–	
t_{su}(SD_MR)	Data input setup time	Master receiver	7.5	–	
t_{su}(SD_SR)		Slave receiver	2	–	
t_{h}(SD_MR)	Data input hold time	Master receiver	0	–	
t_{h}(SD_SR)		Slave receiver	0	–	
t_{v}(SD_ST) t_{h}(SD_ST)	Data output valid time	Slave transmitter(after enable edge)	–	27	
t_{v}(SD_MT)		Master transmitter(after enable edge)	–	20	
t_{h}(SD_MT)	Data output hold time	Master transmitter(after enable edge)	2.5	–	

1. Fs: I2S sampling frequency.

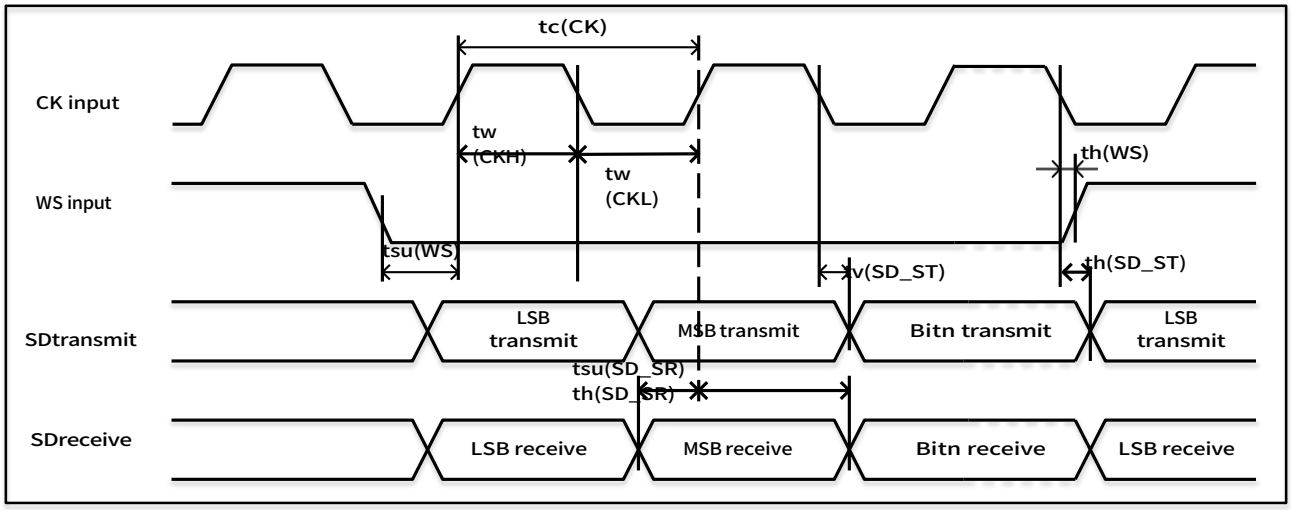


Figure 3-9 I2S Slave Mode Timing (Philips Protocol)

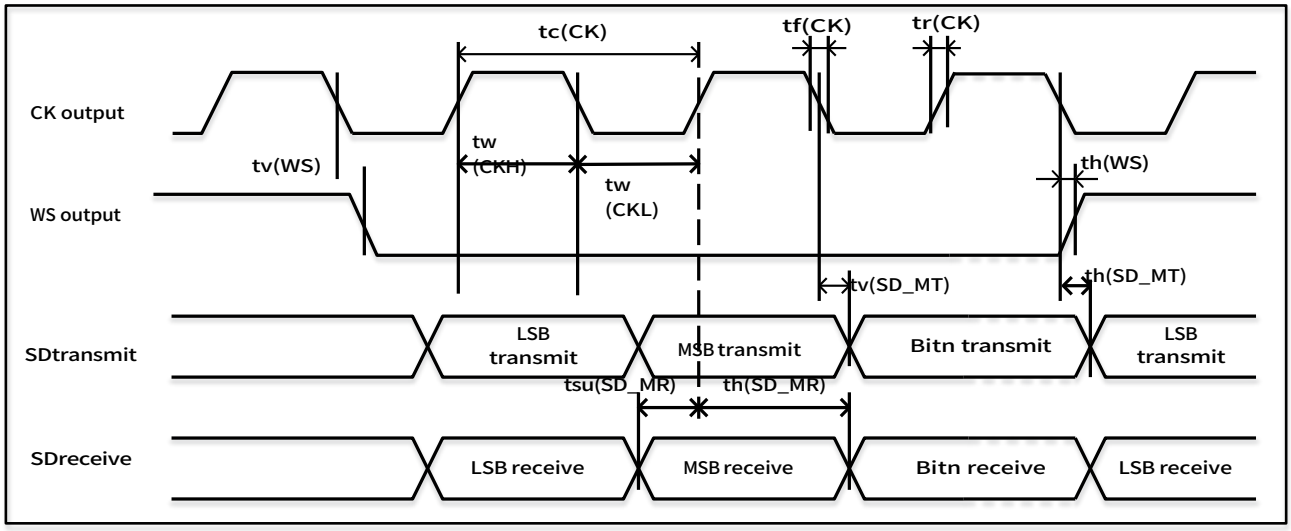


Figure 3-10 I2S Master Mode Timing (Philips Protocol)

3.3.10 I2C Interface Features

Table 3-24 I2C Electrical Characteristics

notation	parameters	Standard Model (SM)		Fast Mode (FM)		unit (of measure)
		Min	Max.	Min	Max.	
fSCL	SCL frequency	0	100	0	400	KHz
tHD;STA	Start condition/restart condition Hold	4.0	–	0.6	–	μs
tLOW	SCL low	4.7	–	1.3	–	μs
tHIGH	SCL high	4	–	0.6	–	μs
tSU;STA	Restart condition Setup	4.7	–	0.6	–	μs
tHD;DAT	Data Hold	0	–	0	–	μs
tSU;DAT	Data Setup	30+ tI2C Reference Clock Cycle	–	30+ tI2C Reference Clock Cycle	–	ns
tR	SCL/SDA rise time	–	1000	–	300	ns
tF	SCL/SDA fall time	–	300	–	300	ns
tSU;STO	Stop condition Setup	4	–	0.6	–	μs
tBUF	BUS idle between stop condition and start condition timing	4.7	–	1.3	–	μs
Cb	load capacitance	–	400	–	400	pF

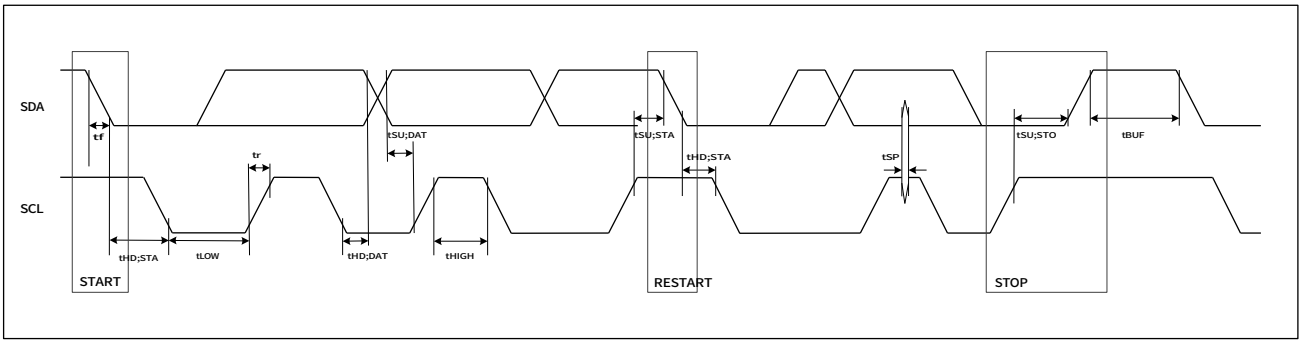


Figure 3-11 I2C Bus Timing Definitions

3.3.11 SPI Interface Features

Table 3-25 SPI Electrical Characteristics

Item		Symbol	Min	Max.	Unit	Test conditions
SCK clock cycle	Master	tspcyc	2 (pclk ≤ 60MHz) 4 (pclk ≤ 60MHz)	4096	tpcyc	Figure 3-12 C=30pF
	Slave		6	4096		
SCK clock rise and fall time	Master	tsckr	–	5	ns	
	Slave	tsckf	–	1	µs	
Data input setup time	Master	tsu	4	–	ns	Figure 3-13 /14/15 C=30pF
	Slave		5	–		
Data input hold time	Master	th	tpcyc	–	ns	
	Slave		20	–		
Data output delay	Master	tod	–	8	ns	
	Slave		–	20		
Data output hold time	Master	toh	0	–	ns	
	Slave		0	–		
MOSI/MISO rise and fall time	Master	tdr	–	5	ns	
	Slave	tdf	–	1	µs	
SS rise and fall time	Master	tssr	–	5	ns	
	Slave	tssf	–	1	µs	

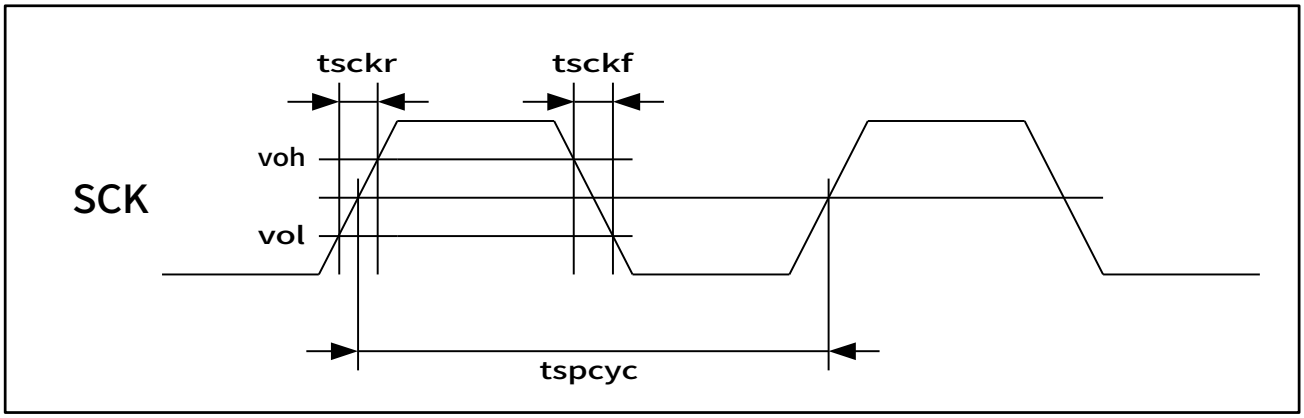


Figure 3-12 SCK Clock Definition

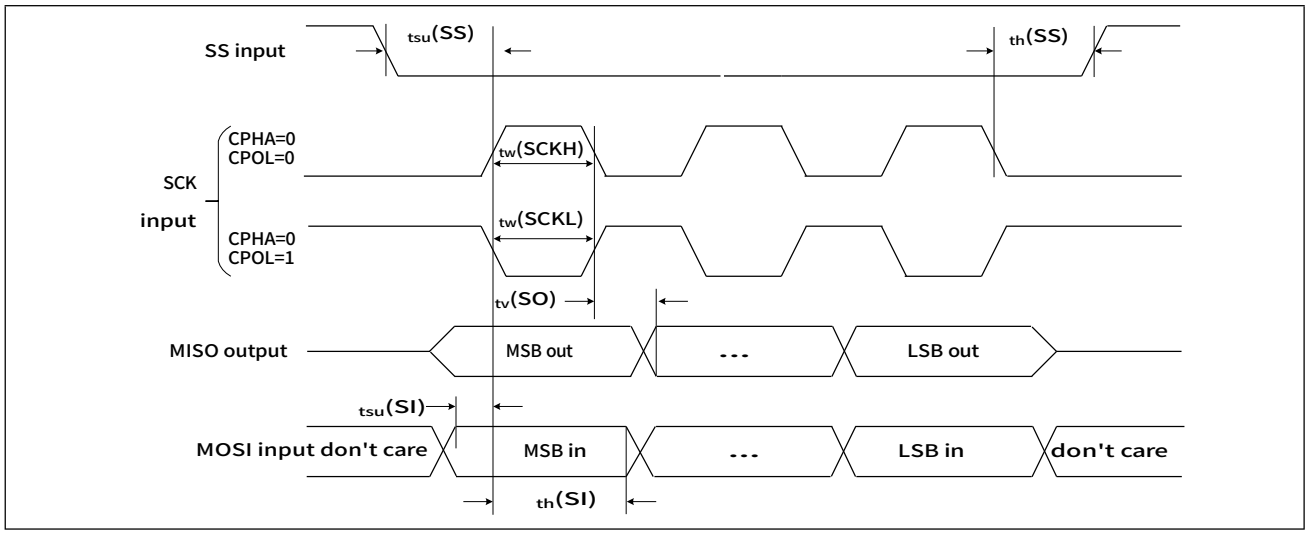


Figure 3-13 SPI timing diagram -slave mode and CPHA=0

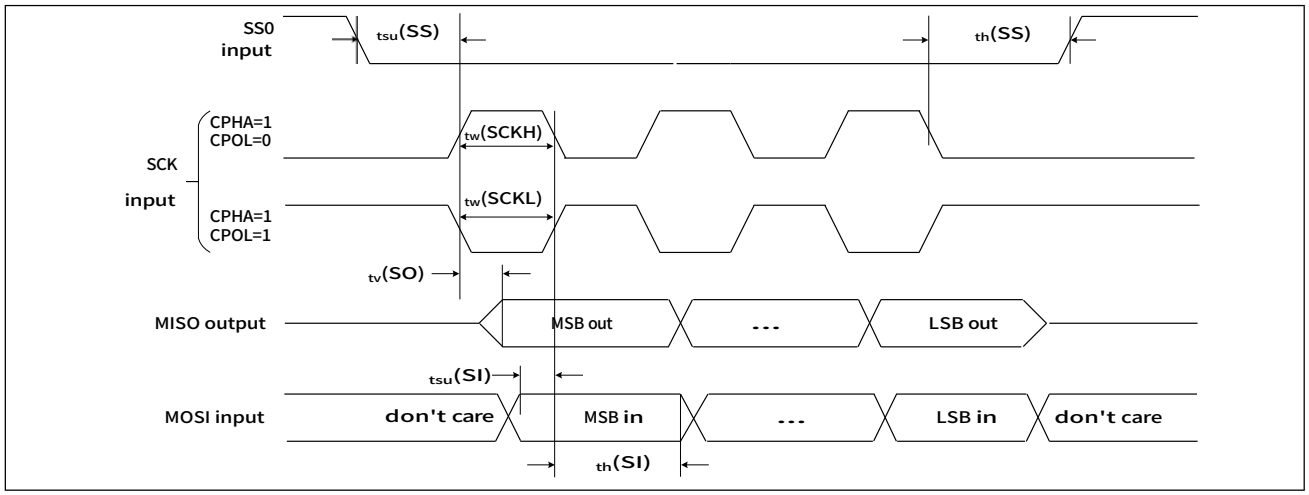


Figure 3-14 SPI timing diagram -slave mode and CPHA=1

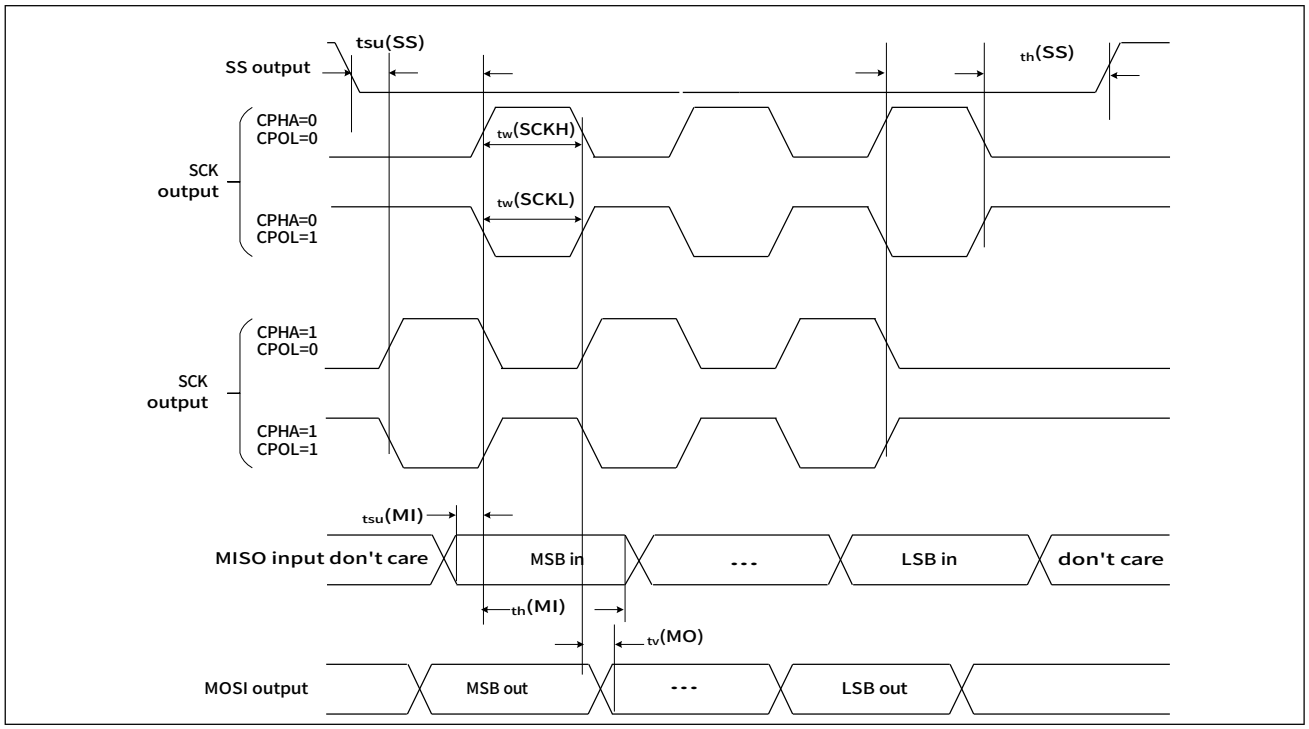


Figure 3-15 SPI timing diagram -master mode

3.3.12 CAN2.0B Interface Features

For the port characteristics of CANx_TX a n d CANx_RX, refer to [I/O Port Characteristics]

3.3.13 USB Interface Features

Table 3-26 USB Full-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
import ation	V_{CC}	operating voltage	–	3.0(2)	–	3.6	V
	V_{IL}	Input Low Level	–	–	–	0.8	V
	V_{IH}	Input High Level	–	2.0	–	–	V
	V_{DI}	Differential Input Sensitivity	–	0.2	–	–	V
	V_{CM}	Differential Common Mode Voltage	–	0.8	–	2.5	V
expor ts	V_{OL}(3)	Static output low level	RL=1.5kΩ to 3.6V(4)	–	–	0.3	V
	V_{OH}(3)	Static Output High	RL=15kΩ to VSS(4)	2.8	–	3.6	V
	V_{CRS}	Cross-over voltage	CL=50pF	1.3	–	2.0	V
	t_R	rising time	CL=50pF. 10%~90% of |VOH-VOL|	4	–	20	ns
	t_F	descent time	CL=50pF. 10%~90% of |VOH-VOL|	4	–	20	ns
	tRFMA	Rise-fall time ratio tR/tF	CL=50pF	90	–	111.1	%
R_{PD}(3)		pull-down resistor	VIN= V_{CC}, in host mode	–	15	–	kΩ
R_{PU}(3)		pull-up resistor	VIN= V_{SS}, idle state	0.900	1.2	1.575	kΩ
			VIN= V_{SS}. in device mode	1.425	2.3	3.090	kΩ

1. All voltages were measured based on local ground potentials.
2. USB Full Speed transceiver functionality is still guaranteed when the operating voltage drops to 2.7V, but full USB Full Speed electrical characteristics are not guaranteed, the latter being degraded over the V_{CC} voltage range of 2.7 to 3.0V.
3. Mass production testing guaranteed.
4. R_L is the load connected to the USB full-speed drive.

Table 3-27 USB Low-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
import ation	V_{CC}	operating voltage	–	3.0(2)	–	3.6	V
	V_{IL}	Input Low Level	–	–	–	0.8	V
	V_{IH}	Input High Level	–	2.0	–	–	V
	V_{DI}	Differential Input Sensitivity	–	0.2	–	–	V
	V_{CM}	Differential Common Mode Voltage	–	0.8	–	2.5	V
exports	V_{OL}(3)	Static output low level	RL=1.5kΩ to 3.6V(4)	–	–	0.3	V
	V_{OH}(3)	Static Output High	RL=15kΩ to VSS(4)	2.8	–	3.6	V
	V_{CRS}(3)	Cross-over voltage	CL=200pF~600pF	1.3	–	2.0	V
	t_R(3)	rising time	CL=200pF~600pF. 10%~90% of |VOH-VOL|	75	–	300	ns
	t_F(3)	descent time	CL=200pF~600pF. 10%~90% of |VOH-VOL|	75	–	300	ns
	t_{RFMA}(3)	Rise-fall time ratio $t_{R/tF}$	CL=200pF~600pF	80	–	125	%
R_{PD}(3)		pull-down resistor	VIN= V_{CC}, in host mode	14.25	–	24.80	kΩ

1. All voltages were measured based on local ground potentials.
2. A drop in operating voltage to 2.7V still guarantees USB low-speed transceiver functionality, but does not guarantee full USB low-speed electrical characteristics, which degrade over the 2.7 to 3.0V V_{CC} voltage range.
3. Mass production testing guaranteed.
4. R_L is the load connected to the USB low speed drive.

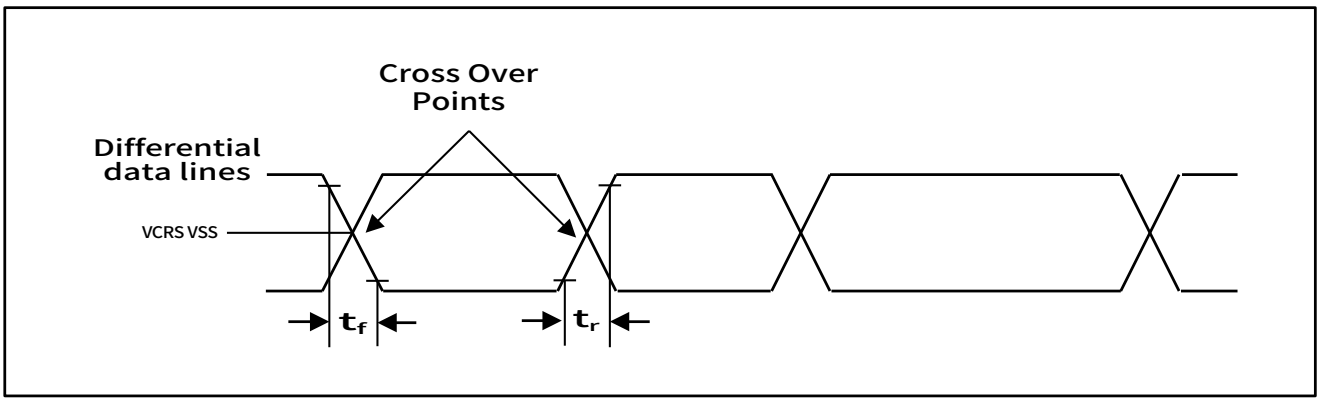


Figure 3-16 USB Rise/Fall Time and Cross Over Voltage Definition

3.3.14 PLL Characterization

Table 3-28 PLL Main Performance Indicators

notation	parameters	conditional	Min	Typ	Max.	Unit
fPLL_IN	PLL PFD (Phase Frequency Detector) input clock(1)	–	1	–	25	MHz
fPLL_OUT	PLL multiplier output clock	–	15	–	240	MHz
fVCO_OUT	PLL VCO output	–	240	–	480	MHz
JitterPLL	Period Jitter	PLL PFD input clock=8MHz. System clock=120MHz. Peak-to-Peak	–	±100	–	ps
	Cycle-to-Cycle Jitter	PLL PFD input clock=8MHz. System clock=120MHz. Peak-to-Peak	–	±150	–	
tLOCK	PLL lock time	–	–	80	120	μs

1. It is recommended to use a higher input clock to obtain good Jitter characteristics.

3.3.15 JTAG Interface Features

Table 3-29 JTAG Interface Characteristics

Synbol	Item	Min	Typ	Max.	Unit
tTCKcyc	JTCK clock cycle time	50	–	–	ns
tTCKH	JTCK clock high pulse width	20	–	–	ns
tTCKL	JTCK clock low pulse width	20	–	–	ns
tTCKr	JTCK clock rise time	–	–	5	ns
tTCKf	JTCK clock fall time	–	–	5	ns
tTMSs	JTMS setup time	8	–	–	ns
tTMSh	JTMS hold time	8	–	–	ns
tTDIs	JTDI setup time	8	–	–	ns
tTDIh	JTDI hold time	8	–	–	ns
tTDOd	JTDO data delay time	–	–	20	ns

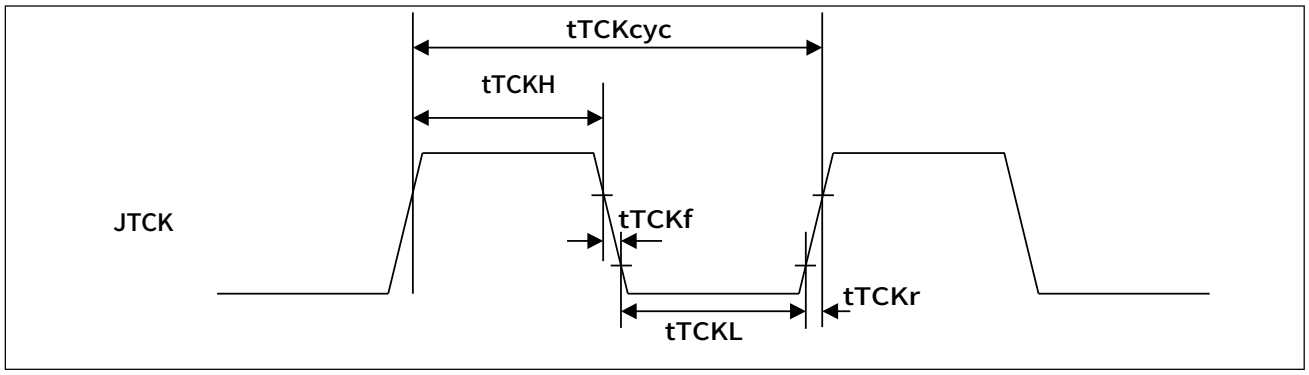


Figure 3-17 JTAG JTCK Clock

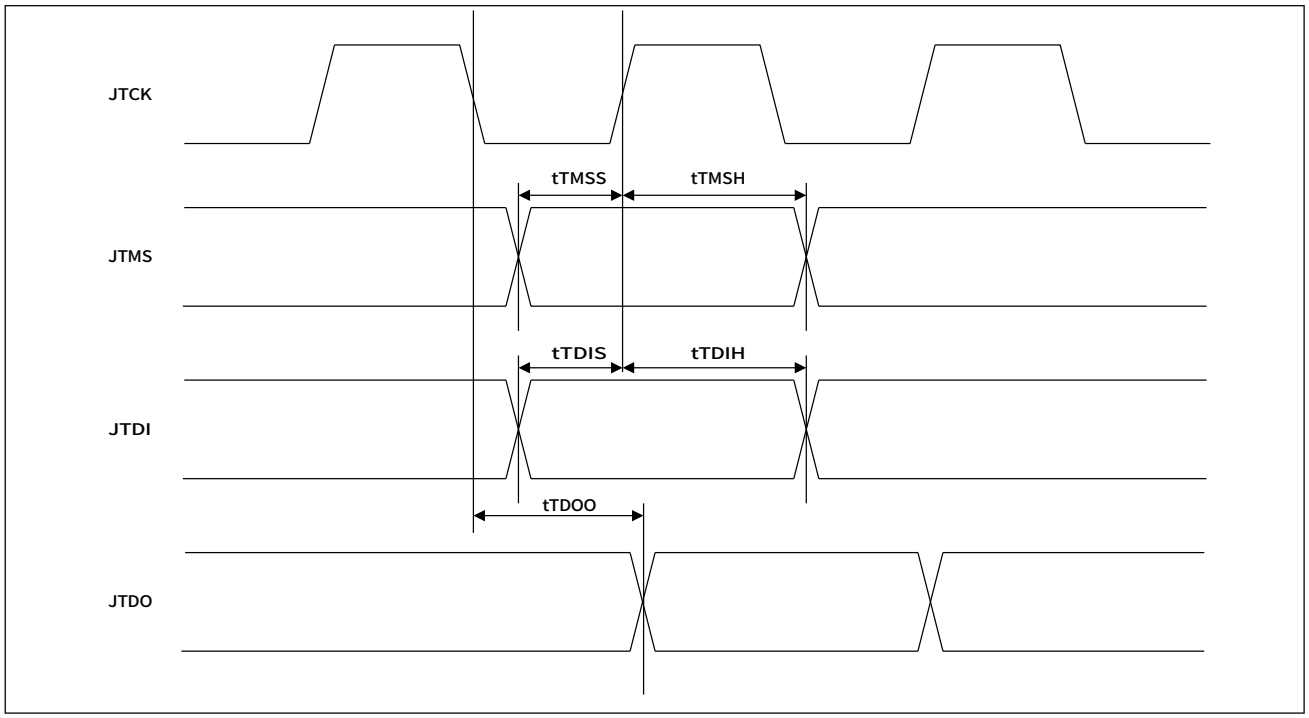


Figure 3-18 JTAG Inputs and Outputs

3.3.16 External Clock Source Characteristics

3.3.16.1 High-speed external user clock generated by an external source

In bypass mode, the XTAL oscillator is turned off and the input pins are standard I/O. The external clock signal must take into account the I/O static characteristics.

Table 3-30 High-Speed External User Clock Characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
f_{XTAL_EXT}	User External Clock Source Frequency	–	1	–	25	MHz
V_{IH_XTAL}	XTAL_EXT input pin high		$0.8*V_{CC}$	–	V_{CC}	V
V_{IL_XTAL}	XTAL_EXT input pin low		V_{SS}	–	$0.2*V_{CC}$	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_EXT Rise or fall time		–	–	5	ns
$Duty_{(XTAL)}$	duty cycle	–	40	–	60	%

3.3.16.2 Crystal / Ceramic Resonators Generate High Speed External Clocks

The high-speed external (XTAL) clock can be generated using a 4 to 25 MHz crystal/ceramic resonator oscillator. In the application, the resonator and load capacitance must be placed as close as possible to the oscillator pins to minimize output distortion and start-up stabilization time. For detailed information on resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-31 XTAL 4-25 MHz Oscillator Characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
f_{XTAL_IN}	oscillator frequency		4	–	25	MHz
R_F(1)	Feedback resistance		–	300	–	kΩ
A_{XTAL}(2)	XTAL Accuracy	–	-500	–	500	ppm
G_{mmax}	Oscillator G_m	vibration	4	–	–	mA/V
$t_{SU(XTAL)}$(3)	activation time	VCC stabilized, crystal = 8MHz	–	2.0	–	ms
		VCC stabilized, crystal = 4MHz	–	4.0	–	ms

1. Mass production testing guaranteed.
2. This parameter depends on the resonator used in the application.
3. $t_{SU(XTAL)}$ is the start-up time, measured from the time the software enables XTAL until a stable 8MHz oscillation frequency is obtained. This value is based on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use a high quality external ceramic capacitor designed specifically for high frequency applications that meets the requirements of a crystal or resonator (see the following figure). C_{L1} and C_{L2} are usually the same size. $C_{L1}=C_{L2}=2*(C_L-C_S)$. C_S is the PCB and MCU pin (XTAL_IN, XTAL_OUT) stray capacitance.

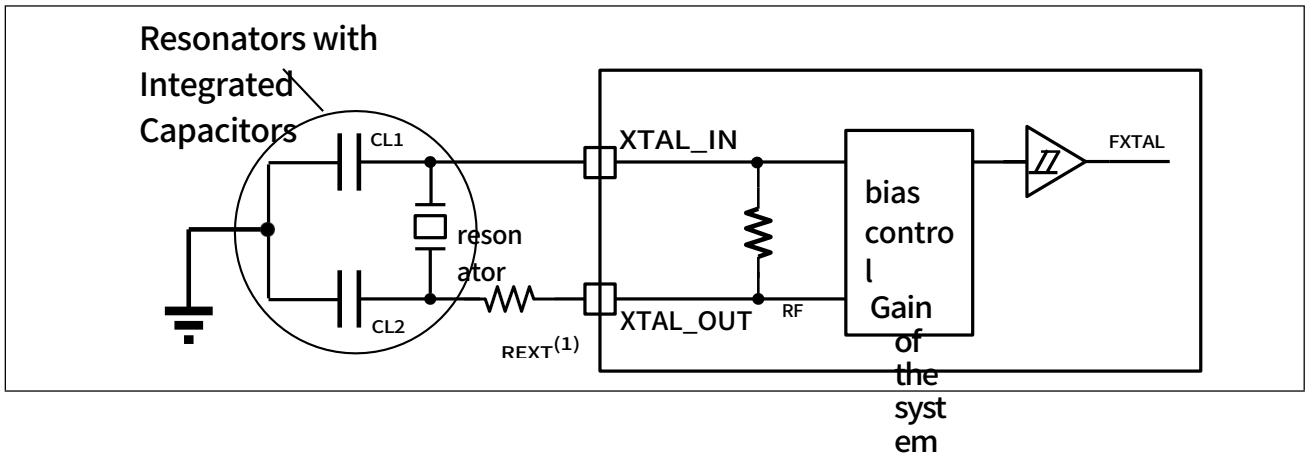


Figure 3-19 Typical Application with 8 MHz Crystals

1. The value of R_{EXT} depends on the crystal characteristics.

3.3.16.3 Crystal / Ceramic Resonator Generated Low Speed External Clocks

The low-speed external clock can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. In the application, the resonator and load capacitance must be placed as close as possible to the oscillator pins to minimize output distortion and start-up stabilization time. For detailed information on resonator characteristics (frequency, package, accuracy, etc.), consult the crystal resonator manufacturer.

Table 3-32 XTAL32 Oscillator Characteristics

notation	parameters	conditional	norm			unit (of measure)
			Min	Typ	Max.	
f_{XTAL32}	frequency	–	–	32.768	–	kHz
R_F(1)	Feedback resistance	–	–	15	–	MΩ
I_{DD_XTAL32}	power wastage	XTAL32DRV[2:0]=000	–	0.8	–	μA
A_{XTAL32}(2)	XTAL32 Accuracy	–	-500	–	500	ppm
G_{mmax}	Oscillator Gm	–	5.6	–	–	uA/V
$t_{SUXTAL32}$	Start-up time (3)	VCC steady state	–	2	–	s

1. Mass production testing guaranteed.
2. This parameter depends on the resonator used in the application.
3. $t_{SUXTAL32}$ is the time to oscillation, measured from the time the software enables XTAL32 until a stable 32.768 kHz oscillation frequency is obtained. This value is based on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high quality external ceramic capacitors (see figure below) C_{L1} and C_{L2} are usually the same size, CL1=CL2=2*(CL-Cs), Cs is the stray capacitance of the PCB and MCU pins (XTAL32_IN, XTAL32_OUT). If C_{L1} and C_{L2} are larger than 18pF, it is recommended to set the XTAL32DRV[2:0]=001 (for larger drivers, the typical value of power consumption increases by 0.2uA). If CL1 and CL2 are larger than 18pF, it is recommended to set XTAL32DRV[2:0]=001 (large driver, power consumption increases by 0.2uA typical)

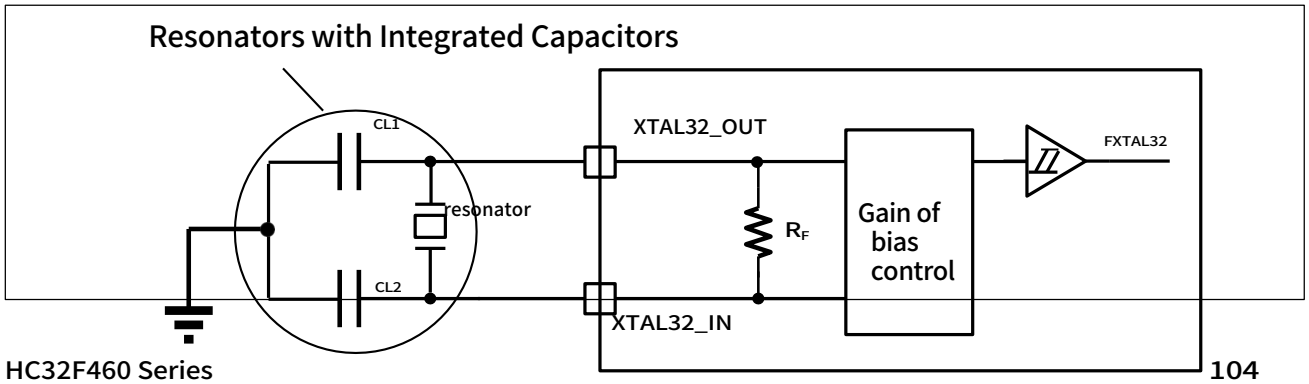


Figure 3-20 Typical Application with 32.768 kHz Crystals

3.3.17 Internal Clock Source Characteristics

Table 3-33 HRC Oscillator Characteristics

3.3.17.1 Internal High Speed (HRC) Oscillator

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
fHRC	Frequency(1)	Model 1	–	16	–	MHz
		Model 2	–	20	–	
	User-adjusted scale	–	–	–	0.2	%
	Frequency accuracy(1)	T_A = -40 to 105 °C	-2	–	2	%
		T_A = -20 to 105 °C	-1.5	–	1.5	%
		T_A = 25 °C	-0.5	–	0.5	%
tst (HRC)	HRC Oscillator Oscillation Stabilization Time	–	–	–	15	μs

1. Mass production test assurance.

3.3.17.2 Internal medium-rate (MRC) oscillator

Table 3-34 MRC Oscillator Characteristics

notation	parameters	minimum value	typical value	maximum values	unit (of measure)
f_{MRC}(1)	frequency	7.2	8	8.8	MHz
tst(MRC)	MRC oscillator stabilization time	–	–	3	μs

1. Mass production test assurance.

3.3.17.3 Internal Low Rate (LRC) Oscillator

Table 3-35 LRC Oscillator Characteristics

notation	parameters	minimum value	typical value	maximum values	unit (of measure)
f_{LRC}(1)	frequency	27.853	32.768	37.683	kHz
tst(LRC)	LRC oscillator stabilization time	–	–	36	μs

1. Mass production test assurance.

Table 3-36 SWDTLRC Oscillator Characteristics

notation	parameters	minimum value	typical value	maximum values	unit (of measure)
$f_{SWDTLRC}$ (1)	frequency	9	10	11	kHz
tst(SWDTLRC)	SWDTLRC oscillator stabilization time	–	–	57.1	μs

1. Mass production test assurance.

3.3.18 12-Bit ADC Characterization

Table 3-37 ADC Characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
V_{AVCC}	electric power source	–	1.8	–	3.6	V
V_{REFH}[1]	Positive reference voltage	–	1.8	–	V_{AVCC}	V
f_{ADC}	ADC Conversion Clock Frequency	Ultra High Speed/High Speed Motion Mode VAVCC=2.4~3.6 V	1	–	60	MHz
		Ultra High Speed/High Speed Motion Mode VAVCC=1.8~2.4 V	1	–	30	
		Ultra low speed action mode	1	–	8	
V_{AIN}	Conversion voltage range	–	V_{AVSS}	–	V_{REFH}	V
R_{AIN}	External Input Impedance	See Equation 1 for details	–	–	50	kΩ
R_{ADC}	Sampling Switch Resistor	–	–	–	6	kΩ
C_{ADC}	Internal sample and hold capacitance	–	–	4	7	pF
t_D	Trigger conversion delay	f_{ADC} = 60 MHz	–	–	0.3	μs

Table 3-38 ADC Characteristics (continued)

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
tS	sampling time	fADC=60MHz	0.183	–	4.266	μs
			11	–	255	1/fADC
tCONV	Total single-channel conversion time (including sampling time)	fADC = 60 MHz 12-bit resolution	0.4	–	–	μs
		fADC = 60 MHz 10-bit resolution	0.36	–	–	μs
		fADC = 60 MHz 8-bit resolution	0.33	–	–	μs
		20 to 268 (sampling time tS+ successive convergence to n-bit resolution+1)				1/fADC
fS	sampling rate fADC = 60 MHz	12-bit resolution single ADC	–	–	2.5	Msps
		12-bit resolution time interpolation Dual ADC	–	–	4.6	
tST	power-on time	–	–	1	2	μs

1. VAVCC-VREFH<1.2V

Equation 1: Formula for RAIN Maximum

$$RAIN = \frac{k-1}{fADC \times CADC \times \ln(2^{N+2})} - RADC$$

The above equation (Equation 1) is used to determine the maximum external impedance that will keep the error below 1/4 LSB. Where N = 12 (12-bit resolution) and k is the number of sample cycles defined in the ADC_SSTR register.

Table 3-39 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=60MHz

notation	parameters	prerequisite	typical value	maximum values	unit (of measure)
E_T	absolute error	Ultra High Speed/High Speed Motion Mode fADC=60MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±4.5	±6	LSB
E_O	offset error		±3.5	±6	LSB
E_G	gain error		±3.5	±6	LSB
E_D	differential linear error (DLE)		±1	±2	LSB
E_L	Integral Linearity Error		±1.5	±3	LSB

Table 3-40 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=30MHz

notation	parameters	conditional	typical value	maximum values	unit (of measure)
E_T	absolute error	Ultra High Speed/High Speed Motion Mode fADC=30MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±4.5	±6	LSB
E_O	offset error		±3.5	±6	LSB
E_G	gain error		±3.5	±6	LSB
E_D(1)	differential linear error (DLE)		±1	±2	LSB
E_L(1)	Integral Linearity Error		±1.5	±3	LSB

1. Mass production test assurance.

Table 3-41 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=30MHz

notation	parameters	conditional	typical value	maximum values	unit (of measure)
E_T	absolute error	Ultra High Speed/High Speed Motion Mode fADC=30MHz Input source impedance <1kΩ VAVCC=1.8 ~2.4V	±4.5	±6	LSB
E_O	offset error		±3.5	±6	LSB
E_G	gain error		±3.5	±6	LSB
E_D	differential linear error (DLE)		±1	±2	LSB
E_L	Integral Linearity Error		±2	±3	LSB

Table 3-42 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=8MHz

notation	parameters	conditional	typical value	maximum values	unit (of measure)
E_T	absolute error	Ultra-low speed	±4.5	±6	LSB
E_O	offset error		±3.5	±6	LSB

EG	gain error	action mode	±3.5	±6	LSB
ED	differential linear error (DLE)	fADC=8MHz	±1	±2	LSB
EL	Integral Linearity Error	Input source impedance <1kΩ VAVCC=1.8 ~3.6V	±2	±3	LSB

Table 3-43 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=60MHz

notation	parameters	conditional	typical value	maximum values	unit (of measure)
E_T	absolute error	Ultra High Speed/High Speed Motion Mode fADC=60MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±5.5	±7	LSB
E_O	offset error		±4.5	±7	LSB
E_G	gain error		±4.5	±7	LSB
E_D	differential linear error (DLE)		±1.5	±2	LSB
E_L	Integral Linearity Error		±2.0	±3	LSB

Table 3-44 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=30MHz

notation	parameters	prerequisite	typical value	maximum values	unit (of measure)
E_T	absolute error	Ultra High Speed/High Speed Motion Mode fADC=30MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±5.5	±7	LSB
E_O	offset error		±4.5	±7	LSB
E_G	gain error		±4.5	±7	LSB
E_D(1)	differential linear error (DLE)		±1.5	±2	LSB
E_L(1)	Integral Linearity Error		±2.0	±3	LSB

1. Mass production test assurance.

Table 3-45 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=30MHz

notation	parameters	conditional	typical value	maximum values	unit (of measure)
E_T	absolute error	Ultra High Speed/High Speed Motion Mode fADC=30MHz Input source impedance <1kΩ VAVCC=1.8 ~2.4V	±5.5	±7	LSB
E_O	offset error		±4.5	±7	LSB
E_G	gain error		±4.5	±7	LSB
E_D	differential linear error (DLE)		±1.5	±2	LSB
E_L	Integral Linearity Error		±2.5	±3	LSB

Table 3-46 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=8MHz

notation	parameters	conditional	typical value	maximum values	unit (of measur

					e)
ET	absolute error	Ultra-low speed action mode fADC=8MHz Input source impedance <1kΩ VAVCC=1.8 ~3.6V	±5.5	±7	LSB
EO	offset error		±4.5	±7	LSB
EG	gain error		±4.5	±7	LSB
ED	differential linear error (DLE)		±1.5	±2	LSB
EL	Integral Linearity Error		±2.5	±3	LSB

Table 3-47 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Dynamic Accuracy @ fADC=60MHz

notation	parameters	prerequisite	minimum value	maximum values	unit (of measure)
ENOB	valid digits	Ultra High Speed/High Speed Motion Mode fADC=60MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	10.6	–	Bits
SINAD	signal-to-noise ratio		64	–	dB
SNR	signal-to-noise ratio		66	–	dB
THD	THD		–	-70	dB

Table 3-48 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Dynamic Accuracy @ fADC=30MHz

notation	parameters	conditional	minimum value	maximum values	unit (of measure)
ENOB	valid digits	Ultra High Speed/High Speed Motion Mode fADC=30MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=1.8~2.4V	10.4	–	Bits
SINAD	signal-to-noise ratio		62	–	dB
SNR	signal-to-noise ratio		64	–	dB
THD	THD		–	-67	dB

Table 3-49 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Dynamic Accuracy @ fADC=8MHz

notation	parameters	conditional	minimum value	maximum values	unit (of measure)
ENOB	valid digits	Ultra-low speed action mode fADC=8MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=1.8~3.6V	10.4	–	Bits
SINAD	signal-to-noise ratio		62	–	dB
SNR	signal-to-noise ratio		64	–	dB
THD	THD		–	-67	dB

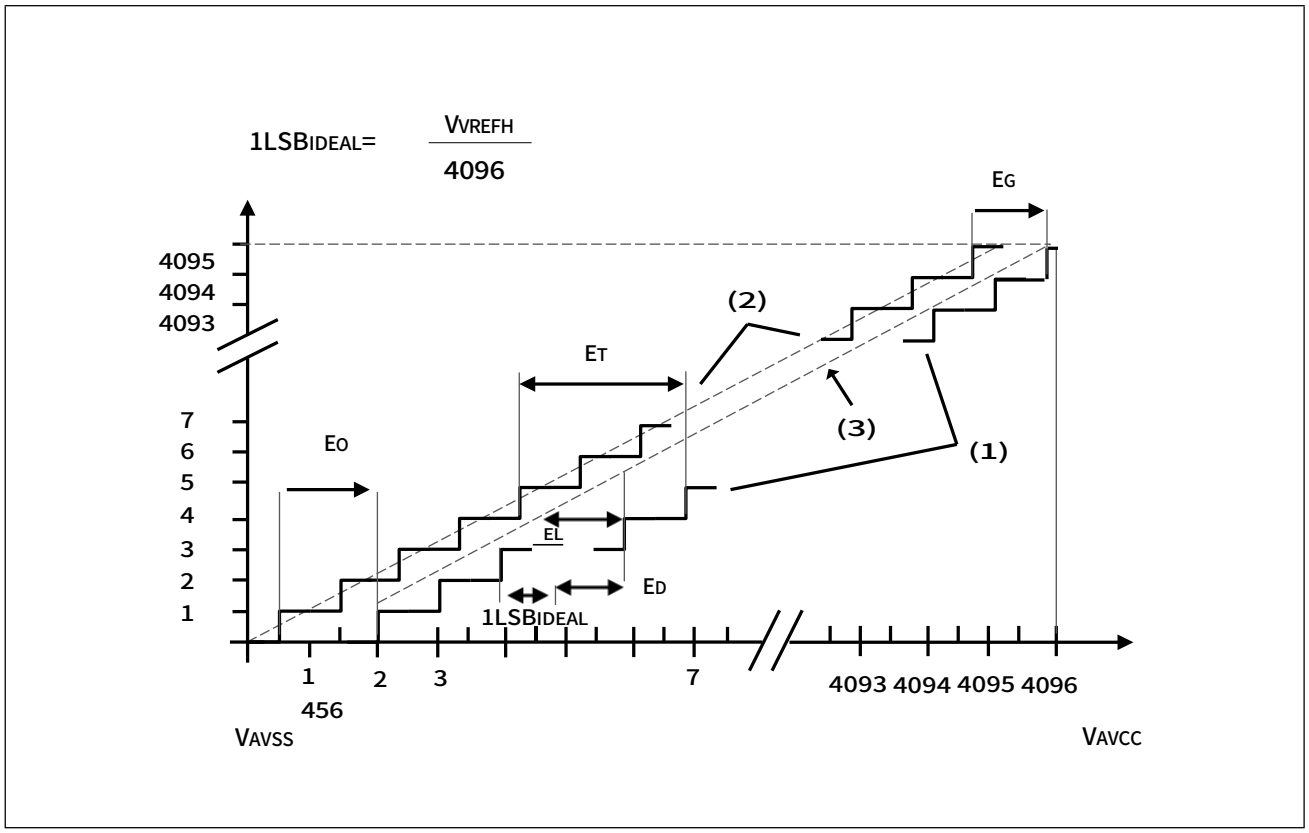


Figure 3-21 ADC Accuracy Characteristics

1. See also the table above.
2. Examples of actual transmission curves.
3. Ideal Transfer Curve.
4. Endpoint correlation lines.
5. $_{ET}$ = Total unadjusted error: maximum deviation between actual and ideal transfer curves. $_{EO}$ = Offset Error: the deviation between the first actual conversion and the first ideal conversion.

   $_{EG}$ = Gain error: the deviation between the last ideal transition and the last actual transition. $_{ED}$ = Differential Linearity Error: Maximum deviation between actual step and ideal.

   $_{EL}$ = Integral Linearity Error: the maximum deviation between any actual conversion and the endpoint correlation line.

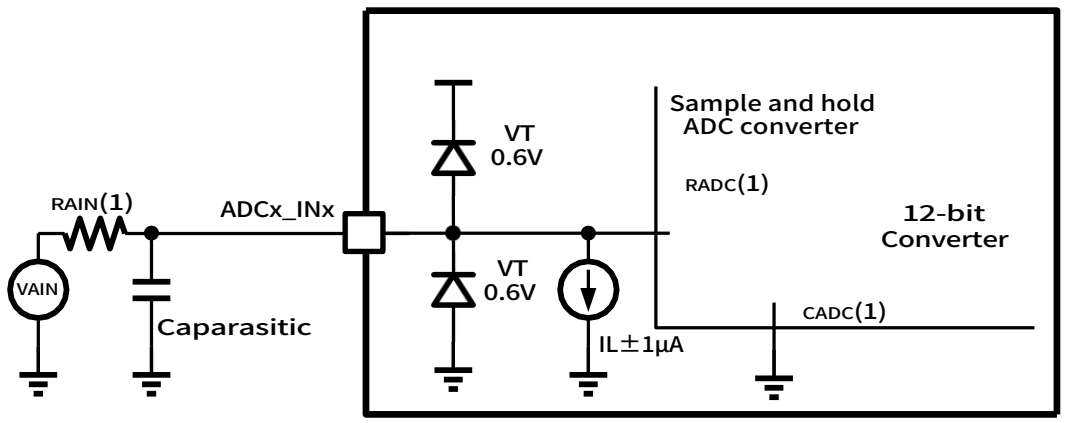


Figure 3-22 Typical Connection Using ADCs

1. See Table 3-37 for information on R_{AIN}, R_{ADC}, and C_{ADC} values.
2. $C_{parasitic}$ indicates the PCB capacitance (depending on the quality of soldering and PCB wiring) as well as the pad capacitance (approx. 5pF). Higher $C_{parasitic}$ values result in lower conversion accuracy. To solve this problem, the f_{ADC} should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the figure below, depending on whether VREFH is connected to AVCC and the number of AVCC pins. 0.1μF capacitors should be (high quality) ceramic capacitors. These capacitors should be placed as close to the chip as possible.

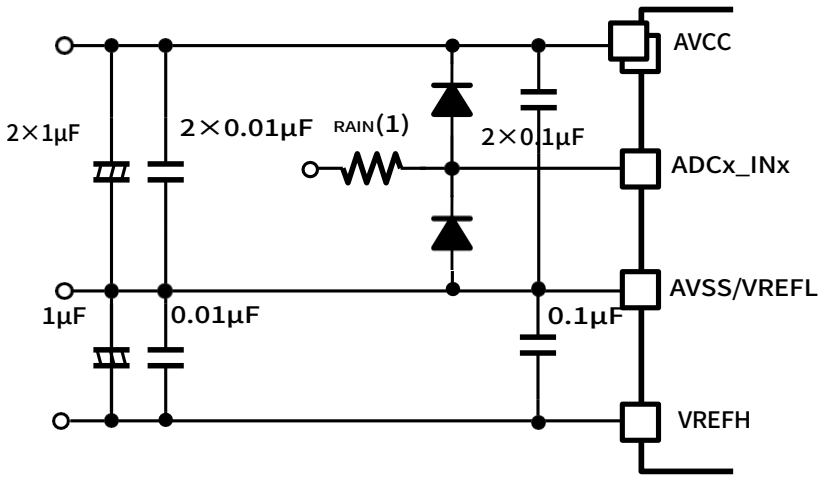


Figure 3-23 Power and Reference Decoupling Example

3.3.19 DAC Characteristics

Table 3-50 DAC Characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
V_{AVCC}	Analog Supply Voltage	–	1.8	3.3	3.6	V
DNL	Differential nonlinear error (deviation between two consecutive codes – 1LSB)	–	–	–	±2	LSB
misalignment	Offset error (difference between the measured value at code (0x80) and the ideal value $V_{AVCC/2}$)	–	–	–	±2	LSB
$T_{SETTLING}$	Build-up time (full scale: applies to 8-bit input code transition between lowest and highest input code until DA0/DA1 reaches its final value of ±4LSB)	–	–	–	8	μs

3.3.20 Comparator Characteristics

Table 3-51 Comparator Characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
V_{AVCC}	Analog Supply Voltage	–	1.8	3.3	3.6	V
V_I	Input Voltage Range	–	0	–	V_{AVCC}	V
T_{cmp}	Comparison time	Comparator resolution voltage = 100mV	–	50	100	ns
T_{set}	Input channel switching stabilization time	–	–	100	200	ns

3.3.21 Gain Adjustable Amplifier Characteristics

Table 3-52 Gain Adjustable Amplifier Characteristics

notation	parameters		conditional	minimum value	typical value	maximum values	unit (of measure)
V_{AVCC}	Analog Supply Voltage		–	1.8	3.3	3.6	V
V_{OS} (1)	Input Offset Voltage		–	-8	–	8	mV
V_I	Input Voltage Range		–	0.1*VAVCC/Gain	–	0.9*VAVCC/Gain	V
G_E	gain error	Use of external ports PGAVSS As the PGA Negative phase input	Gain=2(1)	-1	–	1	%
			Gain=2.133	-1	–	1	%
			Gain=2.286	-1	–	1	%
			Gain=2.667	-1	–	1	%
			Gain=2.909	-1	–	1	%
			Gain=3.2	-1.5	–	1.5	%
			Gain=3.556	-1.5	–	1.5	%
			Gain=4.0	-1.5	–	1.5	%
			Gain=4.571	-2	–	2	%
			Gain=5.333	-2	–	2	%
			Gain=6.4	-3.0	–	3.0	%
			Gain=8	-3.0	–	3.0	%
			Gain=10.667	-4.0	–	4.0	%
			Gain=16	-4.0	–	4.0	%
			Gain=32(1)	-7.0	–	7.0	%
		Using the internal analogical site AVSS Negative	Gain=2(1)	-2	–	2	%
			Gain=2.133	-2	–	2	%
			Gain=2.286	-2	–	2	%
			Gain=2.667	-2	–	2	%
			Gain=2.909	-2	–	2	%
			Gain=3.2	-2.5	–	2.5	%
			Gain=3.556	-2.5	–	2.5	%
			Gain=4.0	-2.5	–	2.5	%
			Gain=4.571	-3.0	–	3.0	%

		for PGA phase input	Gain=5.333	-3.0	–	3.0	%
			Gain=6.4	-4.0	–	4.0	%
			Gain=8	-4.0	–	4.0	%
			Gain=10.667	-5.0	–	5.0	%
			Gain=16	-5.0	–	5.0	%
			Gain=32(1)	-8.0	–	8.0	%

1. Mass production test assurance.

3.3.22 temperature sensor

Table 3-53 Temperature Sensor Characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
TL	relative accuracy	Each chip is individually calibrated according to the user manual	–	–	±5	℃

3.3.23 Memory Characteristics

3.3.23.1 (electronic) flash memory

Flash memory is erased when the device is delivered to the customer.

Table 3-54 Flash Characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
IVCC	Supply Current	Read mode, VCC=1.8 V~3.6V	–	–	5	mA
		Programming mode, VCC=1.8 V~3.6V	–	–	10	
		Block erase mode, VCC=1.8 V~3.6V	–	–	10	
		Full erase mode, VCC=1.8 V~3.6V	–	–	10	

Table 3-55 Flash Programming Erase Time

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
T_{prog} (1)	word programming time	single-programming mode	43+2* T_{hclk} (2)	48+4* T_{hclk} (2)	53+6* T_{hclk} (2)	μs
	word programming time	Continuous Programming Mode	12+2* T_{hclk} (2)	14+4* T_{hclk} (2)	16+6* T_{hclk} (2)	μs
T_{erase} (1)	Block Erase Time	–	16+2* T_{hclk} (2)	18+4* T_{hclk} (2)	20+6* T_{hclk} (2)	ms
T_{mas} (1)	full erase time	–	16+2* T_{hclk} (2)	18+4* T_{hclk} (2)	20+6* T_{hclk} (2)	ms

1. Mass production testing guaranteed.
2. T_{hclk} is 1 cycle of the CPU clock.

Table 3-56 Flash Rewritable Counts and Data Retention Periods

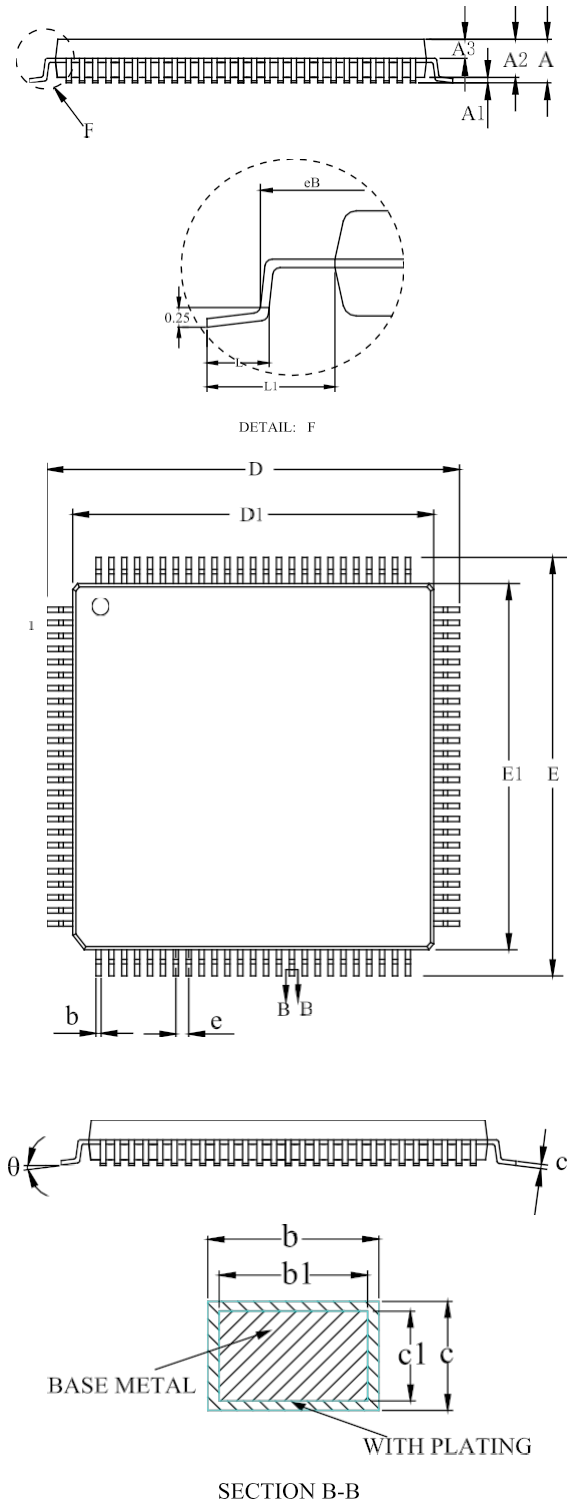
notation	parameters	conditional	numerical value	unit (of measure)
			minimum value	
Nend	Programming, Block Erase Count	T_A = 85°C	10	kcycles
Nend	Full Erase Count	T_A = 85°C	10	kcycles

Tret	Data retention period	T_A = 85°C after 10 kcycles	10	Years

4 Package Information

4.1 Package Size

LQFP100 package



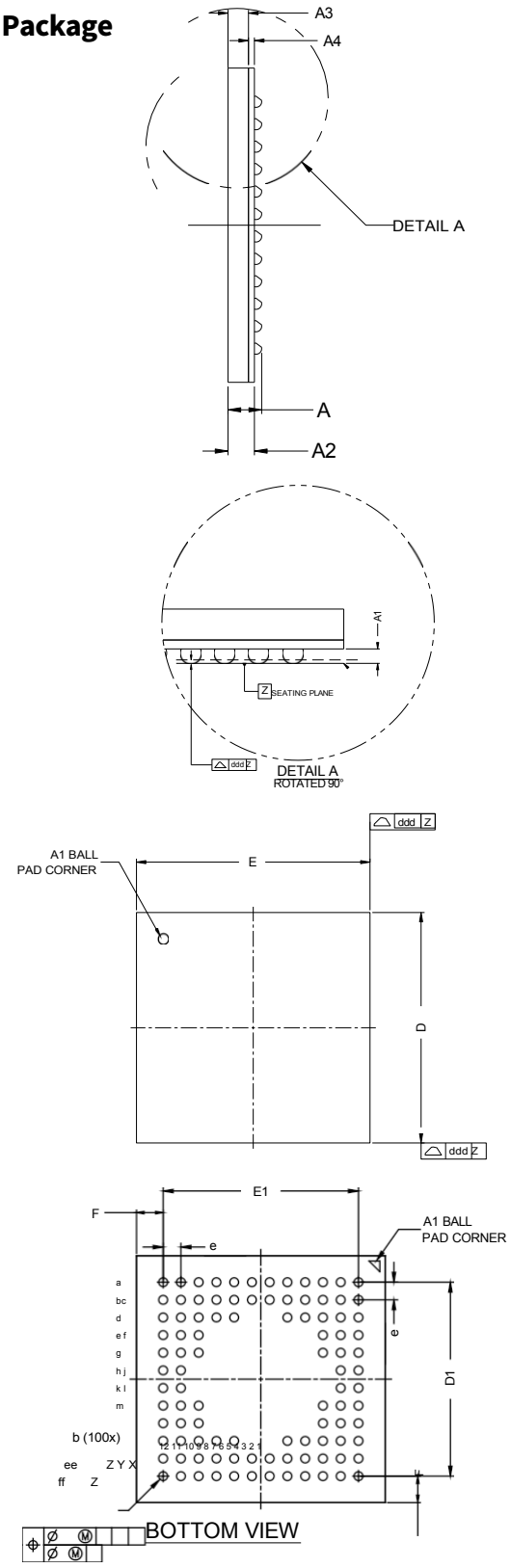
Symbol	14x14 Millimeter		
	Min	Nom	Max.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.27
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°

NOTE.

- Dimensions "D1" and "E1" do not include mold flash.

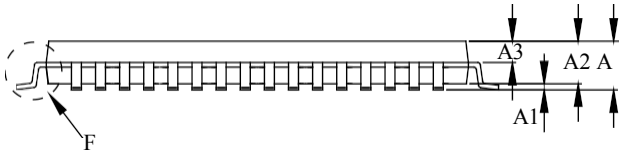
VFBGA100

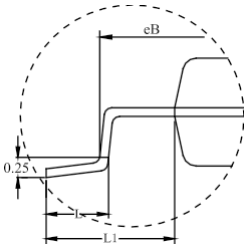
Package



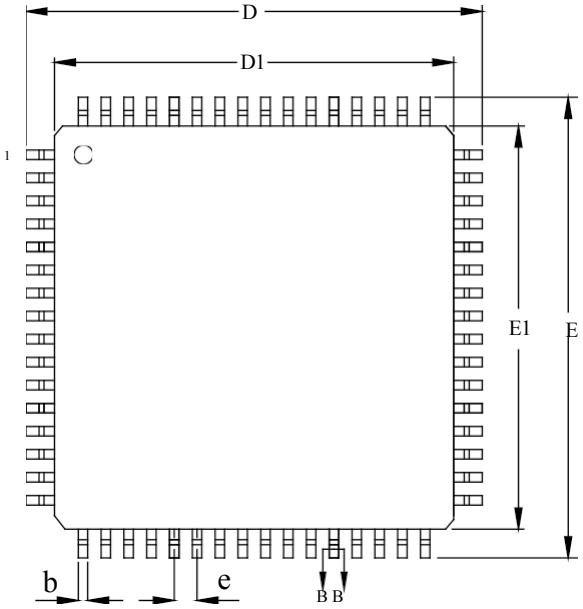
Symbol	7x7 Millimeter		
	Min	Nom	Max.
A	0.67	0.74	0.81
A1	0.11	0.16	0.21
A2	0.54	0.58	0.62
A3	0.45REF		
A4	0.13REF		
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D1	--	5.5	--
E	6.90	7.00	7.10
E1	--	5.5	--
e	--	0.5	--
F	0.75REF		
ddd	--	0.10	--
eee	--	0.15	--
fff	--	0.05	--

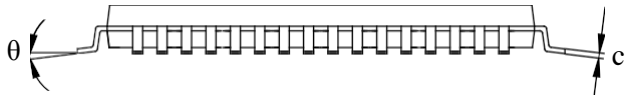
LQFP64 package

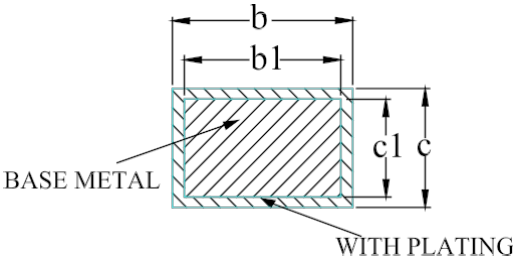




DETAIL: F







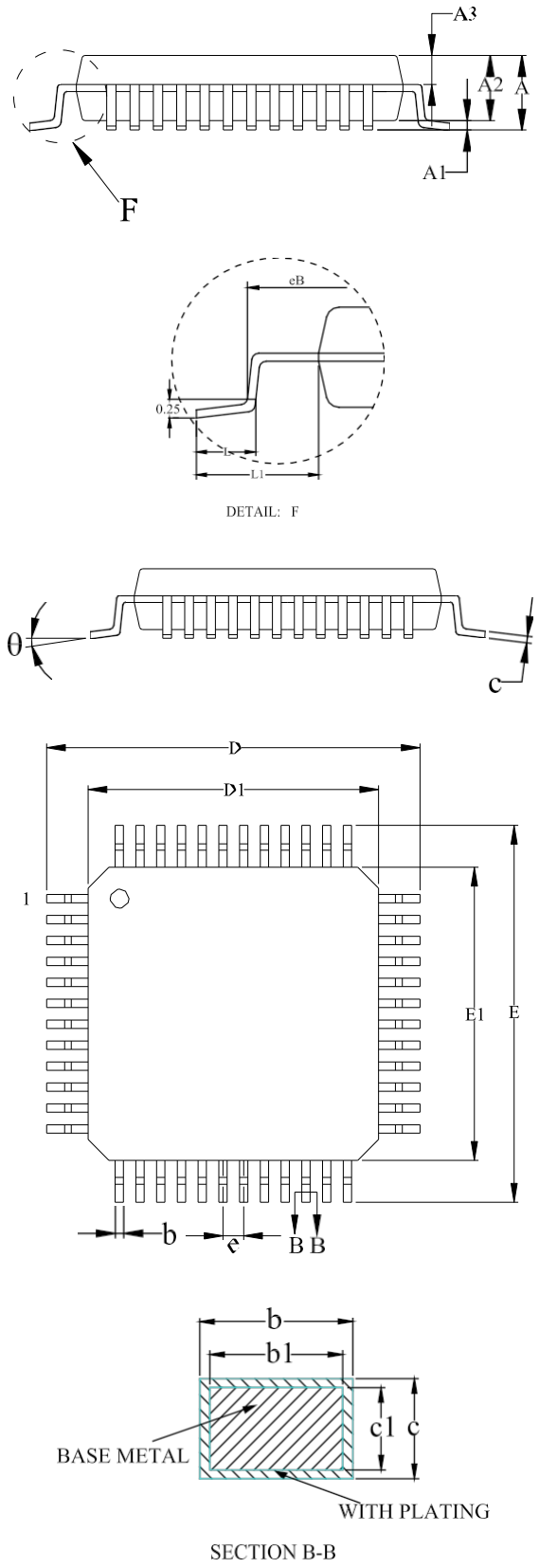
SECTION B-B

Symbol	10x10 Millimeter		
	Min	Nom	Max.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.27
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0°	--	7°

NOTE.

- Dimensions "D1" and "E1" do not include mold flash.

LQFP48 package

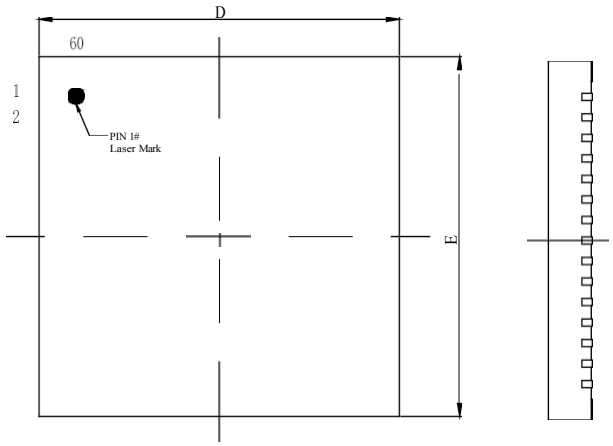


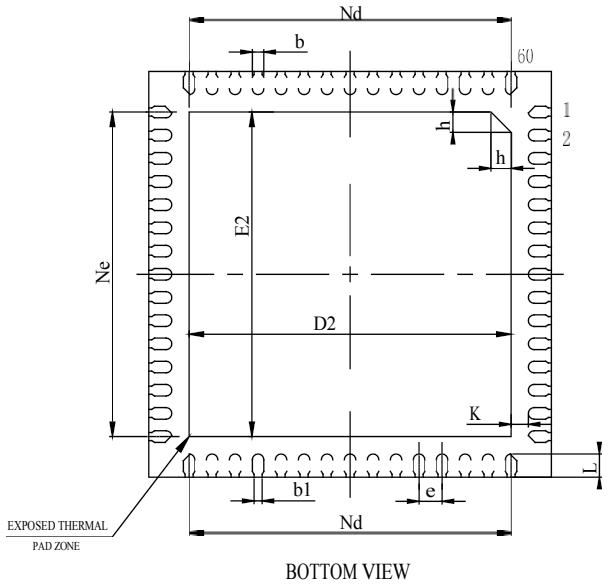
Symbol	7x7 Millimeter		
	Min	Nom	Max.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.27
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.40	--	0.65
L1	1.00REF		
θ	0	--	7°

NOTE.

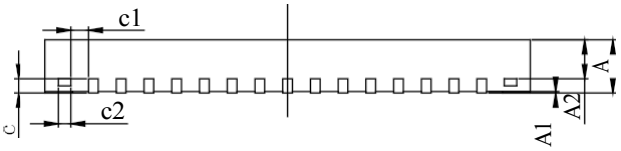
- Dimensions "D1" and "E1" do not include mold flash.

QFN60 package



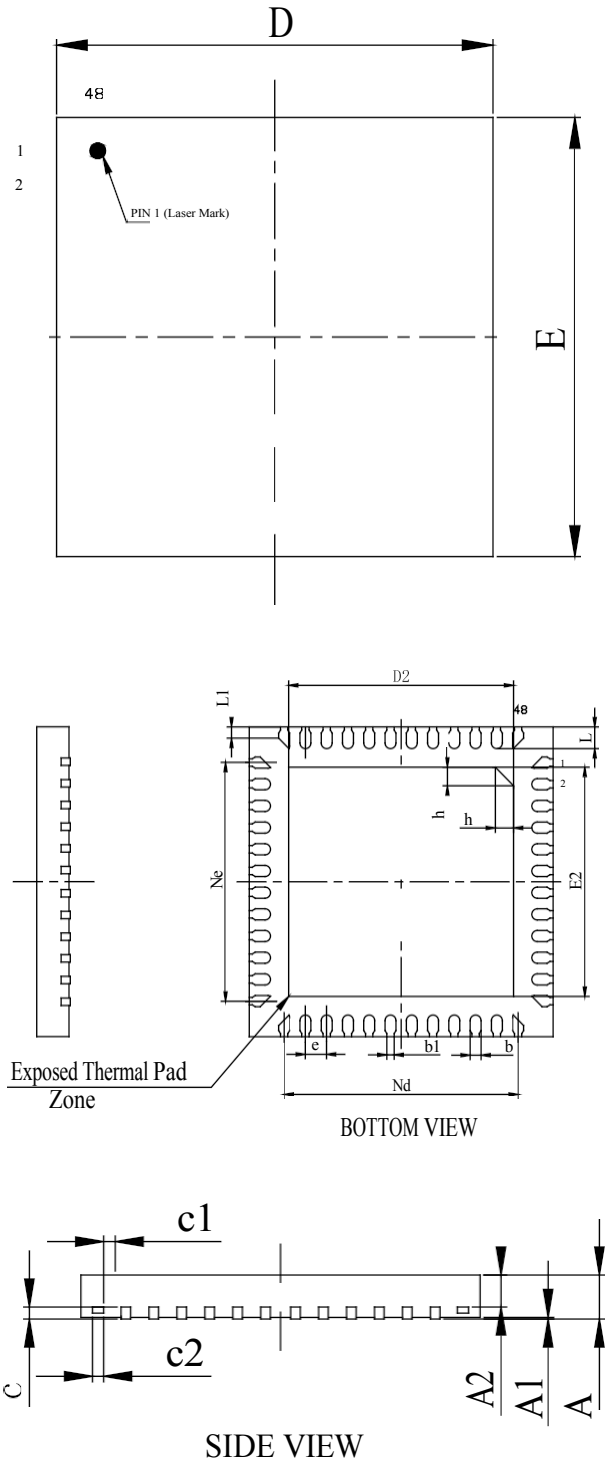


BOTTOM VIEW



Symbol	7x7 Millimeter		
	Min	Nom	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.547REF	
b	0.15	0.20	0.25
b1		0.14REF	
c		0.20REF	
c1		0.255REF	
c2		0.18REF	
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
Nd		5.60BSC	
e		0.40BSC	
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
Ne		5.60BSC	
L	0.35	0.40	0.45
K	0.25	0.30	0.35
h	0.30	0.35	0.40

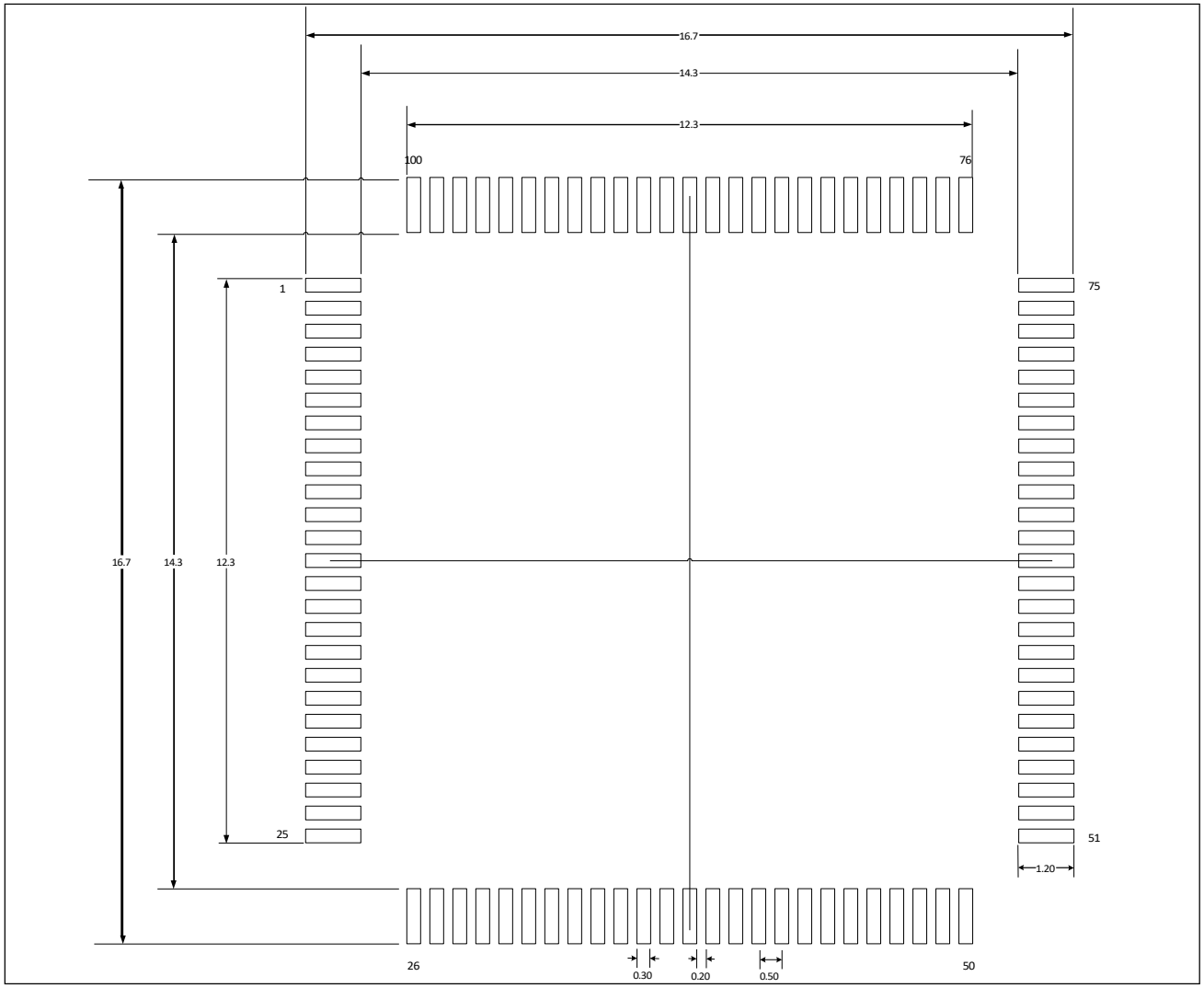
QFN48 Package



Symbol	5x5 Millimeter		
	Min	Nom	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2		0.40REF	
b	0.13	0.18	0.23
b1		0.12REF	
c	0.10	0.15	0.20
c1		0.145REF	
c2		0.140REF	
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e		0.35BSC	
Ne		3.85BSC	
Nd		3.85BSC	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F Carrier sizes		154 x 154	

4.2 Pad Schematic

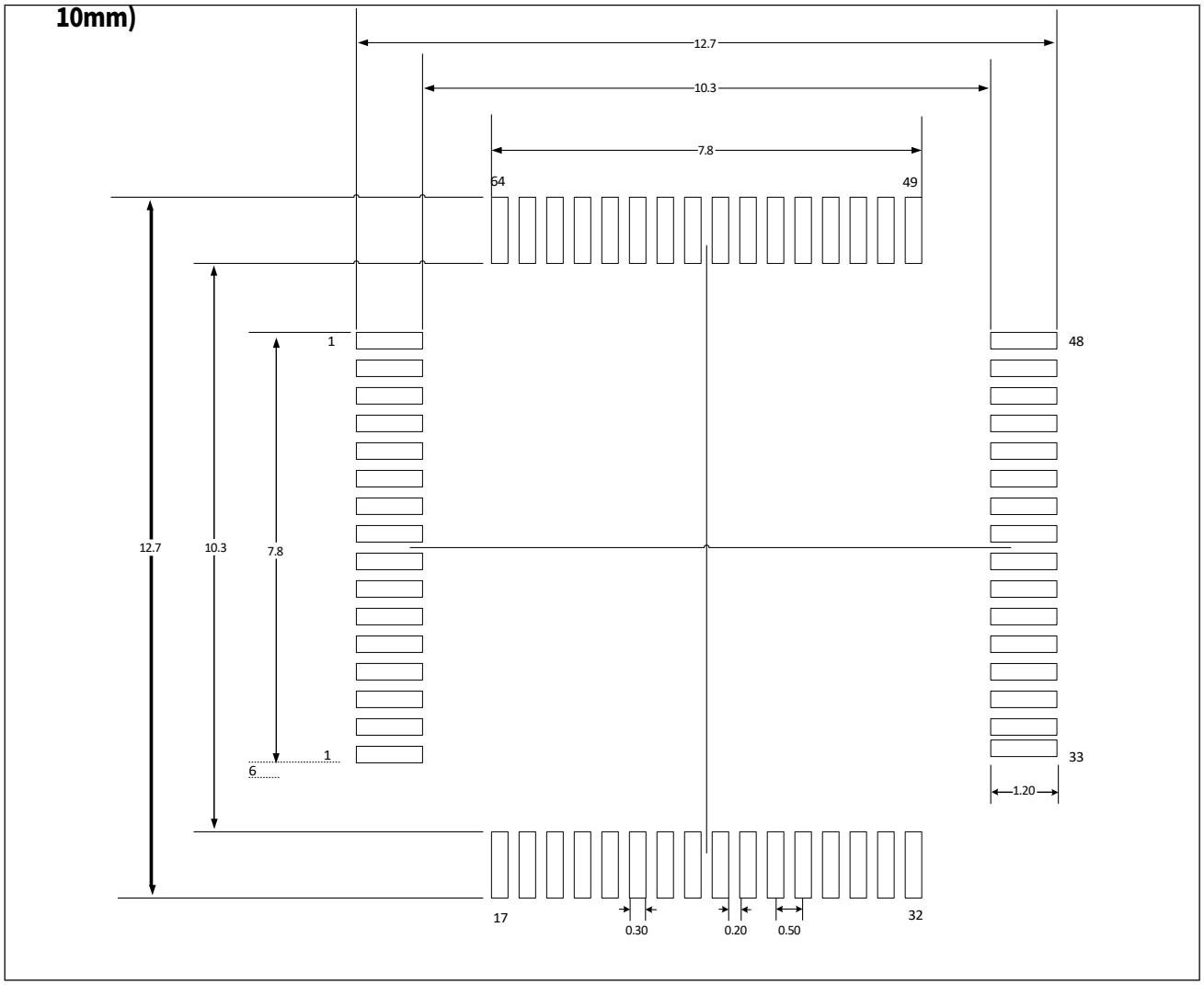
LQFP100 package (14mm x 14mm)



NOTE.

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

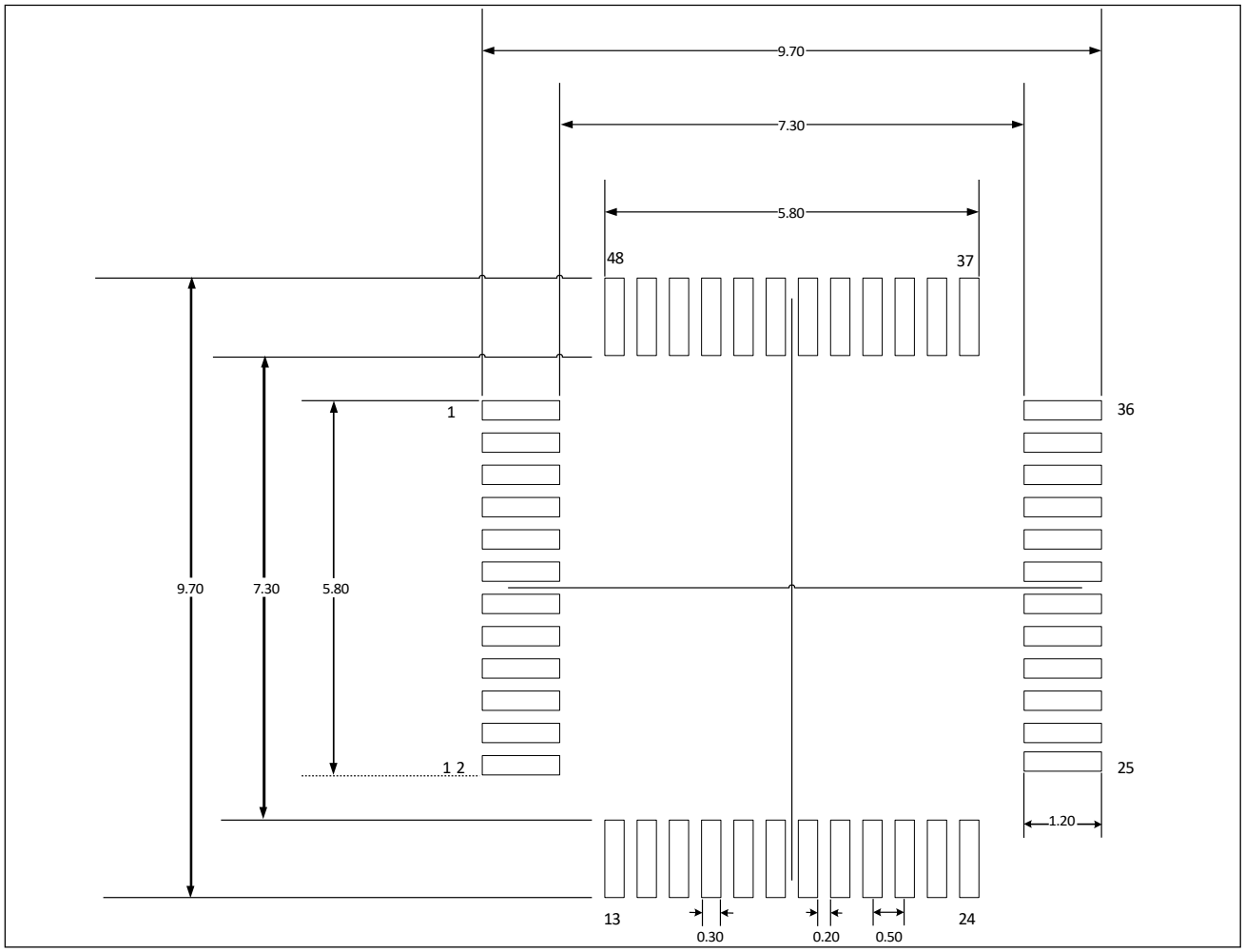
LQFP64 package (10mm x 10mm)



NOTE.

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

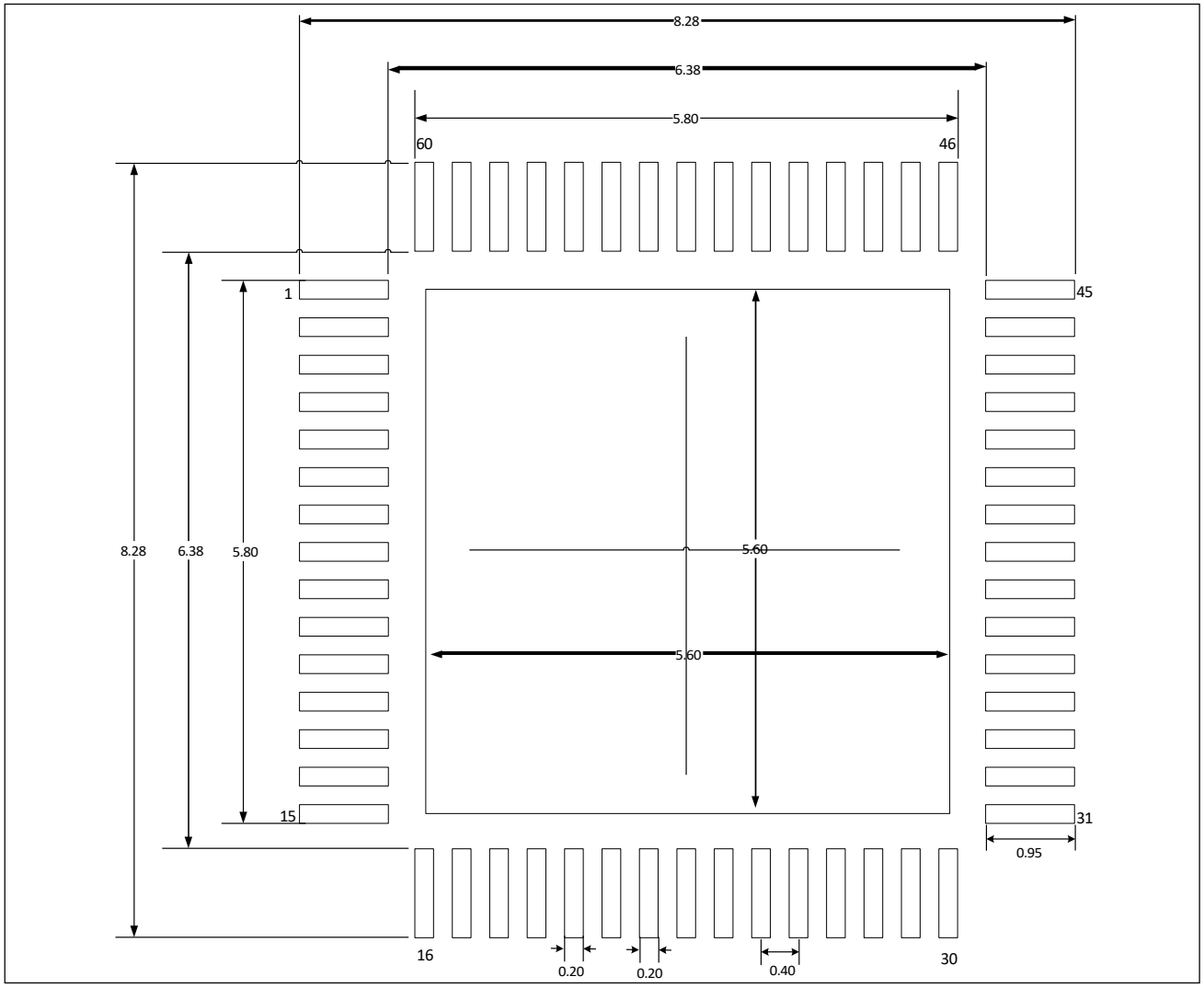
LQFP48 package (7mm x 7mm)



NOTE.

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

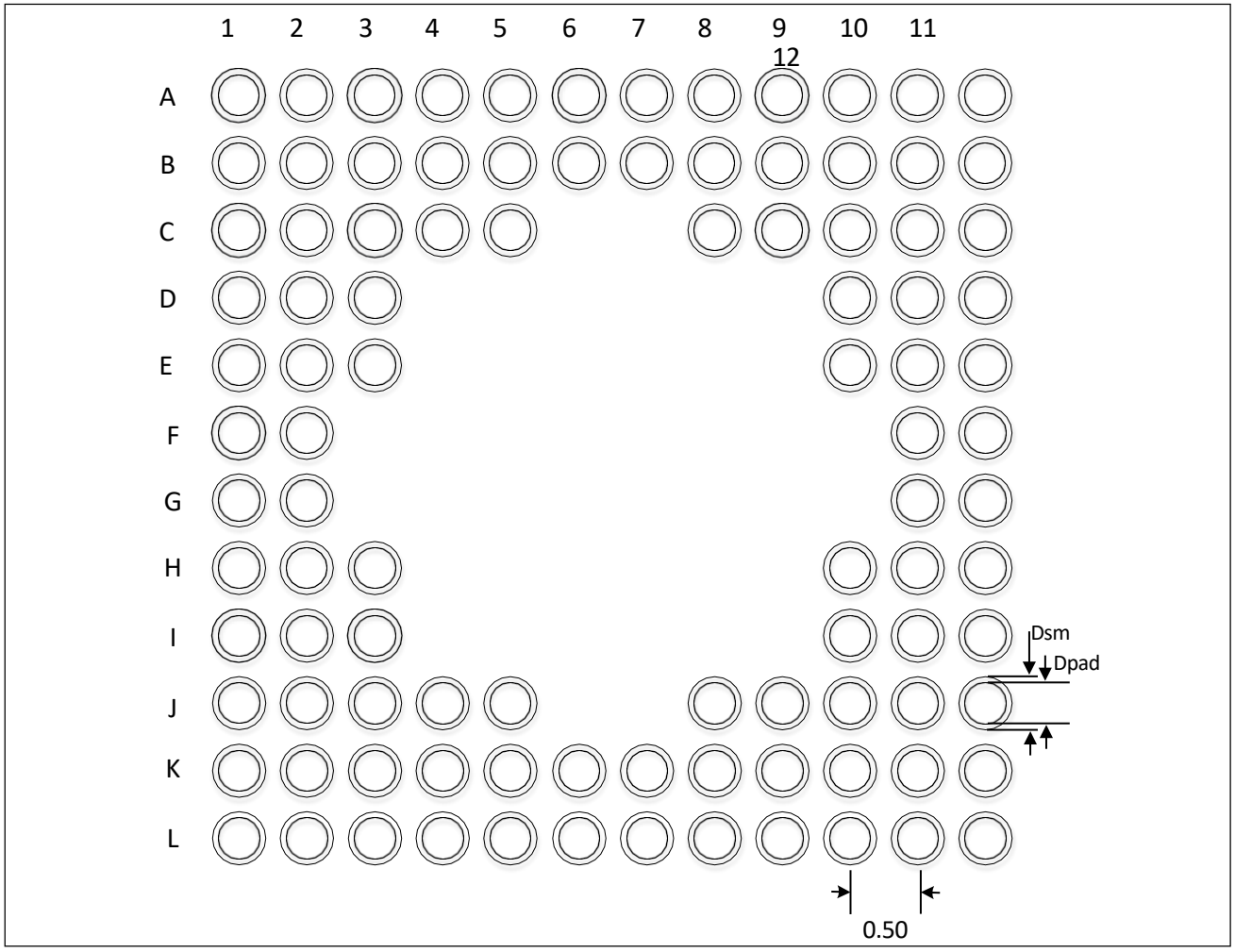
QFN60 package (7mm x 7mm)



NOTE.

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

VFBGA100 package (7mm x 7mm)



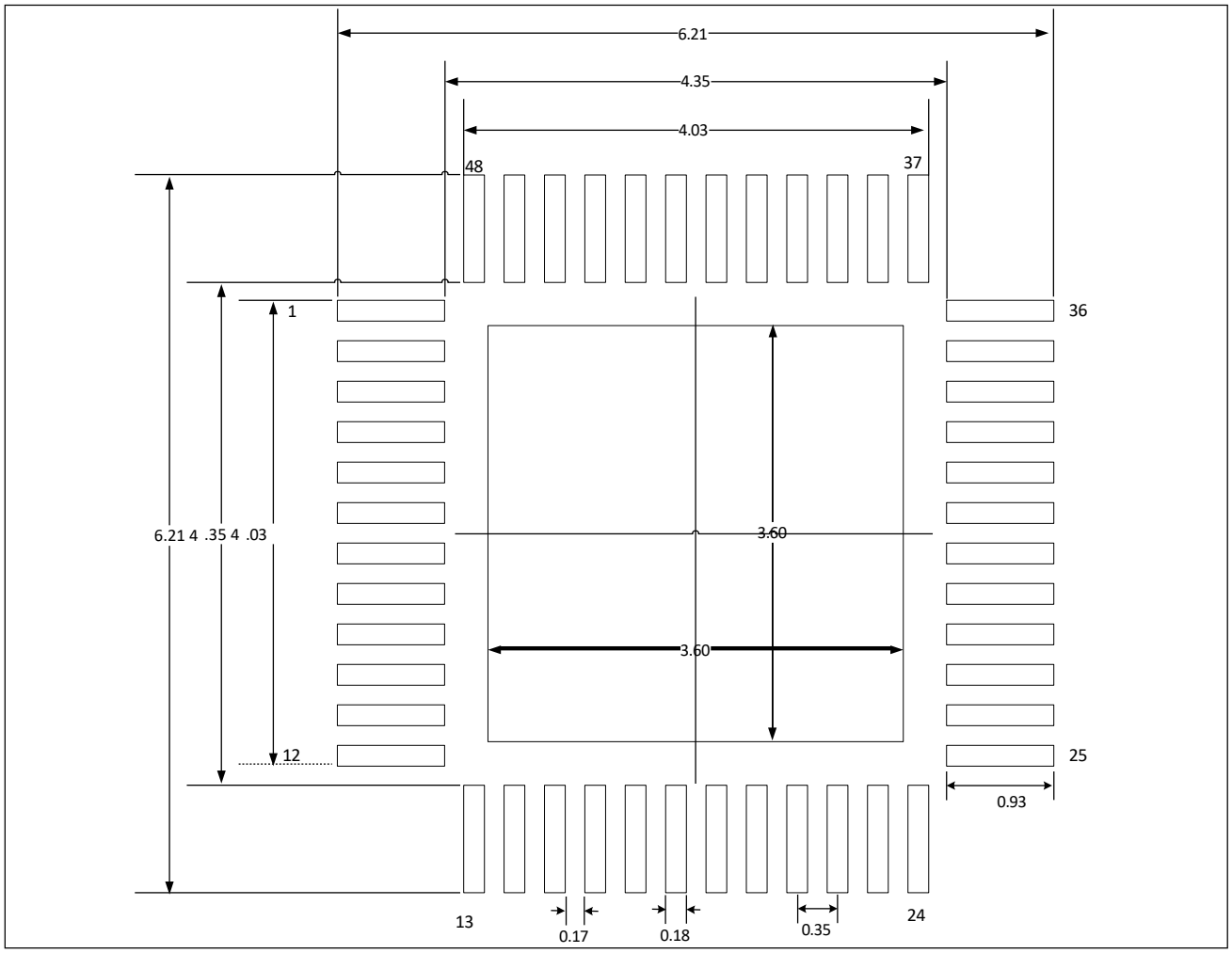
NOTE.

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

VBGA100 recommended PCB design rules (0.5mm pitch)

Dimension	Recommended values
Pitch	0.5mm
Dpad	0.240mm
Dsm	0.340mm typ. (depends on the soldermask registration) tolerance)
Stencil opening	0.240mm
Stencil thickness	Between 0.100mm and 0.125mm

QFN48 package (5mm x 5mm)



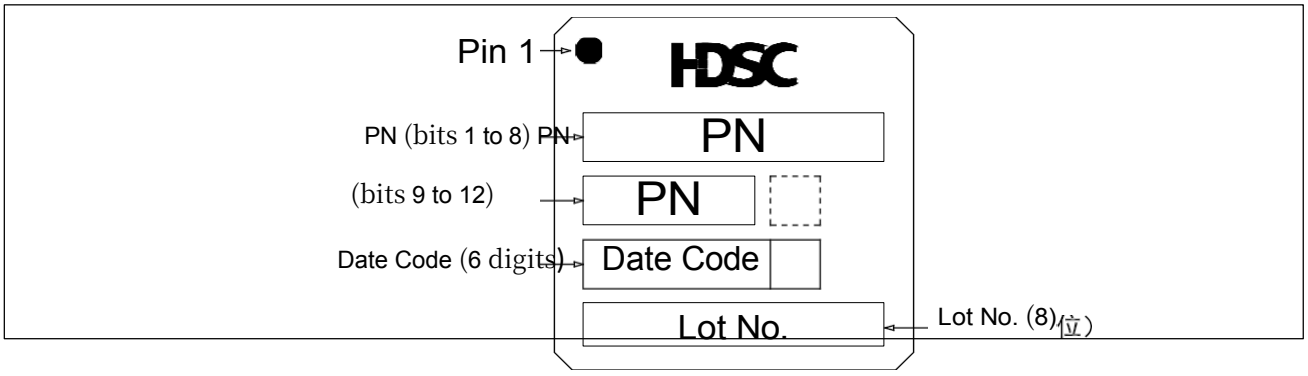
NOTE.

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

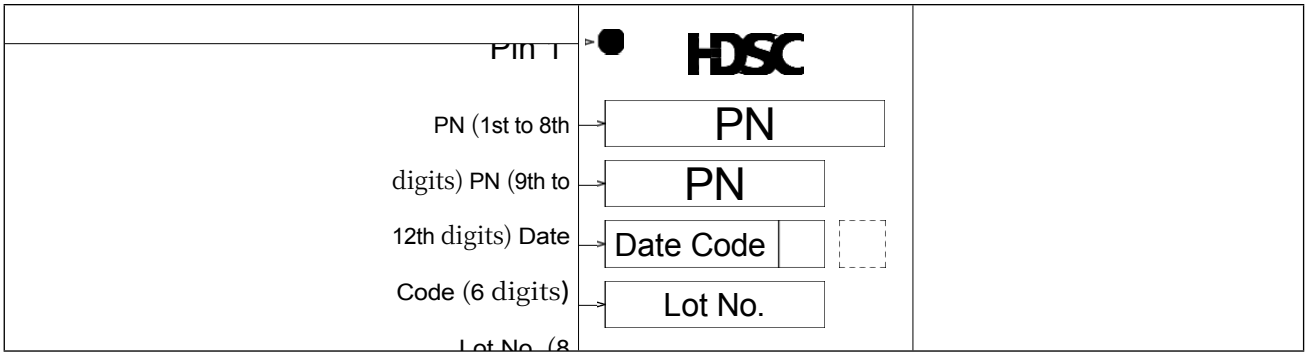
4.3 Screen Printing Instructions

The location of Pin 1 and a description of the information silk-screened on the front of each package are given below.

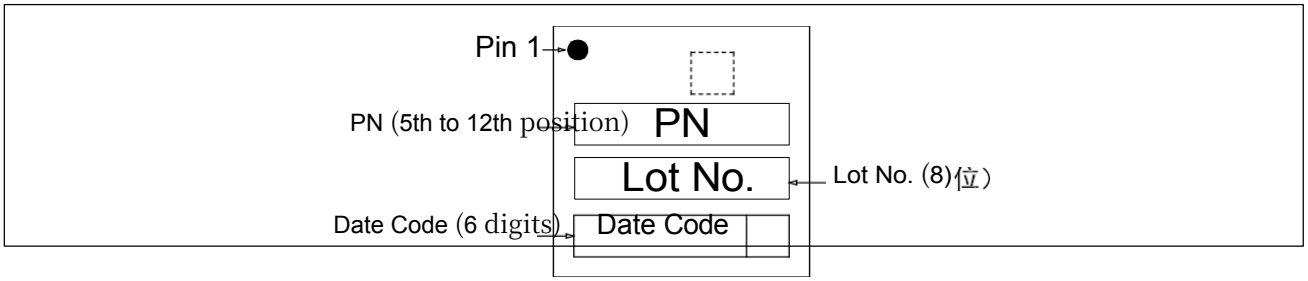
LQFP100 package (14mm x 14mm) / LQFP64 package (10mm x 10mm) LQFP48 package (7mm x 7mm)



QFN60 package (7mm x 7mm) / VFBGA100 package (7mm x 7mm)



QFN48 package (5mm x 5mm)



Attention:

– The blank boxes above indicate optional production-related markers that are not described in this section.

4.4 Package Thermal Resistance

The junction temperature T_j (°C) of the chip surface can be calculated according to the following formula when the packaged chip is operated at the specified operating ambient temperature:

$$Tj = T_A + (P_D \times \theta_{JA})$$

- T_A is the operating ambient temperature in °C at which the packaged chip operates;
- θ_{JA} is the thermal resistance coefficient of the package to the operating environment in °C/W;
- P_D equals the sum of the chip's internal power consumption (P_{INT}) and the power consumption ($P_{I/O}$) generated by the I/O pins while the chip is operating, in W. $P_{INT} = I_{CC} \times V_{CC}$

  $P_{I/O} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{CC} - V_{OH}) \times I_{OH})$

The junction temperature T_j on the surface of the chip when the chip is operated at the specified operating ambient temperature must not exceed the maximum junction temperature T_J allowable for the chip.

Table 4-1 Thermal Resistance Coefficients of Packages

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10%	°C/W
LQFP64 10mm x 10mm / 0.5mm pitch	65 +/- 10%	°C/W
LQFP48 7mm x 7mm / 0.5mm pitch	75 +/- 10%	°C/W
QFN60 7mm x 7mm / 0.4mm pitch	30 +/- 10%	°C/W
QFN48 5mm x 5mm / 0.35mm pitch	42 +/- 10%	°C/W

5 Ordering Information

Product Model	hc32f460jeua-qfn48tr	HC32F460JETA-LQFP48	hc32f460keua-qfn60tr	hc32f460keta-lqfp64	hc32f460petb-lqfp100	hc32f460pehb-vfbga100	HC32F460JCTA-LQFP48	HC32F460KCTA-LQFP64	HC32F460PCTB-LQFP100
Main Frequency (MHz)	200	200	200	200	200	200	200	200	200
kernel (computer science)	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4
Flash (KB)	512	512	512	512	512	512	256	256	256
RAM (KB)	192	192	192	192	192	192	192	192	192
OTP (B)	960	960	960	960	960	960	960	960	960
Package (mm*mm)	QFN48 (5*5) e=0.35	LQFP48 (7*7) e=0.5	QFN60 (7*7) e=0.4	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5	VFBGA100 (7*7) e=0.5	LQFP48 (7*7) e=0.5	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5
Universal IO	38	38	50	52	83	83	38	52	83
Minimum Operating Voltage	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
Maximum working voltage	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
16-bit Timer	11	11	11	11	11	11	11	11	11
Motor Control Timer	3	3	3	3	3	3	3	3	3
12-bit ADC converter unit	2	2	2	2	2	2	2	2	2
Number of 12-bit ADC channels	10	10	15	16	16	16	10	16	16
comparator	3	3	3	3	3	3	3	3	3
Amplifier PGA	1	1	1	1	1	1	1	1	1
SPI	4	4	4	4	4	4	4	4	4
QUADSPI	1	1	1	1	1	1	1	1	1
I S²	4	4	4	4	4	4	4	4	4
I C²	3	3	3	3	3	3	3	3	3
U(S)ART	4	4	4	4	4	4	4	4	4
CAN	1	1	1	1	1	1	1	1	1
SDIO	2	2	2	2	2	2	2	2	2
Full Speed USB OTG	1	1	1	1	1	1	1	1	1
DMA	8	8	8	8	8	8	8	8	8
DCU	4	4	4	4	4	4	4	4	4
PVD	✓	✓	✓	✓	✓	✓	✓	✓	✓
AES128	✓	✓	✓	✓	✓	✓	✓	✓	✓
SHA256	✓	✓	✓	✓	✓	✓	✓	✓	✓
TRNG	✓	✓	✓	✓	✓	✓	✓	✓	✓
CRC	✓	✓	✓	✓	✓	✓	✓	✓	✓
KEYSCAN	✓	✓	✓	✓	✓	✓	✓	✓	✓
RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓
FLASH Physical Encryption	✓	✓	✓	✓	✓	✓	✓	✓	✓
shipment method	reel	cross-loading (on a tray)	reel	cross-loading (on a tray)	cross-loading (on a tray)	cross-loading (on a tray)	cross-loading (on a tray)	cross-loading (on a tray)	cross-loading (on a tray)

Before ordering, please contact the sales window for the latest mass production information.

Version Revision Record

version number	revision date	revision
Rev1.0	2019/11/12	First Edition Release.
Rev1.1	2020/01/10	1) Add 256KB of product descriptions to the full text; 2) VFBGA package description added throughout; 3) Modify the current max value for 105°C in power-down mode in the Electrical Characteristics; 4) Updated silkscreen instructions.
Rev1.2	2020/08/26	1) Addition of ultra-high-speed operation mode description, update CoreMark/DMIPS to add ultra-high-speed mode description. Updated functional block diagrams; 2) The pinout diagram adds 256KB models; 3) Add pad schematic and package thermal resistance factor; 4) Increased BOR/PVD characteristics in ultra-high speed mode, current characteristics; 5) Update the JTAG/SWJ debug port pins;

Rev1.3	2021/12/10	1) Modify declaration, add A2/c1/c2 size of QFN48/60 in package size, modify data retention period in flash memory; 2) External master clock crystal(4-24MHz) to (4-25MHz) 3) Function block diagram modification: USB_DMA -> USBFS_DMA; I2S_1 -> I2S_2; Increase AOS; 4) 1.4.6 Addresses 0x00000400H~0x0000041FH -> 0x0000_0400~0x0000_041F 0x00000408~0x0000041F -> 0x0000_0408~0x0000_041F 5) Added description of "Automated Operating System (AOS)", updated "Keyboard Scanning". (KEYSCAN)" Description; 6) Name fixes and description optimization; 7) Modify the recommended configuration of the analog power supply pin bypass capacitor in the power supply schematic by deleting the 10nF capacitor and modifying the 10uF capacitor to 1uF; 8) Add parameter entries to the Reset and Power Control Module Characterization Table: TIPVD1/ TIPVD2/ TINRST/ TRSTBOR TIPVD2/ TINRST/ TRSTBOR TRSTTAO->TRSTPOR; 9) 3.3.12 Add CAN2.0B interface characterization; 10) The Max value of f_{PLL_IN} in PLL characteristics is changed from 24MHz to 25MHz to increase the Jitter characteristics;
version number	**revision date**	**revision**
		11) 3.3.16.1 f_{XTAL_EXT} Maximum value changed to 25MHz; 12) 3.3.16.2 Add external high-speed oscillator XTAL accuracy metrics and modify C_{L1} and C_{L2} descriptions; 13) 3.3.16.3 Add external low-speed oscillator XTAL32 accuracy indicator, modify C_{L1}

		and $_{CL2}$ related descriptions.
Rev1.4	2022/03/09	Company Logo updated.
Rev1.41	2022/03/29	1) 3.3.13 USB Interface Characteristics $_{RPD}$ Delete MAX, MIN values and add Typ value 15k Ω; 3.3.16 $_{tSU (XTAL)}$ startup time Delete maximum value, add typical value 2) 4.1 LQFP100/LQFP64/LQFP48 b MAX value is revised to 0.27.
Rev1.42	2022/09/14	1) 2.1 In the pinout diagram of each package, "PH0/XTAL_IN" is changed to "PH0/XTAL_EXT/XTAL_EXT". XTAL_IN" is changed to "PH0/ XTAL_EXT/ XTAL_OUT", and "PH1/ XTAL_OUT" is modified as follows "PH1/ XTAL_IN", QFN60 pinout style modified, new QFN48 pinout; 2.2 "PH0/ XTAL_IN" is modified to "PH0/ XTAL_EXT/ XTAL_OUT" and "PH1/ XTAL_OUT" is modified to "PH1/ XTAL_IN"; 2.3 "XTAL_OUT" changed to "XTAL_EXT/ XTAL_OUT", added Description of "XTAL_EXT External clock input"; 2) 3.3.16.1 Amend "XTAL_IN" to "XTAL_EXT"; 3.3.16.2 The "XTAL_IN" and "XTAL_OUT" pins in Figure 3-17 are connected to each other. Change the name; 3.3.18 Change the 10uF capacitor value in Figure 3-21 to 1uF.

Rev1.5	2023/09/27	1) Product Features Corrects the rate of the ADC; 2) 1 Introduction Correct the rate of the ADC; 3) 1.4.16 Correct the ADC rate; 4) 2.4 Table 2-6 Supplemental Pin Descriptions; 5) 3.2 Temperature for correcting thermal characteristics; 6) 3.3.7 Correct Table 3-19 I/O Static Characterization Parameters; 7) 3.3.10 Correct Table 3-24 I2C Electrical Characterization Parameters; 8) 3.3.11 Correct Table 3-25 SPI Electrical Characteristics Diagram Connection, add SPI timing diagram; 9) 4.4 Modified Package Thermal Resistance Coefficient Content Description.