HDSC 华大半导体 HUADA SEMICONDUCTOR

HC32F460 Series

32-bit ARM® Cortex® -M4 Microcontrollers

HC32F460PETB-LQFP100

HC32F460KETA-LQFP64

HC32F460KEUA-QFN60TR

HC32F460JETA-LQFP48

HC32F460JEUA-QFN48TR

Data Sheet

Product Features

ARM Cortex-M4 32bit MCU+FPU, 210DMIPS, 512KB Flash, 192KB SRAM, USB FS (Device/Host) 14 Timers, 2 ADCs, 1 PGA, 3 CMPs, 20 communication interfaces

- ARMv7-M architecture 32bit Cortex-M4 CPU with integrated FPU, MPU, DSP with SIMD instruction support, and CoreSight standard debug unit. Maximum operating main frequency of 168MHz, Flash acceleration unit for 0-wait program execution, up to 210DMPIS or 485Coremarks computing performance
- Built-in memory
  - Up to 512KByte Flash memory with security protection and data encryption*1
  - Up to 192KByte of SRAM, including 32KByte of 168MHz single-cycle access high-speed RAM, 4KByte of Retention RAM
- Power, clock, reset management
  - System power supply (Vcc) 1.8-3.6V
  - 6 independent clock sources: external master clock crystal (4-24MHz) external sub crystal (32.768kHz) internal high speed RC (16/20MHz) internal medium speed RC (8MHz) internal low speed RC (32kHz) internal WDT dedicated RC (10kHz)
  - Includes Power-On Reset (POR) Low Voltage Detect Reset （14 reset sources, including LVDR, Port Reset (PDR), each with individual flag bits
- Low power operation
  - Peripheral functions can be turned off or on independently
  - Three low-power modes: Sleep, Stop, Power down Mode
  - Run mode and Sleep mode support high-speed mode, ultra-low speed mode between the switch
  - Standby power consumption: Stop mode typ.90uA@25°C, Power down mode as low as 1.8uA@25°C
  - Power down mode, supports 16 port wake-up, ultra-low power RTC operation, 4KByte SRAM for data retention
  - Standby fast wake-up, Stop mode wake-up as fast as 2us, Power down mode wake-up as fast as 20us
- Peripheral operation support system significantly reduces CPU processing load
  - 8-channel dual host DMAC

  - DMAC for USBFS
  - Data Computing Unit (DCU)
  - Support peripheral event inter-triggering (AOS)
- High Performance Simulation
  - 2 independent 12bit 2MSPS ADCs
  - 1 programmable gain amplifier (PGA)
  - 3 independent voltage comparators (CMP) supporting 2 internal reference voltages
  - 1 on-chip temperature sensor (OTS)
- Timer
  - 3 multifunctional 16bit PWM timers (Timer6)
  - 3 x 16bit Motor PWM Timer (Timer4)
  - 6 x 16bit Universal Timer (TimerA)
  - 2 x 16bit base Timer (Timer0)
- Maximum 83 GPIOs
  - CPU single-cycle access, 100MHz maximum output
  - Maximum 81 5V-tolerant IO
- Up to 20 communication interfaces
  - 3 I2C, SMBus protocol support
  - 4 USARTs, supports ISO7816-3 protocol
  - 4 SPI
  - 4 I2S, built-in audio PLL supports audio-level sampling accuracy
  - 2 SDIOs supporting SD/MMC/eMMC formats
  - 1 QSPI with 168Mbps high-speed access (XIP)
  - 1 CAN, supports ISO 11898-1 standard protocol
  - 1 USB 2.0 FS, built-in PHY, Device/Host support
- Data encryption function
  - AES/HASH/TRNG
- Package form:
  LQFP100 (14×14mm) LQFP64 (10×10mm)
  QFN60 (7×7mm) QFN48 (5×5mm)
  LQFP48 (7×7mm)

*1: For specific specifications of *Flash* security protection and data encryption, please consult the sales window.

Preface Introduction

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1 Overview

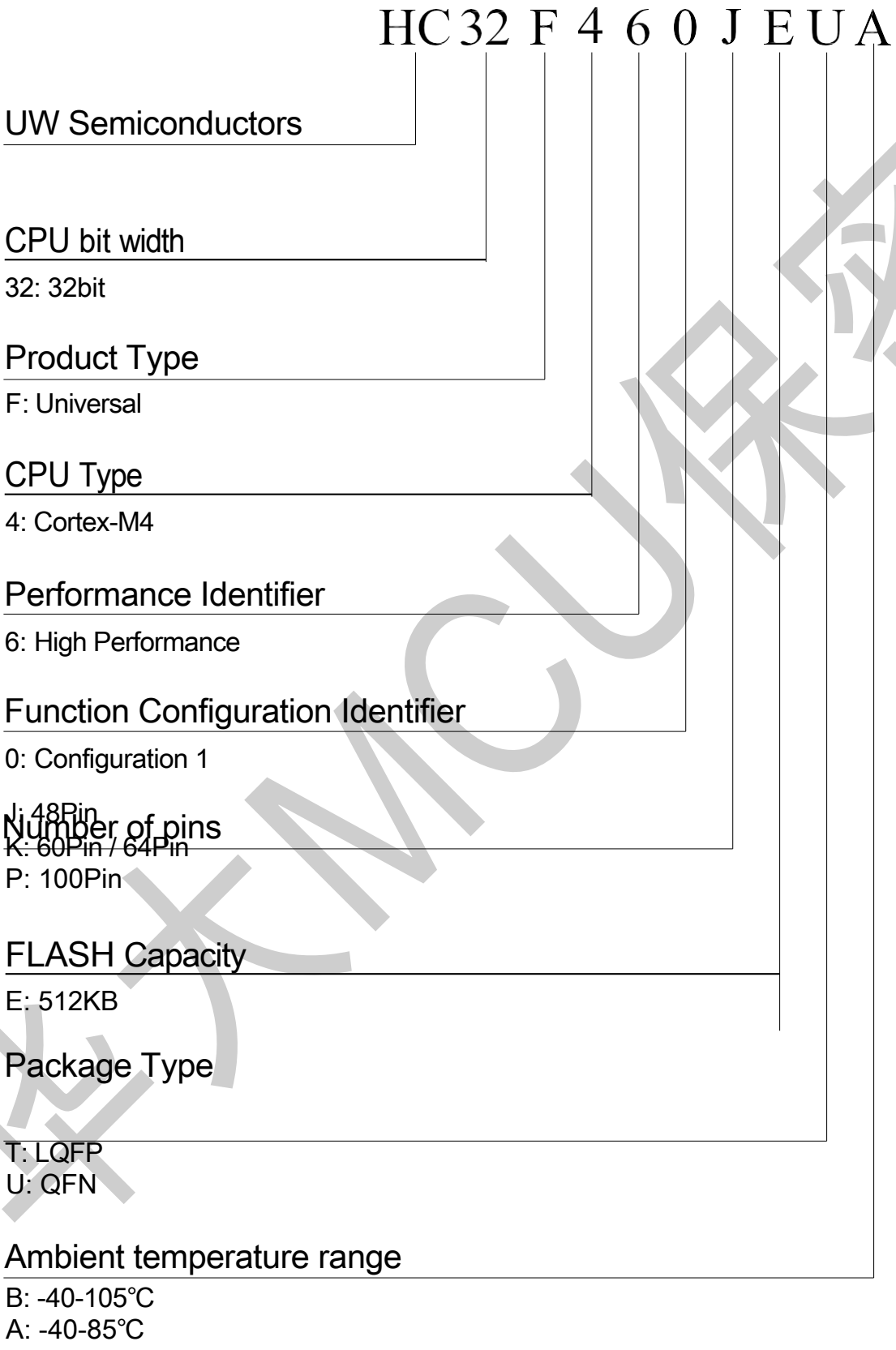
The HC32F460 series is a high-performance MCU based on the ARM® Cortex®-M4 32-bit RISC CPU operating at up to 168 MHz. The Cortex-M4 core integrates a floating-point unit (FPU) and DSP for single-precision floating-point arithmetic operations, supports all ARM single-precision data processing instructions and data types, and supports the full DSP instruction set. The core integrates the MPU unit and overlays the DMAC dedicated MPU unit to ensure the security of system operation. The HC32F460 series integrates high-speed on-chip memory, including up to 512KB of Flash and up to 192KB of SRAM, and an integrated Flash access acceleration unit for single-cycle program execution on Flash by the CPU. The polled bus matrix supports multiple bus hosts to access memory and peripherals simultaneously to improve operational performance. Bus hosts include CPU, DMA, USB dedicated DMA, etc. In addition to the bus matrix, it supports data transfer between peripherals, basic arithmetic operations and event triggering, which can significantly reduce the CPU's transaction processing load.

The HC32F460 series integrates a rich set of peripheral functions. It includes two independent 12bit 2MSPS ADCs, one gain adjustable PGA, three voltage comparators (CMP), three multi-function 16bit PWM timers (Timer6) supporting 6 complementary PWM outputs, three motor PWM timers (Timer4) supporting 18 complementary PWM outputs, six 16bit general-purpose timers (TimerA) supports 3 3-phase quadrature coded inputs and 48 Duty independent configurable PWM outputs, 11 serial communication interfaces (I2C/UART/SPI) 1 QSPI interface, 1 CAN, 4 I2S supporting audio PLL, 2 SDIO, 1 USB FS Controller with on-chip FS PHY supporting Device/ Host. The HC32F460 series supports wide voltage range (1.8-3.6V) wide temperature range (-40-105°C) and various low power modes, switch between high speed mode (8-168MHz) and ultra low speed mode (<8MHz) in Run mode and Sleep mode. Supports fast wake-up in low-power mode, up to 2us for STOP mode and up to 20us for Power Down mode.

Typical Applications

The HC32F460 series is available in 48pin, 64pin, 100pin LQFP packages and 48pin, 60pin QFN packages for high performance motor inverter control, smart hardware, IoT connectivity modules, etc.

1.1 Model naming rules



1.2 Model Function Comparison Table

Function		Product Model			
		HC32F460PETB	HC32F460KETA	HC32F460KEUA	HC32F460JExx
Number of pins		100	64	60	48
Number of GPIOs		83	52	50	38
Number of 5V Tolerant GPIOs		81	50	48	36
Package		LQFP	LQFP	QFN	LQFP/QFN
Temperature range		-40-105℃	-40-85℃		
Power supply voltage range		1.8 ~ 3.6 V			
Memory	Flash	512KB			
	OTP	960Byte			
	SRAM	192KB			
DMA		2unit * 4ch			
External port interrupts		EIRQ * 16vec + NMI * 1ch			
Communcation Interfaces (The minimum number of IOs required per ch is in parentheses)	UART	4ch (2)			
	SPI	4ch (3)			
	I2C	3ch (2)			
	I2S	4ch (3)			
	CAN	1ch (2)			
	QSPI	1ch (6)			
	SDIO	2ch (3)			
	USB-FS	1ch (2)			
Timers	Timer0	2unit			
	TimerA	6unit			
	Timer4	3unit			
	Timer6	3unit			
	WDT	1ch			
	SWDT	1ch			
	RTC	1ch			
Analog	12bit ADC	2unit , 16ch	2unit, 16ch	2unit, 15ch	2unit, 10ch
	PGA	1ch			
	CMP	3ch			
	OTS	√			
AES128		√			
HASH (SHA256)		√			

TRNG	√
Frequency Monitoring Module (FCM)	√
Programmable voltage detection function (PVD)	√
Debugging Interface	SWD

	JTAG

Table 1-1 Model Function Comparison Table

1.3 Functional Block Diagram

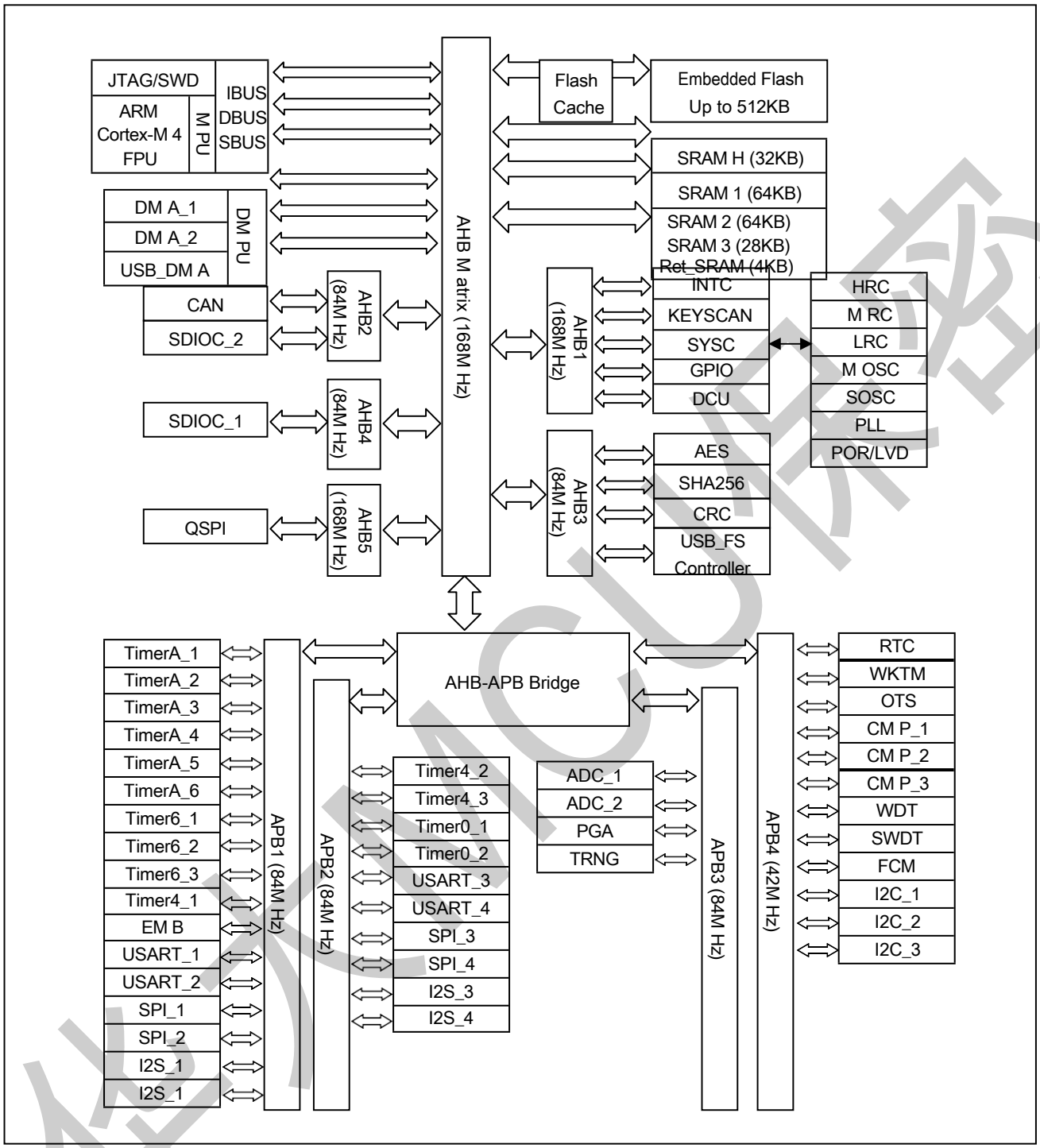


Figure 1-1 Functional Block Diagram

1.4 Function Introduction

1.4.1 CPU

The HC32F460 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit lean instruction CPU, which provides excellent computing performance and fast interrupt response with low pin count and low power consumption. The CPU supports DSP instructions for efficient signal processing operations and complex algorithms. The single point precision FPU unit avoids instruction saturation and accelerates software development.

1.4.2 Bus Architecture (BUS)

The master system consists of a 32-bit multi-layer AHB bus matrix that interconnects the following host and slave buses Host Bus

- Cortex-M4F Core CPUI Bus, CPUD Bus, CPUS Bus
- System DMA_1 bus, System DMA_2 bus
- USB DMA Bus

Slave Bus

- Flash ICODE Bus
- Flash DCODE Bus
- Flash MCODE bus (bus for hosts other than the CPU to access Flash)
- SRAMH bus (SRAMH 32kB)
- SRAMA bus (SRAM1 64KB)
- SRAMB bus (SRAM2 64KB, SRAM3 28KB, Ret_SRAM 4KB)
- APB1 Peripheral Bus (EMB/Timers/SPI/USART/I2S)
- APB2 Peripheral Bus (Timers/SPI/USART/I2S)
- APB3 Peripheral Bus (ADC/PGA/TRNG)
- APB4 Peripheral Bus (FCM/WDT/CMP/OTS/RTC/WKTM/I2C)
- AHB1 Peripheral bus (KEYSCAN/INTC/DCU/GPIO/SYSC)
- AHB2 Peripheral Bus (CAN/SDIOC)
- AHB3 Peripheral Bus (AES/HASH/CRC/USB FS)

- AHB4 Peripheral Bus (SDIOC)
- AHB5 Peripheral Bus (QSPI)

With the help of the bus matrix, efficient concurrent access from the host bus to the slave bus is possible.

1.4.3 Reset control (RMU)

The chip is configured with 14 reset methods.

- Power-On Reset (POR)
- NRST Pin Reset (NRST)
- Undervoltage Reset (BOR)
- Programmable Voltage Detect 1 Reset (PVD1R)
- Programmable voltage detection 2 reset (PVD2R)
- Watchdog Reset (WDTR)
- Dedicated watchdog reset (SWDTR)
- Power-down wake-up reset (PDRST)
- Software Reset (SRST)
- MPU Error Reset (MPUR)
- RAM Parity Reset (RAMPR)
- RAMECC reset (RAMECCR)
- Clock abnormal reset (CKFER)
- External high-speed oscillator abnormal stop reset (XTALER)

1.4.4 Clock Control (CMU)

The clock control unit provides clock functions for a range of frequencies, including: an external high-speed oscillator, an external low-speed oscillator, two PLL clocks, an internal high-speed oscillator, an internal medium-speed oscillator, an internal low-speed oscillator, a SWDT dedicated internal low-speed oscillator, clock prescaler, clock multiplexing, and clock gating circuitry.

The Clock Control Unit also provides a clock frequency measurement function (FCM)

The clock frequency measurement circuit uses the measurement reference clock to monitor and measure the measurement object clock. An interrupt or reset occurs when

the set range is exceeded.

The AHB, APB and Cortex-M4 clocks are all derived from the system clock, which can be sourced from a choice of six clock sources:

1) External high-speed oscillator (XTAL)
2) External low-speed oscillator (XTAL32)
3) MPLL Clock (MPLL)
4) Internal high-speed oscillator (HRC)
5) Internal medium speed oscillator (MRC)
6) Internal low speed oscillator (LRC)

The system clock can run at a maximum frequency of 168MHz.SWDT has a separate clock source: SWDT dedicated internal low-speed oscillator (SWDTLRC) The Real Time Clock (RTC) uses an external low-speed oscillator or an internal low-speed oscillator as clock source. 48MHz clock for USB-FS, optional system clock, MPLL, UPLL as clock source for I2S communication clock.

For each clock source, it can be turned on and off individually when not in use to reduce power consumption.

1.4.5 Power Control (PWC)

The power controller is used to control the power supply, switching, and detection of multiple power domains of the chip in multiple operation modes and low power modes.

The power controller consists of a power consumption control logic (PWC), and a power supply voltage detection unit (PVD).

The chip operates from 1.8 V to 3.6 V. The voltage regulator (LDO) supplies power to the VDD and VDDR domains, and the VDDR voltage regulator (RLDO) supplies power to the VDDR domain in power-down mode. The chip provides two operating modes, high speed and ultra-low speed, and three low power modes, sleep, stop and power down, through the power control logic (PWC).

The power supply voltage detection unit (PVD) provides power-on reset (POR), power-down reset (PDR), under-voltage reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2), etc. Among them, POR, PDR, BOR control the chip reset action by detecting the VCC voltage. PVD2 generates reset or interrupt by detecting VCC voltage or external input detection voltage, and generates reset or interrupt by register selection.

The VDDR area can maintain power through RLDO after the chip enters power-down mode, ensuring that the real-time clock module (RTC) and wake-up timer (WKTM) can continue to operate and maintain data in the 4KB low-power SRAM (Ret-SRAM). The analog module is equipped with dedicated power supply pins to improve analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x00000400H~0x0000041FH (where

0x00000408~0x0000041F is the reserved function address, the 24byte address needs to be set by the user to ensure the chip action is normal) to load the data into the initialization configuration register, the user needs to program or erase the FLASH sector 0 to modify the initialization configuration register.

1.4.7 Embedded FLASH Interface (EFM)

The FLASH interface provides access to FLASH via AHB I-CODE and D-CODE to perform programming, erase and full erase operations on FLASH; accelerates code execution through instruction prefetch and cache mechanisms.

Main features:

- 512KByte FLASH space
- I-CODE Bus 16Byte Prefetch
- Shared 64 caches (1Kbyte) on the I-CODE and D-CODE buses
- Provides 960Bbyte One Time Programming Area (OTP)
- Supports low-power read operations
- Support guide exchange function
- Support security protection and data encryption*1

  *1: For specific specifications of Flash security protection and data encryption, please consult the sales window.

1.4.8 Internal SRAM (SRAM)

This product has 4KB power-down mode retention SRAM (Ret_SRAM) and 188KB system SRAM (SRAMH/SRAM1/ SRAM2/SRAM3)

SRAM can be accessed by byte, half-word (16-bit), or full-word (32-bit). Read and write operations are performed at CPU speed, with the possibility of inserting wait cycles.

Ret_SRAM provides 4KB of data retention space in power down mode.

SRAM3 with ECC checking (Error Checking and Correcting) ECC checking is to correct one error and check two errors; SRAMH/SRAM1/SRAM2/Ret_SRAM with parity checking

(Even-parity check) with one check bit per byte of data.

1.4.9 General Purpose IO (GPIO)

GPIO Key Features:

- 16 I/O pins per port group, may be less than 16 depending on actual configuration
- Support pull-up
- Support push-pull, open-drain output mode
- Supports high, medium and low drive modes
- Inputs supporting external interrupts
- Support I/O pin peripheral function multiplexing, up to 16 selectable multiplexed functions per I/O pin, up to 64 selectable functions for some I/Os
- Each I/O pin can be programmed independently
- Each I/O pin can be selected to have 2 functions active at the same time (2 output functions active at the same time are not supported)

1.4.10 Interrupt Control (INTC)

The functions of the interrupt controller (INTC) are to select interrupt event requests as interrupt inputs to the NVIC to wake up the WFI, and as event inputs to wake up the WFE. select interrupt event requests as wake-up conditions for low-power modes (sleep mode and stop mode); interrupt control functions for the external pins NMI and EIRQ; and interrupt/event selection functions for software interrupts.

Main specifications:

1) NVIC interrupt vectors: Please refer to 12.3.1 Interrupt Vector Table for the actual number of interrupt vectors used (excluding the 16 interrupt lines of the Cortex™-M4F), each interrupt vector can select the corresponding peripheral interrupt event request according to the Interrupt Select Register. For more information on exceptions and NVIC programming, please refer to Chapter 5: Exceptions and Chapter 8: Nested Vector Interrupt Controllers in the ARM Cortex™-M4F Technical Reference Manual.
2) Programmable priority: 16 programmable priority levels (4-bit interrupt priority used)
3) Non-maskable interrupts: In addition to the NMI pin as the source of non-maskable interrupts, multiple system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event request is equipped with independent enable selection, hang, and clear hang register.

4) Equipped with 16 external pin interrupts.
5) Configure multiple peripheral interrupt event requests, please refer to the interrupt event request sequence number list for details.
6) Equipped with 32 software interrupt event requests.
7) The interrupt can wake up the system in sleep mode and stop mode.

1.4.11 Keyboard scanning (KEYSCAN)

KEYSCAN module supports keypad row scan, and the combination with external interrupt IRQ can realize key recognition function, which can support 16*8 keypad array at maximum.

1.4.12 Storage Protection Unit (MPU)

The MPU provides protection for memory and can improve system security by blocking unauthorized access. Four host-specific MPU units and one IP-specific MPU unit are built into this product.

The ARM MPU provides CPU access control to the full 4G address space.

The DMA MPU (DMPU) provides DMA_1/DMA_2/USB FS DMA control of read and write access to the full 4G address space. The MPU action can be set to ignore/bus error/non-maskable interrupt/reset when an access to the prohibited space occurs.

The IP MPU provides access control to the system IP and security-related IPs when in unprivileged mode.

1.4.13 DMA Controller (DMA)

DMA is used to transfer data between memory and peripheral function modules, enabling data exchange between memory, between memory and peripheral function modules, and between peripheral function modules without CPU involvement.

- The DMA bus is independent of the CPU bus and is transmitted according to the AMBA AHB-Lite bus protocol
- 8 independent channels (4 channels each for DMA_1 and DMA_2) allowing independent operation of different DMAs

  Transfer function
- The start request source for each channel is configured via a separate trigger source selection register
- One block of data is transferred per request
- Data blocks can be as small as 1 data, up to 1024 data
- Each data can be configured as 8bit, 16bit or 32bit

- Up to 65535 transmissions can be configured
- Source and destination addresses can be independently configured as fixed, incremental, decremental, cyclic or jump with specified offsets
- Three types of interrupts can be generated, block transfer completion interrupt, transfer completion interrupt, and transfer error interrupt. Each of these interrupts can be configured to be masked or not. The block transfer completion and transfer completion can be used as event output and as trigger source input for other peripheral modules with hardware trigger function.

- Support chain transfer function, which can transfer multiple data blocks in one request
- Support external events to trigger channel reset
- Can be set to enter module stop state when not in use to reduce power consumption

1.4.14 Voltage Comparator (CMP)

The CMP is a peripheral module that compares two analog voltages, INP and INM, and outputs the result of the comparison.The CMP has 3 independent comparison channels, each with 4 input sources for the analog voltages INP and INM. It is possible to select an INP for a single comparison with an INM or to scan multiple INPs with the same INM. The comparison results can be read from registers, output to external pins, and generate interrupts and events.

1.4.15 Analog-to-digital converters (ADCs)

The 12-bit ADC is an analog-to-digital converter that uses successive approximation. It has a maximum of 16 analog input channels and can convert both external ports and internal analog signals. These channels can be combined in any sequence for successive scan conversion, and the sequence can be converted in a single, or continuous scan. The ADC module is equipped with an analog watchdog function that monitors the conversion results of any given channel and detects if the user-set threshold value is exceeded.

ADC Key Features

- High Performance
  - Configurable for 12-, 10-, and 8-bit resolution
  - The frequency ratio between the peripheral clock PCLK4 and the A/D converter clock ADCLK can be selected as follows:
    - PCLK4: ADCLK = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4
    - ADCLK can be selected as a PLL asynchronous to the system clock HCLK, where the clock source of PCLK4 and ADCLK are fixed as PLL at the same time, and the frequency ratio is 1:1, and the original dividing

frequency setting is invalid

- 2MSPS (PCLK4=ADCLK=60MHz, 12-bit, sampling 17 cycles)
- Independent programming of sampling time for each channel
- Independent data register for each channel
- Data register configurable data alignment
- Continuous multiple conversion averaging function

  - Analog watchdog to monitor conversion results
  - The ADC module can be set to stop when not in use
- Analog input channels
  - Up to 16 external analog input channels
  - 1 internal reference voltage
- Conversion start conditions
  - Software Settings Conversion Start
  - Peripheral peripheral synchronization triggers the start of the transition
  - External pins trigger the start of conversion
- Conversion Mode
  - 2 scan sequences A and B, single or multiple channels can be specified at will
  - Sequence A Single Scan
  - Sequence A Continuous Scan
  - Double sequence scanning, sequence A, B independent selection of trigger source, sequence B priority than A
  - Synchronous mode (for devices with two or three ADCs)
- Interrupt and event signal output
  - Sequence A End of Scan Interrupt EOCA_INT and Event EOCA_EVENT
  - Sequence B End of Scan Interrupt EOCB_INT and Event EOCB_EVENT
  - Analog watchdog channel comparison interrupt CHCMP_INT and event CHCMP_EVENT, sequence comparison interrupt SEQCMP_INT and event SEQCMP_EVENT
  - Each of the above 4 events can initiate DMA

1.4.16 Temperature Sensor (OTS)

The OTS can acquire the temperature inside the chip to support reliable operation of the system. After temperature measurement is initiated using software or hardware triggers, the OTS provides a set of temperature-dependent digital quantities that can be calculated using a formula to obtain the temperature value.

1.4.17 Advanced Control Timer (Timer6)

The Advanced Control Timer 6 (Timer6) is a 16-bit count width high performance timer that can be used to count different forms of clock waveforms for output for external use. The timer supports both triangle waveform and sawtooth waveform modes.

The Timer6 can generate various PWM waveforms, software synchronous counting and hardware synchronous counting between units, cache function for each reference register, 2-phase quadrature encoding and 3-phase quadrature encoding, and EMB control. Timer6 with 3 units is included in this series.

1.4.18 Universal control timer (Timer4)

The Universal Control Timer 4 (Timer4) is a timer module for three-phase motor control, providing a variety of three-phase motor control solutions for different applications. The timer supports both triangle waveform and sawtooth waveform modes, generates various PWM waveforms, supports cache function, and supports EMB control. This series is equipped with 3 units of Timer4.

1.4.19 Emergency Brake Module (EMB)

The emergency brake module is to notify the timer when certain conditions are met so that the timer stops outputting PWM to the external motor.

Function module for signals, the following events are used to generate notifications:

- External port input level change
- PWM output port level occurs in phase (same high or same low)
- Voltage comparator comparison results
- External oscillator stops oscillating
- Write register software control

1.4.20 General purpose timer (TimerA)

Universal Timer A (TimerA) is a timer with 16-bit count width and 8 PWM outputs. The timer supports two waveform modes, triangle waveform and sawtooth waveform, and can generate various PWM waveforms; it supports software synchronous start counting; the comparison reference value register supports cache function; and it supports 2-phase quadrature coding counting and 3-phase quadrature coding counting. This series is equipped with 6 units of TimerA, which can achieve a maximum of 48 PWM outputs.

1.4.21 General purpose timer (Timer0)

The general-purpose Timer0 is a basic timer that allows both synchronous counting and asynchronous counting. The timer contains 2 channels and can generate a compare match event during counting. This event can trigger an interrupt or be used as an event output to control other modules, etc. Timer0 of 2 units is installed in this series.

1.4.22 Real Time Clock (RTC)

The Real Time Clock (RTC) is a counter that stores time information in BCD code format. It records the specific calendar time from 00 to 99 years. Supports both 12/24 hour time systems and automatically calculates the number of days based on the month and year 28, 29
(leap year) 30 and 31.

1.4.23 Watchdog counter (WDT)

There are two watchdog counters, a dedicated watchdog counter (SWDT) whose count clock source is a dedicated internal RC (WDTCLK:10KHz), and a general purpose watchdog counter (WDT) whose count clock source is PCLK4. The dedicated watchdog and general purpose watchdog are 16-bit decrementing counters used to monitor for software faults resulting from deviations from normal operation of the application due to external disturbances or unforeseen logic conditions.

Both watchdogs support the window function. The window interval can be preset before the count starts, and when the count value is in the window interval, the counter can be refreshed and the count starts again.

1.4.24 Serial communication interface (USART)

This product is equipped with four units of the serial communication interface module (USART). The serial communication interface module (USART) enables flexible full-duplex data exchange with external devices; the USART supports a universal asynchronous serial communication interface
(UART), clock synchronous communication interface, smart card interface (ISO/IEC7816-3). Supports modem operation (CTS/RTS operation), multi-processor operation.

1.4.25 Integrated Circuit Bus (I2C)

This product is equipped with 3 units of Integrated Circuit Bus (I2C), which is used

as an interface between the microcontroller and the I2C serial bus. It provides multi-master mode function and can control all I2C bus protocols and arbitration. Standard mode and fast mode are supported.

1.4.26 Serial Peripheral Interface (SPI)

This product is equipped with a 4-channel serial peripheral interface SPI, which supports high-speed full-duplex serial synchronous transmission for easy data exchange with peripheral devices. The user can set the 3-wire/4-wire, master/slave and baud rate range as required.

1.4.27 Four-wire serial peripheral interface (QSPI)

The Quad Wire Serial Peripheral Interface (QSPI) is a memory control module used to communicate with serial ROMs with SPI-compatible interfaces. The targets include serial Flash, serial EEPROM and serial FeRAM.

1.4.28 Integrated circuitry with built-in audio bus (I2S)

I2S (Inter_IC Sound Bus) the integrated circuit's built-in audio bus, is dedicated to data transfer between audio devices. This product is equipped with 4 I2S and has the

Function	Main Features
Communication method	• Supports full-duplex and half-duplex communications • Supports master mode or slave mode operation
Data Format	• Selectable channel length: 16/32 bit • Optional transmission data length: 16/24/32 bits • Data shift order: MSB start
Baud rate	• 8-bit programmable linear prescaler for accurate audio sampling frequency • Support sampling frequency 192k, 96k, 48k, 44.1k, 32k, 22.05k, 16k, 8k • Output drive clock to drive external audio components at a fixed rate of 256*Fs (Fs is the audio sampling frequency)
I2S protocol support	• I2S Philips Standard • MSB Alignment Standards • LSB Alignment Standards • PCM Standards
Data buffering	• Input and output FIFO buffers with 2 words deep and 32 bits wide
Clock source	• Internal I2SCLKs (UPLLR/UPLLQ/UPLLP/MPLLR/MPLLQ/MPLLP) can be used; they can also be used by The external clock on the I2S_EXCK pin provides
	• Generate an interrupt when the effective space in the transmit buffer reaches the

1.4.29 CAN communication interface (CAN)

This product is equipped with one unit of CAN communication interface module (CAN) and 512Byte of RAM for CAN to store transmit/receive messages. The CAN2.0B protocol according to ISO11898-1 and the TTCAN protocol according to ISO11898-

4 are supported.

1.4.30 USB 2.0 Full Speed Module (USB FS)

The USB FS is a dual role (DRD) controller that supports both slave and host functions.

The USB FS supports both full-speed and low-speed transceivers in master mode, while only full-speed transceivers are supported in slave mode.

The USB FS module equipped with this product successfully sends SOF tokens in host mode or successfully receives SOF tokens in slave mode.

SOF events can be generated when a token is generated.

1.4.31 Cryptographic Coprocessing Module (CPM)

The Cryptographic Co-Processing Module (CPM) consists of three sub-modules: AES Encryption and Decryption Algorithm Processor, HASH Secure Hash Algorithm, and TRNG True Random Number Generator.

The AES encryption and decryption algorithm processor follows standard data encryption and decryption standards and can perform encryption and decryption operations with 128-bit key length.

The HASH secure hash algorithm is the SHA-2 version of the SHA-256 (Secure Hash Algorithm) which complies with the national standard "FIPS PUB 180-3" published by the National Bureau of Standards and Technology, and can produce 256-bit message digest output for messages up to 2^64 bits in length. message digest output for messages up to 2^64 bits in length.

TRNG True Random Number Generator is a random number generator based on continuous analog noise, providing 64bit random numbers.

1.4.32 Data Computing Unit (DCU)

The Data Computing Unit (DCU) is a module that simply processes data without the help of a CPU. Each DCU unit has 3 data registers, and is capable of adding, subtracting, and comparing the size of 2 data, as well as window comparison functions. The product is equipped with 4 DCU units, each of which can perform its own functions independently.

1.4.33 CRC Calculation Unit (CRC)

The CRC algorithm of this module follows the definition of ISO/IEC13239 and uses 32-bit and 16-bit CRC respectively.

The generating polynomial is $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$. CRC16

The generating polynomial is $X^{16}+X^{12}+X^{5}+1$.

1.4.34 SDIO Controller (SDIOC)

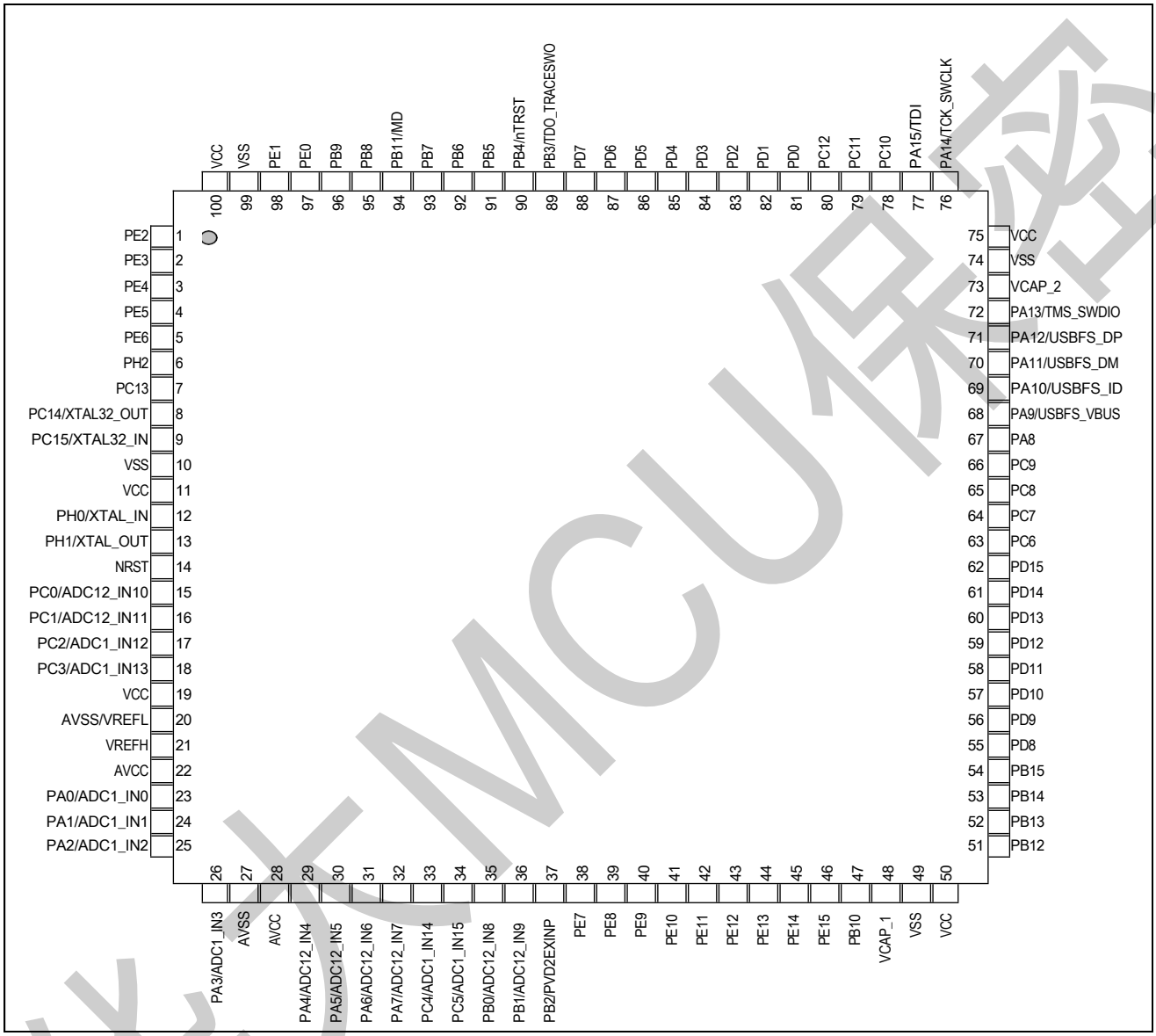
The SDIO controller is the host in the SD/SDIO/MMC communication protocol. The product has 2 SDIO controllers, each providing a host interface for communication with SD cards supporting SD2.0 protocol, SDIO devices and MMC devices supporting eMMC4.51 protocol. SDIOC features are as follows:

- Support SDSC, SDHC, SDXC format SD cards and SDIO devices
- Supports one-wire (1bit) and four-wire (4bit) SD buses
- Supports one-wire (1bit), four-wire (4bit) and eight-wire (8bit) MMC buses
- With card recognition and hardware write protection

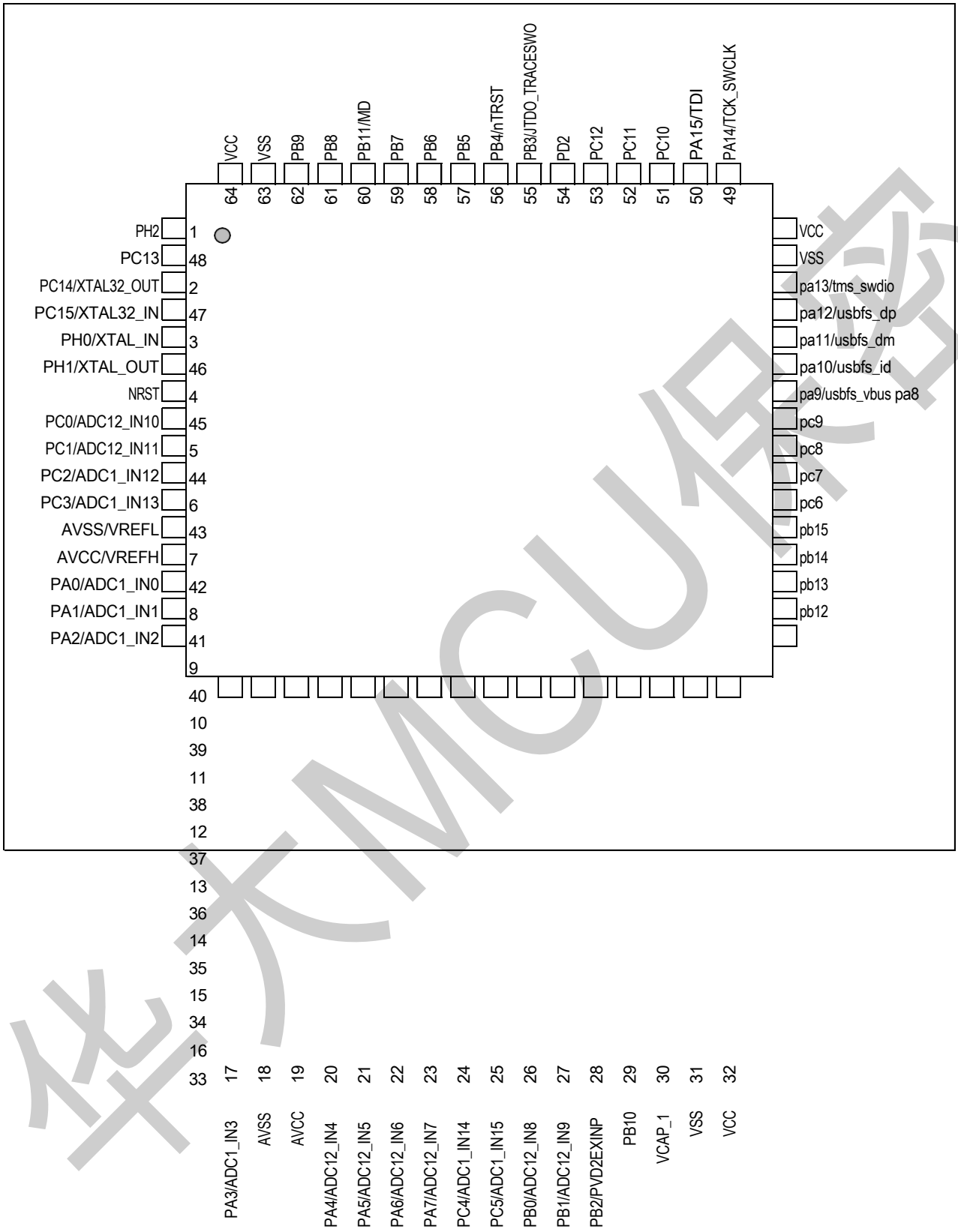
2 Pin Configuration and Function (Pinouts)

2.1 Pin Configuration Diagram

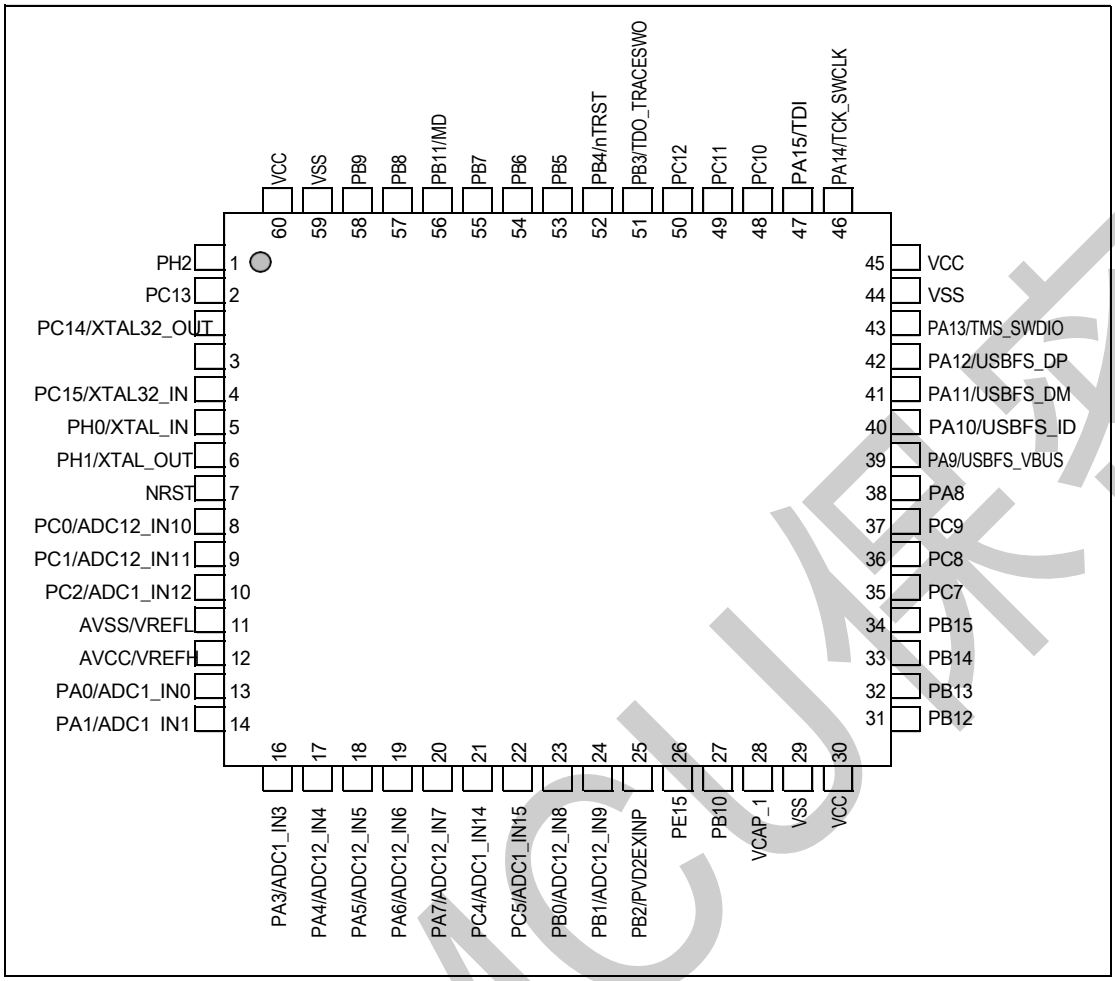
HC32F460PETB-LQFP100



HC32F460KETA-LQFP64



HC32F460ZEUA-QFN60TR



HC32F460JETA-LQFP48 / HC32F460JEUA-QFN48TR

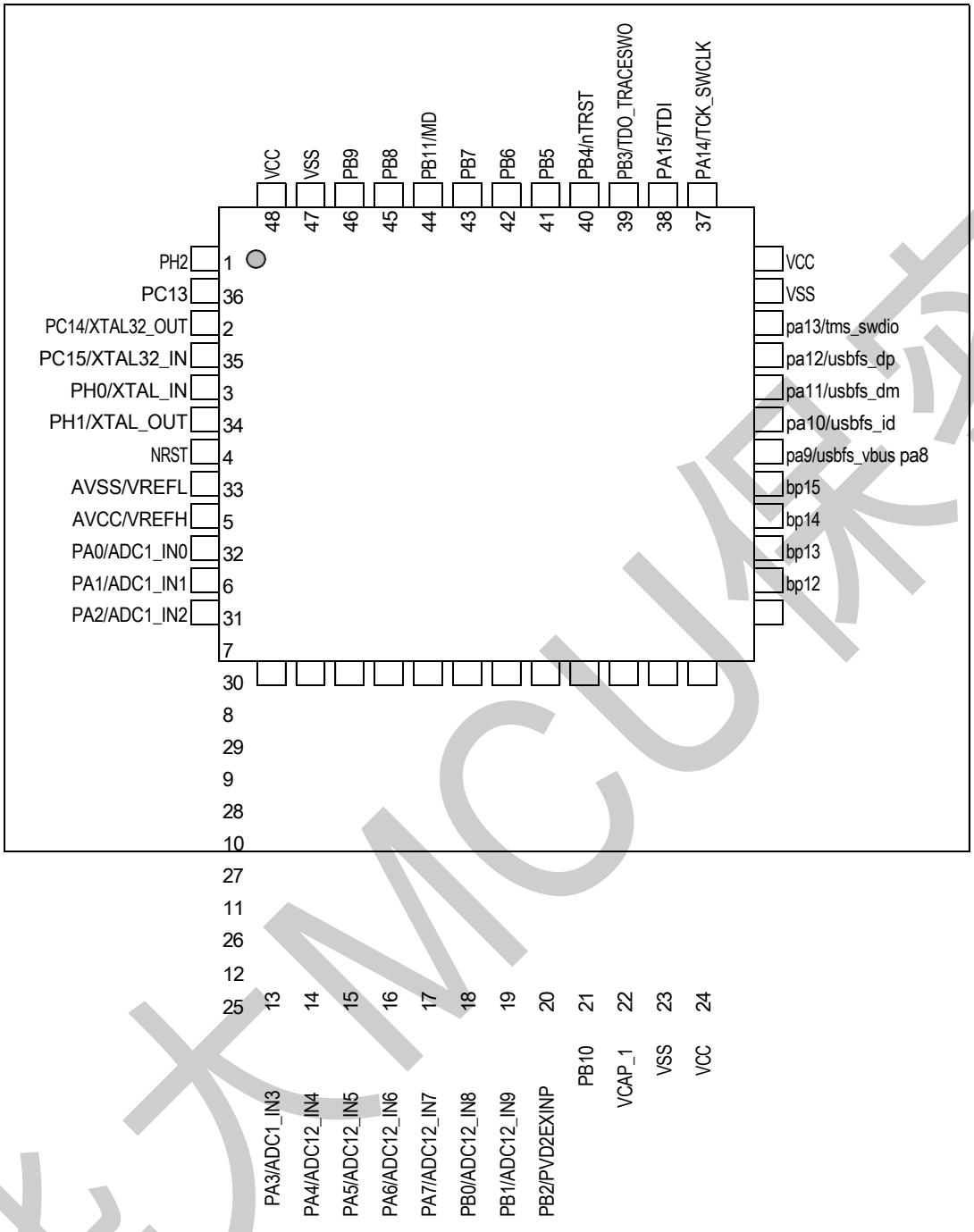


Figure 2-1 Package diagram

2.2 Pin List

LQFP100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WK UP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
								GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
1	-	-	-	PE2		EIRQ2	TRACECLK	GPO				TIMA_3_PWM5			USART3_CK								EVENTOUT		Func_Grp2
2	-	-	-	PE3		EIRQ3	TRACEDATA0	GPO				TIMA_3_PWM6			USART4_CK								EVENTOUT		Func_Grp2
3	-	-	-	PE4		EIRQ4	TRACEDATA1	GPO				TIMA_3_PWM7											EVENTOUT		Func_Grp2
4	-	-	-	PE5		EIRQ5	TRACEDATA2	GPO				TIMA_3_PWM8											EVENTOUT		Func_Grp2
5	-	-	-	PE6		EIRQ6	TRACEDATA3	GPO															EVENTOUT		Func_Grp2
6	1	1	1	PH2		EIRQ2		GPO	FCMREF	TIM4_2_CLK		TIMA_4_PWM7		EMB_IN4			SDIO2_D4	I2S3_EXCK					EVENTOUT		Func_Grp2
7	2	2	2	PC13		EIRQ13		GPO	RTC_OUT			TIMA_4_PWM8					SDIO2_CK	I2S3_MCK				EVNTP313			Func_Grp2
8	3	3	3	PC14	XTAL32_OUT	EIRQ14		GPO				TIMA_4_PWM5										EVNTP314			
9	4	4	4	PC15	XTAL32_IN	EIRQ15		GPO				TIMA_4_PWM6										EVNTP315			
10	-	-	-	VSS																					
11	-	-	-	VCC																					
12	5	5	5	PH0	XTAL_IN	EIRQ0		GPO					TIMA_5_PWM3												
13	6	6	6	PH1	XTAL_OUT	EIRQ1		GPO					TIMA_5_PWM4												
14	7	7	7	NRST																					
15	8	8	-	PC0	ADC12_IN10/CMP3_INP3	EIRQ0		GPO				TIMA_2_PWM5					SDIO2_D5					EVNTP300	EVENTOUT		Func_Grp1
16	9	9	-	PC1	ADC12_IN11	EIRQ1		GPO				TIMA_2_PWM6					SDIO2_D6					EVNTP301	EVENTOUT		Func_Grp1
17	10	10	-	PC2	ADC1_IN12	EIRQ2		GPO				TIMA_2_PWM7		EMB_IN3			SDIO2_D7					EVNTP302	EVENTOUT		Func_Grp1
18	11	-	-	PC3	ADC1_IN13/CMP1_INM2	EIRQ3		GPO				TIMA_2_PWM8					SDIO1_WP					EVNTP303	EVENTOUT		Func_Grp1
19	-	-	-	VCC																					
20	12	11	8	AVSS																					
21	-	-	-	VREFH																					
22	13	12	9	AVCC																					
23	14	13	10	PA0	ADC1_IN0/CMP1_INP1	EIRQ0/WKUP0_0		GPO		TIM4_2_OUH		TIMA_2_PWM1/TIMA_2_CLKA		TIMA_2_TRIG	SPI1_SS1		SDIO2_D4					EVNTP100	EVENTOUT		Func_Grp1
24	15	14	11	PA1	ADC1_IN1/CMP1_INP2	EIRQ1		GPO		TIM4_2_OUL		TIMA_2_PWM2/TIMA_2_CLKB	TIMA_3_TRIG		SPI1_SS2		SDIO2_D5					EVNTP101	EVENTOUT		Func_Grp1

LQFP100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
								GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
25	16	15	12	PA2	ADC1_IN2/CMP1_INP3	EIRQ2		GPO		TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM1/TIMA_5_CLKA		SPI1_SS3		SDIO2_D6					EVNTP102	EVENTOUT		Func_Grp1
26	17	16	13	PA3	ADC1_IN3/PGAVSS/CMP1_INP4	EIRQ3		GPO		TIM4_2_OVL		TIMA_2_PWM4	TIMA_5_PWM2/TIMA_5_CLKB				SDIO2_D7					EVNTP103	EVENTOUT		Func_Grp1
27	18	-	-	AVSS																					
28	19	-	-	AVCC																					
29	20	17	14	PA4	ADC12_IN4/CMP2_INP1/CMP3_INP4	EIRQ4		GPO		TIM4_2_OWH			TIMA_3_PWM5		USART2_CK	KEYOUT0		I2S1_EXCK				EVNTP104	EVENTOUT		Func_Grp1
30	21	18	15	PA5	ADC12_IN5/CMP2_INP2	EIRQ5		GPO		TIM4_2_OWL		TIMA_2_PWM1/TIMA_2_CLKA	TIMA_3_PWM6	TIMA_2_TRIG		KEYOUT1		I2S1_MCK				EVNTP105	EVENTOUT		Func_Grp1
31	22	19	16	PA6	ADC12_IN6/CMP2_INP3	EIRQ6		GPO					TIMA_3_PWM1/TIMA_3_CLKA	EMB_IN2		KEYOUT2	SDIO1_CMD					EVNTP106	EVENTOUT		Func_Grp1
32	23	20	17	PA7	ADC12_IN7/CMP1_INM1/CMP2_INM1/CMP3_INM1	EIRQ7		GPO		TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5	TIMA_3_PWM2/TIMA_3_CLKB	EMB_IN3		KEYOUT3	SDIO2_WP					EVNTP107	EVENTOUT		Func_Grp1
33	24	21	-	PC4	ADC1_IN14/CMP2_INM2	EIRQ4		GPO		TIM4_2_OUH			TIMA_3_PWM7		USART1_CK		SDIO2_CD					EVNTP304	EVENTOUT		Func_Grp1
34	25	22	-	PC5	ADC1_IN15/CMP3_INM2	EIRQ5		GPO		TIM4_2_OUL			TIMA_3_PWM8				SDIO2_CMD					EVNTP305	EVENTOUT		Func_Grp1
35	26	23	18	PB0	ADC12_IN8/CMP3_INP1	EIRQ0		GPO		TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6	TIMA_3_PWM3		USART4_CK	KEYOUT4	SDIO2_CMD					EVNTP200	EVENTOUT		Func_Grp1
36	27	24	19	PB1	ADC12_IN9/CMP3_INP2	EIRQ1/WKUP0_1		GPO		TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_3_PWM4		QSPI_QSSN	KEYOUT5	SDIO2_D3	I2S2_EXCK				EVNTP201	EVENTOUT		Func_Grp1
37	28	25	20	PB2	PVD2EXINP	EIRQ2/WKUP0_2		GPO	VCOUT123		TIM6_TRIGB	TIMA_1_PWM8		EMB_IN1	QSPI_QSIO3		SDIO2_D2	I2S2_MCK				EVNTP202	EVENTOUT		Func_Grp1
38	-	-	-	PE7		EIRQ7		GPO	ADTRG1		TIM6_TRIGA	TIMA_1_TRIG			USART1_CK								EVENTOUT		
39	-	-	-	PE8		EIRQ8		GPO		TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5											EVENTOUT		
40	-	-	-	PE9		EIRQ9		GPO		TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA											EVENTOUT		
41	-	-	-	PE10		EIRQ10		GPO		TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6											EVENTOUT		
42	-	-	-	PE11		EIRQ11		GPO		TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB											EVENTOUT		
43	-	-	-	PE12		EIRQ12		GPO		TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7			SPI1_SS1								EVENTOUT		Func_Grp2

LQFP100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
								GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
44	-	-	-	PE13		EIRQ13		GPO		TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3			SPI1_SS2								EVENTOUT		Func_Grp2
45	-	-	-	PE14		EIRQ14		GPO		TIM4_1_CLK		TIMA_1_PWM4			SPI1_SS3		SDIO1_CD						EVENTOUT		Func_Grp2
46	-	26	-	PE15		EIRQ15		GPO				TIMA_1_PWM8	TIMA_5_TRIG	EMB_IN2	USART4_CK		SDIO1_WP						EVENTOUT		Func_Grp2
47	29	27	21	PB10		EIRQ10		GPO	ADTRG2	TIM4_2_OVH		TIMA_2_PWM3	TIMA_5_PWM8		QSPI_QSIO2		SDIO1_D7	I2S3_EXCK				EVNTP210	EVENTOUT		Func_Grp2
48	30	28	22	VCAP_1																					
49	31	29	23	VSS																					
50	32	30	24	VCC																					
51	33	31	25	PB12		EIRQ12		GPO	VCOUT1	TIM4_2_OVL	TIM6_TRIGB	TIMA_1_PWM8		EMB_IN2	QSPI_QSIO1		SDIO2_D1	I2S3_MCK				EVNTP212	EVENTOUT		Func_Grp2
52	34	32	26	PB13		EIRQ13		GPO	VCOUT2	TIM4_1_OUL	TIM6_1_PWMB	TIMA_1_PWM5			QSPI_QSIO0		SDIO2_D0					EVNTP213	EVENTOUT		Func_Grp2
53	35	33	27	PB14		EIRQ14		GPO	VCOUT3	TIM4_1_OVL	TIM6_2_PWMB	TIMA_1_PWM6			QSPI_QSCK		SDIO1_D6					EVNTP214	EVENTOUT		Func_Grp2
54	36	34	28	PB15		EIRQ15		GPO	RTC_OUT	TIM4_1_OWL	TIM6_3_PWMB	TIMA_1_PWM7	TIMA_6_TRIG	EMB_IN4	USART3_CK		SDIO1_CK					EVNTP215	EVENTOUT		Func_Grp2
55	-	-	-	PD8		EIRQ8		GPO		TIM4_3_OUL			TIMA_6_PWM1/TIMA_6_CLKA		QSPI_QSIO0	KEYOUT7						EVNTP408	EVENTOUT		Func_Grp2
56	-	-	-	PD9		EIRQ9		GPO		TIM4_3_OVL			TIMA_6_PWM2/TIMA_6_CLKB		QSPI_QSIO1	KEYOUT6						EVNTP409	EVENTOUT		Func_Grp2
57	-	-	-	PD10		EIRQ10		GPO		TIM4_3_OWL			TIMA_6_PWM3		QSPI_QSIO2	KEYOUT5						EVNTP410	EVENTOUT		Func_Grp2
58	-	-	-	PD11		EIRQ11		GPO		TIM4_3_CLK			TIMA_6_PWM4		QSPI_QSIO3	KEYOUT4						EVNTP411	EVENTOUT		Func_Grp2
59	-	-	-	PD12		EIRQ12		GPO				TIMA_4_PWM1/TIMA_4_CLKA	TIMA_5_PWM5									EVNTP412	EVENTOUT		
60	-	-	-	PD13		EIRQ13		GPO				TIMA_4_PWM2/TIMA_4_CLKB	TIMA_5_PWM6									EVNTP413	EVENTOUT		
61	-	-	-	PD14		EIRQ14		GPO				TIMA_4_PWM3	TIMA_5_PWM7									EVNTP414	EVENTOUT		
62	-	-	-	PD15		EIRQ15		GPO				TIMA_4_PWM4	TIMA_5_PWM8									EVNTP415	EVENTOUT		
63	37	-	-	PC6		EIRQ6		GPO				TIMA_3_PWM1/TIMA_3_CLKA	TIMA_5_PWM8		QSPI_QSCK	KEYOUT3	SDIO1_D6					EVNTP306	EVENTOUT		Func_Grp2
64	38	35	-	PC7		EIRQ7		GPO		TIM4_2_CLK		TIMA_3_PWM2/TIMA_3_CLKB	TIMA_5_PWM7		QSPI_QSSN	KEYOUT2	SDIO1_D7	I2S2_EXCK				EVNTP307	EVENTOUT		Func_Grp2
65	39	36	-	PC8		EIRQ8		GPO		TIM4_2_OWH		TIMA_3_PWM3	TIMA_5_PWM6		USART3_CK	KEYOUT1	SDIO1_D0	I2S2_MCK				EVNTP308	EVENTOUT		Func_Grp2
66	40	37	-	PC9		EIRQ9		GPO	MCO_2	TIM4_2_OWL		TIMA_3_PWM4	TIMA_5_PWM5			KEYOUT0	SDIO1_D1					EVNTP309	EVENTOUT		Func_Grp1
67	41	38	29	PA8		EIRQ8/WKUP2_0		GPO	MCO_1	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA			USART1_CK		SDIO1_D1	USBFS_SOF				EVNTP108	EVENTOUT		Func_Grp1

LQFP100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
								GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
68	42	39	30	PA9		EIRQ9/WKUP2_1		GPO		TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB					SDIO1_D2	USBFS_VBUS				EVNTP109	EVENTOUT		Func_Grp1
69	43	40	31	PA10		EIRQ10/WKUP2_3		GPO		TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3	TIMA_5_TRIG				SDIO1_CD	USBFS_ID				EVNTP110	EVENTOUT		Func_Grp1
70	44	41	32	PA11		EIRQ11/WKUP2_4		GPO		TIM4_1_CLK		TIMA_1_PWM4		EMB_IN1			SDIO2_CD	USBFS_DM				EVNTP111	EVENTOUT		Func_Grp1
71	45	42	33	PA12		EIRQ12/WKUP3_0		GPO		TIM4_3_OWL	TIM6_TRIGA	TIMA_1_TRIG	TIMA_6_PWM1/TIMA_6_CLKA				SDIO2_WP	USBFS_DP				EVNTP112	EVENTOUT		Func_Grp1
72	46	43	34	PA13		EIRQ13/WKUP3_1	TMS_SWDIO	GPO				TIMA_2_PWM5	TIMA_6_PWM2/TIMA_6_CLKB		SPI2_SS1		SDIO2_D3					EVNTP113	EVENTOUT		Func_Grp1
73	-	-	-	VCAP_2																					
74	47	44	35	VSS																					
75	48	45	36	VCC																					
76	49	46	37	PA14		EIRQ14/WKUP3_2	TCK_SWCLK	GPO				TIMA_2_PWM6	TIMA_6_PWM3	TIMA_4_TRIG	SPI2_SS2		SDIO2_D2	I2S1_EXCK				EVNTP114	EVENTOUT		Func_Grp1
77	50	47	38	PA15		EIRQ15/WKUP3_3	TDI	GPO				TIMA_2_PWM1/TIMA_2_CLKA	TIMA_6_PWM4	TIMA_2_TRIG	SPI2_SS3		SDIO2_D1	I2S1_MCK				EVNTP115	EVENTOUT		Func_Grp1
78	51	48	-	PC10		EIRQ10		GPO		TIM4_3_OUH		TIMA_2_PWM7	TIMA_5_PWM1/TIMA_5_CLKA				SDIO1_D2					EVNTP310	EVENTOUT		Func_Grp1
79	52	49	-	PC11		EIRQ11		GPO		TIM4_3_OVH		TIMA_2_PWM8	TIMA_5_PWM2/TIMA_5_CLKB				SDIO1_D3					EVNTP311	EVENTOUT		Func_Grp1
80	53	50	-	PC12		EIRQ12		GPO		TIM4_3_OWH		TIMA_4_TRIG	TIMA_5_PWM3				SDIO1_CK					EVNTP312	EVENTOUT		Func_Grp1
81	-	-	-	PD0		EIRQ0		GPO	VCOUT123				TIMA_5_PWM4									EVNTP400	EVENTOUT		Func_Grp1
82	-	-	-	PD1		EIRQ1		GPO				TIMA_3_TRIG	TIMA_6_PWM5									EVNTP401	EVENTOUT		Func_Grp1
83	54	-	-	PD2		EIRQ2		GPO				TIMA_2_PWM4	TIMA_6_PWM6				SDIO1_CMD					EVNTP402	EVENTOUT		Func_Grp1
84	-	-	-	PD3		EIRQ3		GPO	VCOUT1				TIMA_6_PWM7									EVNTP403	EVENTOUT		
85	-	-	-	PD4		EIRQ4		GPO	VCOUT2				TIMA_6_PWM8									EVNTP404	EVENTOUT		
86	-	-	-	PD5		EIRQ5		GPO	VCOUT3													EVNTP405	EVENTOUT		
87	-	-	-	PD6		EIRQ6		GPO							USART2_CK							EVNTP406	EVENTOUT		
88	-	-	-	PD7		EIRQ7		GPO							USART2_CK							EVNTP407	EVENTOUT		
89	55	51	39	PB3		EIRQ3/WKUP0_3	TDO_TRACESWO	GPO	FCMREF	TIM4_3_CLK		TIMA_2_PWM2/TIMA_2_CLKB	TIMA_6_PWM5				SDIO2_D0					EVNTP203	EVENTOUT		Func_Grp2
90	56	52	40	PB4		EIRQ4/WKUP1_0	nTRST	GPO		TIM4_3_OWL		TIMA_3_PWM1/TIMA_3_CLKA	TIMA_6_PWM6				SDIO1_D0					EVNTP204	EVENTOUT		Func_Grp2
91	57	53	41	PB5		EIRQ5/WKUP1_1		GPO		TIM4_3_OWH		TIMA_3_PWM2/TIMA_3_CLKB	TIMA_6_PWM7				SDIO1_D3	I2S4_EXCK				EVNTP205	EVENTOUT		Func_Grp2

LQFP100	LQFP64	QFN60	LQFP/QFN48	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG/SWD	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16~31	Func32~63
								GPO	other	TIM4	TIM6	TIMA	TIMA	EMB,TIMA	USART/SPI/QSPI	KEY	SDIO	USBFS/I2S	-	-	-	EVNTPT	EVENTOUT	-	Communication Funcs
92	58	54	42	PB6		EIRQ6/WKUP1_2		GPO	ADTRG2	TIM4_3_OVL		TIMA_4_PWM1/TIMA_4_CLKA	TIMA_6_PWM8				SDIO2_CK	I2S4_MCK				EVNTP206	EVENTOUT		Func_Grp2
93	59	55	43	PB7		EIRQ7/WKUP1_3		GPO	ADTRG1	TIM4_3_OVH		TIMA_4_PWM2/TIMA_4_CLKB					SDIO1_D0					EVNTP207	EVENTOUT		Func_Grp2
94	60	56	44	PB11/MD		NMI																EVNTP211			
95	61	57	45	PB8		EIRQ8		GPO		TIM4_3_OUL		TIMA_4_PWM3				KEYOUT7	SDIO1_D4	USBFS_DRV VBUS				EVNTP208	EVENTOUT		Func_Grp2
96	62	58	46	PB9		EIRQ9		GPO		TIM4_3_OUH		TIMA_4_PWM4	TIMA_6_TRIG		SPI2_SS1	KEYOUT6	SDIO1_D5					EVNTP209	EVENTOUT		Func_Grp2
97	-	-	-	PE0		EIRQ0		GPO	MCO_1			TIMA_4_TRIG			SPI2_SS2								EVENTOUT		Func_Grp2
98	-	-	-	PE1		EIRQ1		GPO	MCO_2	TIM4_3_CLK					SPI2_SS3								EVENTOUT		Func_Grp2
99	63	59	47	VSS																					
100	64	60	48	VCC																					

Table 2-1 Pin Function Table

Notes:

- In the above table, there are 64 pins support Func32~63 function selection, Func32~63 mainly for serial communication function (including USART, SPI, I2C, I2S, CAN) divided into two groups Func_Grp1, Func_Grp2. Please refer to Table 2-2 for details.

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
Func_Grp 1	USART1_TX	USART1_RX	USART1_RTS	USART1_CTS	USART2_TX	USART2_RX	USART2_RTS	USART2_CTS	SPI1_MOSI	SPI1_MISO	SPI1_SS0	SPI1_SCK	SPI2_MOSI	SPI2_MISO	SPI2_SS0	SPI2_SCK
Func_Grp 2	USART3_TX	USART3_RX	USART3_RTS	USART3_CTS	USART4_TX	USART4_RX	USART4_RTS	USART4_CTS	SPI3_MOSI	SPI3_MISO	SPI3_SS0	SPI3_SCK	SPI4_MOSI	SPI4_MISO	SPI4_SS0	SPI4_SCK

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
Func_Grp 1	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2S1_SD	I2S1_SDIN	I2S1_WS	I2S1_CK	I2S2_SD	I2S2_SDIN	I2S2_WS	I2S2_CK				
Func_Grp 2	I2C3_SDA	I2C3_SCL	CAN_TxD	CAN_RxD	I2S3_SD	I2S3_SDIN	I2S3_WS	I2S3_CK	I2S4_SD	I2S4_SDIN	I2S4_WS	I2S4_CK				

Table 2-2 Func32~63 Table

Package	Port Group	Bits																Pin Count	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Total
LQFP100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	83
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP64	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	52
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	-	-	-	-	-	-	-	-	-	-	-	-	-	o	-	-	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
QFN60	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	50
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	-	o	o	-	o	o	o	14	
	PortE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	o	1	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
LQFP48	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	38
QFN48	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	-	-	-	-	-	-	-	-	-	-	-	-	-	3	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	o	3	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Table 2-3 Port Configuration

Port		Pull up	Open Drain Output	Drive Capability	5V withstand voltage	Remarks
PortA	PA0~PA10 PA13~PA15	Support	Support	Low,Medium, High	Support *	
	PA11, PA12	Support	Support	Low,Medium, High	Not supported	
PortB	PB0~PB10. PB12~PB15	Support	Support	Low,Medium, High	Support *	
	PB11	Support	-	-	Support	Input dedicated
PortC	PC0~PC15	Support	Support	Low,Medium, High	Support *	
PortD	PD0~PD15	Support	Support	Low,Medium, High	Support	
PortE	PE0~PE15	Support	Support	Low,Medium, High	Support	
PortH	PH0~PH2	Support	Support	Low,Medium, High	Support	

Table 2-4 General Function Specifications

Notes:

- When used for analog functions, the input voltage must not be higher than VREFH/AVCC.

2.3 Pin Function Description

Category	Function Name	I/O	Description
Power	VCC	I	Power supply
	VSS	I	Power Ground
	VCAP_1~2	IO	Kernel Voltage
	AVCC	I	Analog Power
	AVSS	I	Analog power ground
	VREFH	I	Analog Reference Voltage
	VREFL	I	Analog Reference Voltage
System	NRST	I	Reset Pin, Low Active
	MD	I	Mode Pins
PVD	PVD2EXINP	I	PVD2 External input comparison voltage
Clock	XTAL_IN	I	External master clock oscillator interface
	XTAL_OUT	O	
	XTAL32_IN	I	External sub-clock (32K) oscillator interface
	XTAL32_OUT	O	
	MCO_1~2	O	Internal clock output
GPIO	GPIOxy (x= A~E,H, y=0~15)	IO	General purpose inputs and outputs
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU Event Output
EIRQ	EIRQx (x=0~15)	I	Maskable external interrupts
	WKUPx_y (x,y=0~3)	I	PowerDown mode external wake-up input
	NMI	I	Non-maskable external interrupts
Event Port	EVNTPxy (x=1~4, y=0~15)	IO	Event port input and output function
Key	KEYOUTx(x=0~7)	O	KEYSCAN scan output signal
JTAG/SWD	TCK_SWCLK	I	Online debugging interface
	TMS_SWDIO	IO	
	TDO_TRACESWO	O	
	TDI	I	
	nTRST	I	
TRACE	TRACECLK	O	Track and debug synchronized clock output
	TRACEDATA0~3	O	Trace debug data output
FCM	FCMREF	I	External reference clock input for clock frequency meter measurement
RTC	RTCOUT	O	1Hz clock output

Timer4	TIM4_x_CLK	I	Counting clock port input

Category	Function Name	I/O	Description
(x=1~3)	TIM4_x_OUH	IO	PWM Port U Phase Output
	TIM4_x_OUL	IO	PWM Port U Phase Output
	TIM4_x_OVH	IO	PWM Port V Phase Output
	TIM4_x_OVL	IO	PWM Port V Phase Output
	TIM4_x_OWH	IO	PWM Port W Phase Output
	TIM4_x_OWL	IO	PWM Port W Phase Output
Timer6	TIM6_TRIGA	I	External event triggers A input
(x=1~3)	TIM6_TRIGB	I	External event triggers B input
	TIM6_x_PWMA	IO	External event trigger input or PWM port output
	TIM6_x_PWMB	IO	External event trigger input or PWM port output
TimerA	TIMA_x_TRIG	I	External event triggered input
(x=1~6)	TIMA_x_PWM1/TIMA_x_CLKA	IO	External event trigger input or PWM port output or count clock port output
	TIMA_x_PWM2/TIMA_x_CLKB	IO	External event trigger input or PWM port output or count clock port output
	TIMA_x_PWMy (y=3~8)	IO	External event trigger input or PWM port output
EMB	EMB_INx (x=1~4)	I	Groupx (x=1~4) port input control signal
USARTx	USARTx_TX	IO	Sending data
(x=1~4)	USARTx_RX	IO	Receiving data
	USARTx_CK	IO	Communication Clock
	USARTx_RTS	O	Request to send a signal
	USARTx_CTS	I	Clear send signal
SPIx	SPIx_MISO	IO	Master input/slave output data transfer pins
(x=1~4)	SPIx_MOSI	IO	Master output/slave input data transfer pins
	SPIx_SCK	IO	Transmission Clock
	SPIx_SS0	IO	Slave select input and output pins
	SPIx_SS1~3	O	Slave select output pins
QSPI	QSPI_QSIO0~3	IO	Data Cable
	QSPI_QSCK	O	Clock Output
	QSPI_QSSN	O	Slave Selection
I2Cx	I2Cx_SCL	IO	Clock Lines
(x=1~3)	I2Cx_SDA	IO	Data Cable
I2Sx	I2Sx_SD	IO	Serial Data
(x=1~4)	I2Sx_SDIN	I	Full duplex serial data input

I2Sx_WS	IO	Word selection
I2Sx_CK	IO	Serial Clock

Category	Function Name	I/O	Description
	I2Sx_EXCK	I	External clock source
	I2Sx_MCK	O	Master Clock
CAN	CAN_TxD	O	Sending data
	CAN_RxD	I	Receiving data
SDIOx	SDIOx_Dy (y=0~7)	IO	SD data signal
	SDIOx_CK	O	SD clock output signal
	SDIOx_CMD	IO	SD command and reply signals
	SDIOx_CD	I	SD card recognition status signal
	SDIOx_WP	I	SD card write protect status signal
USBFS	USBFS_DM	IO	USBFS on-chip full-speed PHY D-signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+ signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O	USBFS SOF pulse output signal
	USBFS_DRVVBUS	O	USBFS VBUS driver license signal
CMPx (x=1~3)	VCOUT1	O	Analog comparison channel 1 result output
	VCOUT2	O	Analog comparison channel 2 result output
	VCOUT3	O	Analog comparison channel 3 result output
	VCOUT123	O	Analog comparison channel 1~3 Result OR output
	CMPx_INPy	I	Analog comparator channel x positive voltage y input
	CMPx_INMy	I	Analog comparator channel x negative voltage y input
ADC	ADTRG1	I	ADC1 AD conversion external start source
	ADTRG2	I	ADC2 AD conversion external start-up source
	ADC1_INx (x=0~3,12~15)	I	ADC1 external analog input port
	ADC12_INx (x=4~11)	I	ADC1 and ADC2 share an external analog input port
	PGAVSS	I	PGA Ground input

Table 2-5 Pin Function Description

2.4 Pin Usage Instructions

Pin Name	Instructions for use
VCC	Power supply, connect 1.8V~3.6V voltage and connect decoupling capacitor with VSS pin nearby (refer to electrical characteristics)
VSS	Power ground, connected to 0V
VCAP_1~2	Kernel voltage, connect capacitor to VSS pin nearby to stabilize kernel voltage (refer to electrical characteristics)
AVCC	Analog power supply for analog module, connected to the same voltage as VCC (refer to electrical characteristics) When not using the analog module, please short the connection with VCC
AVSS/VREFL	Analog power ground/reference voltage, connected to the same voltage as AVSS (reference electrical characteristics) Shorted to VSS when not using analog module
VREFH	ADC1, ADC2 analog reference voltage, connected to a voltage not higher than AVCC when not using the ADC, please short with AVCC
PB11/MD	Mode input, fixed to the input state. This pin must be fixed high when the reset pin (NRST) is released (changed from low to high). Recommended connection resistor (4.7KΩ) to VCC (pull-up)
NRST	Reset pin, active low. Connect resistor to VCC (pull-up) when not in use
Pxy, x=A~E,H, y=0~15	General purpose pins. When used as input function, the input voltage should not exceed 5V. when used as analog input, the analog voltage should not exceed VREFH/AVCC Suspend when not in use, or connect resistor to VCC (pull-up)/VSS (pull-down)

Table 2-6 Pin Usage Description

3 Electrical Characteristics

3.1 Parameter Conditions

All voltages are referenced to VSS if not otherwise specified.

3.1.1 Minimum and maximum values

Unless otherwise noted, all device minimum and maximum values are guaranteed by design or characterization testing under worst-case ambient temperature, supply voltage, and clock frequency conditions.

3.1.2 Typical values

Unless otherwise noted, typical data is obtained by design or characterization testing at TA = 25 °C and VCC = 3.3 V.

3.1.3 Typical Curve

Unless otherwise noted, all typical curves are untested and are for design reference only.

3.1.4 Load capacitance

The load conditions used to measure the pin parameters are shown in Figure 3-1 (left).

3.1.5 Pin Input Voltage

The measurement of the input voltage on the device pins is shown in Figure 3-1 (right).

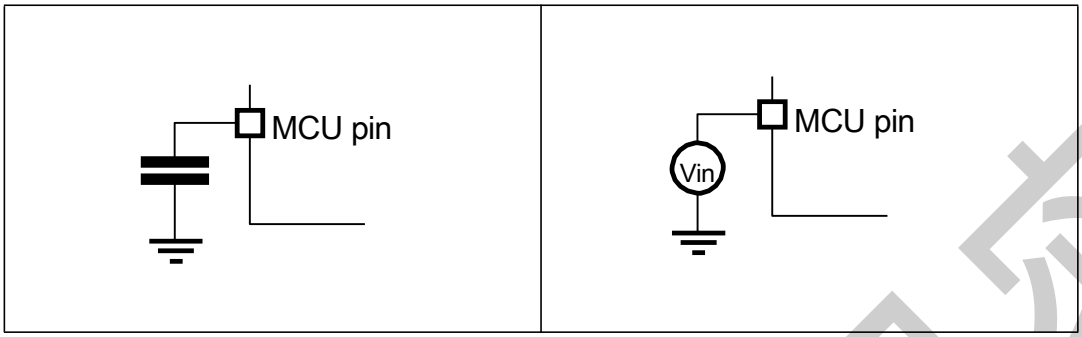


Figure 3-1 Pin load condition (left) and input voltage measurement (right)

3.1.6 Power Solutions

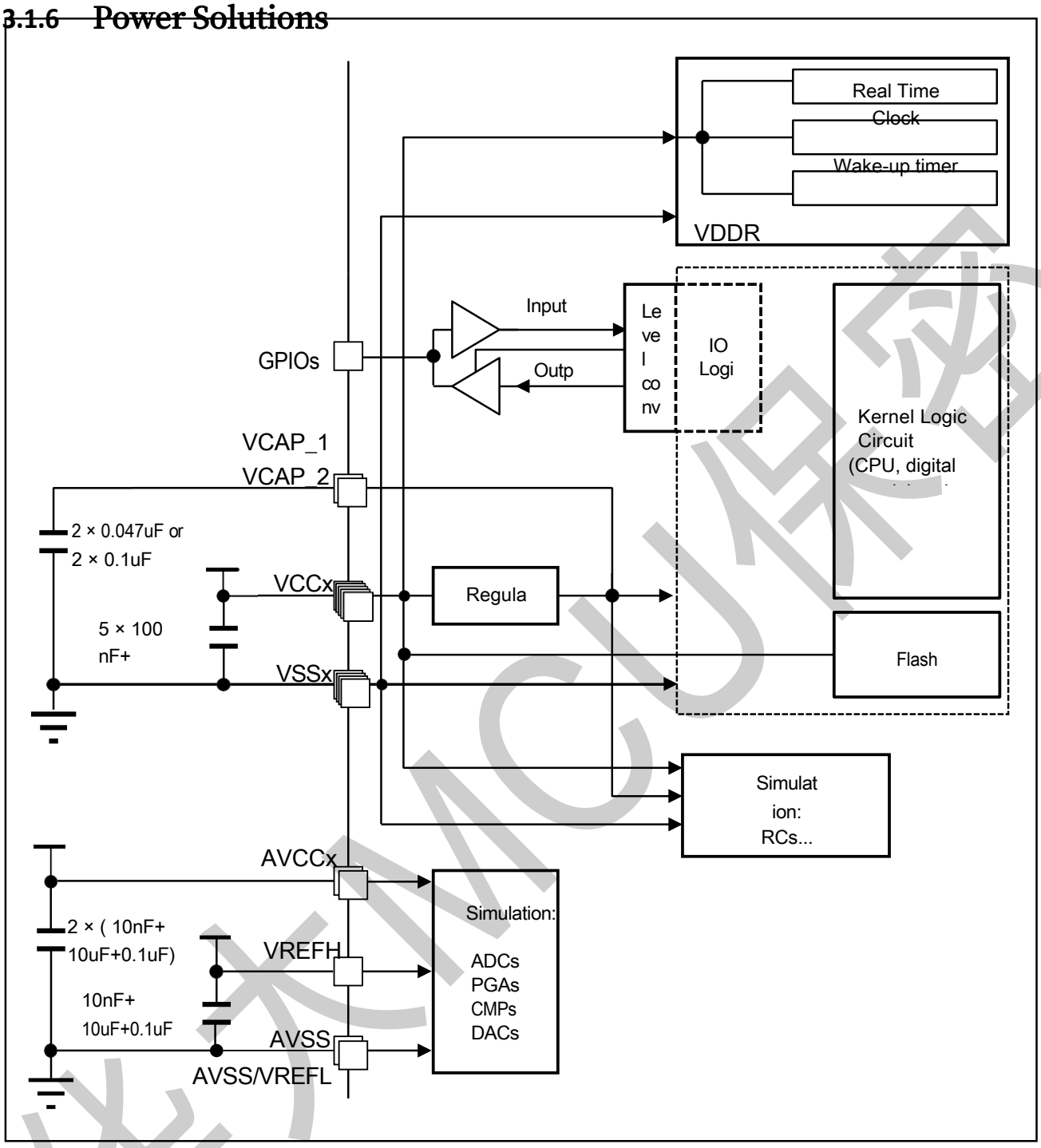


Figure 3-2 Power supply scheme (HC32F460PETB-LQFP100)

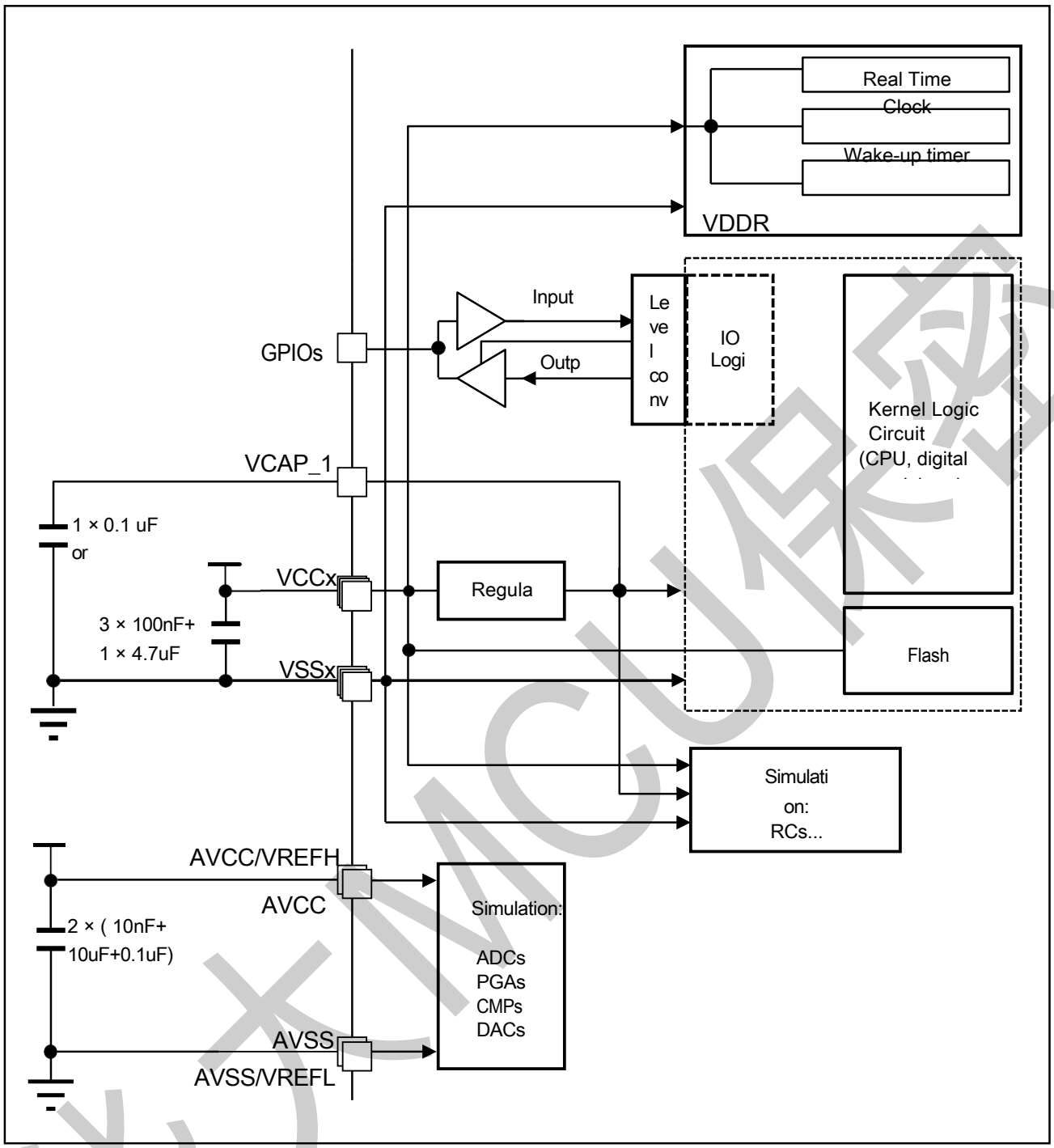


Figure 3-3 Power supply scheme (HC32F460KETA-LQFP64)

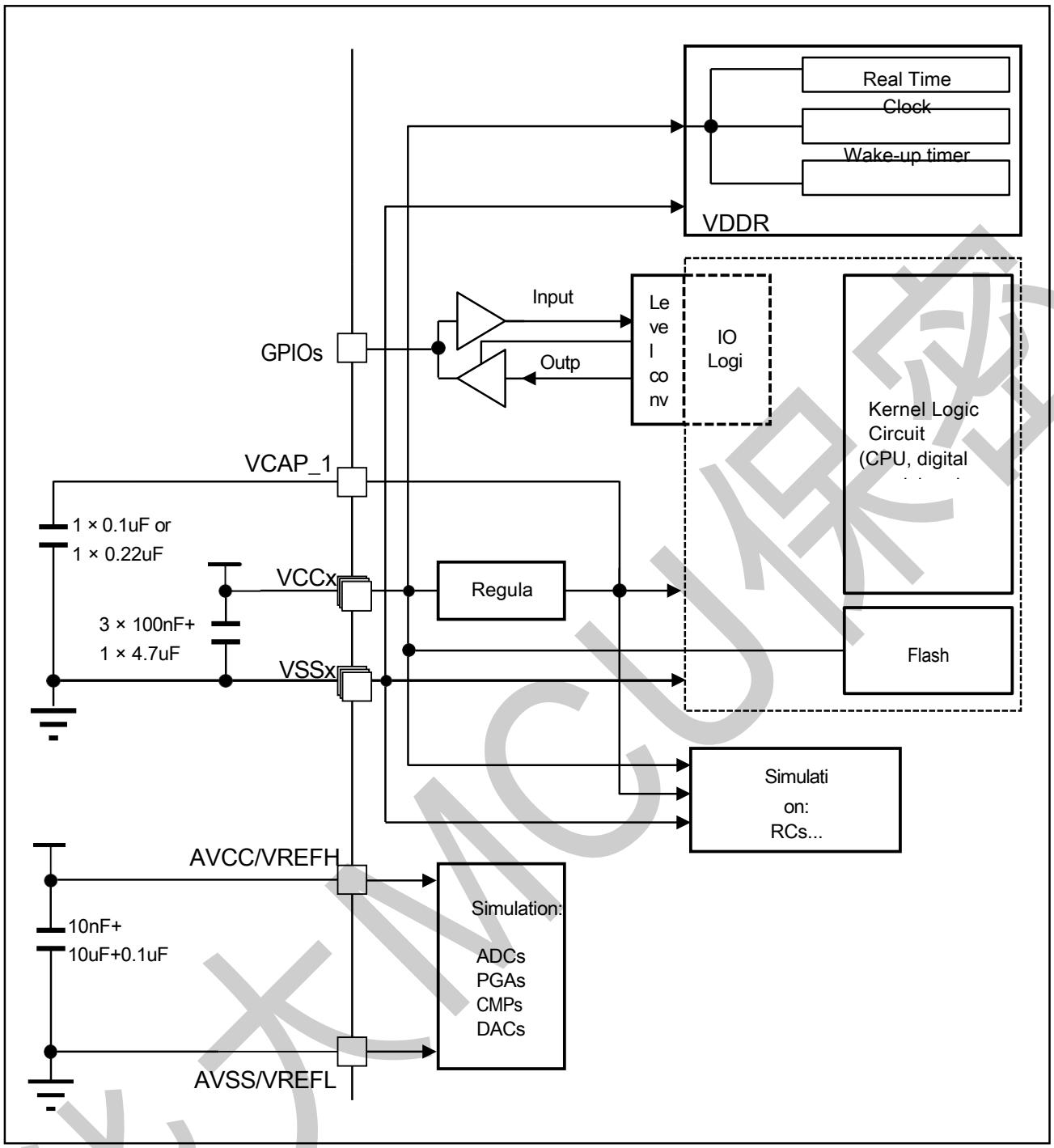


Figure 3-4 Power supply scheme (HC32F460ZEUA-QFN60TR, (HC32F460JETA-LQFP48/HC32F460JEUA-QFN48TR)

1. The 4.7μF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS = VSS.
3. Each power pair (e.g. VCC/VSS, AVCC/AVSS ...) must be decoupled using the filtering ceramic capacitors described above. These capacitors must be as close or as low as possible to the appropriate pins below the PCB to ensure proper device operation. It is not recommended to remove

the filtering capacitors to drop

Low PCB size or cost. This may cause the device to operate improperly.

4. The capacitors used for the VCAP_1/VCAP_2 pins are as follows: 1) For chips with both VCAP_1 and VCAP_2 pins, each pin can use 0.047uF or 0.1uF capacitance (total capacity is 0.094uF or 0.2uF) 2) For chips with only VCAP_1 pin, 0.1uF or 0.22uF capacitance can be used. capacitor. When waking up from power-down mode, VCAP_1/VCAP_2 needs to be charged during the core voltage build-up. On the one hand, a smaller total VCAP_1/VCAP_2 capacity reduces the charge time and brings fast response time to the application; on the other hand, a larger total VCAP_1/VCAP_2 capacity extends the charge time, but also provides better electromagnetic compatibility (EMC). The user can choose a larger or smaller capacitance value depending on the EMC and system response speed requirements. The total capacity of VCAP_1/VCAP_2 must match the value assigned to the PWR_PWRC3.PDTS bit. If the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, you need to make sure the PWR_PWRC3.PDTS bit is cleared before entering the power-down mode.

5. The stability of the main regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin, with the capacitance value CEXT determined according to the stability requirements of the system. The capacitance value CEXT and ESR requirements are as follows:

Symbols	Parameters	Conditions
CEXT	Capacitance value of external capacitor	0.047μF / 0.1μF / 0.22uF

Table 3-1 VCAP_1/VCAP_2 Operating Conditions

3.1.7 Current consumption measurement

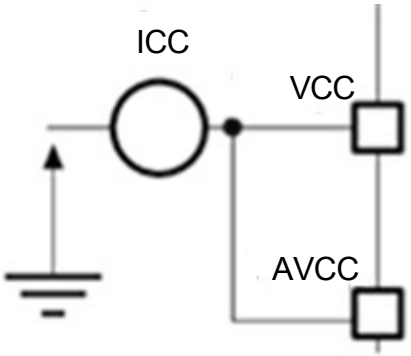


Figure 3-5 Current consumption measurement scheme

3.2 Absolute maximum rating

If the loads applied to the device exceed the absolute maximum ratings listed in Table 3-2 Voltage Characteristics, Table 3-3 Current Characteristics, and Table 3-4 Thermal Characteristics, the device may be permanently damaged. These values are rated stresses only and do not imply that the device functions properly under these conditions. Prolonged operation at maximum rated conditions may affect the reliability of the device.

Symbols	Projects	Minimum value	Maximum value	Unit
VCC-VSS	External mains voltage (including AVCC, VCC)(1)	-0.3	4.0	V
VIN	The input voltage on the 5V withstand voltage pin (2)	VSS-0.3	VCC+4.0 (max. 5.8V)	

Table 3-2 Voltage Characteristics

1. All mains (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the allowed limits.
2. The maximum value of V_{IN} must always be followed. See Table 3-3 for information on the maximum allowable injection current values.

Symbols	Projects	Maximum value	Unit
ΣIVCC	Total current flowing into all VCCx power lines (pull current)(1)	240	mA
ΣIVSS	Total current flowing out of all VSSx grounding lines (potting current) (1)	-240	
IVCC	Maximum current flowing into each VCCx power line (pull current) (1)	100	
IVSS	Maximum current flowing out of each VSSx grounding line (potting current) (1)	-100	
IIO	Output supply current for any I/O and control pins	40	
	Output pull current for arbitrary I/O and control pins	-40	
ΣIIO	Total output supply current on all I/O and control pins	120	
	Total output pull current on all I/O and control pins	-120	

Table 3-3 Current Characteristics

1. All mains (VCC, AVCC) and ground (VSS, AVSS) pins must always be connected to an external power supply, within the allowed limits.

Symbols	Projects	Numerical value	Unit
TSTG	Storage temperature range	-55 to +125	°C
TJ	Maximum junction temperature	125	°C

Table 3-4 Thermal Properties

3.3 Working conditions

3.3.1 General working conditions

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Unit
fHCLK	Internal AHB clock frequency	High-speed mode [1] PWRC2.DVS=11 PWRC2.DDAS=1111	0	-	168	MHz
		Ultra low speed mode PWRC2.DVS=10 PWRC2.DDAS=1000	0	-	8	
VCC	Standard operating voltage	-	1.8	-	3.6	V
VAVCC(2)	Analog operating voltage	-	1.8	-	3.6	
VIN	Input voltage on 5V withstand voltage pins(3)	2 V ≤ VCC ≤ 3.6 V	-0.3	-	5.5	
		VCC ≤ 2 V	-0.3	-	5.2	
	pa11/usbfs_dm pa12/usbfs_dp Input voltage of the pin		-0.3	-	VCC+0.3	
TJ	Junction temperature range		-40	-	125	°C

Table 3-5 General working conditions

1. Mass production test guarantee.
2. If the VREFH pin is present, the following condition must be considered: $V_{AVCC} - V_{REFH} < 1.2$ V.
3. To keep the voltage above VCC+0.3, the internal pull-up/down resistors must be disabled.

3.3.2 Operating conditions at power-up / power-down

TA obeys general working conditions.

Symbols	Parameters	Minimum value	Maximum value	Unit
tVCC	VCC Rise Time Rate	20	20000	μs/V
	VCC down time rate	20	20000	

Table 3-6 Operating conditions at power-up/power-down

3.3.3 Reset and power control module features

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VBOR	Monitoring voltage of the BOR	ICG1.BOR_LEV[1:0]=00	1.80	1.90	2.00	V
		ICG1.BOR_LEV [1:0]=01	1.90	2.00	2.10	V
		ICG1.BOR_LEV [1:0]=10	2.00	2.10	2.20	V
		ICG1.BOR_LEV [1:0]=11	2.20	2.30	2.40	V
VPVD1	PVD1 monitoring voltage (3)	PVD1LVL[2:0]=000	1.90	2.00	2.10	V
		PVD1LVL[2:0]=001	2.00	2.10	2.20	V
		PVD1LVL[2:0]=010	2.20	2.30	2.40	V
		PVD1LVL[2:0]=011	2.43	2.55	2.67	V
		PVD1LVL[2:0]=100	2.53	2.65	2.77	V
		PVD1LVL[2:0]=101	2.63	2.75	2.87	V
		PVD1LVL[2:0]=110	2.73	2.85	2.97	V
		PVD1LVL[2:0]=111	2.83	2.95	3.07	V
VPVD2	PVD2 monitoring voltage (3)	PVD2LVL[2:0]=000	2.00	2.10	2.20	V
		PVD2LVL[2:0]=001	2.20	2.30	2.40	V
		PVD2LVL[2:0]=010	2.43	2.55	2.67	V
		PVD2LVL[2:0]=011	2.53	2.65	2.77	V
		PVD2LVL[2:0]=100	2.63	2.75	2.87	V
		PVD2LVL[2:0]=101	2.73	2.85	2.97	V
		PVD2LVL[2:0]=110 (1)	2.83	2.95	3.07	V
		PVD2LVL[2:0]=111(2)	1.00	1.10	1.20	V
Vpvdhyst	The hysteresis of PVD1,2 (3)		-	100	-	mV
VPOR(1)	Power-up/power-down reset threshold	Rise along VPOR	1.60	1.68	1.76	V
		Descent along the VPDR	1.56	1.64	1.72	V

VPORhyst	POR Hysteresis		-	40	-	mV

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
IRUSH	Inrush current at regulator power-up (POR or wake up from standby)		-	100	150	mA
TNRST	NRST reset minimum width		500	-	-	ns
TRIPT	Internal reset time		140	160	200	us
TRSTTAO	Power-on reset release time		-	2500	3000	us

Table 3-7 Reset and Power Control Module Characteristics

1. Mass production test guarantee.
2. When PVD2LVDL[2:0] = 111, the comparison voltage is the external input comparison voltage of the PVD2EXINP pin
3. PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops when PVD2LVL[2:0] is set to 111, and PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops when PVD2LVD[2:0] is set to a value other than 111.
4. The hysteresis of PVD1,2 is the difference between the monitored voltage when VCC is rising and the monitored voltage when VCC is falling.

   PVD1 monitoring voltage when VCC rises =

   Vpvd1+Vpvdhyst; PVD2 monitoring voltage when

   VCC rises = Vpvd2+Vpvdhyst.

3.3.4 Supply current characteristics

Current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switching rate, location of the program in memory, and the code being run. The measurement of current consumption is presented in Figure 3-5. The current consumption measurements for the various modes of operation described in this section are derived from a set of test codes running in FLASH under laboratory conditions.

The specific conditions are as follows:

1) All I/O pins are in input mode with static values (no load)on VCC or VSS.
2) Clock frequency selection High-speed mode fHCLK=168MHz/120MHz/24MHz and Ultra-low-speed mode
   fHCLK=8MHz/1MHz.
3) The power consumption modes are: normal operation mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP.
   Power down mode ICC_PD and Dhrystone operating mode ICC_DHRYSTONE.
4) Peripheral Clock ON/OFF Please refer to the specific current test item.
5) High speed mode fHCLK=168MHz/120MHz PLL is on.

Mode	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
High Speed Mode	fHCLK= 168MHz	ICC_RUN	while(1),Full module clock OFF	-40	-	13	-	mA
			while(1),full module clock ON	-40	-	23	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	14	-	mA
			CACHE ON	-40	-	15	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	9	-	mA
			Full modular clock ON	-40	-	19	-	mA
		ICC_RUN	while(1),Full module clock OFF	25	-	13	-	mA
			while(1),full module clock ON	25	-	23	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	14	-	mA
			CACHE ON	25	-	15	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	9	-	mA
			Full modular clock ON	25	-	19	-	mA
		ICC_RUN	while(1),Full module clock OFF	85	-	-	18	mA
			while(1),full module clock ON	85	-	-	28	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	18	mA
			CACHE ON	85	-	-	20	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	14	mA
			Full modular clock ON	85	-	-	24	mA
		ICC_RUN	while(1),Full module clock OFF	105	-	-	20	mA
			while(1),full module clock ON	105	-	-	31	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	19	mA
			CACHE ON	105	-	-	23	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	17	mA
			Full modular clock ON	105	-	-	27	mA

Table 3-8 High-speed mode current consumption 1

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Mode	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
High Speed Mode	fHCLK= 120MHz	ICC_RUN	while(1),Full module clock OFF	-40	-	9.5	-	mA
			while(1),full module clock ON	-40	-	16.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	10	-	mA
			CACHE ON	-40	-	11.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	7	-	mA
			Full modular clock ON	-40	-	14.5	-	mA
		ICC_RUN	while(1),Full module clock OFF	25	-	9.5	-	mA
			while(1),full module clock ON	25	-	16.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	10	-	mA
			CACHE ON	25	-	11.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	7	-	mA
			Full modular clock ON	25	-	14.5	-	mA
		ICC_RUN	while(1),Full module clock OFF	85	-	-	14	mA
			while(1),full module clock ON	85	-	-	22	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	14	mA
			CACHE ON	85	-	-	17	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	12	mA
			Full modular clock ON	85	-	-	20	mA
		ICC_RUN	while(1),Full module clock OFF	105	-	-	16	mA
			while(1),full module clock ON	105	-	-	25	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	15	mA
			CACHE ON	105	-	-	19	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	15	mA
			Full modular clock ON	105	-	-	22	mA

Table 3-9 High-speed mode current consumption 2

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Mode	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
High Speed Mode	fHCLK= 24MHz	ICC_RUN	while(1),Full module clock OFF	-40	-	3	-	mA
			while(1),full module clock ON	-40	-	6	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	3.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	2	-	mA
			Full modular clock ON	-40	-	5.5	-	mA
		ICC_RUN	while(1),Full module clock OFF	25	-	3	-	mA
			while(1),full module clock ON	25	-	6	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	3.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	2	-	mA
			Full modular clock ON	25	-	5.5	-	mA
		ICC_RUN	while(1),Full module clock OFF	85	-	-	8	mA
			while(1),full module clock ON	85	-	-	12	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	7	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	8	mA
			Full modular clock ON	85	-	-	11	mA
		ICC_RUN	while(1),Full module clock OFF	105	-	-	10	mA
			while(1),full module clock ON	105	-	-	14	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	8	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	10	mA
			Full modular clock ON	105	-	-	14	mA

Table 3-10 High-speed mode current consumption 3

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Mode	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Ultra Low Speed Mode	fHCLK= 8MHz	ICC_RUN	while(1),Full module clock OFF	-40	-	1	-	mA
			while(1),full module clock ON	-40	-	3.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	1.5	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	1.2	-	mA
			Full modular clock ON	-40	-	3.2	-	mA
		ICC_RUN	while(1),Full module clock OFF	25	-	1	-	mA
			while(1),full module clock ON	25	-	3.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	1.5	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	1.2	-	mA
			Full modular clock ON	25	-	3.2	-	mA
		ICC_RUN	while(1),Full module clock OFF	85	-	-	4	mA
			while(1),full module clock ON	85	-	-	6	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	4	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	3.5	mA
			Full modular clock ON	85	-	-	6	mA
		ICC_RUN	while(1),Full module clock OFF	105	-	-	6	mA
			while(1),full module clock ON	105	-	-	7	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	4.5	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	4	mA
			Full modular clock ON	105	-	-	6.5	mA

Table 3-11 Ultra-low speed mode current consumption 1

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Mode	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Ultra Low Speed Mode	fHCLK= 1MHz	ICC_RUN	while(1),Full module clock OFF	-40	-	0.7	-	mA
			while(1),full module clock ON	-40	-	2.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	0.9	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	0.9	-	mA
			Full modular clock ON	-40	-	2.4	-	mA
		ICC_RUN	while(1),Full module clock OFF	25	-	0.7	-	mA
			while(1),full module clock ON	25	-	2.5	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	0.9	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	0.9	-	mA
			Full modular clock ON	25	-	2.4	-	mA
		ICC_RUN	while(1),Full module clock OFF	85	-	-	4	mA
			while(1),full module clock ON	85	-	-	5	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	3.5	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	3.5	mA
			Full modular clock ON	85	-	-	5	mA
		ICC_RUN	while(1),Full module clock OFF	105	-	-	5	mA
			while(1),full module clock ON	105	-	-	5.5	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	4	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	5	mA
			Full modular clock ON	105	-	-	5.5	mA

Table 3-12 Ultra-low speed mode current consumption 2

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V

Mode	Parameter	Symbol	Conditions (VCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Stop Mode	-	ICC_STP	PWR_PWRC1.STPDAS=00	-40	-	160	-	uA
			PWR_PWRC1.STPDAS=11	-40	-	30	-	uA
			PWR_PWRC1.STPDAS=00	25	-	220	-	uA
			PWR_PWRC1.STPDAS=11	25	-	80	-	uA
			PWR_PWRC1.STPDAS=00	85	-	-	3600	uA
			PWR_PWRC1.STPDAS=11	85	-	-	3400	uA
			PWR_PWRC1.STPDAS=00	105	-	-	4800	uA
			PWR_PWRC1.STPDAS=11(3)	105	-	-	4600	uA
Power down mode	-	ICC_PD	Power down mode 1	-40	-	10	-	uA
			Power down mode 2	-40	-	4	-	uA
			Power down mode 3	-40	-	1.8	-	uA
			Power down mode 4	-40	-	1.8	-	uA
			Power down mode 2+XTAL32+RTC	-40	-	6	-	uA
			Power down mode 2+LRC+RTC	-40	-	9	-	uA
			Power down mode 1	25	-	10	-	uA
			Power down mode 2	25	-	4	-	uA
			Power down mode 3	25	-	1.8	-	uA
			Power down mode 4	25	-	1.8	-	uA
			Power down mode 2+XTAL32+RTC	25	-	6	-	uA
			Power down mode 2+LRC+RTC	25	-	9	-	uA
			Power down mode 1	85	-	-	21	uA
			Power down mode 2	85	-	-	19	uA
			Power down mode 3	85	-	-	19	uA
			Power down mode 4	85	-	-	19	uA
			Power down mode 2+XTAL32+RTC	85	-	-	21	uA
			Power down mode	85	-	-	21	uA

2+LRC+RTC					
Power down mode 1	105	-	-	25	uA
Power down mode 2	105	-	-	23	uA

Mode	Parameter	Symbol	Conditions (VCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
			Power down mode 3	105	-	-	20.5	uA
			Power down mode 4[3]	105	-	-	20.5	uA
			Power down mode 2+XTAL32+RTC	105	-	-	25	uA
			Power down mode 2+LRC+RTC	105	-	-	25	uA

Table 3-13 Low Power Mode Current Consumption

1. Typ Voltage condition VCC=3.3V
2. Max Voltage Condition VCC=1.8~3.6V
3. Mass production test guarantee.

Item	Parameter	Symbol	Condition (VCC=AVCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ	Max	
Modules Current	-	ICC_MODULE	XTAL oscillation mode large drive 24MHz	25	-	1.8	-	mA
			Drive 16MHz in oscillation mode	25	-	1	-	mA
			Oscillation mode small drive 10MHz	25	-	0.8	-	mA
			Oscillation mode ultra-small drive 8MHz	25	-	0.6	-	mA
			XTAL 32K	25	-	0.5	-	mA
			HRC	25	-	0.35	-	mA
			PLL (@480MHz)	25	-	2.3	-	mA
			PLL (@240MHz)	25	-	1.4	-	mA
			ADC	25	-	1.2	-	mA
			DAC	25	-	70	-	uA
			CMP	25	-	0.11	-	mA
			PGA	25	-	1	-	mA
			USBFS(1)	25	-	6	-	mA

Table 3-14 Analog Module Current Consumption

1. Contains the current when the control section is communicating with the USBPHY.

3.3.5 Electrical sensitivity

Different tests (ESD, L U)are performed on the chip using specific measurement methods to determine its performance in terms of electrical sensitivity.

3.3.5.1 Electrostatic Discharge (ESD)

Electrostatic discharge is applied to the pins of each sample for each pin combination. This test complies with the JESD22-A114/C101 standard.

Symbols	Parameters	Conditions	Maximum value	Unit
VESD(HBM)	Electrostatic discharge voltage (human model)	T_A = +25 °C according to JESD22-A114	4000	V

Table 3-15 ESD Characteristics

3.3.5.2 Static Latch-up

To evaluate static Latch-up performance, two complementary static Latch-up tests are performed on the chip:

- Over-voltage applied to each power and analog input pin
- Applying current injection to other inputs, outputs,

and configurable I/O pins these tests comply with the EIA/JESD 78A IC Latch-up standard.

Symbols	Parameters	Conditions	Maximum value	Unit

Table 3-16 Static Latch-up Characteristics

3.3.6 Low-power mode wake-up timings

The wake-up time is measured from the wake-up event trigger to the first instruction executed by the CPU:

- For stop or sleep mode: the wakeup event is WFE.
- The WKUP pin is used to wake up from standby, stop, or sleep mode. All timings are tested at ambient temperature and VCC=3.3 V.

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
TSTOP1	Wake up from stop mode	PWR_PWRC1.VHRCSD=1 and PWR_PWRC1.VPLLSD=1,system clock is MRC,program Sequence execution on RAM	2	5	us
TSTOP2	Wake up from stop mode	The system clock is MRC and the program is executed on Flash	8	15	
$TPD1^{(1)}$	Wake up from power down mode 1	VCAP_1/VCAP_2 total capacity is 0.094uF or 0.1uF	15	25	
		VCAP_1/VCAP_2 total capacity is 0.2uF or 0.22uF	20	30	
$TPD2^{(1)}$	Wake up from	VCAP_1/VCAP_2 total capacity is 0.094uF or 0.1uF	40	50	

Table 3-17 Low Power Mode Wake-up Time

The total VCAP_1/VCAP_2 capacity of the chip must match the value assigned to the PWR_PWRC3.PDTS bit. If the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, you need to ensure that the PWR_PWRC3.PDTS bit is cleared before entering power-down mode.

3.3.7 I/O Port Features

General input/output characteristics

Symbols	Parameters		Conditions	Minimum value	Typical values	Maximum value.	Unit
V_{IL} (1)	Input low level		1.8≤VCC≤3.6	-	-	0.2_{VCC}	V
V_{IH} (1)	Input high level		1.8≤VCC≤3.6	0.8_{VCC}	-	-	V
VHYS	Input hysteresis		1.8≤VCC≤3.6	-	0.2	-	V
I_{LKG}(1)	I/O input leakage current		VSS≤VIN≤VCC	-	-	±1	uA
			VIN = 5.5V(2)	-	-	5	uA
RPU(1)	Weak pull-up equivalent resistance	USBFS_DP, USBFS_DM	-	-	1.5	-	KΩ
		In addition to the USBFS_DP and Other inputs for USBFS_DM Pins	VIN = VSS	-	30	-	KΩ
CIO	I/O pin capacitance	pa11/usbfs_dm pa12/usbfs_dp	-	-	10	-	pF
		In addition to the PA11/USBFS_DM and Other input pins of PA12/USBFS_DP	-	-	5	-	pF

Table 3-18I/O Static Characteristics

1. Mass production test guarantee.
2. To keep the voltage above VCC+0.3 V, the internal pull-up/down resistors must be disabled.

Output Voltage

Driver settings	Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
Low drive	V_{OL} (1)(2)	Low level output	IIO=±1.5mA, 1.8≤VCC<2.7	-	-	0.4	V
	V_{OH} (1)(3)	High level output		VCC-0.4	-	-	
	V_{OL} (1)(2)	Low level output	IIO=±3mA, 2.7≤VCC≤3.6	-	-	0.4	
	V_{OH} (1)(3)	High level output		VCC-0.4	-	-	
	V_{OL} (1)(2)	Low level output	IIO=±6mA, 2.7≤VCC≤3.6	-	-	1.3	
	V_{OH} (1)(3)	High level output		VCC-1.3	-	-	
Medium drive	V_{OL} (1)(2)	Low level output	IIO=±3mA, 1.8≤VCC<2.7	-	-	0.4	
	V_{OH} (1)(3)	High level output		VCC-0.4	-	-	
	V_{OL} (1)(2)	Low level output	IIO=±5mA, 2.7≤VCC≤3.6	-	-	0.4	
	V_{OH} (1)(3)	High level output		VCC-0.4	-	-	
	V_{OL} (1)(2)	Low level output	IIO=±12mA, 2.7≤VCC≤3.6	-	-	1.3	
	V_{OH} (1)(3)	High level output		VCC-1.3	-	-	
High drive	V_{OL} (1)(2)	Low level output	IIO=±6mA, 1.8≤VCC<2.7	-	-	0.4	
	V_{OH} (1)(3)	High level output		VCC-0.4	-	-	
	V_{OL} (1)(2)	Low level output	IIO=±8mA, 2.7≤VCC≤3.6	-	-	0.4	
	V_{OH} (1)(3)	High level output		VCC-0.4	-	-	
	V_{OL} (1)(2)	Low level output	IIO=±20mA, 2.7 ≤VCC≤3.6	-	-	1.3	

	V_{OH}(1)(3)	High level output		VCC-1.3	-	-	

Table 3-19 Output Voltage Characteristics

1. Mass production test guarantee.
2. The I_{IO} supply current of the device must always take into account the absolute maximum rating specified in Table 3-3. The sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} pull current of the device must always follow the absolute maximum ratings listed in Table 3-3, and the sum of the I_{IOs} (I/O ports and control pins) must not exceed I_{VCC}.

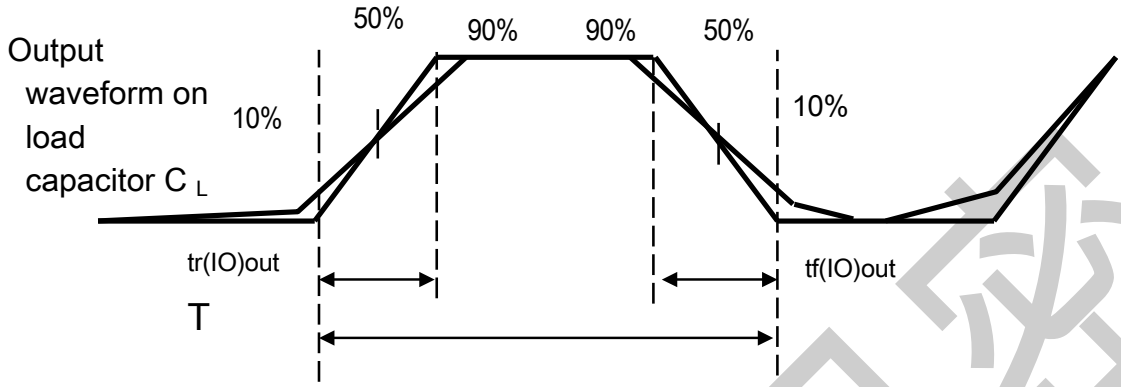
Input/output AC characteristics

Driver settings	Symbols	Parameters	Conditions (3)	Minimum value	Typical values	Maximum value	Unit
Low drive	f_{max}(IO)out	Maximum frequency (1)	CL=30 pF, VCC≥ 2.7V	-	-	20	MHz
			CL=30 pF, VCC≥1.8V	-	-	10	
			CL=10pF, VCC≥2.7V	-	-	40	
			CL=10pF, VCC≥1.8V	-	-	20	
	t_f(IO)out t_r(IO)out	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	-	-	15	ns
			CL=30 pF, VCC≥1.8V	-	-	25	
			CL=10pF, VCC≥2.7V	-	-	7.5	
			CL=10pF, VCC≥1.8V	-	-	15	
Medium drive	f_{max}(IO)out	Maximum frequency (1)	CL=30 pF, VCC≥ 2.7V	-	-	45	MHz
			CL=30 pF, VCC≥1.8V	-	-	22.5	
			CL=10pF, VCC≥2.7V	-	-	90	
			CL=10pF, VCC≥1.8V	-	-	45	
	t_f(IO)out t_r(IO)out	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	-	-	7.5	ns
			CL=30 pF, VCC≥1.8V	-	-	12	
			CL=10pF, VCC≥2.7V	-	-	4	
			CL=10pF, VCC≥1.8V	-	-	7.5	
High drive	f_{max}(IO)out	Maximum frequency (1)	CL=30 pF, VCC≥2.7V	-	-	100	MHz
			CL=30 pF, VCC≥1.8V	-	-	50	
			CL=10pF, VCC≥2.7V	-	-	180	
			CL=10pF, VCC≥1.8V	-	-	100	
	t_f(IO)out t_r(IO)out	Output high to low level fall time and output low to high level rise time	CL=30 pF, VCC≥2.7V	-	-	4	ns
			CL=30 pF, VCC≥1.8V	-	-	6	
			CL=10pF, VCC≥2.7V	-	-	2.5	
			CL=10pF, VCC≥1.8V	-	-	4	

Table 3-20 I/O AC Characteristics

1. The maximum frequency is defined in Figure 3-6.
2. Load capacitance $_{CL}$ must take into account the capacitance of the PCB and MCU pins (pin to board capacitance can be roughly estimated)

for 10pF)



Maximum frequency condition: $(t_r + t_f) \leq (2/3)T$ and Duty cycle= 50%±5% (load capacitance C)$_L$

(indicated in the "Conditions" column of the "Input/output AC characteristics" table)

Figure 3-6 I/O AC Characteristics Definition

3.3.8 USART Interface Features

符号	参数		最小值	最大值	单位
t_{cyc}	输入时钟周期数	UART	4	-	t_{PCLK1}
		CSI	6	-	
t_{CKw}	输入时钟宽度		0.4	0.6	t_{Scyc}
t_{CKr}	输入时钟上升时间		-	5	ns
t_{CKf}	输入时钟下降时间		-	5	ns
t_{TD}	发送延迟时间	CSI	-	28	ns
t_{RDS}	接收数据建立时间	CSI	15	-	ns
t_{RDH}	接收数据保持时间	CSI	5	-	ns

Table 3-21 USART AC Timing

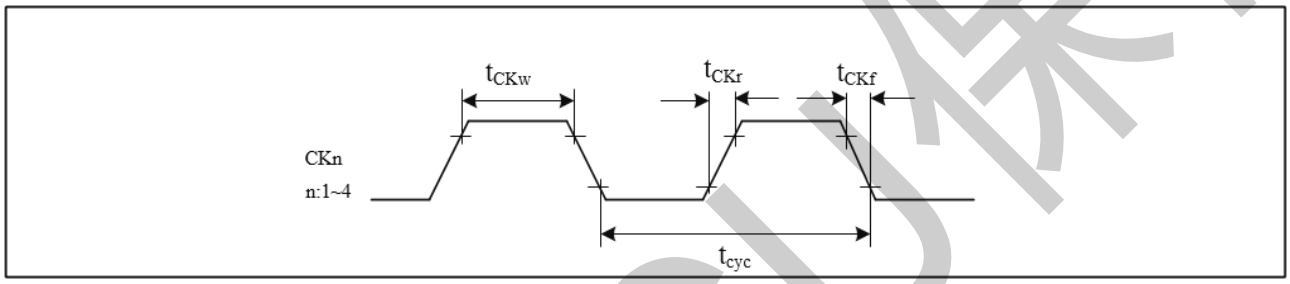


Figure 3-7 USART Clock Timing

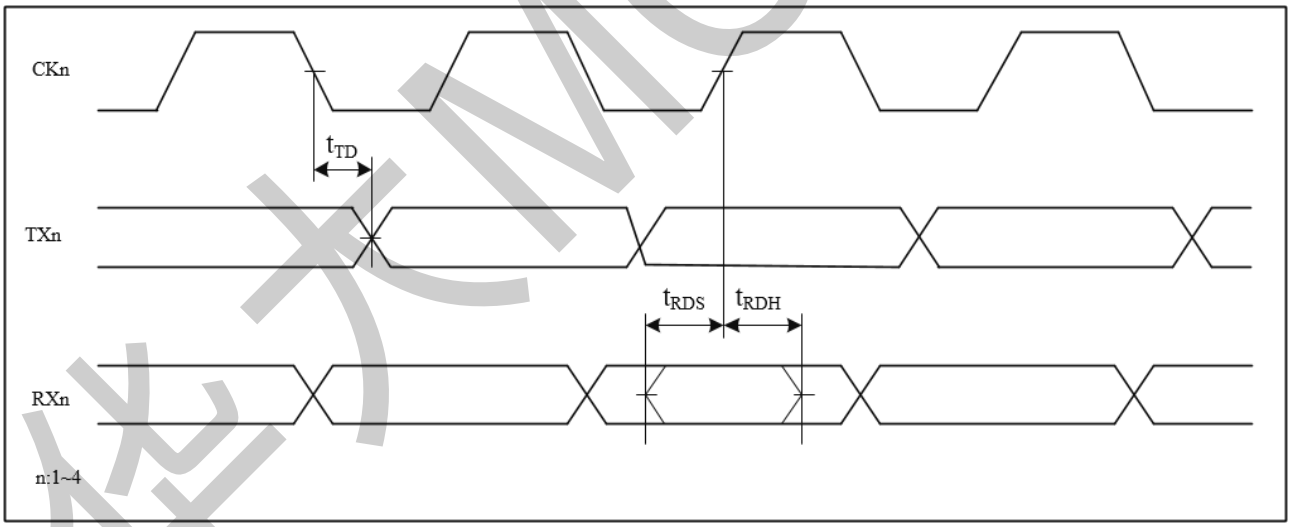


Figure 3-8 USART (CSI) Input and Output Timing

3.3.9 I2S Interface Features

Symbols	Performance Indicators	Conditions	Min	Max	Unit
fMCK	I2S main clock output	-	256 *8K	256*Fs	MHz
fCK	I2S clock frequency	Master data: 32 bits	20	64*Fs	MHz
		Slave data: 32 bits	-	64*Fs	
DCK	I2S clock frequency duty cycle	Slave receiver	30	70	%
t_v(WS)	WS valid time	Master mode	0	-	ns
t_h(WS)	WS hold time	Master mode	0	-	
t_{su}(WS)	WS setup time	Slave mode	1	-	
t_h(WS)	WS hold time	Slave mode	0	-	
t_{su}(SD_MR)	Data input setup time	Master receiver	7.5	-	
t_{su}(SD_SR)		Slave receiver	2	-	
t_h(SD_MR)	Data input hold time	Master receiver	0	-	
t_h(SD_SR)		Slave receiver	0	-	
t_v(SD_ST) t_h(SD_ST)	Data output valid time	Slave transmitter(after enable edge)	-	27	
t_v(SD_MT)		Master transmitter(after enable edge)	-	20	
t_h(SD_MT)	Data output hold time	Master transmitter(after enable edge)	2.5	-	

Table 3-22 I2S Electrical Characteristics

1. Fs: I2S sampling frequency

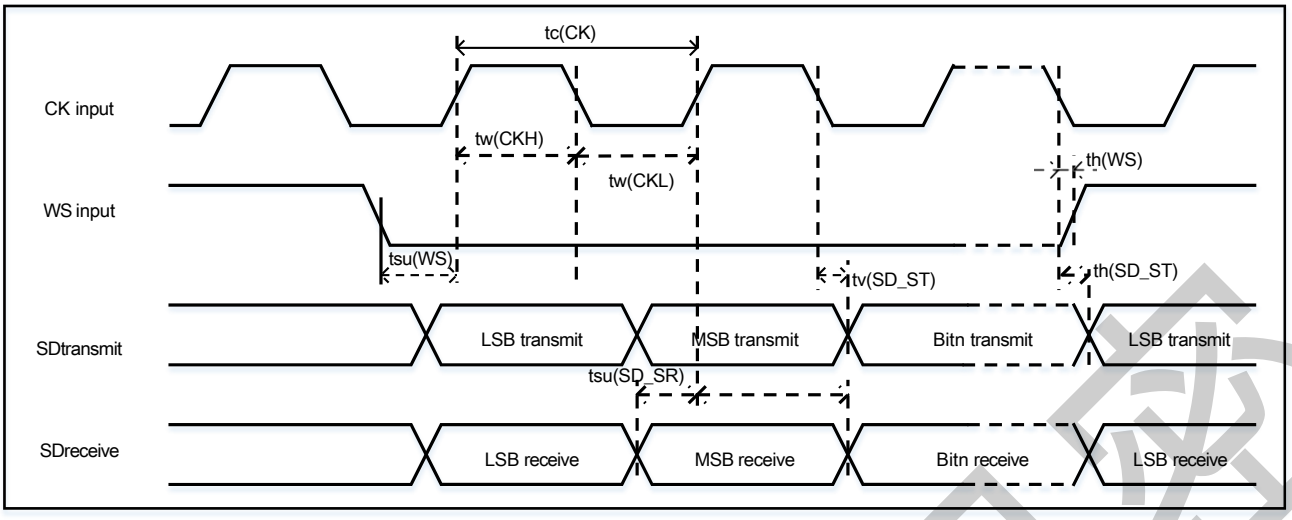


Figure 3-9 I2S Slave Mode Timing (Philips Protocol)

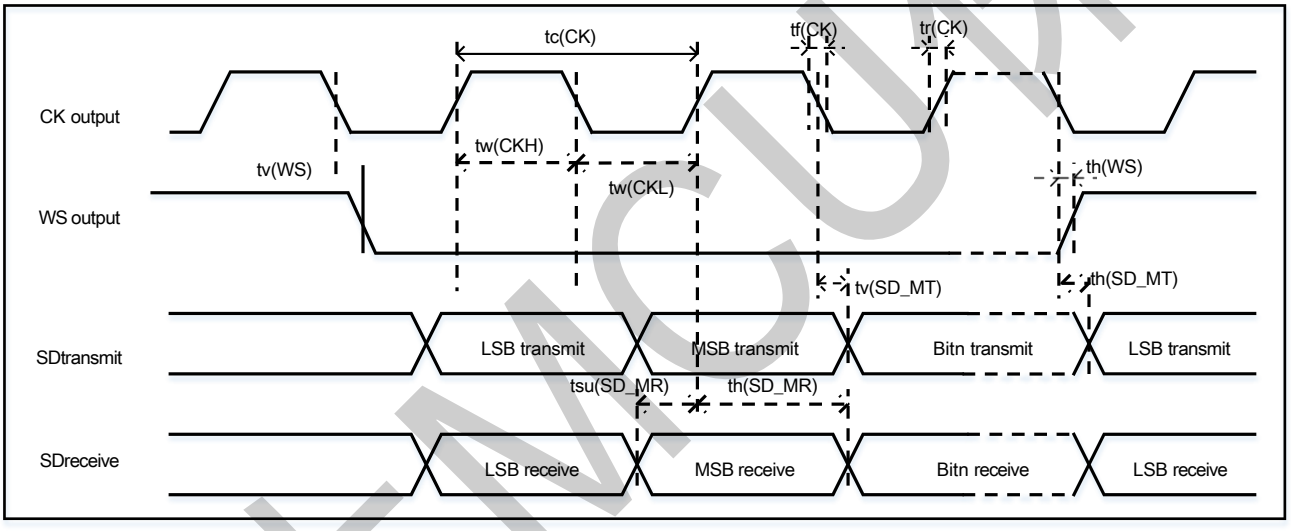


Figure 3-10 I2S Master Mode Timing (Philips Protocol)

3.3.10 I2C Interface Features

Symbols	Parameters	Standard Mode (SM)		Fast Mode (FM)		Unit
		Min	Max	Min	Max	
fSCL	SCL Frequency	0	100	0	400	KHz
tHD;STA	Start condition/restart condition Hold	4.0	-	0.6	-	us
tLOW	SCL low	4.7	-	1.3	-	us
tHIGH	SCL high level	4	-	0.6	-	us
tSU;STA	Restart conditionSetup	4.7	-	0.6	-	us
tHD;DAT	Data Hold	0	-	0	-	us
tSU;DAT	DataSetup	50+ tI2C reference clock period	-	50+ tI2C reference clock period	-	ns
tR	Rise time of SCL/SDA	-	1000	6.5	300	ns
tF	SCL/SDA drop time	-	300	6.5	300	ns
tSU;STO	Stop conditionSetup	4	-	0.6	-	us
tBUF	Between the stop condition and the start condition BUS free time	4.7	-	1.3	-	us
Cb	Load capacitance	-	400	-	400	pF

Table 3-23 I2C Electrical Characteristics

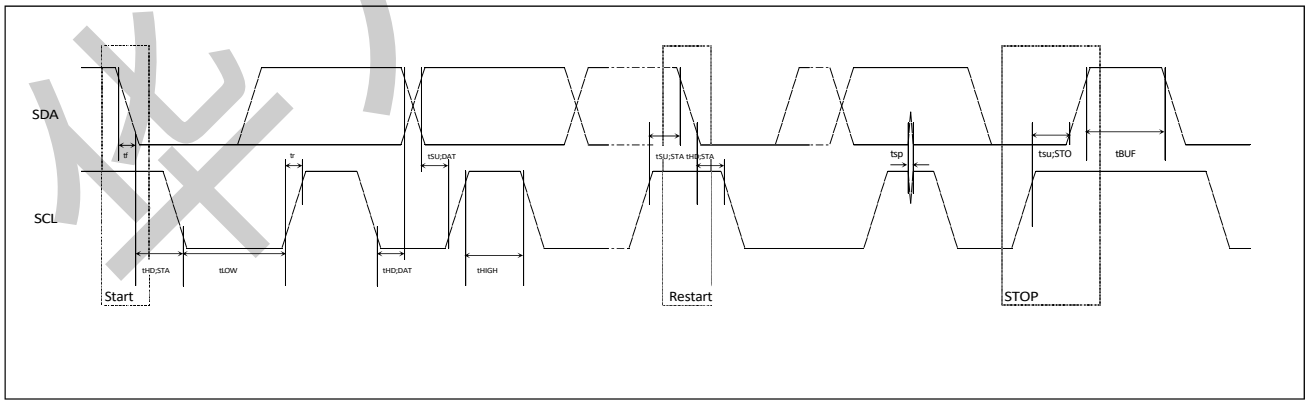


Figure 3-11 I2C Bus Timing Definition

3.3.11 SPI Interface Features

Item			Symbol	Min	Max	Unit	Test conditions
	SCK clock cycle	Master	tspcyc	2 (pclk ≤60MHz) 4 (pclk ≤60MHz)	4096	tpcyc	Figure 3-12 C=30pF
		Slave		6	4096		
	SCK clock rise and fall time	Master	tsckr	-	5	ns	
		Slave	tsckf	-	1	us	
	Data input setup time	Master	tsu	4	-	ns	Figure 3-13 C=30pF
		Slave		5	-		
	Data input hold time	Master	th	tpcyc	-	ns	
		Slave		20	-		
	Data output delay	Master	tod	-	8	ns	
		Slave		-	20		
	Data output hold time	Master	toh	0	-	ns	
		Slave		0	-		
	MOSI/MISO rise and fall time	Master	tdr	-	5	ns	
		Slave	tdf	-	1	us	
	SS rise and fall time	Master	tssr	-	5	ns	
		Slave	tssf	-	1	us	

Table 3-24 SPI Electrical Characteristics

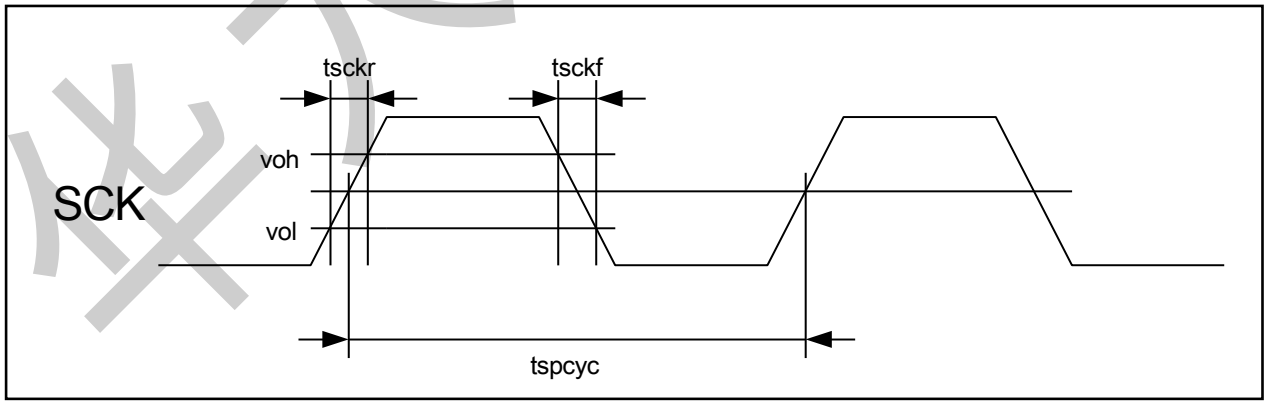


Figure 3-12 SCK Clock Definition

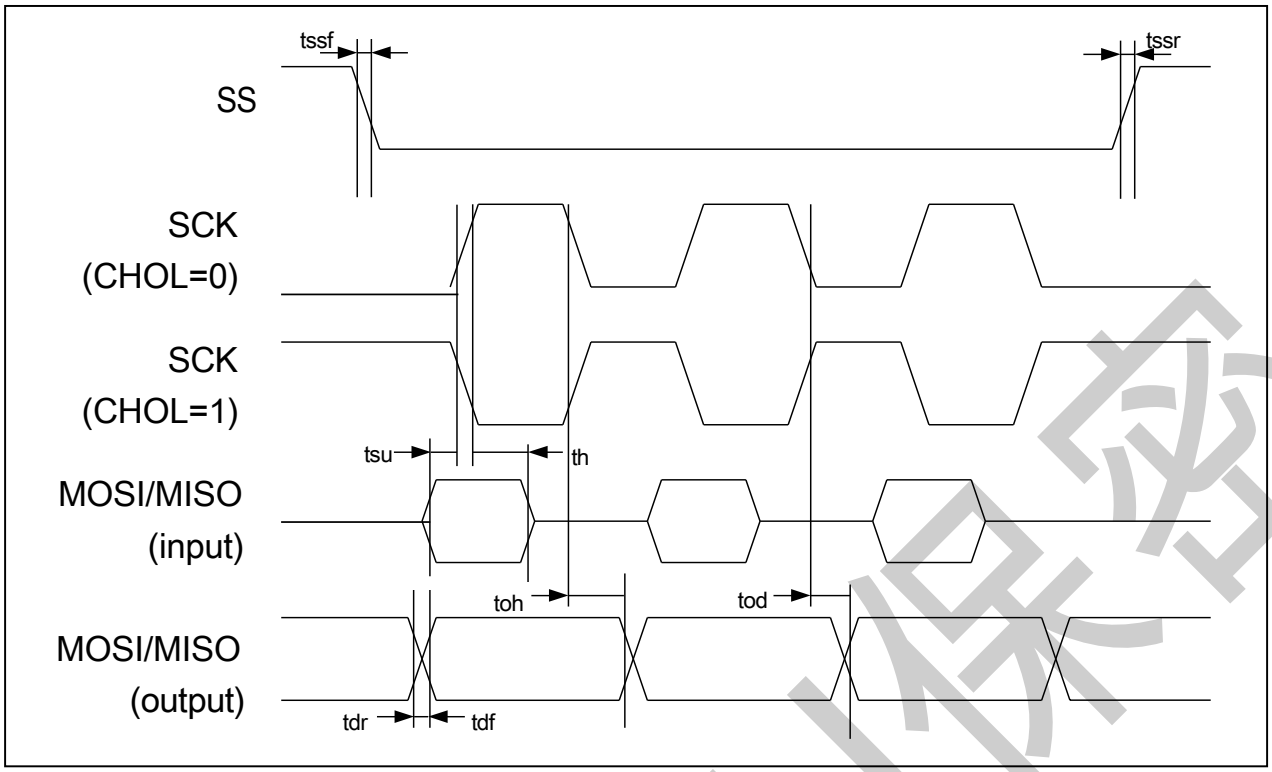


Figure 3-13 SPI Interface Timing Requirements

3.3.12 USB Interface Features

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input	VCC	Operating Voltage	-	3.0(2)	-	3.6	V
	VIL	Input low level	-	-	-	0.8	V
	VIH	Input high level	-	2.0	-	-	V
	VDI	Differential input sensitivity	-	0.2	-	-	V
	VCM	Differential common mode voltage	-	0.8	-	2.5	V
Output	VOL(3)	Static output low level	RL=1.5kΩ to 3.6V(4)	-	-	0.3	V
	VOH(3)	Static output high level	RL=15kΩ to VSS(4)	2.8	-	3.6	V
	VCRS	Cross-over voltage	CL=50pF	1.3	-	2.0	V
	tR	Rise time	CL=50pF. 10%~90% of |VOH-VOL|	4	-	20	ns
	tF	Descent time	CL=50pF. 10%~90% of |VOH-VOL|	4	-	20	ns
	tRFMA	Rise and fall time ratio tR/tF	CL=50pF	90	-	111.1	%
RPD(3)		Pull Down Resistors	VIN= VCC, in host mode	14.25	-	24.80	kΩ
RPU(3)		Pull-up resistors	VIN= VSS, idle state	0.900	1.2	1.575	kΩ
			VIN= VSS. in device mode	1.425	2.3	3.090	kΩ

Table 3-25 USB Full-Speed Electrical Characteristics

1. All voltages were measured based on local ground potential.
2. Operating voltage drops to 2.7V still guarantees USB full-speed transceiver functionality, but not full USB full-speed electrical characteristics, which degrade over the VCC voltage range of 2.7 to 3.0V.
3. Mass production test guarantee.
4. RL is the load connected to the USB full-speed drive.

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input	VCC	Operating Voltage	-	3.0(2)	-	3.6	V
	VIL	Input low level	-	-	-	0.8	V
	VIH	Input high level	-	2.0	-	-	V
	VDI	Differential input sensitivity	-	0.2	-	-	V
	VCM	Differential common mode voltage	-	0.8	-	2.5	V
Output	VOL(3)	Static output low level	RL=1.5kΩ to 3.6V(4)	-	-	0.3	V
	VOH(3)	Static output high level	RL=15kΩ to VSS(4)	2.8	-	3.6	V
	VCRS(3)	Cross-over voltage	CL=200pF~600pF	1.3	-	2.0	V
	tR(3)	Rise time	CL=200pF~600pF, 10%~90% of |VOH-VOL|	75	-	300	ns
	tF(3)	Descent time	CL=200pF~600pF, 10%~90% of |VOH-VOL|	75	-	300	ns
	tRFMA(3)	Rise and fall time ratio tR/tF	CL=200pF~600pF	80	-	125	%
RPD(3)		Pull Down Resistors	VIN= VCC, in host mode	14.25	-	24.80	kΩ

Table 3-26 USB Low-Speed Electrical Characteristics

1. All voltages were measured based on local ground potential.
2. Operating voltage drops to 2.7V still guarantees USB low-speed transceiver functionality, but not full USB low-speed electrical characteristics, which deteriorate over the VCC voltage range of 2.7 to 3.0V.
3. Mass production test guarantee.
4. RL is the load connected to the USB low-speed drive.

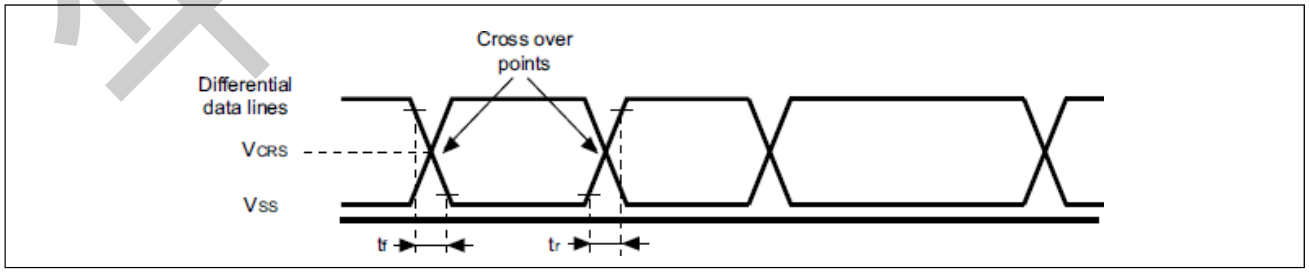


Figure 3-14 USB Rise/Fall Time and Cross Over Voltage Definition

3.3.13 PLL Features

Symbols	Parameters	Conditions	Min	Typ	Max	Unit
fPLL_IN	PLL input clock(1)	-	1	-	24	MHz
fPLL_OUT	PLL multiplier output	-	15	-	240	MHz
fVCO_OUT	PLL VCO output	-	240	-	480	MHz
tLOCK	PLL lock time	-	-	80	120	μs
JitterPLL	Period Jitter	PLL input clock = 4MHz System clock = 120MHz	-	-	±200	ps

Table 3-27 PLL Key Performance Indicators

1. A higher input clock is recommended to obtain good Jitter characteristics.

3.3.14 JTAG interface features

Synbol	Item	Min	Typ	Max	Unit
tTCKcyc	TCK clock cycle time	50	-	-	ns
tTCKH	TCK clock high pulse width	20	-	-	ns
tTCKL	TCK clock low pulse width	20	-	-	ns
tTCKr	TCK clock rise time	-	-	5	ns
tTCKf	TCK clock fall time	-	-	5	ns
tTMSs	TMS setup time	8	-	-	ns
tTMSh	TMS hold time	8	-	-	ns
tTDIs	TDI setup time	8	-	-	ns
tTDIh	TDI hold time	8	-	-	ns
tTDOd	TDO data delay time	-	-	20	ns

Table 3-28 JTAG interface features

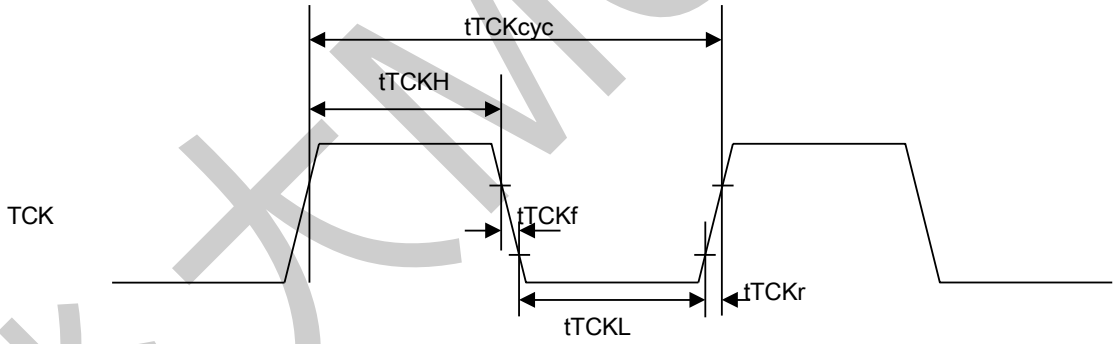


Figure 3-15 JTAG TCK clock

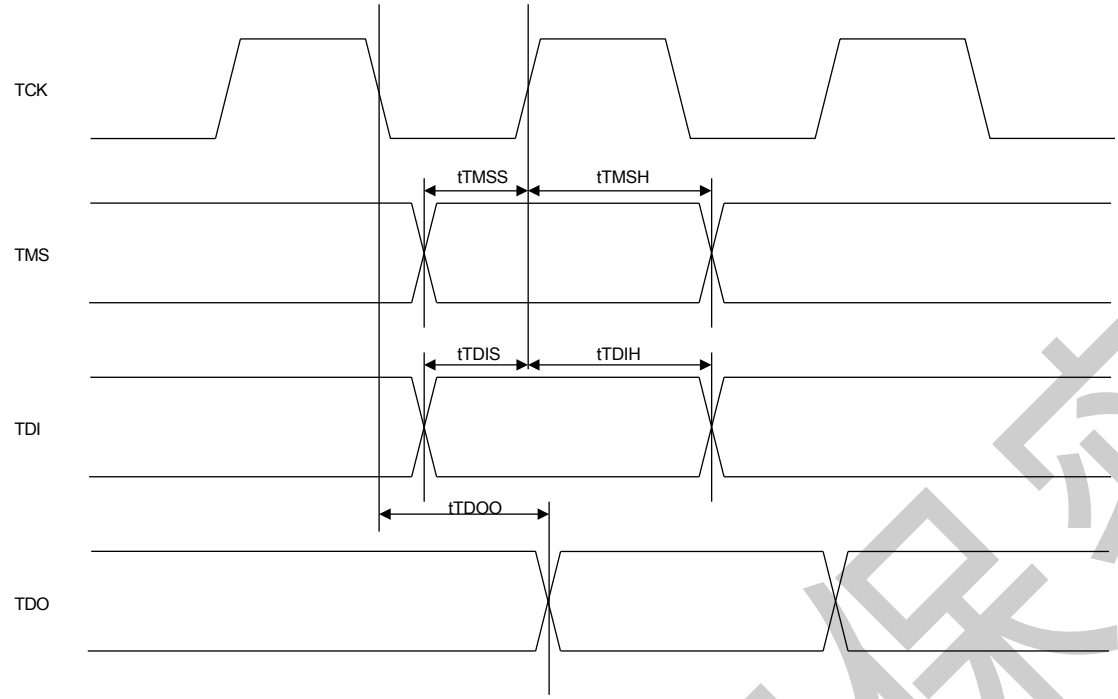


Figure 3-16 JTAG input and output

3.3.15 External clock source characteristics

3.3.15.1 High-speed external user clock generated by external sources

In bypass mode, the XTAL oscillator is off and the input pins are standard I/O. The external clock signal must be considered I/O

Static properties.

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{XTAL_EXT}	User external clock source frequency	-	1	-	24	MHz
V_{IH_XTAL}	XTAL_IN input pin high level voltage		$0.8*V_{CC}$	-	V_{CC}	V
V_{IL_XTAL}	XTAL_IN input pin low level voltage		V_{SS}	-	$0.2*V_{CC}$	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_IN rise or fall time		-	-	5	ns
$Duty_{(XTAL)}$	Duty Cycle	-	40	-	60	%

Table 3-29 High-speed external user clock characteristics

3.3.15.2 Crystal / Ceramic Resonator Generates High Speed External Clock

A high-speed external (XTAL) clock can be generated using a 4 to 24 MHz crystal/ceramic resonator oscillator. The resonator and load capacitor must be placed as close to the oscillator pins as possible in the application to minimize output distortion and stabilization time. For more information on resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
fXTAL_IN	Oscillator frequency		4	-	24	MHz
R_F (1)	Feedback Resistor		-	300	-	kΩ
Gmmax	-	Vibration	4	-	-	mA/V
$t_{SU(XTAL)}$ (2)	Start-up time	VCC stable, crystal = 8MHz	-	-	2.0	ms

Table 3-30XTAL 4-24 MHz Oscillator Characteristics

1. Mass production test guarantee.
2. $t_{SU(XTAL)}$ is the start-up time, which is the time measured from the time the software enables XTAL until a stable 8MHz oscillation frequency is obtained. This value is based on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high quality external ceramic capacitors designed for high frequency applications that meet the requirements of the crystal or resonator and are between 5 pF and 25 pF (typical) in size (see figure below) C_{L1} and C_{L2} are typically the same size. The load capacitance specified by the crystal manufacturer is usually a series combination of C_{L1} and C_{L2}. The capacitance of the PCB and MCU pins must be taken into account when sizing C_{L1} and C_{L2} (pin-to-board capacitance can be roughly estimated at 10 pF)

Resonators with integrated capacitors

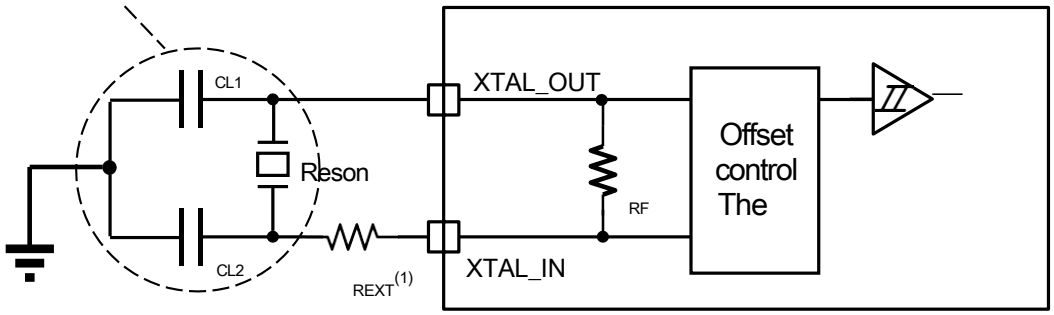


Figure 3-17 Typical Application with 8 MHz Crystal

1. The value of R_{EXT} depends on the crystal characteristics.

3.3.15.3 Low-speed external clock generated by crystal/ceramic resonator

A low-speed external clock can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. In applications, the resonator and load capacitor must be placed as close to the oscillator pins as possible to minimize output distortion and start-up stability time. For more information on resonator characteristics (frequency, package, accuracy, etc.), please consult the crystal resonator manufacturer.

Symbols	Parameters	Conditions	Specification			Unit
			Min	Typ	Max	
FXTAL32	Frequency	-	-	32.768	-	KHz
R_F (1)	Feedback Resistor	-	-	15	-	MΩ

Table 3-31 XTAL32 Oscillator Characteristics

1. Mass production test guarantee.
2. $T_{SUXTAL32}$ is the start-up time, which is the time measured from the time XTAL32 is enabled by software until a stable 32.768 kHz oscillation frequency is obtained. This value is based on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

3.3.16 Internal clock source characteristics

3.3.16.1 Internal High Speed (HRC) Oscillator

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
fHRC	Frequency(1)	Mode 1	-	16	-	MHz
		Mode 2	-	20	-	
	User adjustable scale	-	-	-	0.2	%
	Frequency accuracy (1)	TA = -40 to 105 °C	-2	-	2	%
		TA = -20 to 105 °C	-1.5	-	1.5	%
		TA = 25 °C	-0.5	-	0.5	%
tst(HRC)	HRC oscillator oscillation	-	-	-	15	μs

Table 3-32HRC Oscillator Characteristics

1. Mass production test guarantee.

3.3.16.2 Internal medium speed (MRC) oscillator

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit
fMRC(1)	Frequency	7.2	8	8.8	MHz
tst(MRC)	MRC oscillator stabilization time	-	-	3	μs

Table 3-33 MRC Oscillator Characteristics

1. Mass production test guarantee.

3.3.16.3 Internal low speed (LRC) oscillator

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit
f_{LRC}(1)	Frequency	27.853	32.768	37.683	KHz
$t_{st(LRC)}$	LRC oscillator stabilization time	-	-	36	μs

Table 3-34 LRC oscillator characteristics

1. Mass production test guarantee.

3.3.16.4 SWDT Dedicated Internal Low Speed (SWDTLRC) Oscillator

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit
$f_{SWDTLRC}$(1)	Frequency	9	10	11	KHz
tst(SWDTLRC)	SWDTLRC oscillator stabilization time	-	-	57.1	μs

Table 3-35 SWDTLRC Oscillator Characteristics

1. Mass production test guarantee.

3.3.17 12-bit ADC Features

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VAVCC	Power supply	-	1.8	-	3.6	V
V_{REFH}(1)	Positive reference voltage	-	1.8	-	VAVCC	V
fADC	ADC conversion clock frequency	In high speed action mode VAVCC=2.4 ~3.6V	1	-	60	MHz
		In high speed action mode VAVCC=1.8 ~2.4V	1	-	30	

		Ultra low speed action mode	1	-	8	
VAIN	Conversion voltage range	-	VAVSS	-	VREFH	V
RAIN	External Input Impedance	See Equation 1 for details	-	-	50	kΩ
RADC	Sampling switch resistance	-	-	-	6	kΩ
CADC	Internal sample and hold capacitors	-	-	4	7	pF
tD	Trigger transition delay	f_{ADC} = 60 MHz	-	-	0.3	μs

Table 3-36ADC Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
tS	Sampling time	fADC=60MHz	0.183	-	4.266	μs
			11	-	255	1/ fADC
tCONV	Total conversion time for a single channel (including sampling time)	fADC = 60 MHz 12-bit resolution	0.4	-	-	μs
		fADC = 60 MHz 10-bit resolution	0.36	-	-	μs
		fADC = 60 MHz 8-bit resolution	0.33	-	-	μs
		20 to 268 (sampling time tS+ converges to n-bit resolution + 1)				1/fADC
fS	Sampling rate fADC = 60 MHz	12-bit resolution single ADC	-	-	2.5	Msps
		12-bit resolution time-interpolated dual ADC	-	-	4.6	
tST	Power-up time	-	-	1	2	μs

Table 3-37ADC Characteristics (continued)

1. VAVCC-VREFH<1.2V

Formula 1: RAIN maximum value formula

$$\square\square\square\square = \frac{\square}{\square\square\square \times C \times \ln(2^{N+2}) - \square\square\square} - \frac{k-1}{\square\square\square}$$

The above equation (Equation 1) is used to determine the maximum external impedance to bring the error below 1/4 LSB. Where N = 12 (12-bit resolution) and k is the number of sampling periods defined in the ADC_SSTR register.

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
E_T	Absolute error	In high speed action mode fADC=60MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±4.5	±6	LSB
E_O	Offset Error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linearity error		±1.5	±3	LSB

Table 3-38 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=60MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
E_T	Absolute error	In high speed action mode fADC=30MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±4.5	±6	LSB
E_O	Offset Error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D(1)	Differential linear error		±1	±2	LSB
E_L(1)	Integral linearity error		±1.5	±3	LSB

Table 3-39 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=30MHz

1. Mass production test guarantee.

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
E_T	Absolute error	In high speed action mode fADC=30MHz Input source impedance <1kΩ VAVCC=1.8 ~2.4V	±4.5	±6	LSB
E_O	Offset Error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linearity error		±2	±3	LSB

Table 3-40 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=30MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
E_T	Absolute error	In ultra-low speed action mode fADC=8MHz Input source impedance <1kΩ VAVCC=1.8 ~3.6V	±4.5	±6	LSB
E_O	Offset Error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential linear error		±1	±2	LSB
E_L	Integral linearity error		±2	±3	LSB

Table 3-41 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Accuracy @ fADC=8MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
E_T	Absolute error	In high speed action mode fADC=60MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±5.5	±7	LSB
E_O	Offset Error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential linear error		±1.5	±2	LSB
E_L	Integral linearity error		±2.0	±3	LSB

Table 3-42 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=60MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
E_T	Absolute error	In high speed action mode fADC=30MHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	±5.5	±7	LSB
E_O	Offset Error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D(1)	Differential linear error		±1.5	±2	LSB
E_L(1)	Integral linearity error		±2.0	±3	LSB

Table 3-43 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=30MHz

1. Mass production test guarantee.

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error	In high speed action mode fADC=30MHz Input source impedance <1kΩ VAVCC=1.8 ~2.4V	±5.5	±7	LSB
EO	Offset Error		±4.5	±7	LSB
EG	Gain error		±4.5	±7	LSB
ED	Differential linear error		±1.5	±2	LSB
EL	Integral linearity error		±2.5	±3	LSB

Table 3-44 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=30MHz

Symbols	Parameters	Conditions	Typical values	Maximum value	Unit
ET	Absolute error	In ultra-low speed action mode fADC=8MHz Input source impedance <1kΩ VAVCC=1.8 ~3.6V	±5.5	±7	LSB
EO	Offset Error		±4.5	±7	LSB
EG	Gain error		±4.5	±7	LSB
ED	Differential linear error		±1.5	±2	LSB
EL	Integral linearity error		±2.5	±3	LSB

Table 3-45 ADC1_IN12~15, ADC12_IN8~11 Input Channel Accuracy @ fADC=8MHz

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
ENOB	Valid digits	In high speed action mode fADC=60MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=2.4 ~3.6V	10.6	-	Bits
SINAD	Signal-to-noise harmonic ratio		64	-	dB
SNR	Signal-to-noise ratio		66	-	dB
THD	Total Harmonic Distortion		-	-70	dB

Table 3-46 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy @ fADC=60MHz

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
ENOB	Valid digits	In high speed action mode fADC=30MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=1.8~2.4V	10.4	-	Bits
SINAD	Signal-to-noise harmonic ratio		62	-	dB
SNR	Signal-to-noise ratio		64	-	dB
THD	Total Harmonic Distortion		-	-67	dB

Table 3-47 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy @ fADC=30MHz

Symbols	Parameters	Conditions	Minimum value	Maximum value	Unit
ENOB	Valid digits	In ultra-low speed action mode fADC=8MHz Input signal frequency = 2kHz Input source impedance <1kΩ VAVCC=1.8~3.6V	10.4	-	Bits
SINAD	Signal-to-noise harmonic ratio		62	-	dB
SNR	Signal-to-noise ratio		64	-	dB
THD	Total Harmonic Distortion		-	-67	dB

Table 3-48 ADC1_IN0~3, ADC12_IN4~IN7 Input Channel Input Channel Dynamic Accuracy @ fADC=8MHz

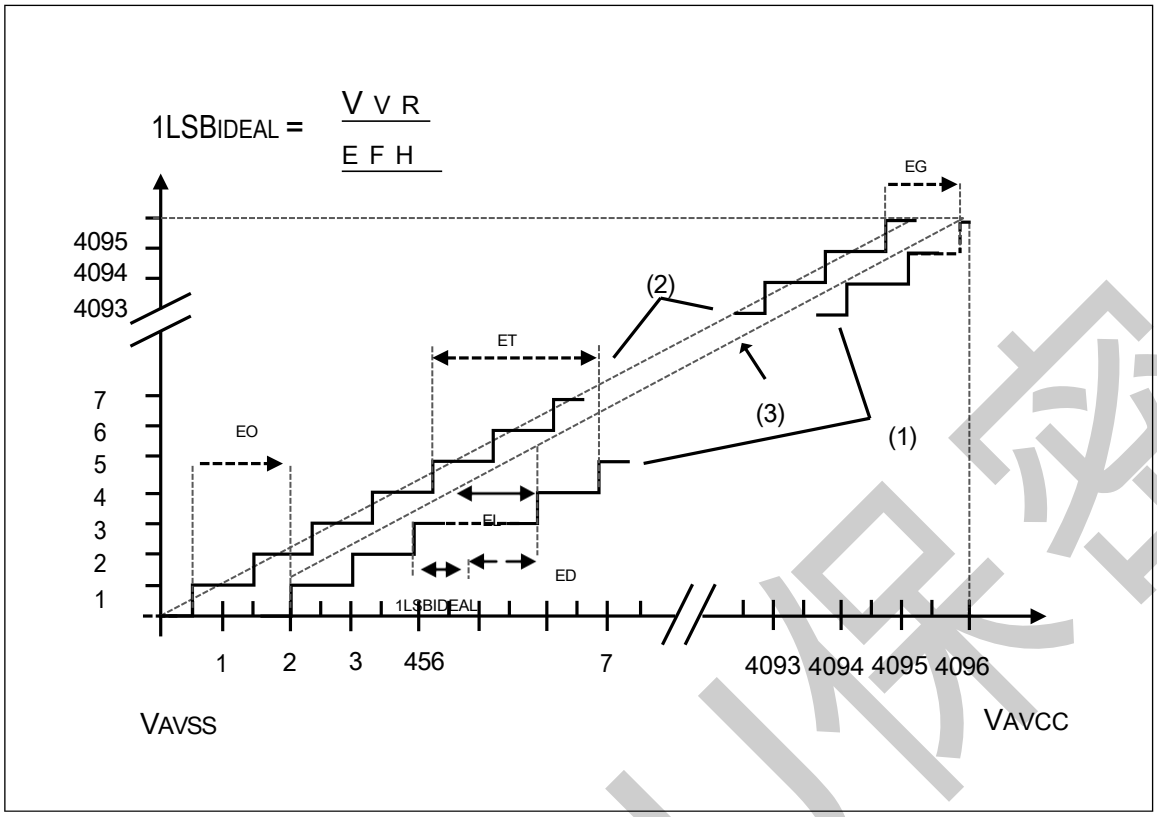


Figure 3-18 ADC Accuracy Characteristics

1. Please also see the table above.
2. Example of actual transmission curve.
3. Ideal transmission curve.
4. Endpoint correlation line.
5. $_{ET}$ = Total unadjusted error: the maximum deviation between the actual and ideal transmission curves.

   $_{EO}$ = Offset error: the deviation between the first actual conversion and the first ideal conversion.

   $_{EG}$ = Gain error: the deviation between the last ideal conversion and the last actual conversion.

   $_{ED}$ = Differential linearity error: the maximum deviation between the actual step and the ideal value.

   $_{EL}$ = Integral linearity error: the maximum deviation between any actual conversion and the endpoint correlation line.

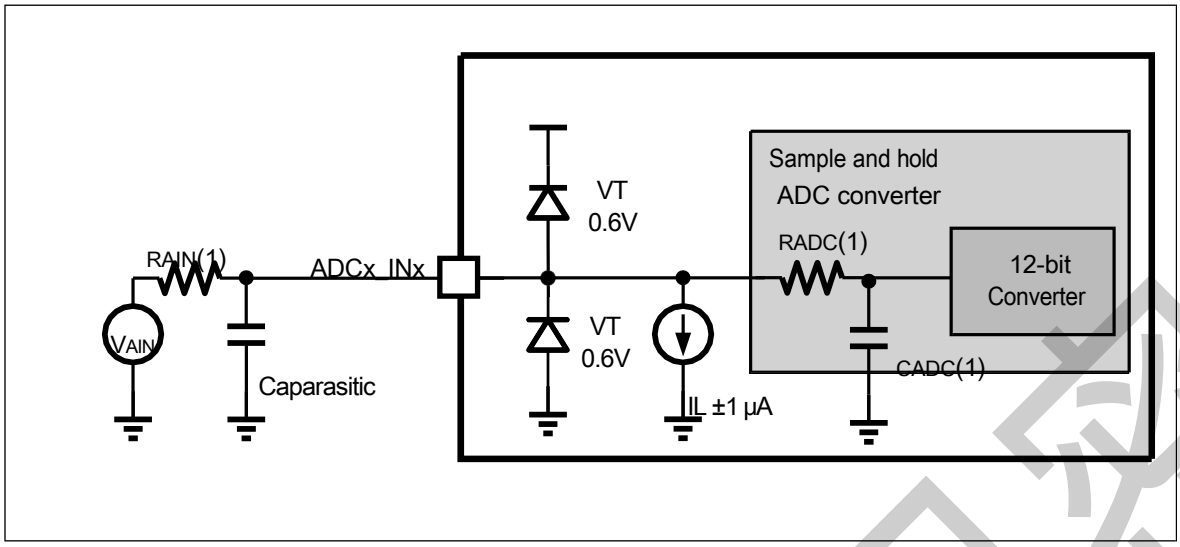


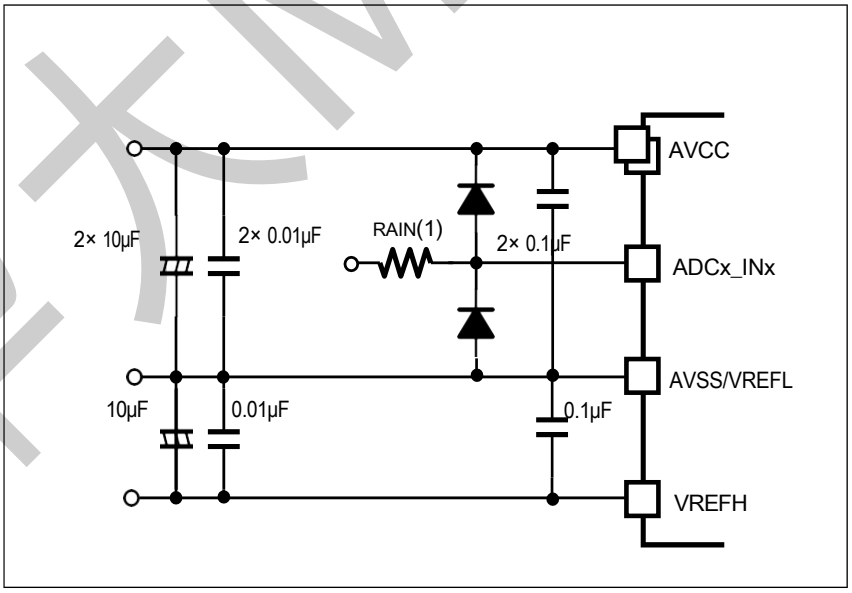
Figure 3-19 Typical Connection Using ADC

1. See Table 3-36 for information on R_{AIN}, R_{ADC}, and C_{ADC} values.
2. Cparasitic indicates PCB capacitance (depending on soldering and PCB wiring quality) and pad capacitance (approx. 5 pF).cparasitic

   Higher values result in lower conversion accuracy. To solve this problem, the fADC should be reduced.

General PCB Design Guidelines

The power supply should be decoupled as shown in the diagram below, depending on whether VREFH is connected to AVCC and the number of AVCC pins. 0.1μF capacitors



should be (high quality) ceramic capacitors. These capacitors should be as close to the chip as possible.

Figure 3-20 Example of decoupling power supply and reference power supply

3.3.18 DAC Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VAVCC	Analog supply voltage	-	1.8	3.3	3.6	V
DNL	Differential nonlinear error (deviation between two consecutive codes - 1LSB)	-	-	-	±2	LSB
Offset	Offset error (difference between the measured value at code (0x80) and the ideal value VAVCC/2)	-	-	-	±2	LSB
TSETTLING	Build-up time (full scale: applies to the ratio of the lowest input code to the highest input code by the time DA0/DA1 reaches its final value of ±4LSB) (Inter 8-bit input code conversion)	-	-	-	8	μs

Table 3-49 DAC Characteristics

3.3.19 Comparator Features

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
VAVCC	Analog supply voltage	-	1.8	3.3	3.6	V
VI	Input Voltage Range	-	0	-	VAVCC	V
Tcmp	Compare times	Comparator resolution voltage = 100mV	-	50	100	nS
Tset	Input channel switching stability time	-	-	100	200	nS

Table 3-50 Comparator Characteristics

3.3.20 Gain Adjustable Amplifier Features

Sym	Par		Con	Minimum	Typic	Maximum	Unit
VAVCC	Analog supply voltage		-	1.8	3.3	3.6	V
V (1) OS	Input derating voltage		-	-8	-	8	mV
VI	Input Voltage Range		-	0.1*VAVCC/Ga	-	0.9*VAVCC/Ga	V
GE	Gain error	Using the Mouth As a PGA Phase input	Gain=2(1)	-1	-	1	%
			Gain=2.133	-1	-	1	%
			Gain=2.286	-1	-	1	%
			Gain=2.667	-1	-	1	%
			Gain=2.909	-1	-	1	%
			Gain=3.2	-1.5	-	1.5	%
			Gain=3.556	-1.5	-	1.5	%
			Gain=4.0	-1.5	-	1.5	%
			Gain=4.571	-2	-	2	%
			Gain=5.333	-2	-	2	%
			Gain=6.4	-3.0	-	3.0	%
			Gain=8	-3.0	-	3.0	%
			Gain=10.667	-4.0	-	4.0	%
			Gain=16	-4.0	-	4.0	%
			Gain=32(1)	-7.0	-	7.0	%
		Use the Simulated AVSS as PGA Enter	Gain=2(1)	-2	-	2	%
			Gain=2.133	-2	-	2	%
			Gain=2.286	-2	-	2	%
			Gain=2.667	-2	-	2	%
			Gain=2.909	-2	-	2	%
			Gain=3.2	-2.5	-	2.5	%
			Gain=3.556	-2.5	-	2.5	%

			Gain=4.0	-2.5	-	2.5	%
			Gain=4.571	-3.0	-	3.0	%
			Gain=5.333	-3.0	-	3.0	%
			Gain=6.4	-4.0	-	4.0	%
			Gain=8	-4.0	-	4.0	%
			Gain=10.667	-5.0	-	5.0	%
			Gain=16	-5.0	-	5.0	%
			Gain=32(1)	-8.0	-	8.0	%

Table 3-51 Gain Adjustable Amplifier Characteristics

1. Mass production test guarantee.

3.3.21 Temperature Sensor

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
TL	Relative Accuracy	Each chip is individually calibrated according to the user manual	-	-	±5	℃

Table 3-52 Temperature Sensor Characteristics

3.3.22 Memory Features

3.3.22.1 Flash Memory

The flash memory is erased when the device is delivered to the customer.

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
IVCC	Supply current	Read mode, VCC=1.8 V~3.6V	-	-	5	mA
		Programming mode, VCC=1.8 V~3.6 V	-	-	10	
		Block erase mode, VCC=1.8 V~3.6V	-	-	10	
		Full erase mode, VCC=1.8 V~3.6V	-	-	10	

Table 3-53 Flash Memory Characteristics

Symbols	Parameters	Conditions	Minimum value	Typical values	Maximum value	Unit
T_{prog} (1)	Word programming time	Single Programming Mode	43+2* T_{hclk} (2)	48+4* T_{hclk} (2)	53+6* T_{hclk} (2)	μs
	Word programming time	Continuous programming mode	12+2* T_{hclk} (2)	14+4* T_{hclk} (2)	16+6* T_{hclk} (2)	μs
T_{erase} (1)	Block Erase Time	-	16+2* T_{hclk} (2)	18+4* T_{hclk} (2)	20+6* T_{hclk} (2)	ms
T_{mas} (1)	Full Erase Time	-	16+2* T_{hclk} (2)	18+4* T_{hclk} (2)	20+6* T_{hclk} (2)	ms

Table 3-54 Flash Programmed Erase Time

1. Mass production test guarantee.
2. T_{hclk} is 1 cycle of the CPU clock.

Symbols	Parameters	Conditions	Numerical value	Unit

			Minimum value	
Nend	Programming, block erase times	TA = 85°C	10	thousand times
Nend	Number of full erasures	TA = 85°C	10	thousand times
Tret	Data retention period	TA = 85°C	10	Year

Table 3-55 Flash memory rewritable times and data retention period

4 Package Size Diagram

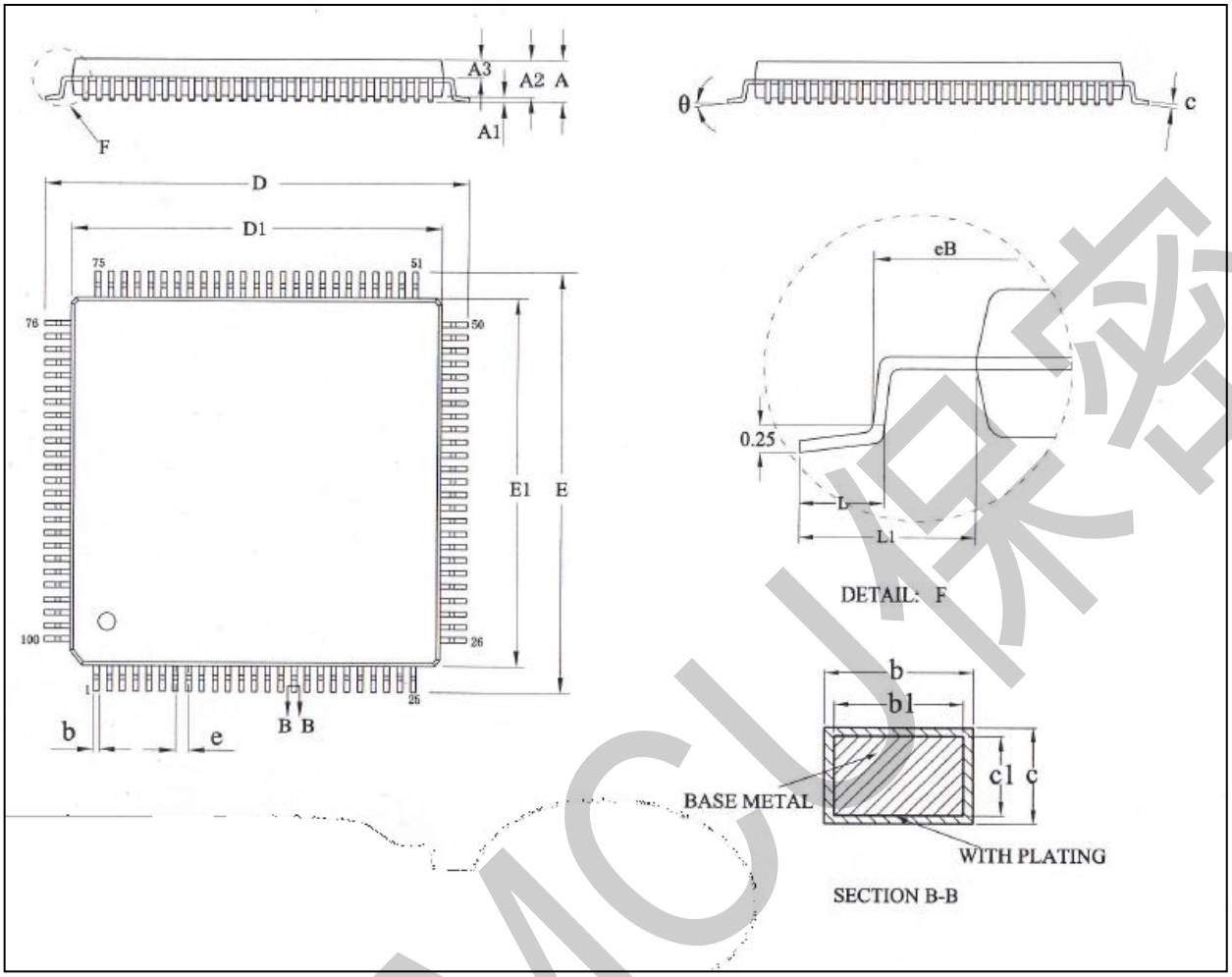


Figure 4-1 LQFP100L 14 x 14 mm 100-pin package outline

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Table 4-1 LQFP100L 14 x 14 mm 100-pin package mechanical data

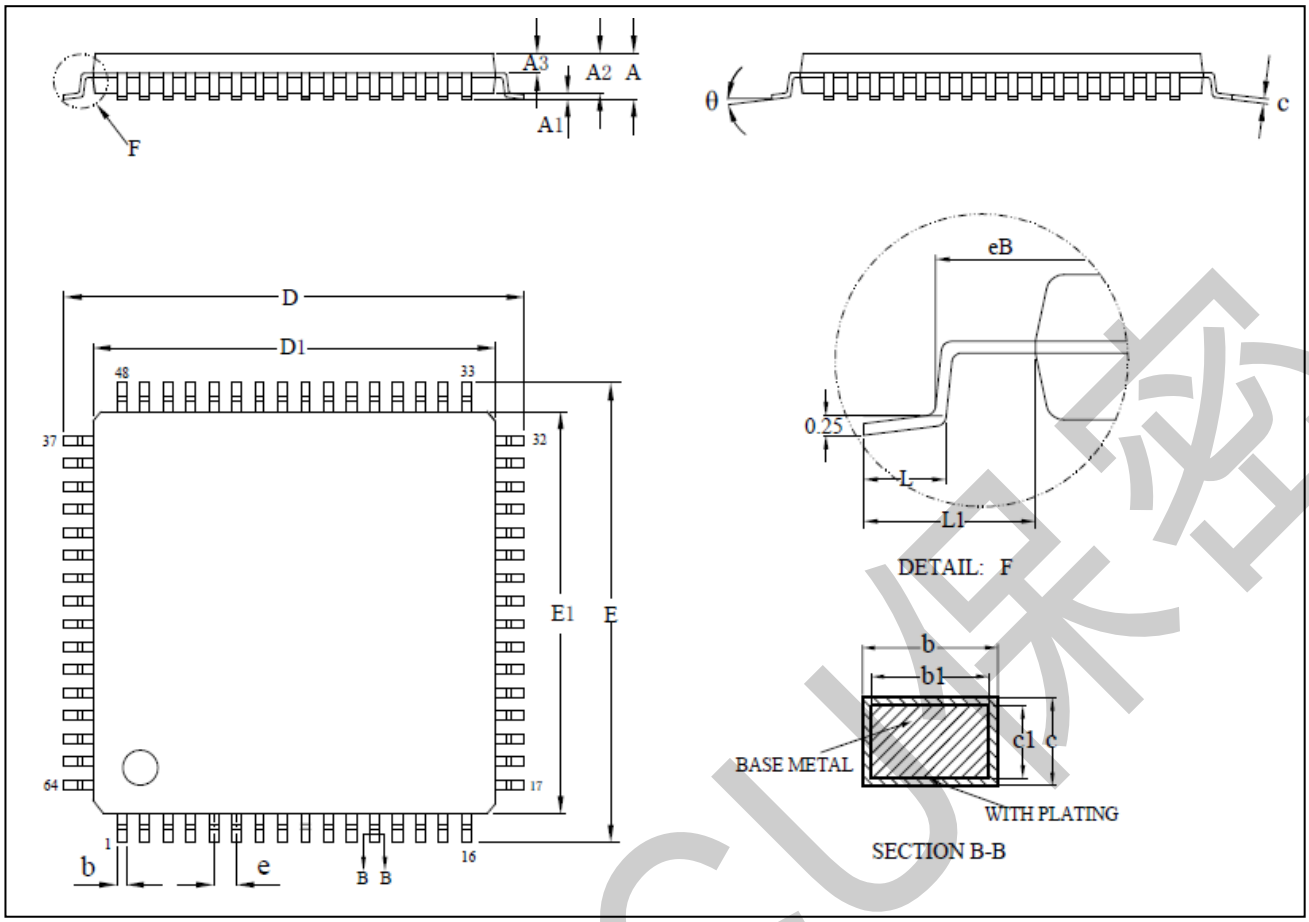


Figure 4-2 LQFP64L 10 x 10 mm 64-pin package outline

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.25	—	11.45
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Table 4-2 LQFP64L 10 x 10 mm 64-pin package mechanical data

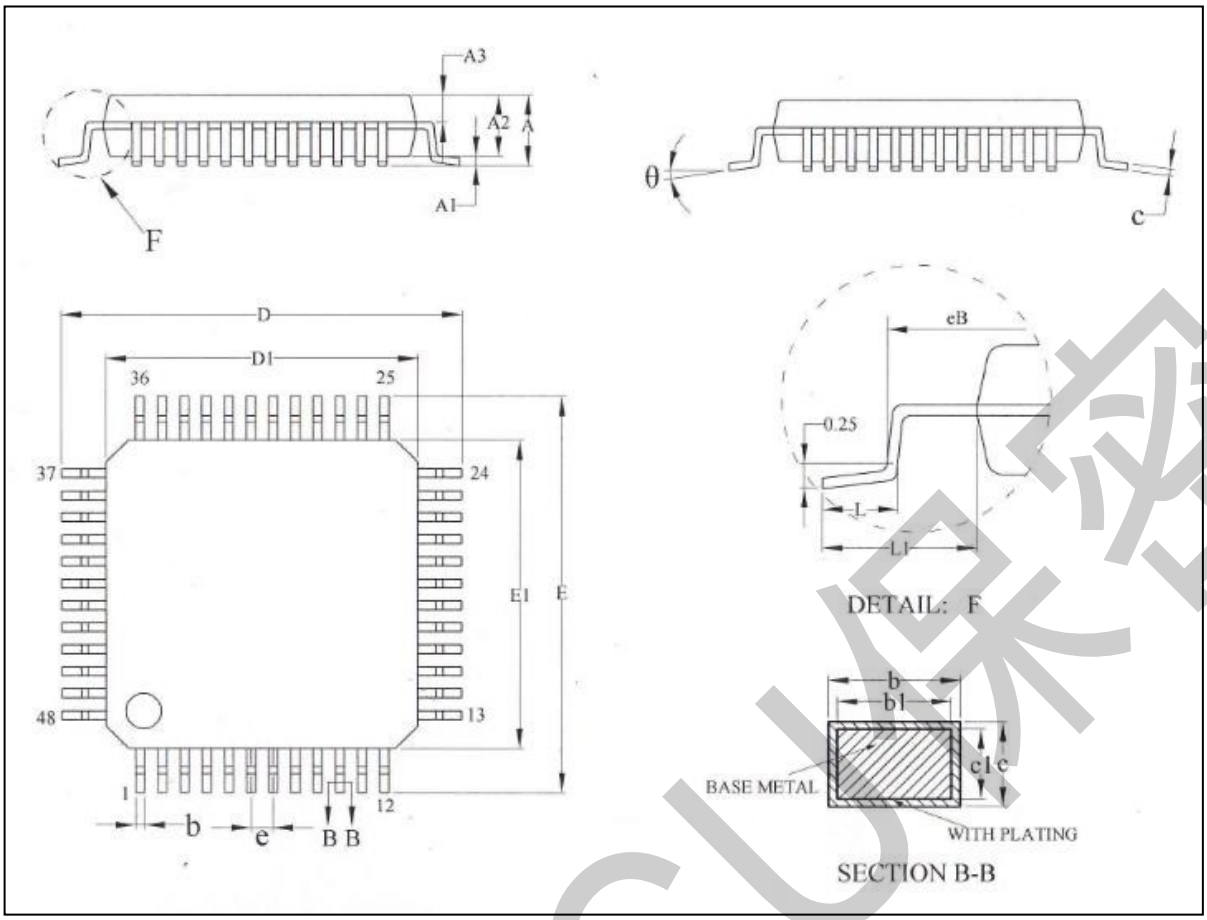


Figure 4-3 LQFP48L 7 x 7 mm 48-pin package outline

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
eB	8.10	—	8.25
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.40	—	0.65
L1	1.00REF		
θ	0	—	7°

Table 4-3 LQFP48L 7 x 7 mm 48-pin package mechanical data

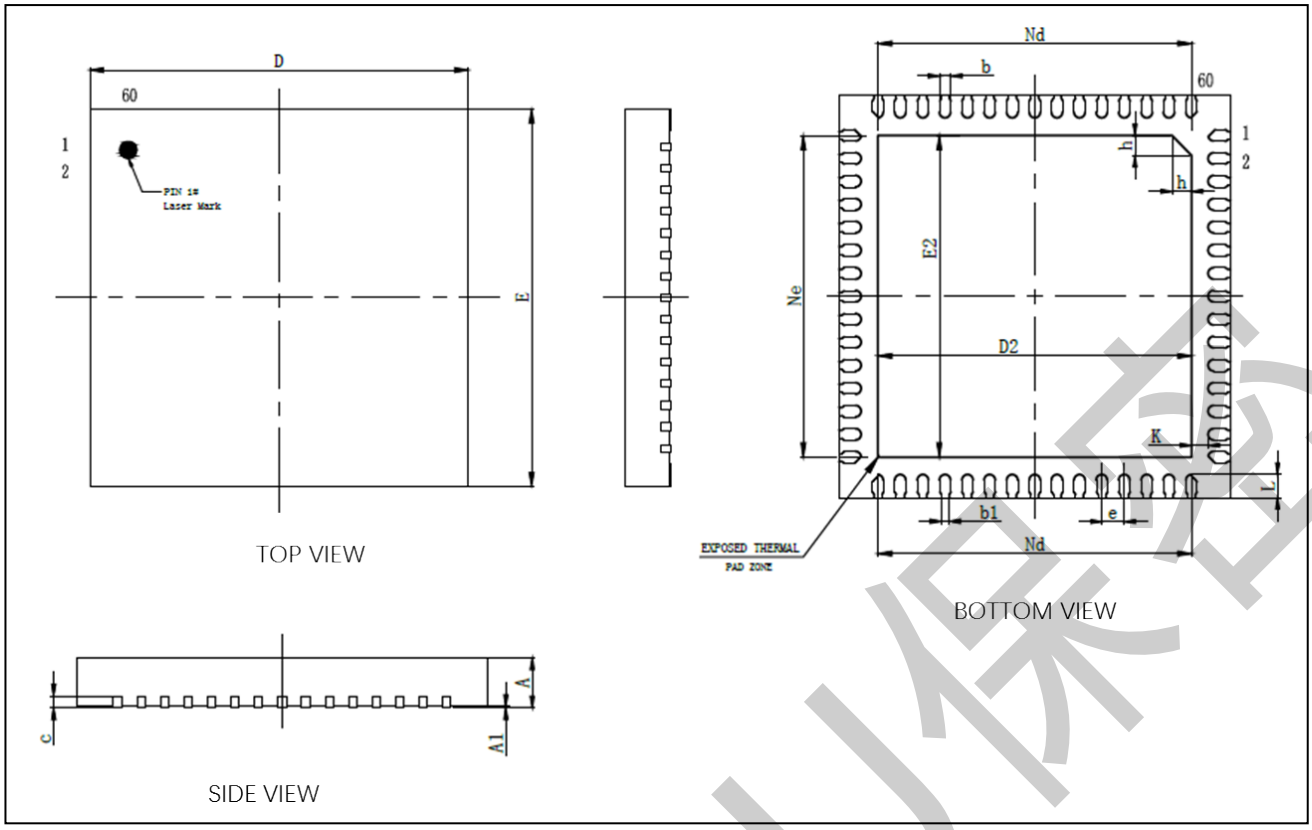


Figure 4-4 QFN60L 7 x 7 mm 60-pin package outline

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.14REF	
c		0.20REF	
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
Nd		5.60BSC	
e		0.40BSC	
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
Ne		5.60BSC	
L	0.35	0.40	0.45
K	0.25	0.30	0.35
h	0.30	0.35	0.40

Table 4-4 QFN60L 7 x 7 mm 60-pin package mechanical data

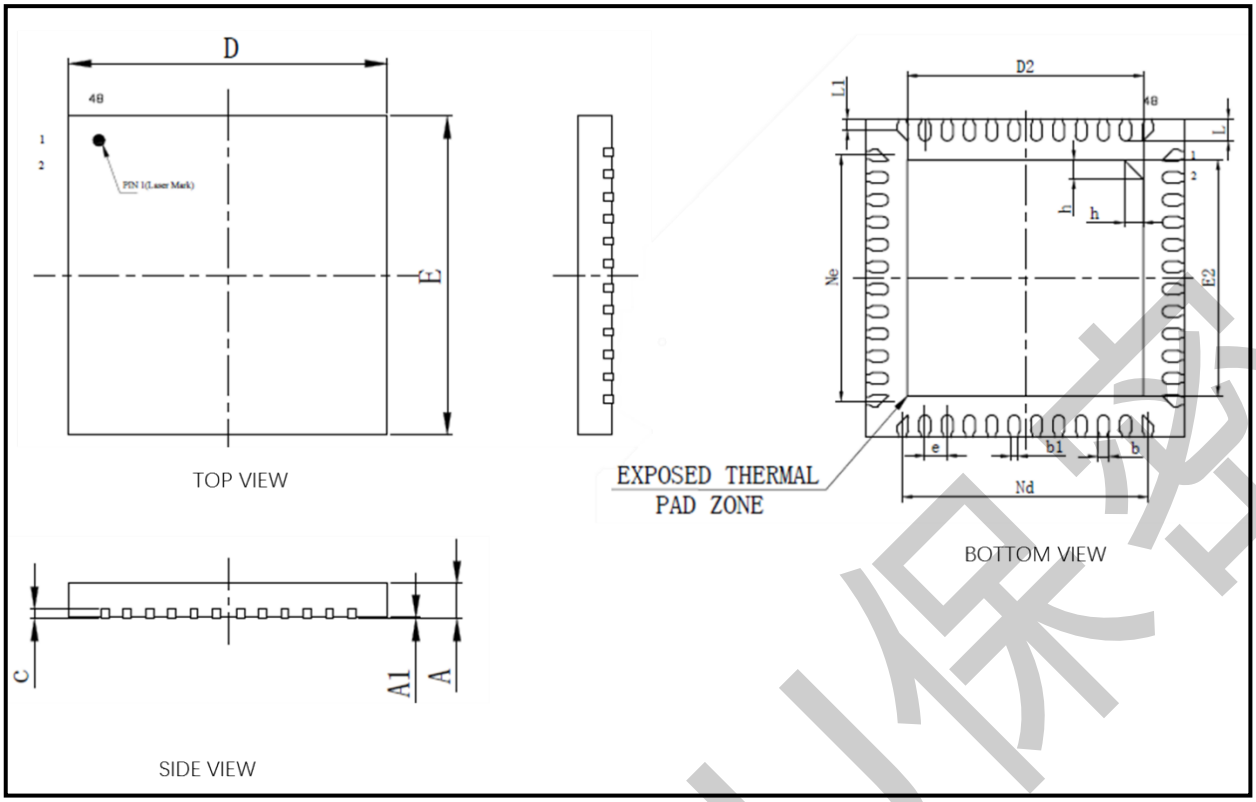


Figure 4-5 QFN48L 5 x 5 mm 48-pin package outline

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.13	0.18	0.23
b1		0.12REF	
c	0.10	0.15	0.20
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e		0.35BSC	
Ne		3.85BSC	
Nd		3.85BSC	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
载体尺寸 (mil)		154 × 154	

Table 4-5 QFN48L 5 x 5 mm 48-pin package mechanical data

5 Ordering Information

Product Model	HC32F460JEUA-QFN48TR	HC32F460JETA-LQFP48	HC32F460KEUA-QFN60TR	HC32F460KETA-LQFP64	HC32F460PETB-LQFP100
Main Frequency (MHz)	168	168	168	168	168
Kernel	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4	ARM Cortex-M4
Flash (KB)	512	512	512	512	512
RAM (KB)	192	192	192	192	192
OTP (B)	960	960	960	960	960
Package (mm*mm)	QFN48 (5*5) e=0.35	LQFP48 (7*7) e=0.5	QFN60 (7*7) e=0.4	LQFP64 (10*10) e=0.5	LQFP100 (14*14) e=0.5
General IO	38	38	50	52	83
Minimum operating voltage	1.8	1.8	1.8	1.8	1.8
Maximum working voltage	3.6	3.6	3.6	3.6	3.6
16-bit timer	11	11	11	11	11
Motor control timer	3	3	3	3	3
12-bit ADC conversion unit	2	2	2	2	2
Number of 12-bit ADC channels	10	10	15	16	16
Comparator	3	3	3	3	3
Amplifier PGA	1	1	1	1	1
SPI	4	4	4	4	4
QUADSPI	1	1	1	1	1
I S^2	4	4	4	4	4
I C^2	3	3	3	3	3
U(S)ART	4	4	4	4	4
CAN	1	1	1	1	1
SDIO	2	2	2	2	2
Full-speed USB OTG	1	1	1	1	1
DMA	8	8	8	8	8
DCU	4	4	4	4	4
LVD	√	√	√	√	√
AES128/192/256	√	√	√	√	√
SHA256	√	√	√	√	√
TRNG	√	√	√	√	√
CRC	√	√	√	√	√
KEYSCAN	√	√	√	√	√
RTC	√	√	√	√	√
FLASH Physical Encryption	√	√	√	√	√
Shipping method	Tape and Reel	Tray loading	Tape and Reel	Tray loading	Tray loading

Revised content

v1.1	Product Features External master clock crystal modified to 4~24MHz. 1. Introduction Standardize the case of the TIMER module designation. 2.1/2.2 100pin pins 27, 28, 64pin pins 18, 19 changed to AVSS, AVCC, original pin name VSSA changed to AVSS, VCCA changed to AVCC. 2.2 Delete the pin function name suffixes "_A", "_B", etc., and related usage restrictions. 2.2/2.3 Change the function names of JTAG, QSPI, etc. to be consistent with other sections. 3 Electrical characteristics update T.B.D value. 3.1.6 Power supply scheme update, add VCAP_1/VCAP_2 capacitor selection instructions. 3.3.6 External capacitor capacity update, low-power mode wake-up timing update. 3.3.10 I2C electrical characteristics update. 3.3.17 Increase the accuracy and dynamic characteristics of the 12-bit ADC in high-speed action mode with VCCA=1.8 ~2.4V and ultra-low-speed action mode.

Version Information & Contact information

Versions	Date	Summary of Revisions
v1.0	2018/12/28	Initial release.
v1.1	2019/4/12	Content updated, see revisions for details.

If you have any comments or suggestions in the process of purchase and use, please feel free to contact us.

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