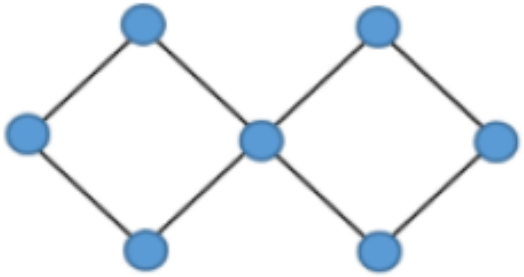
Reminder: Why having the integration milestones (waypoints)?

- Build highly complex system with strong interdependencies between different tasks.
- Make progress more visible, keep momentum high, and create short-term success stories.
- Develop common sense of what the most challenging & uncertain components are.
- Create awareness of incompatible interfaces.
- Foster team work, create common vision, and make teams deliver well-tested components in time.

How to define a meaningful waypoint?

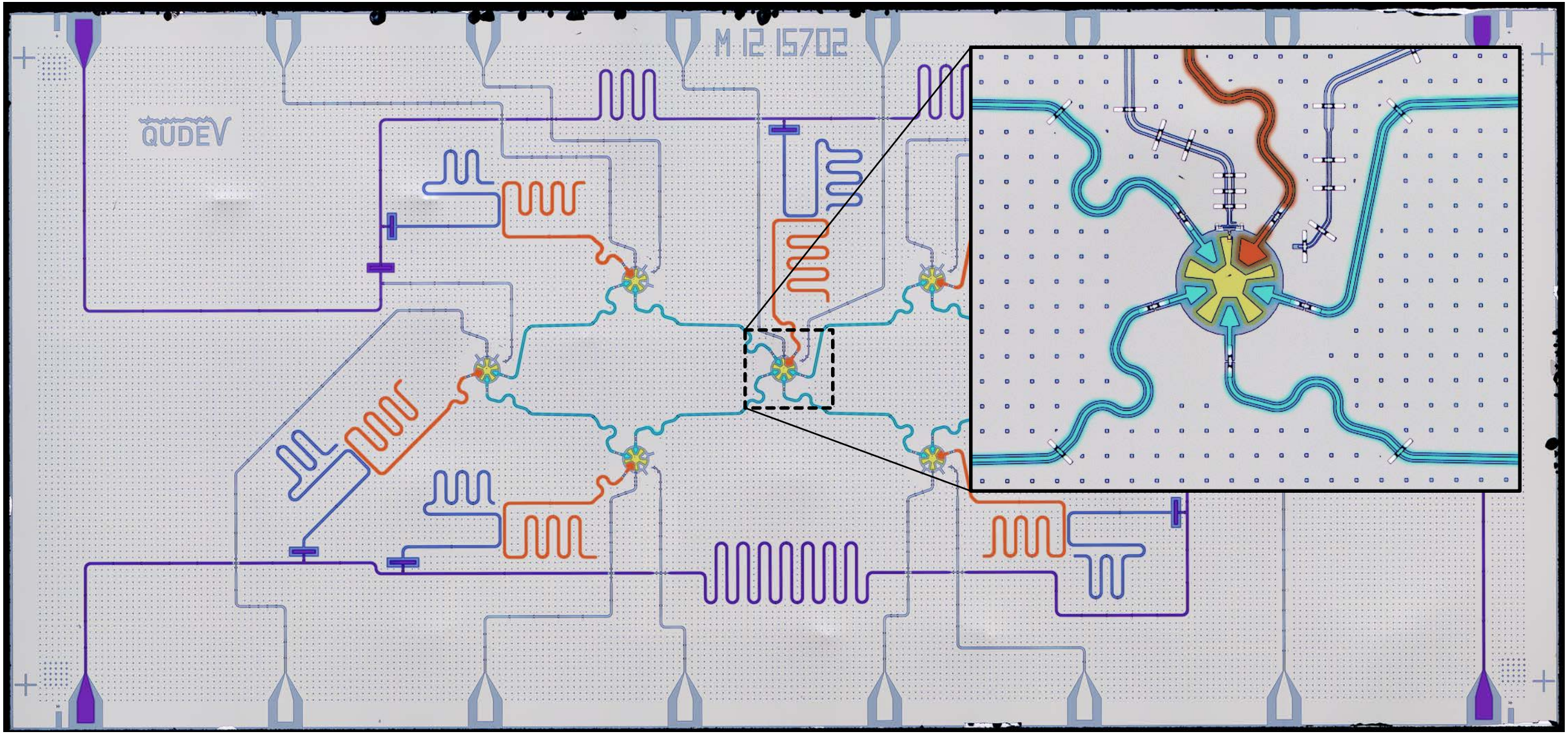
- Ideally all teams are involved and contribute to it.
- Achieve ambitious but realistic high-level goal, e.g. “Solve electronic structure problem x using VQE algorithm, measure quantum volume, … on 7-qubit quantum processor.”

Waypoint 1 (experiment consolidated at ETHZ)



- Chip (WP2)
  - … designed at ETHZ
  - … fabricated at ETHZ
  - Develop and test TSVs wafers (jointly by VTT/Chalmers)
- Operated in (WP3)
  - … XLD system with modular wiring scheme
  - … using custom components for filtering/shielding developed by ETHZ
- Controlled by (WP4)
  - … ZI equipment & using PycQED
  - Test and bring-up of ZI Programmable Quantum System Controller (PQSC).
- **Perform benchmarking and application inspired experiments (WP1 and ALL)**
  - **… with algorithms developed and tailored to 7Qubit Quantum hardware by theory teams.**

ETHZ Surface-7 chip



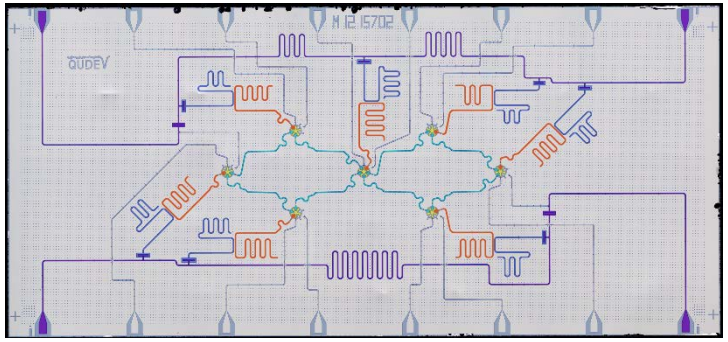
Qubit parameters

	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Qubit Frequency	5.731 GHz	5.849 GHz	4.919 GHz	5.142 GHz	5.299 GHz	4.361 GHz	4.562 GHz
Qubit Lifetime, T1	19 us	14.3 us	20 us	2.7 us	22 us	14.5 us	14.3 us
Qubit Coherence time, T2*	12.7 us	21.2us	16.5 us	2.9 us	14 us	24.2 us	14.9 us
Correct readout state assignment probability	91.4%	96.3%	97.8%	98.0%	95.0%	97.9%	95.1%

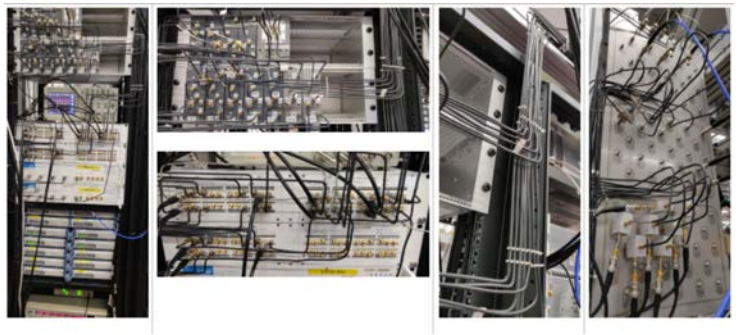
Lifetime of Q4 is significantly below our average lifetimes
(limits gates and readout)

Status Waypoint 1 at ETHZ

- WP2: Chip design & fabrication
  - First generation of 7 Qubit device fabricated and installed in the setup.
  - All elements are functional.
  - Coherence times are below target.
  - Design of 2nd generation of chip completed and fabrication in progress.



- WP3 and WP4: Setup and control electronics
  - Electronics setup fully integrated to control and measure 7 qubits.
  - Tune-up and characterization of 2Q gates in progress.



What remains to be done for successful completion of Waypoint1?

1) Integrate work on algorithms from theorists (WP1) & demonstrate application/benchmarking inspired experiment.
   - Ongoing work by USAAR on a potential QAOA (and optionally: volumetric benchmarking) experiment.
   - Experimetalists perspective: “Provide gate decomposition tailored to the hardware specifications of 7Q chip.”
   - “… and simulate expected performance under realistic conditions”

2) Technical developments and system integration
   - Bring-up and basic verification of PQSC in small test setup (ZI and ETHZ)
   - Conclude development and testing of TSVs (VTT & Chalmers)

Points to be discussed

- Status WP1 on algorithms and mapping to existing 7Q quantum hardware?
- Do we stick to the originally planned due date September 30?
- In which form do we want to wrap up the waypoint?
  - E.g. presentation + debriefing at meeting in Chalmers?