

Through Throw-away prototypes

(i) undocumented (ii) not quality ^{standard}

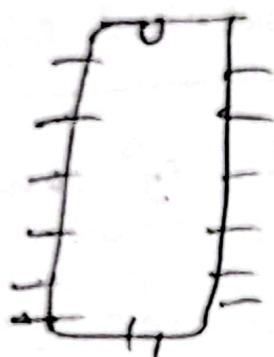
Boehm's spiral model. / Boehm's spiral model

Microprocessor and Interfacing

Lecture: 01

RM 02-11-22

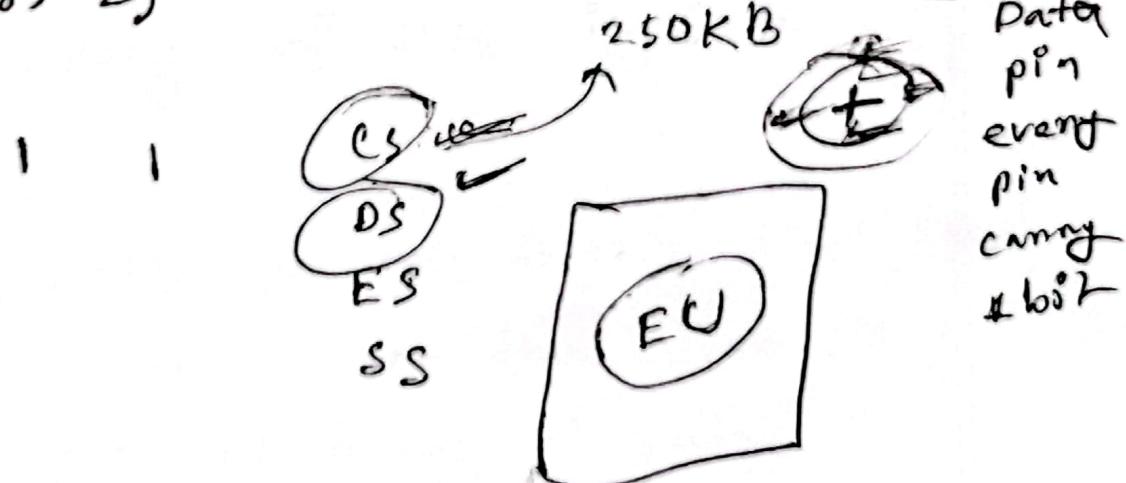
8086 mp overview.



$$2^{20} = 1\text{MB}$$

8086
1MB

Pages 28, 29



Name: MD Zuleyqine Abne Noman
Roll: 2002

Topic Name: Microprocessor

Day: _____
Time: _____ Date: / /

1. Briefly describe the overview of 8086 microprocessors.

Main Features of 8086:

1. 8086 is a 16-bit processor. Its ALU, internal registers work with 16-bit binary words.
2. 8086 has a 16-bit data bus. It can read or write data to a memory/port, either 16 bits or 8 bits at a time.
3. 8086 has a 20-bit address bus which means it can address up to 2^{20} bytes = 1 MB memory location.
4. Frequency range of 8086 is 6-10 MHz.
5. Like 8085, 8086 too can do only fixed point arithmetic as the IC of that time did not permit to put additional circuitry to do floating point operations.

Topic Name: Assignment - 1

Day:

Time:

Date: / /

6. The 8086 is designed to operate in two modes, minimum and maximum. In minimum mode, the 8086 processor works in a single processor environment. The maximum mode is designed to be used to work with the coprocessor 8087.
7. The 8086 works in a multiprocessor environment. Control signals for memory and I/O are generated by an external Bus controller.
8. It can pre-fetch up to six instruction bytes from memory and queues them in order to speed up instruction execution.
9. It requires +5V power supply.
10. It uses a 40 pin dual in line package.
- 8086 has two blocks
1. The Bus Interface Unit (BIU)
 2. The Execution Unit (EU)

Topic Name: Assignment - 1. Day: _____
Time: _____ Date: / /

The Execution Unit: Main components are -

1. General purpose registers.
2. The ALU
3. Special purpose registers.
4. The instruction registers.
5. Instruction Decoders.
6. The Flag/ Status Registers.

8086 has four 16 bit general purpose registers. A₁₅
BX, CX, DX which store intermediate values during
execution. Each of this has two 8-bit parts (higher
and lower)

- AX register : Combination of A_L and A_H Registers
- BX register : B_L + B_H
- CX register : C_L + C_H
- DX register : D_L + D_H

P.T.

Topic Name: Assignment - 1.Day: _____
Time: _____ Date: / /ALU:

Performs 8-bit and 16-bit arithmetic and logic operations.

Instruction Register and Instruction Decoder:

The EU fetches an opcode from the queue into the instruction register. The instruction decoder decodes it and sends the information to the control unit for execution.

Flag / status register:6 status flags

1. Carry flag.

2. Parity flag.

3. Auxiliary carry flag.

4. Zero flag.

5. Sign flag.

6. Overflow flag.

Topic Name: AS-1.

Day:

Time:

Date: / /

3 control flags

- Trap flag.

- Interrupt flag.

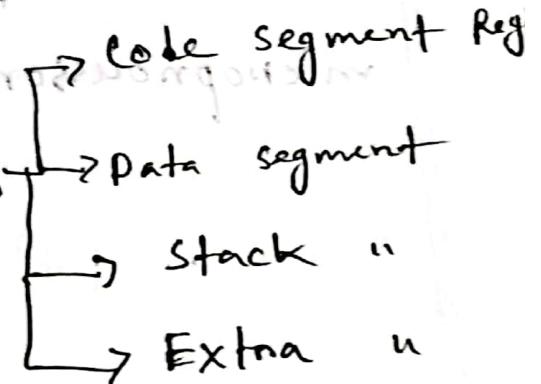
- Direction flag.

The Bus Interface Unit:

- It generates the 20 bit physical address for memory access.
- It fetches instructions from memory.
- It transfers data to and from the memory and I/O.
- Maintains the 6 byte pre-fetch instruction queue. (supports pipelining).

BIU contains

- 4 segment registers



- Instruction pointer

- Pre-fetch queue.

- Address Generation circuit.

Topic Name: AS-1

Day: _____
Time: _____ Date: / /

Question 2: Why physical memory size is 1MB for the 8086 microprocessor?

→ The 8086 has a 20 bit address bus. So it can address any one of 2^{20} or 1,048,576 memory locations.

We know,

$$1 \text{ byte} = 2^3 \text{ bits}$$

$$1 \text{ KB} = 2^{10} \text{ bytes}$$

$$\therefore 1 \text{ MB} = 2^{20} \text{ bytes}$$

Hence, the physical memory size for the 8086 microprocessor is 1MB.

Microprocessors and Interfacing

Topic Name: Software Engineering

Time:

Date: 9 / 11 / 2022

2.10 (Figure)

OS: chapter 9.10

Memory to memory

Illegal operation

MOV [1000] [2000]

Illegal

MOV BX [43 X A]

MARUT

Software Engineering

9-11-2022
Wednesday

Microprocessor

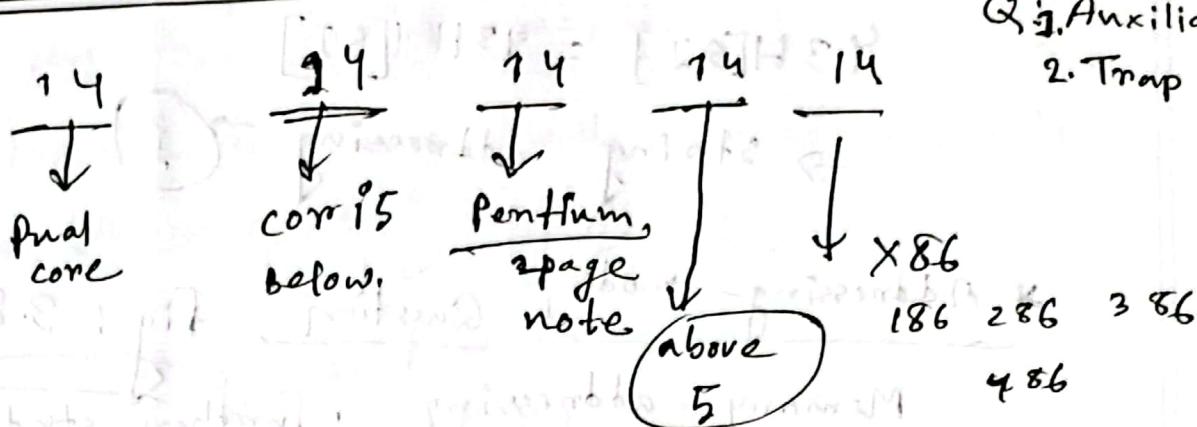
Simulation and Modeling

Topic Name:

Day:

Time:

Date: 14 / 11 / 22



- Q: Auxilany flag
2. Trap flag.

1. Pin diagram.
2. Memory size.
3. Registers.
4. Flag registers.

Next Monday.

OSWE OSSO MPO

80286: address bus, $2^{24} = 16 \text{ Mb}$.

Data bit/pin = 16.

80386: Data bit = 32.

① Address bus $2^{32} = 4 \text{ Gib - physical memory}$

80486:

(I) D+B: 32 + (co-processors)

(II) A+B: 2^{32}

8087, 80287, 60387

$$43H[S,I] = 43H + [S,I]$$

→ string addressing → ?

* Addressing mode, Question, fig: 3.8

Memory addressing : Further study → H.W.

N.C.: Assembly → soft copy for flag register.

* 4.30 - 5.00 % MP Assignment.

* 5.00 - 5.30 : among + programs,

* 5.30 - 7.00 % Soft SWE.

• DS = std. stack

• SS = std. stack

- do P. = first end words

• DS = std. stack (1)
 • SS = std. stack (II)

Topic Name:

Microprocessor and interfacing:

Time:

Date: 21/11/2022

chapter-2

MOV AX BX (0-15) flag register.

ADD AX BX
X₁₀ 16 bit

carry flag

emulator / Assemblers → used to run assembly language.

61 page

Source Operand → op code table এর মধ্যে রয়েছে।

General Register

General Register → YES.

4.1

Assembly language syntax

DB

Define byte.

DW

Define word.

DD

Define double word.

DQ

Define Quadword

DT

Define tenbytes.

Page 65: 4.4: Memory Models

SMALL, + Code in one segment
data in " " "

medium
COMPACT
LARGE

HUGE → more than one segment >
may longer. 64 bytes

4.7.2 Data segment:

.DATA

WORD1

WORD2

MSG

MASK

DW 2

DW 5

DB 'This is a message'

4.7.3 Stack Segment

stack 100H

CS
DS

stack 100H

SS

4.7.4 Code Segment

.CODE name

Page 69

MOV AH, 2 ; display character function

MOV DL, '?' ; character is '?'

INT 21H ; display character.

Read a character:

MOV AH, 1 ; read character function
INT 21H

MOV BL, AL ; save it in BL

<u>ASCII code (Hex)</u>	<u>Symbol</u>	<u>Function</u>
7	BEL	beep (sounds a tone)
8	BS	backspace
9	HT	tab.
A	LF	line Feed (new line)

Page - 29

Print String Program

; return to DOS

MOV AH, 4CH

INT 21H

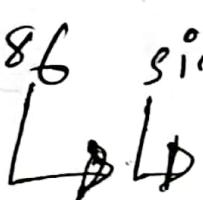
4.12

case conversion

Program

Page - 26

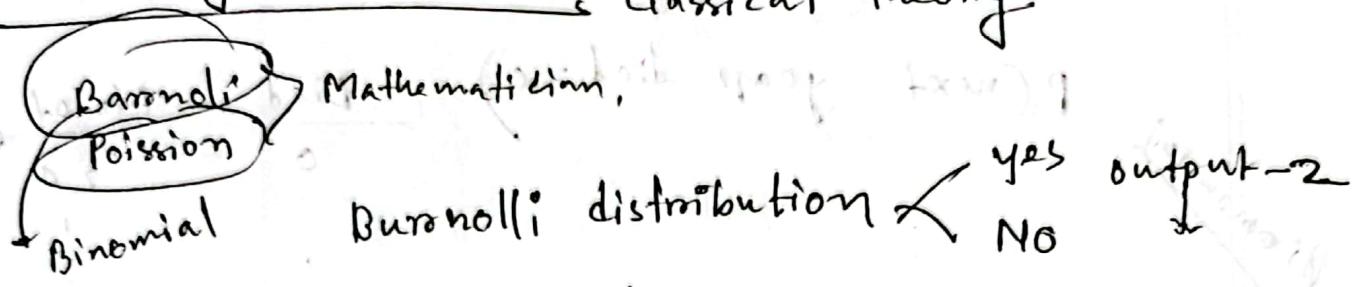
case conversion Program → Program



Uppercase to
lowercase

Jump Operation. Chapter - 4

Probability distribution, classical theory



Binomial distribution.



with 5 C₂

$$1 \times (0.25)^5$$

$$P(S)$$

$$P(Y) = P(N)$$

$$\checkmark = \binom{m}{x} P^x (1-P)^{m-x}$$

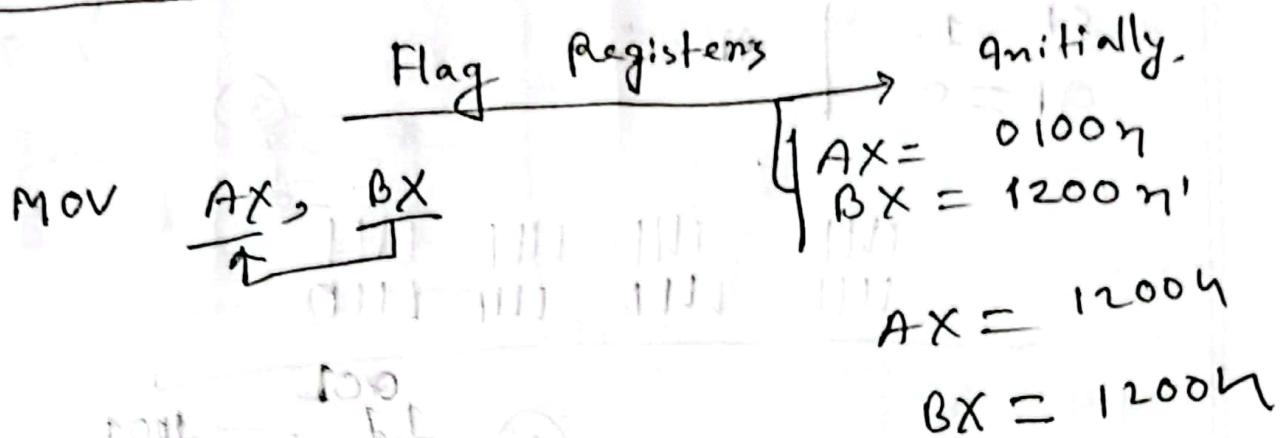
conditions \rightarrow check.

$$\binom{3}{3} P^3 \cdot P(N)$$

$$P(B) = 0.2 \\ P(N-B) = 0.8$$

$$\checkmark = \binom{3}{3} \cdot (0.2)^3 \cdot (0.8)^0$$

The Processor status and the flags register's



Instructions

MOV / XCHGADD / SUBINC / DECNEG.Affects flags

none

All (6 flags)

all

all except CF

all (CF = 1 unless result is 0)

OF = 1 if word operand is 0000

8000H or byte -

Control

 $\overbrace{\text{FF}}$
 $\overbrace{\text{9F}}$
 $\overbrace{\text{DF}}$

5.2: Example

ADD AX, BX,

(1) $1111\ 1111\ 1111\ 1111$; $1000\ 1111\ 1111\ 1111$
 ↓ ↓ ↓ ↓
 1 0 1 0
 ↓ ↓ ↓ ↓
 1 0 0 0

SF = 1

P.F = 0, because there are 2 odd numbers of 1's in the low byte of the result.

Day : _____

Topic Name : _____

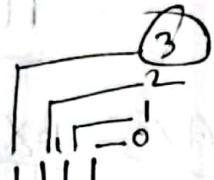
Time : _____

Date : / /

$ZF = 0$ because the result is non zero.

 $CF = 1$. $OF = 0$ AF

1111	1111	1111	1110
1111	1111	1111	1110


 $1101 - 1101$
 $\begin{array}{r} 1101 \\ \hline 1101 \end{array}$

$\therefore AF = 1$

Sign Flag, HP_{MSB-1} , $SF = 1$.

$SF = 0$, $msb = 0$

SHL — Shift left

SHR " Right.

$SHL = 2$

 1001
 0100
 $\underline{\underline{0010}}$
 0010
 $\underline{\underline{0100}}$

$SHR = 2$

Topic Name : C

Day :

Time :

Date :

MOV CX $\underline{\underline{0604}}_H$
MOV AX $\underline{\underline{0B98}}_H$
SHL AH CL
ADD CX AX

$\overline{0}, \overline{1}, \overline{0}, \overline{0}, \overline{0}, \overline{0}$
CF PF AF ZF SF
--- = --- - - - [For 1st instru]
--- - - - T+ [I-2]

SHL

$\underline{\underline{0B}}$
 $\underline{\underline{0000}} \quad \underline{\underline{1011}}$

SHL \rightarrow
MSB \leftarrow LSD
SHR MSB \rightarrow LSD

00101100

✓

1011 0000

B 0

AX = B098

CX = 0604

AX = B098

0000, 0110 ; 0000, 10100
1011, 0000 ; 1001, 1000

1011, 0110 ; 1001, 1100

AF = 0

B ; 6 ; 9

Topic Name : _____ Day : _____

Time : _____ Date : / /

MOV CX 1003H	CF	PF	AF	ZF	SF
MOV AX 8FOAH	-	-	-	-	-
SHR AL CL	0	0	0	1	0
ADD CX AX	0	0	0	00	1

8F 03 AL = OA

~~1000 1111~~
~~0100 0111~~
~~0010 0011~~
~~0001 0001~~

~~= 0000 1010~~
~~= 0000 0101~~
~~= 0000 0010~~
~~= 0000 0001~~

AL → 0 1

~~0001 0000 1101~~
~~1003 = 0001 0000 1000 0110 0011~~
~~1000 1111, 0000 0001~~

1001 1111 { 0000 0100

9 F 0 4 → X
80C4 → X

Chapter - 6, 7 (Logic Instructions), 9 (Multiplication and Division)

Manu → Example Practice 4010 224,

HW → OF → Overflow flag.

Overflow Bit :

0 0 > 0 1 8

$$OF = 1$$

is too large to fit in the number of bits

Otherwise $OF = 0$

$$\begin{array}{r} \text{or} \\ \overbrace{11111111}^{\text{or}} \end{array} \rightarrow OF = 1$$

$OF = 0$, 6, 7 both generate carry,
or both not generate carry.

$$\begin{array}{r} 0101 \cdot 1100 \quad (5Ch) \\ 0100 \quad 0101 \quad (45h) \\ \hline 10100002 \quad (A9h) \end{array} \begin{array}{l} \text{carry} \\ 6 \rightarrow 7 \end{array}$$

$$\therefore OF = 0,$$

$$\begin{array}{r} \text{or} \\ OF = 0 \end{array}$$

Ex-3 92 -

$$\begin{array}{r} 0101 \quad 1100 \\ 1100 \quad 0101 \\ \hline 100100001 \end{array}$$

0 0 1

$$\begin{array}{r} \cancel{0}100101 \\ 01000101 \\ 10111010 \\ \hline 10111011 \end{array}$$

Topic Name : _____ Day : _____

Time : _____ Date : / /

0101 1100

1100 0101

1100 0101

0101 1100

1010 0011

+1

10100100

50 - 80

32

nuanced; wrong

Input - 8h

0101 1100

1010 0100

10000 0000

69

- 92
—
— 23

AOD

50h

32h

00110010

00100000

0101 0010

0101 0000

0011 0020

1000 0020

Wednesday

8

2

82
82

Topic Name:

Microprocessors and Interfacing

Time:

Date: 30/11/2022

MOV AX BX

source &
destination of AX

Addressing mode
check.

language.

MOV AX BX → opcode generate → actual
machine

MOV → opcode → 6 bit

Add

Sub

LEA

MUL

SDIV

INC

JMP

D: Direction

to AX (1)

from BX (0)

D=0

D=1

MOV AX [Z4]

to AX

from [Z4]

D=0/1

= 1 (target

word
register).

W → Byte / Word

MOV AX BX

AL/Ah, BH, BL

Byte

word
operation
46 bit

Figure: 3.2.6

~~AX 000~~

$W \rightarrow 1 \leftarrow \text{word}$, ~~000~~ — AX register.

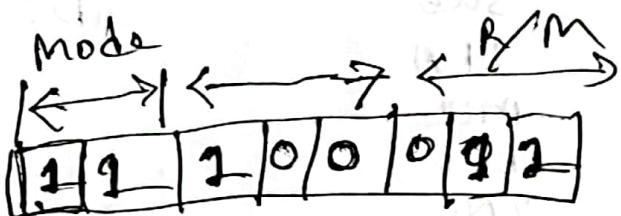
$W \rightarrow 0 \rightarrow 000$ ~~000~~ — AL

MOV SP BX

Byte 1 Byte 2

$\Rightarrow 0 = 1$

~~1 0 1 0 0 1 2 0 1 1~~



MOV AX word

BL (0) BX

(0) AX word

[PF] word

$\Rightarrow 0 = 6$

$\Rightarrow 0 = 1$
Registers & Mode

From BX

Mode neg R/M

~~1 0 0 0 1 0 0 1 1 1 0 1 1 1 1 0 0~~

Op code

Topic Name : _____

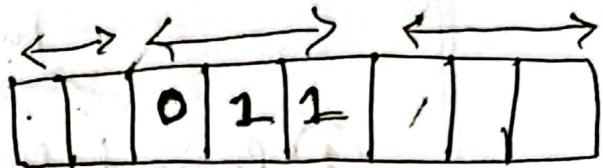
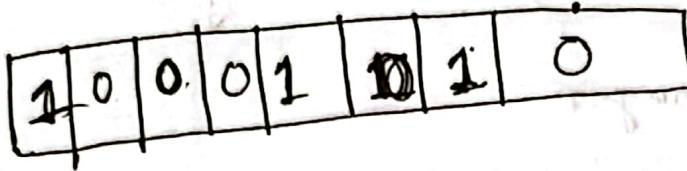
To Day : _____

Time : _____

Date : / /

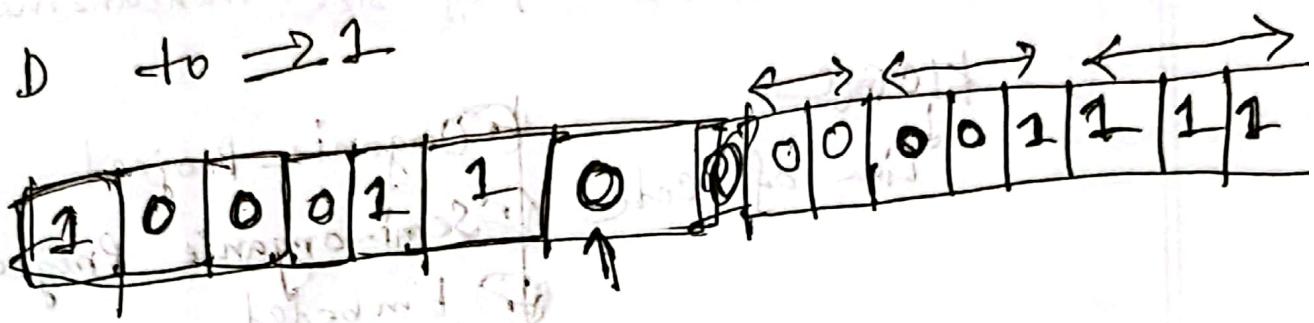
From

MOV CL [BX]



MOV CL [BX]

D → 21



Next lab: Sunday

Interpret (1), trap (1), trap (1) 2 question
with traps (1) with traps (1) with traps (1)

942 938 974

742 + 970 = 9718

743 + 10.0 + 200 = 945

Interpret
trap
trap
trap

? what is it?

Lab
Topic Name: Microprocessor and interfacing Day: _____
Time: _____ Date: 9/22/2022

9-12, 11-12, 18-12 Exam: 1st Exam (Lab-Exam-1)
(AH, AL) - register (Registers).

MD Zuleyeneen Ibne Norman.

Bangladesh

Gazipur

Mirzapur, Dhaka - 1216

Middle Paikpara, 42/1

45, 45 45, 45

$$\begin{array}{r} 127 \\ 111 \\ \hline 238 \end{array}$$

Goal

XOR BX, BX

MO cl, 4

→ 0000 0001
clear BX // BX will hold

binary value.

Input a character // 0 or 1

while character <= 0

Convert character to binary value.

left shift BX 4 times.

Insert value into lower 4 bits of BX.

Input a character.

END_while

find 13 - 16

Topic Name : _____

~~MOV BX, 0~~

Mov cl, 4

'Print "Enter Hex Number";'

MOV AH, 1

FOR 1^o

921 244

· CMP AL, ODH

JE END-FOR

DO

1100 0000 ←

10000001

000000.11

2010-2011

100

~~o~~ - ~~32d~~ p xg flint 1721

⇒ Class Room ~~प्र०~~ code

Sab 265

ଶ୍ରୀ କର୍ଣ୍ଣାନୀ

- ~~sp~~ sub mif.

Topic Name :

Microprocessors and

Interface

Day:

Time:

Date:

/ /

Opcode

3.11 Figure

MOV 43H[SI], DH

Exercise: ~~12 → (b,c)~~ — Practice 40, P 270
~~offset/effective~~

MOV 43H[SI], DH
Memory Register.
To

Offset/effective address.

[SI] 20000H
+ 43H 43

B-1 B-2 B-3 B-4

D8 — Displacement 8 bit

SI + D8

`MOV CX [432A4H]`

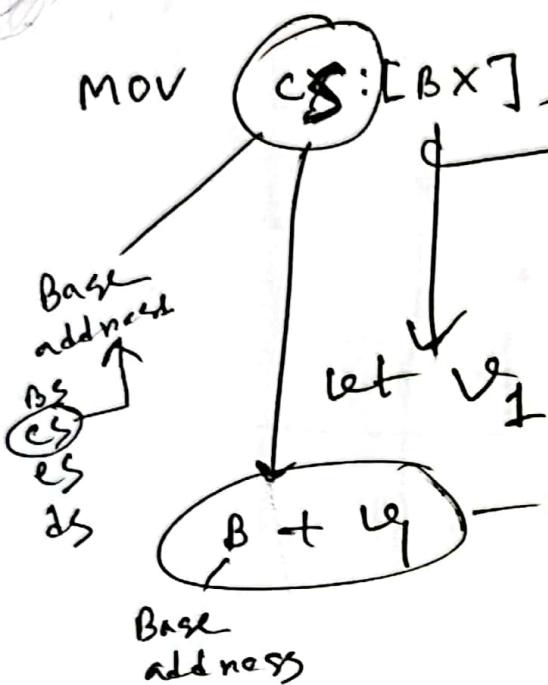
$\downarrow 16$ ← direct address.

Byte 4

Byte 3

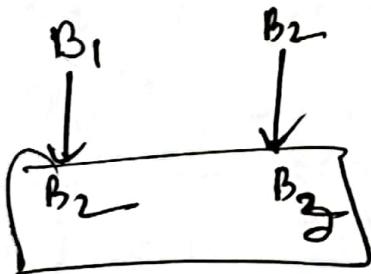
`MOV CS:[BX], DL`

Indirect.



(Byte 2, Byte 3)

Byte 1, Byte 2 replace
Byte 1, Byte 2



Op code.
10010110

$B_1 \rightarrow$

001 XX110

01

Roll No: 2002

Topic Name: MPI Assignment

Day:

Time:

Date: 11/12/2022

Instruction	AF	SF	OF	ZF	PF	CF
MOV AL, 04	-	-	-	-	-	-
INC AL	0	0	0	0	1	0
MOV BL, FE ₁₆	-	-	-	-	-	-
DEC BL	0	1	0	0	0	-
ADD AL, BL	1	0	0	0	0	1
SUB AL, BL	0	0	0	0	1	1
NEG AL	0	1	0	0	0	0

①

0	0	0	0	1	0	0
---	---	---	---	---	---	---

 AL register

②

0	0	0	0	0	1	0	1
---	---	---	---	---	---	---	---

 AL register

③

1	1	1	1	1	1	0	0
---	---	---	---	---	---	---	---

 BL register

④

1	1	1	1	1	1	0	1
---	---	---	---	---	---	---	---

 BL register.

⑤ AL 0000 0101
BL 1111 1101

① 0000 0010
Carry

⑦ NEGAL ; AL \Rightarrow 05h
AL = 0000 0101
1's complement 1111 1010
2's complement +1

1111 1010

⑥ AL 0000 0010
BL 1111 1101

① 0000 0101
Carry

CF = 0 , OF = 0's sign

$02H \rightarrow 2$ Decimal

$FDH \rightarrow 253$ Decimal.

$1111\ 1101$

$\begin{array}{r} 0000\ 0010 \\ +1 \end{array}$

$\begin{array}{r} 0000\ 0011 \\ 0000\ 0010 \end{array}$

$0000\ 0101$

$1111\ 1010$

$1111\ 1011$

253

$+2$

-251

Logical shift operations

$AF \rightarrow$ undefined.

$SF, PF, RF \rightarrow$ reflected the result.

$CF =$ last bit shifted out.

$OF = 1$ if result changes sign on shift.

Example

7.2

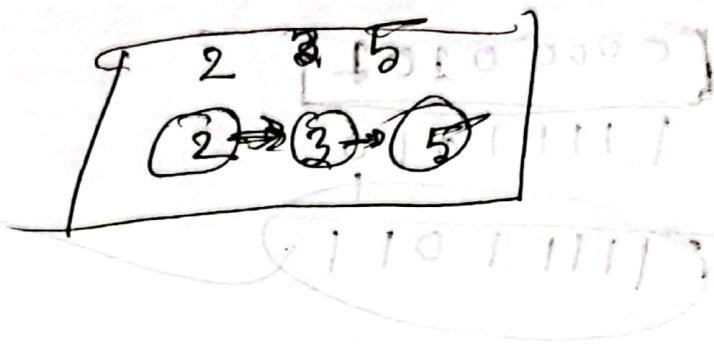
Chapter - 7

$$8 \times 10 = 80$$

Multiplication by left shift.

$$\begin{array}{r} 12 \rightarrow \\ \quad \quad \quad 1100 \\ \quad \quad \quad \quad \quad 00 \\ \hline \begin{array}{r} 11000 \\ 16 \overline{) 8} \\ = 24 \end{array} \end{array}$$

11101



Example : 8.8

$$0000\ 0000 \quad 0000\ 1100 \quad \xrightarrow{\text{W=0130, AX=72}}$$

SAL ~~shift left~~ and ~~shift right~~ SRL

$$\begin{array}{r} 1100 \\ 1100 \\ 1100 \\ 1100 \\ \hline 16+8=24 \end{array}$$

11001100

$$\begin{array}{r} 01101000 \\ 11001100 \\ \hline 11001100 \end{array}$$

① overlaps

Interfacing Lab

Topic Name: Microprocessor and 8085 Day: _____
Time: _____ Date: / /

ch-9 (Marud)

SF, ZF, AF, PE: undefined

CF/OF:

After mul with $CF/OF = 0$ if the upper half
of the result is zero
 $= 1$, otherwise

" " 9mul, $CF/OF = 0$, if the upper
half of the result is

Example

MUL source

9.1

$$AX = FFFFH$$

$$BX = FFFFH$$

~~MUL BX~~ 4294836225 FFF

8086 Unconditional Jumping Instructions

4.8 4.8

Fig-4.8

JMP Back BACK

4.10 table

Mnemonic

Condition

tested

Jump if

JA/JNBE

(CF or ZF) = 0

above
not
below
non
equal.

4.11

table (like 13 column)

compare CX, BX

condition,

CX > BX 1

ZF

0

CX < BX 0

0

CX = BX 0 1

Near ()

Segment to this segment

far ()

(segment to diff segment)

Page → 4.9 → Fig 4.7

Opcode @mt Ex memorize
রাগতৃষ্ণ

NOP ? Non operation.

JMP → 2

$$\begin{array}{r}
 0000\ 0000\ 0000\ 00000110 \\
 +1111\ 1111\ 1111\ 1111001 \\
 \hline
 1111\ 1111\ 1111\ 1111010
 \end{array}$$

4.10 → 1st column

4.9 → 90 80(5)

EBH → FAH

E9 → 16 bit (90 00)

Jump (90) → opcode for 8 bit

Near Indirect

mem-low

mem-high

8bit

16bit

→ chapter - 3

→ op1 op2 op3

QMN → 3.18 → D.W, 0

level

Assume

modulen

Editors, short

Assemblers - not

Jmp

and call

jmpq jump table 2¹⁸; 23

Quiz 2:

(10-01-2023)

start part 2¹⁸

exam

MP1 ~~but~~ theory

Syllabus:

Flag registers

vinc/DIV Rotation

Opcode generation - JUMP

Lab exam

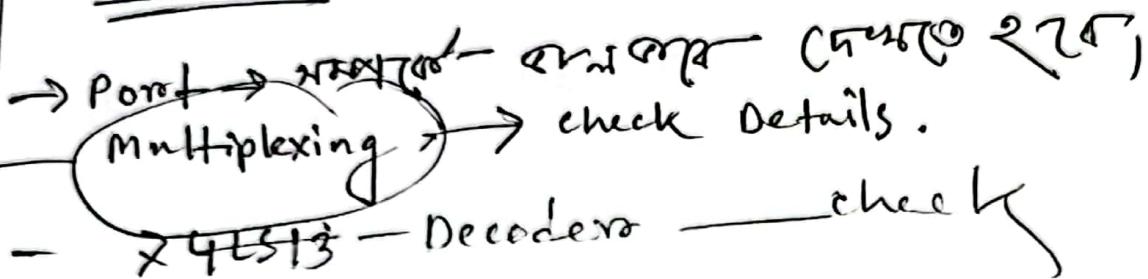
Next ~~program~~ lab exam

8-01-2023 exam evaluation
continuous

9.10

8086 Interrupts and Interrupt

Response .

ch-10: Digital Interfacing.ch-8

(i) Software Interrupt

(ii) Hardware Interrupt

8255 (Priority Interrupt)
working procedureFig : 10.1STB → low (\ominus negt) sig

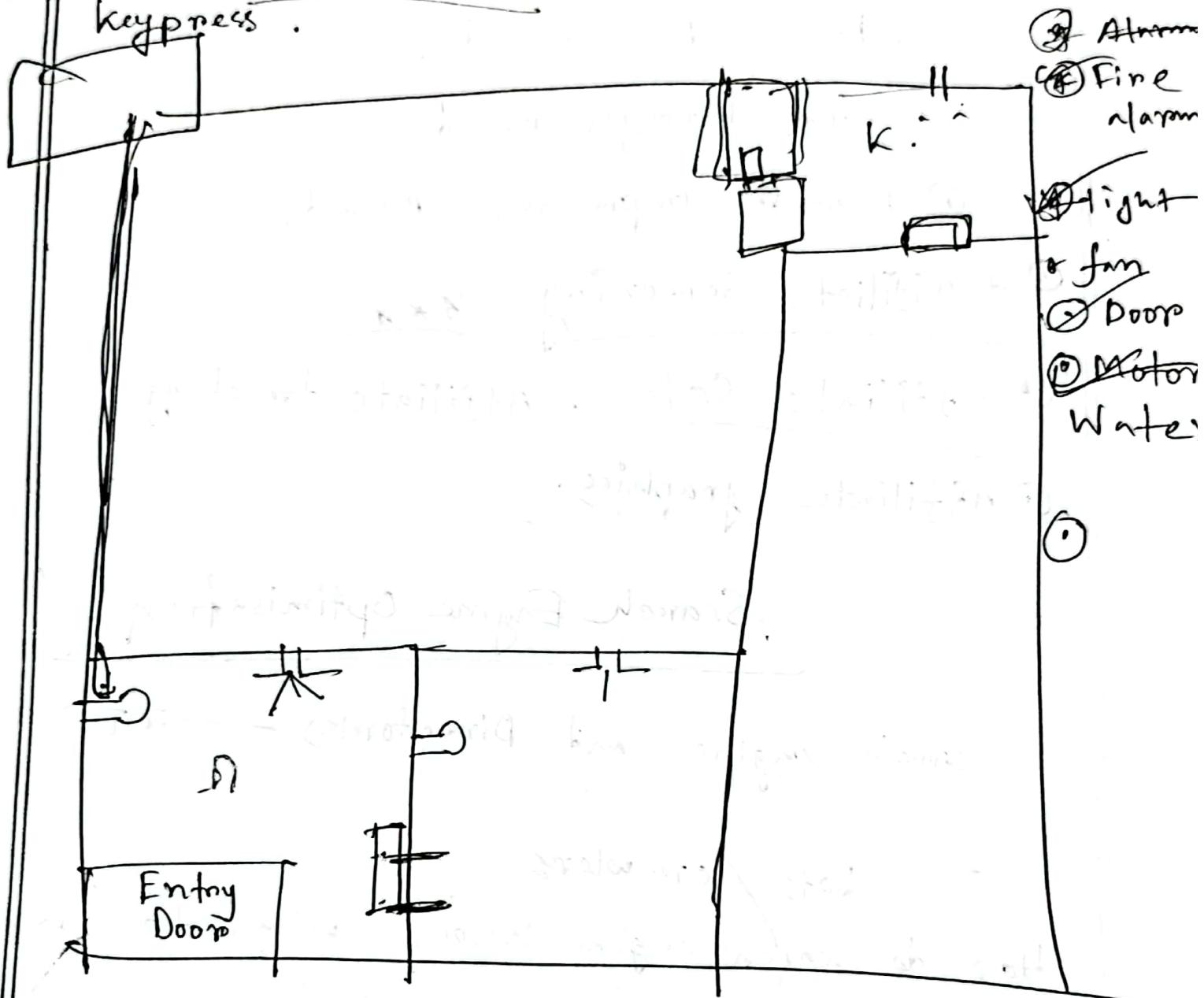
: 10.2
8255 Board examp — Master Port

Topic Name : _____

Fig : 10.3 : 8255 A-port

Fig: 10.19 : Detecting a matrix key board

~~keyness~~.



8255A Operational modes and Initialization Mode 0, Mode 1, Mode 2

MODE 0

without handshaking

- ① port A, B → initialized in mode 0.
- ② then C port

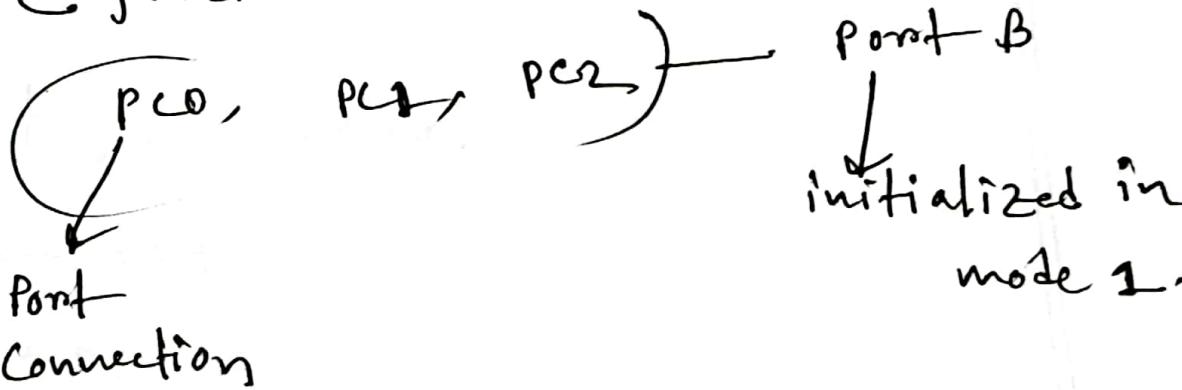
Port C lines → outputs.

two halves → independent

One is input Other output.

Mode 1 : handshaking → A, B

port C function → handshaking lines



If port A → input port

PC3, PC4, PC5

Port C pinning
PC4, PC5 → available for input / output

Mode 2 Only port A can be initialized in mode 2.

port C lower as input
port C Z output

key board interfacing

- ① Flow chart: PIC → ~~ACM~~ ~~and~~
↓ important
→ control word logic part;



drop down & go

224 224 224

key board interfacing - 224 224

Topic Name: MPU Lab and theory

Day:

Time:

Date: ⁹ / 01 / 2023

Next Sunday — Quiz QCTI

$a \oplus b$
if $a < b$
2's complement
otherwise 1's complement

not

0011
1100

8

Next Monday — MPU exam.

Next n → Economics → exam.

17 → ~~12~~ terrible exam: MPU

MCQ Lab

- ① Arithmetic operation
- ② Fundamental knowledge of 8086.
- ③ 8 bit report.

next report — 15 hours

MPU (edited)

Address pin \rightarrow

12 no. rom \rightarrow 4 pin $\rightarrow 2^4$

8 \rightarrow 3 pin $\rightarrow 2^3$

18 no \rightarrow 5 pin $\rightarrow 2^5$

fig: 7.9 : Parallel ROMs with decoders

MUL/9MULSF, ZF, AF, PF \rightarrow undefined.

CF/OF :

MUL : CF/OF = 0 if the upper half of the result is zero.
otherwise = 1.

: 0 , if the upper half of the result is the sign extension of the lower half
= 1 , otherwise .

~~F40~~
~~256~~ 16 1
 F4 C

$$1 \times 12 = 12$$

$$16 \times 4 = 64$$

$$256 \times 15 = 3840$$

$$\underline{3916}$$

- keep dividing by 16

use integers only

$$1453 \div 16 = 90.8$$

$$90 \div 16 = 5.6$$

$$5 \div 16 = 0.3$$

final : remo

(5AD)

~~051013~~
 A 1 1

$$\begin{array}{r} \text{FFFFH} \\ + 16^2 \times 15 + 1 \times 15 \\ \hline \text{BX} \quad \text{FFFFH} \end{array}$$

$$\begin{array}{r} 1111 \quad 1111 \\ 0000 \quad 0000 \\ + 1 \\ \hline 01 \end{array}$$

$$BX = -1$$

$$\begin{array}{c} -1 \\ \oplus \\ -1 \end{array} =$$

$$\begin{array}{r} 0001 \\ 1110 \\ + 1 \\ \hline 1111 \end{array}$$

$$\text{FFFF FFFF}$$

start → 15

$$CF = 1$$

$$AL \quad 80H \rightarrow$$

$$8 \times 16 = 128$$

$$BL \quad FFH -$$

$$290 + 15 = 255$$

$$\begin{array}{r} 26 \mid 383 \\ \hline \end{array}$$

$$\begin{array}{r} 1000 \quad 0000 \\ 1111 \quad 1111 \\ \hline \end{array}$$

$$\textcircled{1} \quad 0111 \quad 1111$$

$$OF =$$

FXXXH

$$\begin{array}{r} 383 \\ 368 \\ \hline 15 \end{array}$$

2

0 2

Topic Name : MPI lab

Day: _____

Time :

Date : 29/01/2023

starts:

mov ax, @data
mov ds, ax

mov dx, offset msg1

call puts

call gets

mov bl, al

add bl, 32d

ECAEG

30/01/2023