

INSTITUTE OF INFORMATION TECHNOLOGY JAHANGIRNAGAR UNIVERSITY

Number of Lab Report: 04

Name of Lab Report : Ring counter with D flipflop.

Course Tittle : Digital Logic Design Lab

Course Code : ICT – 2104

Submission Date : 18/02/2021

Submitted To

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Roll - 2023

2nd year 1st Semester

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County 4.

Experiment name: Ring Counter with D flip-flop.

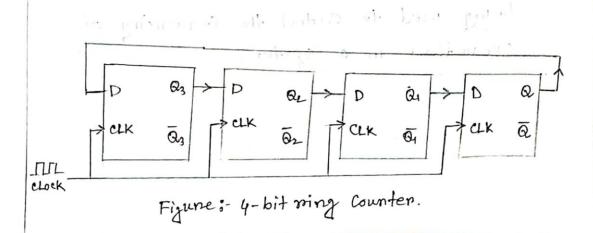
Objective:

Counter. Counter.

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2. To learn how to nun the output in cincular motion.

The simplest shift register counter is essentially a circulating shift register. Connected so that the last FF shifts its value into the first FF. This armangement is drawn in the figure. Using D Flip-flop.



The Flip-flop are connected so that information shifts from left to night and back arount from a to as.

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In most instances only a single 1 is in the register and it is made to circulate around the register are long as clock Pulses are applied. For this reason it is called a ring Counter.

Despite the fact that is is less efficient in the use of flip flop a ming counter is still use ful because no decoding gate is needed to decode this. This counter is especially better in application where the counter is being used to control the sequencing of openations in a system.

11) = 10 11) 12 11 12 11

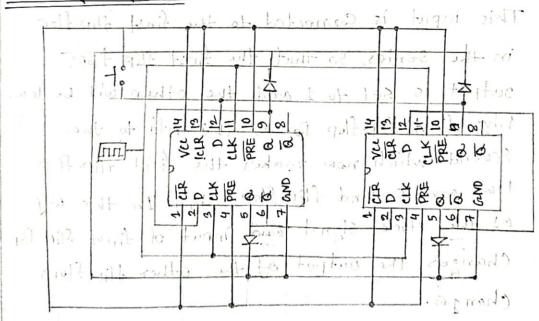
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Apparatus;

- i. Bread board resultante offe all example in
- 3. 7474 IC (4 Pes)
- 4. Capasiton (1 kF)
- 5. Resistons (1m, 100k) [3 2901-71]
 - 6. Connecting wines the an endlight wit
- 7. Power Source 21 of briggs of 172747 Working Diagnomes to trypic



Working Procedure: After Placing all the Components as drawn in the diagram to operate Properly a 11' data is Passed through one flip-flop. By inputing 11' data we will pass it throught the flip-flops. By Passing the neset signal initially the flip-flops are at RESET. State. When the PRESET is applied to the ring counter, the input of the circuit becomes. 1.

This input is connected to the first flip-flops in the Series, so that the first flip-flops output is set to 1 and the other will be low. When first flip-flop Passes the data to the Second which now makes the first flip-flop low and Second flip-flop high. In this way, as the clock signal and input of first flip-flop Changes the output of the other flip-flops change.

As the last output is connected to the first in the ring counter.

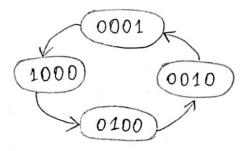
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Result:

Observed 4-bit ring Counter

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Q3	a_	04	2
1	0	0	0
0	1	0	0
0	0,	1	0
0	0	0	1

Sequence:



The ming Counter is Prepared and Observed

Reference: Illamin 21 happy had all A

- 1. Digital System Principles and Applications 12th edition by Ronald J. Tocci
- 2. WWW. auona. Com
- 3. WWW. Academia. Com

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