INSTITUTE OF INFORMATION TECHNOLOGY

JAHANGIRNAGAR UNIVERSITY

Number of Lab Report : 01

Name of Lab Report : D flip flop (7474) truth table visualization.

Course Tittle : Digital Logic Design Lab

Course Code : ICT – 2104

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Submitted To

Dr. Md. Sazzadur Rahman

Assistant Professor

IIT – JU

Submitted By

MD. Shakil Hossain

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2nd year 1st Semester

IIT – JU

Md. Shakil Hossain

Roll - 2023

Theory :- D flip-flop are used as a part of memory storage elements and data processors as well D flip-flop can be built using NAND gate or with NOR gate. Due to its versatifily they are availble as IC Packages. The major applications of D flip-flop are to introduce delay in liming circuit. as a buffer sampling data of specific intervals. D flip-flop is simpler in terms of wiring connection compared to JK flip-flop. Here we are using NAND gates for demonstrating the D flip-flop.

Whereever the clock signal is low the input is never going to affact the output state. The clock has to be high for the input to get active. Thus D flip-flop is a controlled Bi-Stable latch where the clock signal is the control signal.

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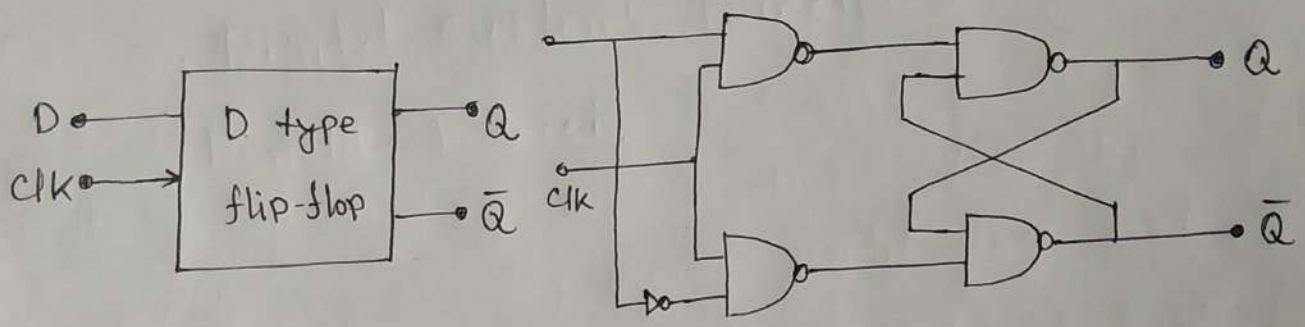
Again this gets divided into Positive edge triggred D flip-flop and negetive edge triggred D flip-flop. Thus the output has two stable based on the inputs which have been discussed below.



Symbol Circuit

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Truth table for the D type flip-flop :-

CLK	D	Q	$\bar{Q}$	Description
↓ >> 0	×	Q	$\bar{Q}$	Memory No change
↑ >> 1	0	0	1	Reset Q >> 0
↑ >> 1	1	1	0	Set Q >> 1

Note that: ↓ and ↑ indicates direction of clock Pulse as it is assumed D-type flip-flop are edge triggered.

Apparatus:-

1. IC SN 74LS 74AN
2. Power Source
3. LED
4. Breadboard
5. Connection wires

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Circuit diagram:—

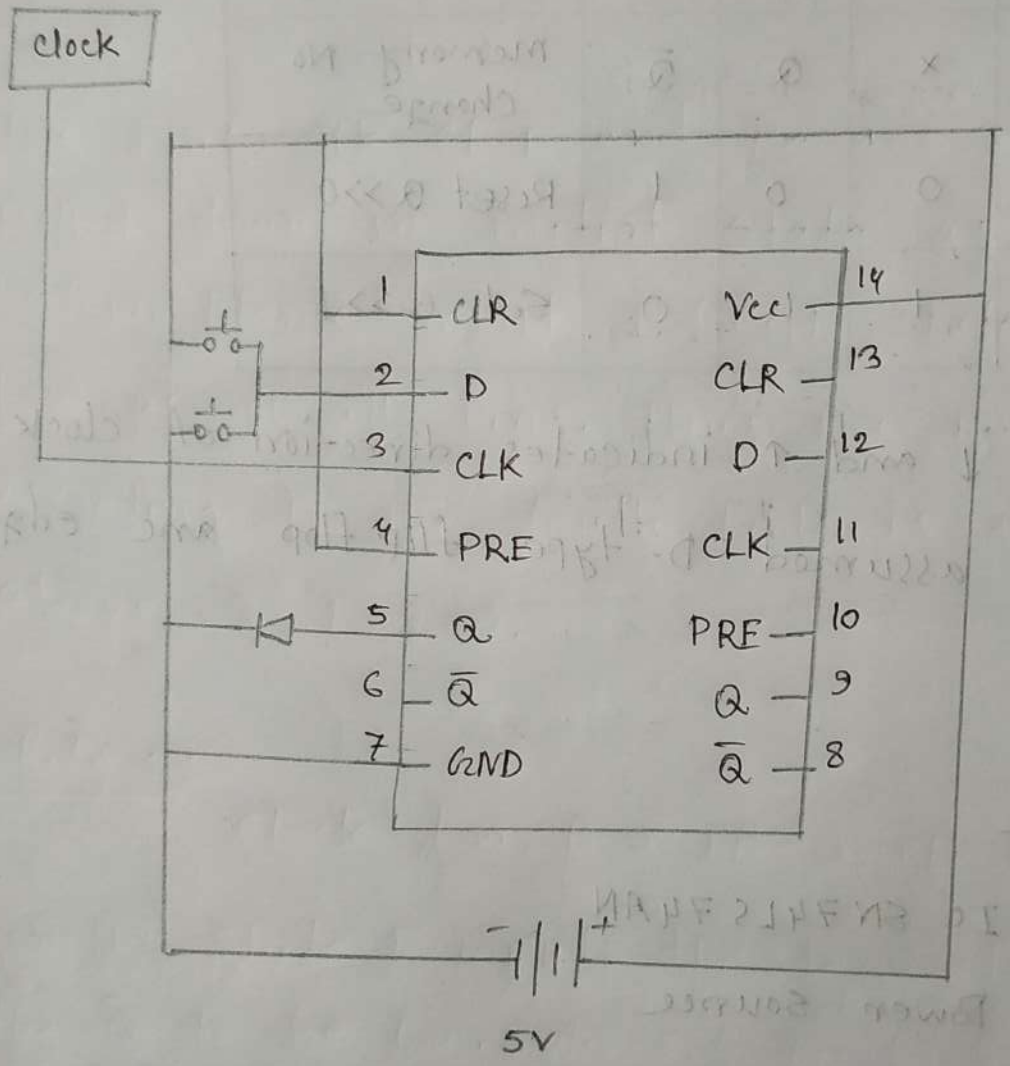

Figure:- 7474 circuit diagram.

Pin Diagram:-

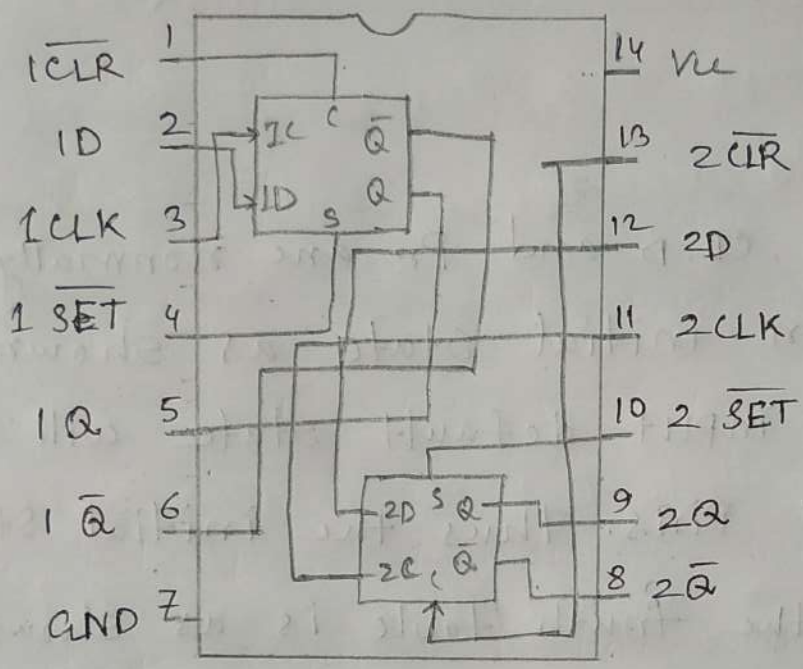

figure:- 7474 Pin diagram.

Working Procedure:

The buttons D, DR, CLK, CL are the inputs for the D flip-flop. The two led Q and $\bar{Q}$ represent the output states of the flip-flop. The Power Source acts as the input to the voltage. The Power Source output is used as the Vcc and Pin supply to the Ic.

Thus for different input at D the Corres-Ponding output can be seen through led Q and $\bar{Q}$.

The Pins clk, CL, D and Pr are normally Pulled down in initial state as shown below. Hence input default state will be Low across all Pins. Thus the initial state according to the truth table is as shown above. Q = 1, Q = 0.

State 1:

Clock - low, D-0, PR-0, CL-1, Q-0, $\bar{Q}$-1

For the state 1 inputs the led glows indicating the $\bar{Q}$ to be low. As set to high. Q is reset to 0 and can be seen above.

State 2: clock - low. D-0, PR-1 CL-1, Q-0, $\bar{Q}$-1

For the state 1 inputs the led glows indicating the $\bar{Q}$. The Red and green led glows indicating the Q and $\bar{Q}$ to be high initially. When the PR and CL are Pulled down or releasing the buttons the states goes to clear.

State 3:- Clock- low, D-0, PR-1, CL-0, Q-1, $\bar{Q}$-0.

For the state 3 inputs the green led glows indicating the Q to be high and red led to be low. As discussed above when Preset is set to high. Q is set to 1 and can be seen above.

State 4:- clock - High, D-0, PR-0, CL-0, Q-0, $\bar{Q}$-1

For the state 4 inputs the led of red be glows indicating the $\bar{Q}$ to be high and green led shows Q to be low.

This state is stable and stays there until the next clock and input. Since the clock is low to high edge triggered D input button should be Pressed befor. Pressing the clock button.

State 5:

Clock - High, D-1, PR-0, CL-0, Q-1, $\bar{Q}$ - 0.

For the state 5 inputs the green Led glows indicating the Q to be High and red Led to be low. This State is also stable and stay there until the next clock and input. Since the clock is low to High edge triggred D input button should be Pressed before Pressing the clock button.

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Discussion:- The D flip-flop tracks the input making transition with match those of the input D. The D stands for "data" this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. A D flip-flop can be made from a set/reset flip-flop by typing the set to the reset through an inverter. The result made by clocked.

Reference:-

1. Digital System Principles twelve edition Ronald J. Tocci.

2. www. Electrical-Tutorial. Com

3. www. Electrical-Lab-Tutorial. Com

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