



INSTITUTE OF INFORMATION TECHNOLOGY
JAHANGIRNAGAR UNIVERSITY

Number of Lab Report : 02

Name of Lab Report : JK flip flop(7473) truth table visualization.

Course Tittle : Digital Logic Design Lab

Course Code : ICT – 2104

Submission Date : 04/02/2021

Submitted To

Dr. Md. Sazzadur Rahman

Assistant Professor

IIT – JU

Submitted By

MD. Shakil Hossain

Roll – 2023

2nd year 1st Semester

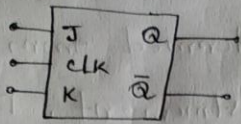
IIT – JU

Theory:

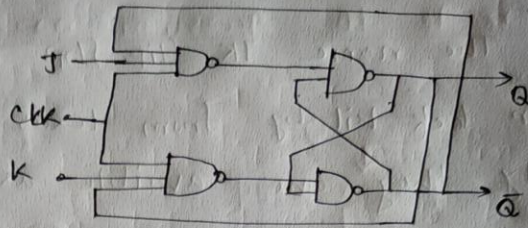
The name JK flip-flop is termed from the inventor Jack Kilby from Texas instrument. Due to Versatility they are available as IC Package. The major applications of JK flip-flop are Shift-register Storage registers, Counters and Control circuits. In spite of the simple wiring D type flip-flops JK flip-flops has a toggling nature. This has been an added advantage. Hence they are mostly used in counters PWM generation etc. Here we are using NAND gates for demonstrating the JK flip-flop.

Whenever the clock signal is low the input is never going to affect the output state. The clock has to be high for the inputs to get active.

Thus JK-flip-flop is a controlled Bi stable latch where the clock signal is the control signal. Thus the output has two stable states based on the inputs which has been discussed below.



Symbol JK flip-flop



Circuit

The Truth Table for JK flip-flop:

clock	Input		Output		Description
	J	K	Q	\bar{Q}	
X	0	0	1	0	memory no change
X	0	0	0	1	
\downarrow	0	1	1	0	Reset $Q \rightarrow 0$
X	0	1	0	1	Set $Q \rightarrow 1$
\downarrow	1	0	0	1	
X	1	0	1	0	Toggle
\downarrow	1	1	0	1	
X	1	1	1	0	

Apparatus :

1. IC MC74HC73A Dual (JK flip-flop)
2. Power Source
3. LED
4. Bread board
5. Connecting wires.

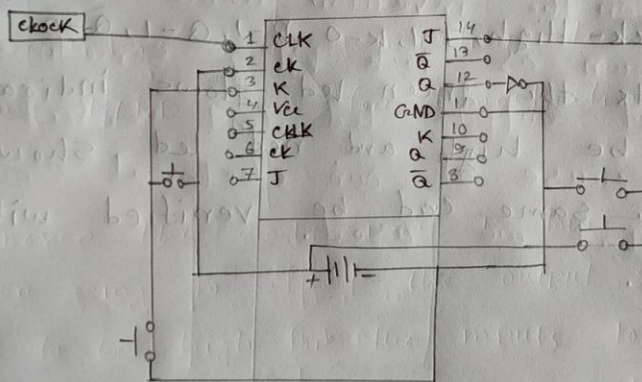
Circuit Diagram :

Fig. 7473 JK flip-flop circuit diagram

Working Procedure:

State 1:- Clock-High, $J=0$, $K=1$, $R=1$, $Q=0$, $\bar{Q}=1$. For the State inputs the Red led glows indicating the Q to be high and green led shows Q to be low the working can be verified with the truth table.

Note:- R is already pulled up so no need to Press the button to make it 1.

State 2:- Clock-High, $J=1$, $K=0$, $R=1$, $Q=1$, $\bar{Q}=0$. For the State 2 inputs the green led glows indicating the Q to be high and red led shows Q to be low The same can be verified with the truth table.

State 3:- Clock-High, $J=1$, $K=1$, $R=1$, Q/\bar{Q} -Toggle between two states. For the State 3 input red and green led glows alternatively for each clock pulse indicating the toggling action.

2021/2/4 11:49

The output toggle from the Previous state to another state and this process continues for each clock pulse.

State 4:

clock-low, $J=0$, $K=0$, $R=0$, $Q=0$, $\bar{Q}=1$.

The state 4 output shows that the input change does not affect under this state. The output red led glows indicating the Q to be high and green led shows Q to be low. This state is state and stay there until the next clock and input is applied with RESET as high pulse.

State 5:

The remaining state and No Change state during which the output will similar to previous output state the changes do not affect the output states you can verify with the truth table above.

Discussion: The JK flip-flop is the most widely used flip-flop. It is considered to be a universal flip-flop circuit. The sequential operation of the JK flip-flop is the same as for the RS flip-flop with the same SET and RESET input. The difference is that the JK flip-flop does not have the invalid input states of the RS latch. The JK flip-flop name has been kept on the inventor name of the circuit known as Jack Kilby. Sometimes our circuit output led to some imperfect results because of our electrical components problems that we used.

Reference:

1. www.Electrical-Tutorial.Com [Access date:- 03.02.2021]

2. www.Electrical-Lab-tutorial.com [Access date:- 03.02.2021]

3. Digital Systems Principles twelve edition
Ronald J. Tocci.

State 1: When the input is high, the output is high. When the input is low, the output is low. This state is stable and stays there until the next clock edge. When the input is high, the output is high. When the input is low, the output is low. This state is stable and stays there until the next clock edge.

State 2: When the input is high, the output is low. When the input is low, the output is high. This state is stable and stays there until the next clock edge. When the input is high, the output is low. When the input is low, the output is high. This state is stable and stays there until the next clock edge.

THE END