MOTOROLA

SN54/74LS181

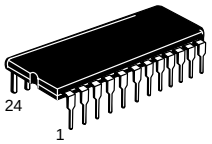
4-BIT ARITHMETIC LOGIC UNIT

The SN54/74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

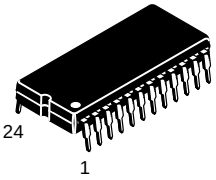
- Provides 16 Arithmetic Operations Add, Subtract, Compare, Double, Plus Twelve Other Arithmetic Operations
- Provides all 16 Logic Operations of Two Variables Exclusive — OR, Compare, AND, NAND, OR, NOR, Plus Ten other Logic Operations
- Full Lookahead for High Speed Arithmetic Operation on Long Words
- Input Clamp Diodes

4-BIT ARITHMETIC LOGIC UNIT

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 623-05

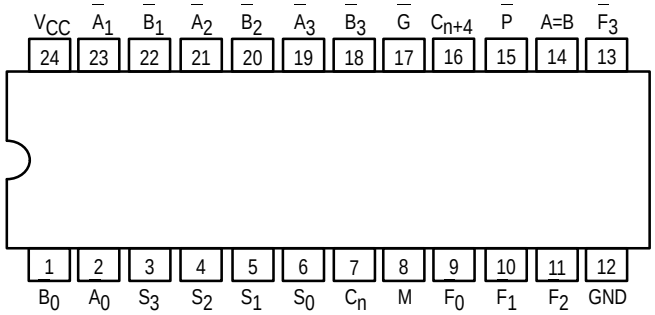


N SUFFIX
PLASTIC
CASE 649-03

ORDERING INFORMATION

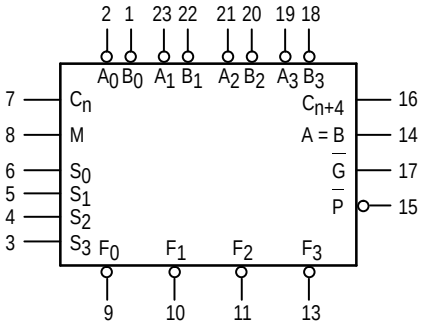
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC SYMBOL



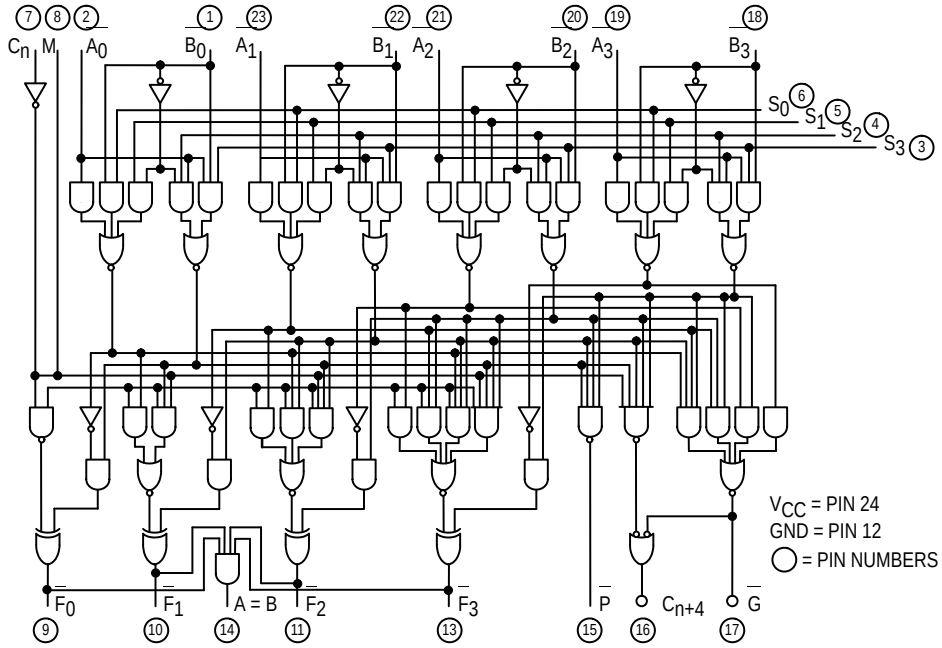
VCC = PIN 24
GND = PIN 12

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{A}_0-\overline{A}_3$, $\overline{B}_0-\overline{B}_3$	Operand (Active LOW) Inputs	1.5 U.L.	0.75 U.L.
S_0-S_3	Function — Select Inputs	2.0 U.L.	1.0 U.L.
M	Mode Control Input	0.5 U.L.	0.25 U.L.
$\underline{C}_n$	Carry Input	2.5 U.L.	1.25 U.L.
$\overline{F}_0-\overline{F}_3$	Function (Active LOW) Outputs	10 U.L.	5 (2.5) U.L.
$\underline{A}$ = B	Comparator Output	Open Collector	5 (2.5) U.L.
$\overline{G}$	Carry Generator (Active LOW) Output	10 U.L.	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output	10 U.L.	5 U.L.
C_{n+4}	Carry Output	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN54/74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals P (Carry Propagate) and G (Carry Generate), P and G are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of the four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the LS181 goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more then four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A>B and A<B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

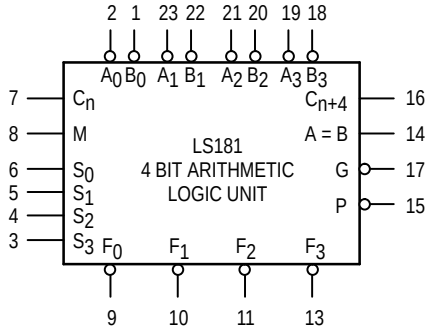
FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
				LOGIC	ARITHMETIC**	LOGIC	ARITHMETIC**
S_3	S_2	S_1	S_0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	A	A
L	L	L	H	$\overline{AB}$	AB minus 1	A + B	A + B
L	L	H	L	A + B	AB minus 1	$\overline{AB}$	A + B
L	L	H	H	Logical 1 minus 1		Logical 0 minus 1	
L	H	L	L	$\overline{A}$ + B	A plus (A + B)	$\overline{AB}$	A plus AB
L	H	L	H	B	AB plus (A + B)	B	(A + B) plus AB
L	H	H	L	$A \oplus \overline{B}$	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$\overline{A}$ + B	A + B	$\overline{AB}$	AB minus 1
H	L	L	L	AB	A plus (A + B)	$\overline{A + B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	AB plus (A + B)	B	(A + B) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logical 0 A plus A*		Logical 1 A plus A*	
H	H	L	H	AB	AB plus A	A + B	(A + B) plus A
H	H	H	L	AB	AB plus A	A + B	(A + B) Plus A
H	H	H	H	A	A	A	A minus 1

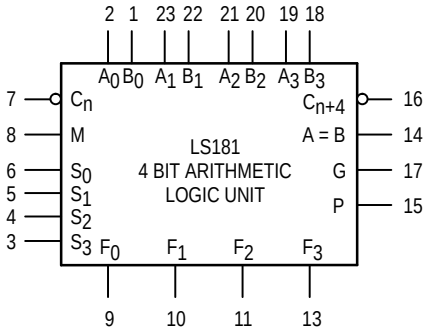
L = LOW Voltage Level
H = HIGH Voltage Level
*Each bit is shifted to the next more significant position
**Arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA
V_{OH}	Output Voltage — High (A = B only)	54, 74			5.5	V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage Except G and P	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
	Output $\overline{G}$	54, 74			0.7	V	I_{OL} = 16 mA	
	Output $\overline{P}$	54			0.6	V	I_{OL} = 8.0 mA	
		74			0.5			
I_{OH}	Output HIGH Current	54, 74			100	µA	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{IH}	Input HIGH Current Mode Input Any A or B Input Any S Input C_n Input				20 60 80 100	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Mode Input Any A or B Input Any S Input C_n Input				0.1 0.3 0.4 0.5	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Mode Input Any A or B Input Any S Input C_n Input				−0.4 −1.2 −1.6 −2.0	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 2)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current See Note 1A	54			32	mA	V_{CC} = MAX	
		74			34			
	See Note 1B	54			35			
		74			37			

Note 1.
With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

Note 2: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND, C_L = 15 pF)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})		18 13	27 20	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I and II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ Outputs)		17 13	26 20	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		19 15	29 23	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		21 21	32 32	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		20 20	30 30	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		20 22	30 33	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}_X$ or $\overline{B}_X$ Inputs to $\overline{F}_X$ Output)		21 13	32 20	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}_X$ or $\overline{B}_X$ Inputs to $\overline{F}_X$ Output)		21 21	32 32	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	(A_X or B_X Inputs to F_{XH} Outputs)			38 26	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	(A_X or B_X Inputs to F_{XH} Outputs)			38 38	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{F}$ Outputs)		22 26	33 38	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		25 25	38 38	ns	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		27 27	41 41	ns	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode)
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to A = B Output)		33 41	50 62	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V R_L = 2.0 kΩ (Diff Mode) See Fig. 5 and Table II

AC WAVEFORMS

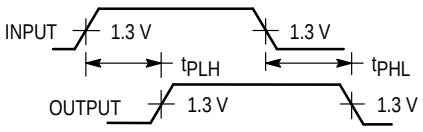


Figure 4

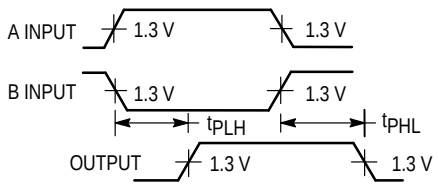


Figure 5

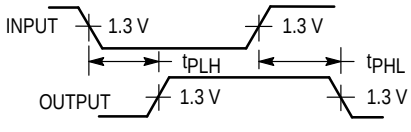


Figure 6

SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining A and B	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining A and B	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining A and B	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining A and B	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining A and B, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining A and B, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining B	Remaining A, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining B	Remaining A, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining B	Remaining A, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining B	Remaining A, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All A	All B	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining A	Remaining B, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining A	Remaining B, C_n	$\overline{F}_I$
t_{PLH} t_{PHL}	$\overline{A}_I$	None	$\overline{B}_I$	Remaining B, C_n	Remaining A	$\overline{F}_{I+1}$
t_{PLH} t_{PHL}	$\overline{B}_I$	$\overline{A}_I$	None	Remaining B, C_n	Remaining A	$\overline{F}_{I+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining A and B, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining A and B, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining A and B_I, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining A and B, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining A	Remaining B, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining A	Remaining B, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining A and B, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining A and B, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Function Inputs
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining A and B, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining A and B, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V