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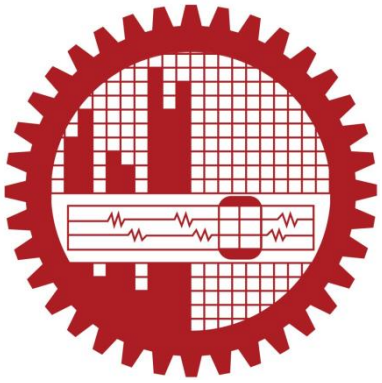

ASSIGNMENT

On *Modified Simple As Possible Computer* (MSAP-2015)

PHASE-I SUBMISSION

Course: **EEE 315**
Microprocessor and Interfacing

Submitted to:

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Section: A
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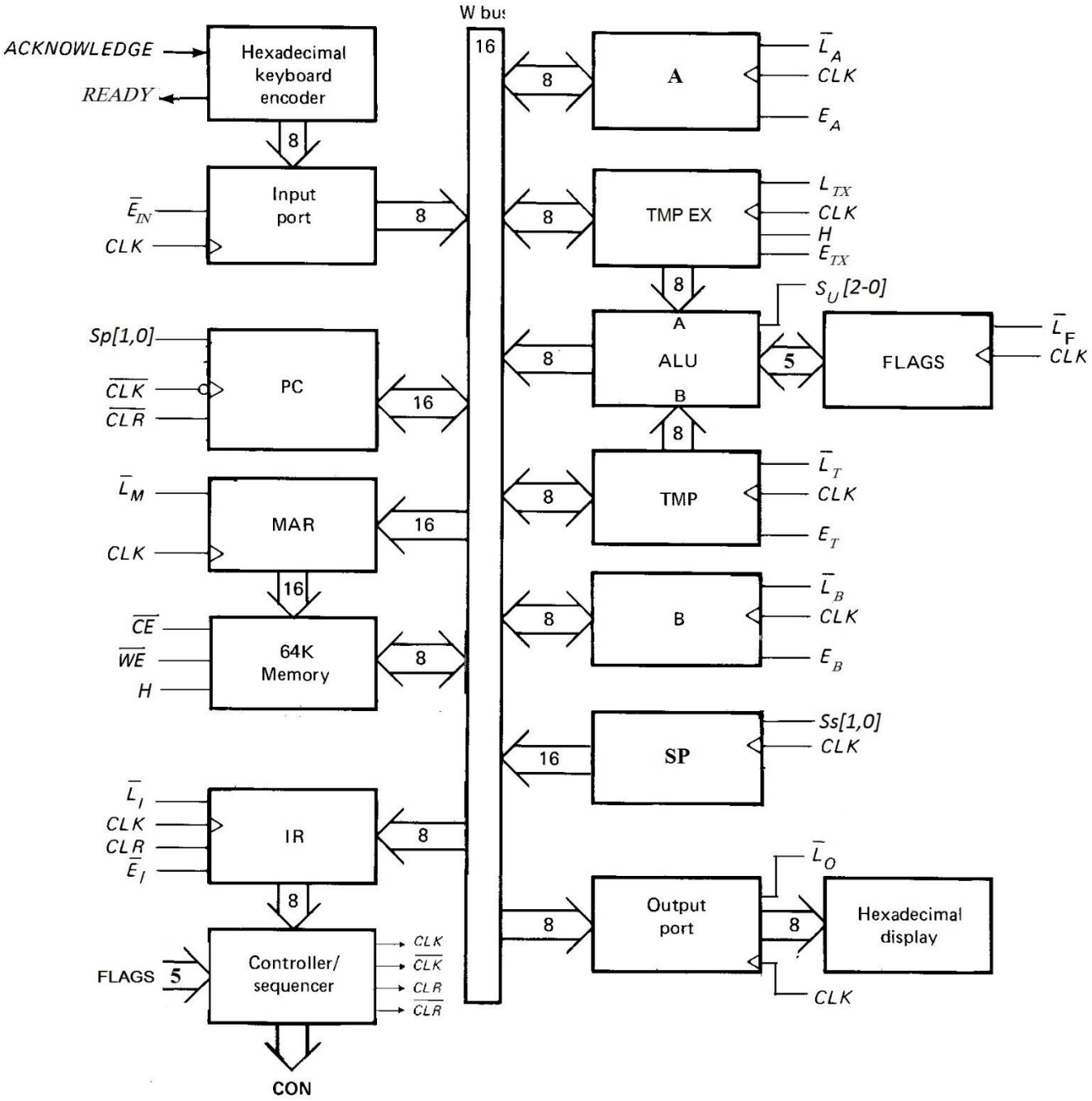
Block Diagram:



ALU Opcodes:

Opcode: S_U[2-0]	S_{U2} S_{U1} S_{U0}	Operation	Load Flags	$\bar{L}_F$
0	000	Z (High Impedance/Disabled)	No	1
1	001	$Logic: \bar{B}$	Yes	0
2	010	$Logic: A + B$	Yes	0
3	011	$Logic: AB$	Yes	0
4	100	$Logic: A \oplus B$	Yes	0
5	101	$Rotate\ Left\ with\ carry: B$	Yes	0
6	110	$Arithmatic: A + B$	Yes	0
7	111	$Arithmatic: A - B$	Yes	0

NB: The S_U signal determines whether the ALU is enabled and whether the Flags register loads.

Program Counter Select Pins:

Opcode: S_P[1-0]	S_{P1} S_{P0}	Operation
0	00	Disabled
1	01	Enabled
2	10	Count Up
3	11	Load

Stack Pointer Select Pins:

Opcode: S_S[1-0]	S_{S1} S_{S0}	Operation
0	00	Disabled
1	01	Enabled
2	10	Count Down [Moves Up]
3	11	Count Up [Moves Down]

Additional Control Signals:

H: Connect High Signal: Controls whether corresponding element (RAM/ TMP EX) is connected to the lower or upper 8-bit of W bus. H=0 and 1 connects the element to the lower and upper 8 bit respectively. Read and write is performed accordingly.

When H=1, TMP EX and TMP combine to connect as a 16 bit register with the W bus. Otherwise both TMP EX and TMP are connected to lower 8 bit of the W bus.

W: Wait Signal: Freezes the T state by stopping the ring and presettable counters and makes the CPU wait for input until Ready=1 at the positive edge of the clock. When W is turned off the Acknowledge signal is turned on at the next positive clock edge which is turned off when Ready=0.

H_{LT}: Halt: Halts processing by turning off the clock. *Not part of the control word.*

N_{OP}: No Operation: marks the end of the variable machine cycle. *Part of the control word.*

Microprogramming:

Fetch Cycle:

T State	Active Signals	Microinstruction $[S_S S_P \quad L_I L_M \overline{WE}\ \overline{CE} \quad \bar{L}_A E_A \bar{L}_B E_B \quad \bar{L}_O E_{IN} \bar{L}_T E_T \quad HSu \quad N_{OP} W L_{TX} E_{TX}]$
T_1	$Sp = 1, \bar{L}_M$	1BAA00
T_2	$\overline{CE}, L_I, Sp = 2$	26AA00

Execution Cycle:

Op Code	Instruction	T State	Active Signals	Microinstruction $[S_S S_P \quad L_I L_M \overline{WE}\ \overline{CE} \quad \bar{L}_A E_A \bar{L}_B E_B \quad \bar{L}_O E_{IN} \bar{L}_T E_T \quad HSu \quad N_{OP} W L_{TX} E_{TX}]$
00	**JZ**	CONDITION: ZF=0		
		T_3	N_{OP}	0FAA08
		CONDITION: ZF=1		
		T_3	$Sp = 1, \bar{L}_M$	1BAA00
		T_4	$\overline{CE}, \bar{L}_T, Sp = 2$	2EA800
		T_5	$Sp = 1, \bar{L}_M$	1BAA00
		T_6	$H, \overline{CE}, E_T, Sp = 3$	3EAB80
		T_7	N_{OP}	0FAA08
01	**NOT B**	T_4	$E_B, \bar{L}_T$	0FB800
		T_5	$S_U = 1, \bar{L}_B$	0F8A10
		T_6	N_{OP}	0FAA08`
02	**Call** [Address]	T_3	$Sp = 1, \bar{L}_M$	1BAA00
		T_4	$\overline{CE}, \bar{L}_T, Sp = 2$	2EA800
		T_5	$Sp = 1, \bar{L}_M$	1BAA00
		T_6	$\overline{CE}, L_{TX}, Sp = 2, Ss = 2$	AEAA02
		T_7	$Ss = 1, \bar{L}_M$	4BAA00
		T_8	$H, \overline{CE}, \overline{WE}, Sp = 1, Ss = 2$	9CAA80
		T_9	$Ss = 1, \bar{L}_M$	4BAA00

		T_{10}	$\overline{CE}, \overline{WE}, Sp = 1$	1CAA00
		T_{11}	$H, E_{TX}, E_{T,}\ Sp = 3$	3FAB81
		T_{12}	N_{OP}	0FAA08
03	**RET**	T_3	$Ss = 1, \bar{L}_M$	4BAA00
		T_4	$\overline{CE}, \bar{L}_T, Ss = 3$	CEA800
		T_5	$Ss = 1, \bar{L}_M$	4BAA00
		T_6	$H, \overline{CE}, E_T, Sp = 3, Ss = 3$	FEAB80
		T_7	N_{OP}	0FAA08
04	**MOV** B, byte	T_3	$Sp = 1, \bar{L}_M$	1BAA00
		T_4	$\overline{CE}, \bar{L}_B, Sp = 2$	2E8A00
		T_5	N_{OP}	0FAA08
05	**HLT**	T_3	H_{LT}	-
06	**MOV** A, [address]	T_3	$Sp = 1, \bar{L}_M$	1BAA00
		T_4	$\overline{CE}, \bar{L}_T, Sp = 2$	2EA800
		T_5	$Sp = 1, \bar{L}_M$	1BAA00
		T_6	$H, \overline{CE}, E_{T,} \bar{L}_M, Sp = 2$	2AAB80
		T_7	$\overline{CE}, \bar{L}_A$	0E2A00
		T_8	N_{OP}	0FAA08
07	**PUSH** A	T_3	$Ss = 2$	8FAA00
		T_4	$Ss = 1, \bar{L}_M$	4BAA00
		T_5	$\overline{CE}, \overline{WE}, E_A$	0CEA00
		T_6	N_{OP}	0FAA08
08	**OUT** A	T_3	$\bar{L_O}, E_A$	0FE200
		T_4	N_{OP}	0FAA08

09	TEST **A, [Address]**	T_3	$\boldsymbol{Sp = 1, \bar{L}_M}$	1BAA00
		T_4	$\overline{CE}, \bar{L}_T, Sp = 2$	2EA800
		T_5	$Sp = 1, \bar{L}_M$	1BAA00
		T_6	$H, \overline{CE}, E_T, \bar{L}_M, Sp = 2$	2AAB80
		T_7	$\overline{CE}, \bar{L}_T$	0EA800
		T_8	E_A, L_{TX}	0FEA02
		T_9	$Su = 3$	0FAA30
		T_{10}	N_{OP}	0FAA08
0A	**IN** B	T_3	W	0FAA04
		T_4	$E_{IN}, \bar{L}_B$	0F8E00
		T_5	N_{OP}	0FAA08
0B	**POP** [address]	T_3	$Ss = 1, \bar{L}_M$	4BAA00
		T_4	$\overline{CE}, L_{TX}, Ss = 3$	CEAA02
		T_5	$Sp = 1, \bar{L}_M$	1BAA00
		T_6	$\overline{CE}, \bar{L}_T, Sp = 2$	2EA800
		T_7	$Sp = 1, \bar{L}_M$	1BAA00
		T_8	$H, \overline{CE}, E_T, \bar{L}_M, Sp = 2$	2AAB80
		T_9	$\overline{CE}, \overline{WE}, E_{TX}$	0CAA01
		T_{10}	N_{OP}	0FAA08
0C	**SUB** A, B	T_3	E_A, L_{TX}	0FEA02
		T_4	$E_B, \bar{L}_T$	0FB800
		T_5	$S_U = 7, \bar{L}_A$	0F2A70
		T_6	N_{OP}	0FAA08
0D	**XCHG** [address], B	T_3	$Sp = 1, \bar{L}_M$	1BAA00
		T_4	$\overline{CE}, \bar{L}_T, Sp = 2$	2EA800

		T_5	$Sp = 1, \bar{L}_M$	1BAA00
		T_6	$H, \overline{CE}, E_{T,} \bar{L}_M, Sp = 2$	2AAB80
		T_7	$\overline{CE}, \bar{L}_T$	0EA800
		T_8	$\overline{CE}, \overline{WE}, E_B$	0CBA00
		T_9	$E_T, \bar{L}_B$	0F8B00
		T_{10}	N_{OP}	0FAA08
0E	**RCL** A	T_3	$E_A, \bar{L}_T$	0FE800
		T_4	$Su = 5, \bar{L}_A$	0F2A50
		T_5	N_{OP}	0FAA08
0F	**XOR** [address], B	T_3	$Sp = 1, \bar{L}_M$	1BAA00
		T_4	$\overline{CE}, \bar{L}_T, Sp = 2$	2EA800
		T_5	$Sp = 1, \bar{L}_M$	1BAA00
		T_6	$H, \overline{CE}, E_{T,} \bar{L}_M, Sp = 2$	2AAB80
		T_7	$H, \overline{CE}, L_{TX}, E_B, \bar{L}_T$	0EB882
		T_8	$S_U = 4, \overline{CE}, \overline{WE}$	0CAA40
		T_9	N_{OP}	0FAA08