

October 1988 Revised April 2000

DM74LS181 4-Bit Arithmetic Logic Unit

General Description

The DM74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

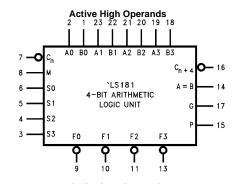
Features

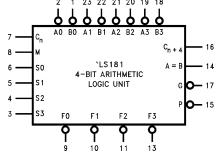
- Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations
- Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations
- Full lookahead for high speed arithmetic operation on long words

Ordering Code:

Order Number	Package Number	Package Description
DM74LS181N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide

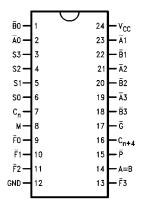
Logic Symbols





V_{CC} = Pin 24 GND = Pin 12

Connection Diagram



Pin Descriptions

Pin Names	Description
A0-A3	Operand Inputs (Active LOW)
B0-B3	Operand Inputs (Active LOW)
S0-S3	Function Select Inputs
M	Mode Control Input
C _n	Carry Input
F0-F3	Function Outputs (Active LOW)
A = B	Comparator Output
G	Carry Generate Output (Active LOW)
P	Carry Propagate Output (Active LOW)
C _{n+4}	Carry Output

Functional Description

The DM74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals P (Carry Propagate) and G (Carry Generate). In the ADD mode, \overline{P} indicates that \overline{F} is 15 or more, while $\overline{\underline{G}}$ indicates that \overline{F} is 16 or more. In the SUBTRACT mode, \overline{P} indicates that \overline{F} is zero or less, while \overline{G} indicates that \overline{F} is less than zero. \overline{P} and \overline{G} are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (Cn+4) signal to the Carry input (Cn) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four

DM74LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four \overline{F} outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

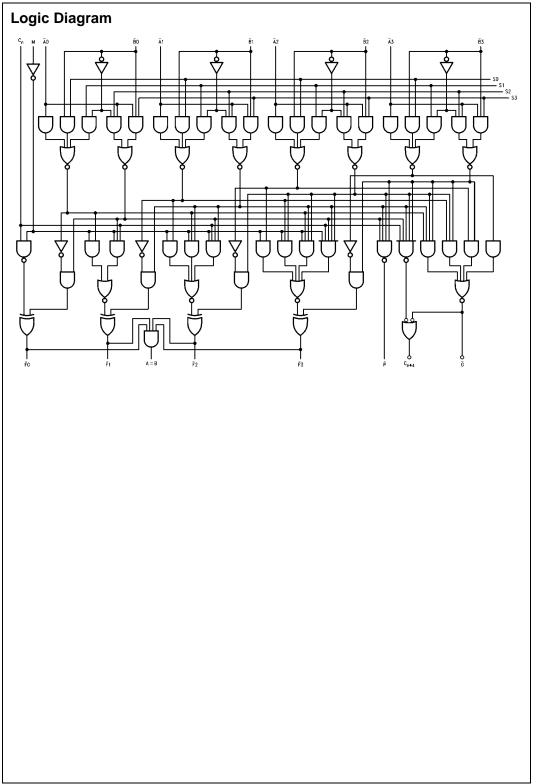
The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

Mode Select				Acti	Active LOW Operands		ve HIGH Operands
	Inputs				& F _n Outputs		& F _n Outputs
				Logic	Arithmetic (Note 2)	Logic	Arithmetic (Note 2)
S3	S2	S1	S0	(M = H)	(M = L) ($C_n = L$)	(M = H)	$(\mathbf{M}=\mathbf{L})\;(\mathbf{C_n}=\mathbf{H})$
L	L	L	L	Ā	A minus 1	Ā	A
L	L	L	Н	AB	AB minus 1	$\overline{A} + \overline{B}$	A + B
L	L	Н	L	$\overline{A} + \overline{B}$	AB minus 1	ĀВ	$A + \overline{B}$
L	L	Н	Н	Logic 1	minus 1	Logic 0	minus 1
L	Н	L	L	$\overline{A} + \overline{B}$	A plus $(A + \overline{B})$	AB	A plus AB
L	Н	L	Н	В	AB plus $(A + \overline{B})$	B	$(A + B)$ plus $A\overline{B}$
L	Н	Н	L	$\overline{A} \oplus \overline{B}$	A minus B minus 1	A B	A minus B minus 1
L	Н	Н	Н	$A + \overline{B}$	$A + \overline{B}$	AB	AB minus 1
Н	L	L	L	Ā B	A plus (A + B)	$\overline{A} + B$	A plus AB
Н	L	L	Н	$A \oplus B$	A plus B	$\overline{A} \oplus \overline{B}$	A plus B
Н	L	Н	L	В	$A\overline{B}$ plus $(A + B)$	B	$(A + \overline{B})$ plus AB
Н	L	Н	Н	A + B	A + B	AB	AB minus 1
Н	Н	L	L	Logic 0	A plus A (Note 1)	Logic 1	A plus A (Note 1)
Н	Н	L	Н	$A\overline{B}$	AB plus A	$A + \overline{B}$	(A + B) plus A
Н	Н	Н	L	AB	AB minus A	A + B	$(A + \overline{B})$ plus A
Н	Н	Н	Н	Α	Α	Α	A minus 1

Note 1: Each bit is shifted to the next most significant position.

Note 2: Arithmetic operations expressed in 2s complement notation.



Absolute Maximum Ratings(Note 3)

Supply Voltage 7V Input Voltage 7V Operating Free Air Temperature Range $0^{\circ}\text{C to } +70^{\circ}\text{C}$ Storage Temperature Range $-65^{\circ}\text{C to } +150^{\circ}\text{C}$

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
Гон	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level	$V_{CC} = Min, I_{OH} = Max,$		2.7			V
	Output Voltage	V _{IL} = Max		2.1			V
V _{OL}	LOW Level	$V_{CC} = Min, I_{OL} = Max,$			0.35	0.5	
	Output Voltage	$V_{IH} = Min$			0.55	0.5	V
		$I_{OL} = 4 \text{ mA}, V_{CC} = Min$			0.25	0.4	
I _I	Input Current @ Max	$V_{CC} = Max, V_I = 7V$	M input			0.1	
	Input Voltage		\overline{A}_n , \overline{B}_n			0.3	mA
			S _n			0.4	111/4
			C _n			0.5	
I _{IH}	HIGH Level	$V_{CC} = Max, V_I = 2.7V$	M input			20	
	Input Current		$\overline{A}_n,\overline{B}_n$			60	μА
			S _n			80	μΛ
			C _n			100	
I _{IL}	LOW Level	$V_{CC} = Max, V_I = 0.4V$	M input			-0.4	
	Input Current		\overline{A}_n , \overline{B}_n			-1.2	mA
			S _n			-1.6	III/A
			C _n			-2.0	
Ios	Short Circuit	V _{CC} = Max		-20		-100	mA
	Output Current	(Note 5)		-20		.00	111/4
I _{CC}	Supply Current	$V_{CC} = Max, \overline{B}_n, C_n = GND$				37	mA
		S_n , M , $\overline{A}_n = 4.5V$				31	IIIA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = 5V, T_A = 25^{\circ}C$

Symbol	Parameter	Conditions	C _L =	C _L = 15 pF	
Symbol	Parameter	Conditions	Min	Max	Units
t _{PLH}	Propagation Delay	M = GND		27	ns
t _{PHL}	C _n to C _{n+4}			20	ris
t _{PLH}	Propagation Delay	M = GND		26	no
t _{PHL}	C _n to F			20	ns
t _{PLH}	Propagation Delay	$M, S_1, S_2 = GND;$		29	
t _{PHL}	A or B to G (Sum)	S_1 , $S_3 = 4.5V$		23	ns
t _{PLH}	Propagation Delay	$M, S_0, S_3 = GND;$		32	
t _{PHL}	A or B to G (Diff)	S_1 , $S_2 = 4.5V$		26	ns
t _{PLH}	Propagation Delay	$M, S_1, S_2 = GND;$		30	
t _{PHL}	A or B to P (Sum)	$S_0, S_3 = 4.5V$		30	ns
t _{PLH}	Propagation Delay	$M, S_0, S_3 = GND;$		30	
t _{PHL}	A or B to P (Diff)	S_1 , $S_2 = 4.5V$		33	ns
t _{PLH}	Propagation Delay	$M, S_1, S_2 = GND;$		32	ns
t _{PHL}	\overline{A}_i or \overline{B}_i to \overline{F}_i (Sum)	S_0 , $S_3 = 4.5V$		25	115
t _{PLH}	Propagation Delay	$M, S_0, S_3 = GND;$		32	ns
t _{PHL}	\overline{A}_i or \overline{B}_i to \overline{F}_i (Diff)	S_1 , $S_2 = 4.5V$		33	115
t _{PLH}	Propagation Delay	M = 4.5V		33	
t _{PHL}	A or B to F (Logic)			29	ns
t _{PLH}	Propagation Delay	$M, S_1, S_2 = GND;$		38	ns
t _{PHL}	\overline{A} or \overline{B} to C_{n+4} (Sum)	S_0 , $S_3 = 4.5V$		38	115
t _{PLH}	Propagation Delay	$M, S_0, S_3 = GND;$		41	ns
t _{PHL}	\overline{A} or \overline{B} to C_{n+4} (Diff)	S_1 , $S_2 = 4.5V$		41	115
t _{PLH}	Propagation Delay	$M, S_0, S_3 = GND;$		50	no
t _{PHL}	\overline{A} or \overline{B} to $A = B$	S_1 , $S_2 = 4.5V$;		62	ns
		$R_L = 2 \text{ k}\Omega \text{ to } 5.0 \text{V}$			

Sum Mode Test Table 1 Function Inputs

S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Input Under	Other Input Same Bit		Other Da	Output Under	
	Test	Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	Test
PLH PHL	\overline{A}_{i}	B _i	None	Remaining Ā and B	C _n	F _i
PLH	B _i	Ā _i	None	Remaining A and B	C _n	F _i
PLH PHL	Ā	B	None	None	Remaining A and B, C _n	P
t _{PLH}	В	Ā	None	None	Remaining A and B, C _n	P
t _{PLH}	Ā	None	В	Remaining B	Remaining \overline{A} , C_n	G
PLH PHL	В	None	Ā	Remaining B	Remaining \overline{A} , C_n	G
PLH PHL	Ā	None	В	Remaining B	Remaining \overline{A} , C_n	C _{n+4}
^t PLH ^t PHL	В	None	Ā	Remaining B	Remaining \overline{A} , C_n	C _{n+4}
t _{PLH} t _{PHL}	C _n	None	None	All Ā	All B	Any F or C _{n+4}

Diff Mode Test Table 2 Function Inputs S1 = S2 = 4.5V, S0 = S3 = M = 0V Other Input Other Data Inputs Output Symbol Under Same Bit Under Test Apply Apply Apply Apply Test 4.5V GND 4.5V Ā None Remaining Remaining Fi $\mathsf{t}_{\mathsf{PLH}}$ Ā B, C_n t_{PHL} В t_{PLH} Ā None Remaining Remaining Ā B, C_n t_{PHL} Ā None None Remaining t_{PLH} \overline{A} and \overline{B} , C_n t_{PHL} t_{PLH} В A None None Remaining t_{PHL} \overline{A} and \overline{B} , C_n t_{PLH} A None None Remaining \overline{A} and \overline{B} , C_n t_{PHL} В t_{PLH} None None Remaining $\overline{\overline{A}}$ and $\overline{\overline{B}},$ C_n t_{PHL} A None Remaining Remaining $\mathsf{A}=\mathsf{B}$ t_{PLH} Ā B, C_n t_{PHL} В Remaining t_{PLH} None Remaining $\mathsf{A}=\mathsf{B}$ A B, C_n t_{PHL} A В None None Remaining C_{n+4} t_{PLH} $\overline{\overline{A}}$ and $\overline{\overline{B}}$, C_n t_{PHL} t_{PLH} В None None Remaining C_{n+4} $\overline{\overline{A}}$ and $\overline{\overline{B}},$ C_n t_{PHL}

Logic Mode Test Table 3 Function Inputs

 C_n

None

S1 = S2 = M = 4.5V, S0 = S3 = 0V

 t_{PLH}

 $\mathsf{t}_{\mathsf{PHL}}$

Symbol	Input Under		Input e Bit	Other D	Pata Inputs	Output Under
	Test	Apply	Apply	Apply	Apply	Test
		4.5V	GND	4.5V	GND	
t _{PLH} t _{PHL}	Ā	B	None	None	Remaining A and B, C _n	Any F
t _{PLH}	B	Ā	None	None	Remaining A and B, C _n	Any F

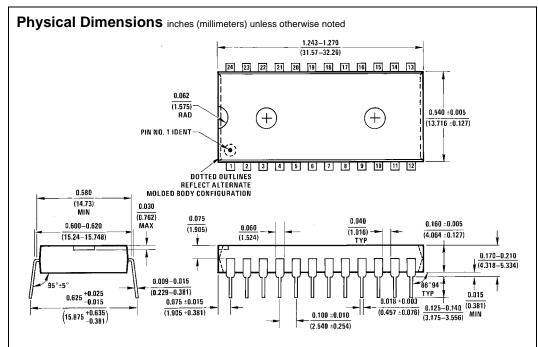
None

All

A and B

None

C_{n+4}



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide Package Number N24A

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