OBJECTIVE:

The objective of this project is to simulate ASK (amplitude shift keying) and PSK (phase shift keying) modulated signal generation and detection.

INTRODUCTION:

ASK: It is a modulation process in which the binary ones and zeros of the digital intelligence signal are represented by a high and low amplitude carrier.

PSK: It is a modulation process in which the transition of binary ones and zeros of the digital intelligence signal are represented by a phase difference of a carrier.

ASK signals can be demodulated by either a synchronous or asynchronous detector but PSK can only be demodulated synchronously.

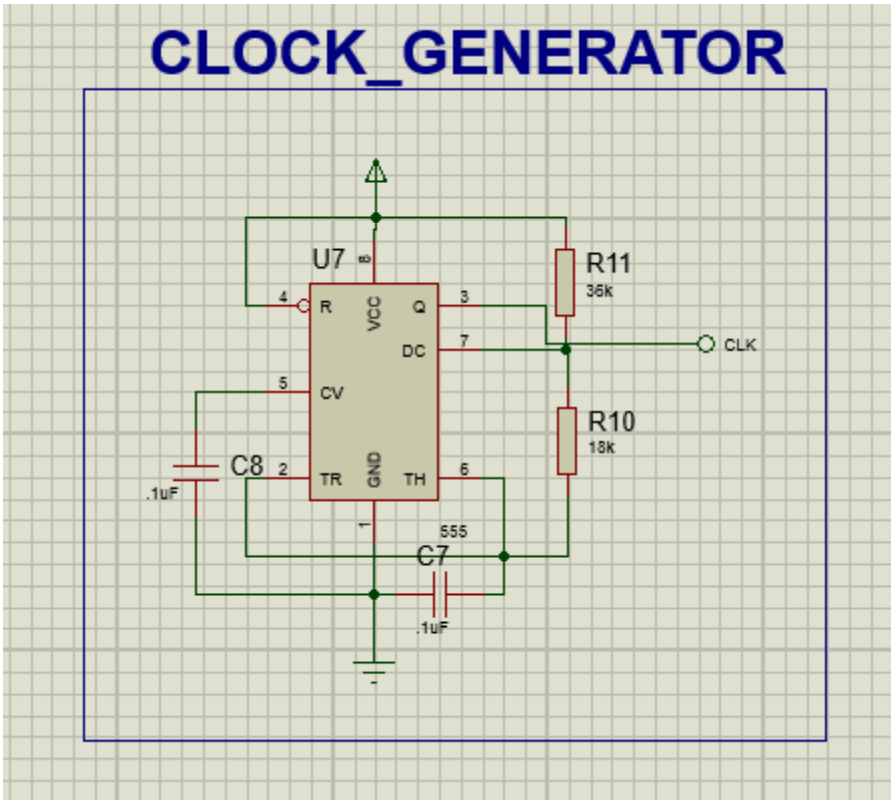
BASIC PRINCIPLES:

In this simulation project we generated a digital intelligent signal using logic circuitry and then modulated the signal with a higher frequency carrier using a balanced modulator. An offset voltage was added to the digital signal before modulation which determines whether the modulated signal should be ASK/PSK.
We designed two demodulators i.e. an envelope detector and a product detectors for demodulation of the signal. ASK signal can be demodulated by either the product/envelope detector but PSK signal can only be demodulated using the envelope detector.
Lastly a voltage comparator is used to recover the original logic level from the demodulated signal.

We used a clock frequency of 200 Hz and carrier frequency of 10 kHz.

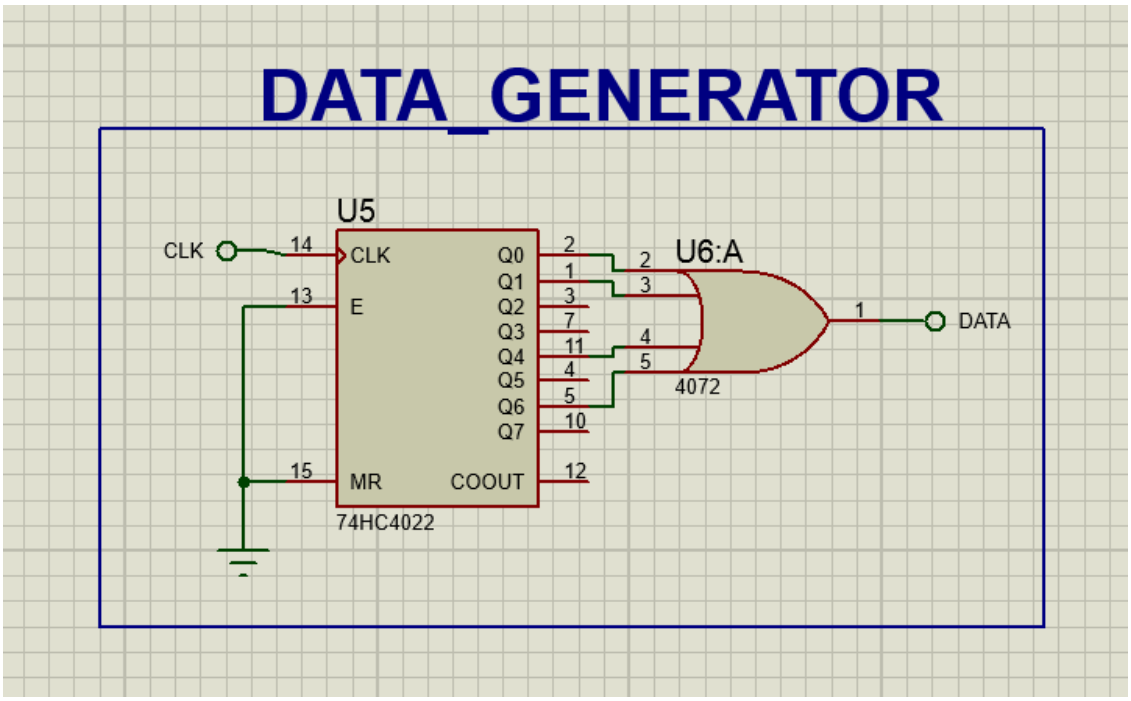
DESCRIPTION AND FUNCTION OF THE COMPONENTS USED IN THE SIMULATION:

1. **CLOCK GENERATOR:**



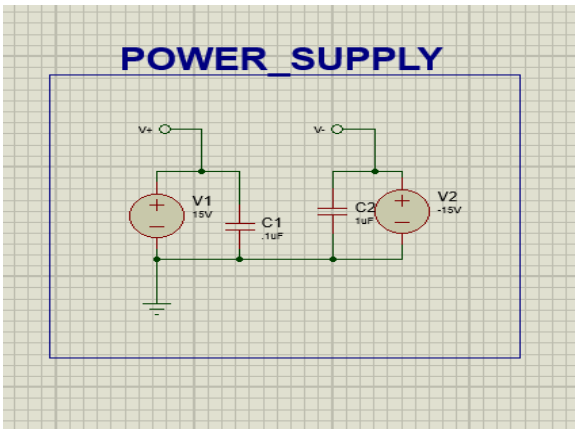
The clock generator is used to produce the clock signal which drives the data generator. It is a 555 timer/oscillator that generates the clock signal. Clock frequency = 200 kHz.

2. DATA GENERATOR:



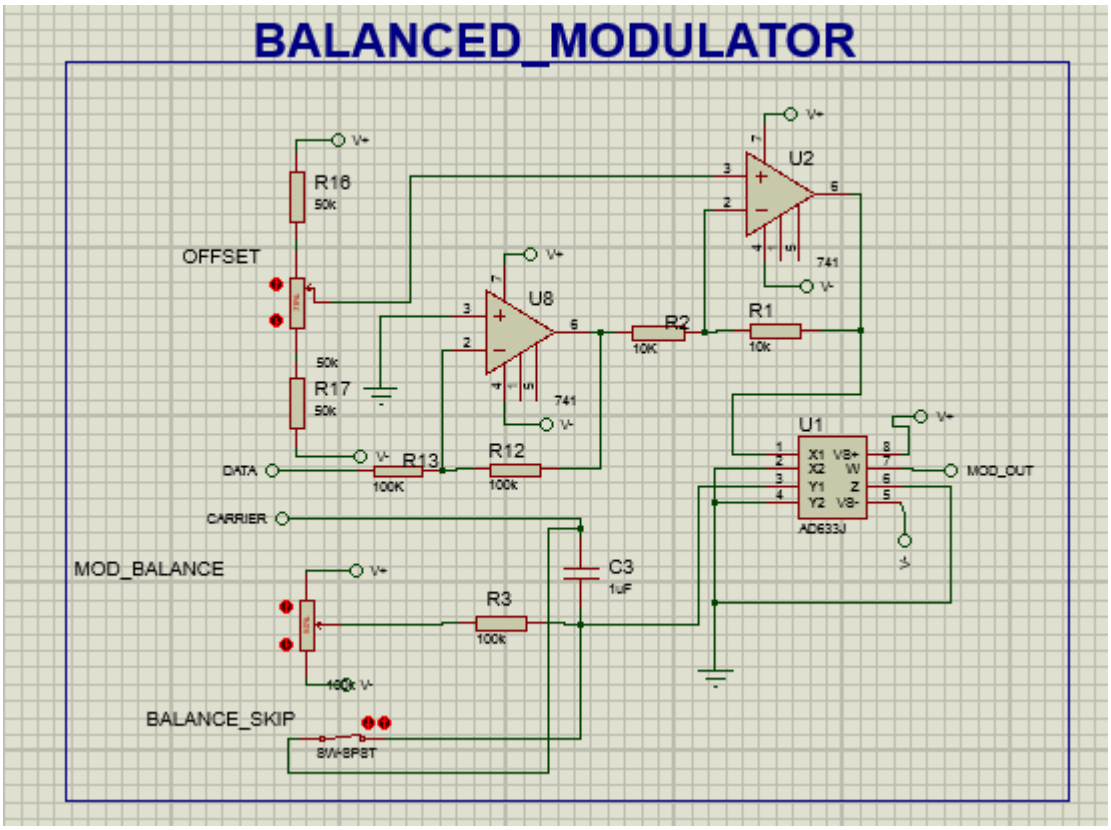
IC 74HC4022 is used as data generator. It is a 4 stage divide by 8 johnson counter. It is a shift register fed back on its self. The data pattern contained within the shift register will recirculate as long as clock pulses are applied. This component produces the digital intelligence signal that is to be modulated. The bit pattern is 11001010… which is repeated indefinitely.

3. POWER SUPPLY:



This block produces +15V and -15V dc supply that are used for dc biasing of operational amplifiers.

4. BALANCED MODULATOR:

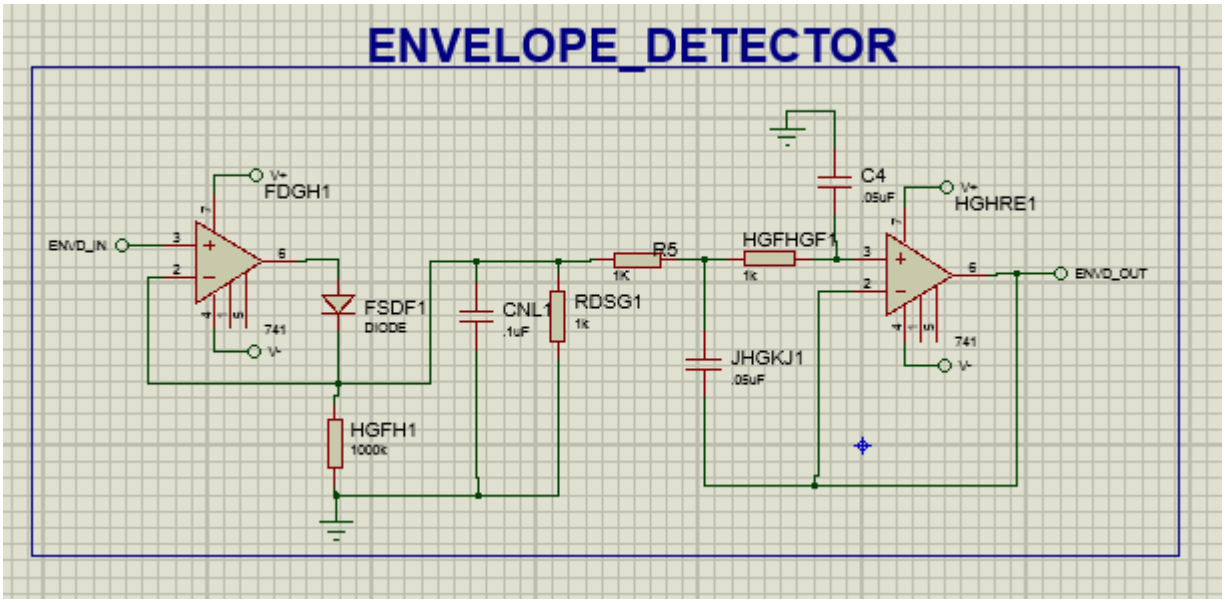


This block performs the operation of modulation. Both ASK and PSK modulated signals can be generated from this block through changing the offset. The offset is adjusted by a potentiometer. For ASK the offset is adjusted to add a dc voltage to the digital signal so that a binary 0 is above zero volt. OOK (on off keying) is one sort of ASK. Here the offset of the balanced modulator is adjusted in such a way that it adds a voltage to the digital signal to make a binary 0 equal to zero volt. For PSK, the offset is adjusted so that when the digital signal is binary one, the carrier is multiplied by a positive voltage. When the signal changes to binary 0, the carrier is multiplied by a negative voltage. This inverts the product making binary 0 representation of the PSK signal 180 degrees out of phase with binary one and vice versa. The absolute value of the positive and negative voltages should be kept equal.

The mod balance adjusts the amount of carrier. This is done by biasing the carrier on a dc voltage. For our purpose the modulator should always be balanced. So there is provision for skipping the balance control in case it is not needed.

The AD633J is an analog multiplier that multiplies the data and carrier to produce ASK, PSK or OOK modulated signals based on the offset. The negative terminals of the differential inputs (X- and Y-) have been grounded.

5. ENVELOPE DETECTOR:

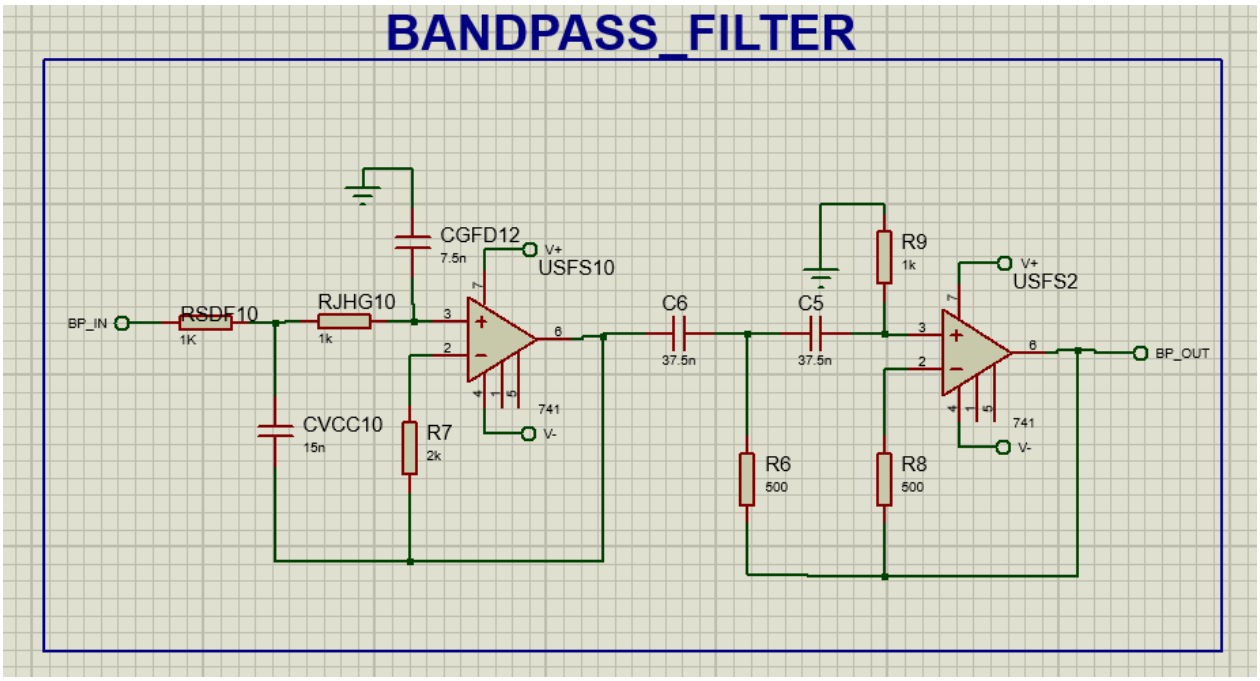


The circuit for an envelope detector requires diode, resistor and capacitor. The capacitor holds the peak value, while the resistor decays it. The decay can be made slower by choosing a larger capacitor and resistor and vice versa.

Here we used a Super-diode/ Precision Rectifier circuit in place of a simple diode for more accuracy.

This stage is followed by a low pass filter which removes the high frequency ripples formed by the envelope detection process.

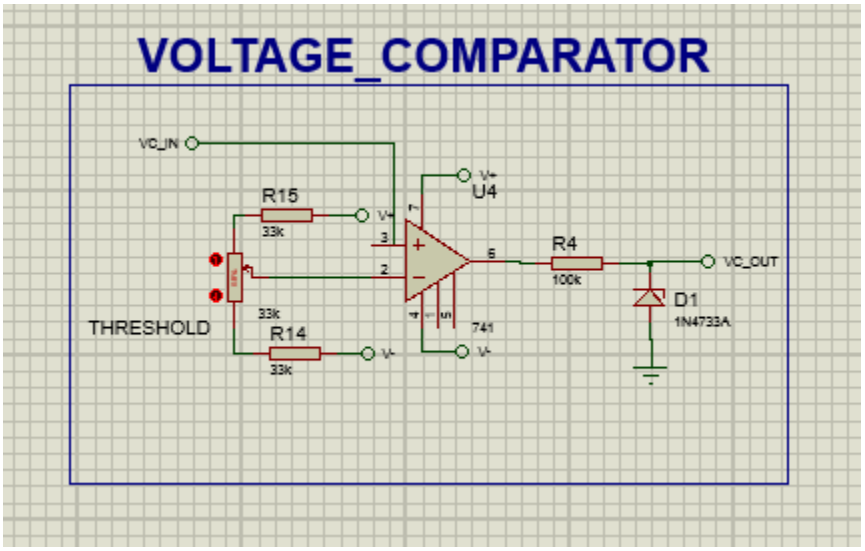
6. BANDPASS FILTER:



The bandpass filter is made by cascading a low pass filter and high pass filter. The modulated signal is passed through this filter to limit the bandwidth of the modulated signal. It is required to minimize interference in case other messages are being sent over the same channel.

This stage can be optionally skipped as in our case only one signal is being sent over the channel.

7. VOLTAGE COMPARATOR:

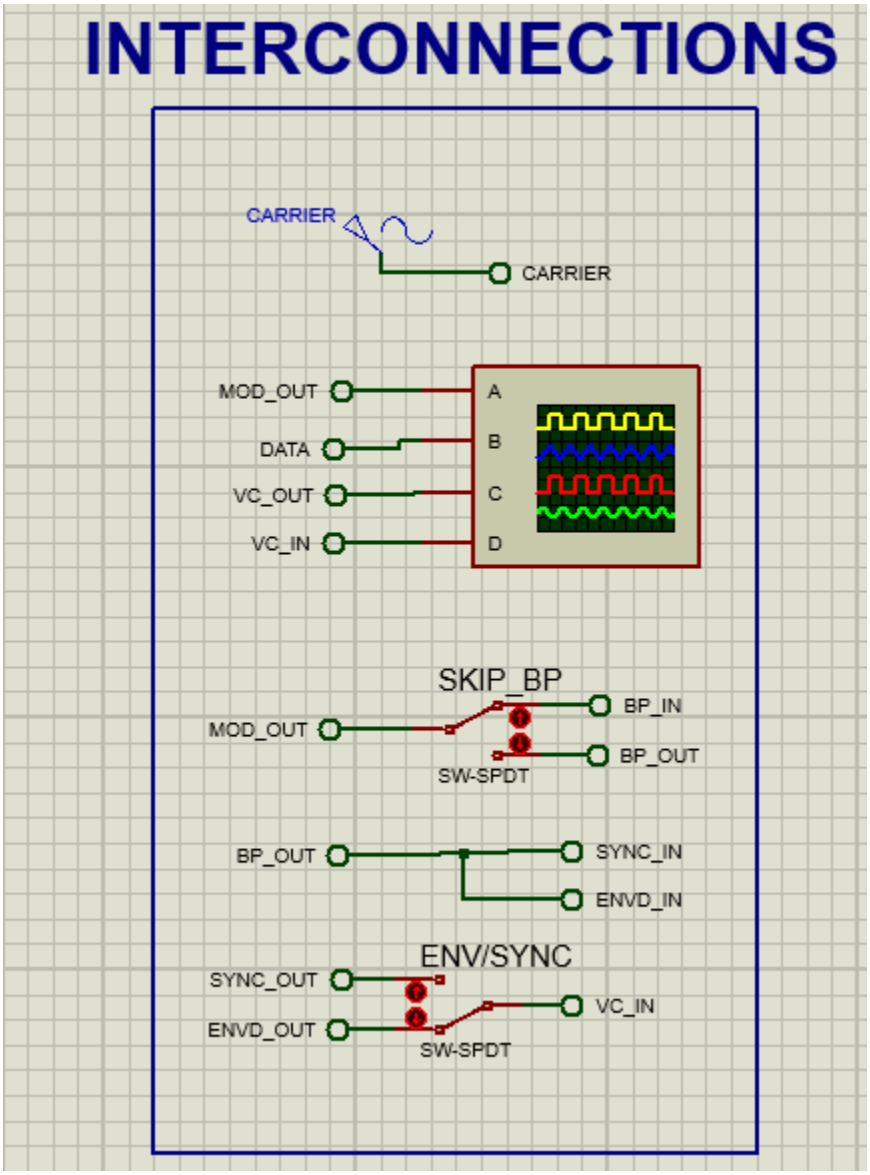


This block compares the envelope/synchronous detected signal with a particular threshold voltage and makes decision.

If the comparison yields a higher value than the threshold voltage, a high voltage level (+5V) representing binary one, otherwise a low voltage level (0V) representing binary zero will be produced.

The threshold voltage needs to be adjusted in case of envelope detection of ASK signals. For product detection it is kept exactly 0V (GND) for proper detection.

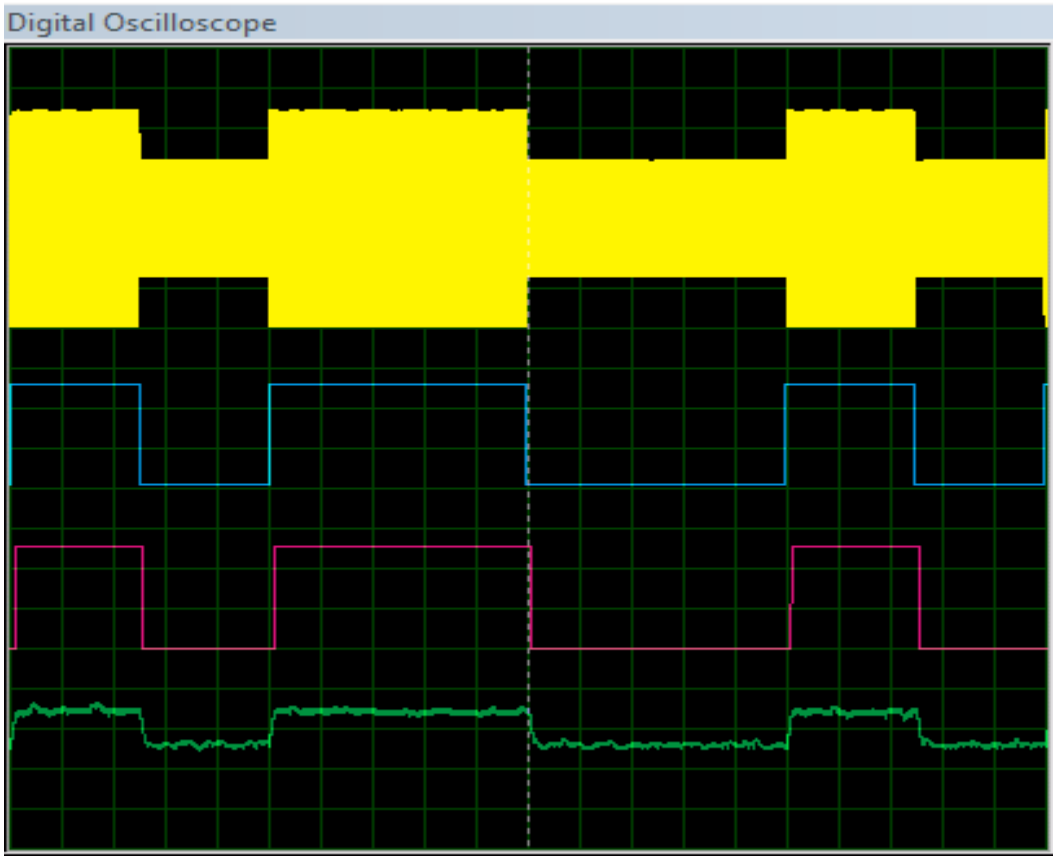
8. INTERCONNECTIONS:



This block works as user interface. A sine carrier is generated here. The oscilloscope shows all the outputs. The user can determine whether synchronous detector or envelope detectors is to be selected. Accordingly, the envelope detector/ synchronous detector output will be active. The user can also choose to skip the Bandpass Filter.

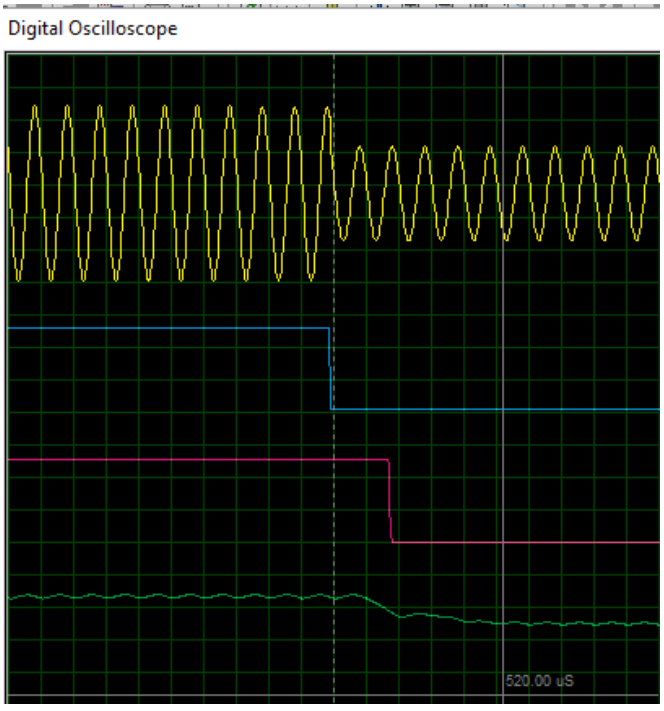
OUTPUTS:

1. **ASK MODULATED SIGNAL GENERATION AND ENVELOPE DETECTION:**

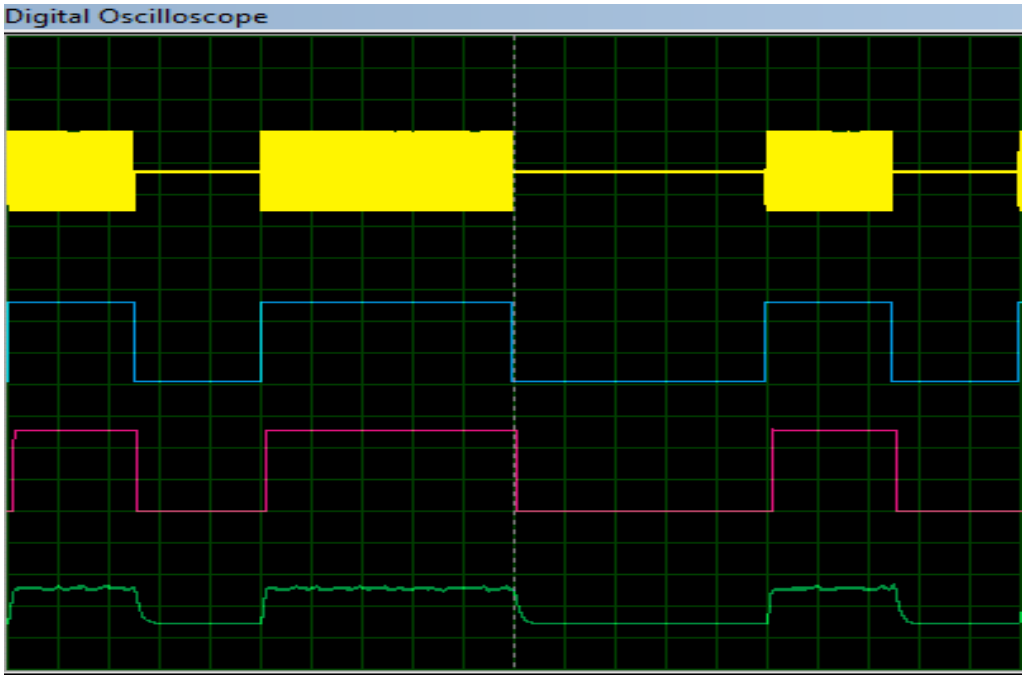


The yellow colored signal shows the ASK modulated signal and the blue colored one is the digital intelligence signal. The binary one and zeros are represented by a high and low amplitude carrier respectively. the green colored signal shows the output of envelope detector. The maroon colored is the output from voltage comparator.

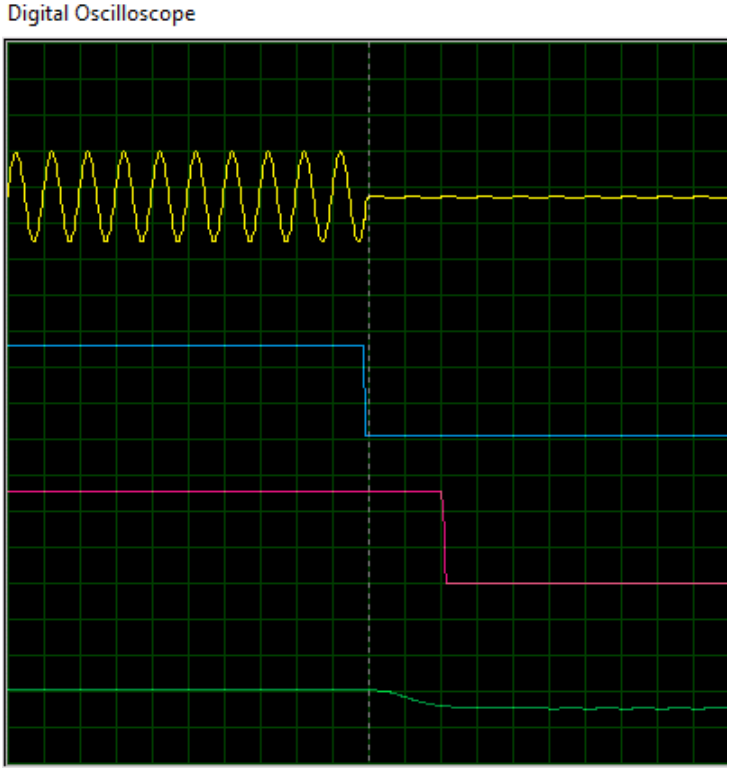
A delay from input to output is observed.



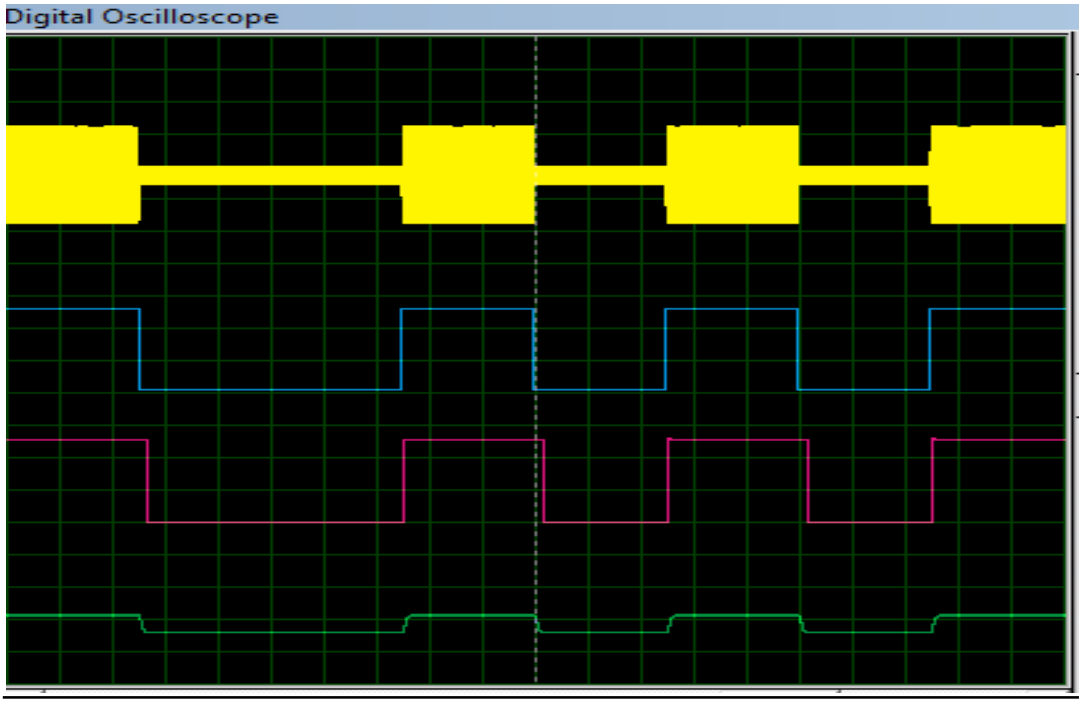
2. OOK MODULATED SIGNAL GENERATION AND ENVELOPE DETECTION:



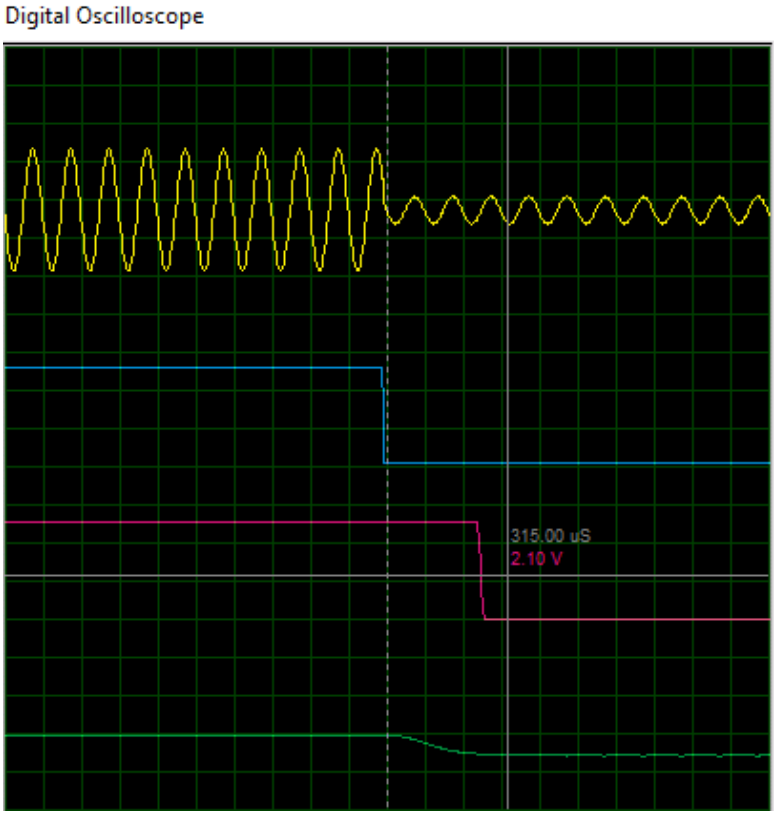
The yellow colored signal shows the OOK modulated signal and the blue colored one is the digital intelligence signal. The binary one and zeros are represented by a high and low amplitude carrier respectively. The green colored signal shows the output of envelope detector. The maroon colored is the output from voltage comparator.



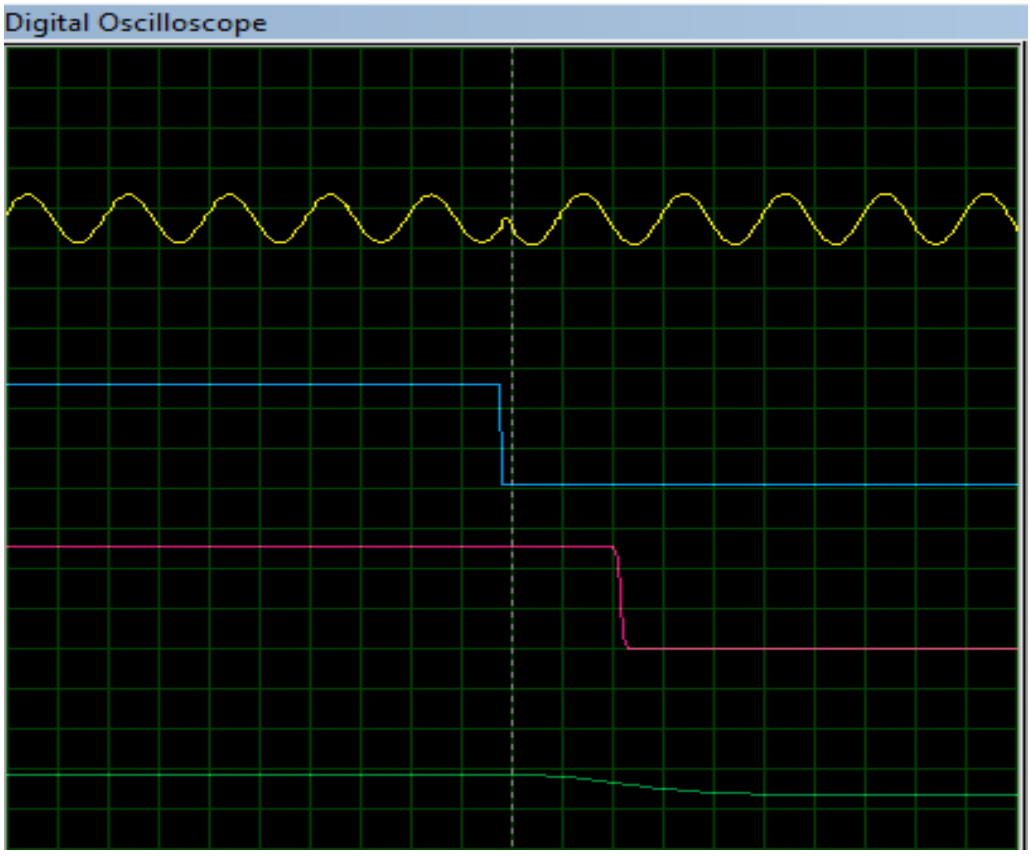
3. ASK MODULATED SIGNAL GENERATION AND COHERENT DETECTION:



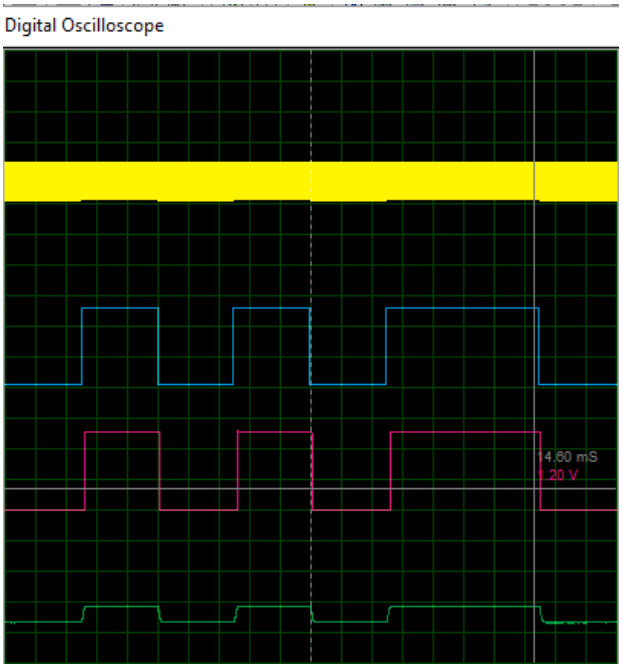
The yellow colored signal shows the ASK modulated signal and the blue colored one is the digital intelligence signal. The binary one and zeros are represented by a high and low amplitude carrier respectively. The green colored signal shows the output of PRODUCT detector. The maroon colored is the output from voltage comparator.



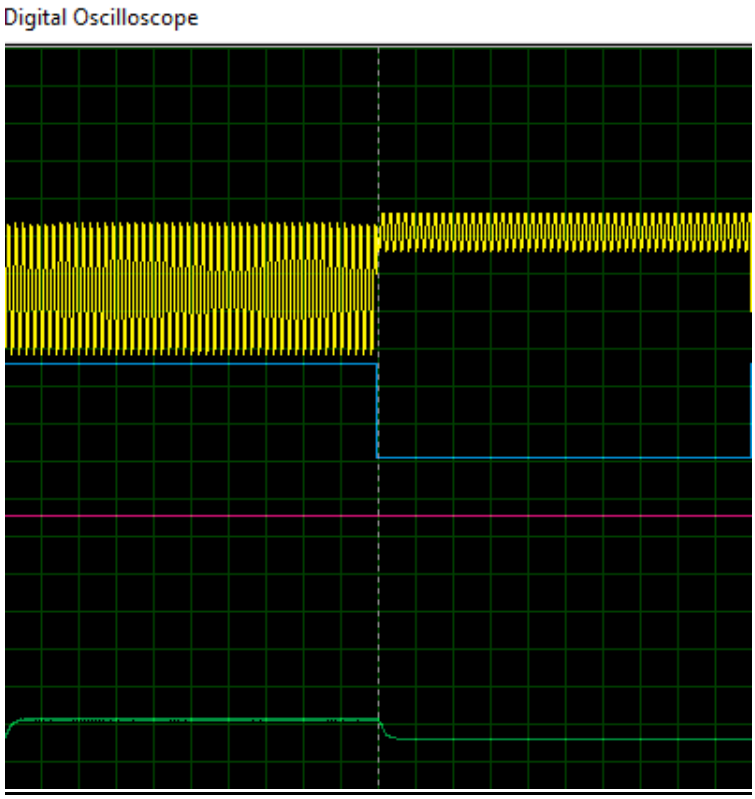
4. PSK modulated signal:



The yellow colored signal shows the PSK modulated signal and the blue colored one is the digital intelligence signal. The green colored signal shows the output of PRODUCT detector. The maroon colored is the output from voltage comparator. The amplitude of the modulated signal is constant but 180-degree phase shift is observed at the transition of the binary one and zero.



5. **Effect of changing balance of the balanced modulator:**



If the modulator is unbalanced a certain value of carrier is present in the output which leads to error in the modulation process.

Discussions:

- **Reason for delay in the detected signal:**
  There is a finite delay from the modulating signal to the output of the voltage comparator. This result from the fact that the output of the demodulators is passed through a low pass filter before voltage comparison. The low pass filter adds a certain amount of delay, which inhibits sharp change of voltage level at its output. So a certain time is required for the output signal to cross the voltage threshold of the comparator resulting in a delay. The digital circuitry and ICs also have inherent delays which is usually insignificant.
- **Further improvement:**
  We intended to add a carrier generator and frequency adjustment circuitry to our design. Also the clock and the carrier could be synchronized. But addition of these features leads to excessive CPU loads while simulation and results in SPICE convergence issues. So we omitted them from the final design.
- **Band pass Filter:**
  We did not make the band pass filter highly selective because only one signal was sent over the channel which is contrary to the situation when multiple signals closely spaced in the frequency spectrum is sent over the same channel.
- **Threshold voltage selection:**
  The threshold voltage selection process could be automated using proper logic circuitry which was omitted for simplicity.