CSC258 - Lab 1

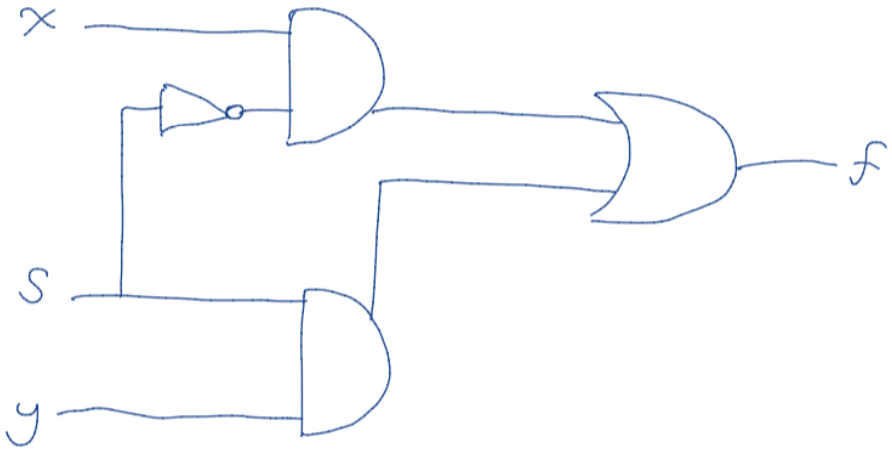
Building Circuits using Logisim Evolution

Morgan Chang

1005127113

Part I

1. Gate diagram of $f = xs' + ys$

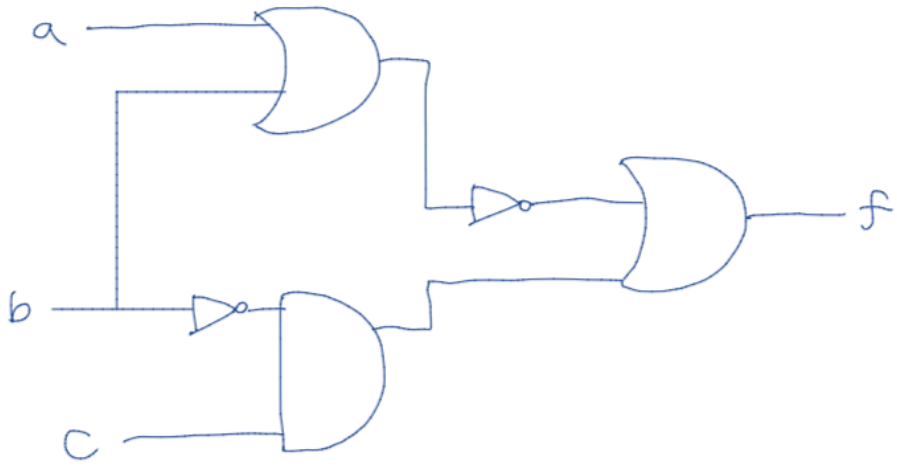


2. Truth table

s	input x	input y	output f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Part II

1. Gate diagram of $f = (a + b)' + cb'$



2. Truth table

a	b	c	output f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

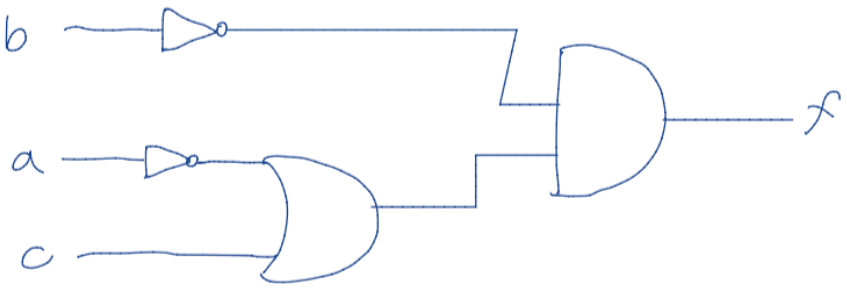
3. Yes, there is a cheaper implementation for the design, and we can achieve it by simplifying the boolean function.

$f = (a + b)' + cb'$

$= a'b' + cb'$ #de Morgan's law

$= b'(a' + c)$

Then, the gate diagram will look like:



which it has 1 fewer gate than the gate diagram from Q1.