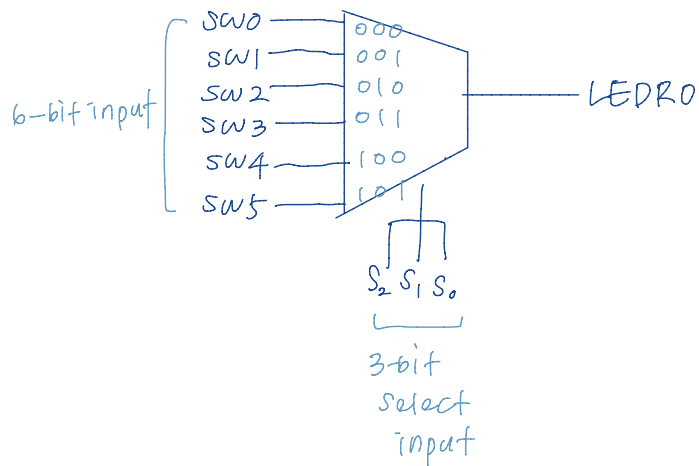


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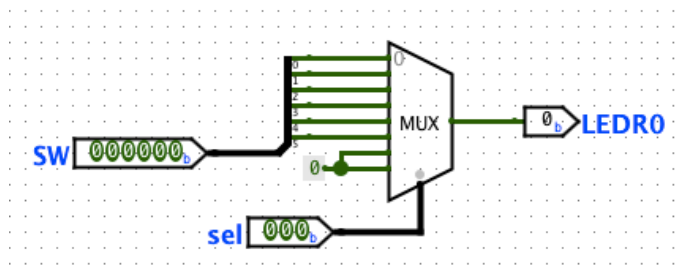
Part I

1.



(b) The multi-bit input needs to be 6 bits to provide all the inputs to a 7-to-1 mux, along with a select input.

2.

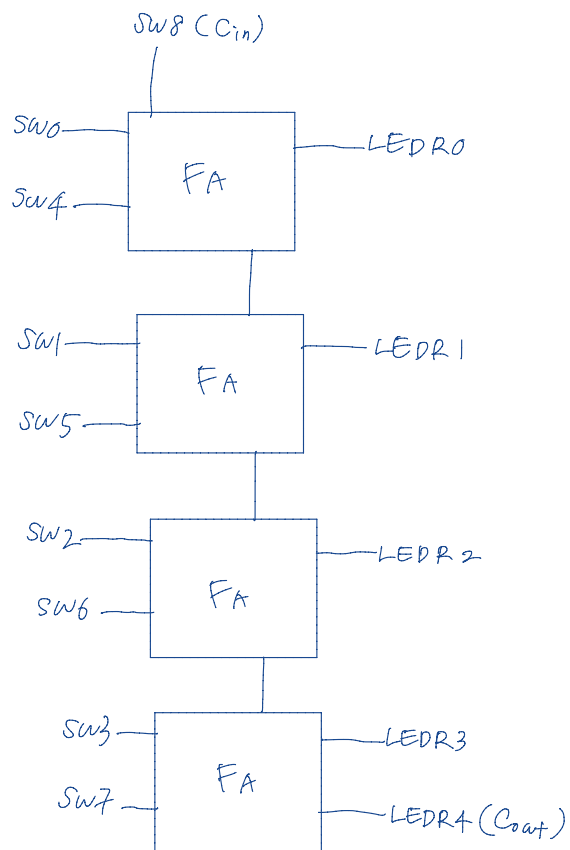


3.

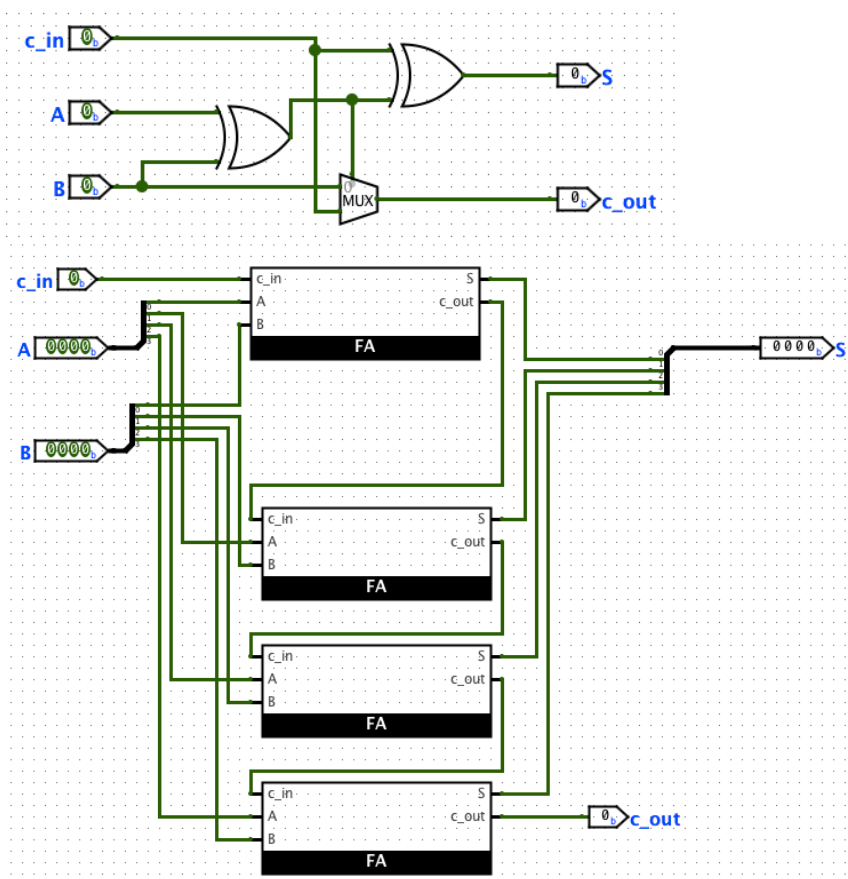
Passed: 17 Failed: 0				
status	SW	sel	LEDR0	
pass	00 0001	000	1	
pass	11 1111	000	1	
pass	00 0000	001	0	
pass	00 0010	001	1	
pass	11 1111	001	1	
pass	00 0000	010	0	
pass	00 0100	010	1	
pass	11 1111	010	1	
pass	00 0000	011	0	
pass	00 1000	011	1	
pass	11 1111	011	1	
pass	00 0000	100	0	
pass	01 0000	100	1	
pass	11 1111	100	1	
pass	00 0000	101	0	
pass	10 0000	101	1	
pass	111111	101	1	

Part II

1.



2.



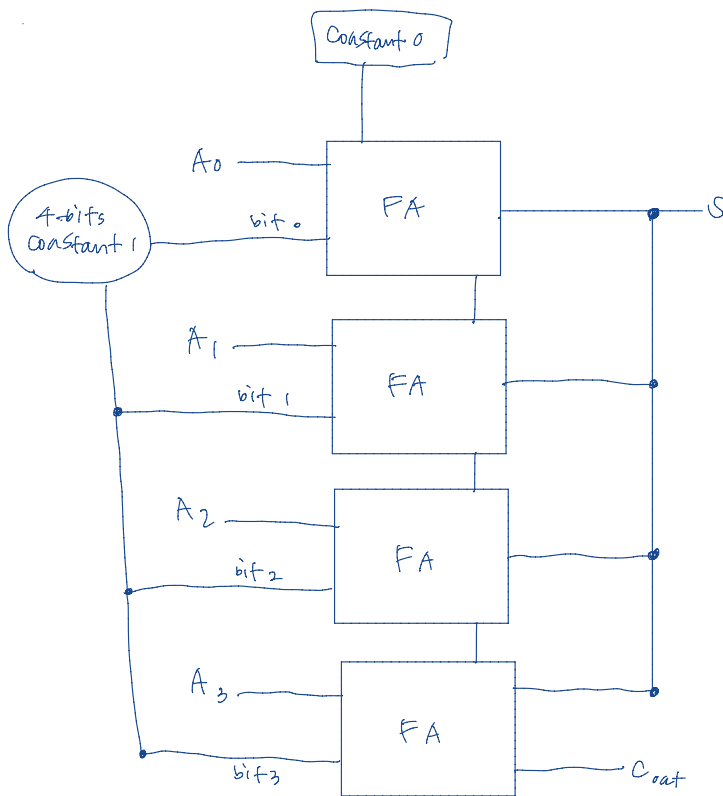
3.

Passed: 6 Failed: 0					
status	c_in	A	B	c_out	S
pass	0	0000	0000	0	0000
pass	1	0000	0000	0	0001
pass	0	1111	1111	1	1110
pass	1	1111	1111	1	1111
pass	0	1010	0101	0	1111
pass	1	1010	0101	1	0000

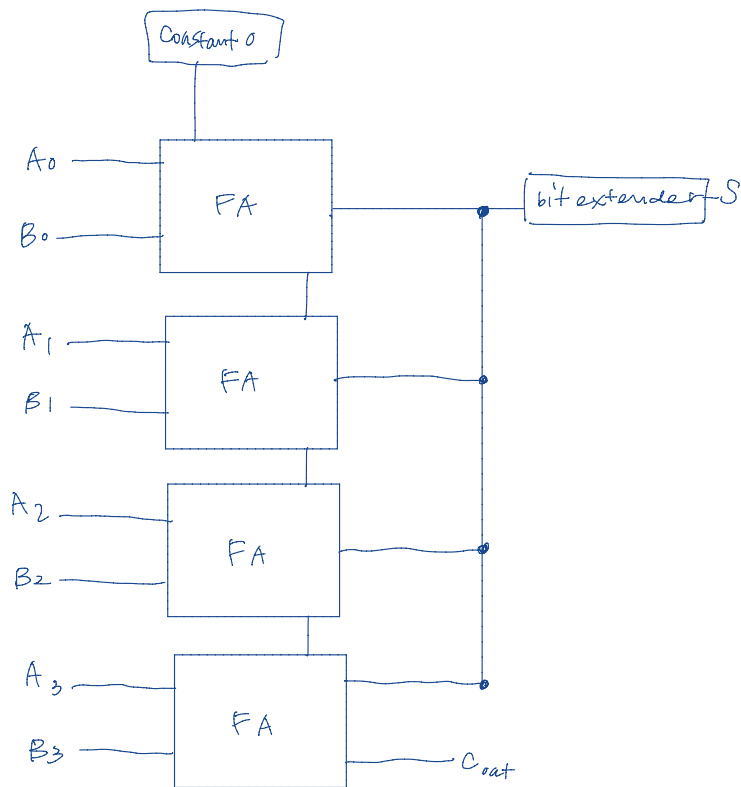
Part III

1.

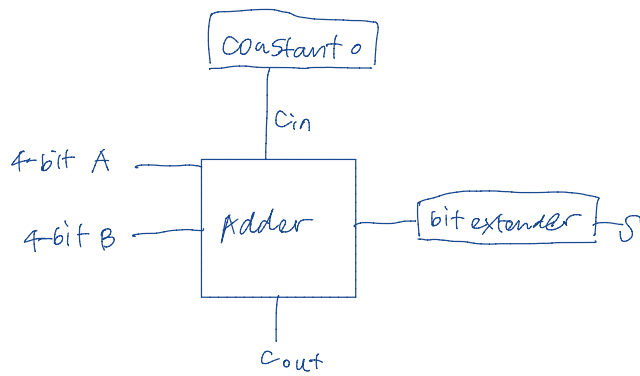
function value 0



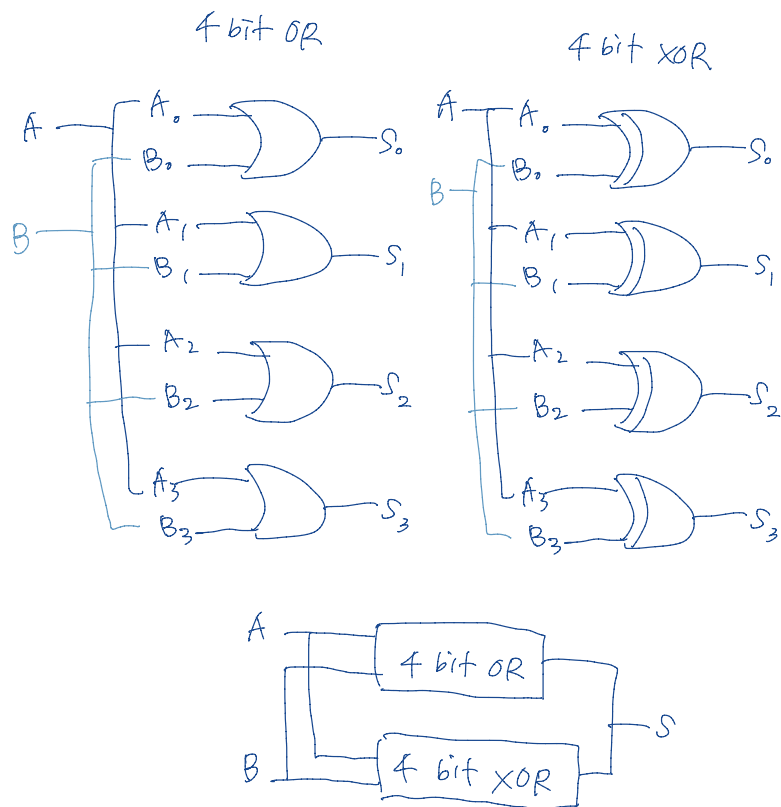
function value 1



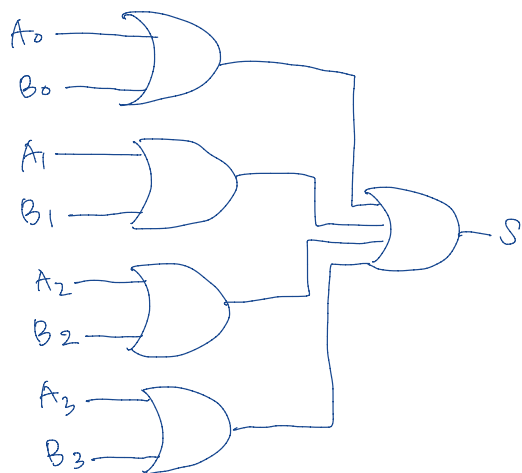
function value 2



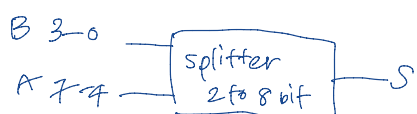
function value 3



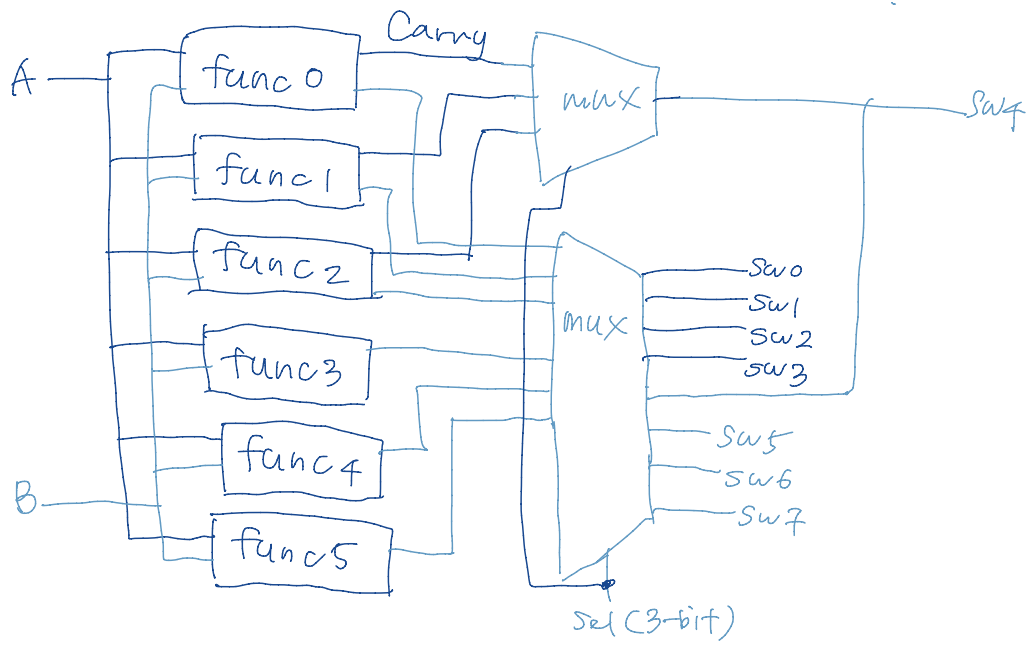
function value 4



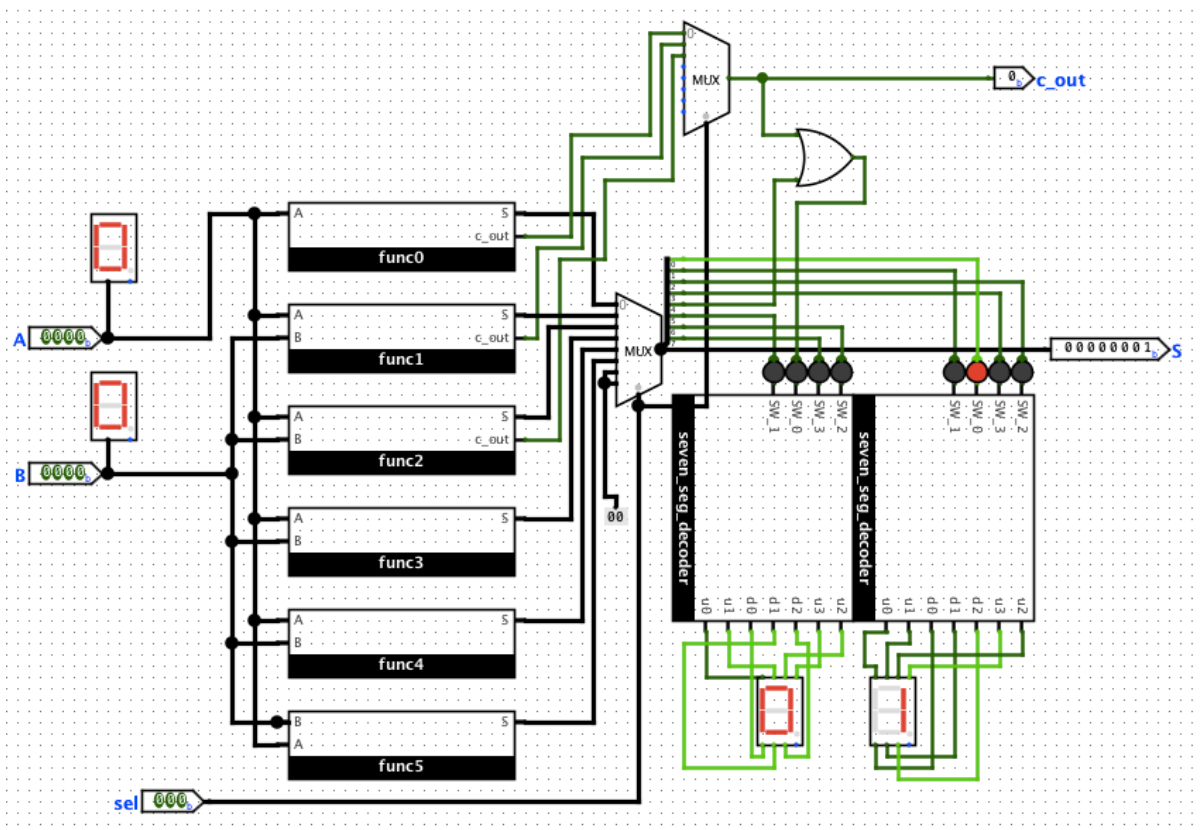
function value 5



ALU



2.



3.

Passed: 12 Failed: 0						
status	A	B	sel	c_out	S	
pass	0000	0000	000	0	0000	0001
pass	1111	0000	000	1	0000	0000
pass	0011	0101	001	0	0000	1000
pass	1111	0101	001	1	0000	0100
pass	0011	0101	010	0	0000	1000
pass	1111	0101	010	1	0000	0100
pass	1111	0101	011	x	1010	1111
pass	0000	0101	011	x	0101	0101
pass	0000	0000	100	x	0000	0000
pass	0010	0000	100	x	0000	0001
pass	0101	1010	101	x	0101	1010
pass	1000	0001	101	x	1000	0001