CSC258

Lab 4

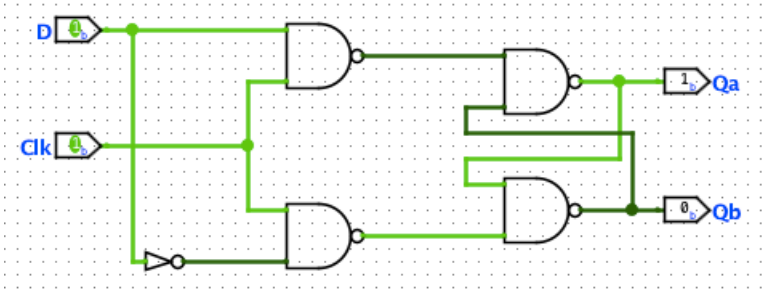
Morgan Chang

1005127113

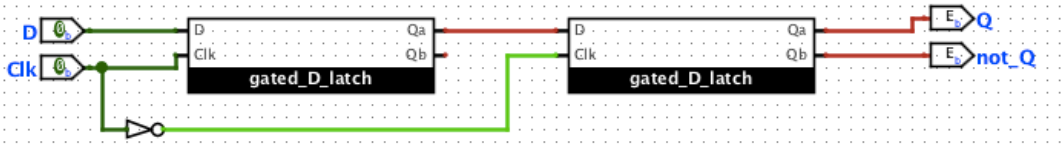
Part I

1.

gated D latch



master slave flip-flop



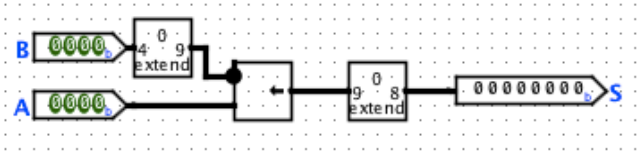
2. For the latch, when the Clk input is low, even if the input D changes, the output Q will not change. The output Q will stay at the same value as its previous stage whenever the Clk is low. For the flip-flop, the output Q will change after every two switches of the Clk input. When the Clk signal is high, the input D is sent out from the first latch to the second. And when the Clk signal goes from high to low, the D signal transmits to the output Q.

3. We should not first test the latch and the flip-flop when the Clk input is low. When the Clk input is first set to low, no matter input D is high or low, no signal will go through the stage. And thus, no signal be at the output Q.

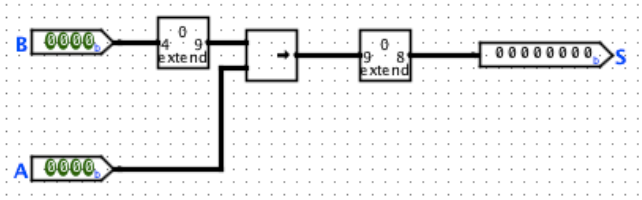
Part II

1.

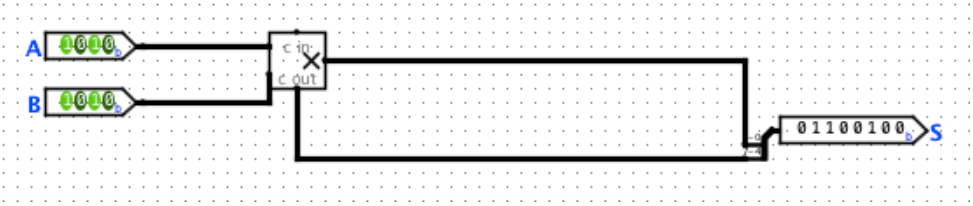
function value 5



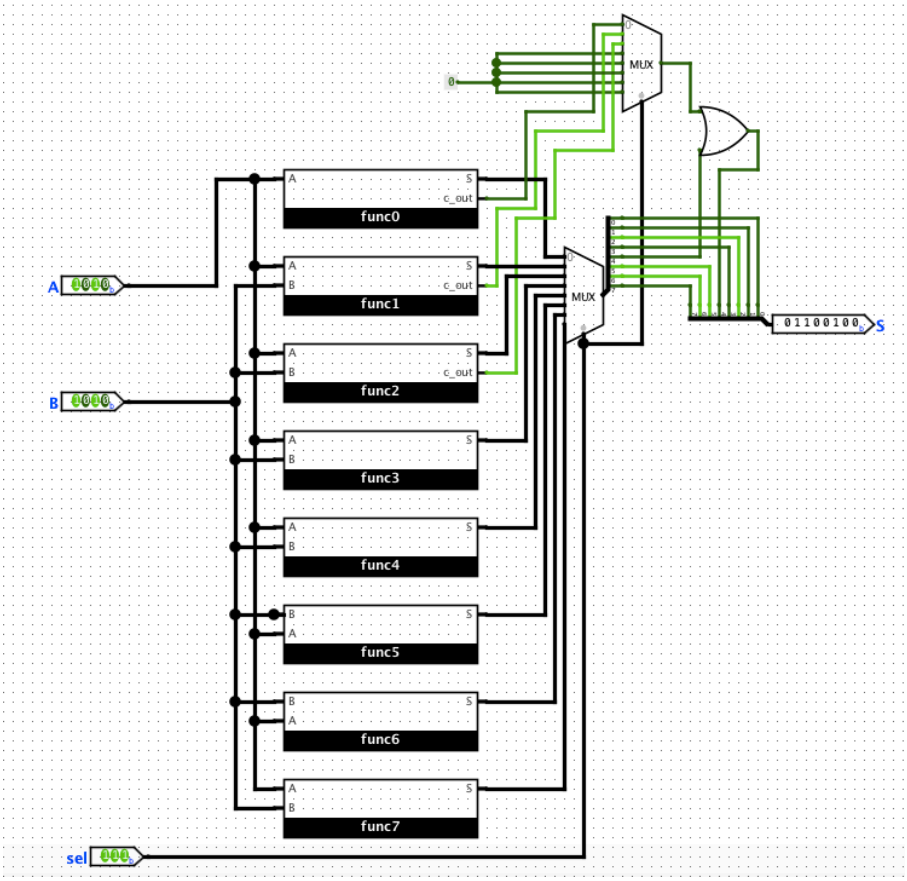
function value 6



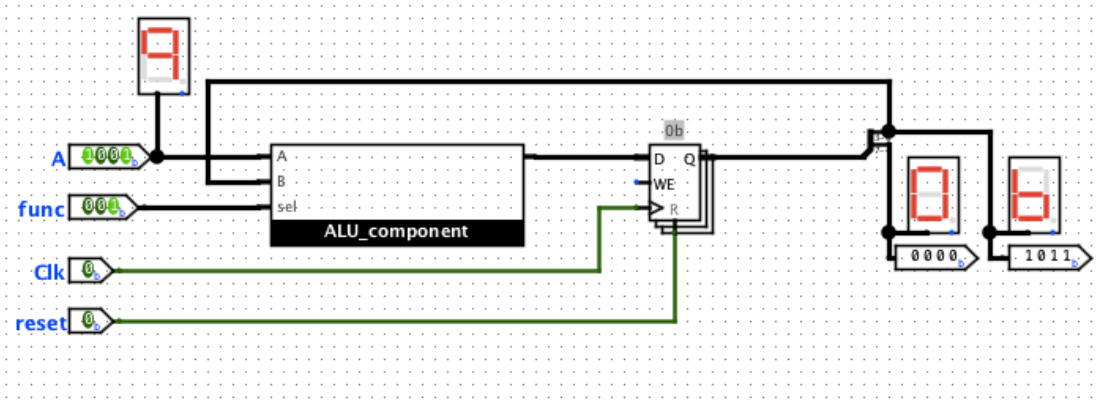
function value 7



ALU component



ALU



2.

(a) If we didn't include the register in the diagram, the circuit of input B will enter an infinite loop.

(b) The result will be 2n bit long when multiplying two n-bit binary numbers.

3.

(a)

Each row is the result of each rising edge of the clock pulse, without resetting (reset = 0) throughout the test.

A[4] S1[4] S2[4]

#function value 0 (000)

0001 0000 0010

0111 0000 1000

#function value 1 (001)

0101 0000 1101

1001 0001 0110

#function value 2 (010)

0001 0000 0111

0011 0000 1010

#function value 3 (011)

0011 1001 1011

0000 1011 1011

#function value 4 (100)

0000 0000 0000

0000 0000 0001

#function value 5 (101)

0000 0000 0001

0001 0000 0010

#function value 6 (110)

0001 0000 0001

#function value 7 (111)

0011 0000 0011

0111 0001 0101

(b)

function value 5

Passed: 5 Failed: 0

status	B	A	S
pass	1010	0001	0001 0100
pass	1010	0010	0010 1000
pass	1010	0011	0101 0000
pass	1010	0100	1010 0000
pass	1010	1111	0000 0000

function value 6

Passed: 5 Failed: 0

status	B	A	S
pass	1010	0001	0000 0101
pass	1010	0010	0000 0010
pass	1010	0011	0000 0001
pass	1010	0100	0000 0000
pass	1010	1111	0000 0000

function value 7

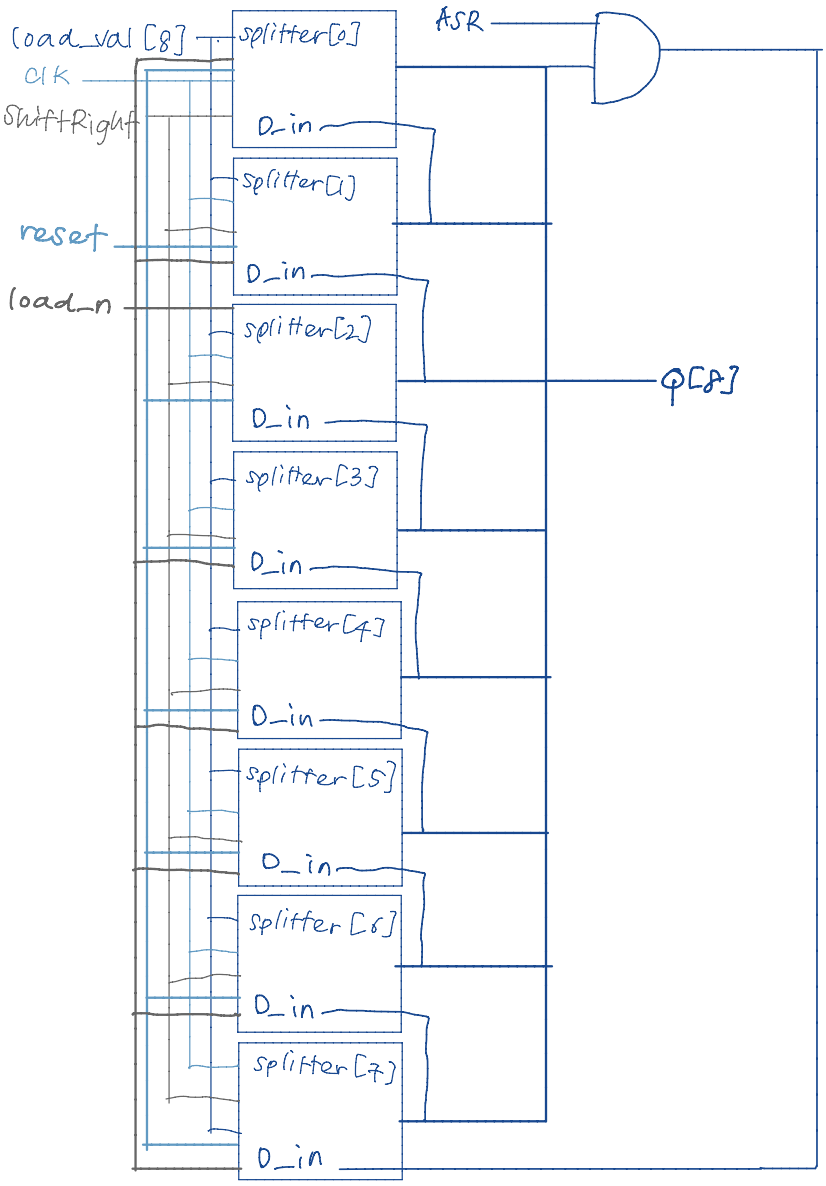
Passed: 6 Failed: 0

status	A	B	S
pass	1010	1010	0110 0100
pass	0000	1010	0000 0000
pass	1010	0000	0000 0000
pass	0001	1010	0000 1010
pass	0001	0001	0000 0001
pass	1111	1111	1110 0001

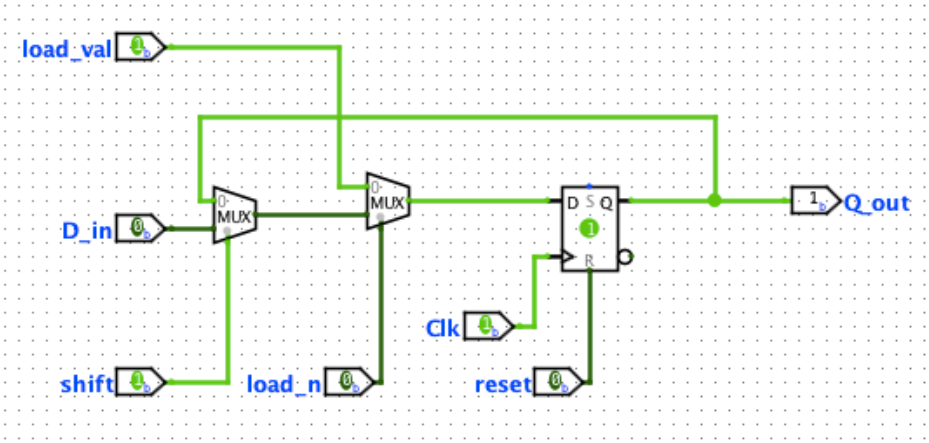
Part III

1. Without turning ShiftRight high, the bits of the register will not shift and stays at the same place on every positive clock edge.

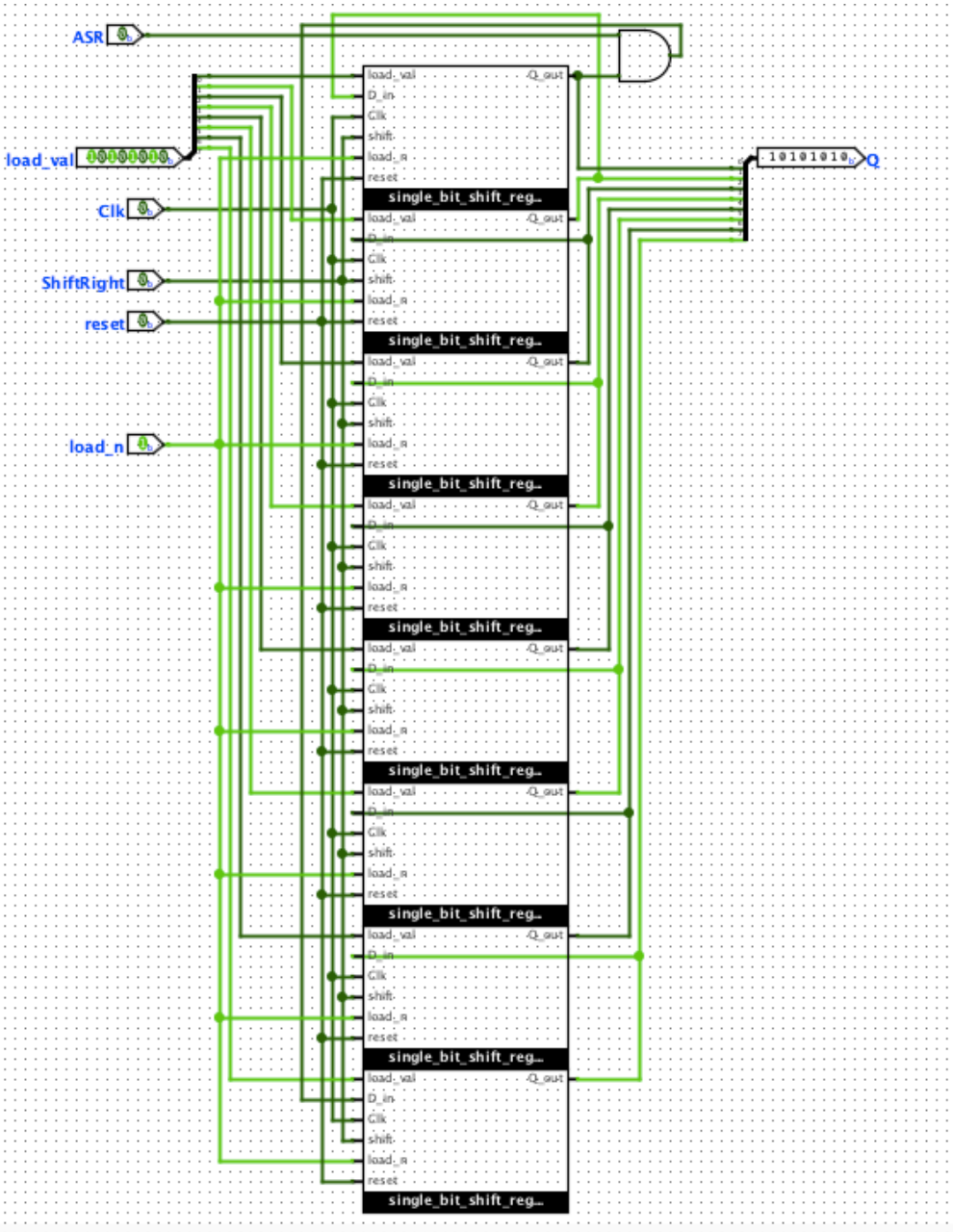
2. Each square represent a single-bit shift-register.



3.

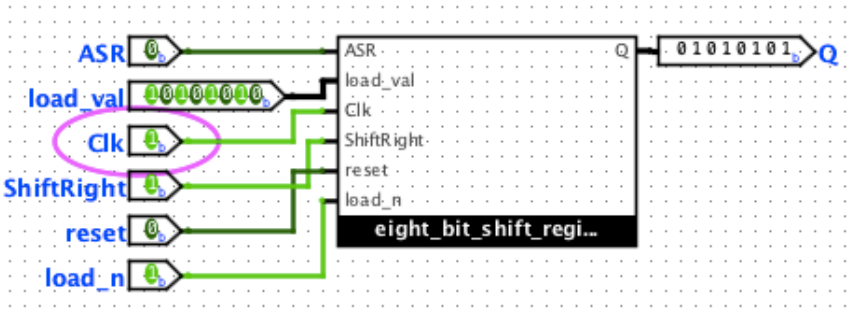

load_val
D_in
shift
load_n
Clk
reset
MUX
MUX
D S Q
R
Q_out

4.

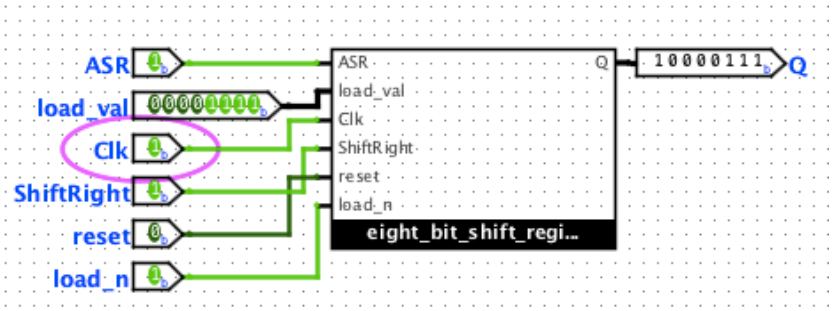

ASR
load_val
Clk
ShiftRight
reset
load_n
10101010
Q
single_bit_shift_reg...

5.

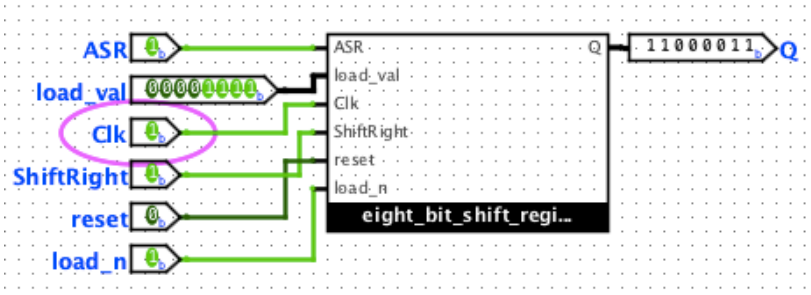
load_val = 10101010, ASR = 0, ShiftRight = 1, load_n = 1, after one positive clock edge (cycle 1):



load_val = 00001111, ASR = 1, ShiftRight = 1, load_n = 1, after one positive clock edge (cycle 1):



cycle 2:



load_val = 10000001, ASR = 0, ShiftRight = 0, load_n = 1, after one positive clock edge (cycle 1):