CSC258

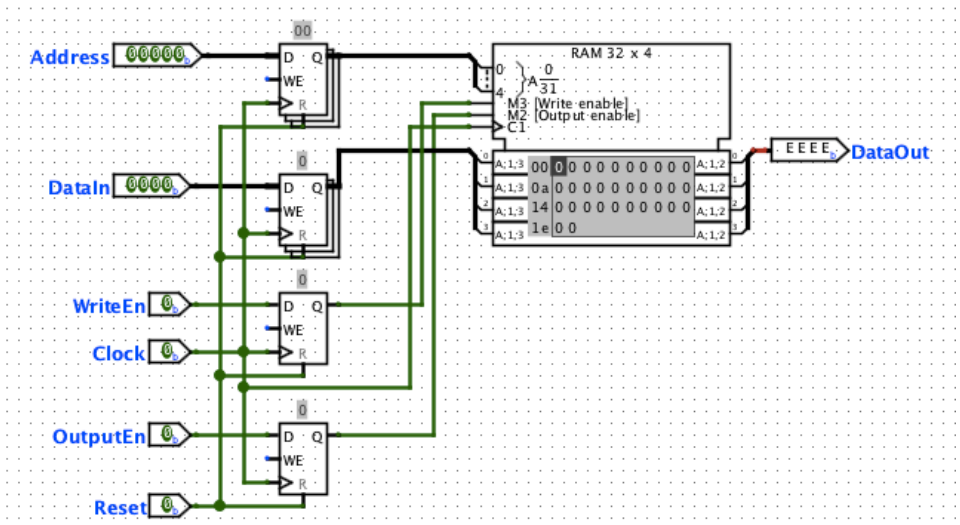
Lab 7

Morgan Chang

1005127113

Part I

1.



2.

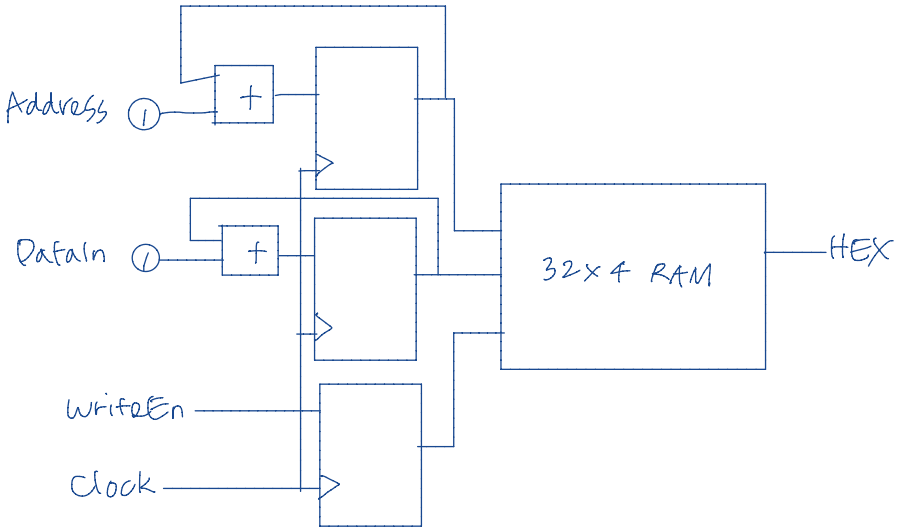
What happens if both Write Enable and Output Enable signals are off when the clock goes high?

Nothing is written into the RAM nor shown on the DataOut output signal.

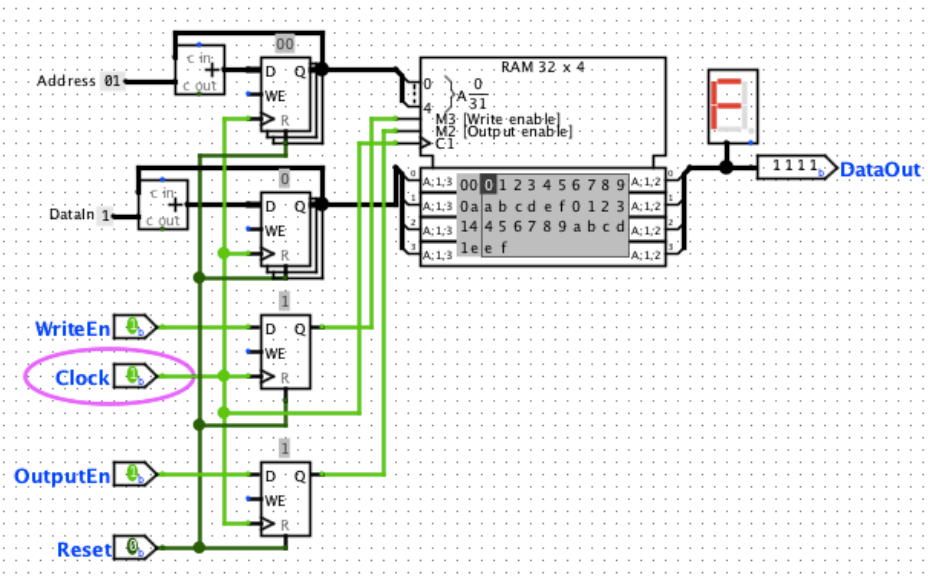
What happens when both signals are on?

The specified address is highlighted in the RAM at the first positive clock pulse and the DataIn is written into the RAM at that specified address and is shown on the DataOut output at the second positive clock pulse.

5.


Address
1
+
DataIn
1
+
32x4 RAM
HEX
WriteEn
Clock

6.


Address 01
c in
c out
00
D Q
WE
R
DataIn 1
0
1
WriteEn
Clock
OutputEn
Reset
RAM 32 x 4
A
M3 [Write enable]
M2 [Output enable]
C1
1111
DataOut

Part II

What happens if you don't turn Enable off before updating X and Y?

The square will be drawn at a wrong location since the x and y coordinate will not be updated correctly. In my implementation specifically, the location of y-coordinate will remain the same because it is only loaded at the first positive clock edge after the enable turn off then back on.

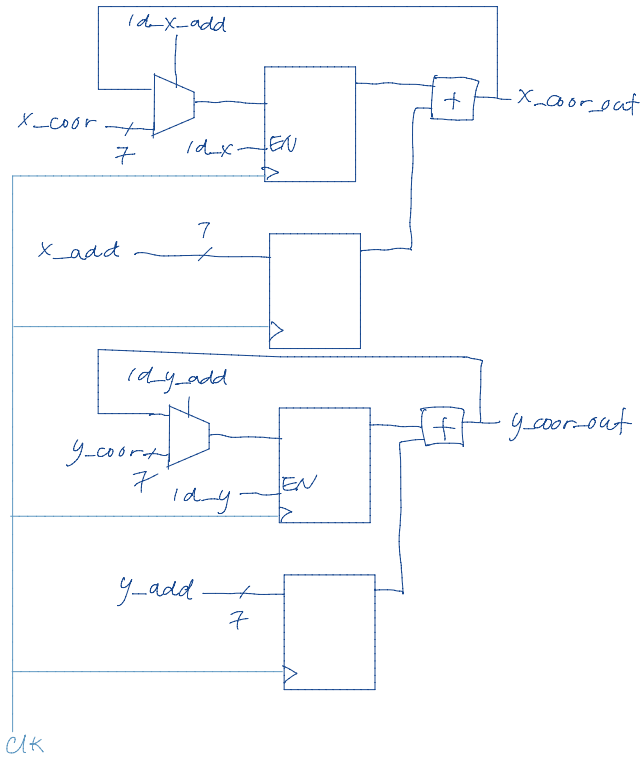
What happens if you turn Enable off before 256 clock cycles have passed?

Nothing will be painted onto the screen. The circuit will draw squares on the screen only when the enable signal is high.

What happens if you turn Reset on while Enable is on?

Nothing will be drawn onto the screen because the reset signal sets the screen to all black when it's high.

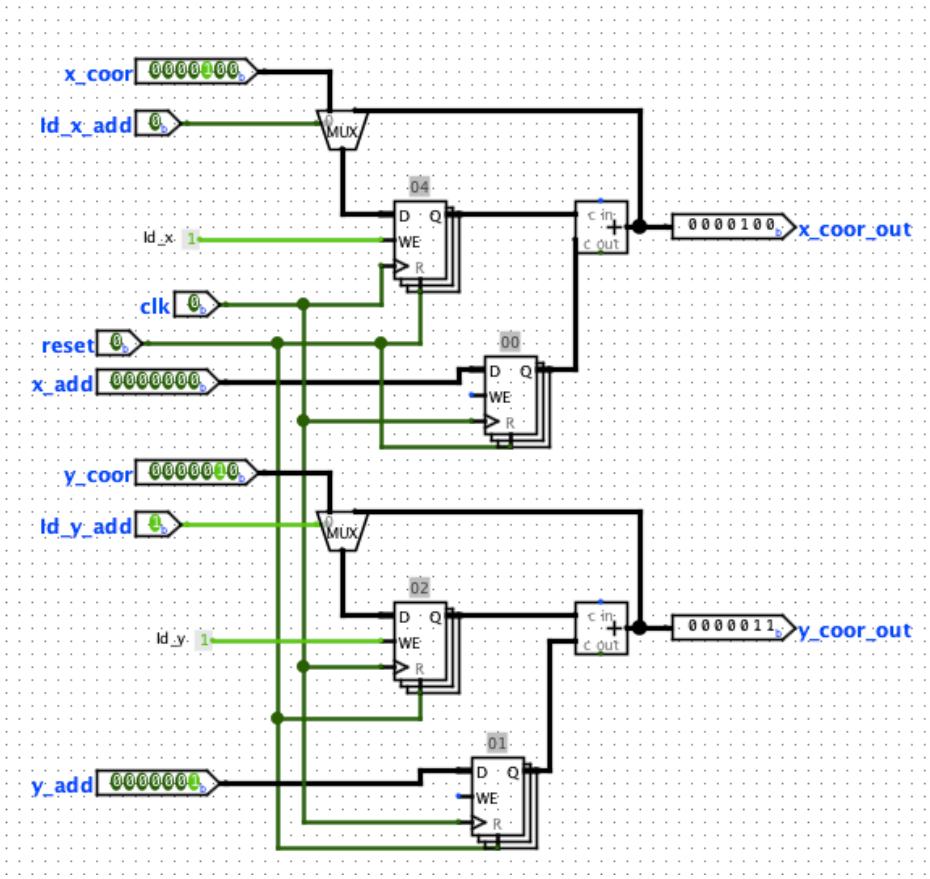
1.



Id_x & Id_y: load x_coor and y_coor into the register

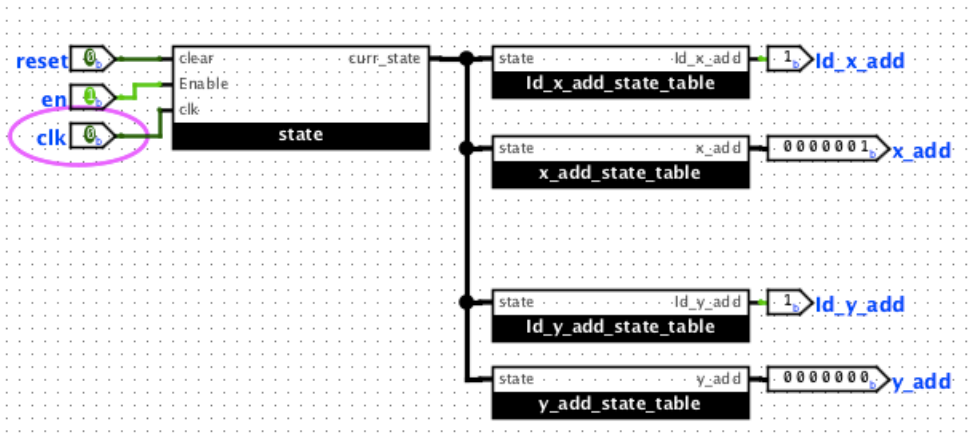
x_add & y_add: add 1 to x_coor and y_coor

Id_x_add & Id_y_add: when 1, allow rewrite into the register that stores x_coor and y_coor

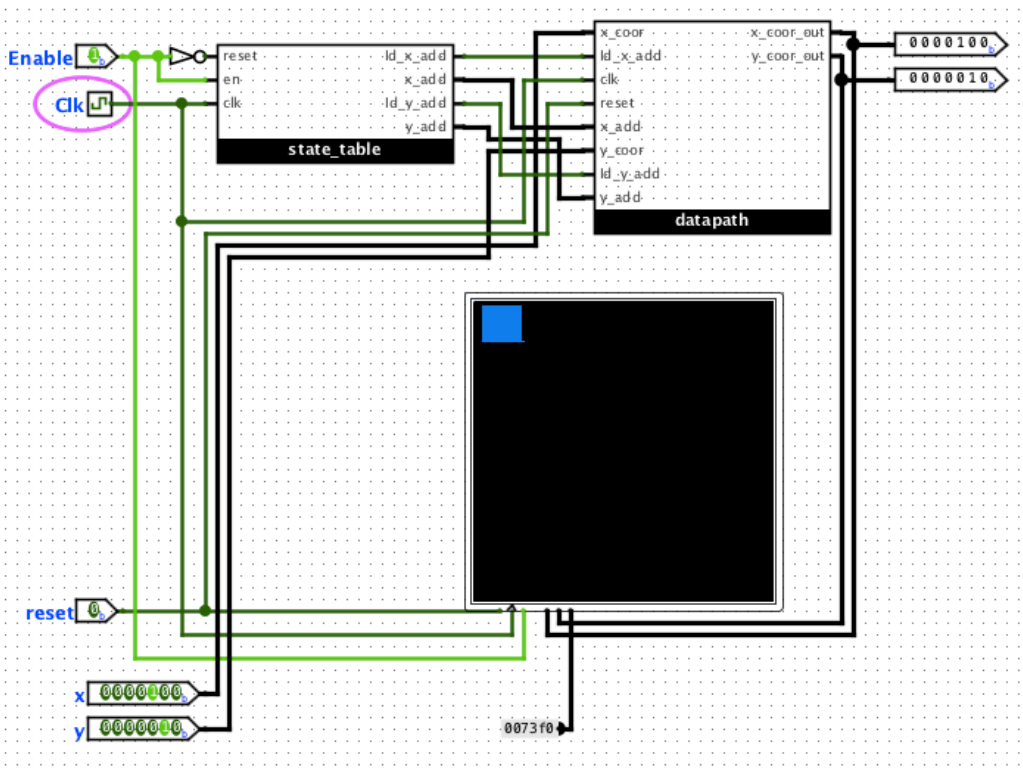


2.

state	ld_x	ld_x_add	x_add	ld_y	ld_y_add	y_add
00000	1	0	0	1	0	0
11111	1	1	1	1	1	0
11110	1	1	1	1	1	0
11101	1	1	1	1	1	0
11100	1	1	1	1	1	0
11011	1	1	1	1	1	0
11010	1	1	1	1	1	0
11001	1	1	1	1	1	0
11000	1	1	1	1	1	0
10111	1	1	1	1	1	0
10110	1	1	1	1	1	0
10101	1	1	1	1	1	0
10100	1	1	1	1	1	0
10011	1	1	1	1	1	0
10010	1	1	1	1	1	0
10001	1	1	1	1	1	0
10000	1	0	0	1	1	1



3.


Enable
Clk
reset
en
clk
ld_x_add
x_add
ld_y_add
y_add
state_table
x_coor
ld_x_add
clk
reset
x_add
y_coor
ld_y_add
y_add
datapath
x_coor_out
y_coor_out
0000100
0000010
reset
x
y
0073f0