CSC258

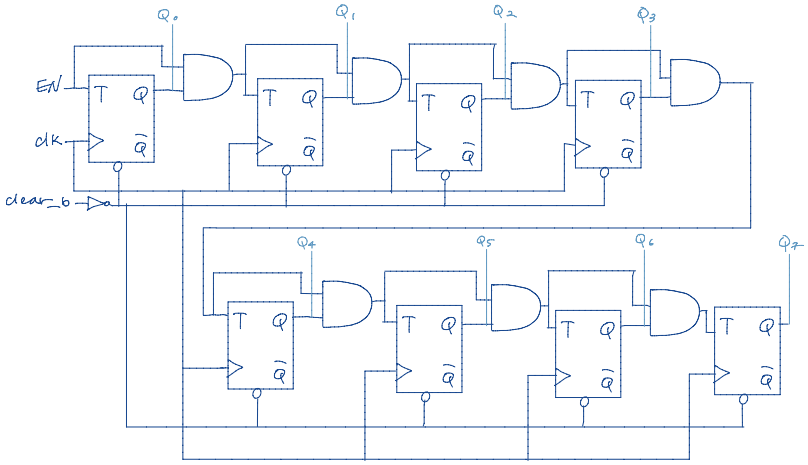
Lab 5 Pre Lab

Morgan Chang

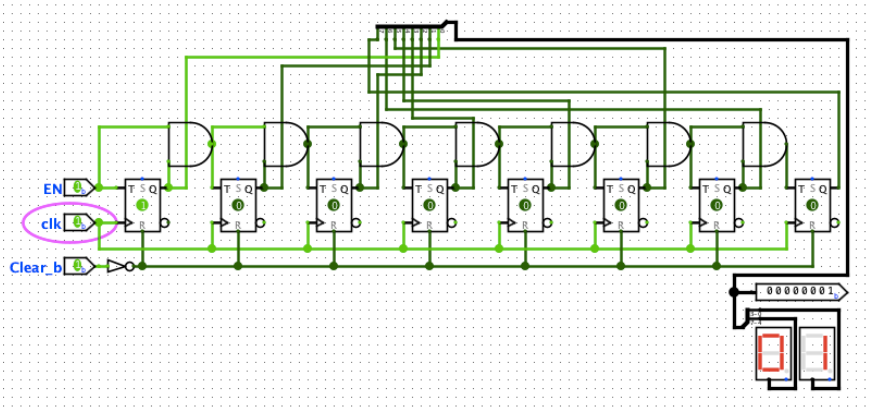
1005127113

Part I

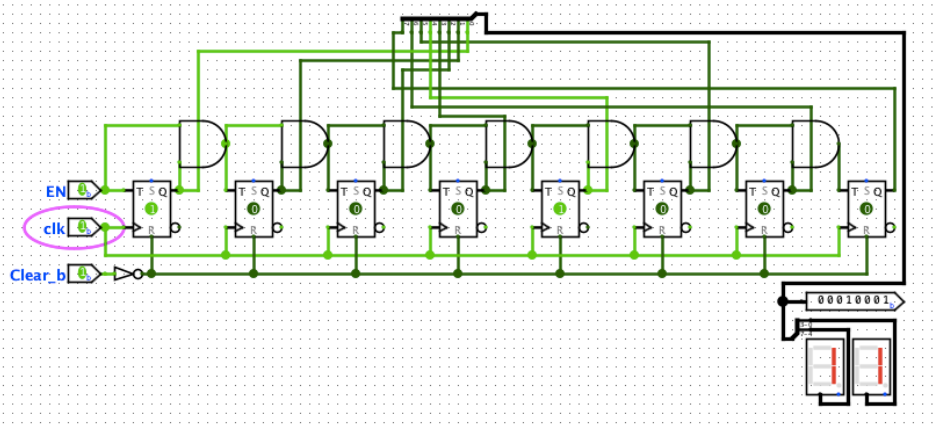
1 & 2.



5. After one positive edge of the clock:



After 17 positive edge of the clock:



Part II

Figure 2: 4-bit counter

1. The check for maximum value is not necessary in the example because counting in hexadecimal is the default setting.
2. If we want this 4-bit counter to count from 0-9, we first have to change the maximum value in this counter's properties. Then we will have to remove bit 1 and bit 2 of this counter's output to the AND gate.
3.

- Wrap around: the value get back to 0
- Stay at value: the value remains at the maximum
- Continue counting: the value continue incrementing
- Load next value: load next value from the D input

Figure 3:

Calculate how large a counter would be required to count 50 million clock cycles, as illustrated by Figure 3. How many binary bits would that counter need to represent such a value?

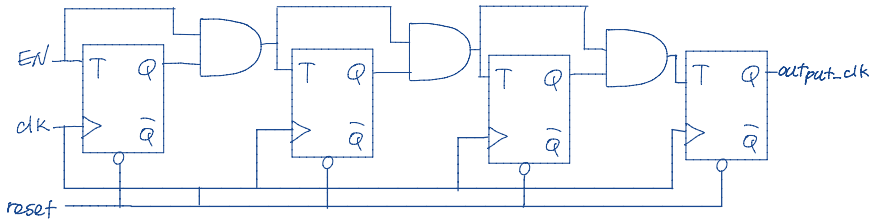
We will need 26 binary bits, then we would have $2^{26} > 50$ million to represent such value.

Circuit:

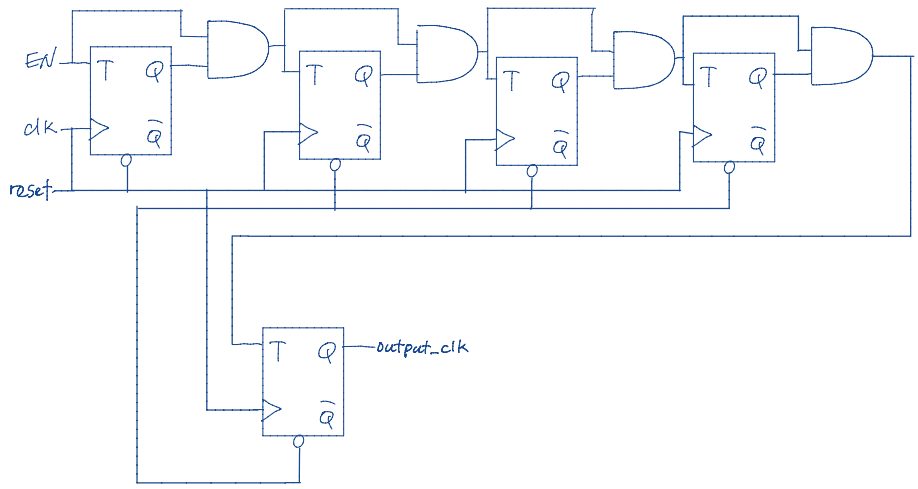
1. *revision after simulation:

- Adding constant 1 using Arithmetic Adder to the output of each speed. (If constant 1 is not added, the output of main circuit will not work properly for the first 7-segment display increment, which it will increase by 1 after only half the amount of 16 Hz clock pulses)
- Changing the final OR gate in RD to a 4-to-1 mux, with select input connected to SW[0] and SW[1]

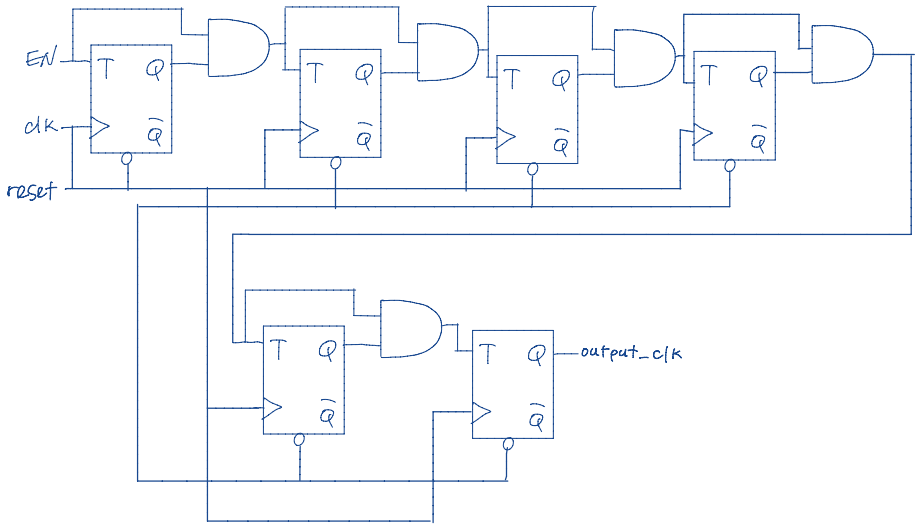
Speed: 1Hz



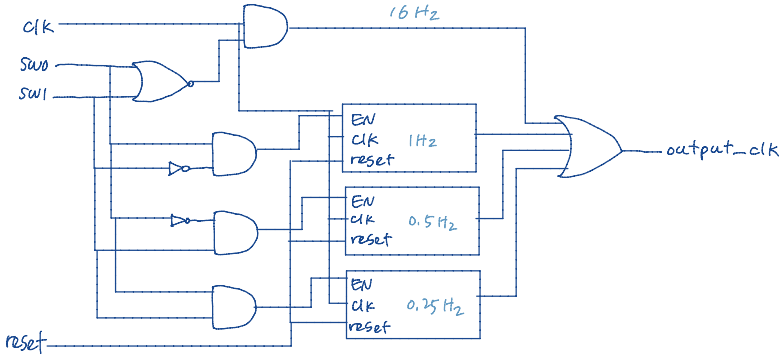
Speed: 0.5 Hz



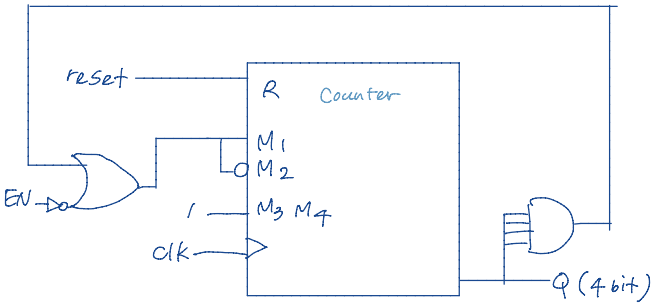
Speed: 0.25 Hz



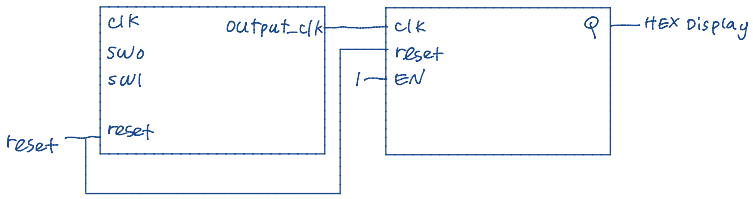
Rate Divider



Display Counter



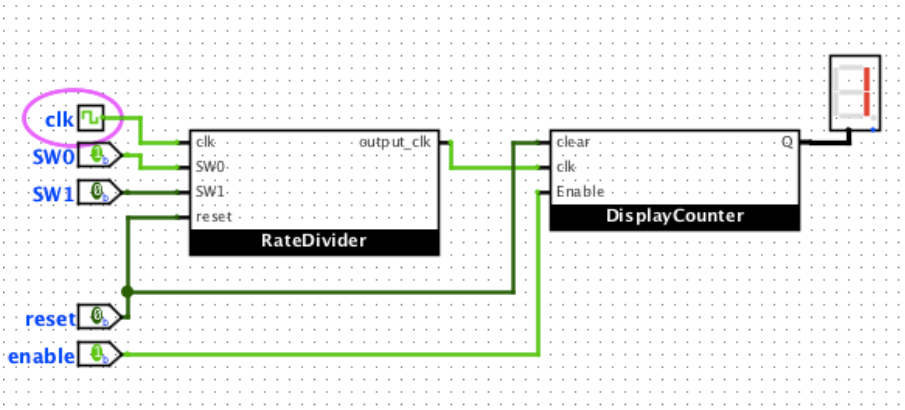
main circuit



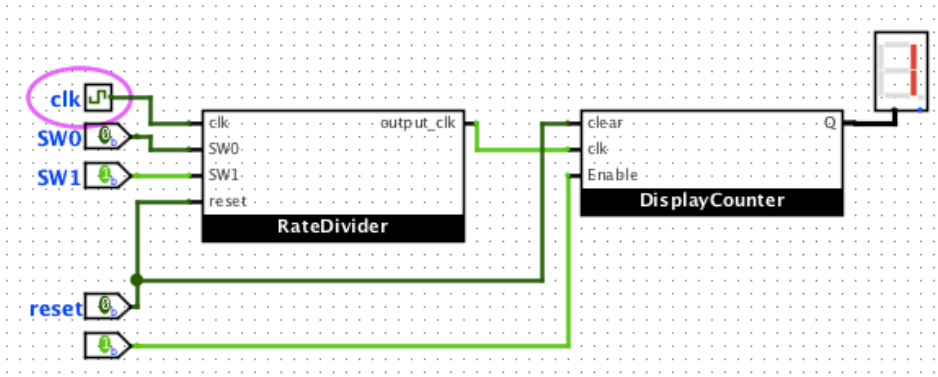
3. How many 16 Hz clock pulses will you need to simulate to show that the RateDivider is properly outputting a 1 Hz pulse?

We will need to simulate the clock with 16 positive edge of 16 Hz clock pulses and see if the 7-segment display increases by 1 to show the RateDivider is properly outputting a 1 Hz pulse.

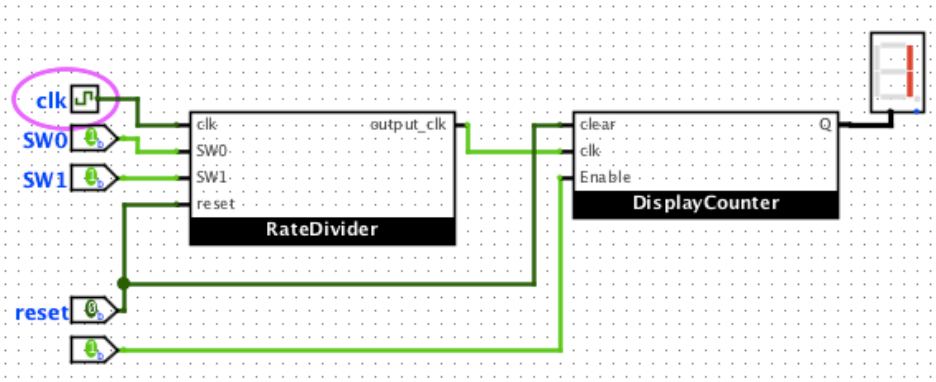
Speed: 1 Hz. After 16 positive clock edge of 16 Hz clock pulses, the 7-segment display increases by 1.



Speed: 0.5 Hz. After 32 positive clock edge of 16 Hz clock pulses, the display increases by 1.



Speed: 0.25 Hz. After 64 positive clock edge of 16 Hz clock pulses, the display increases by 1.

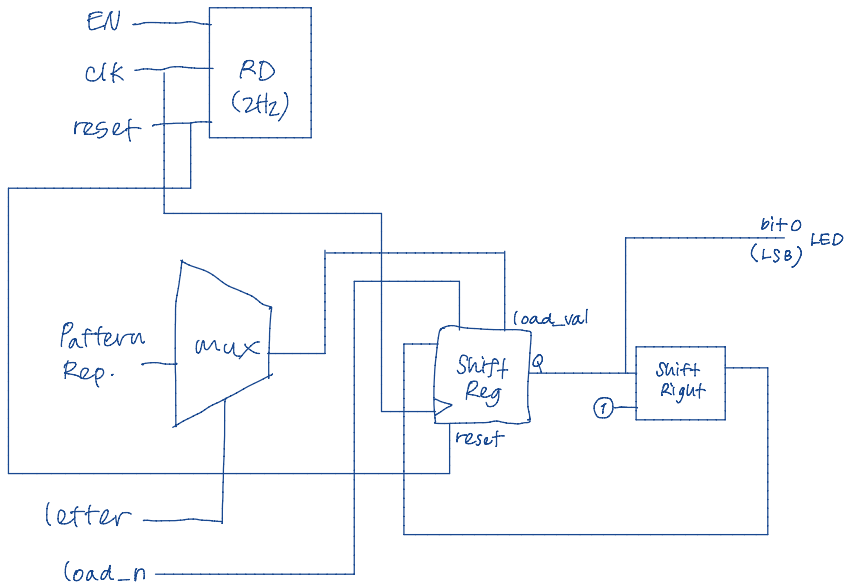


Part III

1. Table 1 (LUT):

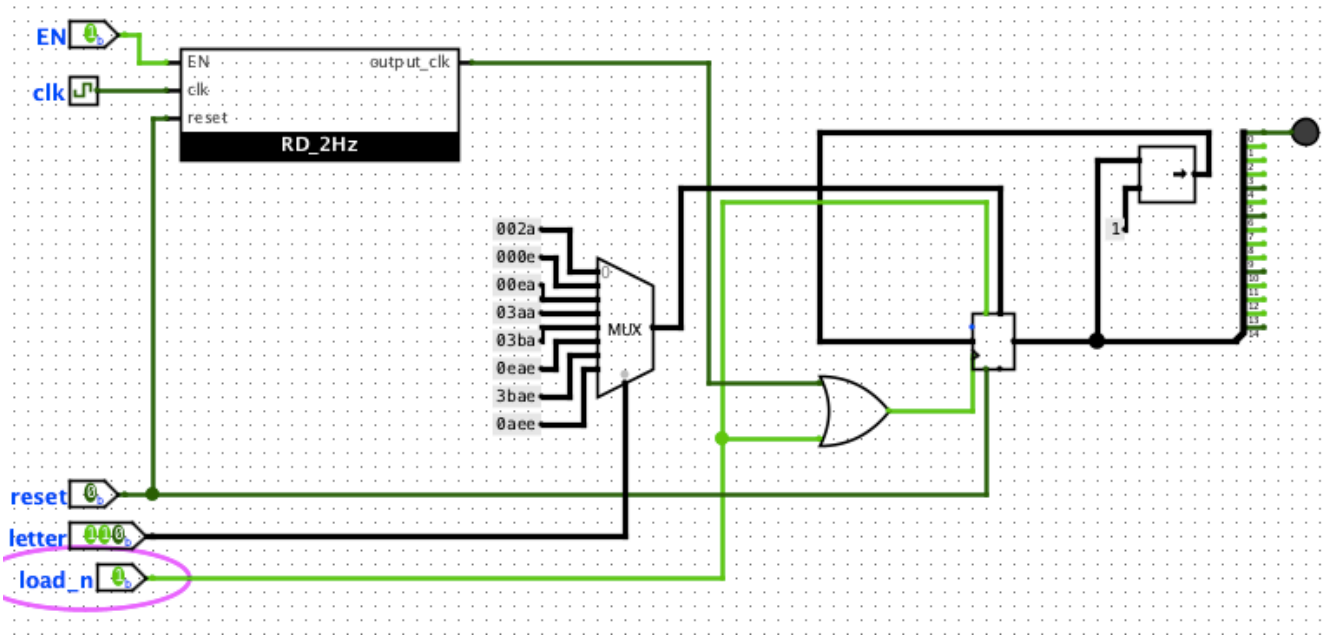
Letter	Pattern Representation (sequence length is 14-bits)	Select bit
S	00000000101010	000
T	00000000001110	001
U	00000010101110	010
V	00001010101110	011
W	00001011101110	100
X	00111010101110	101
Y	11101011101110	110
Z	00111011101010	111

2.



*Revision: I flip the pattern (14-bits) because Im using a shift right register, and I need the first number shifting out to correspond to the first number to the letter's pattern representation. I also change my sequence length to 15-bits long to have the last bit of flipped representation to be 0.

4. Letter Y:



Letter Z: