
STM32
CubeMX

1. Description

1.1. Project

Project Name	MicDelta
Board Name	controller
Generated with:	STM32CubeMX 6.4.0
Date	02/20/2022

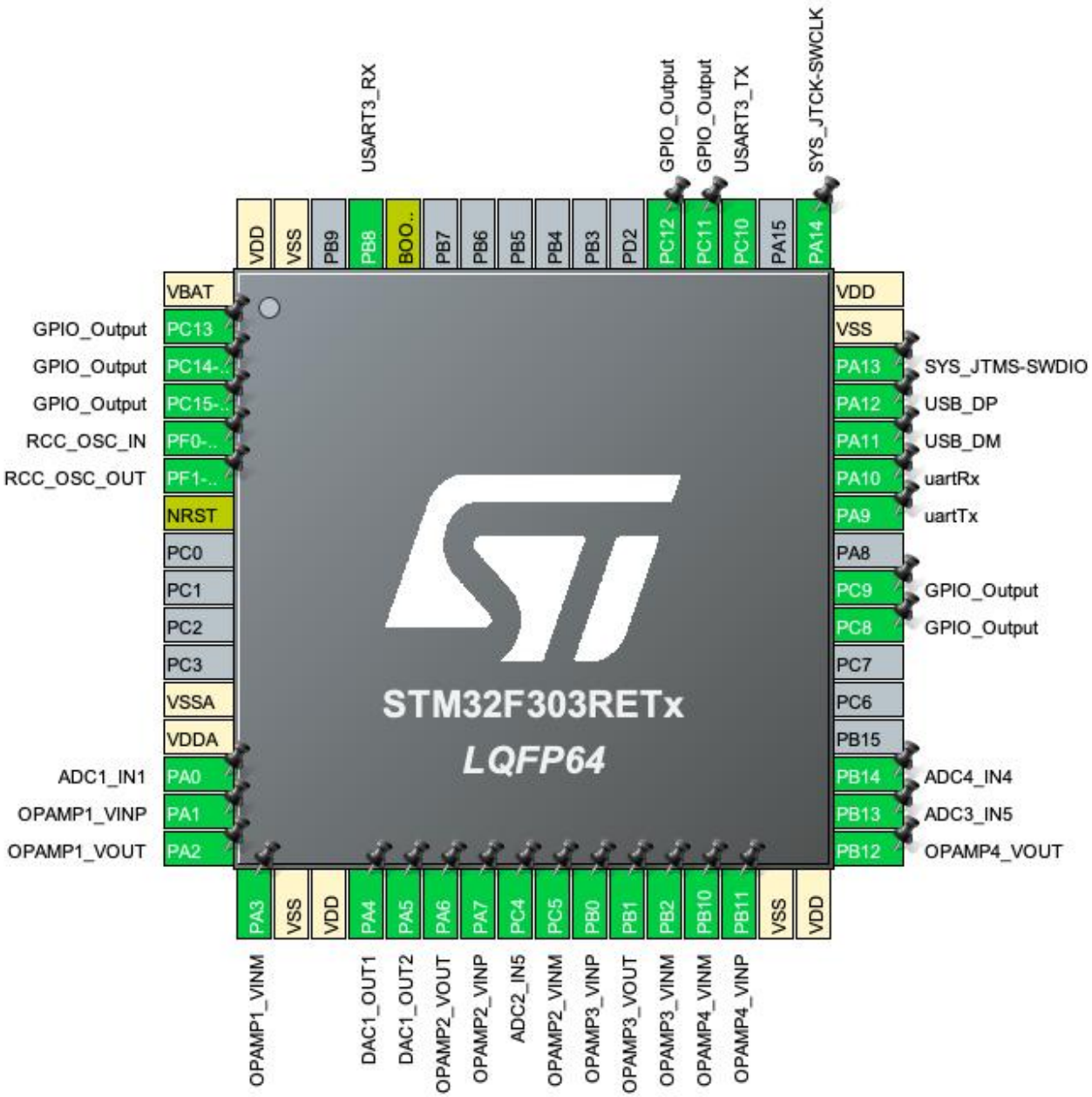
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



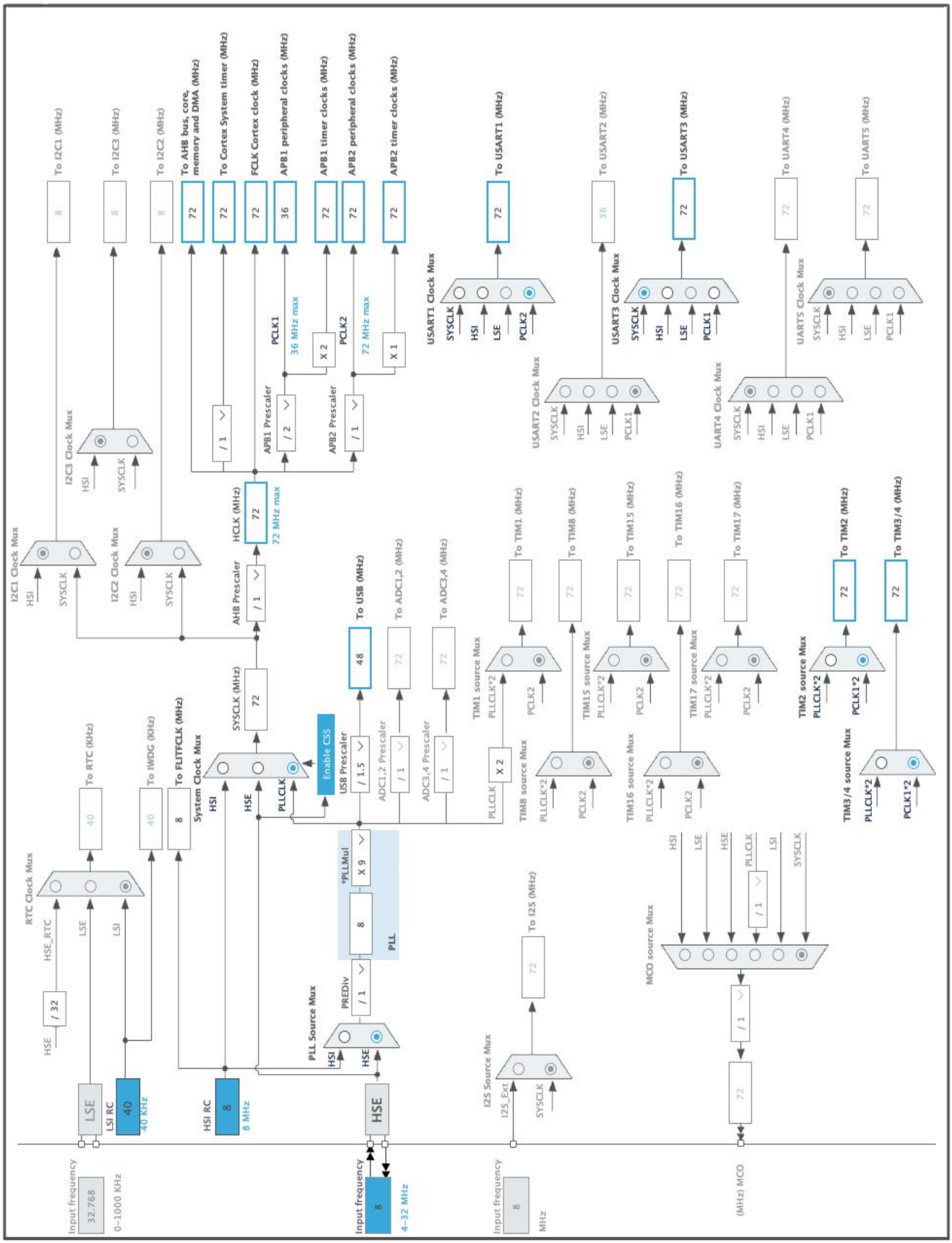
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	
3	PC14-OSC32_IN *	I/O	GPIO_Output	
4	PC15-OSC32_OUT *	I/O	GPIO_Output	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0	I/O	ADC1_IN1	
15	PA1	I/O	OPAMP1_VINP	
16	PA2	I/O	OPAMP1_VOUT	
17	PA3	I/O	OPAMP1_VINM	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	DAC1_OUT1	
21	PA5	I/O	DAC1_OUT2	
22	PA6	I/O	OPAMP2_VOUT	
23	PA7	I/O	OPAMP2_VINP	
24	PC4	I/O	ADC2_IN5	
25	PC5	I/O	OPAMP2_VINM	
26	PB0	I/O	OPAMP3_VINP	
27	PB1	I/O	OPAMP3_VOUT	
28	PB2	I/O	OPAMP3_VINM	
29	PB10	I/O	OPAMP4_VINM	
30	PB11	I/O	OPAMP4_VINP	
31	VSS	Power		
32	VDD	Power		
33	PB12	I/O	OPAMP4_VOUT	
34	PB13	I/O	ADC3_IN5	
35	PB14	I/O	ADC4_IN4	
39	PC8 *	I/O	GPIO_Output	
40	PC9 *	I/O	GPIO_Output	
42	PA9	I/O	USART1_TX	uartTx
43	PA10	I/O	USART1_RX	uartRx
44	PA11	I/O	USB_DM	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
45	PA12	I/O	USB_DP	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
51	PC10	I/O	USART3_TX	
52	PC11 *	I/O	GPIO_Output	
53	PC12 *	I/O	GPIO_Output	
60	BOOT0	Boot		
61	PB8	I/O	USART3_RX	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MicDelta
Project Folder	/Users/benh/STM32CubeIDE/workspace_1.1.0/MicDelta
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.3
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x800

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_OPAMP2_Init	OPAMP2
5	MX_ADC2_Init	ADC2
6	MX_TIM3_Init	TIM3
7	MX_OPAMP4_Init	OPAMP4
8	MX_ADC4_Init	ADC4
9	MX_DAC1_Init	DAC1
10	MX_OPAMP3_Init	OPAMP3
11	MX_ADC1_Init	ADC1

Rank	Function Name	Peripheral Instance Name
12	MX_ADC3_Init	ADC3
13	MX_USART1_UART_Init	USART1
14	MX_TIM2_Init	TIM2
15	MX_USB_DEVICE_Init	USB_DEVICE
16	MX_TIM4_Init	TIM4
17	MX_OPAMP1_Init	OPAMP1
18	MX_USART3_UART_Init	USART3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303RETx
Datasheet	DS10362_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

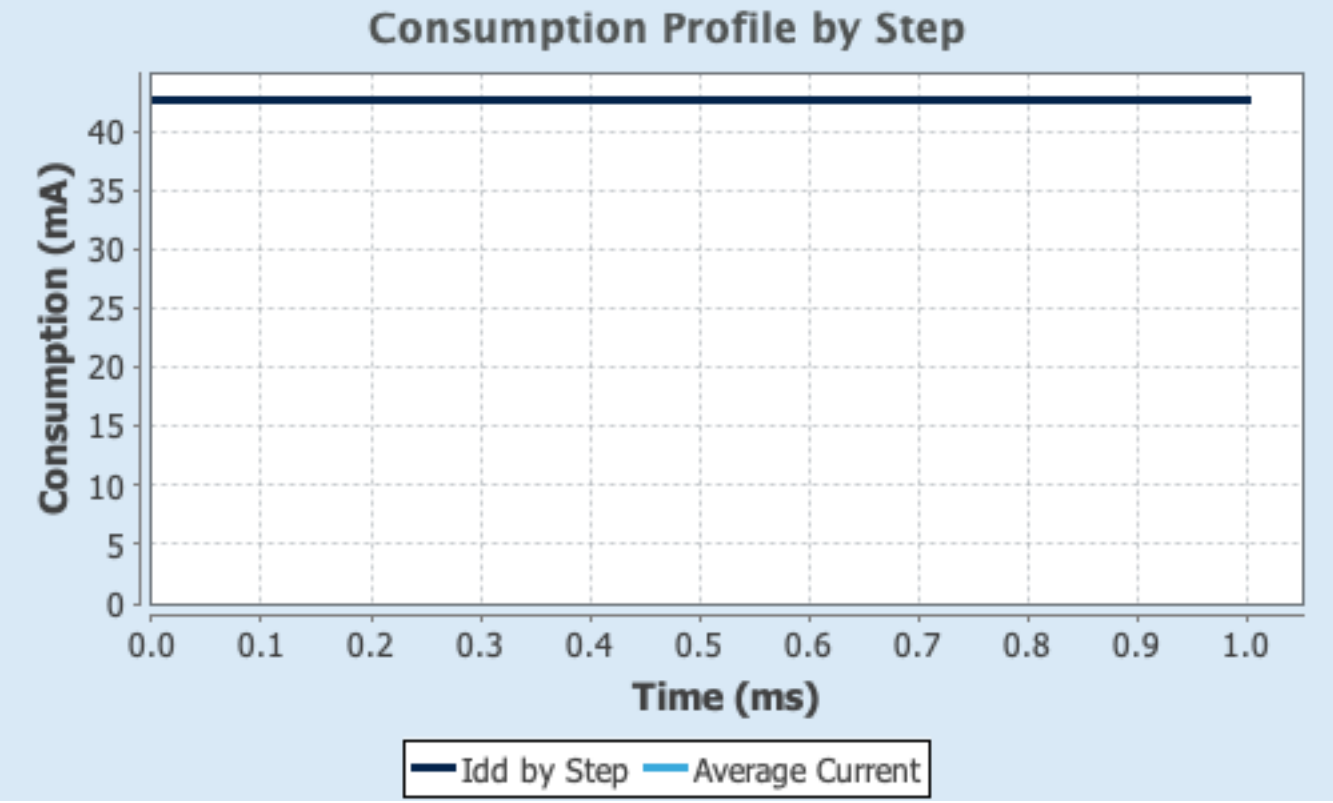
6.4. Sequence

Step	Step1
Mode	RUN
Vdd	3.6
Voltage Source	Vbus
Range	No Scale
Fetch Type	FLASH
CPU Frequency	72 MHz
Clock Configuration	HSE PLL
Clock Source Frequency	8 MHz
Peripherals	ADC1:Single-ended_5MSPS ADC2:Single-ended_5MSPS ADC3:Single-ended_5MSPS ADC4:Single-ended_5MSPS APB1-Bridge APB2-Bridge Bus-Matrix DAC:OUT1+OUT2-Worst_code DMA1 DMA2 GPIOA GPIOB GPIOC GPIOD TIM2 TIM3 TIM4 TIM6 USB
Additional Cons.	0 mA
Average Current	42.69 mA
Duration	1 ms
DMIPS	63.0
Ta Max	97.93
Category	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	42.69 mA
Battery Life	0	Average DMIPS	63.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
40
35
30
25
20
15
10
5
0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN3: OPAMP1 Output Single-Ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 1 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
SequencerNbRanks	1
Rank	1
Channel	**Channel 3 ***
Sampling Time	61.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	**true ***
Watchdog Mode	Single regular channel
Analog WatchDog Channel	**Channel 3 ***
High Threshold	**2500 ***
Low Threshold	**1500 ***

Interrupt Mode	**Enabled ***

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

IN3: OPAMP2 Output Single-Ended

IN5: IN5 Single-ended

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 1 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
SequencerNbRanks	1
Rank	1
Channel	Channel 3
Sampling Time	61.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	**true ***
Watchdog Mode	Single regular channel
Analog WatchDog Channel	Channel 3
High Threshold	**2500 ***
Low Threshold	**1500 ***
Interrupt Mode	**Enabled ***

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC3

IN1: OPAMP3 Output Single-ended

mode: IN5

7.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 1 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
SequencerNbRanks	1
Rank	1
Channel	Channel 1

Sampling Time	61.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	**true ***
Watchdog Mode	Single regular channel
Analog WatchDog Channel	Channel 1
High Threshold	**2500 ***
Low Threshold	**1500 ***
Interrupt Mode	**Enabled ***

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. ADC4

IN3: OPAMP4 Output Single-Ended

IN4: IN4 Single-ended

7.4.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 1 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable

Number Of Conversion	1
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
SequencerNbRanks	1
Rank	1
Channel	Channel 3
Sampling Time	61.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	**true ***
Watchdog Mode	Single regular channel
Analog WatchDog Channel	Channel 3
High Threshold	**2500 ***
Low Threshold	**1500 ***
Interrupt Mode	**Enabled ***

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.5. DAC1

mode: OUT1 Configuration

mode: OUT2 Configuration

7.5.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

7.6. OPAMP1

Mode: PGA Connected

7.6.1. Parameter Settings:

Basic Parameters:

PGA Gain	**16 ***
User Trimming	Disable

7.7. OPAMP2

Mode: PGA Connected

7.7.1. Parameter Settings:

Basic Parameters:

PGA Gain	**16 ***
User Trimming	Disable

7.8. OPAMP3

Mode: PGA Connected

7.8.1. Parameter Settings:

Basic Parameters:

PGA Gain	**16 ***
User Trimming	Disable

7.9. OPAMP4

Mode: PGA Connected

7.9.1. Parameter Settings:

Basic Parameters:

PGA Gain	**16 ***
User Trimming	Disable

7.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.10.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.11. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.12. TIM2

Clock Source : Internal Clock

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**71 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0xffffffff
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.13. TIM3

Clock Source : Internal Clock

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**719 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.14. TIM4

Clock Source : Internal Clock

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**28 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.15. USART1

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. USART3

Mode: Asynchronous

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	**4000000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	**Transmit Only ***
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	**Enable ***
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.17. USB

mode: Device (FS)

7.17.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy

Power Parameters:

Low Power	Disabled
Link Power Management	Disabled

7.18. ARM.CMSIS.5.6.0

mode: CMSISJjDSP

7.19. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.19.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USB CDC Rx Buffer Size	1000
USB CDC Tx Buffer Size	1000

7.19.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC4	ADC2_IN5	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PB13	ADC3_IN5	Analog mode	No pull-up and no pull-down	n/a	
ADC4	PB14	ADC4_IN4	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
OPAMP1	PA1	OPAMP1_VINP	Analog mode	No pull-up and no pull-down	n/a	
	PA2	OPAMP1_VOUT	Analog mode	No pull-up and no pull-down	n/a	
	PA3	OPAMP1_VINM	Analog mode	No pull-up and no pull-down	n/a	
OPAMP2	PA6	OPAMP2_VOUT	Analog mode	No pull-up and no pull-down	n/a	
	PA7	OPAMP2_VINP	Analog mode	No pull-up and no pull-down	n/a	
	PC5	OPAMP2_VINM	Analog mode	No pull-up and no pull-down	n/a	
OPAMP3	PB0	OPAMP3_VINP	Analog mode	No pull-up and no pull-down	n/a	
	PB1	OPAMP3_VOUT	Analog mode	No pull-up and no pull-down	n/a	
	PB2	OPAMP3_VINM	Analog mode	No pull-up and no pull-down	n/a	
OPAMP4	PB10	OPAMP4_VINM	Analog mode	No pull-up and no pull-down	n/a	
	PB11	OPAMP4_VINP	Analog mode	No pull-up and no pull-down	n/a	
	PB12	OPAMP4_VOUT	Analog mode	No pull-up and no pull-down	n/a	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	uartTx
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	uartRx
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	
	PB8	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
MEMTOMEM	DMA1_Channel3	Memory To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
ADC4	DMA2_Channel2	Peripheral To Memory	**Medium ***
ADC3	DMA2_Channel5	Peripheral To Memory	**Medium ***
ADC2	DMA2_Channel1	Peripheral To Memory	**Medium ***
TIM4_UP	DMA1_Channel7	Memory To Peripheral	**Very High ***
ADC1	DMA1_Channel1	Peripheral To Memory	**Medium ***
USART3_TX	DMA1_Channel2	Memory To Peripheral	**High ***

MEMTOMEM: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Src Memory Increment:	**Enable ***
Dst Memormy Increment:	**Enable ***
Src Memory Data Width:	Byte
Dst Memormy Data Width:	Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC4: DMA2_Channel2 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC3: DMA2_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA2_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

TIM4_UP: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Byte ***
Memory Data Width:	**Byte ***

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word

Memory Data Width:	Half Word

USART3_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
ADC1 and ADC2 interrupts	true	0	0
USB low priority or CAN_RX0 interrupts	true	0	0
TIM2 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	0	0
ADC3 global interrupt	true	0	0
DMA2 channel1 global interrupt	true	0	0
DMA2 channel2 global interrupt	true	0	0
DMA2 channel5 global interrupt	true	0	0
ADC4 interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
DMA1 channel3 global interrupt	unused		
USB high priority or CAN_TX interrupts	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	unused		
TIM6 global interrupt and DAC1 underrun interrupt	unused		
USB high priority interrupt remap	unused		
USB low priority interrupt remap	unused		
Floating point unit interrupt	unused		

8.3.2. NVIC Code generation

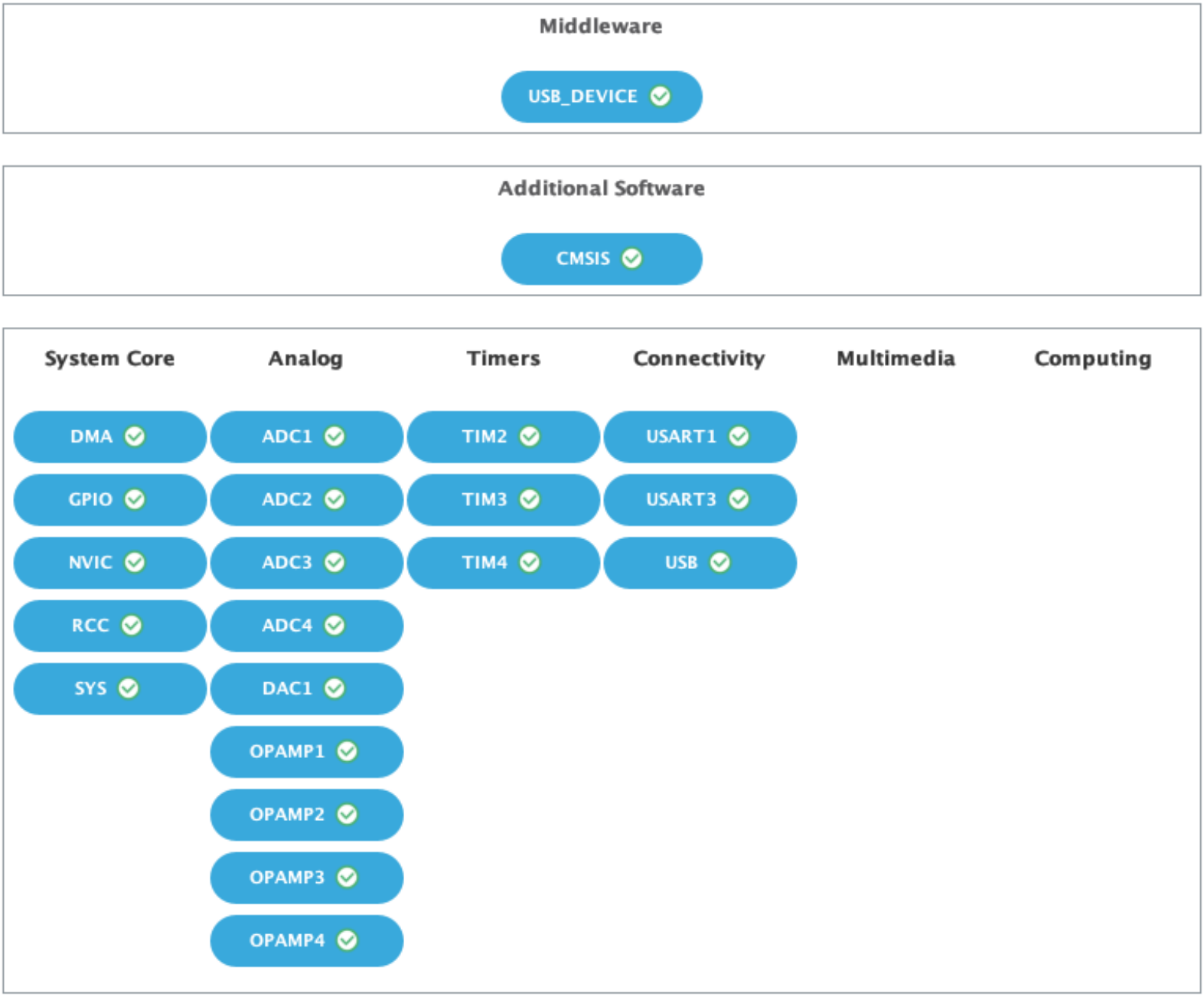
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
DMA1 channel7 global interrupt	false	true	true
ADC1 and ADC2 interrupts	false	true	true
USB low priority or CAN_RX0 interrupts	false	true	true
TIM2 global interrupt	false	true	true
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	false	true	true
ADC3 global interrupt	false	true	true
DMA2 channel1 global interrupt	false	true	true
DMA2 channel2 global interrupt	false	true	true
DMA2 channel5 global interrupt	false	true	true
ADC4 interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
ARM	CMSIS	5.6.0	Class : CMSIS Group : DSP Variant : Library Version : 1.7.0

11. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00118585.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00043574.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00118589.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00047998.pdf
Application note	http://www.st.com/resource/en/application_note/DM00053084.pdf
Application note	http://www.st.com/resource/en/application_note/DM00070391.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00074240.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00083249.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129600.pdf
Application note	http://www.st.com/resource/en/application_note/DM00157785.pdf

Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00210617.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00260340.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269146.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442720.pdf
Application note	http://www.st.com/resource/en/application_note/DM00445657.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf