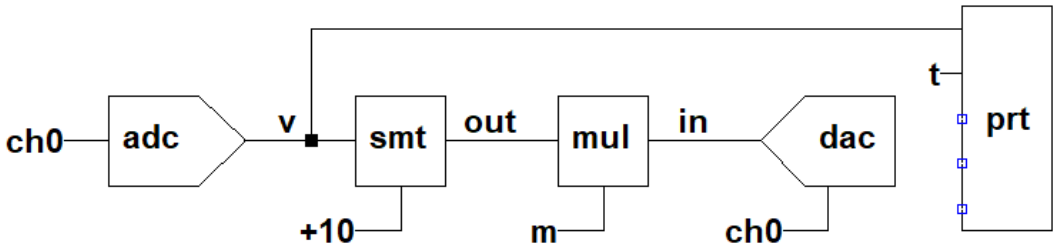
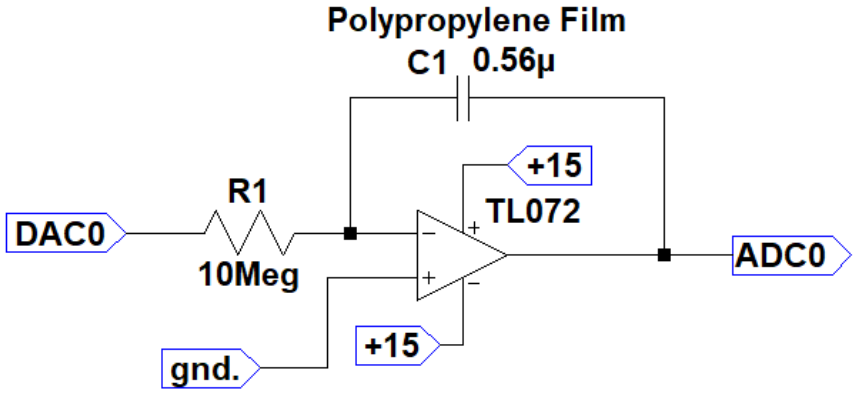
Testing the ADC Linearity

The RP2040 data sheet specifies the ADC as 12-bits with and effective number of bits = 9. Measuring the ADC linearity requires a measurement system that is better than the one we are testing. It is possible to make a very linear voltage ramp by using an integrator. The ramp resolution is very good but it is not possible to know the exact voltage (with our test setup).

For an integrator with a constant input, the output = Vin * gain * t. Only time t is needed to generate a linear equation (y = mx+b) of the voltage ramp. A second linear equation is generated from the end points of the ADC readings. The voltage ramp is normalized to the ADC end points. Finally, the difference between the integrator ramp and the ADC readings is used to calculate a linearity error for the ADC.

An external op amp integrator is required to generate the test voltage. The voltage ramp is created by applying a constant DAC voltage to the input. The ±15V supply from the Pico Block board can be used as the op amp power source. It is important to use a polypropylene capacitor. It has a low dielectric absorption which is a needed characteristic for the integrator.

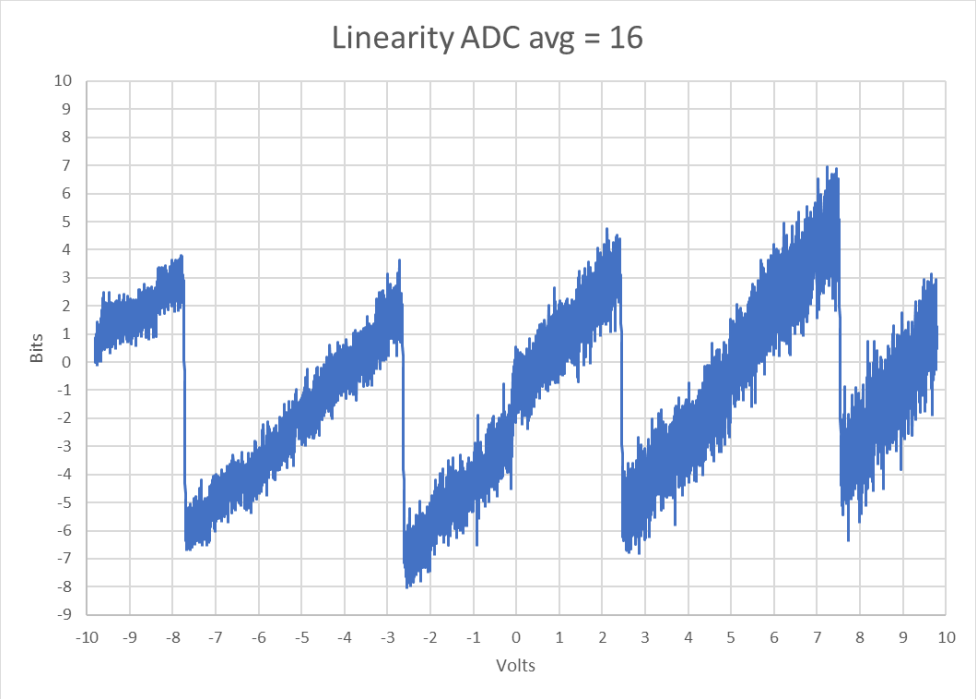




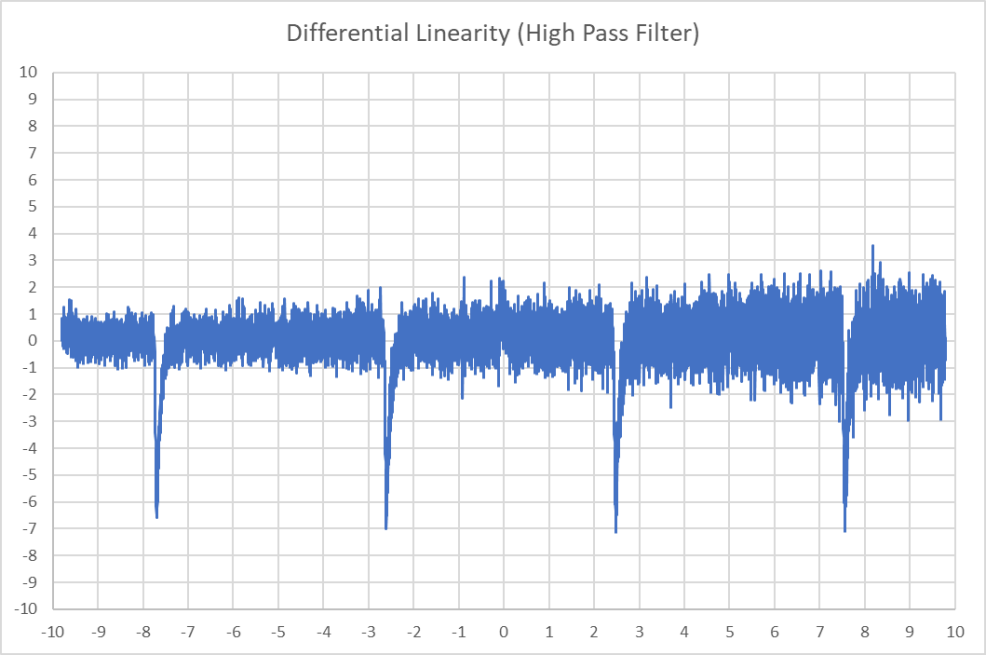
The block program sets the Schmidt trigger threshold to just under 10V. This ensures the returned ADC voltage will exceed the trigger point. The op amp integrator gain is 1/5.6 sec = 0.179/s. With 2.5V applied to the input, it changes 0.44V every second. Ramping -9.8 to +9.8V takes about 44 seconds.

The program generates a repetitive triangular waveform. The data we need is from approximately -9.8V ramping to +9.8V. The text data can be captured to a file in simpleCRT and exported to a spreadsheet for analysis.

```
clr
adc ch0 v
smt v +10 out
mul out m in
dac in ch0
prt v t
end
set dt .004
set out -1
set max 100
set +10 9.8
set avg 16
set m -2.5
```



The linearity test shows large jumps at the 000111111111_2 to 001000000000_2 transitions. The jumps are just around 8-LSBs. This verifies the specified effective number of bits at around 9.



A pseudo differential linearity can be generated by passing the linearity data through a high pass filter. The progressive widening of the local bit transitions is due to increases noise. The larger ADC values do not divide the reference noise as much as the smaller values near zero (-10V is zero).

Here is a recipe for calculating linearity from the captured data:

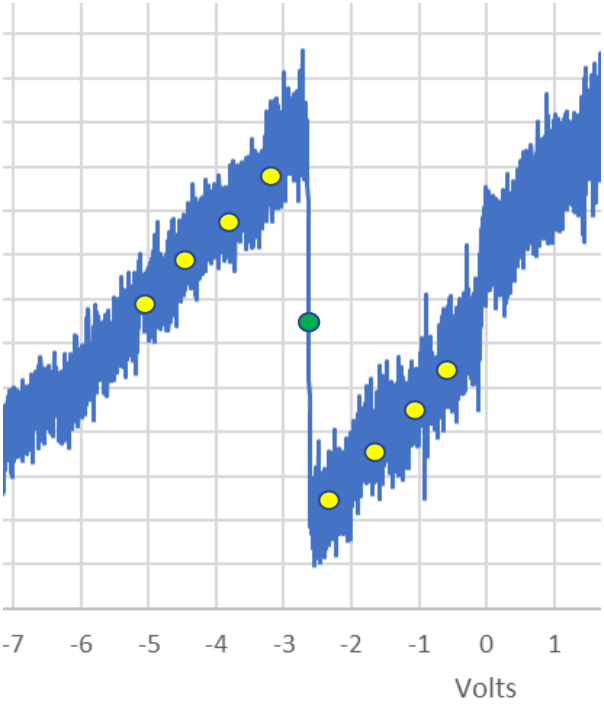
- Run the block program
- Wait for the voltage to go to +9.8 then down to -9V
    - simpleCRT Capture File (data.txt)
- Wait for the voltage to go to +9.8 then down to +9
    - simpleCRT Capture Close
- Use a text editor
    - Remove top data ~-9 to min ~-9.8
    - Remove end data max ~+9.8 to ~9
    - Save file
- Spreadsheet
    - Import data.txt file into columns A and B
    - Cell C1 set cell name = gain, value = (last A – A1)(last B – B1), last = last column value
    - Cell D1 set cell name = os, value = B1
    - Cell D2 set cell name = start, set value = A1
    - Set value E1 = (B1 -os)*gain+start (this is the linear fit end to end)
        - Copy E1 and paste in E2 to last E
    - Set value F1 = A1-E1 (this is the linear error in volts)
        - Copy F1 and paste in F2 to last F
    - Set value G1 = F1/0.0048828 (convert volts to bits)
    - Select column A and column G then scatter plot to show linearity error
    - To find the differential error, use a high pass filter on column G
        - Set H1 = 0
        - H2 = 0.99*G2-0.99*G1+0.98*H1
        - Copy H2 and paste in H3 through last H
    - Select column A and column H then scatter plot to show differential error

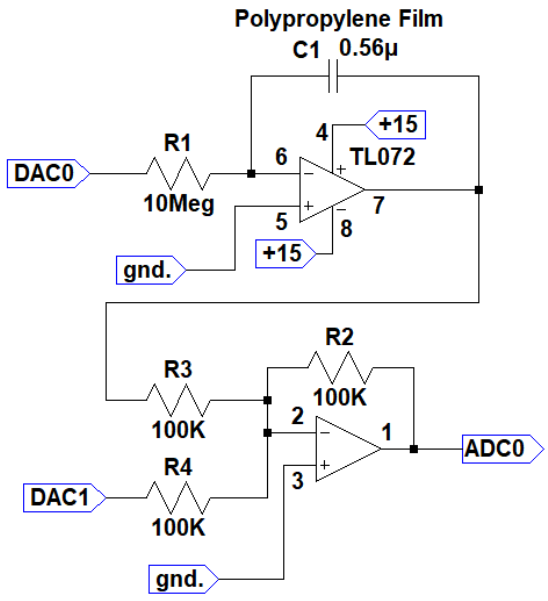
The linearity error is about ±20mV over a range of 20V. It is a relatively small error of ±0.1% of full scale but the ADC is not monotonic to 12-bits. When the input voltage changes around -2.5V, it needs to move 40mV not 5mV before the ADC increments one digit. Unlike gain and offset error from the resistors, this type of error can't be corrected with a simple addition and multiplication.

The ADC has much better performance around the zero voltage crossing. This is good since small signals will not be distorted much.

We will look at a dither technique to improve the monotonic performance and the linearity. Keep in mind, this method adds complexity. It may be simpler to just add an external 12-bit or 14-bit SPI bus ADC (and DAC if you want more DAC bits).

By adding a voltage to the input we can move the input to a region where the ADC has no large gaps between values. The problem target area (green dot) can be moved above or below (yellow dots). If several readings in these areas are averaged, then it is possible to reduce the gap to a smaller value.



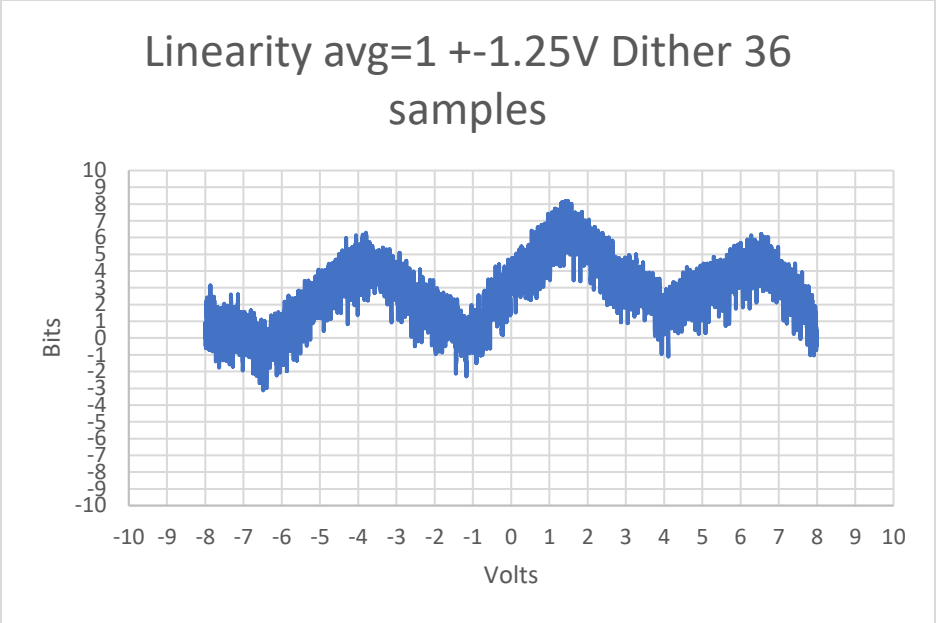


With the addition of a summing amplifier, DAC1 can be used to add an offset to the integrator ramp voltage. The output will be inverted and the program must correct for the negation. Also, the DAC output has a slow response. So only small steps must be used and a delay added before the ADC read.

The resulting ADC input with a triangular dither added. The dither signal takes about 2ms and this will limit our sample rate to about 500Hz maximum.

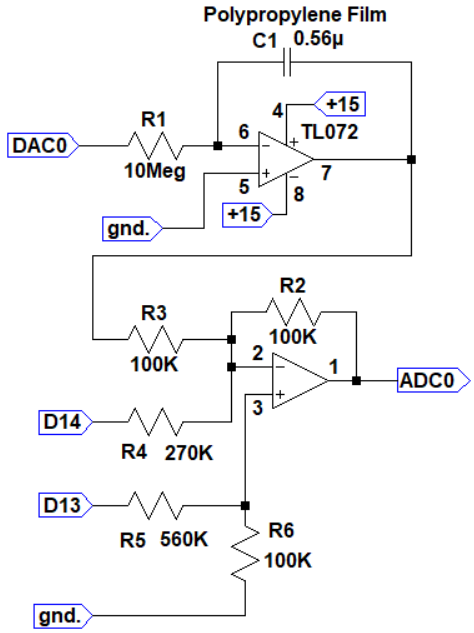
```
clr
rst 0 p
rst 0 vs
rst 8 cnt
dac p ch1
adc ch0 v
adc ch0 v
sum p dp p
sum v vs vs
sub cnt 1 cnt
brp cnt -6
rst 17 cnt
dac p ch1
adc ch0 v
adc ch0 v
sub p dp p
sum v vs vs
sub cnt 1 cnt
brp cnt -6
rst 9 cnt
dac p ch1
adc ch0 v
adc ch0 v
sum p dp p
sum v vs vs
```

```
sub cnt 1 cnt
brp cnt -6
div vs 36 vs
smt vs 8 out
mul out m in
dac in ch0
prt vs t
end
set dt .004
set out 1
set max 1000
set 8 8
set m -2.5
set avg 1
set ch1 1
set p 2.0
set dp 0.156
set .3 .33
set -6 -6
set 9 9
set 8 8
set 17 17
set 1 1
set 36 -36
```

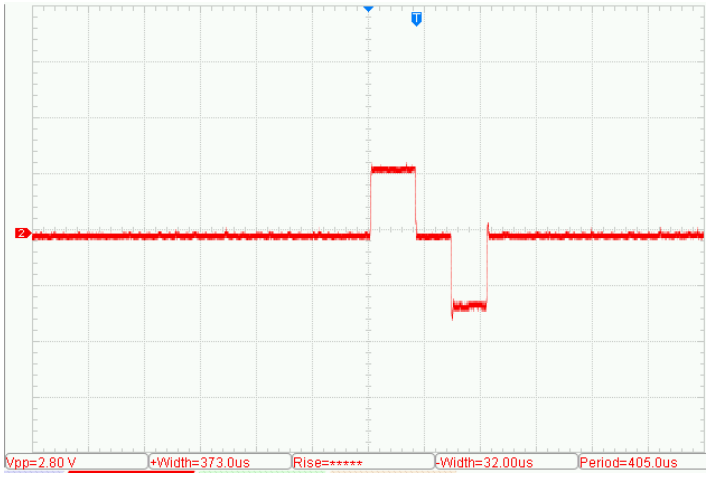


The dithered measurement shows there are no large jumps or discontinuities in the codes. The linearity error is reduced by about half. The sweep was reduced to ±8V. The dither signal reduces the input range by about 1.25V on each end.

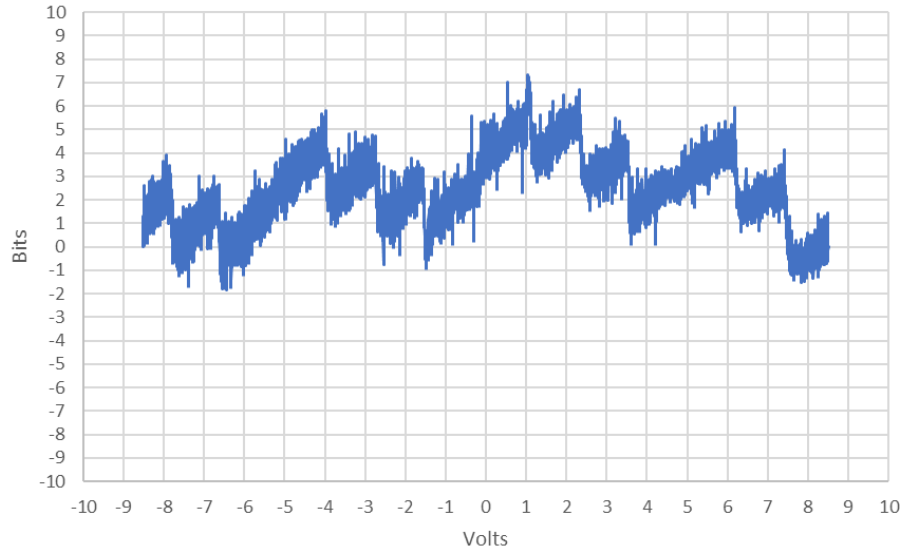
The use of a DAC for the dither voltage can be eliminated by making a two bit DAC with resistors and digital outputs. The digital outputs have a faster response but there will be only three output voltage combinations. The levels are adjustable with R4 and R5.



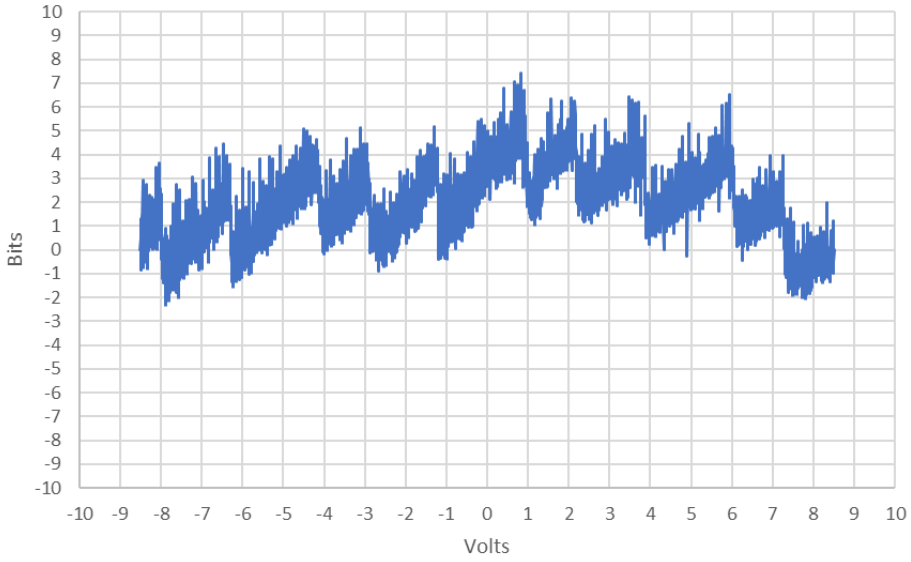
```
clr
out 1 D13
adc ch0 v3
out 0 D13
adc ch0 v1
out 1 D14
adc ch0 v2
out 0 D14
sum v1 v2 vs
sum vs v3 vs
mul vs -33 vs
smt vs 8 out
mul out m in
dac in ch0
prt vs t
end
set dt .004
set out 1
set max 1000
set m -2.5
set 8 8.5
set avg 4
set 1 1
set -33 -.3333
set D14 14
set D13 13
```



A o'scope capture of a three-step dither signal. The three samples take about 120us.



Linearity using a ±1.25V three step dither.



Linearity using a ±1.6V three step dither.