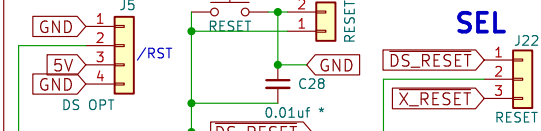


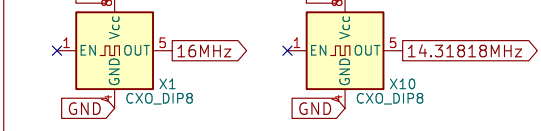
## RESET



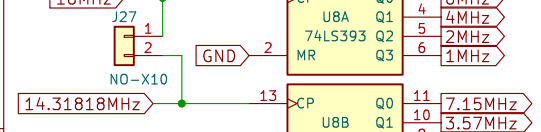
Install OS to proper pin!  
DS1813 pins 2,3 - Reset with Pushbutton  
DS1813 pins 1,2,3 - Reset - Install 0.01uF cap

## CLOCKS

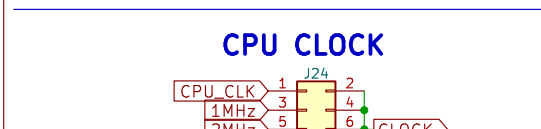
Half-Can Oscillator Half-Can Oscillator



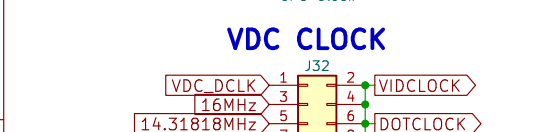
Pullup on 1 and 13



CPU CLOCK

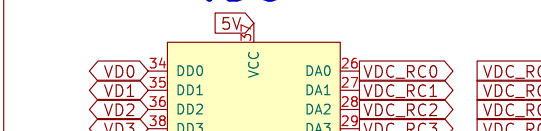


VDC CLOCK

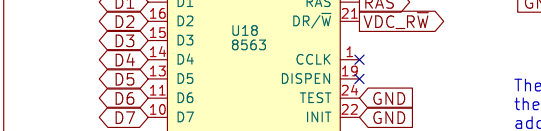


## VIDEO

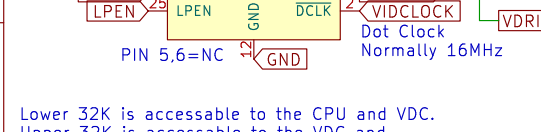
VDC LATCH



DPGRAM CPU SIDE



VDC SIDE



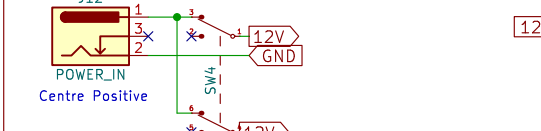
Lower 32K is accessible to the CPU and VDC.  
Upper 32K is accessible to the VDC and is used to store the system FONTS.  
FONT ROM is 64K holding 8 sets.

CONTROL LINES



## POWER

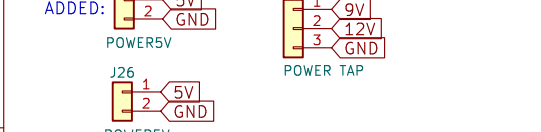
INPUT / SWITCH



VOLTAGE REG



POWER TAPS



LED



## DESCRIPTION

This is a development board for producing a working "SuperColourPET". It uses currently available chips where possible and PLCC footprints to keep the board small. It has a Programmable CPLD and it has lots of RAM and ROM and a VDC video system using a dual-port RAM that allows clocking the CPU and VIDEO systems independently. It includes CLCD IO for IEC. It has three processors for PET, SuperPET, and CP/M.

CHIP SELECTS

CS1: \$E81x - PIA  
CS2: \$E2x - VIA 1  
CS3: \$E84x - VIA 2  
CS4: \$E80x - VIA: IEC/Control  
CS5: \$E88x - VDC  
CS6: \$8000-AFFF - VID RAM (Dual Port)  
CS7: \$E890-EBAF - SID#1  
CS8: \$E880-EBCF - SID#2

ADDRESS SPACE

\* AD-A14 (32K SIZE) to DPGRAM  
\* AD-A11 (4K 51x) to all RAM/ROM/IO  
\* A12-A18 replaced by MA12-MA18 to RAM/ROM  
\* MMU translates MA lines to map in appropriate ranges

CPLD INFO

\* Reset to SYSTEM MENU  
\* Select 6502 and system ROM CODE bank  
\* Generates Chip Selects  
\* Control Register  
- 3 bits for CPU select  
- 3 bits for SPEED divisor (16/8/4/2/1)  
- 1 bit for SYSTEM ROM select  
\* Generate WAIT for slow devices  
\* Register for 8296 Mode at \$77FF

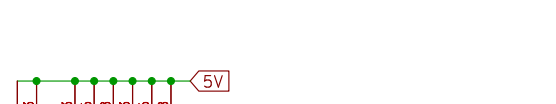
NOTES:

- uMMF Altera MAX CPLD  
- CPUs: 65C02, 63C09, Z84C0020  
- Video uses DPGRAM for 80 col or extended modes.  
- Character ROM size increased.  
- TTL Serial for Bluetooth/WiFi  
- Internal headers for ports  
- Firmware will need to be patched to support VDC.  
- Use an RGB output to a modern VGA/HDMI panel.

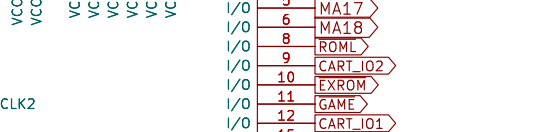
Started: 2023-01-12  
Updated: 2023-02-20

Work in Progress!!!

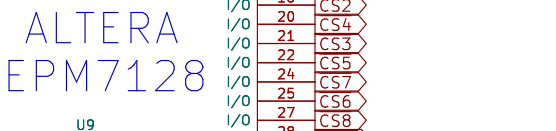
## CPLD



EXTENDED ADDRESS lines to MEMORY.

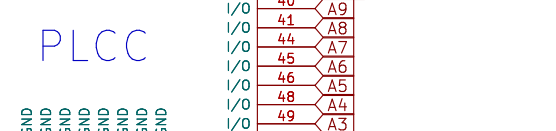


CORE chip selects



DATA lines are used to set MMU registers.  
DATA lines are INPUT only to the CPLD.

ADDRESS lines (A7-A15) are used to generate EXTENDED ADDRESS (MA10-MA19) lines to MEMORY and I/O.



Lines that don't fit... bo.

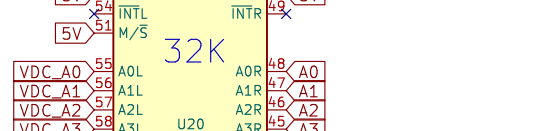


VIDEO

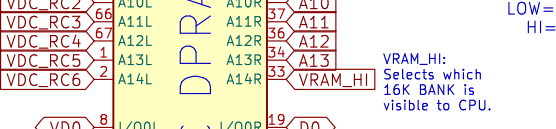
VDC



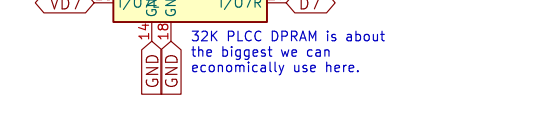
LATCH



DPGRAM CPU SIDE



VDC SIDE



Lower 32K is accessible to the CPU and VDC.  
Upper 32K is accessible to the VDC and is used to store the system FONTS.  
FONT ROM is 64K holding 8 sets.

CONTROL LINES



POWER

INPUT / SWITCH



VOLTAGE REG



POWER TAPS



LED



DESCRIPTION

This is a development board for producing a working "SuperColourPET". It uses currently available chips where possible and PLCC footprints to keep the board small. It has a Programmable CPLD and it has lots of RAM and ROM and a VDC video system using a dual-port RAM that allows clocking the CPU and VIDEO systems independently. It includes CLCD IO for IEC. It has three processors for PET, SuperPET, and CP/M.

CHIP SELECTS

CS1: \$E81x - PIA  
CS2: \$E2x - VIA 1  
CS3: \$E84x - VIA 2  
CS4: \$E80x - VIA: IEC/Control  
CS5: \$E88x - VDC  
CS6: \$8000-AFFF - VID RAM (Dual Port)  
CS7: \$E890-EBAF - SID#1  
CS8: \$E880-EBCF - SID#2

ADDRESS SPACE

\* AD-A14 (32K SIZE) to DPGRAM  
\* AD-A11 (4K 51x) to all RAM/ROM/IO  
\* A12-A18 replaced by MA12-MA18 to RAM/ROM  
\* MMU translates MA lines to map in appropriate ranges

CPLD INFO

\* Reset to SYSTEM MENU  
\* Select 6502 and system ROM CODE bank  
\* Generates Chip Selects  
\* Control Register  
- 3 bits for CPU select  
- 3 bits for SPEED divisor (16/8/4/2/1)  
- 1 bit for SYSTEM ROM select  
\* Generate WAIT for slow devices  
\* Register for 8296 Mode at \$77FF

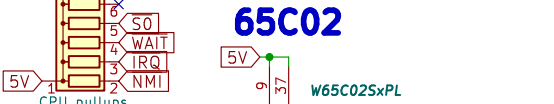
NOTES:

- uMMF Altera MAX CPLD  
- CPUs: 65C02, 63C09, Z84C0020  
- Video uses DPGRAM for 80 col or extended modes.  
- Character ROM size increased.  
- TTL Serial for Bluetooth/WiFi  
- Internal headers for ports  
- Firmware will need to be patched to support VDC.  
- Use an RGB output to a modern VGA/HDMI panel.

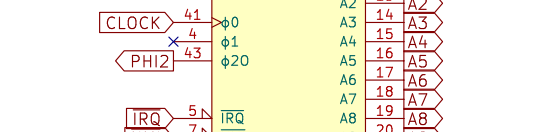
Started: 2023-01-12  
Updated: 2023-02-20

Work in Progress!!!

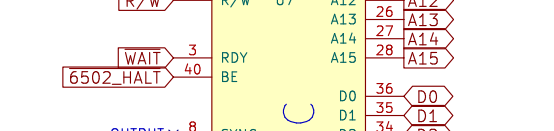
## CPLD



EXTENDED ADDRESS lines to MEMORY.

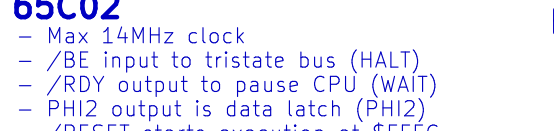


CORE chip selects



DATA lines are used to set MMU registers.  
DATA lines are INPUT only to the CPLD.

ADDRESS lines (A7-A15) are used to generate EXTENDED ADDRESS (MA10-MA19) lines to MEMORY and I/O.



Lines that don't fit... bo.



VIDEO

VDC



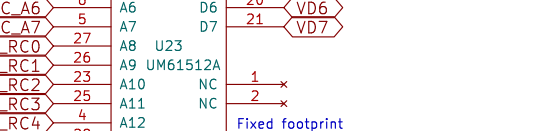
LATCH



DPGRAM CPU SIDE



VDC SIDE



Lower 32K is accessible to the CPU and VDC.  
Upper 32K is accessible to the VDC and is used to store the system FONTS.  
FONT ROM is 64K holding 8 sets.

CONTROL LINES



POWER

INPUT / SWITCH



VOLTAGE REG



POWER TAPS



LED



DESCRIPTION

This is a development board for producing a working "SuperColourPET". It uses currently available chips where possible and PLCC footprints to keep the board small. It has a Programmable CPLD and it has lots of RAM and ROM and a VDC video system using a dual-port RAM that allows clocking the CPU and VIDEO systems independently. It includes CLCD IO for IEC. It has three processors for PET, SuperPET, and CP/M.

CHIP SELECTS

CS1: \$E81x - PIA  
CS2: \$E2x - VIA 1  
CS3: \$E84x - VIA 2  
CS4: \$E80x - VIA: IEC/Control  
CS5: \$E88x - VDC  
CS6: \$8000-AFFF - VID RAM (Dual Port)  
CS7: \$E890-EBAF - SID#1  
CS8: \$E880-EBCF - SID#2

ADDRESS SPACE

\* AD-A14 (32K SIZE) to DPGRAM  
\* AD-A11 (4K 51x) to all RAM/ROM/IO  
\* A12-A18 replaced by MA12-MA18 to RAM/ROM  
\* MMU translates MA lines to map in appropriate ranges

CPLD INFO

\* Reset to SYSTEM MENU  
\* Select 6502 and system ROM CODE bank  
\* Generates Chip Selects  
\* Control Register  
- 3 bits for CPU select  
- 3 bits for SPEED divisor (16/8/4/2/1)  
- 1 bit for SYSTEM ROM select  
\* Generate WAIT for slow devices  
\* Register for 8296 Mode at \$77FF

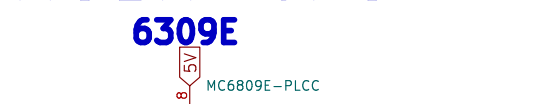
NOTES:

- uMMF Altera MAX CPLD  
- CPUs: 65C02, 63C09, Z84C0020  
- Video uses DPGRAM for 80 col or extended modes.  
- Character ROM size increased.  
- TTL Serial for Bluetooth/WiFi  
- Internal headers for ports  
- Firmware will need to be patched to support VDC.  
- Use an RGB output to a modern VGA/HDMI panel.

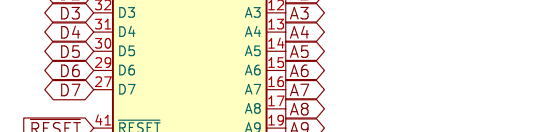
Started: 2023-01-12  
Updated: 2023-02-20

Work in Progress!!!

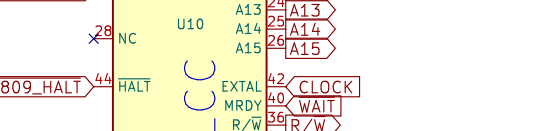
## MAIN MEMORY



EXTENDED ADDRESS lines to MEMORY.

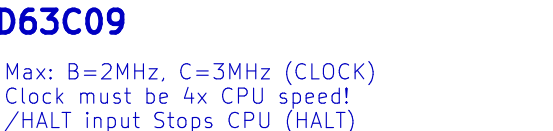


CORE chip selects

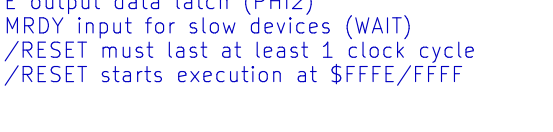


DATA lines are used to set MMU registers.  
DATA lines are INPUT only to the CPLD.

ADDRESS lines (A7-A15) are used to generate EXTENDED ADDRESS (MA10-MA19) lines to MEMORY and I/O.



Lines that don't fit... bo.



VIDEO

VDC



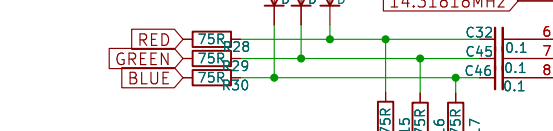
LATCH



DPGRAM CPU SIDE



VDC SIDE



Lower 32K is accessible to the CPU and VDC.  
Upper 32K is accessible to the VDC and is used to store the system FONTS.  
FONT ROM is 64K holding 8 sets.

CONTROL LINES



POWER

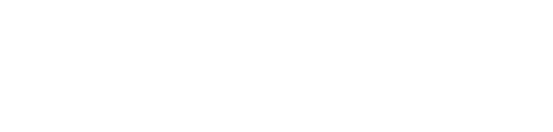
INPUT / SWITCH



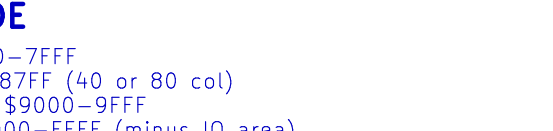
VOLTAGE REG



POWER TAPS



LED



DESCRIPTION

This is a development board for producing a working "SuperColourPET". It uses currently available chips where possible and PLCC footprints to keep the board small. It has a Programmable CPLD and it has lots of RAM and ROM and a VDC video system using a dual-port RAM that allows clocking the CPU and VIDEO systems independently. It includes CLCD IO for IEC. It has three processors for PET, SuperPET, and CP/M.

CHIP SELECTS

CS1: \$E81x - PIA  
CS2: \$E2x - VIA 1  
CS3: \$E84x - VIA 2  
CS4: \$E80x - VIA: IEC/Control  
CS5: \$E88x - VDC  
CS6: \$8000-AFFF - VID RAM (Dual Port)  
CS7: \$E890-EBAF - SID#1  
CS8: \$E880-EBCF - SID#2

ADDRESS SPACE

\* AD-A14 (32K SIZE) to DPGRAM  
\* AD-A11 (4K 51x) to all RAM/ROM/IO  
\* A12-A18 replaced by MA12-MA18 to RAM/ROM  
\* MMU translates MA lines to map in appropriate ranges

CPLD INFO

\* Reset to SYSTEM MENU  
\* Select 6502 and system ROM CODE bank  
\* Generates Chip Selects  
\* Control Register  
- 3 bits for CPU select  
- 3 bits for SPEED divisor (16/8/4/2/1)  
- 1 bit for SYSTEM ROM select  
\* Generate WAIT for slow devices  
\* Register for 8296 Mode at \$77FF

NOTES:

- uMMF Altera MAX CPLD  
- CPUs: 65C02, 63C09, Z84C0020  
- Video uses DPGRAM for 80 col or extended modes.  
- Character ROM size increased.  
- TTL Serial for Bluetooth/WiFi  
- Internal headers for ports  
- Firmware will need to be patched to support VDC.  
- Use an RGB output to a modern VGA/HDMI panel.

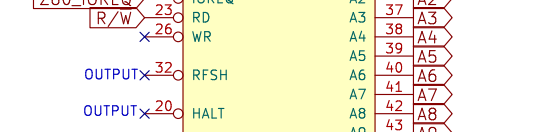
Started: 2023-01-12  
Updated: 2023-02-20

Work in Progress!!!

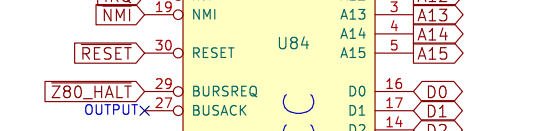
## MAIN MEMORY



EXTENDED ADDRESS lines to MEMORY.



CORE chip selects

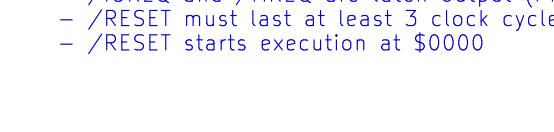


DATA lines are used to set MMU registers.  
DATA lines are INPUT only to the CPLD.

ADDRESS lines (A7-A15) are used to generate EXTENDED ADDRESS (MA10-MA19) lines to MEMORY and I/O.



Lines that don't fit... bo.



VIDEO

VDC



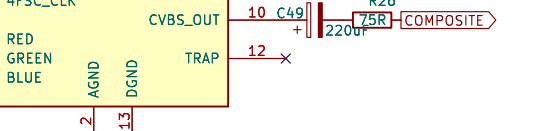
LATCH



DPGRAM CPU SIDE



VDC SIDE



Lower 32K is accessible to the CPU and VDC.  
Upper 32K is accessible to the VDC and is used to store the system FONTS.  
FONT ROM is 64K holding 8 sets.

CONTROL LINES



POWER

INPUT / SWITCH



VOLTAGE REG



POWER TAPS



LED



DESCRIPTION

This is a development board for producing a working "SuperColourPET". It uses currently available chips where possible and PLCC footprints to keep the board small. It has a Programmable CPLD and it has lots of RAM and ROM and a VDC video system using a dual-port RAM that allows clocking the CPU and VIDEO systems independently. It includes CLCD IO for IEC. It has three processors for PET, SuperPET, and CP/M.

CHIP SELECTS

CS1: \$E81x - PIA  
CS2: \$E2x - VIA 1  
CS3: \$E84x - VIA 2  
CS4: \$E80x - VIA: IEC/Control  
CS5: \$E88x - VDC  
CS6: \$8000-AFFF - VID RAM (Dual Port)  
CS7: \$E890-EBAF - SID#1  
CS8: \$E880-EBCF - SID#2

ADDRESS SPACE

\* AD-A14 (32K SIZE) to DPGRAM  
\* AD-A11 (4K 51x) to all RAM/ROM/IO  
\* A12-A18 replaced by MA12-MA18 to RAM/ROM  
\* MMU translates MA lines to map in appropriate ranges

CPLD INFO

\* Reset to SYSTEM MENU  
\* Select 6502 and system ROM CODE bank  
\* Generates Chip Selects  
\* Control Register  
- 3 bits for CPU select  
- 3 bits for SPEED divisor (16/8/4/2/1)  
- 1 bit for SYSTEM ROM select  
\* Generate WAIT for slow devices  
\* Register for 8296 Mode at \$77FF

NOTES:

- uMMF Altera MAX CPLD  
- CPUs: 65C02, 63C09, Z84C0020  
- Video uses DPGRAM for 80 col or extended modes.  
- Character ROM size increased.  
- TTL Serial for Bluetooth/WiFi  
- Internal headers for ports  
- Firmware will need to be patched to support VDC.  
- Use an RGB output to a modern VGA/HDMI panel.

Started: 2023-01-12  
Updated: 2023-02-20

Work in Progress!!!

## MAIN MEMORY