RESET

Install DS to proper pins!

DS1813 pins 2,3,4 – Reset with Pushbutton
DS1233 pins 1,2,3 – Reset + Install 0.01uF cap

SEL

CLOCKS

Half-Can Oscillator

Pullup on 1 and 13

CPU CLOCK

VDC CLOCK

CPLD

CPU Clock Out
Master Clock IN

EXTENDED ADDRESS lines to MEMORY.

CORE chip selects

DATA lines are used to set MMU

DATA lines are INPUT only to the CPLD.

ADDRESS lines (A7–A15) are used to generate EXTENDED ADDRESS (MA10–MA19) lines to MEMORY and I/O.

Lines that don't fit... boo.

MULTI–CPU

65C02

- Max 14MHz clock
- /BE input to tristate bus (HALT)
- /RDY output to pause CPU (WAIT)
- PHI2 output is data latch (PHI2)
- /RESET starts execution at $FFFC

6309E

HD63C09

- Max: B=2MHz, C=3MHz (CLOCK)
- Clock must be 4x CPU speed!
- /HALT input and sets busses to HI–Z.
- /IRQ input for interrupts.
- E output data latch (PHI2)
- MRDY input for slow devices (WAIT)
- /RESET must last at least 1 clock cycle
- /RESET starts execution at $FFFE/FFFF

Z84C0020

Z80CPU–LCC

Z84C0020

- Max 20MHz clock (CLOCK)
- /BUSREQ input tristates bus. Needs pullup (HALT)
- /WAIT is input for slow devices (WAIT)
- /IORQ is output. Used to select IO devices
- /MREQ is output. Used to select Memory devices.
- /IOREQ and /MREQ are latch output (PHI2)
- /RESET must last at least 3 clock cycles.
- /RESET starts execution at $0000

MAIN MEMORY

RAM

Qualified by PHI2?

ROM

4K

256

1MB

SUPER I/O

ACIA

TTL HEADER

EXPANSION

JOYSTICKS

VIA: IEC / CONTROL

IEC

CONTROL HEADER

IEC CONNECTOR

C64–LIKE CARTRIDGE PORT

Cartridge/Expansion (44 PIN FEMALE) CN2

VIDEO

VDC

LATCH

DPRAM

FONT ROM

VDC RAM

RGBI BUFFER

RGBI HEADER

INTERNAL MONITOR HEADER

RGBI TO RGB

RGB TO COMPOSITE

SPARES

Bypass Caps

CONTROL LINES

- CTRL0 – FONTSET – Select TEXT/GRAPHIC Set
- CTRL1 – FONTOPT – Select ALT Font Set
- CTRL2 – –
- CTRL3 – –
- CTRL4 – –
- CTRL5 – –
- CTRL6 – VDC_HI – Select VDC upper 32K. 0=ROM, 1=RAM.
- CTRL7 – VRAM_HI – Select VRAM 16K BANK: 0=Lower, 1=Upper.

PET I/O

PIA#1: KEYBOARD / CASSETTE

KEYBOARD PORT

AUDIO

PIEZO SOUND

SID#1

SID#2

SID POWER SELECT

?: Can we support two ARMSID2 dual SID chips??

POWER

INPUT / SWITCH

VOLTAGE REG

POWER TAPS

LED

PIA#2: IEEE

IEEE PORT

VIA: IEEE/USER/CASSETTE

Not Implemented

USER PORT

CASSETTE PORTS

CASS#1

CASS#2

AUDIO MIX

VIDEO/AUDIO PORT

DESCRIPTION

This is a development board for producing a working "SuperColourPET". It uses currently available chips where possible and PLCC footprints to keep the board small. It has a Programmable CPLD and it has lots of RAM and ROM and a VDC video system using a dual–port RAM that allows clocking the CPU and VIDEO systems independantly. It includes CLCD IO for IEC. It has three processors for PET, SuperPET, and CP/M.

CHIP SELECTS

CS_RAM: $0000–$7FFF – Core Main RAM
CS_ROM: $8000–$FFFF – Core Main ROM
CS_ACIA: $EFF0–$EFFFF – Core ACIA

CS1: $E81x – PIA
CS2: $E82x – VIA 1
CS3: $E84x – VIA 2
CS4: $E80x – VIA: IEC/Control
CS5: $E88x – VDC
CS6: $8000–AFFF – VID RAM (Dual Port)
CS7: $E890–EBAF – SID#1
CS8: $EB80–EBCF – SID#2

ADDRESS SPACE

* A0–A14 (32K SIZE) to DPRAM
* A0–A11 (4K six) to all RAM/ROM/IO
* A12–A18 replaced by MA12–MA18 to RAM/ROM
* MMU translates MA lines to map in appropriate ranges

CPLD INFO

* Reset to SYSTEM MENU
  – Select 6502 and system ROM CODE bank
* Generates Chip Selects
* Control Register
  – 3 bits for CPU select
  – 3 bits for SPEED divisor (16/8/4/2/1)
  – 1 bit for SYSTEM ROM select
* Generate WAIT for slow devices
* Register for 8296 Mode at $????

NOTES:

- uMMF Altera MAX CPLD
- CPUs: 65C02, 63C09, Z84C0020
- Video uses DPRAM for 80 col or extended modes.
- Character ROM size increased.
- TTL Serial for Bluetooth/WiFi
- Internal headers for ports
- Firmware will need to be patched to support VDC.
- Use an RGBI output to a modern VGA/HDMI panel.

TODO:

– ADD COMPOSITE OUTPUT

TODO:

* Check power requirements!
* Add internal PET power header
* ARMSID2 support
* VDC Composite out

6502

PET MODE

* Standard Memory Map
* 32K RAM
* $8000–87FF – Video (40 or 80 col)
* $9000–9FFF – Option ROM 1
* $A000–AFFF – Option ROM 2
* $B000–DFFF – BASIC ROM
* $E000–EFFF – Editor ROM (minus IO area)
* $E800–EFFF – I/O (no mirroring)
* $E000–FFFF – KERNAL ROM

8296 MODE

* Standard PET plus...
* Expanded Memory
* $FFF0 – Config register

ColourPET MODE

* Standard PET plus...
* Enhanced Editor ROM
* $8800–8FFF – Colour RAM (40/80 col)

6809

SuperPET MODE

* 32K RAM at $0000–7FFF
* Video at $8000–$87FF (40 or 80 col)
* Expansion RAM at $9000–9FFF
* Sytem ROM at $E000–FFFF (minus IO area)
* I/O at $E800–$EBFF (no mirroring)
* Control Registers:
  * $EFFE – $9xxx RAM/ROM select
  * $EFFC – Bank select
  * $EFFB – System Latch
* $EFEx – ACIA
* $EFEx – 6702 Protection

Z80

CP/M MODE

* $0000–7FFF – 32K RAM
* $8000–FFFF – 32K DPRAM
* Video anywhere inside $8000–$87FF (40 or 80 col)
* Sytem ROM loaded to DPRAM
* I/O NOT mapped into ram $E800–$EBFF
* Jump at $0000 to ROM (prepped by SYSTEM MENU)

Started: 2023–01–12
Updated: 2023–02–20

Work in Progress!!!

SuperColourPET–VDC	
Steve J. Gray	
Sheet: /	
File: SuperColourPET.kicad_sch	
Title: SuperColourPET	
Size: A1	Date: 2023–02–24
KiCad E.D.A. kicad 7.0.6	Rev: Id: 1/1