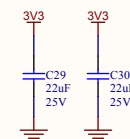
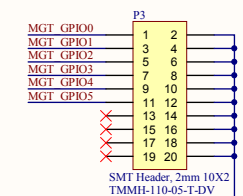
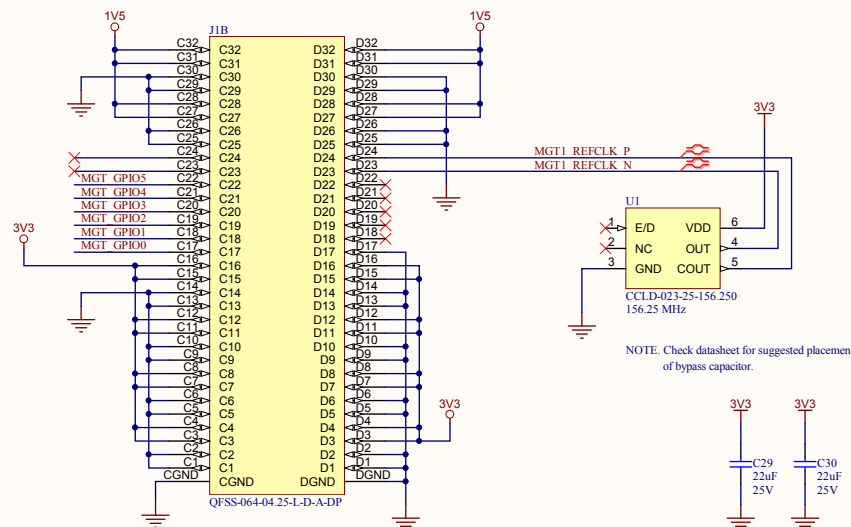
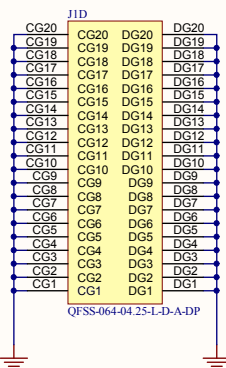
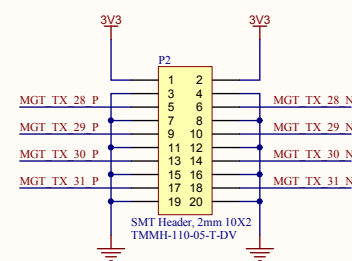
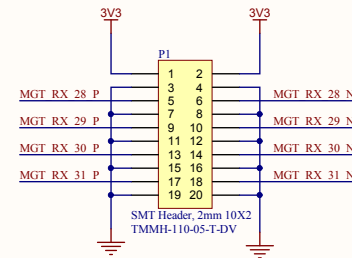
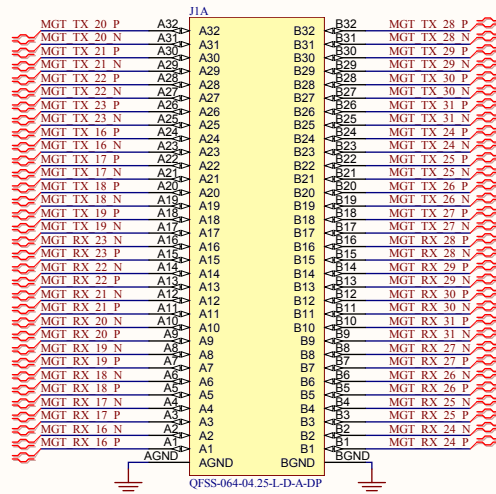
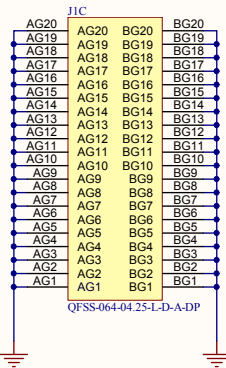


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NOTE: Check on decoupling requirements for the power rails on the SAMTEC connectors coming into the PCB.
Place 22uF caps as close to the incoming 3V3 as possible.

NOTE: Possible FINE pitch SAMTEC header. Will depend on space available on PCB. May want Power on spare pins?

NOTE: D17 connected to GND to enable CLK



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DOCUMENT NUMBER:	XXXX
SCHEMATIC FILENAME:	CX4_3port_card_SchDoc
DESIGNER:	P. Gibbs
ENGINEER:	D. George
APPROVED:	

CIRCUIT DIAGRAM
CX4 Mezzanine Card
FPGA Mezzanine Cards

DATE:	Dec 2010
SHEET:	1 of 1
REVISION:	A

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