SFP+: Advantages and Challenges in designing-in SFP+

SFP+ is the next generation transceiver module form factor designed for Fibre Channel and the Ethernet applications. SFP+ is being specified by the ANSII T11 group (for the 8.5Gbit/s and 10Gbit/s Fibre Channel) and the SFF committee. Mechanically the module is similar to SFP (used for lower bit rates like 1Gbit/s-4Gbit/s) which is 30% smaller in size than XFP. Besides the size, SFP+ has other advantages such as low power consumption, simple optical design and low cost compared to XFP. SFP+ will support IEEE 802.3ae (Clause 52), IEEE 802.3aq (Clause 68) and 8G/10G Fibre Channel (FC-PI-4). Different port types include 10GBASE-SR, 10GBASE-LR, 10GBASE-ER and 10GBASE-LRM. For 8G Fibre Channel it will support SW (short wavelength) and LW (long wave).

SFP+ Advantage

10Gbit/s market has seen at least 5 prominent form factors over the last 7 years with SFP+ being the latest. Fig 1 compares SFP+ to its predecessors in the 10G arena. For all these form factors, the trend has been to push some functions to the host board and simplify the optical module. With SFP+, the signal conditioning function has been moved from the module to the host card along with SerDes, Clock Data Recovery (CDR), EDC (Electronic Dispersion Compensator) and the PCS, PMA, PHY and MAC layers. This simplifies the optical design from a component count point of view with just the electrical-to-optical and optical-to-electrical functions. The small size and low power consumption of SFP+ will enable a higher port density with lower cost per Gigabit which is ideal for the increasing bandwidth needs.

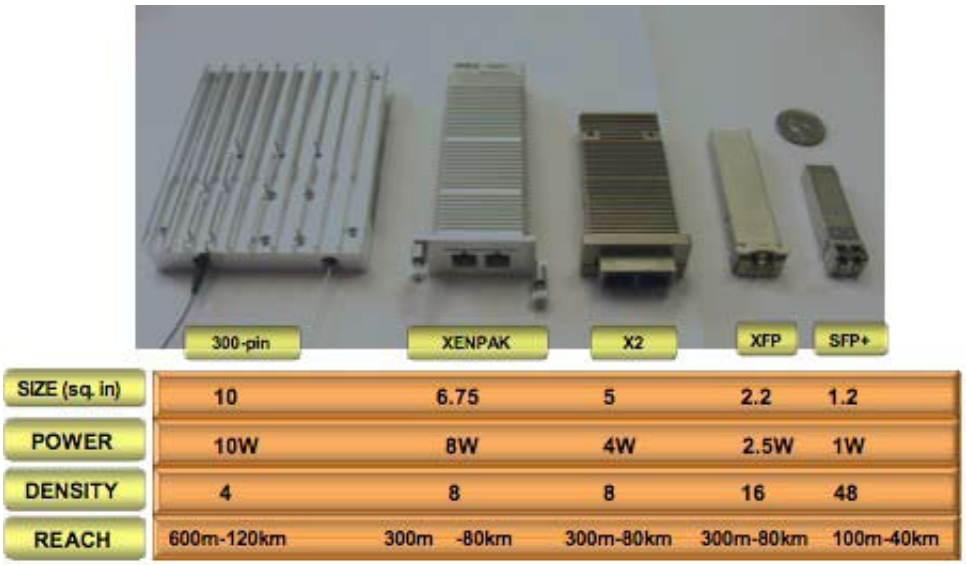

Figure 1: 10G Form Factor comparison. The market trend has always been to reduce to the size and power consumption of the optics and increase the port density on the host board.

The arrival of SFP+ in the marketplace is coinciding with the availability of 65nm CMOS process technology from Silicon foundries. SFP+ can make use of the 65nm CMOS technology to help reduce the cost and power consumption. 65nm

CMOS technology has good frequency response and is fast enough to drive 10G signals. Optical modules such as SFP+ have always been an attractive alternative to copper solutions due to their superior EMI performance. Existing 10Gbit/s copper solutions are bulky, require expensive packaging, or have high power dissipation limiting their popularity. The ease of use and familiarity of SFP are added advantages of SFP+. The simplicity of SFP+ will enable volume production. Because of all these reasons many optical component suppliers are developing SFP+ and system vendors are selecting SFP+ for next generation systems.

Design challenges

The functionality of SFP+ Optics has been simplified by moving the CDR block to the host board. Since the host board invests in large ASICs with millions of gates, the incremental cost to add functionality to the host board is lower than having silicon gates in both the module and the host. The trade-off is that now the host must have this functionality on all ports – even those that may ship out to customer networks initially empty. A block diagram of SFP+ transceiver and Host IC is shown in Fig 2. On the Tx side, SFP+ module has a laser driver to drive the transmit data and a Transmitter Optical Sub-assembly (TOSA) to transmit the data via fiber. On the Rx side, it has a Receiver Optical Sub-assembly (ROSA) with a built-in trans-impedance amplifier (TIA) and potentially a post amplifier.

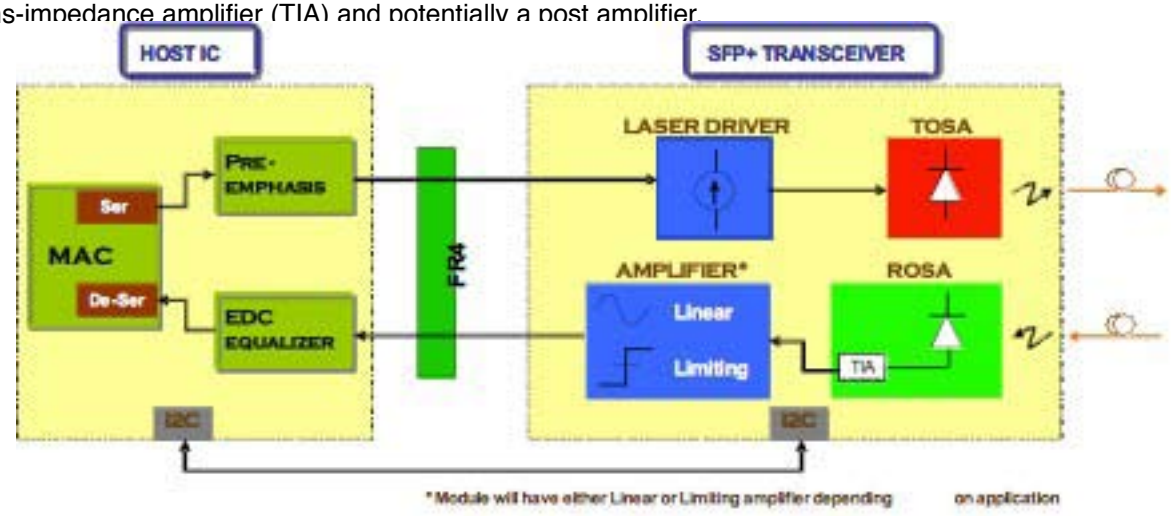

Figure 2: SFP+ Block Diagram. SFP+ Optics has a laser driver and a Transmit Optical Sub-assembly on the transmit side, a Receiver Optical Sub-assembly and one or more amplifiers on the Receiver side. The MAC IC on the host board has a Serializer and Pre-Emphasis on the Transmit side and an EDC and Deserializer on the Receive side.

The SFP+ transceiver has a 20pin Electrical connector with a serial data interface to communicate with the Host IC. The trace length between the SFP+ transceiver and the Host IC is specified at 200mm of improved FR4 or 150mm of standard FR4. Designing the Electrical trace can be a challenge because eliminating the CDR IC from the Optics has removed redundancy and margin from the electrical trace. In order to overcome this challenge the Host IC will have to carry some additional functionality to compensate for the tight jitter budget and the noise from the trace. The Host IC which interfaces with the SFP+ should have some emphasis control to mitigate signal degradation due to PCB and external media impairments as the data is transferred to the SFP+ and converted to an optical signal. Emphasis control on host IC will improve the jitter and the optical eye mask margin of the transmitted data. On the receiver side, the Host IC will have an equalizer like EDC (Electronic Dispersion Compensator) to mitigate host Rx trace characteristics. Some system vendors may choose to implement a high complexity equalizer such as the EDC which is specified in 10GBASE-LRM in order to provide a system which supports all port types. Other system vendors will choose a simple equalizer to compensate for parasitic effects of the host board.

An SPF+ transceiver either has a limiting post amplifier or a linear amplifier depending on the application. A limiting stage in the amplifier “slices” the data at the decision level, and then amplifies the result – this has the effect of enhancing the vertical opening of the eye, but it retains the jitter. There is no signal reshaping in the case of linear amplification, so all of the frequency data is passed along the trace to the decision circuit on the host board ASIC. 10GBase-LRM application requires a linear signal to be processed by an equalizer in order to meet the distance spec (220m with FDDI grade multi-mode fiber). So SFP+ LRM has a strong TIA instead of TIA-Post Amplifier combination to provide a linear signal to the EDC on the Host IC. The EDC has to compensate for the optical impairments as well as the electrical loss of the signal on the host board.

The system error rate is determined by the entire receive chain, so the designer must carefully select a PHY IC, SFP+ Optical Transceiver and optimize the design of the electrical path on the host board. It is recommended that the PCB traces meet 100±10 differential impedance with nominal 7% differential coupling. To further complicate matter, most systems intend for multiple SFP+ port types from multiple manufacturers to all have good performance in the same host board slot. Thorough interoperability testing should be completed with PHY ICs and SFP+ modules to determine if the specification is fully met. A good combination should provide satisfactory jitter performance and provide enough mask margin to meet the Transmitter specification. Voltage, temperature and Humidity effects on Data Dependent Jitter (DDJ) should be tested. The receiver and the EDC combination should operate error-free at and between the Receiver sensitivity and overload limits.

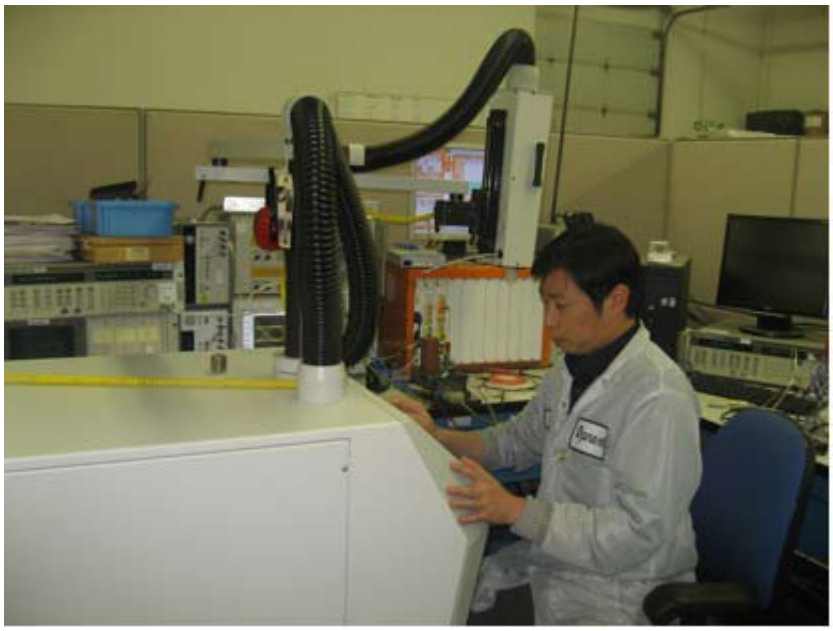

FIGURE 3: Engineer testing for interoperability with Opnext SFP+ LRM and various PHY ICs using a stress tester.

40Km SFP+

Samples of 8G Fibre Channel, 10GBase-SR, LR and LRM are already available today. But 10GBase-ER will be challenging in terms of maximum power consumption. The SFF Committee has specified 1.0W as the maximum power consumption for Power Level 1 modules and 1.5W for Power Level 2 modules. Achieving 1.5W target for 10GBase-ER is feasible by using an uncooled EA-DFB Laser. Uncooled Electro-absorption (EA) modulator integrated distributed feedback (DFB) lasers are suitable for this application due to its low chirp, low driving voltage and compact size. Uncooled EA-DFB lasers operate without Thermo Electric Coolers (TEC) and hence burn less power. Opnext had demonstrated a live 40km 10GBase-ER SFP+ at OFC 2007 with an in-house Uncooled EA-DFB Laser with ~1.2W power consumption at a module case temperature of 70°C. An example of test results using Opnext uncooled EA-DFB is shown in Fig 4.

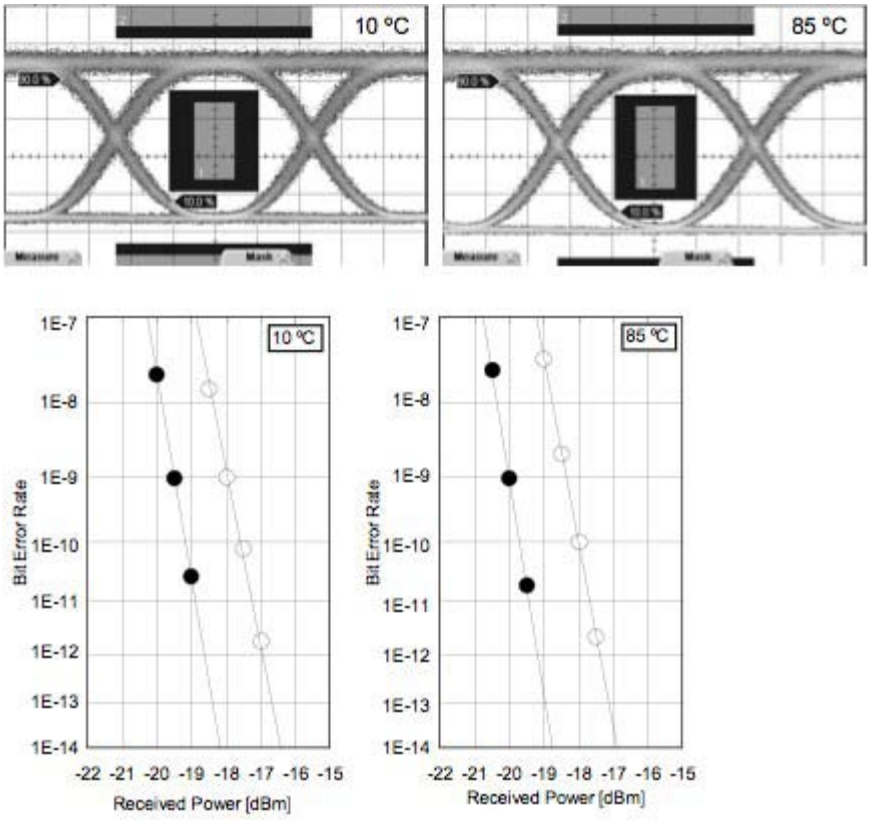

Figure 4: Above: Back to Back eye diagrams under 10.7-Gbit/s operation at 10ºC (left) and 85ºC (right) after 200 waveforms accumulations. Below: Bit Error Rate curves of Back to Back and after 40 km (800 ps/nm) SMF transmission under 10.7 Gbit/s operation at 10ºC (left) and 85ºC (right)

Fibre Channel Vs 10G Ethernet

Even though SFP+ is the preferred form factor for Fibre Channel (FC) and Ethernet groups, the specifications are different. Fibre Channel Specification is defined by FC-PI-4 (Fibre Channel Physical Interface-4) and was written contemporaneously with the SFP+ requirements. The IEEE 10GbE specifications were written to be form factor agnostic and thus the SFP+ is not as optimized for 10GbE. The SFP+ transmitter and receiver specification for Fibre Channel was written to be easier to meet compared to the Ethernet SFP+. In addition to lower cost, the lower data rate and transmission distance requirements for 8G Fibre Channel enable backward compatibility to previous 4G and 2G Fibre Channel generations. Below table shows some of the key transmitter and receiver specifications for 8G Fibre Channel and 10GbE.

	8G Fibre Channel SW (Limiting Design)	10Gbase-SR (Limiting Design)
Bit Rate	8.5 Gbit/sec	10.3125 Gbit/sec
Transmission distance	150m (over OM3 Fiber)	300m (over OM3 fiber)
Spectral Width	Triple Tradeoff Curve <0.45 nm	0.65nm
Minimum Average Launch Power	-8.0 dBm	-7.3 dBm
Unstressed Receiver Sensitivity in OMA	-11.2 dBm	-11.1

Conclusion

As the market demand for 10Gbit/sec increases, it will be challenging for the legacy forms factors like XENPAK, X2 and XFP to meet the cost/density requirements. Copper solutions cannot deliver the densities required for volume production for at least in the near future. This makes SFP+ very attractive and hence it is set to become the preferred form factor for the next generation 10Gbit/s applications. Systems vendors can achieve low cost per Gigabit with a careful board design and thorough testing for interoperability.

References

1.SFF-8431 Specifications for Enhanced 8.5 and 10Gigabit Small Form Factor Pluggable Module “SFP+”, Revision 2.1, 30 August 2007

2.Fibre Channel Physical Interface-4 (FC-PI-4) Rev 7.00

3.N. Sasada, et al., “Un-cooled operation (10 ºC to 85ºC) of a 10.7-Gbit/s 1.55-mm electro-absorption modulator integrated DFB laser for 40-km transmission” Proc. 33rd European Conf. on Opt. Commun., no.We8.1.5, pp.215-216, Berlin, Germany, Sept.2007.

About the author

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