Design Document
KAT ADC Test Gateware

Introduction

The KAT ADC Test gateware is a simple design which allows 128KB of data from any two KAT ADC channels to be captured and retrieved.

KAT ADC Test Register Map

Name	Addr	Size	Function
CTRL	0x1000000	0x4	A positive edge on bit 0 of this 32-bit register will start an ADC capture. Bits 9:8 and 13:12 control the ADC channel source for QDR0 and QDR1 respectively. The source is decoded as follow: 0 – ADC0 I, 1 – ADC0 Q, 2 – ADC1 – I, 3 – ADC 1 - Q
STATUS	0x1000100	0x4	When least significant bit of this register is set the ADC is busy with a capture
OVERRANGE	0x1000200	0x4	When bits 0:1 are set these indicates an out-of-range condition for ADC0 channel I **OR** Q. When bits 9:8 are set these indicates an out-of-range condition for ADC1 channel I **OR** Q
SYNC_COUNT0	0x1000300	0x4	This value indication the number of pulses received from the sync input on ADC 0
SYNC_COUNT1	0x1000400	0x4	This value indication the number of pulses received from the sync input on ADC 1
ADC_CTRL	0x20000	0x10	This register provides control functions for both KAT ADCs. See OPB KAT ADC Controller register map below for detailed behaviour.
IIC_ADC0	0x40000	0x10	This maps a KAT IIC Controller to access the IIC on ADC0. See below for further details on IIC access.
IIC_ADC1	0x48000	0x10	This maps a KAT IIC Controller to access the IIC on ADC1. See below for further details on IIC access.
QDR0	0x2000000	0xFFFFFF	This memory contains the data from a capture, the source of which depends on the CTRL source setting.
QDR1	0x3000000	0xFFFFFF	This memory contains the data from a capture, the source of which depends on the CTRL source setting.
BOARD_ID	0x0	0x2	This should always contain 0xdeaf

OPB KAT ADC Controller Register Map

Name	Offset	Length	Function
DCMCTRL	0x1	0x1	Bit 1 controls the direction of the clock to data phase adjustment of ADC0; writing 1 to bit 0 will adjust the clock phase by one increment Bit 5 controls the direction of the clock to data phase adjustment of ADC1; writing 1 to bit 4 will adjust the clock phase by one increment
RESET	0x3	0x1	Writing '1' to bit 0 resets ADC0; writing '1' to bit 1 resets ADC1
ADC0_DATA	0x4	0x2	Sets the data word for the three wire interface (ADC0)
ADC0_ADDR	0x6	0x1	Sets the address for the three wire interface (ADC0)
ADC0_START	0x7	0x1	Writing '1' to bit 0 will start a three-wire interface configuration word load (ADC0)
ADC1_DATA	0x8	0x2	Sets the data word for the three wire interface (ADC1)
ADC1_ADDR	0xa	0x1	Sets the address for the three wire interface (ADC1)
ADC1_START	0xb	0x1	Writing '1' to bit 0 will start a three-wire interface configuration word load (ADC1)

KAT IIC Controller Register Map

Name	Offset	Length	Function
OPFIFO	0x2	0x2	Setting Bit 10 will terminate the IIC byte access with a STOP Sequence and send a “No Acknowledge” with on the associated read. Setting Bit 9 will initiate the IIC byte access with a START Sequence. When bit 8 is high the byte transfer is a read, when low a write. Bits 7:0 contain the data to be written and are unused in the write case This FIFO will latch on a LSByte write.
RXFIFO	0x6	0x2	Bits 7:0 of this FIFO contains the data read during a byte read transfer. This FIFO will latch on a LSByte read.
STATUS	0xb	0x1	Bit[0] RXFIFO empty flag Bit[1] RXFIFO full flag Bit[2] RXFIFO overflow error latch Bit[4] OPFIFO empty flag Bit[5] OPFIFO full flag Bit[6] OPFIFO overflow error latch Bit[8] NACK on write error latch Any write to these register will clear all latches and reset all fifos

KAT IIC Notes

OPFIFO and RXFIFO are 32 deep.

KAT ADC / KAT IIC Examples (From UBoot)

Note: when entering Uboot commands ensure operations are entered all at once otherwise iic device will timeout

To Access Local (Ambient) Temperature on TMP421 (IIC ADDR 0x4C, REGISTER ADDR 0x0)

```
mw d0040000 298; # START, WRITE, DATA=0x98 (4C << 1 + 0x0(IIC WRITE))
mw d0040000 000; # WRITE, DATA=0x00 (Register Address)
mw d0040000 299; # START(REPEATED), WRITE, DATA=0x99 (4C << 1 + 0x1(IIC READ))
mw d0040000 500; # STOP, READ
md d0040004 1; # Read Data from RXFIFO

mw d0040000 298; mw d0040000 000; mw d0040000 299; mw d0040000 500; md d0040004 1;
```

To Access ADC Temperature on TMP421 (IIC ADDR 0x4C, REGISTER ADDR 0x1)

```
mw d0040000 298; # START, WRITE, DATA=0x98 (4C << 1 + 0x0(IIC WRITE))
mw d0040000 001; # WRITE, DATA=0x01 (Register Address)
mw d0040000 299; # START(REPEATED), WRITE, DATA=0x99 (4C << 1 + 0x1(IIC READ))
mw d0040000 500; # STOP, READ
md d0040004 1; # Read Data from RXFIFO

mw d0040000 298; mw d0040000 001; mw d0040000 299; mw d0040000 500; md d0040004 1;
```

To Write EEPROM DATA (IIC ADDR 0x51, ADDR 0x4, DATA 0xDEADBEEF)

```
mw d0040000 2A2; # START, WRITE, DATA=0xA2 (0x51 << 1 + 0x0(IIC WRITE))
mw d0040000 004; # WRITE, DATA=0x04 (Register Address)
mw d0040000 0de; # WRITE, DATA=0xde
mw d0040000 0ad; # WRITE, DATA=0xad
mw d0040000 0be; # WRITE, DATA=0xbe
mw d0040000 4ef; # WRITE, DATA=0xef

mw d0040000 2A2; mw d0040000 004; mw d0040000 0de; mw d0040000 0ad; mw d0040000 0be;  mw d0040000 4ef;
```

To READ EEPROM DATA (IIC ADDR 0x51, ADDR 0x4)

```
mw d0040000 2A2; # START, WRITE, DATA=0xA2 (0x51 << 1 + 0x0(IIC WRITE))
mw d0040000 004; # WRITE, DATA=0x04 (Register Address)
mw d0040000 2A3; # START(REP), WRITE, DATA=0xA2 (0x51 << 1 + 0x1(IIC READ))
mw d0040000 100; # READ
mw d0040000 100; # READ
mw d0040000 100; # READ
mw d0040000 500; # STOP, READ
md d0040004  1;
md d0040004  1;
md d0040004  1;
md d0040004  1;
```

To SET ADC1 PCA9555 Output 0 [7:0] to enabled (IIC ADDR 0x21, ADDR 0x6)

```
mw d0040000 242; # START, WRITE, DATA=0x42 (21 << 1 + 0x0(IIC WRITE))
mw d0040000 006; # WRITE, DATA=0x06 (Register Address)
mw d0040000 400; # STOP, WRITE, DATA=0x00 (OE_n [7:0] = 0x0)
```

To SET ADC1 PCA9555 Output 0 [7:0] (IIC ADDR 0x21, ADDR 0x2, Data 0xF0)

```
mw d0040000 242; # START, WRITE, DATA=0x42 (21 << 1 + 0x0(IIC WRITE))
mw d0040000 002; # WRITE, DATA=0x02 (Register Address)
mw d0040000 4F0; # STOP, WRITE, DATA=0xF0
```