Nicholas Kelly

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Objective

To advance my education and experience in Computer Engineering so that I can contribute to the field of Computer Architecture.

Education

Jan 2014 - May 2016

University of Texas at Austin — Austin, TX
M.S. in Computer Architecture and Embedded Systems (3.92 GPA) - Spring 2016

Sept 2009 - Jun 2013

Oregon State University — Corvallis, OR
B.S. in Electrical/Computer Engineering (3.91 GPA) - Spring 2013

Relevant Experience

Jun 2016 - Present

CPU Core Architect — Intel | Hillsboro, OR

- Core memory system micro-architecture
- CPU performance modeling (C++) and analysis
- Tooling improvements for data collection/anaylsis (Python, Ruby)

Jan 2015 - May 2016

Graduate Research Assistant — Prof. Mattan Erez | UT Austin | Austin, TX

- Resiliency characterization through error injection and simulation (C++, Python, Verilog)

May 2015 - Aug 2015

Validation Intern — ARM | Austin, TX

- Interconnect power and clocking validation/coverage

Qualifications

Computer Arch.

CPU simulation using C++, visualization, and anaylsis in Python/Pandas/Jupyter
Scripting with Python, Ruby, Perl, and Tcl
Embedded assembly and/or C development (PIC, AVR, MSP430, ARM)
VLSI design with Verilog/SystemVerilog/UVM and various EDA tools
Graphics theory and programming (OpenGL, CUDA)
Coursework and research in computer architecture

Software

Continuous integration with TeamCity/GitHub/GitLab, for JS, Python, Ruby, and C++
Unit-test frameworks, linting, coverage, and static-analysis within JS, Python, Ruby, and C++
Runtime and memory profiling of C++ programs (VTune, valgrind, jeprof)
Software-engineering practices (e.g. testing, OO, design patterns, etc.) teaching in industry

Additional

Communication and support skills, across teams
Able to learn new material quickly

Selected Projects

Jan 2014 - June 2016

Computer Architecture and Embedded (UT)

- x86 (subset of ISA) processor in structural-verilog (SystemVerilog, Python, x86)
- Realtime GPU Raytracing
- Lightcuts and Illumination
- An analysis of 3DIC Kogge-stone Adders
- Auto-Multithreading extension for Node.js and V8
- GPU Power virus (genetic algorithm, code generator)
- SDF scheduling genetic algorithm to optimize towards energy usage
- Development of custom RTOS for TI Launchpad (ARM)

Sept 2012 - Jun 2013

VLSI/Analog Design and Simulation Projects (OSU)

- Simulation of power-gating and near-threshold effects on power and delay for XOR gate
- Designed bike POV circuit using SystemVerilog, ModelSim, and Cadence Encounter (Place-and-route)
- Design, simulation (HSPICE/Spectre), and layout (Cadence) of OTAs for different specifications

Publications

Conferences

- Chang, C.; Lym, S.;**Kelly, N.**; Sullivan, M. B.; Erez, M., "Evaluating and Accelerating High-Fidelity Error Injection for HPC," In Proceedings of The International Conference for High Performance Computing, Networking, Storage, and Analysis (SC). Dallas, TX. November, 2018.
- Meier, R.;**Kelly, N.**; Almog, O.; Chiang, P., "A Piezoelectric Energy-Harvesting Shoe System for Podiatric Sensing" Engineering in Medicine and Biology Society (EMBC), 2014 36th Annual International Conference of the IEEE , pp.622,625,26-30 August 2014.

Workshops

- Chang, C.; Lym, S.;**Kelly, N.**; Sullivan, M. B.; Erez, M., "Hamartia: A Fast and Accurate Error Injection Framework," Workshop on Silicon Errors in Logic–System Effects (SELSE). Boston, MA. April, 2018.

References available on request. Additional experience and qualifications available in alternate (e.g. web) resumes.