DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
UNIVERSITY OF BRITISH COLUMBIA
CPEN 211 Introduction to Microcomputers, Fall 2022

Lab Proficiency Test 1 (LPT-1)

October 28th, 2022: 4:10pm-5:40pm. Code to be submitted via Canvas at 5:40pm

1 Description

Question — 5 marks Your LPT-1 is available on Canvas. Please download the pdf file to start your test.

1. Create a file named "q1.sv" and inside it write synthesizable Verilog that implements the Moore finite state machine illustrated in the Figure 1.

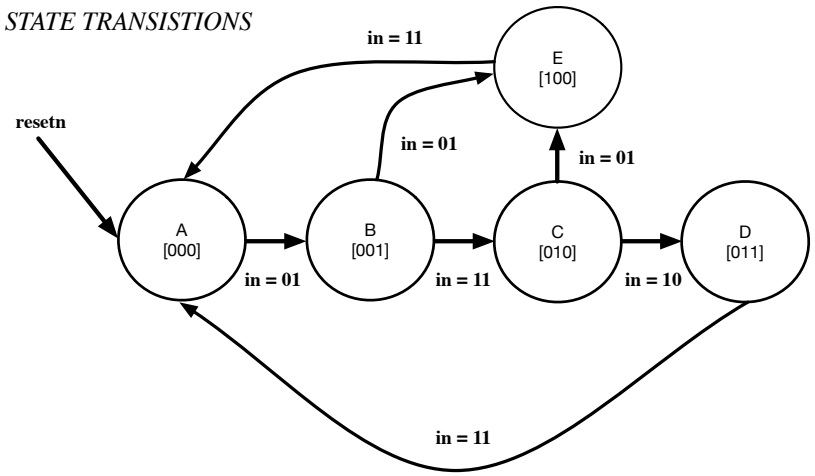

Figure 1: The state transistion diagram. You need to implement this for your LPT-1.

2. State transitions occur on the rising edge of input "clk" and the resetn is synchronous (occurs on the rising edge of clk) and is active low (resetn equal to 1'b0 means RESET).

3. Bits on the left are most significant (have higher index value).

4. Transitions from a state to itself are not explicitly shown.

5. The input "in" is 2-bits wide.

6. The output "out" is 3-bits wide. The output for each state is shown in square brackets. For example, when in state A, out should be 000, and if "in" is 01, then the next state should be B. You can use any state names as you like, provided they follow the same state-transistion diagram.

7. **The autograder used to mark your answer will assume your top-level module is called "top_module" with inputs "clk", "reset" and "in", output "out"** declared as shown in Figure 2.

2 Important Points

1. Your q1.sv file must include definitions for any modules instantiated inside top_module (even those from the slides or textbook).

2. You are strongly encouraged to test your code and you can include testbench modules in q1.sv, but testbench modules inside q1.sv will be ignored by the autograder.

```
module top_module(clk,resetn,in,out);
    input clk, resetn;
    input [1:0] in;
    output [2:0] out;
```

Figure 2: The top-level module. This module MUST be present in your submitted code. This module should implement the state-machine.

3. Upload your Verilog file named "q1.sv" by attaching it as your solution to Question under "Lab Proficiency Test 1" on Canvas before 5:40 pm.
4. In case your computer's time differs from Canvas submit early and resubmit as needed. No submissions will be accepted after 5:40 pm (emailed submissions will not be accepted).
5. **The file you upload for this question must be called "q1.sv" or the autograder script will not mark it. If this occurs, you will get ZERO points and we will not manually grade you. DO NOT UPLOAD ZIP FILES OR ANY OTHER FILE, etc., you only need to upload your q1.sv file.**

3 HOW TO NOT LOSE POINTS

You will lose points for each of the following conditions — the minimum points you can get is ZERO and the maximum is FIVE:

- Your last "Lab Proficiency Test 1" attempt on Canvas does not consist entirely of "q1.sv" (e.g., you submitted a zip file, etc.) — **You will get a ZERO for the entire LPT**.
- Your q1.sv file does not compile using ModelSim (e.g., due to syntax errors, etc.) — **You will get a ZERO for the entire LPT**.
- Your q1.sv file does not contain a module called `top_module` with inputs/outputs **exactly** as described in Figure 2. — **You will get a ZERO for the entire LPT**.
- Your top_module cannot be simulated (e.g., due to missing module definitions in q1.sv) — **You will get a ZERO for the entire LPT**.
- The Verilog used by your top_module is not synthesizable by Quartus — **You will lose 3 points**.
- The Verilog used by your top_module has any inferred latches — **You will lose 2 points**.
- Your top_module output "out" does not **exactly** match the output of the state machine in Figure 1 for all possible sequences of input values for "clk", "resetn" and "in" — **You *may* get some partial credit depending on how many transitions are *reachable and correct***.