Pioneer Board 图文详情

关键日程安排

时间	主要的事项	Owner
4月4日	和厦门开芯会讨论一起发布的事宜。	
4月5日	提交TRM以及Datasheet初版本	魏超
4月8日	网站资料全部准备完毕	
4月12日	PR准备-CNX和RISC-V Foundation	
4月15日	上线，同步厦门开芯会发布	

Meeting：

4.4 11:45

Plain Text 复制代码

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陆吉年 邀请您参加腾讯会议
会议主题：Pionner预售
会议时间：2023/04/04 11:40-12:10 (GMT+08:00) 中国标准时间 - 北京

点击链接入会，或添加至会议列表：
https://meeting.tencent.com/dm/szOSGVrlmubc

#腾讯会议：302-343-435

复制该信息，打开手机腾讯会议即可参与
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制图规范

色彩

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	主色	#0F8DFF	
	辅助	#05EAFF	可与主色结合渐变
	辅助	#00FFCB	可与主色结合渐变

白色为全F

字体

*不强制规定字体，仅作字体参考。按需选择**可商用**字体即可*

- 阿里巴巴普惠体

设计素材

请谨慎选择，避免版权问题

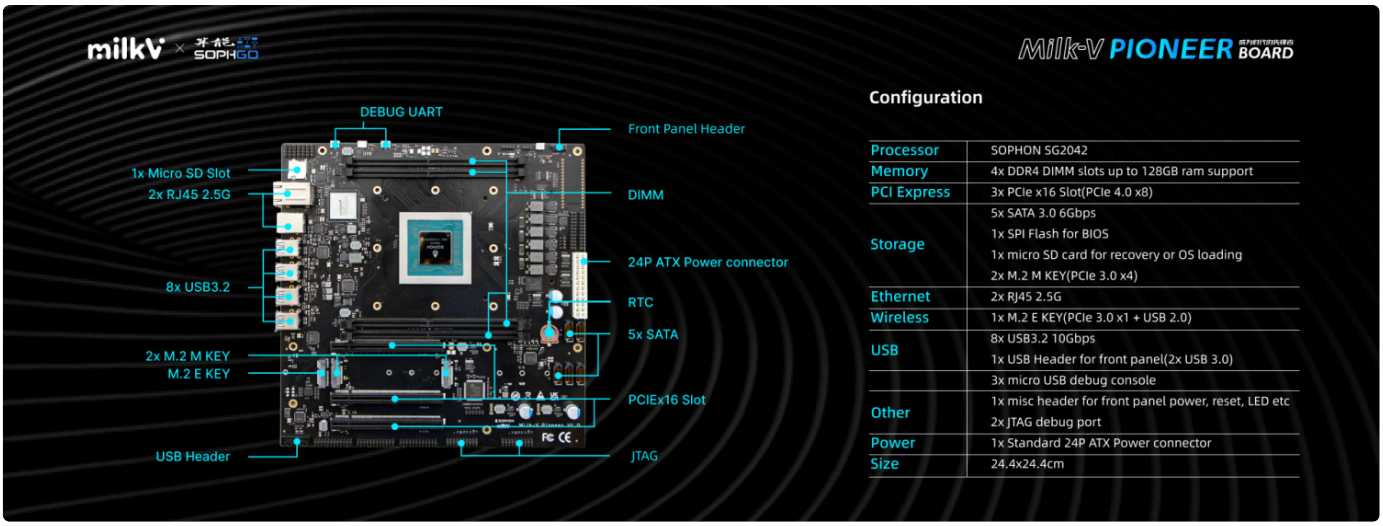
设计一个主图：更新EVB为Pionner Board，还需要确定配色，主色和辅色。

芯片+板子+算能logo+milkV logo+”Embracing the RISC-V Era“+“The first 64-core RISC-V CPU motherboard”

万莫斯

内容部分：

Pioneer Board基本情况介绍 introduction to Pioneer Board



Specification

Specification	
Processor	SOPHON SG2042
Memory	4x DDR4 DIMM slots up to 128GB ram support
PCI Express	3x PCIe x16 Slot(PCIe 4.0 x8)
Storage	5x SATA 3.0 6Gbps
	1x SPI Flash for BIOS
	1x micro SD card for recovery or OS loading
	2x M.2 M KEY(PCIe 3.0 x4)
Ethernet	2x RJ45 2.5G
Wireless	1x M.2 E KEY(PCIe 3.0 x1 + USB 2.0)
USB	8x USB3.2 10Gbps
	1x USB Header for front panel(2x USB 3.0)
	3x micro USB debug console
Other	1x misc header for front panel power, reset, LED etc
	2x JTAG debug port
Power	1x Standard 24P ATX Power connector

Size	24.4x24.4cm

Appllication

- PC
- Workstartion
- Compile Server
- Web Server
- Storge Server
- Soft Router
- Firewall

Why it's named Pioneer

Pioneer意为开拓者、先锋者。SOPHON SG2042的面世，标志着属于RISC-V的时代已经来临。每一个新的时代都会有敢于拥抱新事物的英雄，就像敢为人先的你一样。谨以Pioneer为名，让时代记住所有的英雄。

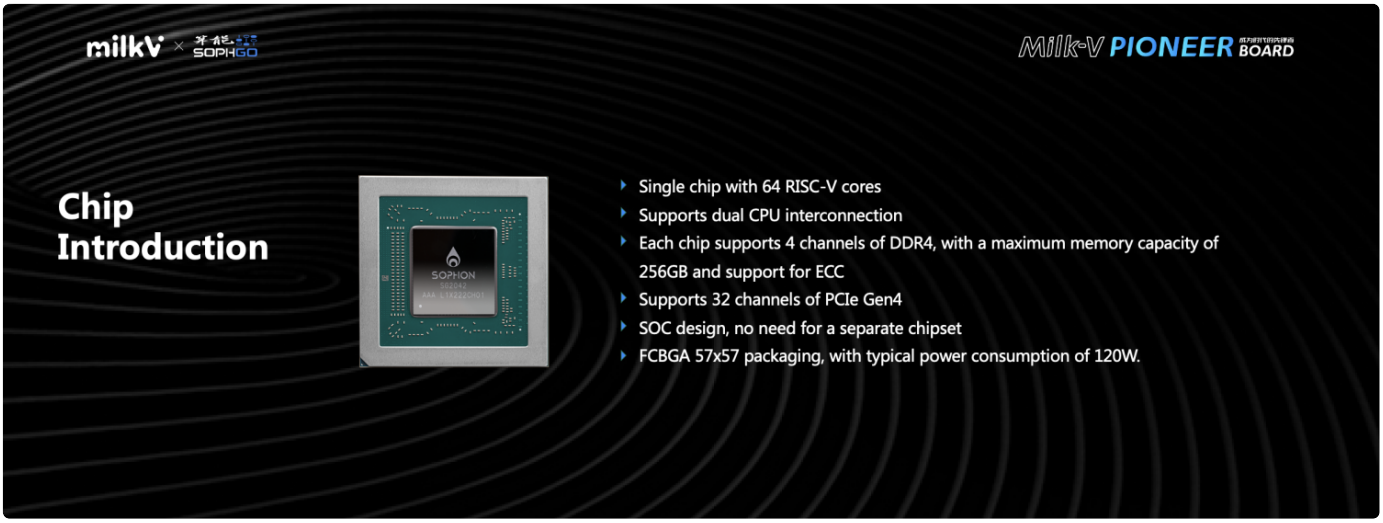
The name Pioneer represents a trailblazer or a person who leads the way in exploring new ideas or areas. With the introduction of the SOPHON SG2042 chip, this product aims to be at the forefront of the RISC-V era, honoring all those who embrace innovation and progress.

Why we made this product

我们希望RISC-V开发者和爱好者可以以一个更低的门槛真正的参与到RISC-V的发展中，参与并体验自己做出的贡献！通过Pioneer Board，你可以轻松地组装一台 RISC-V PC，甚至是搭建一台 RISC-V 工作站。

We hope that RISC-V developers and enthusiasts can truly participate in the development of RISC-V with a lower barrier to entry, getting involved and experiencing the contributions they make! With the Pioneer Board, you can easily assemble a RISC-V PC, or even build a RISC-V workstation.

SG2042基本情况介绍 Introduction to SG2042 Server Level Chip



算能：

SG2042服务器芯片是基于RISC-V指令集架构（ISA），拥有64核的芯片，旨在满足高性能计算需要。RISC-V指令集架构是一个开放的、免费的、基于标准体系结构的指令集，因其开放基础和灵活性得到了广泛关注和应用。

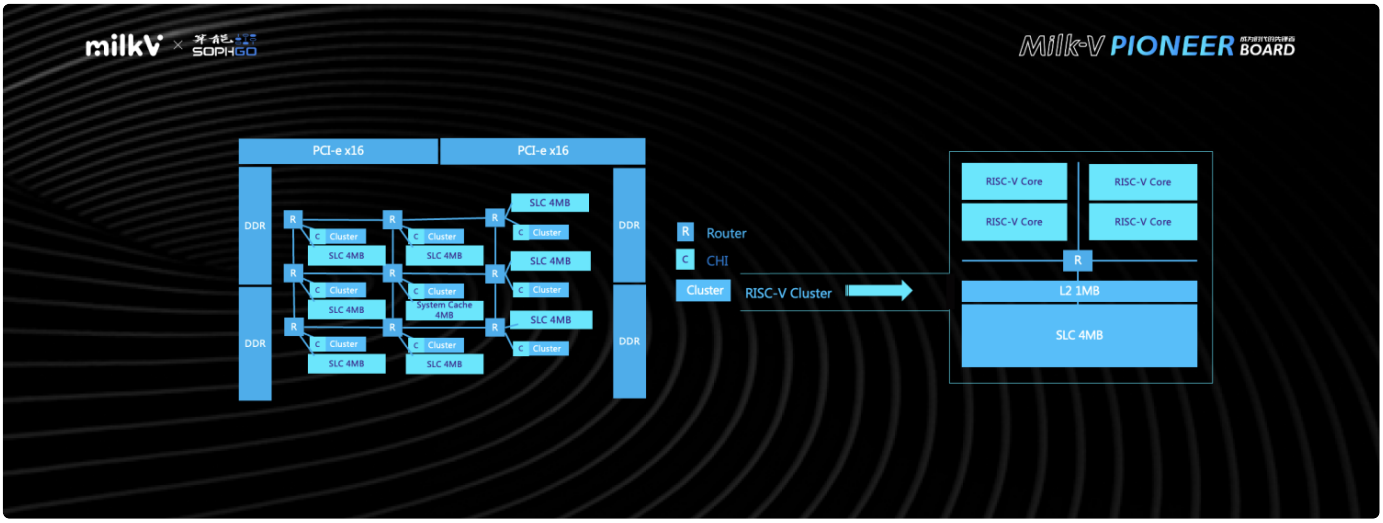
The SG2042 server chip is based on the RISC-V instruction set architecture (ISA) and has 64 cores, designed to meet high-performance computing needs. The RISC-V ISA is an open, free and standards-based instruction set that has gained widespread attention and application due to its open foundation and flexibility.

SG2042服务器芯片的特点包括可扩展性、灵活性和定制化。它们具有高速缓存（L3Cache 64MB、内存控制器（4个 DDR4-3200）、网络接口、PCI Express®控制器（x32 PCI Express Gen4.0）等集成电路，支持通用操作系统（如Linux®等）。

The characteristics of the SG2042 server chip include scalability, flexibility, and customization. They incorporate integrated circuits such as high-speed caches (L3Cache 64MB), memory controllers (4 DDR4-3200), network interfaces, PCI Express® controllers (x32 PCI Express Gen4.0), and support for general-purpose operating systems such as Linux®.

RISC-V芯片生态环境不断扩大，越来越多的公司和组织加入到RISC-V ISA和芯片的开发中。SG2042 RISC-V服务器芯片发布是未来高性能计算和数据中心的一个重要里程碑。

The RISC-V chip ecosystem is constantly expanding, with more and more companies and organizations joining the development of RISC-V ISA and chips. The release of the SG2042 RISC-V server chip is an important milestone for future high-performance computing and data centers.



SG2042主频2GHz

SG2042 has 2GHz.

SG2042采用16个cluster的设计，每个cluster拥有4个RISC-V Core。

It is designed with 16 clusters, each cluster containing 4 RISC-V cores.

每个core，拥有L1-D 64KB，L1-I 64KB的设计。

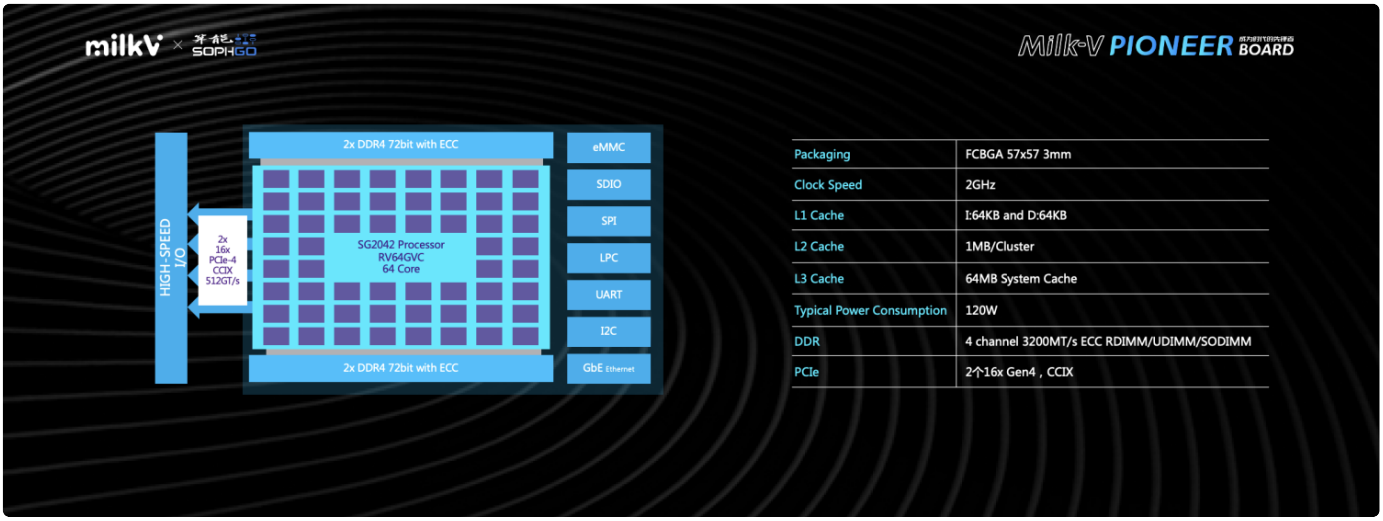
Each core has L1-D of 64KB and L1-I of 64KB.

每4个core组成一个cluster，每个cluster共享L2 1MB的设计。

Every 4 cores form a cluster, and each cluster shares a design of L2 of 1MB.

采用了先进的MESH设计。L3 System cache为64MB。

SG2042 features advanced MESH architecture and an L3 system cache of 64MB.



SG2042 支持通过CCIX两个芯片互联

SG2042 supports two sockets through CCIX.

SG2042具有4个DDR4-3200控制器，支持RDIMM，ECC，UDIMM

SG2042 has 4 DDR4-3200 controllers, supporting RDIMM UDIMM and ECC.

片内具有32x PCI E Gen4.0接口

SG2042 has 32x PCI E Gen4.0 interfaces integrated on-chip.

片内集成eMMC5.1 ，SDIO 3.0，SPI x2，I2C x4，UART x4 以及千兆以太网MAC

SG2042 integrates eMMC5.1, SDIO 3.0, SPI x2, I2C x4, UART x4, and Gigabit Ethernet MAC.

What Pioneer Board can do

Pioneer Board 跟 PC 主板无异，在拿到它的时候，只需插上外设，像寻常的主板一样启动它！

The Pioneer Board is no different from PC motherboards. When you get it, all you need to do is plug in peripherals and start it up just like any regular motherboard!

- Be a PC

  通过给Pioneer Board插上基本的外围设备，让Pioneer Board成为你的个人电脑。轻松办公，开发 RISC-V 软件甚至你可以用它来玩游戏。

  By connecting basic peripherals to the Pioneer Board, you can turn it into your personal computer. Effortlessly handle office tasks, develop RISC-V software, or even use it for gaming.

- Be a Workstation

  通过给Pioneer Board插上更专业的外围设备，如高算力的显卡或计算卡、更多的硬盘。轻松完成软件的编译和视频渲染等专业生产，让RISC-V帮助你提高生产力。

  By connecting more professional peripherals to the Pioneer Board, such as high-performance graphics or computing cards and additional hard drives, you can easily accomplish tasks like software compilation and

video rendering for professional production. Let RISC-V help you boost your productivity.

- Be a Server

  凭借Pioneer Board丰富的SATA接口与M.2 MKEY接口，你可以搭建一个拥有巨额存储的服务器。64核RISC-V核心，可以给你提供超强的多进程处理能力。试试在上面运行你的服务！这一定能使你惊艳。你可以通过PCIE接口连接Intel X520-2，为你的Server添加双10G的网口！

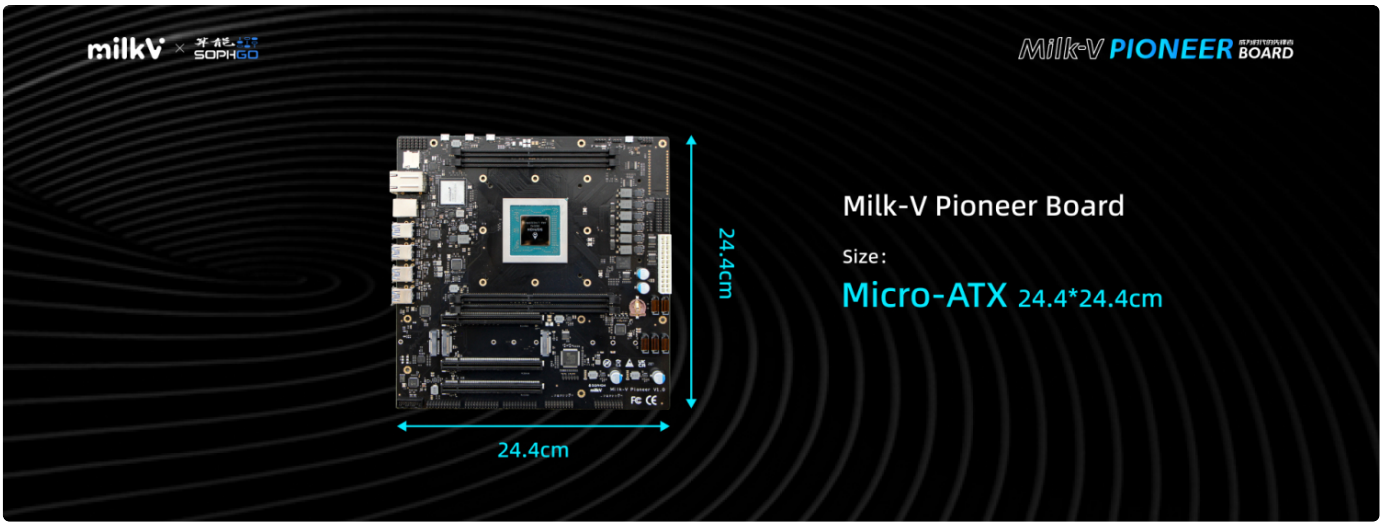
  With the abundant SATA and M.2 MKEY interfaces on the Pioneer Board, you can build a server with massive storage capacity. The 64-core RISC-V processor provides exceptional multiprocessing capabilities. Give it a try by running your services on it – the performance is sure to impress you! You can also connect an Intel X520-2 via the PCIe interface to add dual 10G network ports to your server!

- Be a Switch

  The Pioneer Board provides the option to enhance network capabilities by installing an Intel X520-2 network card, transforming it into a dual-port 10G switch. This optional upgrade allows users to significantly improve their networking performance, enabling faster data transfers and enhanced communication between devices. With the flexibility to add the Intel X520-2 network card, the Pioneer Board offers a powerful and customizable solution for users who require high-speed networking for their projects or applications.

Features

- Micro-ATX form factor



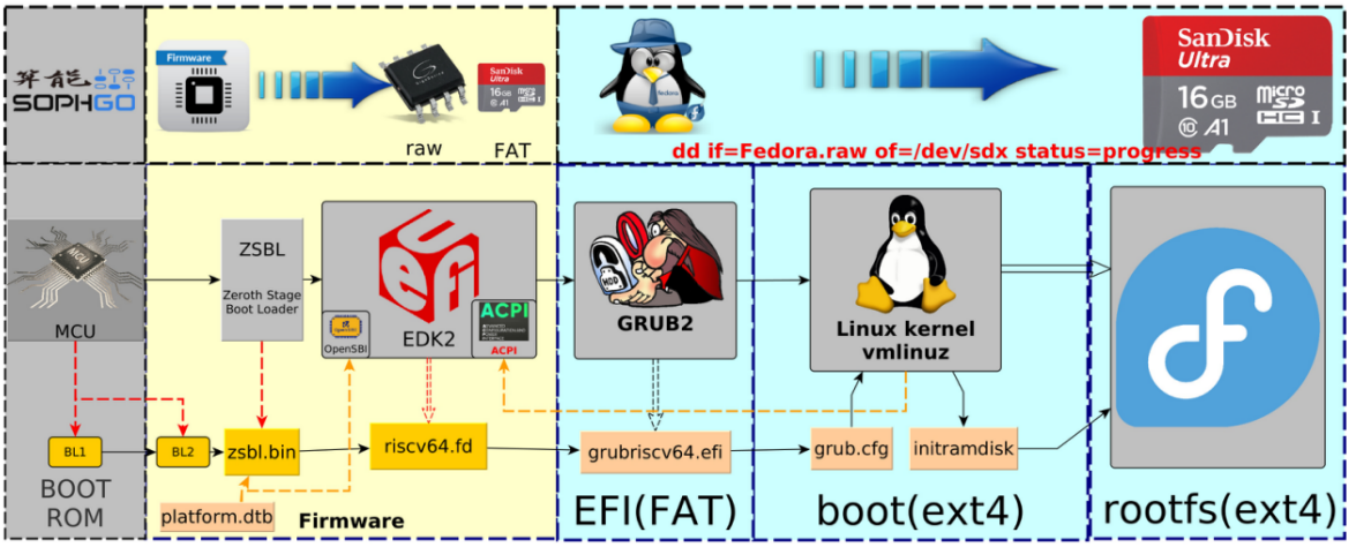
  The Micro-ATX form factor is characterized by its compact size and versatility, offering a balance between space efficiency and expandability. This smaller design allows for more streamlined and space-saving systems, while still providing enough room for sufficient expansion slots and connectivity options. Its compatibility with standard ATX cases and power supplies makes it an attractive choice for a wide range of users and applications.

- Supports UEFI boot

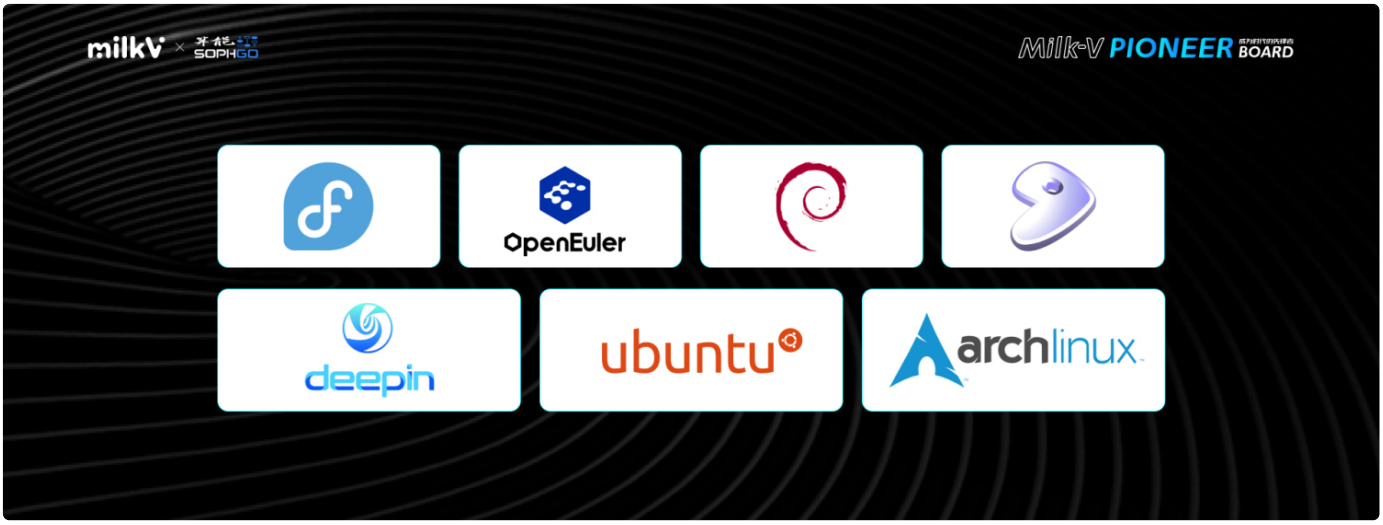
On the firmware, by the efforts of the R&D personnel of Sophgo, the latest OpenSBI mainline code has been successfully boot on the system.

Yixun Lan, the developer of Gentoo, completed the basic porting of U-Boot, and now we can use U-Boot to boot the OS instead of Linuxboot.

As SG2042 is a server-level chip, UEFI/ACPI is usually used as the firmware on servers. the engineers from Sophgo are also working hard to port EDK2 and it will be possible to boot the platform in Q2 this year. The boot flow at that time is as follows:



- Supports various Linux distributions



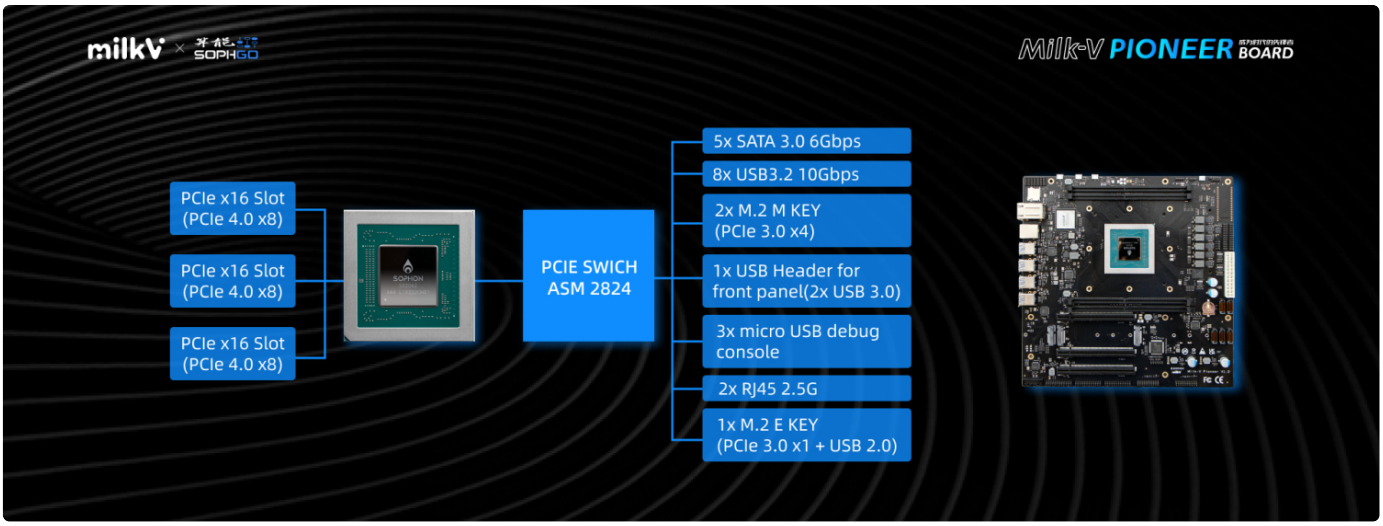
The Pioneer Board supports a wide variety of Linux distributions, allowing you as a user to choose the operating system that best suits your needs and preferences. This compatibility provides you with the flexibility to take advantage of the diverse range of features, tools, and software packages available in different Linux distributions. By supporting various Linux systems, our product enables you to tailor your computing experience according to your specific use cases and requirements, ultimately enhancing your productivity and satisfaction.

- Optimized for 64-core performance

//多核优化测试图

The SG2042 chip is specifically optimized for 64-core performance, providing several advantages to users. With 64 cores integrated into the SG2042, it is capable of handling a significant number of simultaneous tasks, delivering exceptional multi-threading and parallel processing capabilities. This enables you to efficiently run multiple applications or processes on devices equipped with the SG2042, reducing wait times and enhancing overall system performance. Whether you're running demanding workloads, complex simulations, or resource-intensive applications on devices powered by the SG2042, the chip's 64-core optimization ensures a smooth and responsive computing experience.

- Powerful onboard interfaces



The Pioneer Board is designed with a diverse range of powerful and versatile interfaces, making it an ideal choice for various applications and use cases. The onboard interfaces include 2x RJ45 2.5G for fast network connectivity, 5x SATA 3.0 6Gbps for high-speed storage devices, 2x M.2 M KEY (PCIe 3.0 x4) and 1x M.2 E KEY (PCIe 3.0 x1 + USB 2.0) for flexible SSD and expansion card options, 8x USB3.2 10Gbps for ultra-fast data transfers, 3x micro USB debug console for easy debugging, and 2x JTAG debug port for advanced debugging capabilities. These comprehensive connectivity options provide users with the flexibility to create tailored solutions and maximize the potential of the Pioneer Board for various computing needs.

- High-performance RISC-V compiler and hardware-software co-design kit

  兆松科技推出的ZCC编译器套件已全面支持算丰SG2042 RISC-V服务器芯片，这套工具集支持RISC-V敏捷芯片设计，开发和验证，并且全面支持RISC-V软件开发，调试，仿真，性能分析，以及软硬件协同仿真和验证。在SPECInt2006服务器基准测试中，zcc编译器可以让SG2042的单核性能平均提升15%以上；在一些常用的AI算子库自动向量化性能测试中，zcc自动向量化的算子库相较于手写RVV builtin算子库平均有18%的性能改进，相较于开源GCC和LLVM RISC-V编译器，zcc最高可以提升100倍的的性能。随着zcc OpenMP自动并行化对SG2042的支持，使用zcc高性能编译器不仅可以取得最好的单核和多核性能，更可以大幅降低RISC-V函数库和AI算子库的维护成本。

  ZCC toolchain from Terapines has fully supported SG2042 RISC-V chip, this toolset supports agile chip design, develoment and verification for RISC-V based SoC, also fully supports RISC-V software development, debugging, simulation, profiling & performance analysis, software/hardware co-design and co-verification. zcc can increase the single core performance of SG2042 by 15% in average in SPECInt2006 benchmark. zcc also greatly improves the performance of AI kernels, in a benchmark of popular AI kernels, zcc auto-vectorized kernels show 18% average improvements against hand optimized kernels written in RVV builtins, zcc auto-vectorized kernels show at most 100 times performance improvements against kernels compiled by open source GCC and LLVM RISC-V compilers. With the adoption of OpenMP auto-parallelization for SG2042, using zcc can not only achieve the best single core performance and multi-thread throughput, but can also greatly reduce the cost of maintaining libraries and AI kernels for RISC-V.

Enjoy it,Pioneers!

//各种使用图片，实拍，视频

Support for Pioneer Board

High performance RISC-V compiler and software/hardware co-design toolchain

兆松科技推出的ZCC编译器套件已全面支持算丰SG2042 RISC-V服务器芯片，此套件包含的高性能C/C++/Fortran编译器zcc，DSP函数库libml, 调试器zdb，ISA和周期精准仿真器zemu，性能分析工具zprof，虚拟模型建模工具zvboard，车规安全检测工具zchecker，高性能HDL逻辑仿真器zvc， 集成开发环境zstudio等，这套工具集支持RISC-V敏捷芯片设计，开发和验证，并且全面支持RISC-V软件开发，调试，仿真，性能分析，以及软硬件协同仿真和验证。

ZCC toolchain from Terapines has fully supported SG2042 RISC-V chip, the toolchain includes high performance C/C++/Fortran compiler zcc, DSP library libml, debugger zdb, ISA and Cycle accurate simulator zemu, Performance analysis tool zprof, virtual prototyping toolset zvboard, functional safety rule checker zchecker, high performance HDL logic simulator zvc, integrated development environment zstudio

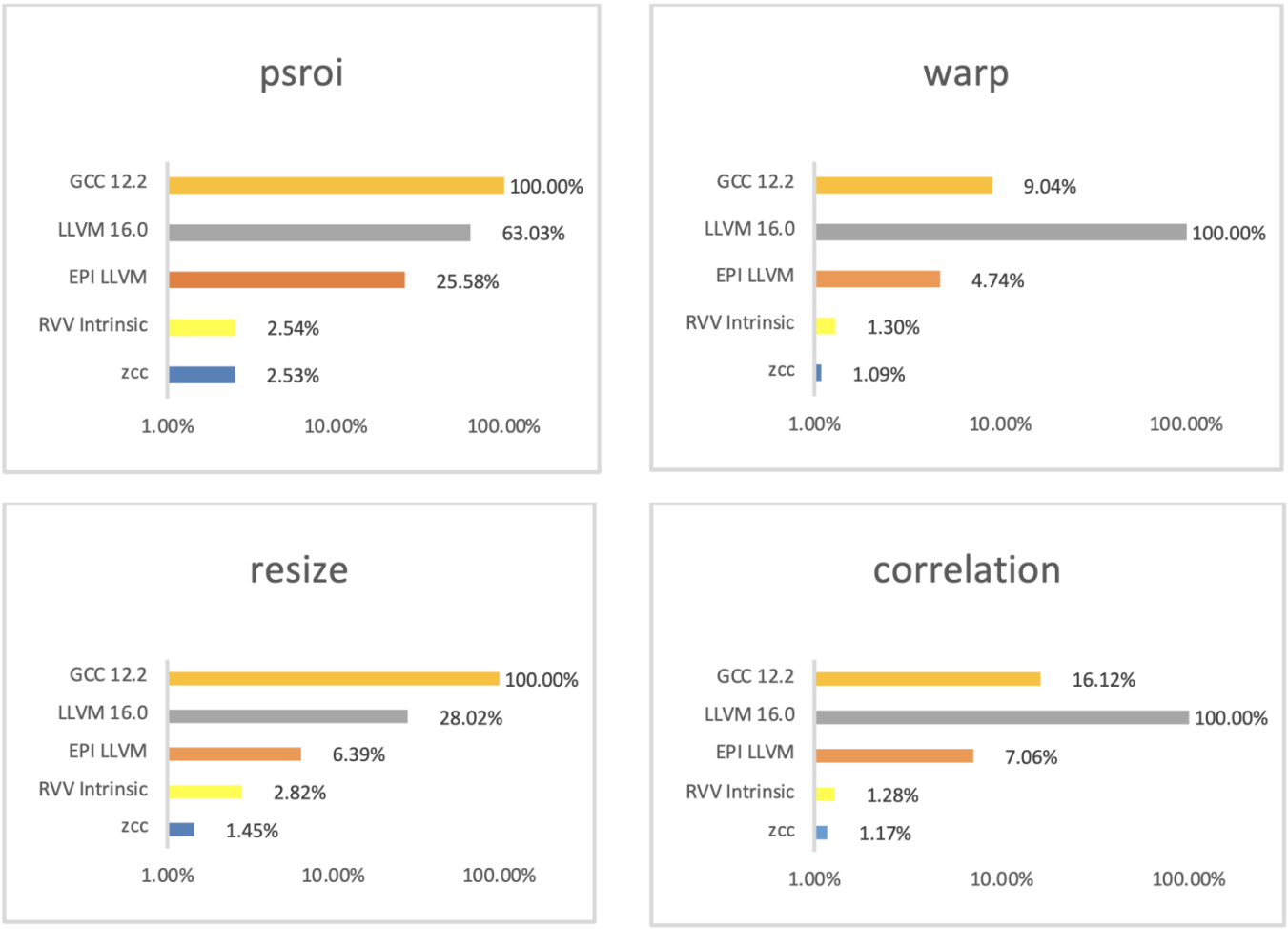
etc. This toolset supports agile chip design, develoment and verification for RISC-V based SoC, also fully supports RISC-V software development, debugging, simulation, profiling & performance analysis, software/hardware co-design and co-verification.

兆松科技研发的zcc高性能编译器不仅针对服务器应用和AI应用，做了大量的优化，也对代码密度做了大量的优化。我们以SPECInt2006作为HPC的基准性能测试用例，指令集使用RV64GC，开启O3优化以及链接时优化选项，在不包括RVV自动向量化的优化情况下，zcc得分比GCC 12.2和LLVM 16平均好10%，在引入RVV自动向量化的情况下，zcc相对于GCC 12.2和LLVM 16有超过15%的性能优势。

Terapines zcc compiler is not only optimized for HPC and AI applications, but is also optimized for code size for embedded applications. We evaluated the performance of zcc against GCC and LLVM, zcc shows average 10% better performance in SPECInt2006 than GCC 12.2 and LLVM 16 does for RV64GC with O3 and LTO enabled. zcc shows more than 15% better performance in SPECInt2006 than GCC 12.2 and LLVM 16 does for RV64GCV with O3 and LTO enabled.

除了针对标准的SPECInt2006进行性能评估之外，我们还针对一些流行的AI算子库进行了自动向量化的性能评估，如下图所示，我们使用了zcc, LLVM, EPI LLVM, GCC分别对psroi, warp, resize和correlation 4个AI算子进行了自动向量化，并且我们和手写RVV内敛函数（RVV Intrinsic)的算子库做了横向的动态指令数的对比，可以看出，使用zcc自动向量化的算子库，平均比手写RVV内敛函数的算子库性能提升18%，比EPI LLVM (9cfcff6873) 最高提升10倍，比LLVM 16最高提升100倍，比GCC 12.2最高提升69倍。这4个算子库的C源代码，RVV内敛汇编源代码，编译选项可以在 https://github.com/dodohack/rv_lib <https://github.com/dodohack/rv_lib> 找到。

We have also benchmarked some popular AI kernels in addition to SPECInt2006. As shown in below, we have evaluated the auto-vectorization performance of zcc, LLVM, EPI LLVM, GCC against 4 kernels includes psroi, warp, resize and correlation, we have also compared the dynamic instruction count agaist hand optimized kernels written with RVV builtins. zcc shows 18% average better performance against hand optimized kernels, at most 10 times faster than EPI LLVM (9cfcff6873), 100 times faster than LLVM 16 and 69 times faster than GCC 12.2. You can find the source code and build commands of these 4 kernels from https://github.com/dodohack/rv_lib <https://github.com/dodohack/rv_lib> .



相对动态指令数，数据越小越好

Dynamic instruction count, lower is better

zcc编译器不仅支持RVV 1.0的多层循环自动向量化，也即将推出支持算丰SG2042的RVV 0.71的多层循环自动向量化。自动向量化完美诠释RISC-V Vector扩展在HPC应用，AI推理和训练上的性能优势和代码移植性优势；兆松目前已经完成对RVV 0.71的指令编码，汇编和反汇编等支持，并已全部开源，完整源码可在 https://github.com/Terapines/llvm-project <https://github.com/Terapines/llvm-project> 查看，后续对RVV 0.71 builtins的支持，也将开源到此仓库。

zcc does not only support multi-level loops auto-vectorization for RVV 1.0, it also will support auto-vectorization for RVV 0.71 on SG2042 in near future. Auto-vectorization fully exposes the performance and portability potential of RISC-V scalable vector extension on HPC, AI training and inference applications. Terapines has already implemented instruction encoding, assembler and disassembler for RVV 0.71, and open-sourced it on https://github.com/Terapines/llvm-project <https://github.com/Terapines/llvm-project> , the support of RVV 0.71 builtins will be open-sourced to this repository as well.

作为第一款64核RISC-V服务器CPU，在兆松高性能zcc编译器的加持下，随着zcc OpenMP自动并行化对SG2042芯片的支持，使用zcc编译器不仅可以取得最好的单核和多核性能，更可以大幅降低RISC-V函数库和AI算子库的维护成本。

As the first 64 core RISC-V server CPU, with the support of Terapines high performance zcc compiler, with the adoption of OpenMP auto-parallelization for SG2042, using zcc can not only achieve the best single core performance and multi-thread throughput, but can also greatly reduce the cost of maintaining libraries and AI kernels for RISC-V.

Fedora Helps to enrich Pioneer Board Software Ecosystem

运行复杂的操作系统，可以综合验证开发板的各项功能和模块间的协同，更好地发现潜在的问题。在 Pioneer Board 的调试验证阶段，Fedora系统就被用作目标测试系统。

如今在 Pioneer Board 上，Fedora系统已经可以稳定运行 LXDE、XFCE 和 GNOME桌面环境，并获得了丰富的软件生态支持，如podman、Libreoffice办公软件，Firefox浏览器、音乐和视频播放等等，甚至可以玩很多Linux下的经典3D游戏，就像一台Linux PC一样。此外，Fedora系统上还可以运行ROS2系统，为今后更多的人工智能和机器人方向的应用在 Pioneer Board 上打下坚实的基础。

Fedora镜像使用方便，只需一个"dd"命令刷入TF 卡便可启动到桌面系统。整个启动流程也尽可能遵循当前RISC-V系统的通用启动流程，可作为其他OS启动和对比测试的参照，很好地助力其他OS镜像的开发。

Running complex OS can comprehensively validate the various functions and modules of the development board and discover potential problems more effectively. In the debugging and verification stage of the Pioneer Board, the Fedora was used as the target testing OS.

Nowadays, the Fedora system can run LXDE, XFCE, and GNOME desktop environments stably on the Pioneer Board, and has obtained rich software ecosystem support, such as podman, Libreoffice, Firefox browser, music and video playback, even many classic 3D video games on Linux, just like a Linux PC. In addition, the Fedora system can also run ROS2, laying a solid foundation for AI and robotics applications on the Pioneer Board.

The Fedora image is easy to use, and only requires a "dd" command to be written onto an SD card, then Milk-V can boot into the GUI desktop. The entire boot flow follows the universal boot flow for current RISC-V systems as much as possible. it can be a reference for other OS on booting and comparative testing, which greatly helps in the development of other OS images.

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1. 吴伟 10分钟 《全体起立，迎接一百万RISC-V开发者用户》
2. Pioneer Board 产品发布 20分钟 《从Pioneer Board开始，拥抱RISC-V生态》
3. SOPHGO2042芯片介绍 10分钟
4. 魏超（算能）10分钟
5. 傅炜（Fedora）20分钟 算丰服务器平台部署Linux发行版 -- Fedora部署实践
6. 雷依钒（兆松）20分钟 高性能RISC-V编译器及软硬件协同设计套件

   雷依钒个人介绍：兆松科技软件仿真器组组长。