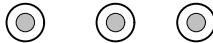


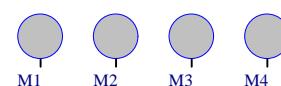
Rev	Description	Date (DD/MM/YY)	Author
1.0	Initial Release.	01/07/20	Yan C. de Azeredo
2.0	Adding fourth PCB "4_iip_closure" and "4_iip_camera" PCBs, updating mounting holes pads, block diagram, SpaceLab logo and layout of N°3 IIP board.	28/06/21	Yan C. de Azeredo

### Revision History

Fiducials



Mechanical Holes



### PCB Elements

Insterstage Interface Panels for a 2U or 3U CubeSat

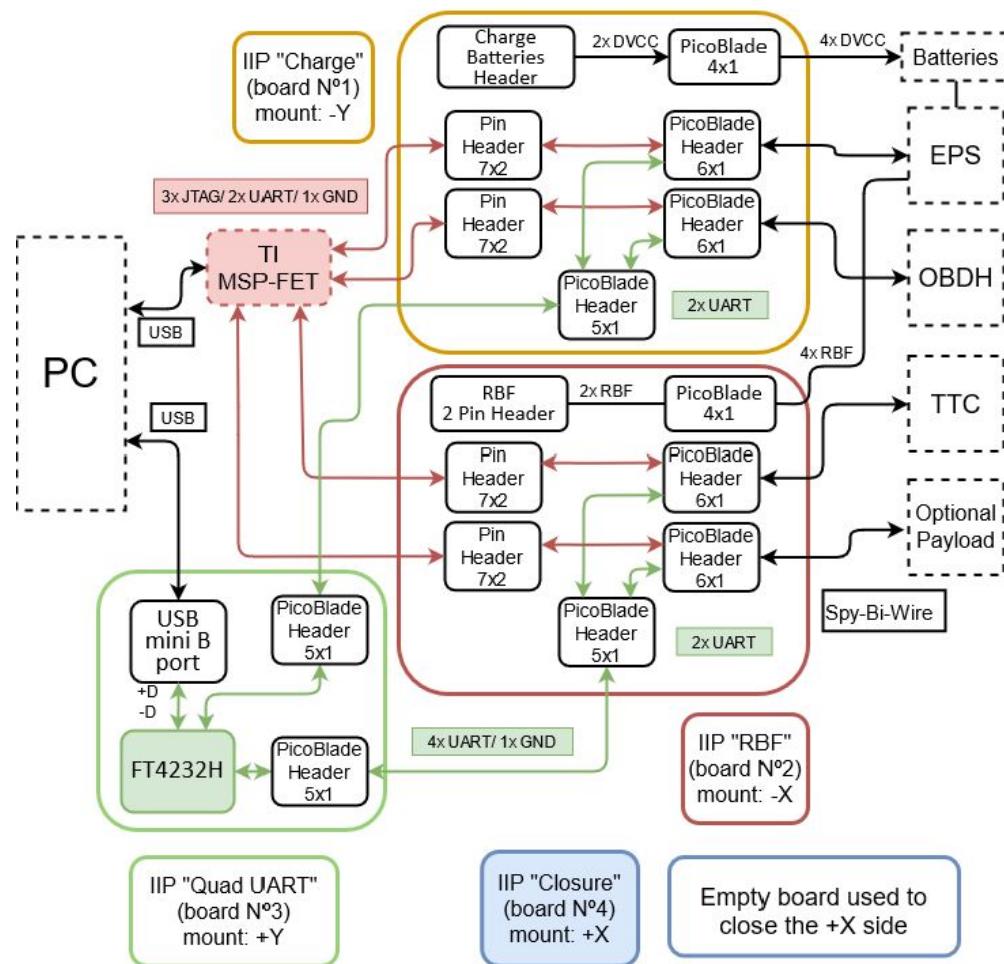
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To view a copy of this license, visit  
<https://ohwr.org/project/cernohl/wikis/Documents/CERN-OHL-version-2>.

- Designed by: Yan Castro de Azeredo
- Reviewers: Gabriel M. Marcelino and André M. P. Mattos
- Support: Gabriel M. Marcelino, André M. P. Mattos and Kleber Gouveia
- Mechanical validation: Edemar M. Filho and Caique S. M. Gomes

### Project Information

## Interstage Interface Panels



## Full System Block Diagram

SpaceLab - Federal University of Santa Catarina	
Project: <a href="#">3_iip_quad_uart.PnjPCB / [No Variations]</a>	
Title: <a href="#">IIP Hardware Architecture</a>	
Designed by: Yan Castro de Azeredo	

Date: 7/1/2021 Revision: 2.0 Sheet 1 of 2 Project Code: IIP Size: A4

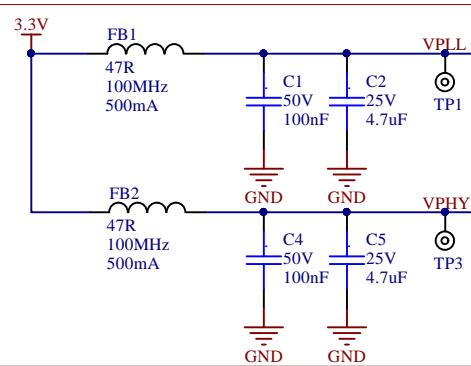
1

2

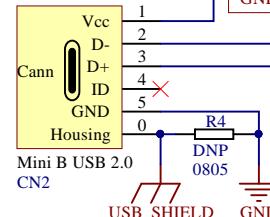
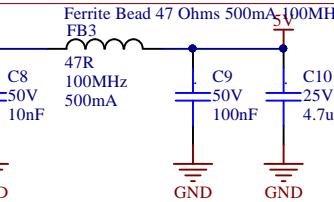
3

4

### Low pass LC filters for VPLL and VPHY

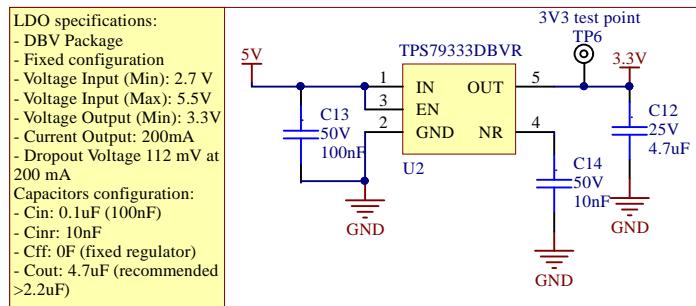


### USB VBUS Filter

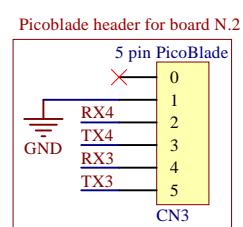
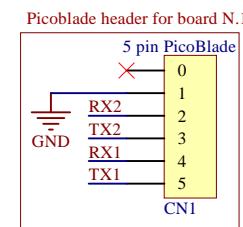
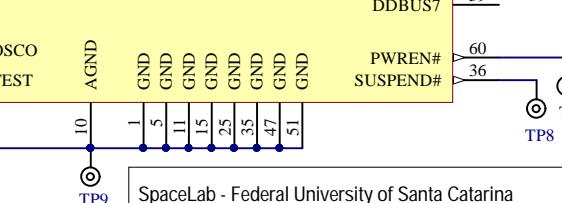
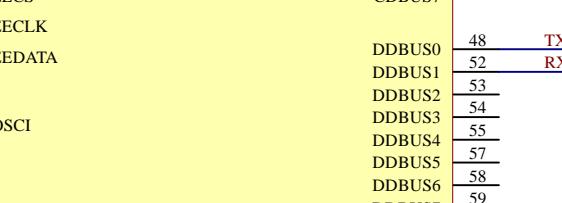
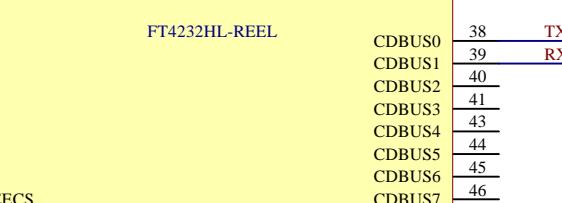
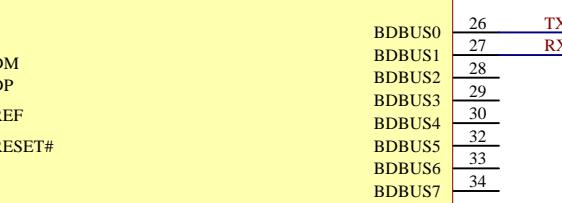
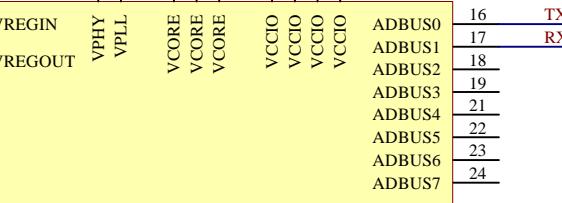
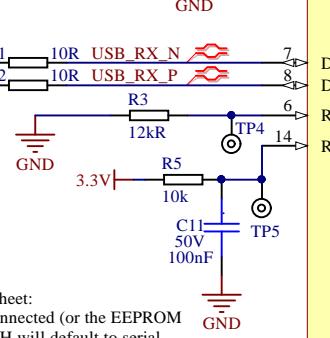
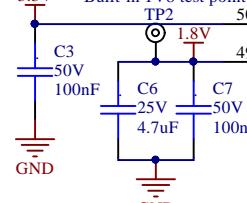
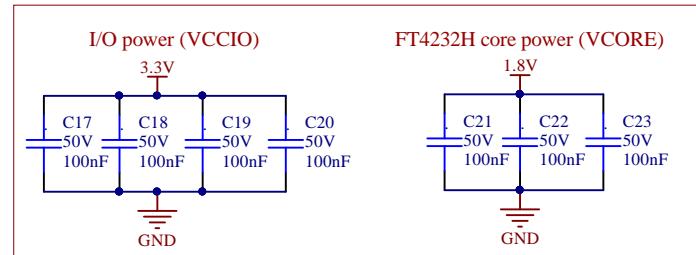


Optional zero-ohm resistor for a DC path, or capacitor for a high-frequency path between shield and signal ground to minimize signal noise and provide EMC compatibility (to be tested if required).

### Linear Voltage Regulator for VREGIN (LDO)



### Decoupling Capacitors



Testpoints for debugging IC  
PWREN#=0: Normal operation.  
PWREN#=1: USB SUSPEND mode or device has not been configured.  
SUSPEND#: Active low when USB is in suspend mode.

SpaceLab - Federal University of Santa Catarina

Project: [3\\_iip\\_quad\\_uart.PnjPCB / \[No Variations\]](#)

Title: [IIP N3 Board Interfaces and FT4232 Circuit](#)

Designed by: Yan Castro de Azevedo



Project Code: [IIPN3](#)

Date: [7/1/2021](#) Revision: [2.0](#) Sheet [2](#) of [2](#) Size: [A4](#)

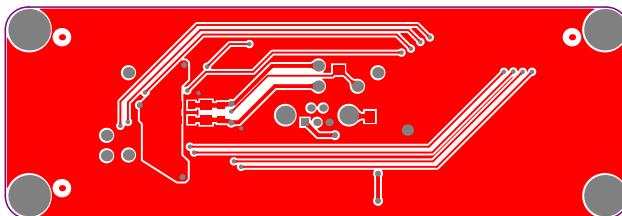
1

2

3

4

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.8	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	59.06mil	4.5	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.8	
7	Bottom Overlay				



#### Fabrication specifications:

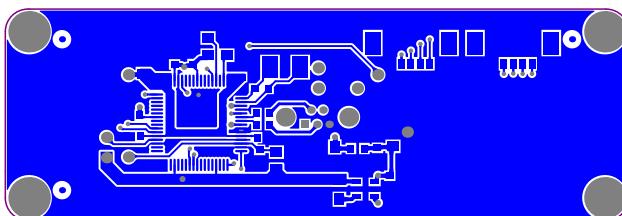
- Copper base: 1oz
- PCB Material: Prepeg FR4—Standard
- PCB Thickness: 1.6mm
- PCB Surface: HASL (with lead)
- Silkscreen Color: White (top and bottom)
- Soldermask Color: Green
- Vias: Force Complete Tenting
- Stack-up: Table herein included
- Special requirements: None

#### Assembly specifications:

- Solder composition: Include lead
- Fiducials: 3 top and 3 bottom available

SpaceLab - Federal University of Santa Catarina	
Project: Interstage Interface Panel N°3	
Layer: <b>Top Layer</b> Board edge	
Designed by: Yan C. de Azeredo	Project Code: IIP3
Date: 7/1/2021	Version: v2.0
	Size: A4

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.8	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	59.06mil	4.5	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.8	
7	Bottom Overlay				



#### Fabrication specifications:

- Copper base: 1oz
- PCB Material: Prepeg FR4—Standard
- PCB Thickness: 1.6mm
- PCB Surface: HASL (with lead)
- Silkscreen Color: White (top and bottom)
- Soldermask Color: Green
- Vias: Force Complete Tenting
- Stack-up: Table herein included
- Special requirements: None

#### Assembly specifications:

- Solder composition: Include lead
- Fiducials: 3 top and 3 bottom available

SpaceLab - Federal University of Santa Catarina	
Project: Interstage Interface Panel N°3	
Layer: Bottom Layer Board edge	
Designed by: Yan C. de Azeredo	Project Code: IIP3
Date: 7/1/2021	Version: v2.0
	Size: A4

A

A

B

B

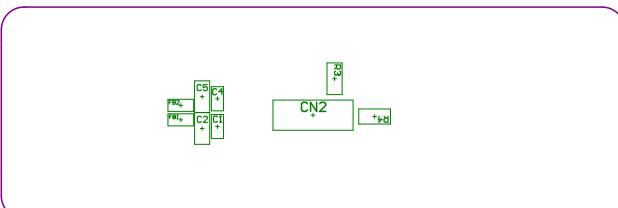
C

C

D

D

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.8	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	59.06mil	4.5	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.8	
7	Bottom Overlay				



### Fabrication specifications:

- Copper base: 1oz
- PCB Material: Prepeg FR4—Standard
- PCB Thickness: 1.6mm
- PCB Surface: HASL (with lead)
- Silkscreen Color: White (top and bottom)
- Soldermask Color: Green
- Vias: Force Complete Tenting
- Stack-up: Table herein included
- Special requirements: None

### Assembly specifications:

- Solder composition: Include lead
- Fiducials: 3 top and 3 bottom available

SpaceLab - Federal University of Santa Catarina	
Project: Interstage Interface Panel Nº3	
Layer: Top ASM      Board edge	
Designed by: Yan C. de Azeredo	
Date: 7/1/2021	Project Code: IIP3
Version: v2.0	Size: A4

A

A

B

B

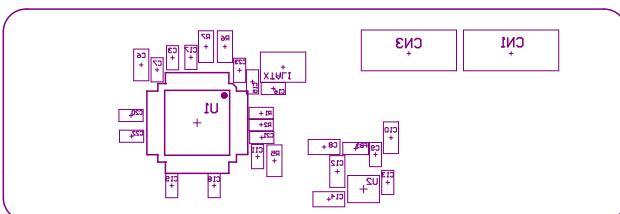
C

C

D

D

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.8	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	59.06mil	4.5	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.8	
7	Bottom Overlay				



#### Fabrication specifications:

- Copper base: 1oz
- PCB Material: Prepeg FR4—Standard
- PCB Thickness: 1.6mm
- PCB Surface: HASL (with lead)
- Silkscreen Color: White (top and bottom)
- Soldermask Color: Green
- Vias: Force Complete Tenting
- Stack-up: Table herein included
- Special requirements: None

#### Assembly specifications:

- Solder composition: Include lead
- Fiducials: 3 top and 3 bottom available

SpaceLab - Federal University of Santa Catarina



Project: Interstage Interface Panel Nº3

Layer: Bottom ASM Board edge

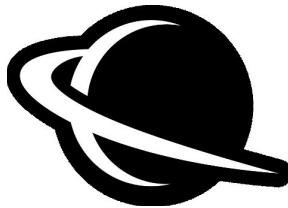
Designed by: Yan C. de Azeredo

Project Code: IIP3

Date: 7/1/2021

Version: v2.0

Size: A4



## Bill of Materials

Source Data From: 3\_iip\_quad\_uart.PrjPCB

Project: 3\_iip\_quad\_uart.PrjPCB

Variant: None

Project Code: IIPN3

Report Date: 7/1/2021 12:12:55 AM

Print Date: 01/07/2021 00:13:04

#	Designator	Quantity	Manufacturer	Manufacturer Part Number	Description	Part Number	Focus	Error	Fitted
1	C1, C3, C4, C7, C9, C11, C13, C17, C18, C19, C20, C21, C22, C23	14		C1608X7R1H104K080AA	TDK - C1608X7R1H104K080AA - SMD Multilayer Ceramic Capacitor, 0.1 µF, 50 V, 0603 [1608 Metric], ± 10%, X7R, C Series				Fitted
2	C2, C5, C6, C10, C12	5		C2012X7R1E475K125AB	Ceramic Capacitor SMD Multilayer, 0805 [2012 Metric], 4.7 uF, 25 V, 10%, X7R, C Series				Fitted
3	FB1, FB2, FB3	3		742792608	WURTH ELEKTRONIK 742792608 FERRITE BEAD, 0.1 OHM, 0.5A, 0603				Fitted
4	R5, R6, R7	3		CRCW080510K0FKEA	RES 10.0K OHM 1/8W 1% 0805 SMD				Fitted
5	C8, C14	2		08055C103KAT4A	AVX - 08055C103KAT4A - SMD Multilayer Ceramic Capacitor, 10000 pF, 50 V, 0805 [2012 Metric], ± 17%; 10%, X7R				Fitted
6	CN1, CN3	2		53398-0571	Wire-To-Board Connector, Vertical, PicoBlade 53398 Series, Surface Mount, Header, 5, 1.25 mm				Fitted
7	C15, C16	2		CL10C120JB8NNNC	Cap Ceramic 12pF 50VDC COG 5% SMD 0603 Paper T/R				Fitted
8	R1, R2	2		RC0603FR-0710RL	YAGEO (PHYCOMP) - RC0603FR-0710RL - RES, THICK FILM, 10R, 1%, 0.1W, 0603				Fitted
9	CN2	1		651005136421	WURTH ELEKTRONIK - 651005136421 - Conector USB, Mini USB Tipo B, USB 2.0, Receptáculo, 5 Vias, Montaje de Agujero Pasante, Vertical				Fitted
10	XTAL1	1		AA-12.000MAGE-T	Crystals 12.000MHz 30ppm 12pF -40C to 85C				Fitted
11	R4	1		CRCW08050000Z0EA	VISHAY - CRCW08050000Z0EA - SMD Chip Resistor, Jumper, 0805 [2012 Metric], 0 ohm, CRCW e3 Series, 150 V, Thick Film, 125 mW				Fitted
12	U1	1		FT4232HL-REEL	FTDI - FT4232HL-REEL - USB-UART/MPSSE, 4232, QUAD, 64LQFP				Fitted
13	R3	1		RMCF0805FT12K0	Resistor, SMT, 0805, 12K Ohm, +/-1%, +/-10ppm, Thk Film, T/R Marked				Fitted
14	U2	1		TPS79333DBVR	TEXAS INSTRUMENTS - TPS79333DBVR - IC, V REG, LINEAR, 0.2A, SOT-23-5				Fitted