| Rev | Description | Date | Author |
|-----|-------------|------|--------|
| 1.0 | Initial Release. | 01/07/20 | Yan C. de Azeredo |
|     |             |      |        |
|     |             |      |        |
|     |             |      |        |

## Revision History

## Fiducials

FD1  FD2  FD3

## Mechanical Holes

M1  M2  M3  M4
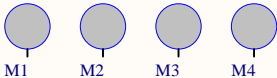
## PCB Elements

Semi USB Insterstage Interface Panels of FloripaSat-2 2U CubeSat

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- Drawn by: Yan Castro de Azeredo
- Reviewers: Gabriel M. Marcelino and André M. P. Mattos
- Support: Gabriel M. Marcelino, André M. P. Mattos and Kleber Gouveia
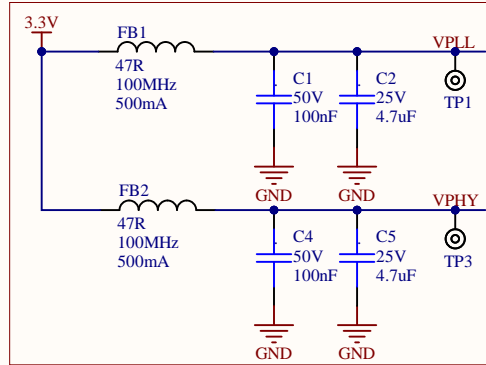- Mechanical validation: Edemar Morsch Filho

## Project Information
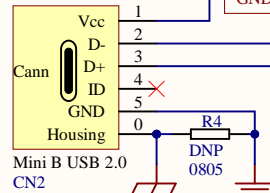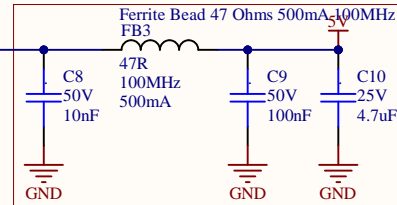


Semi USB Interstage Interface Panels

Full System Block Diagram

# Low pass LC filters for VPLL and VPHY

3.3V — FB1 47R 100MHz 500mA — VPLL
C1 50V 100nF — GND
C2 25V 4.7uF — GND
TP1

FB2 47R 100MHz 500mA — VPHY
C4 50V 100nF — GND
C5 25V 4.7uF — GND
TP3

# USB VBUS Filter

5V — Ferrite Bead 47 Ohms 500mA 100MHz
FB3 47R 100MHz 500mA
C8 50V 10nF — GND
C9 50V 100nF — GND
C10 25V 4.7uF — GND

**Cann** Mini B USB 2.0 CN2
1 Vcc
2 D-
3 D+
4 ID
5 GND
Housing
0 — R4 DNP 0805
USB_SHIELD GND

USB_TX_N
USB_TX_P

Optional zero-ohm resistor for a DC path, or capacitor for a high-frequency path between shield and signal ground to minimize signal noise and provide EMC compatibility (to be tested if required).
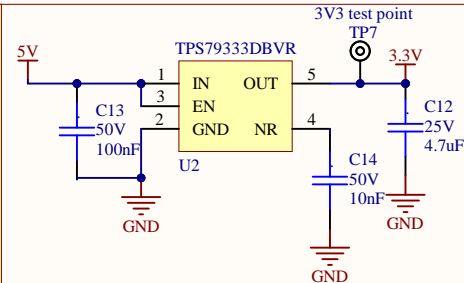
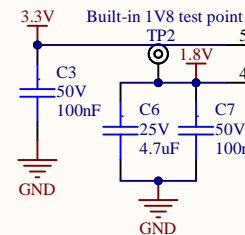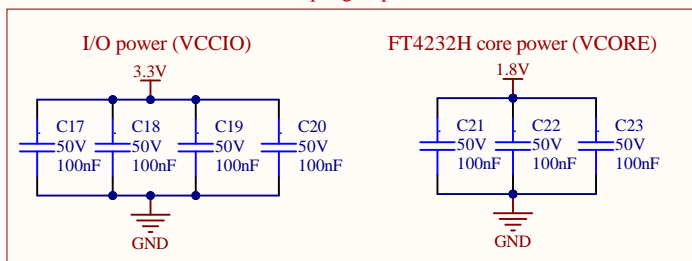# Linear Voltage Regulator for VREGIN (LDO)

LDO specifications:
- DBV Package
- Fixed configuration
- Voltage Input (Min): 2.7 V
- Voltage Input (Max): 5.5V
- Voltage Output (Min): 3.3V
- Current Output: 200mA
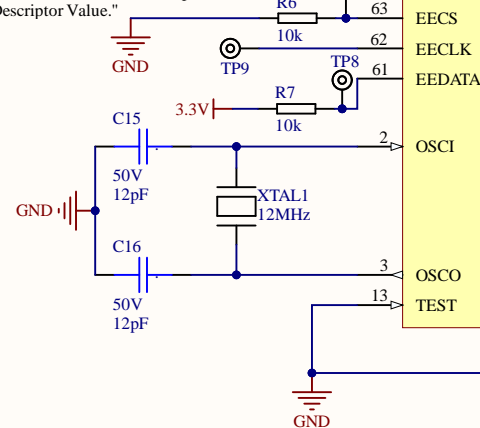- Dropout Voltage 112 mV at 200 mA
Capacitors configuration:
- Cin: 0.1uF (100nF)
- Cinr: 10nF
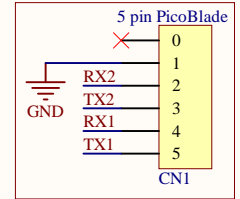- Cff: 0F (fixed regulator)
- Cout: 4.7uF (recommended >2.2uF)

5V — TPS79333DBVR U2
1 IN   OUT 5
3 EN
2 GND  NR 4
C13 50V 100nF — GND
3V3 test point TP7 — 3.3V
C12 25V 4.7uF — GND
C14 50V 10nF — GND

# Decoupling Capacitors

## I/O power (VCCIO)
3.3V
C17 50V 100nF
C18 50V 100nF
C19 50V 100nF
C20 50V 100nF
GND

## FT4232H core power (VCORE)
1.8V
C21 50V 100nF
C22 50V 100nF
C23 50V 100nF
GND

# U1 — FT4232HL-REEL

3.3V — Built-in 1V8 test point TP2 — 1.8V
C3 50V 100nF — GND
C6 25V 4.7uF — GND
C7 50V 100nF — GND

1.8V   3.3V
VPLL
VPHY

50 VREGIN
49 VREGOUT
4 VPHY
9 VPLL
12 VCORE
37 VCORE
64 VCORE
20 VCCIO
31 VCCIO
42 VCCIO
56 VCCIO

R1 10R USB_RX_N — 7 DM
R2 10R USB_RX_P — 8 DP

R3 12kR — 6 REF
TP4 — 14 RESET#
R5 10k — 3.3V
C11 50V 100nF — GND
TP5

ADBUS0 16 — TX1
ADBUS1 17 — RX1
ADBUS2 18
ADBUS3 19
ADBUS4 21
ADBUS5 22
ADBUS6 23
ADBUS7 24

BDBUS0 26 — TX2
BDBUS1 27 — RX2
BDBUS2 28
BDBUS3 29
BDBUS4 30
BDBUS5 32
BDBUS6 33
BDBUS7 34

CDBUS0 38 — TX3
CDBUS1 39 — RX3
CDBUS2 40
CDBUS3 41
CDBUS4 43
CDBUS5 44
CDBUS6 45
CDBUS7 46

DDBUS0 48 — TX4
DDBUS1 52 — RX4
DDBUS2 53
DDBUS3 54
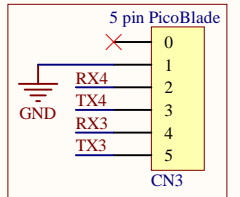DDBUS4 55
DDBUS5 57
DDBUS6 58
DDBUS7 59

From FT4232H datasheet:
"If no EEPROM is connected (or the EEPROM is blank), the FT4232H will default to serial ports. The device uses its built-in default VID (0403), PID (6011) Product Description and Power Descriptor Value."

R6 10k — 63 EECS
TP6
62 EECLK
TP9
R7 10k — 3.3V — 61 EEDATA
TP8

C15 50V 12pF
XTAL1 12MHz
GND — 2 OSCI
C16 50V 12pF
3 OSCO
13 TEST

PWREN# 60
SUSPEND# 36
TP10
TP11

AGND
GND: 10, 1, 5, 11, 15, 25, 35, 47, 51
TP12
GND

# Picoblade header for board N.1
5 pin PicoBlade CN1
0
1
2
3
4
5
RX2
TX2
RX1
TX1
GND

# Picoblade header for board N.2
5 pin PicoBlade CN3
0
1
2
3
4
5
RX4
TX4
RX3
TX3
GND

Testpoints for debugging IC
PWREN# = 0: Normal operation.
PWREN# =1: USB SUSPEND mode or device has not been configured.
SUSPEND#: Active low when USB is in suspend mode.

SpaceLab - Federal University of Santa Catarina
Project: *3_iip_quad_uart.PrjPCB / [No Variations]*
Title: *IIP N3 Board Interfaces and FT4232 Circuit*
Designed by: *Yan Castro de Azeredo*
Project Code: *IIPN3*
Date: 11/29/2020   Revision: 1.0   Sheet 2 of 2   Size: A4
SPACE LAB