

A

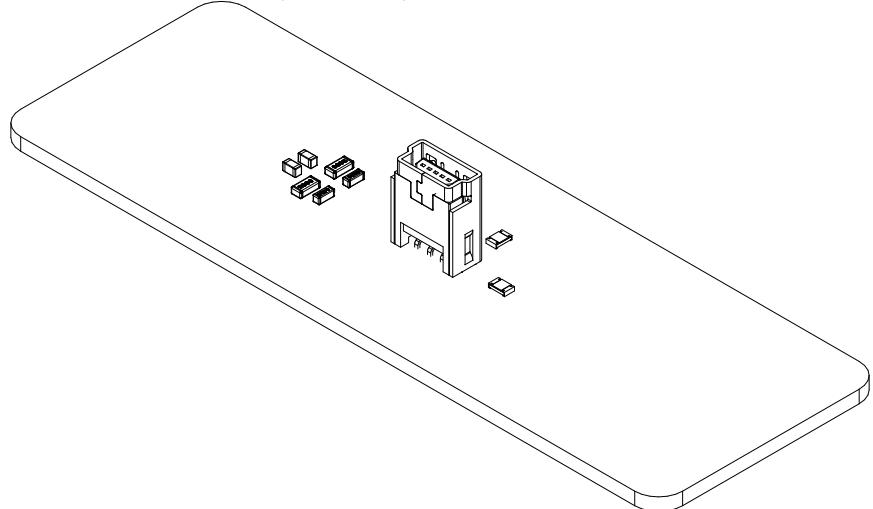
B

C

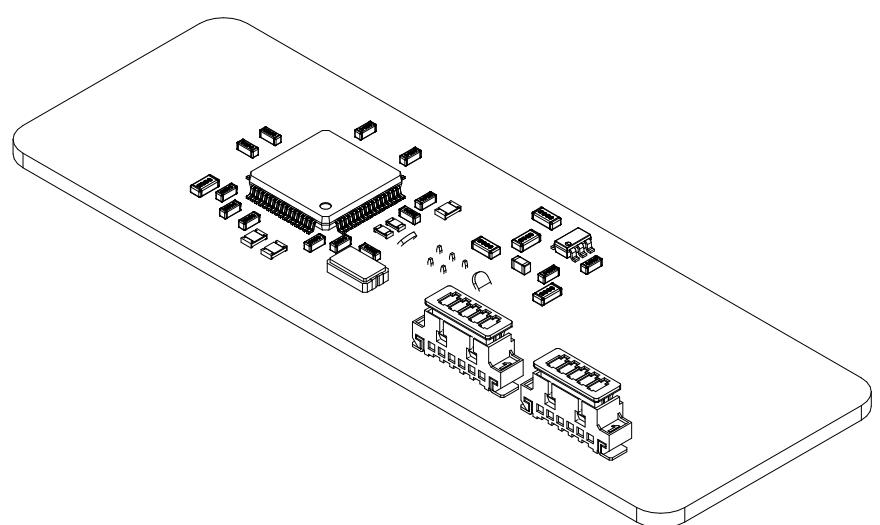
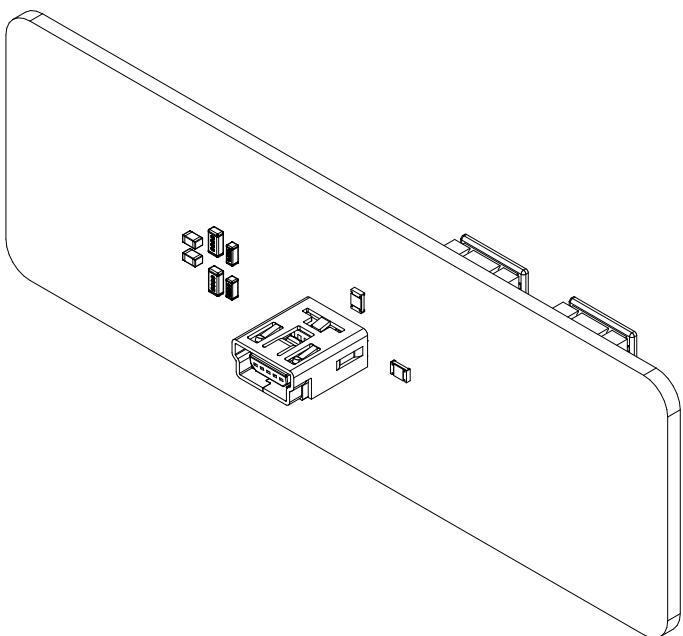
D

E

View from Front side (Scale 1.5)



View from Top side (Scale 1.5)



#### Interstage Interface Panel N°3 "Quad UART" Hardware:

- Designed by: Yan C. de Azeredo.
- Reviewers: Gabriel M. Marcelino and Andre M. P. Mattos.
- Support: Edemar M. Filho and Caique S. M. Gomes

Copyright © 2021 by Universidade Federal de Santa Catarina.

This hardware project is licensed under CERN-OHL-S, version 2.

Github repository: <https://github.com/spacelab-ufsc/interface-board>

More info about SpaceLab: <https://spacelab.ufsc.br/>

View from Back side (Scale 1.5)

SpaceLab - Federal University of Santa Catarina

Project: Interstage Interface Panel N°3

Title: Project info and board isometric views

Designed by: Yan Castro de Azeredo

Date: 7/1/2021 Version: 2.0 Sheet 1 of 3

**SPACELAB**

Project code: IIPN3

Sheet size: A4

A

B

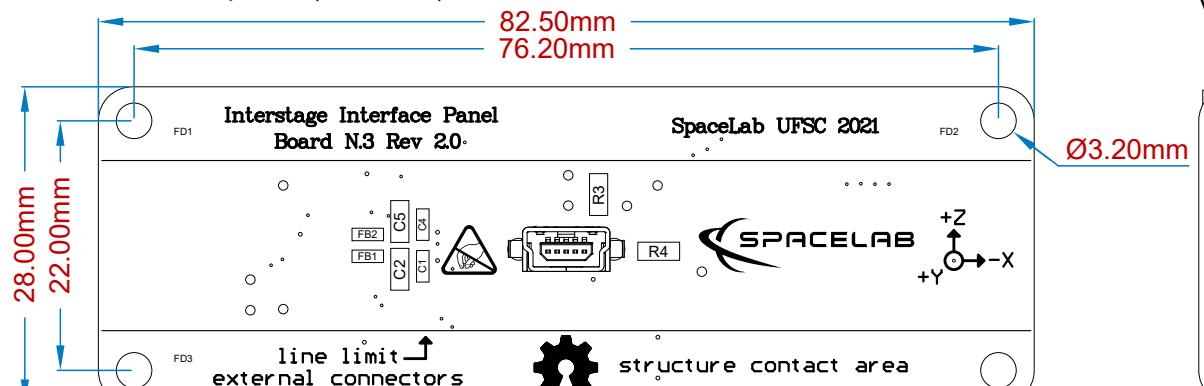
C

D

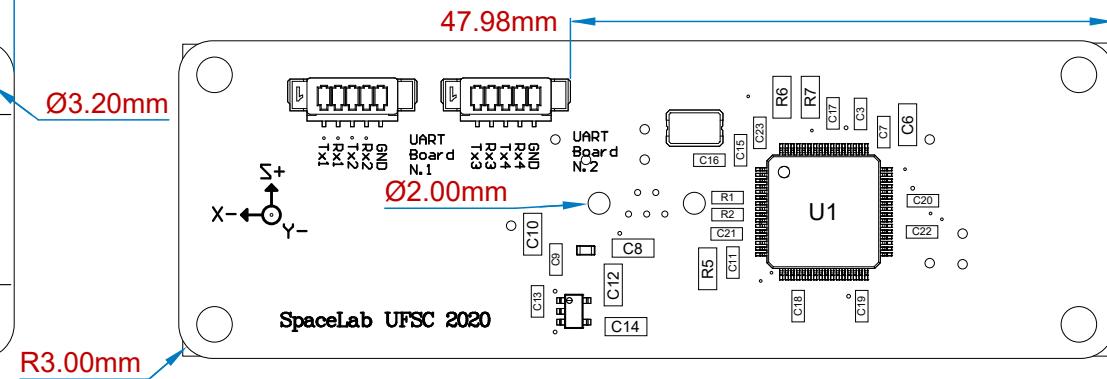
E

Displayed components within a red mesh box   
are not supposed to be soldered in the flight model of the board.

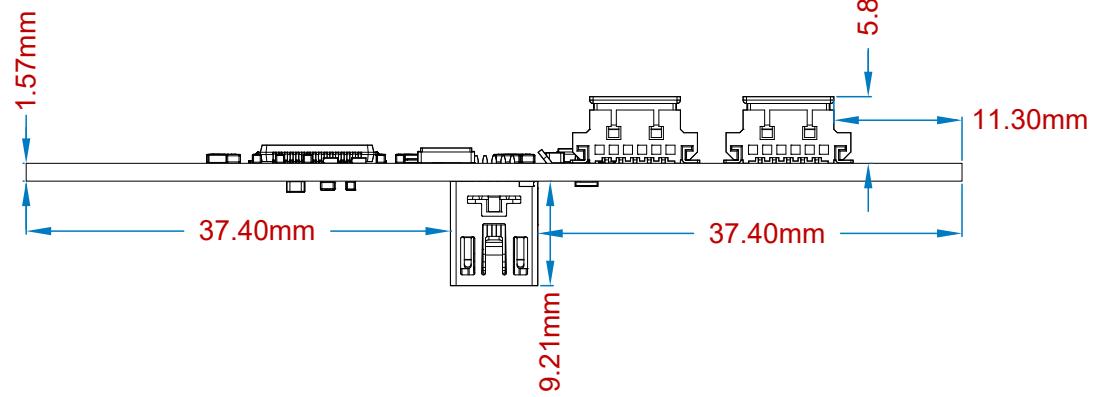
View from Top side (Scale 1.5)



View from Bottom side (Scale 1.5)



View from Back side (Scale 1.5)



SpaceLab - Federal University of Santa Catarina

Project: Interstage Interface Panels N°3

Title: Assembly components and mechanical dimensions

Designed by: Yan Castro de Azeredo

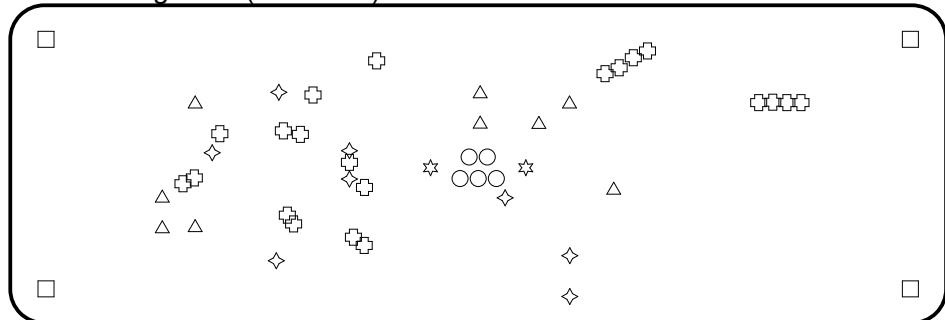
Date: 7/1/2021 Version: 2.0 Sheet 2 of 3



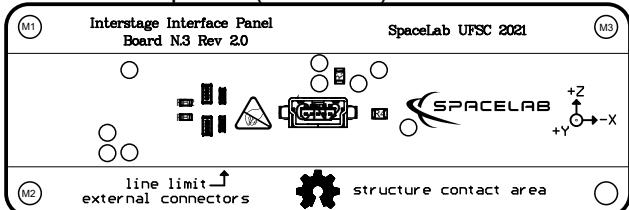
Project code: IIPN3

Sheet size: A4

## A Drill Drawing View (Scale 1.5)



## E View from Top side (Scale 1:1)



## B Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Paste			Paste Mask	GTP
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.04mm		Signal	GTL
		1.50mm	FR-4	Dielectric	
Copper	Bottom Layer	0.04mm		Signal	GBL
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
	Bottom Paste			Paste Mask	GBP

Total thickness: 1.59mm

## D Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
+	21	0.30mm	Plated	None
◊	8	0.40mm	Plated	None
○	5	0.60mm	Plated	None
△	9	0.90mm	Plated	None
☆	2	2.00mm	Plated	None
□	4	3.20mm	Plated	None
49 Total				

SpaceLab - Federal University of Santa Catarina

Project: Interstage Interface Panel N°3

Title: Layer stack and drill tables

Designed by: Yan Castro de Azereedo

Project code: IIPN3

Date: 7/1/2021 Version: 2.0 Sheet 3 of 3

Sheet size: A4