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Documentation of Interstage Interface Panels

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SpaceLab, Universidade Federal de Santa Catarina, Florianópolis - Brazil

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1.0	Yan C. de Azeredo	First release	12/2020
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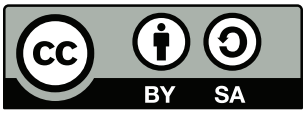

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CHAPTER 1

Introduction

The Interstage Interface Panels (IIP) are three vertical internally mounted PCBs designed to give external access up to four modules inside of a 2U CubeSat during final assembly, integration and testing (AIT) before launch. The complete set of the boards allow the nanosatellite to be charged, programed and debugged. The usage of this hardware platform is taking into account the use of a MSP-FET: MSP430 Flash Emulation Tool from Texas Instruments for JTAG programing and debugging, UART debugging through a mini USB type B port interfacing the FT4232H USB bridge IC from FTDI, a JST XH header for charging internal batteries and a Remove Before Flight (RBF) pin header. These tools and methodology for testing are definied directly from the project main use on the GOLDS-UFSC mission [1] been done with the support of SpaceLab UFSC.

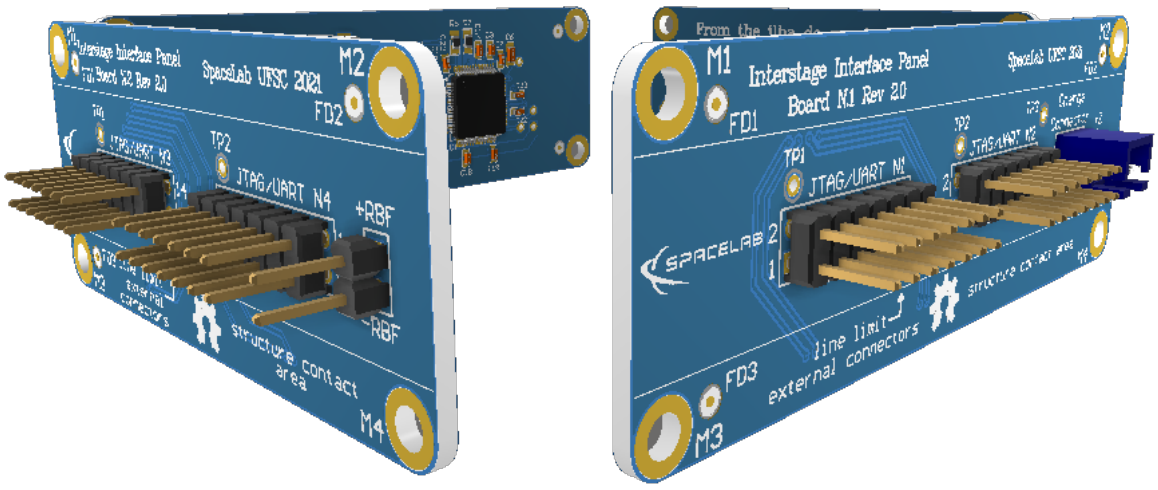

Figure 1.1: Interstage Interface Panels fullset.

All the project, source and documentation files are available freely on a GitHub repository [2].

CHAPTER 2

System Overview

2.1 Block Diagram

On figure 2.1 is displayed the full system block diagram with external devices such as the MSP-FET and a personal computer (PC) during normal usage of IIP. Up to four CubeSat modules can be acessed from its interfaces, been though the pin headers or the USB port. For a specific project, the core modules (EPS, OBDH and TTC) and a optional payload are already represented with their respective interconnections. These connections are done internally with PicoBlade connectors, which are compatible with SpaceLab's modules.

2.2 Board Numeration

Since the IIP is divided up to 3 boards, a numeration was adopted for better refering each PCB on this document. The numeration followed the criteria of the mounting sides determined by the cartesian axis of a Poly Picosatellite Orbital Deployer (P-POD) [3]. Starting the numeration "Nº1" from the referenced -Y plane, the other boards are classified clock-wise that can be found on figure 2.4, each labeled axis can be better seen on figures 3.1 to 3.6. The boards also received names with their unique functionality, Nº1 board is also called "IIP Charge", Nº2 board the "IIP RBF" and Nº3 board the "IIP Quad UART", these nominations are present on the PCBs source files.

2.3 Board Dimensions

IIP is to be mouted vertically inside on the sides of a 2U CubeSat structure, this makes de Nº1 and Nº3 boards having the same PCB dimensions because they are on the same X plane of reference, see figure 2.5. The Nº2 board dimensions can be seen in figure 2.6. The "structure contact area" is the place where the metal frame of the CubeSat structure will be overlapping. All other measurements important to integration and assembly are present in the draftsman PDF documents of each board here [4] on GitHub.

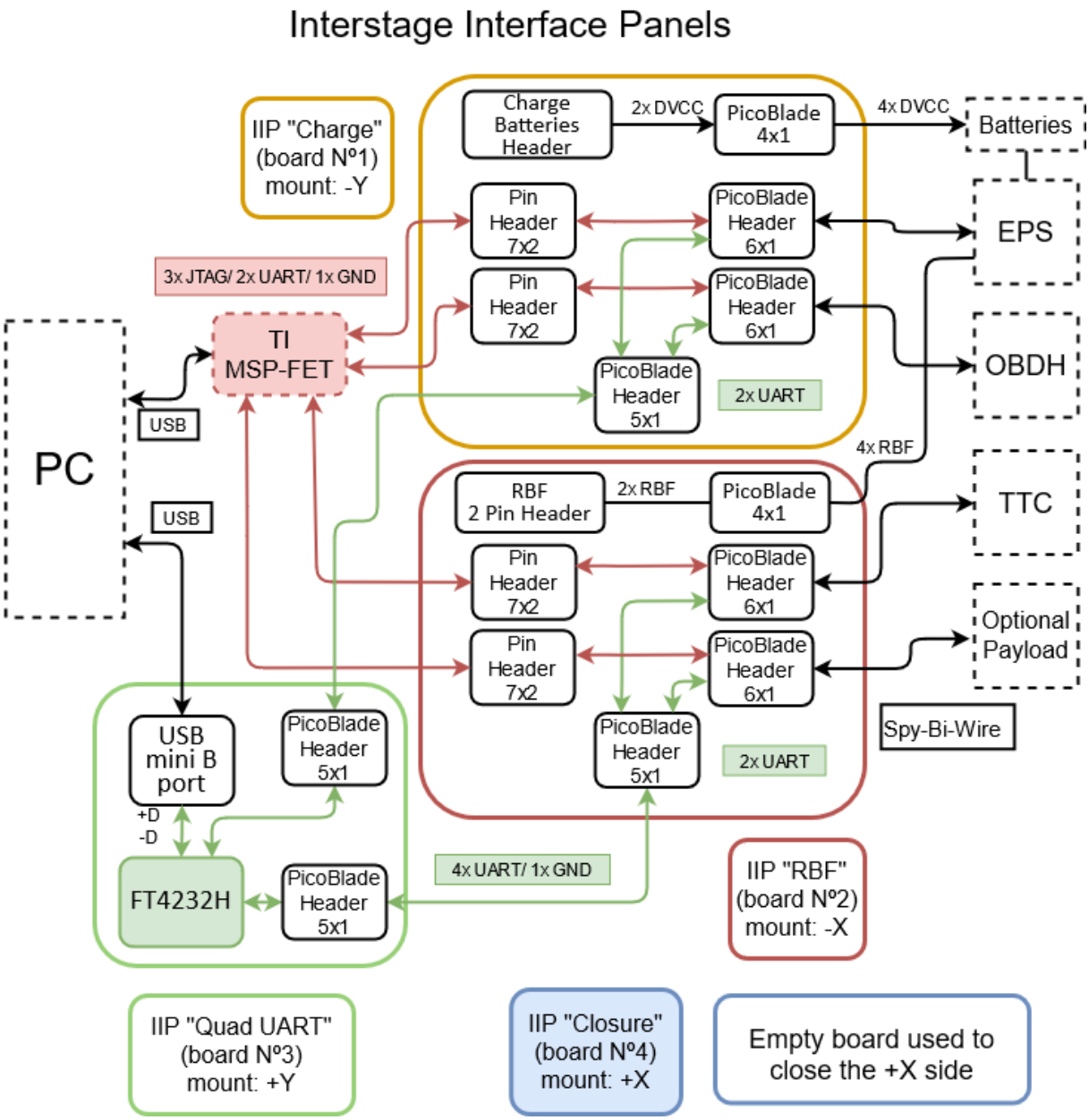

Figure 2.1: IIP hardware block diagram.

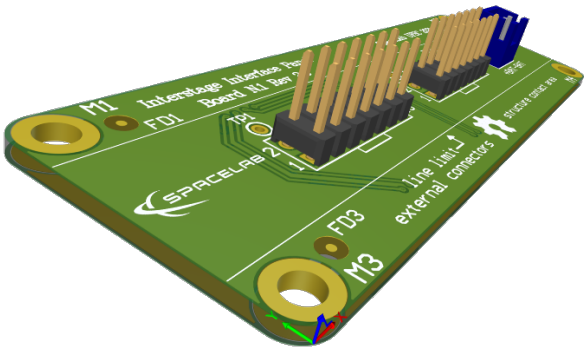

Figure 2.2: IIP Nº1 board.

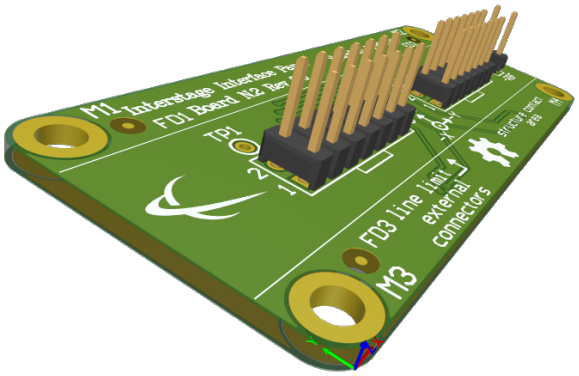

Figure 2.3: IIP Nº2 board.

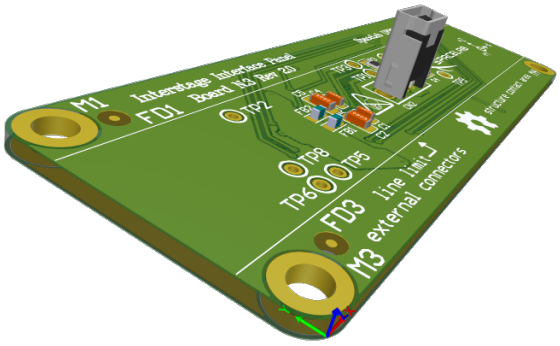

Figure 2.4: IIP Nº3 board.

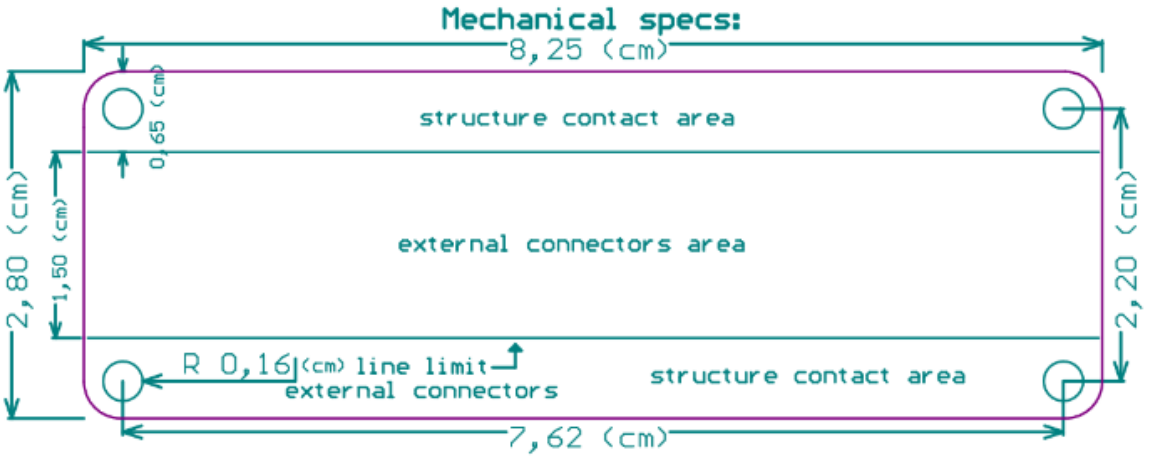

Figure 2.5: IIP Nº1 and Nº3 top dimensions.

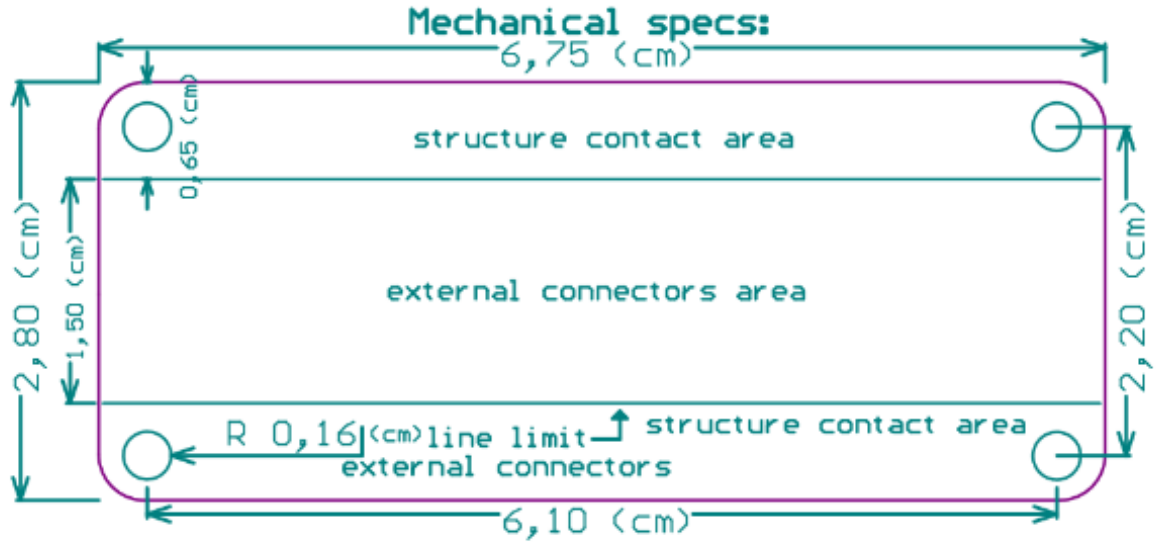

Figure 2.6: IIP Nº2 board top dimensions.

CHAPTER 3

Hardware

IIP is designed to be mouted vertically on the sides of a 2U CubeSat structure and provide all the minimal features for AIT. In the following sections, the hardware design, external and internal connectors, the FT4232H IC and test points are described in detail. On figures 3.1 to 3.6 is displayed top and bottom PCB prints of the three boards.

3.1 Hardware Design

To be low cost, IIP has the default two layer stackup, HASL finish, 0.3mm minimal hole size, 2.54mm miminal track width and no controled impedance. While for fast USB communication it is recommended a controled impedance of 90 ohms, as exposed in USB Hardware Design Guidelines for FTDI ICs [5], IIP Nº3 board is not meant to operate with high speed signals. The hightest baund rate for UART log messages for debbuging purposes is expected to be 115200 bps, this parameter is defined for SpaceLab's core modules. Although not a serious concern, the tracks used for the mini USB type B connector to the FT4232H IC were made the shortest possible and most of the guidelines of FTDI were followed.

Components size and positioning were decided for conforming with the CubeSat 2U standard of maximum connector height on the sides of the P-POD structure [3] and to a specific project scenario using SpaceLab's core modules for the GOLDS-UFSC mission [1].

3.2 External and internal connectors

In this section all external and internal connectors are exposed in detail.

3.2.1 JTAG/UART Pin Headers

There are four 14 pin headers (2.54mm pitch) on IIP for JTAG and UART usage, two are present in Nº1 board and the other two in Nº2 board, they can be seem on the two figures 3.7 and 3.8. These headers were choosen to be used with MSP-FET tool and its standard cable connector. Their pionout is showed on table 3.1.

Internally these pin headers are interfaced via PicoBlades to be connected to the four modules inside the CubeSat. As can be seen in the block diagram figure 2.1 present on the overview chapter, each one of these PicoBlades is assigned to a specific module, they are showed in figures 3.9 and 3.10.

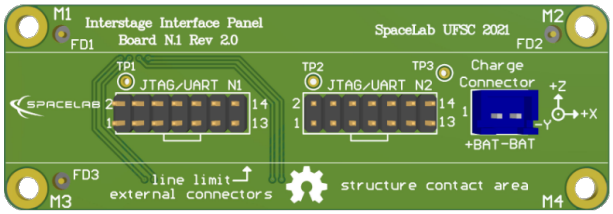

Figure 3.1: IIP Nº1 board top view.

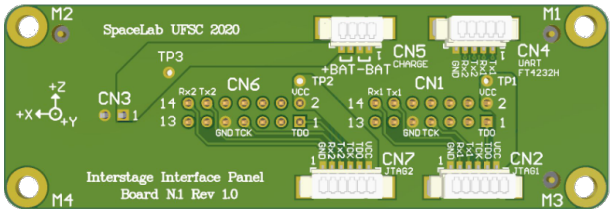

Figure 3.2: IIP Nº1 board bottom view.

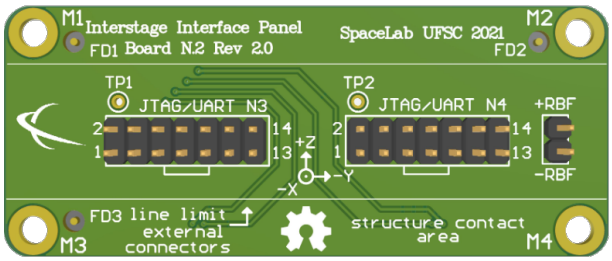

Figure 3.3: IIP Nº2 board top view.

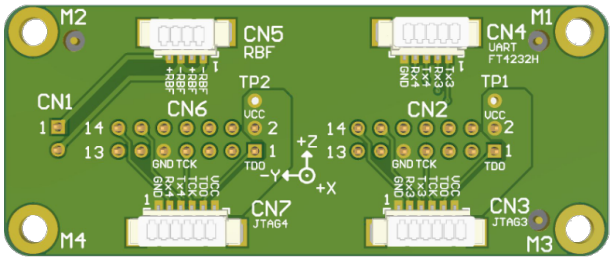

Figure 3.4: IIP Nº2 board bottom view.

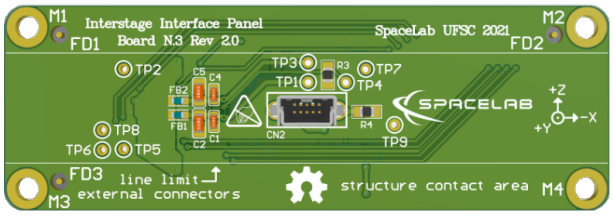

Figure 3.5: IIP Nº3 board top view.

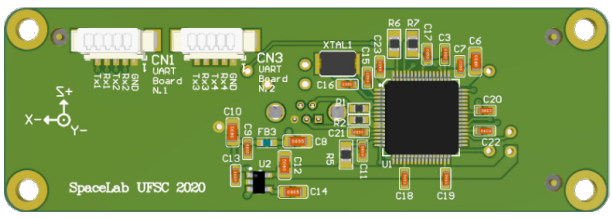

Figure 3.6: IIP Nº3 board bottom view.

Pin [A-B]	*Row A*	*Row B*
1-2	TDO_TDI	VCC_3V3
3-4	-	-
5-6	-	-
7-8	TCK	-
9-10	GND	-
11-12	-	UART_TX
13-14	-	UART_RX

Table 3.1: JTAG pin headers pinout.

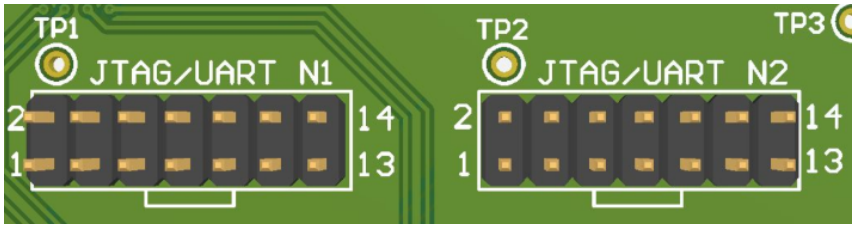

Figure 3.7: IIP Nº1 JTAG pin headers.

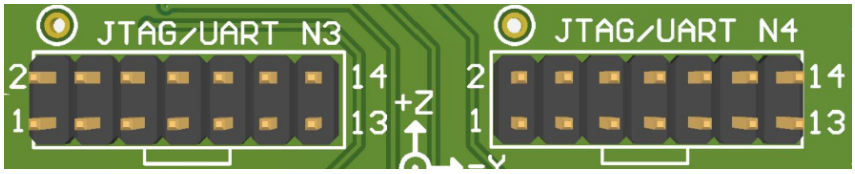

Figure 3.8: IIP Nº2 JTAG pin headers.

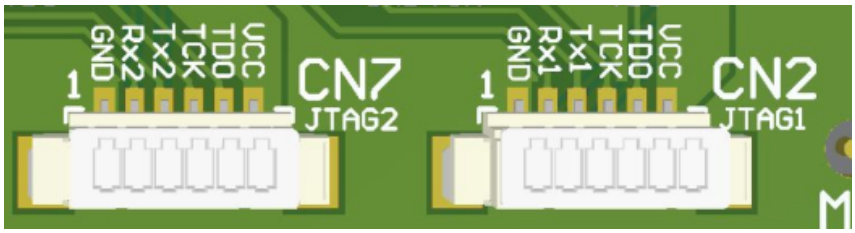

Figure 3.9: IIP Nº1 JTAG PicoBlades.

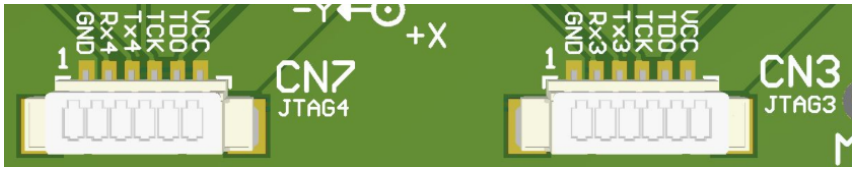

Figure 3.10: IIP Nº2 JTAG PicoBlades.

3.2.2 Charge Header

On board Nº1 there is a JST XH 2 position header [B2B-XH-A-M(LF)(SN)] for charging batteries of the CubeSat, it can be seen in figure 3.11. The component can suport up to 3000mA of current, but in practice it will be used with less than 1500mA. The internal 4 pin PicoBlade connector showed in figure 3.12 is to be connected to the EPS module to make the interconnection for the JST header. The charge header also provides a detent lock for fastening and avoid mistankenly reverse connection.

Figure 3.11: IIP Nº1 charge header.

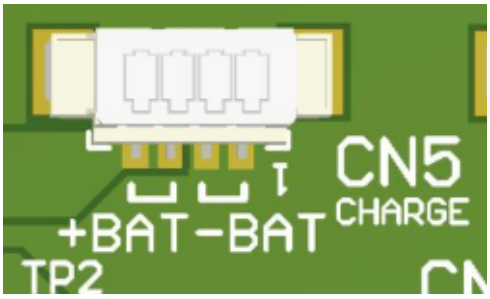

Figure 3.12: IIP Nº1 charge PicoBlade.

3.2.3 RBF Pin Header

The Remove Before Flight pin header is located on board Nº2, see figure 3.13. The choice of its location was according to the CubeSat Design Specification from Cal Poly SLO [6] that required the RBF pin to be located on the X plane of the P-POD. This ensures that the CubeSat subsystems will be powered off on test phase using a simple jumper wire conecting the pins, even with kill-swithes already enabled to do this fuctionality by been pressed againts the spring mechanism. The interconnection between the header and the EPS module is done by a internal 4 pin PicoBlade, showed in figure 3.14.

Figure 3.13: IIP Nº2 RBF pin header.

3.2.4 Mini USB Type B Port

On Nº3 board there is a vertical mini USB type B 2.0 port (651005136421) to be used for UART debbuging, the connector is seen on figure 3.15. This is done though the FT4232HL-REEL IC and its subcircuitry located on the bottom side of the PCB, a better

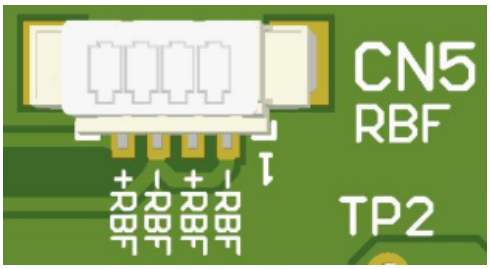

Figure 3.14: IIP Nº2 RBF PicoBlade.

vision is showed on figure 3.16. The circuit is self powered by the USB cable, not requiring any external power supply.

There are two internal 5 pin PicoBlade connectors that connects with boards Nº1 and Nº2 to acquire the UART log data from the modules, these components are showed on figure 3.17. The other Picoblades that makes this interconnection between interface panels are seen in figures 3.18 and 3.19, for Nº1 and Nº2 boards respectively.

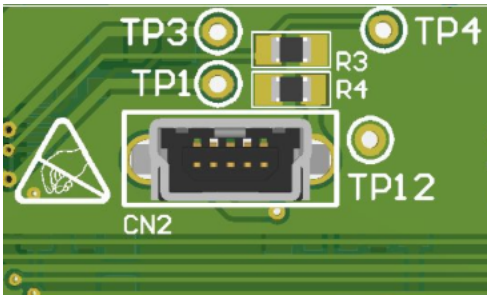

Figure 3.15: IIP Nº3 mini USB type B port.

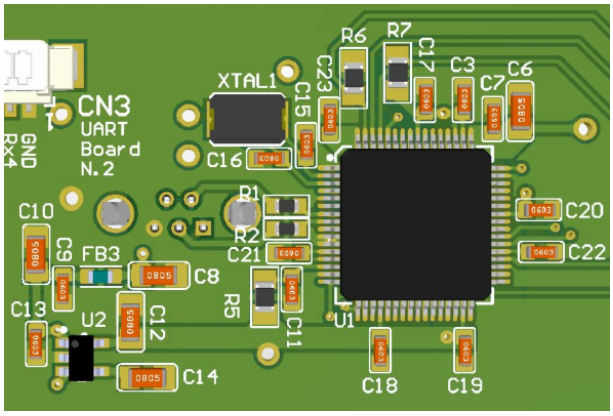

Figure 3.16: IIP Nº3 USB auxiliary circuitry.

3.3 FT4232H IC

For UART to USB conversion the FT4232HL-REEL IC from FTDI [7] was chossen for enabling the debbuging though log messages for 4 independent modules. The REEL form factor was decided to be easier to be soldered manually if necessary. The IC gives flexibility to have an integrated UART to USB conversion in the inferface of IIP, not needing

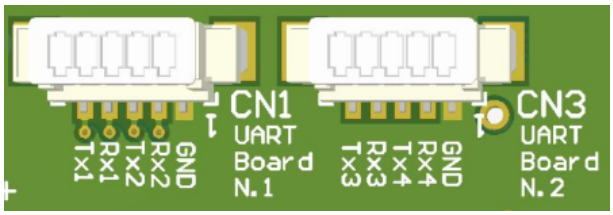

Figure 3.17: IIP Nº3 UART PicoBlades.

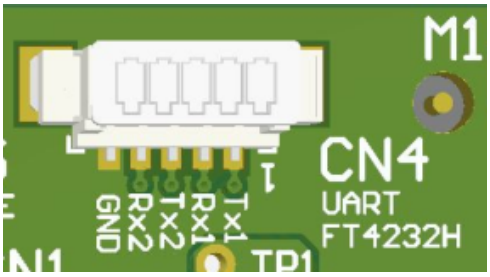

Figure 3.18: IIP Nº1 UART PicoBlade.

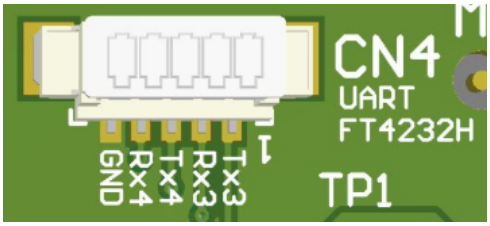

Figure 3.19: IIP Nº2 UART PicoBlade.

the use of a external device like the FT232. The component and its auxiliary subcircuitry can be seen on figure 3.16.

3.4 Test Points

On the three boards of IIP there are some test points that can be easily acessed from the front side of the panels. Others that are present on the "structure contact area" will not be available when the interface is assembled on the 2U CubeSat structure, see the PCBs top and bottom prints on figures figures 3.1 to 3.6. The reason for this is that the metal frame of the structure will be at the front blocking the access, referer to chapter 4 for more details. Next is presented the tables of the test points labels and their description of the boards Nº1: 3.2, Nº2: 3.3 and Nº3: 3.4.

Label	*Description*
TP1	JTAG 1 3V3 power
TP2	JTAG 2 3V3 power
TP3	Battery charge header positive polarity

Table 3.2: IIP Nº1 board test points.

Label	*Description*
TP1	JTAG 3 3V3 power
TP2	JTAG 4 3V3 power

Table 3.3: IIP Nº2 board test points.

Label	*Description*
TP1	(VPLL) 3V3 FT4232H power input.
TP2	(VREGOUT) 1V8 FT4232H internal power output.
TP3	(VPHY) 3V3 FT4232H power input.
TP4	(REF) Current reference for FT4232H.
TP5	(RESET#) Reset input for FT4232H.
TP6	(EECS) EEPROM chip select - pulled down by 10k resistor.
TP7	(VCCIO) I/O interface 3V3 power supply input.
TP8	(EEDATA) EEPROM data I/O - pulled up by 10k resistor.
TP9	(EECLK) Clock signal to EEPROM - not used.
TP10	(PWREN#) Active low power-enable output.
TP11	(SUSPEND#) Active low when USB is in suspend mode.
TP12	(GND) 0V ground input for FT4232H.

Table 3.4: IIP Nº3 board test points.

CHAPTER 4

Board Assembly

IIP has the Bill of Material (BOM) for each board avalaible at its GitHub repository in excel spreeadsheets format. Also the PCBs can be assembled by a Pick-and-place machine using the .txt file found on the hardware/fabrication folder if desired, fiducials are placed on each board to make this possible. All components are to be fitted on the IIP boards, the only exception is the one described below. The draftsman PDF documents of each board shows all the components positioning, they can be found here [4].

4.1 DNP component

There is only one "do not place" (DNP) component present in the Nº3 board, it is the labeled R4 pad with 0805 size (2012 metric) available for soldering the mini USB type B chassi to GND for Electromagnetic compatibility (EMC), see 3.15. This can be done soldering a zero-ohm resistor for a DC path or capacitor for a high-frequency path between shield and signal ground, see section 2.2.2 of the document [5].

4.2 Integration

IIP board Nº1 is to be mouted vertically inside the 2U strucuture on the -X referenced plane. IIP board Nº3 is to be mouted in the same plane of reference but in the other side, that is the +X plane. IIP board Nº2 is to be mouted on the -Y plane. The integration order of the interface panels follows their numeration, this means the first PCB to be integrated is Nº1, then Nº2 and at last Nº3. The internal PicoBlade connections to the modules must be done before proceding to mount the other panels.

The last cables to be connected are between Nº3 (figure 3.17) and Nº1 and Nº2 (figures 3.18 and 3.19) for the labeled "UART" PicoBlades. The only interface of IIP that can be acessed when the 2U satellite is already integrated to the P-POD is the Nº2 board which is located the RBF pin and JTAGs 3 and 4.

CHAPTER 5

Usage Instructions

IIP interfaces can be used depending on the project if it's followed the hardware features and constraints.

5.1 Charging batteries

To charge the batteries it will be needed a cable compatible with the JST XH header. The compatible housing is a XHP-2 receptacle, the jumper lead socket to socket to be used can be ASXHSXH22K305, or any other with AWG #30 to #22. The only constraint is that the current cannot excel 2000mA, because the PicoBlades connectors used to interconnect the JST header to the modules only support 1000mA per pin. For safe usage it is recommended to use the header with a 1500mA maximum charge current.

5.2 Programming and Debugging Modules Though JTAG

Following the pinout of the pin headers showed at 3.1 the JTAG interface can be used according to any debugger and programmer tool and cable assembly with dual row 14 pin 2.54mm pitch. If more than one pin header is to be used simultaneously in the same panel, the length of the cable assemblies housing must be considered to avoid mechancial incopability. For IIP it was tested on a EDA tool using a 61201423021 14 Position Rectangular Receptacle Connector from Würth Elektronik, garanting the use of the default cable of the MSP-FET in this situation.

5.3 Debugging though USB

Connecting a type A to mini type B USB cable to a PC and the USB port present on IIP Nº3, the four USB to UART channels should be ready to be used. Note that the computer will recognize the port as four different devices. The IIP Nº3 doesn't have an EEPROM, so it will be already configured to operate as default serial ports. The FT4232H will have the built-in default VID (0403) and PID (6011).

Bibliography

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