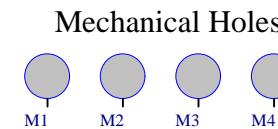
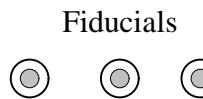


| Rev | Description | Date (DD/MM/YY) | Author |
|-----|--|-----------------|-------------------|
| 1.0 | Initial Release. | 01/07/20 | Yan C. de Azeredo |
| 2.0 | Adding fourth PCB "4_iip_closure" and "4_iip_camera" PCBs, updating mounting holes pads, block diagram, SpaceLab logo and layout of N°3 IIP board. | 28/06/21 | Yan C. de Azeredo |
| | | | |
| | | | |

Revision History



PCB Elements

Insterstage Interface Panels for a 2U or 3U CubeSat

Copyright © 2021
by Universidade Federal de Santa Catarina.

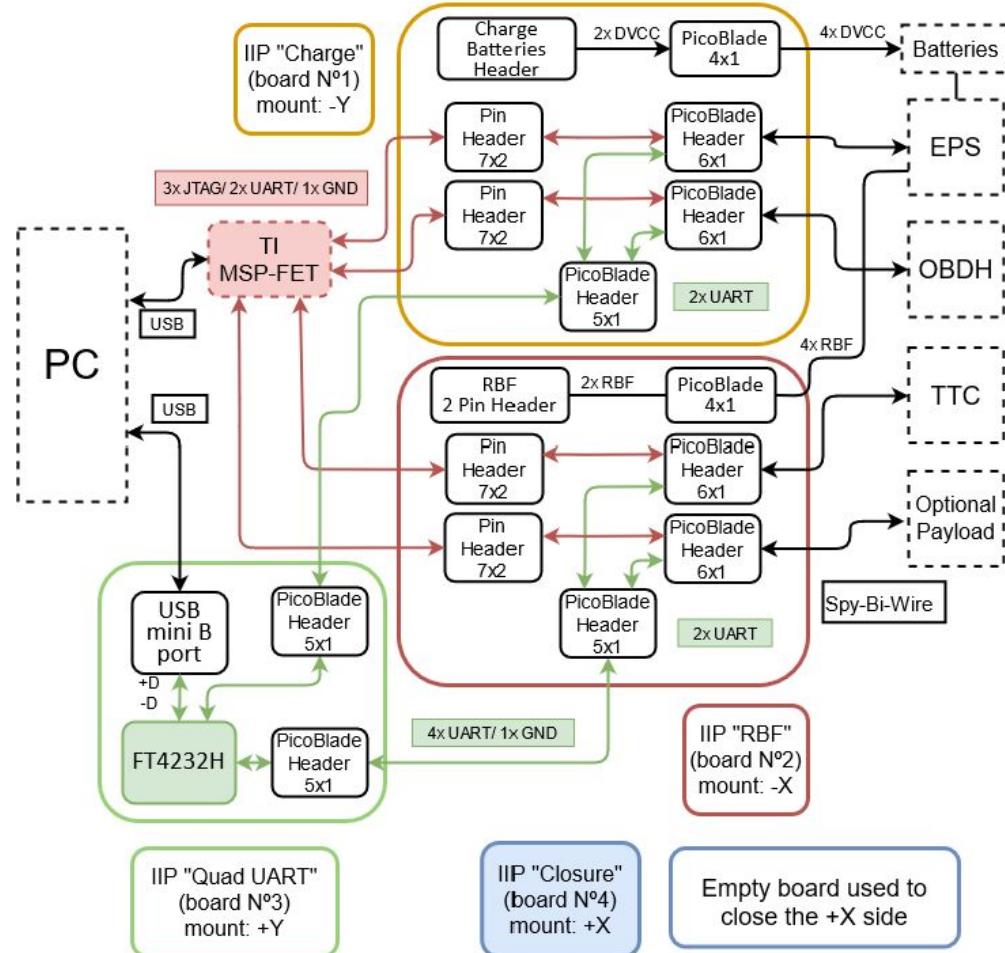
This work is licensed under the CERN-OHL-S Open Hardware License version 2.

To view a copy of this license, visit
<https://ohwr.org/project/cernohl/wikis/Documents/CERN-OHL-version-2>.

- Designed by: Yan Castro de Azeredo
- Reviewers: Gabriel M. Marcelino and André M. P. Mattos
- Support: Gabriel M. Marcelino, André M. P. Mattos and Kleber Gouveia
- Mechanical validation: Edemar M. Filho and Caique S. M. Gomes

Project Information

Interstage Interface Panels



Full System Block Diagram

| | |
|--|--|
| SpaceLab - Federal University of Santa Catarina | |
| Project: I_iip_charge.PrjPCB [No Variations] | |
| Title: IIP Hardware Architecture | |
| Designed by: Yan Castro de Azeredo | |

A

B

C

D

A

B

C

D

