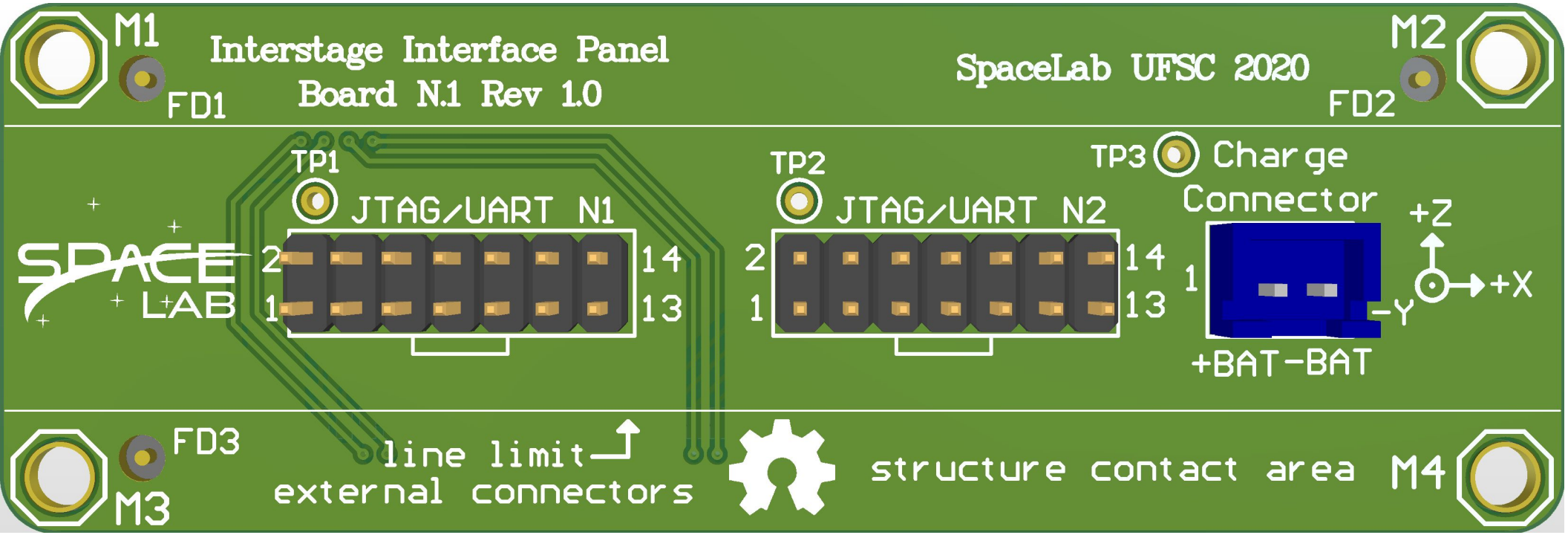
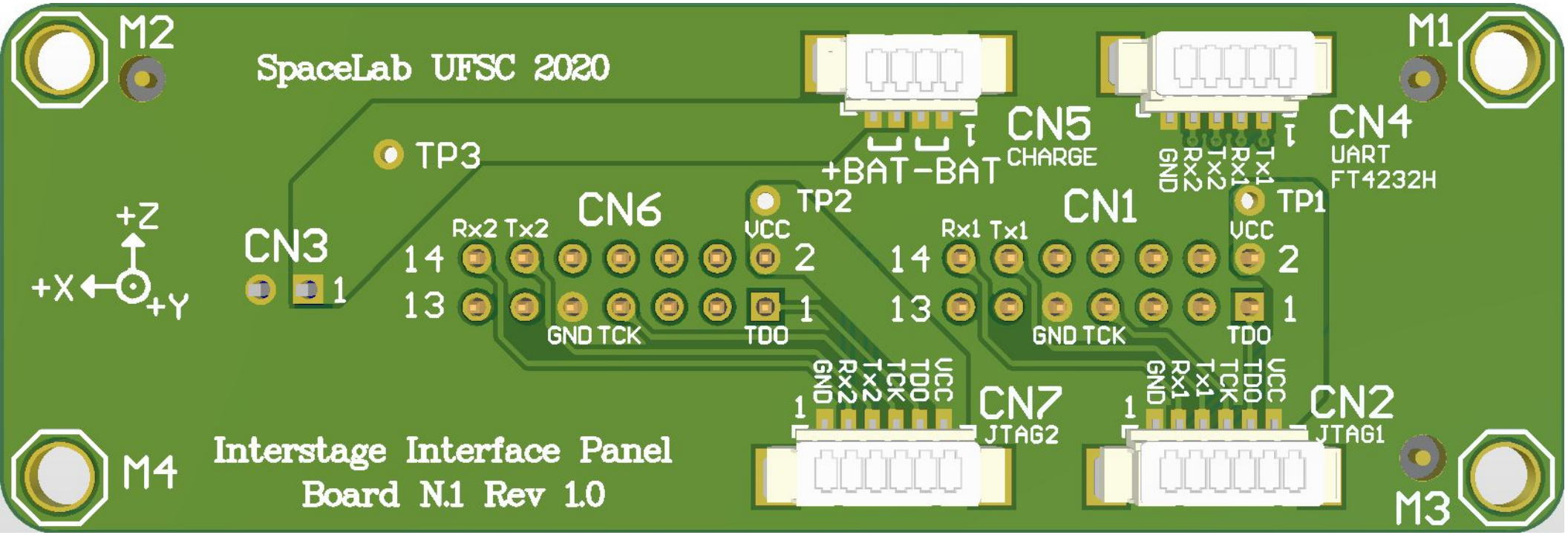
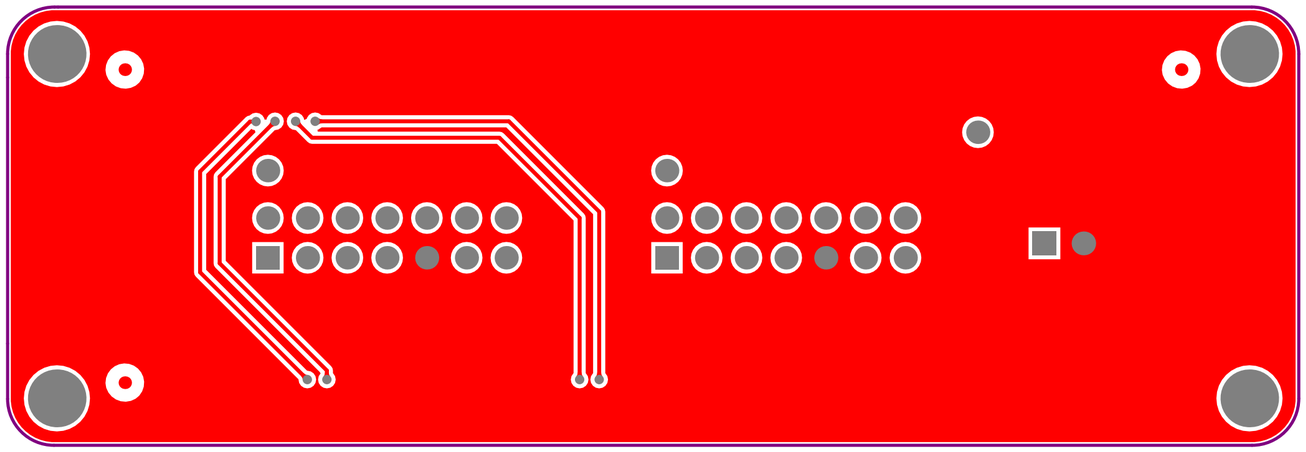

M1
Interstage Interface Panel
Board N.1 Rev 1.0
SpaceLab UFSC 2020
M2
FD1
FD2
TP1
JTAG/UART N1
TP2
JTAG/UART N2
TP3
Charge
Connector
+Z
+X
-Y
+BAT
-BAT
SPACE
LAB
2
1
14
13
FD3
M3
line limit
external connectors
structure contact area
M4


M2
SpaceLab UFSC 2020
M1
TP3
CN5
CHARGE
+BAT
-BAT
CN4
UART
FT4232H
GND
RX2
TX2
RX1
TX1
+Z
+X
+Y
CN3
1
CN6
Rx2 Tx2
14
13
GND TCK
TP2
VCC
2
1
TDO
CN1
Rx1 Tx1
TP1
CN7
JTAG2
CN2
JTAG1
TCK
TDI
TMS
M4
Interstage Interface Panel
Board N.1 Rev 1.0
M3

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.010mm	3.5	
1	Top Layer	Copper	0.035mm		
	Dielectric 1	FR-4	1.500mm	4.2	
2	Bottom Layer	Copper	0.035mm		
	Bottom Solder	Solder Resist	0.010mm	3.5	
	Bottom Overlay				



TITLE: IIP N.1 BOARD CHARGE		REV: 1.0	DATE: 01/07/2020
MATERIAL: FR4	Silkscreen color: white	Project: IIP	
Board Thickness: 1.6mm	Layers: 02	Space Technology Research Laboratory Federal University of Santa Catarina **SpaceLab UFSC**	
PCB Surface: HASL	Drawing: Yan C. de Azeredo		

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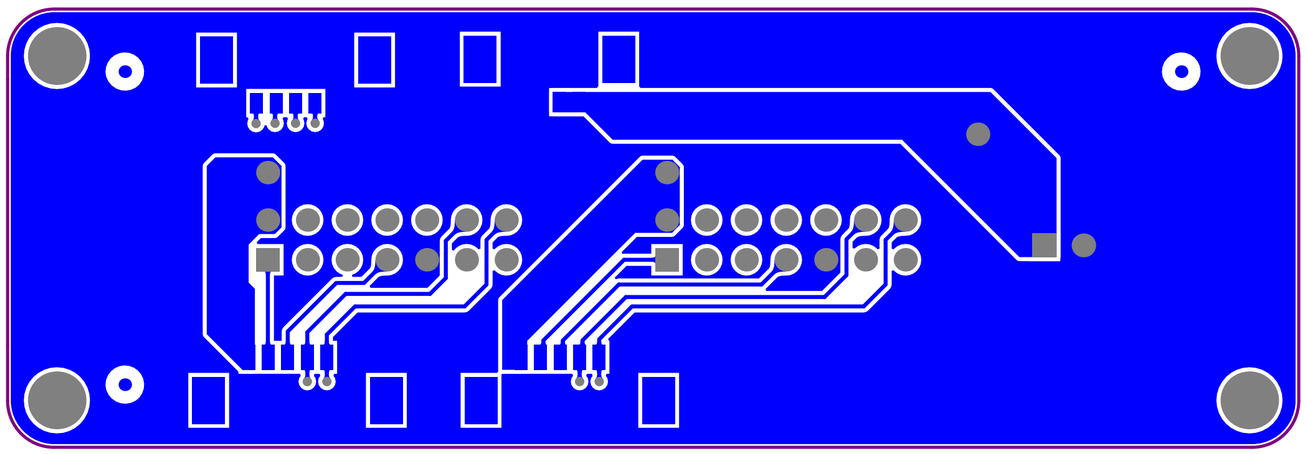

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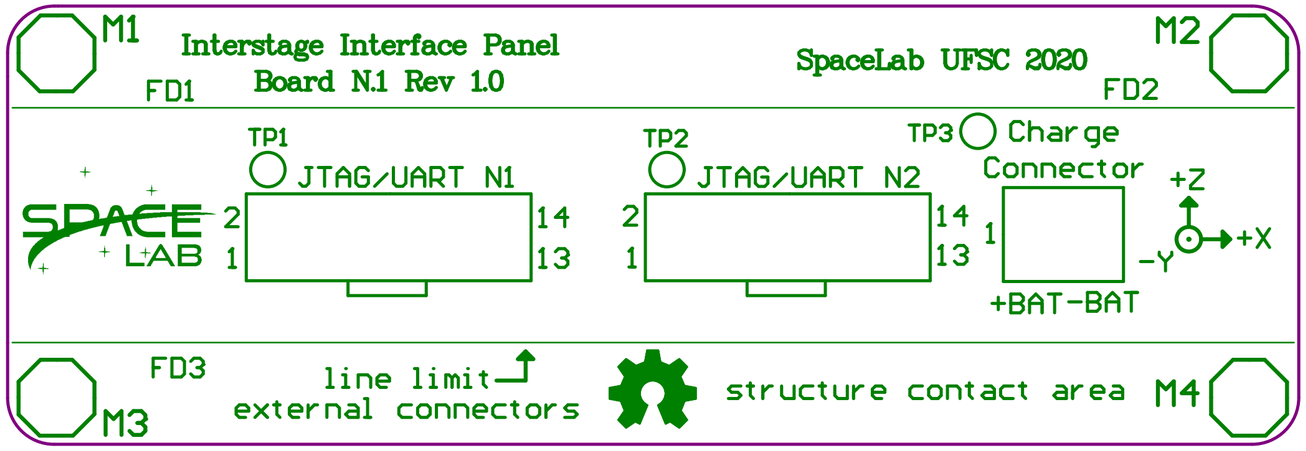

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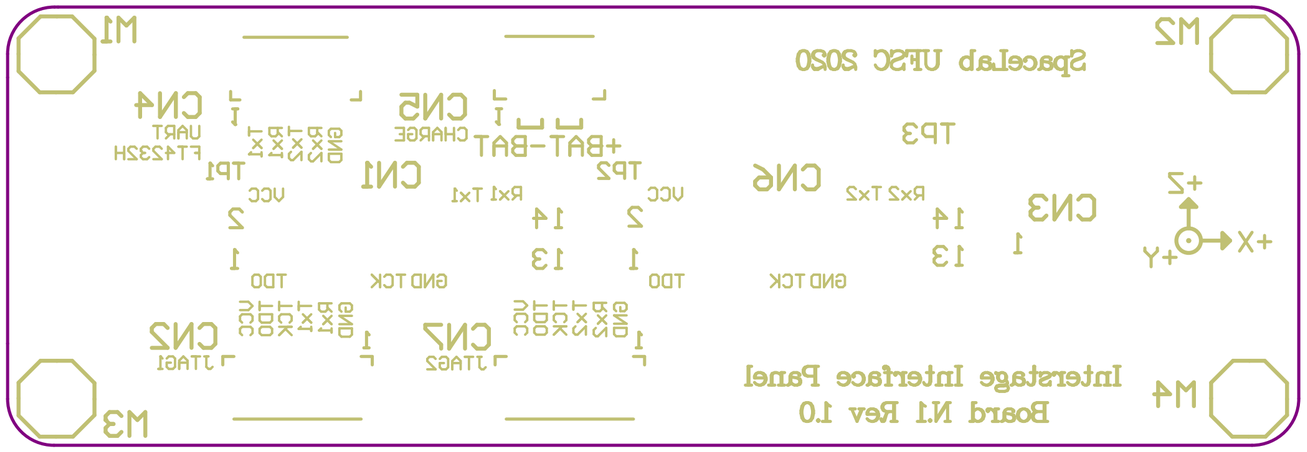

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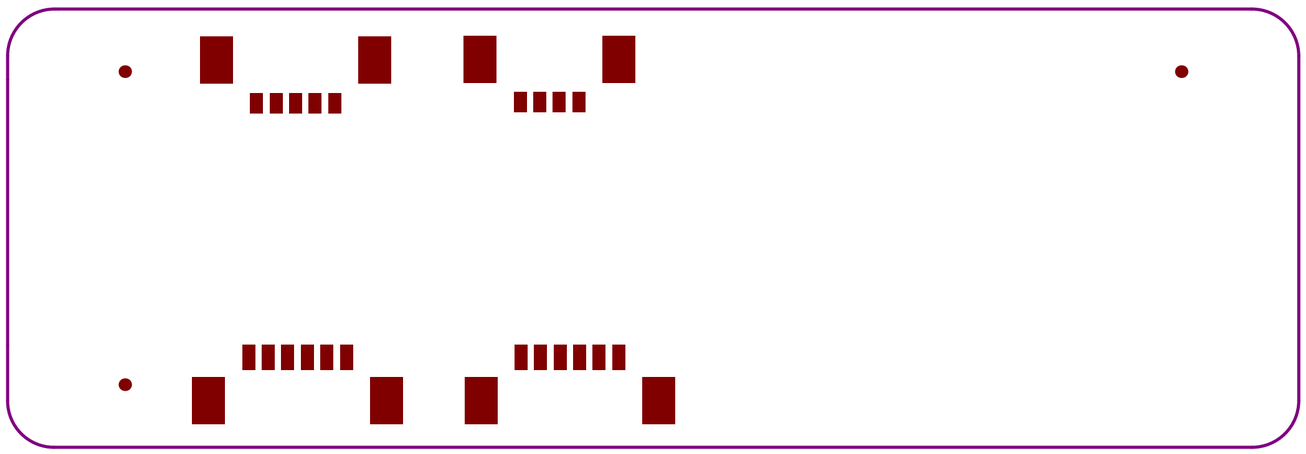

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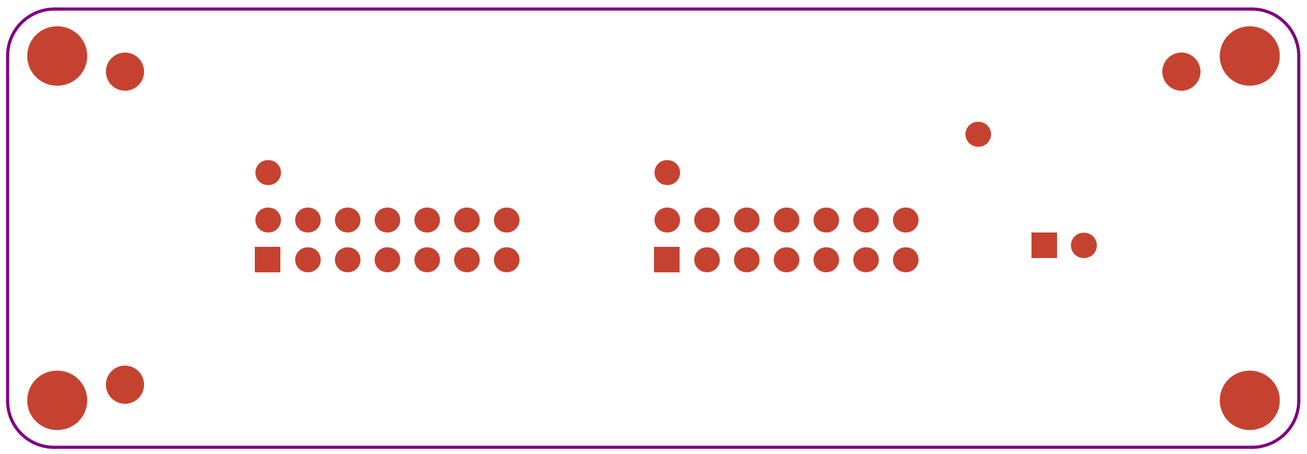

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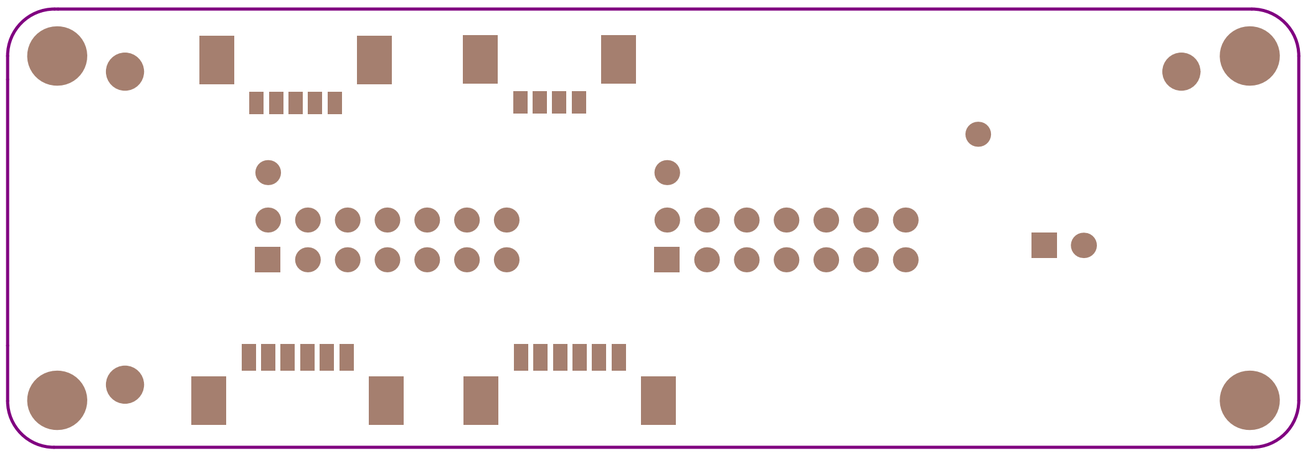

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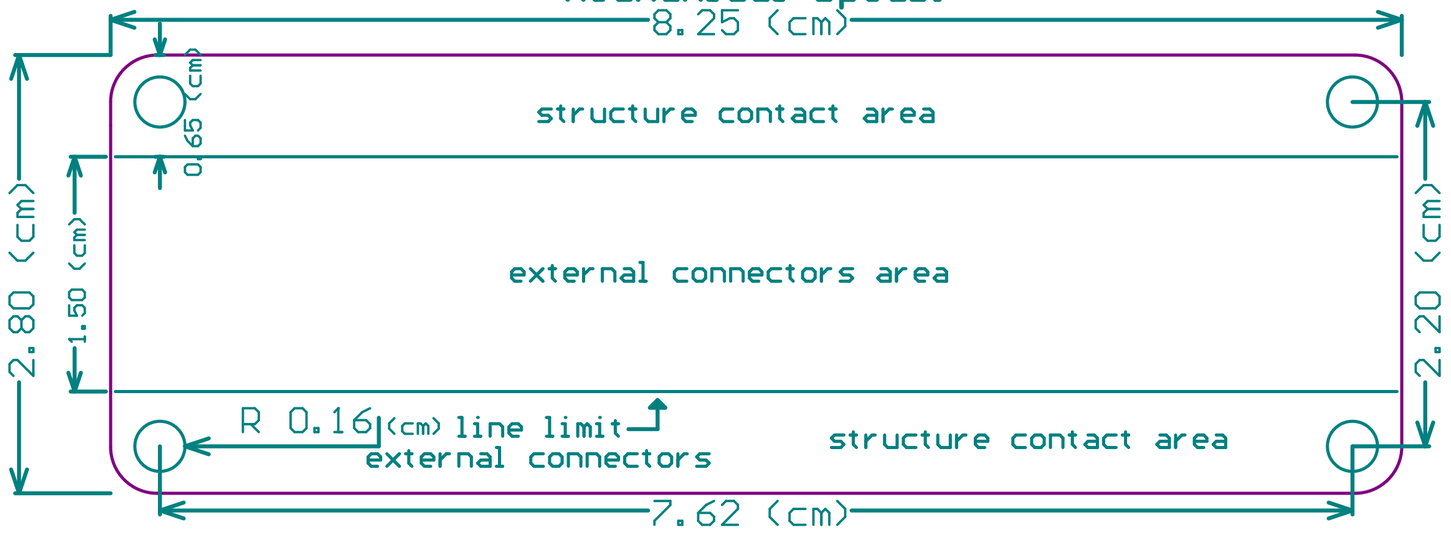
Mechanical specs:



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Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
✡	8	0.300mm (11.81mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v60h30m0mx0
▽	3	0.900mm (35.43mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c150h90
○	30	1.000mm (39.37mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
□	4	3.200mm (125.98mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c370h320
	45 Total							

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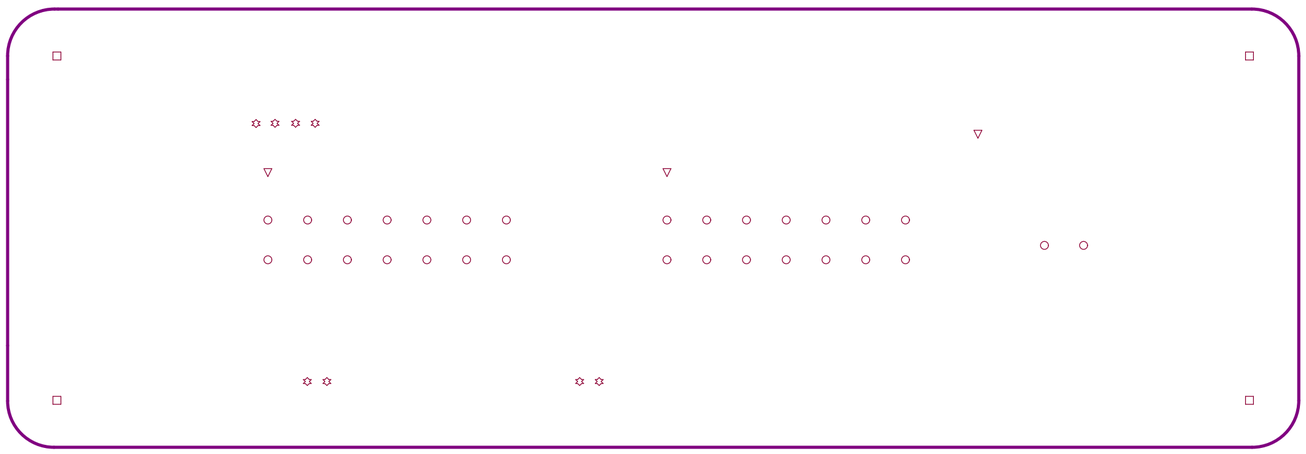

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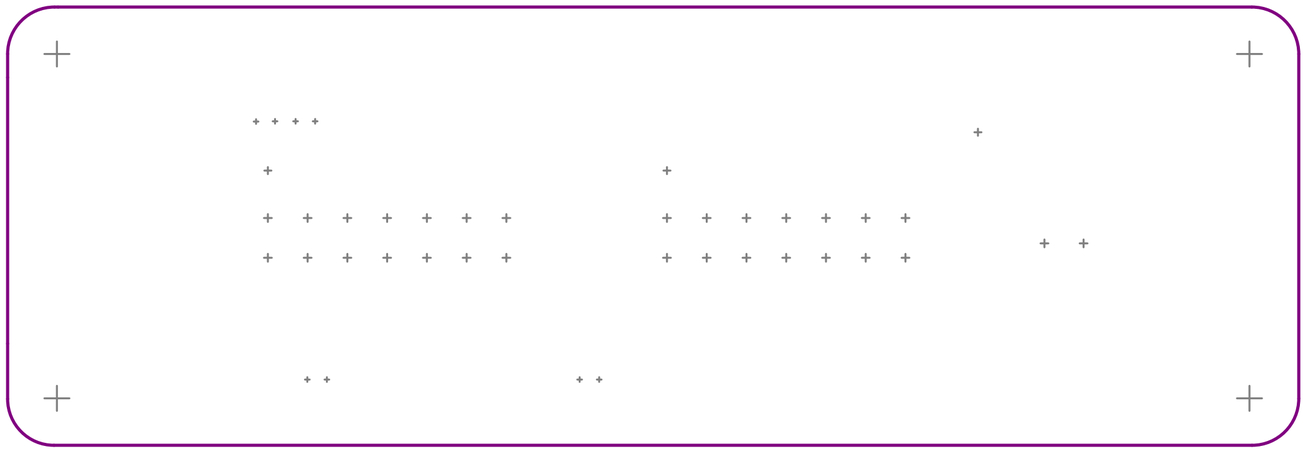

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