

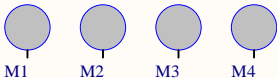
Rev	Description	Date	Author
1.0	Initial Release.	01/07/20	Yan C. de Azeredo

Revision History

Fiducials



Mechanical Holes



PCB Elements

Semi USB Interstage Interface Panels of FloripaSat-2 2U CubeSat

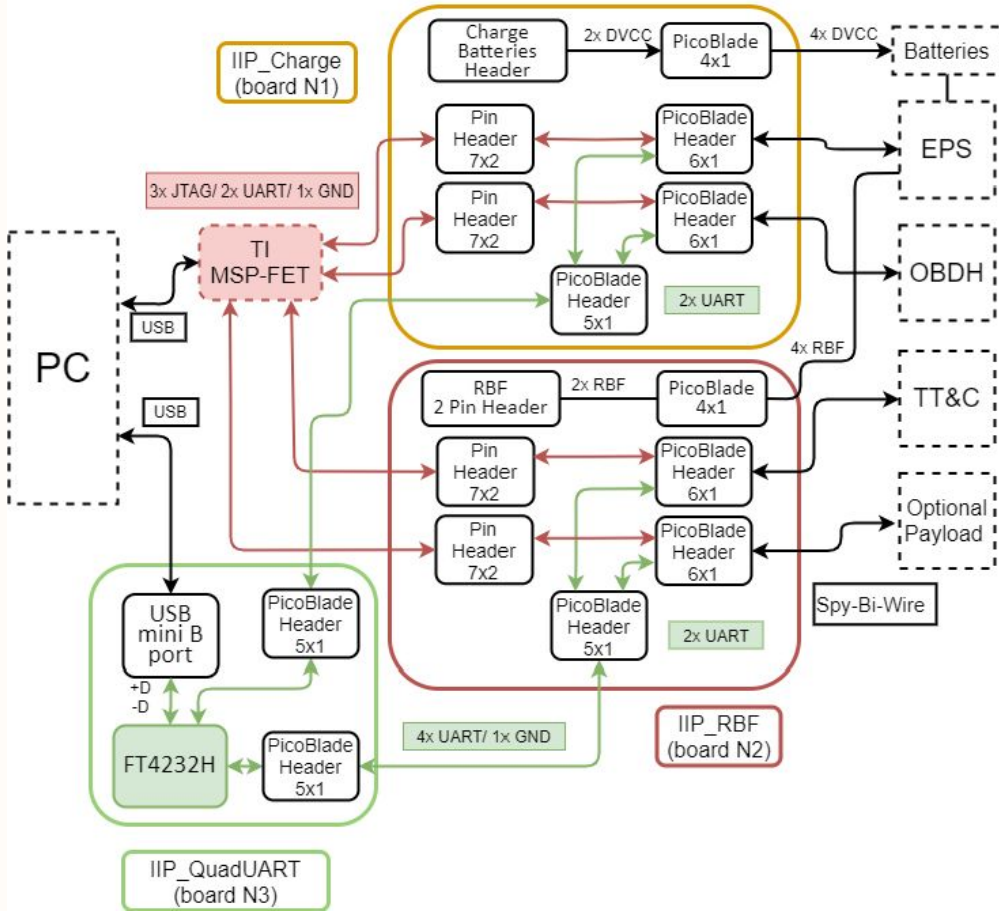
Copyright © 2020
by Universidade Federal de Santa Catarina.

This work is licensed under the Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license, visit <http://creativecommons.org/licenses/by-sa/4.0/>.


- Drawn by: Yan Castro de Azeredo
- Reviewers: Gabriel M. Marcelino and André M. P. Mattos
- Support: Gabriel M. Marcelino, André M. P. Mattos and Kleber Gouveia
- Mechanical validation: Edemar Morsch Filho

Project Information

Semi USB Interstage Interface Panels

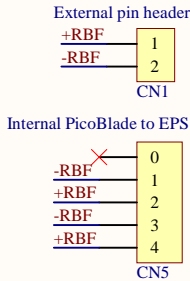


Full System Block Diagram

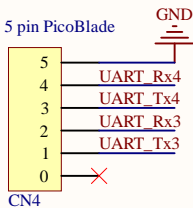
Title: 0_Architecture.SchDoc				<i>UFSC - SpaceLab</i> <i>University Campus - Trindade</i> <i>Dep. of Electrical Engineering - CTC</i> <i>Florianópolis, Santa Catarina, Brazil</i> <i>CEP: 88040 - 900</i>	
Size: A4	Project: 2_IIP_RBF.PrjPCB		Revision: 1.0		
Date: 19/07/2020	Time: 00:20:16	Sheet 1 of 2			
Drawn By: Yan Castro de Azeredo		Model: Engineering			



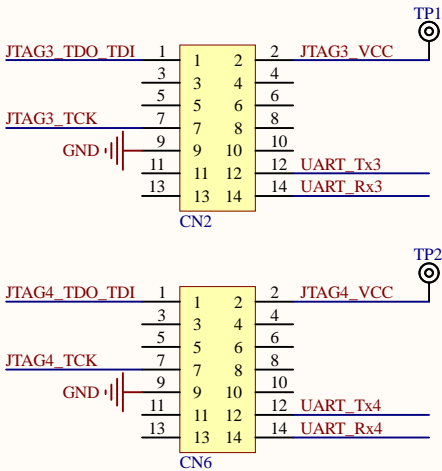
Remove Before Flight (RBF)



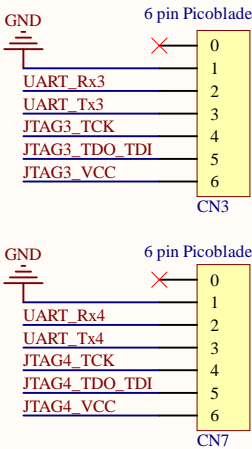
FT4232H UART signals



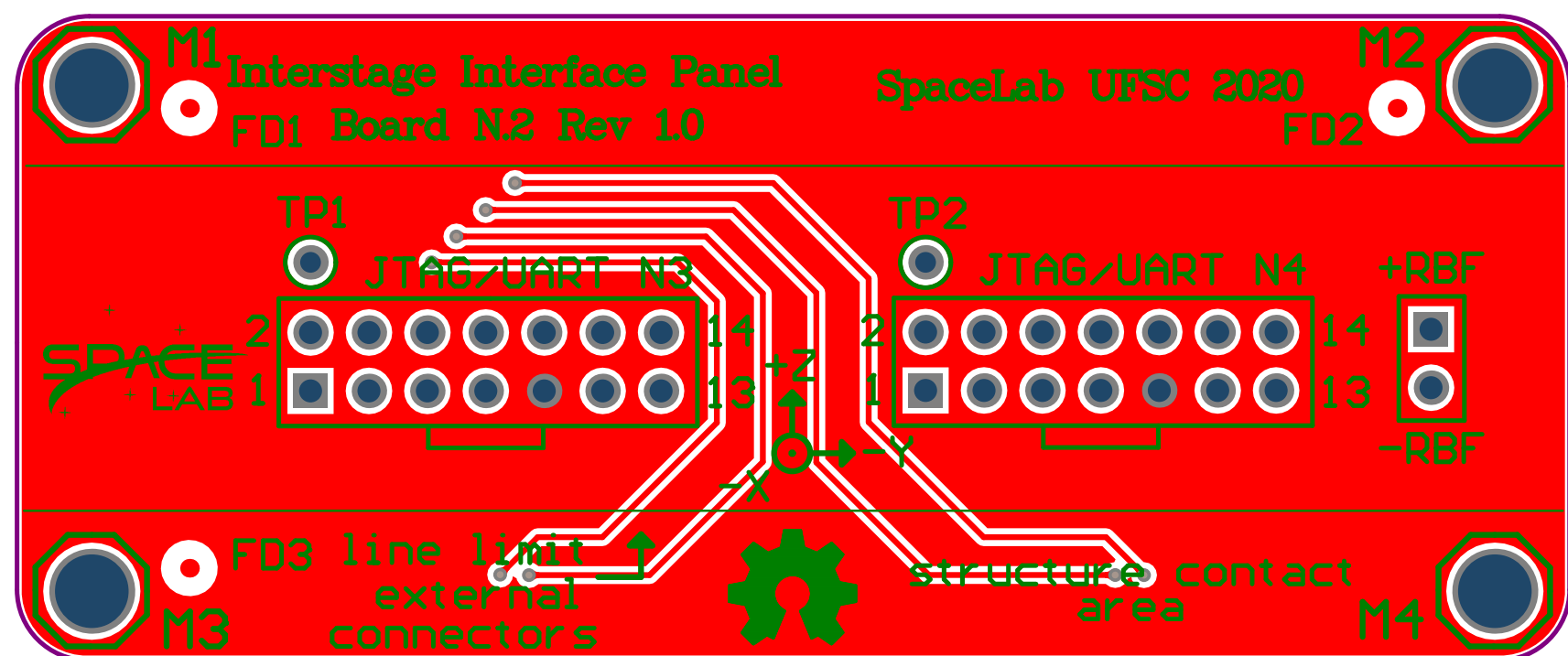
JTAG and redundant UART headers



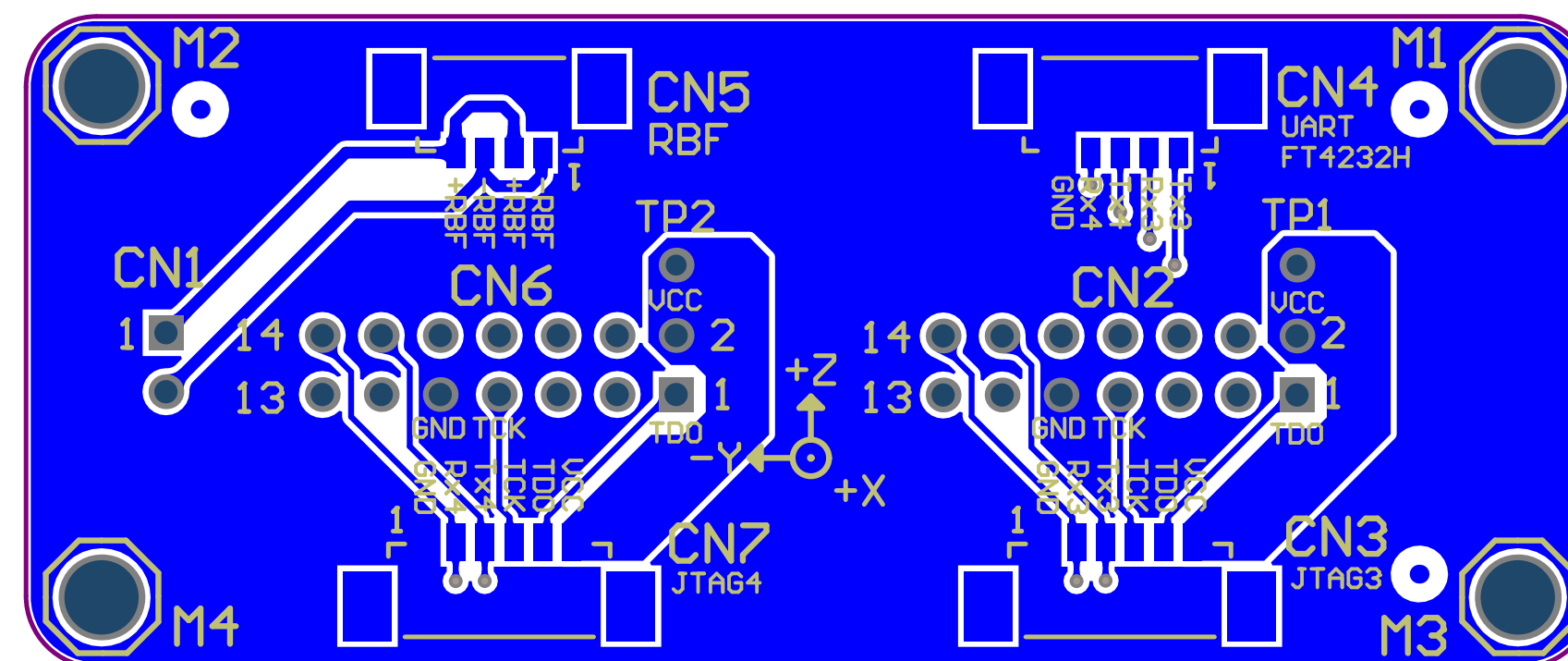
Debug and programming interfaces

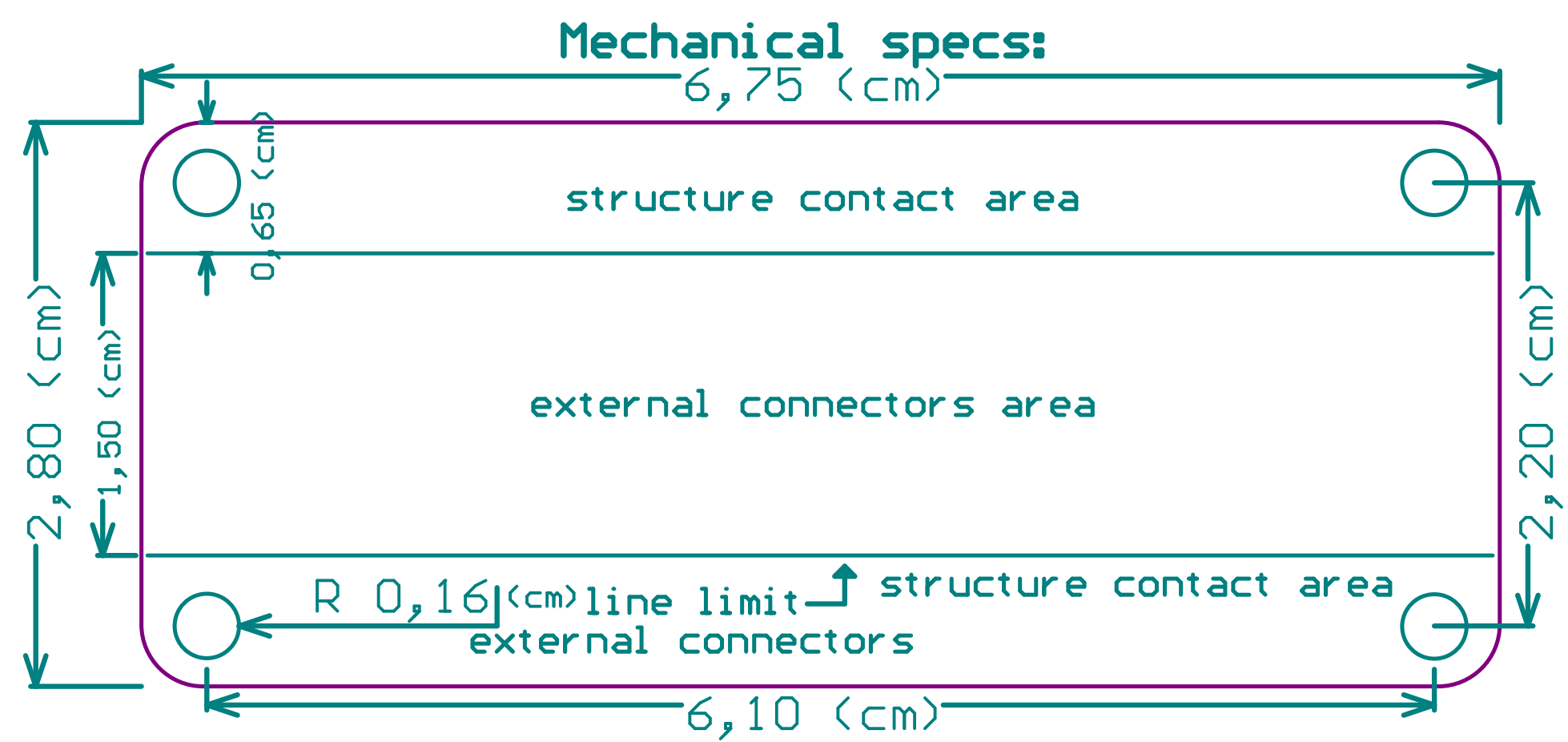


Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0,010mm	3,5	
1	Top Layer	Copper	0,036mm		
	Dielectric 1	FR-4	1,500mm	4,8	
2	Bottom Layer	Copper	0,036mm		
	Bottom Solder	Solder Resist	0,010mm	3,5	
	Bottom Overlay				



TITLE: IIP SEMI USB N.2 BOARD		REV: 1.0	DATE: 02/07/2020
MATERIAL: FR4	Silkscreen color: white	Project: IIP FloripaSat-2	
Board Thickness: 1.6mm	Layers: 02	Space Technology Research Laboratory Federal University of Santa Catarina SpaceLab UFSC	
PCB Surface: HASL	Drawing: Yan C. de Azeredo		





CN2
+

CN6
+

CN1
+

CN5
+

CN4
+

CN7
+

CN3
+

M1 Interstage Interface Panel
FD1 Board N.2 Rev 1.0

SpaceLab UFSC 2020

M2
FD2

TP1

JTAG/UART N3

SPACE
LAB



+Z

-X

TP2

JTAG/UART N4



+RBF

-RBF

M3 FD3 line limit
external
connectors



structure contact
area

M4

