Rev	Description	Date	Author
1.0	Initial Release.	01/07/20	Yan C. de Azeredo

Revision History

Fiducials

FD1 FD2 FD3

Mechanical Holes

M1 M2 M3 M4

PCB Elements

Project Information
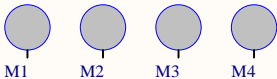
Semi USB Interstage Interface Panels
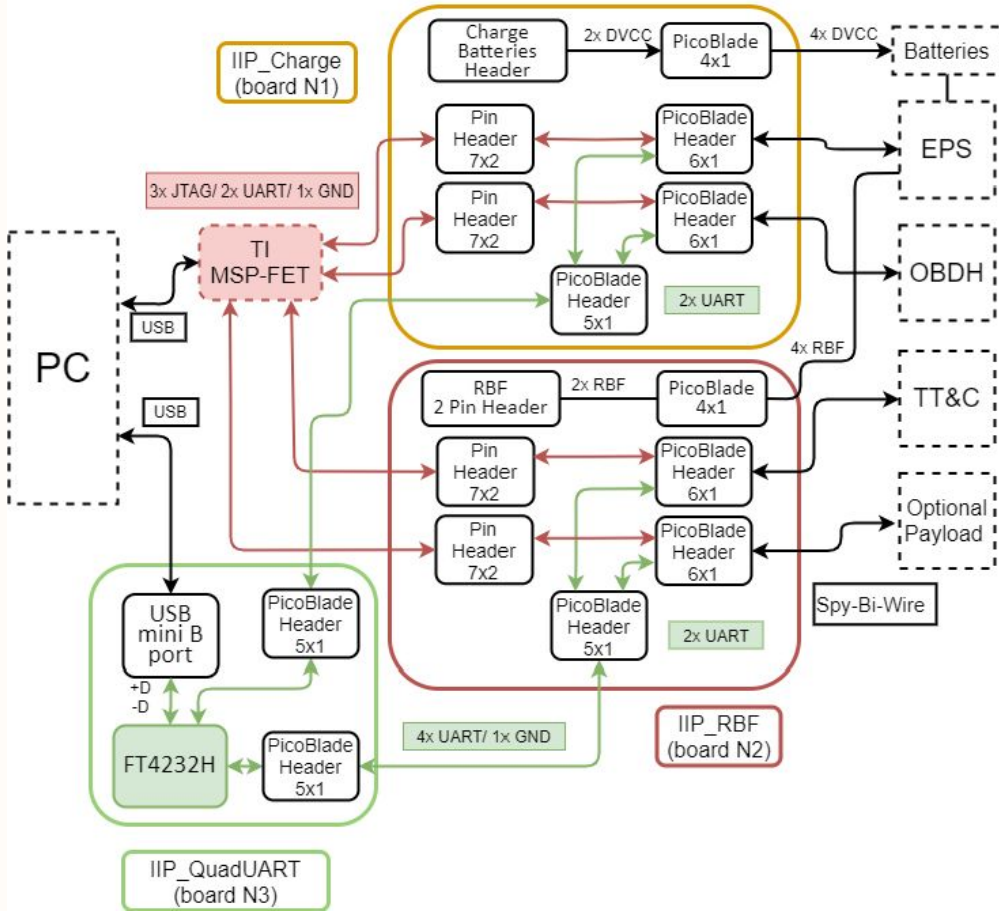
Full System Block Diagram

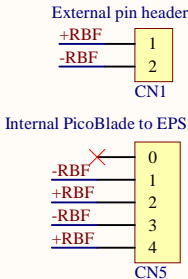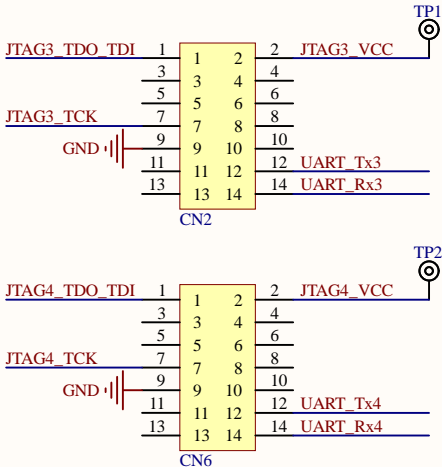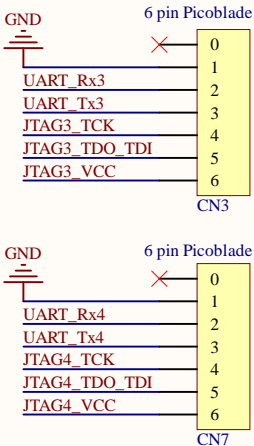| SpaceLab - Federal University of Santa Catarina	
Project: *2_iip_rbf.PrjPCB / [No Variations]*	
Title: *IIP Hardware Architecture*	
Designed by: *Yan Castro de Azeredo*	Project Code: *IIP*
Date: 11/29/2020 Revision: *1.0* Sheet *1* of *2*	Size: A4

Remove Before Flight (RBF)

External pin header

+RBF — 1
-RBF — 2

CN1

Internal PicoBlade to EPS

-RBF — 0
+RBF — 1
-RBF — 2
+RBF — 3
+RBF — 4

CN5

FT4232H UART signals

5 pin PicoBlade   GND

5
4 — UART_Rx4
3 — UART_Tx4
2 — UART_Rx3
1 — UART_Tx3
0

CN4
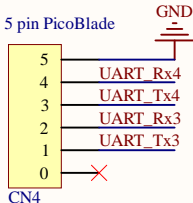
JTAG and redundant UART headers

TP1

JTAG3_TDO_TDI — 1 | 1 | 2 | 2 — JTAG3_VCC
3 | 3 | 4 | 4
5 | 5 | 6 | 6
JTAG3_TCK — 7 | 7 | 8 | 8
GND — 9 | 9 | 10 | 10
11 | 11 | 12 | 12 — UART_Tx3
13 | 13 | 14 | 14 — UART_Rx3

CN2

TP2

JTAG4_TDO_TDI — 1 | 1 | 2 | 2 — JTAG4_VCC
3 | 3 | 4 | 4
5 | 5 | 6 | 6
JTAG4_TCK — 7 | 7 | 8 | 8
GND — 9 | 9 | 10 | 10
11 | 11 | 12 | 12 — UART_Tx4
13 | 13 | 14 | 14 — UART_Rx4

CN6

Debug and programming interfaces

GND   **6 pin Picoblade**

0
1
UART_Rx3 — 2
UART_Tx3 — 3
JTAG3_TCK — 4
JTAG3_TDO_TDI — 5
JTAG3_VCC — 6

CN3

GND   **6 pin Picoblade**

0
1
UART_Rx4 — 2
UART_Tx4 — 3
JTAG4_TCK — 4
JTAG4_TDO_TDI — 5
JTAG4_VCC — 6

CN7