



Documentation of Interstage Interface Panels

Documentation of Interstage Interface Panels

SpaceLab, Universidade Federal de Santa Catarina, Florianópolis - Brazil

Documentation of Interstage Interface Panels

July, 2020

Project Chief:

Eduardo Augusto Bezerra

Authors:

Yan Castro de Azeredo

Contributing Authors:

Revision Control:

Version	Author	Changes	Date
0.1	Yan Castro de Azeredo	Document creation	07/2020



© 2020 by Universidade Federal de Santa Catarina. Interstage Interface Panels. This work is licensed under the Creative Commons Attribution-ShareAlike 4.0 International License. To view a copy of this license, visit <http://creativecommons.org/licenses/by-sa/4.0/>.

List of Figures

2.1	IIP Semi USB full system block diagram.	3
2.2	Nº1 board top view.	4
2.3	Nº1 board bottom view.	4
2.4	Nº2 board top view.	4
2.5	Nº2 board bottom view.	5

List of Tables

Contents

List of Figures	v
Lista of Tables	vii
Nomenclature	vii
1 Introduction	1
2 System Overview	3
2.1 Block diagram	3
2.2 Board numeration	3
2.2.1 Semi USB	4
2.3 Mechanical dimensions	5
3 Hardware	7
3.1 External connectors	7
3.2 Interfaces	7
3.3 PCB layout	7
4 Requeriments	9
4.1 Semi USB variant	9
5 Mouting Instructions	11
6 Usage Instructions	13
References	13

CHAPTER 1

Introduction

The Interstage Interface Panels (IIP) are vertical mounted PCBs designed to give external access to the modules inside of a 2U CubeSat during final assembly, integration and testing (AIT) before launch. IIP is composed of 3 different boards, the complete set allows for the nanosatellite to be charged, programed and debugged. The project is inspired by other solutions already developed, such as the GOMspace NanoUtil Interstage. The design was developed taking into account the use of a MSP-FET: MSP430 Flash Emulation Tool from Texas Instruments for JTAG interfacing, and the FT4232H USB bridge IC from Future Technologies Devices International (FTDI) for quad UART debug channels.

The main motivation for the project was the necessity of a custom off the shelf solution for making the external interface of the FloripaSat-2 CubeSat. The Interface Board of the first CubeSat launched by SpaceLab UFSC, FloripaSat-1, was designed for 1U structure. While both interfaces are very different, some hardware choices were inherited because of the already features in the core modules used, such as the use of PicoBlade connectors for internal connection between modules and interface.

CHAPTER 2

System Overview

2.1 Block diagram

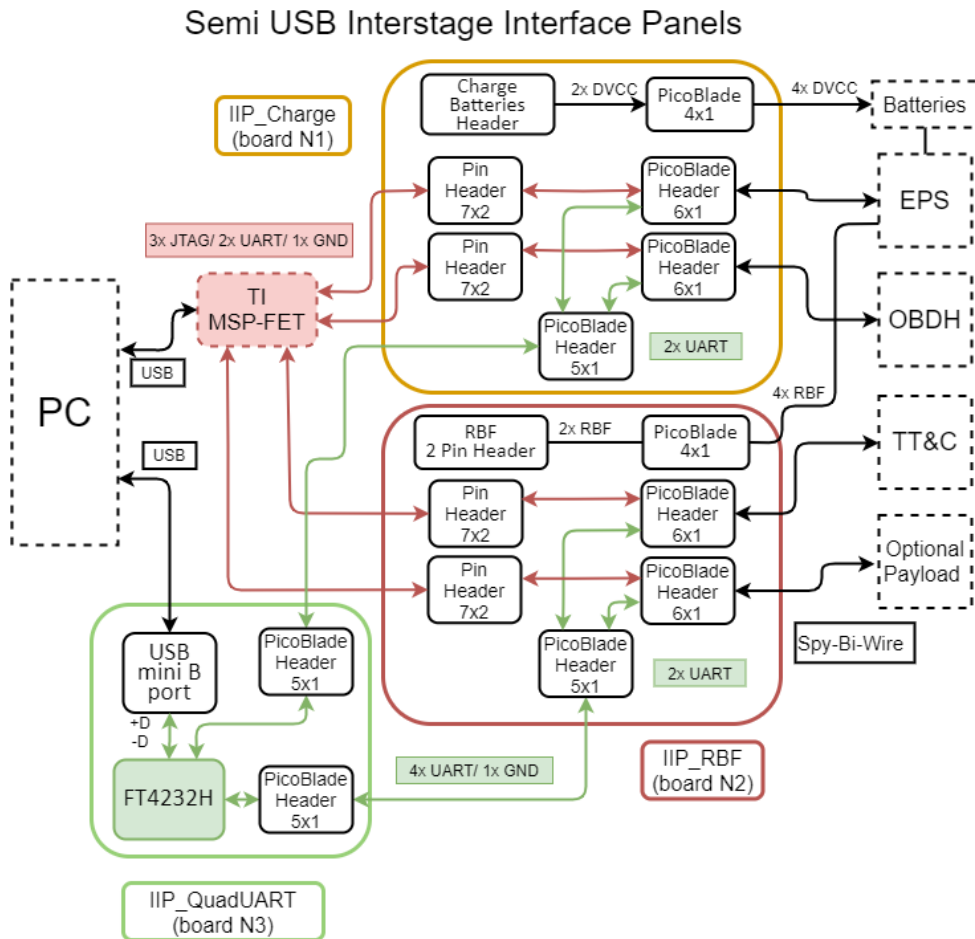


Figure 2.1: IIP Semi USB full system block diagram.

2.2 Board numeration

Since the IIP is divided up to 3 boards, a numeration was designed for better referring each PCB. The numeration followed the criteria of the mounting sides determined by the

cartesian coordinates followed by the CubeSat's modules and Fit Check on the P-POD. Starting the numeration N1 from the refereced -X plane front of the nanosatellite the other boards are classified clock-wise.

2.2.1 Semi USB

Image A (full board assembly image)

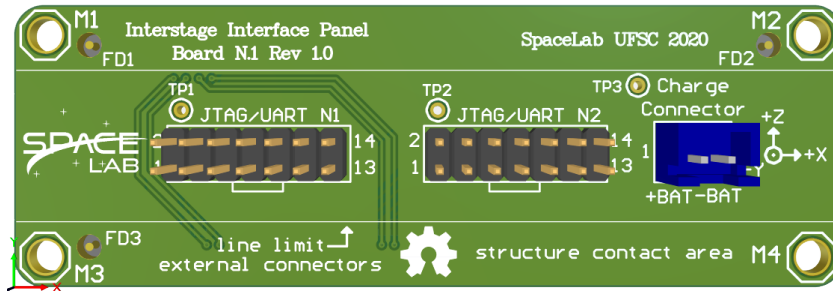


Figure 2.2: N⁰1 board top view.

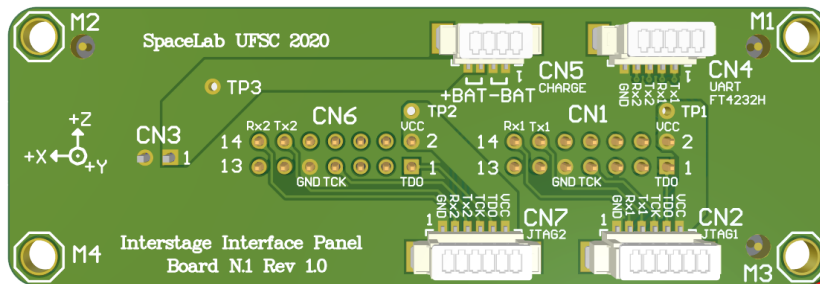


Figure 2.3: N⁰1 board bottom view.

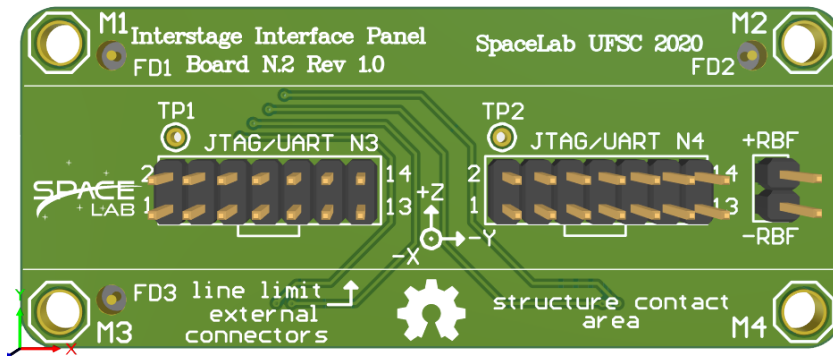
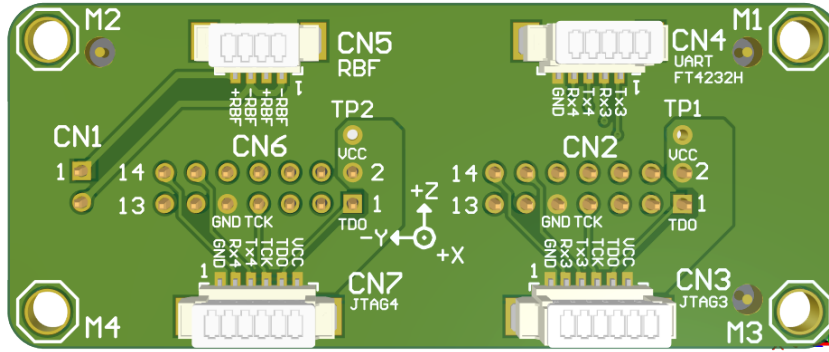


Figure 2.4: N⁰2 board top view.

Figure 2.5: N² board bottom view.

2.3 Mechanical dimensions

The dimensions for the mounting holes on the X and Y planes of the ISIS 2 CubeSat structure are different, for this reason IIP has two mechanical dimension standards.

Image A (Mechanical dimensions for N1 and N3 boards mounted in the Y plane)

Image B (Mechanical dimensions for N2 board)

CHAPTER 3

Hardware

3.1 External connectors

3.2 Interfaces

The internal interfaces are the EPS, OBDH, TTC and "Payload 1" made by 6 pin Picoblade headers positioned inside the 2U structure.

(insert image here)

The pin assigment of each Picoblade is mirroed to match the correponding mating header on each module.

(insert image here)

Specially for the EPS, two 4 pin Picoblades are used for interfacing the Charge and RBF headers on the module.

(insert image here)

3.3 PCB layout

The PCB design uses two layer configuration with two ground planes for mechanical and thermal balancing.

Direct contact on power polygons and GND connections was opted for better current flow and lesser heating on the copper traces.

Three fiducials are placed in each board variants for component machinery fitting if needed. While the boards that don't have many many SMD components like N1 and N2, the fiducials were also placed for flexibilty in PCB manufacturing.

CHAPTER 4

Requeriments

The Interstage Interface Panels have different hardware and software requirements depending on the variant. Both have a external JST header for charging batteries and a 2 pin header for the Remove Before Flight (RBF) Switch. The only recommended counterpart connector for charging batteries is THE XHP-2, the RBF header can be used with any commom jumper wire, the direct compatible housing is M20-1060200.

(include images)

4.1 Semi USB variant

The Semi USB uses 0.1 inch (2.54mm) spacing pin header for JTAG, any other housing can be used for own custom programing and flashing. The USB header is a mini B port, that requires a maximum cable of 5 meters, according to the standard for high speed operation (480 Mbit/s). (include images)

CHAPTER 5

Mouting Instructions

CHAPTER 6

Usage Instructions
