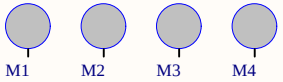
Rev	Description	Date	Author
1.0	Initial Release.		Yan C. de Azeredo

Revision History

PCB

Fidutials

Mechanical Holes



PCB Elements

Semi USB Insterstage Interface Panels of FloripaSat-2 2U CubeSat

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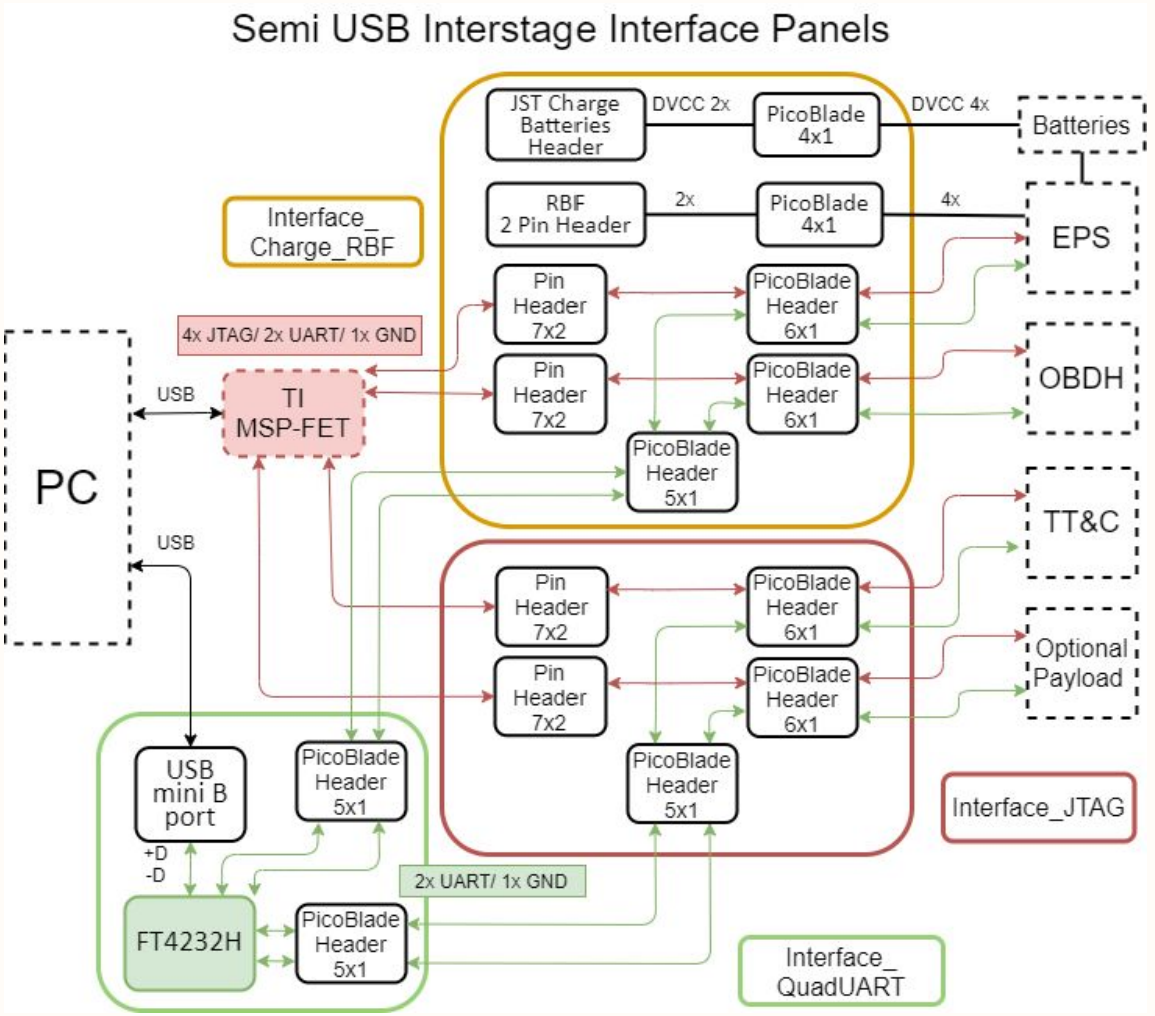
- Drawn by: Yan Castro de Azeredo
- Reviewers: Gabriel M. Marcelino
- Support: Gabriel M. Marcelino and André M. P. Mattos

Project Information



Full System Block Diagram

Title: 0_Architecture.SchDoc			
Size: A4	Project: 1_Interface_Charge_RBF.PrjPCB		Revision:
Date: 28/05/2020	Time: 22:53:37	Sheet 1 of 2	
Drawn By: Yan Castro de Azeredo		Model: Engineering	

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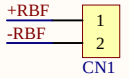
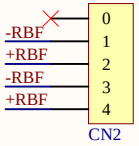
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900

Remove Before Flight (RBF)

External pin header

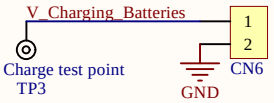


Internal PicoBlade to EPS



Battery charging headers

External JST XH header



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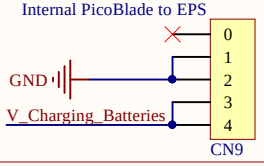
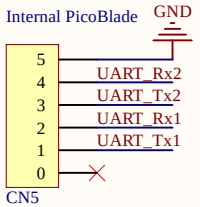
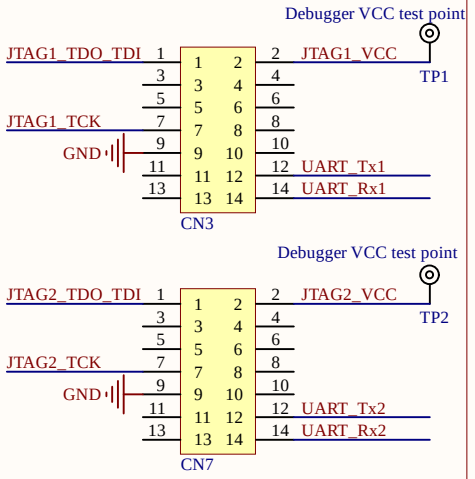


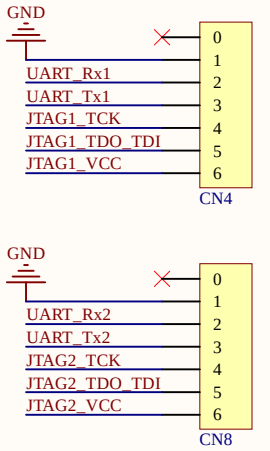
FT4232H UART signals



JTAG and reduntant UART headers



Debug and programming interfaces



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Date: 28/05/2020	Time: 22:53:37	Sheet 2 of 2	
Drawn By: Yan Castro de Azeredo		Model: Engineering	

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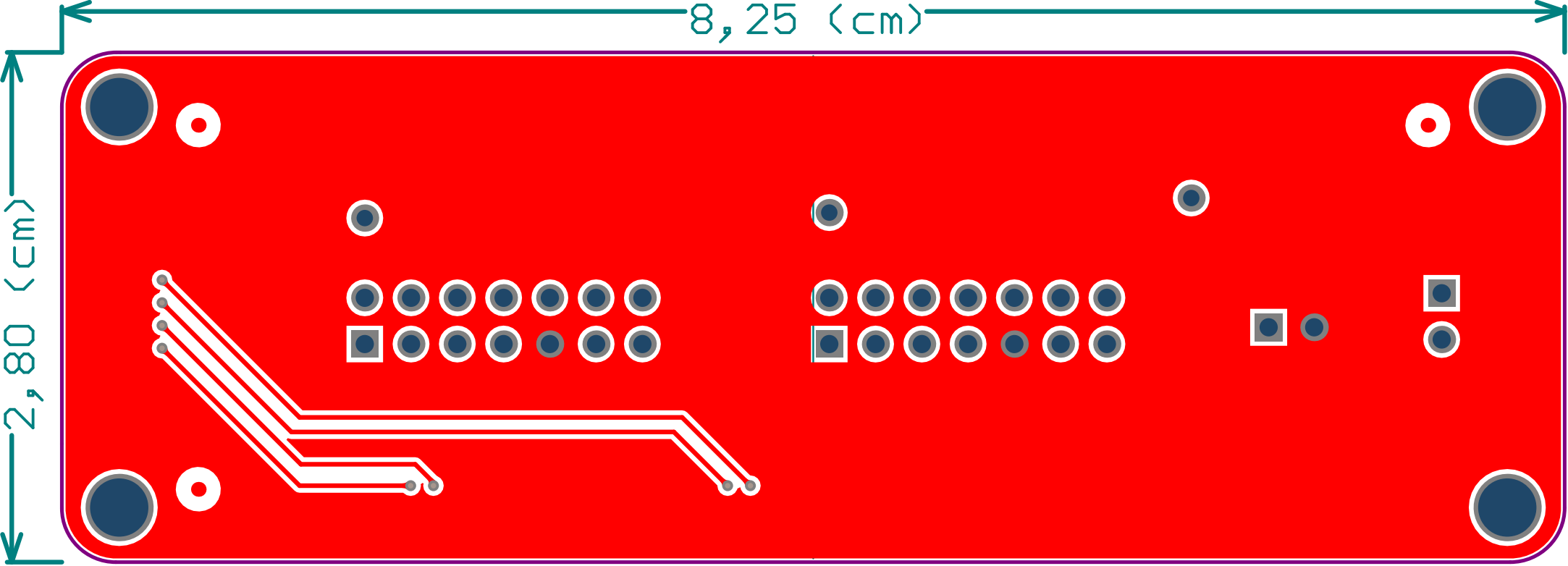
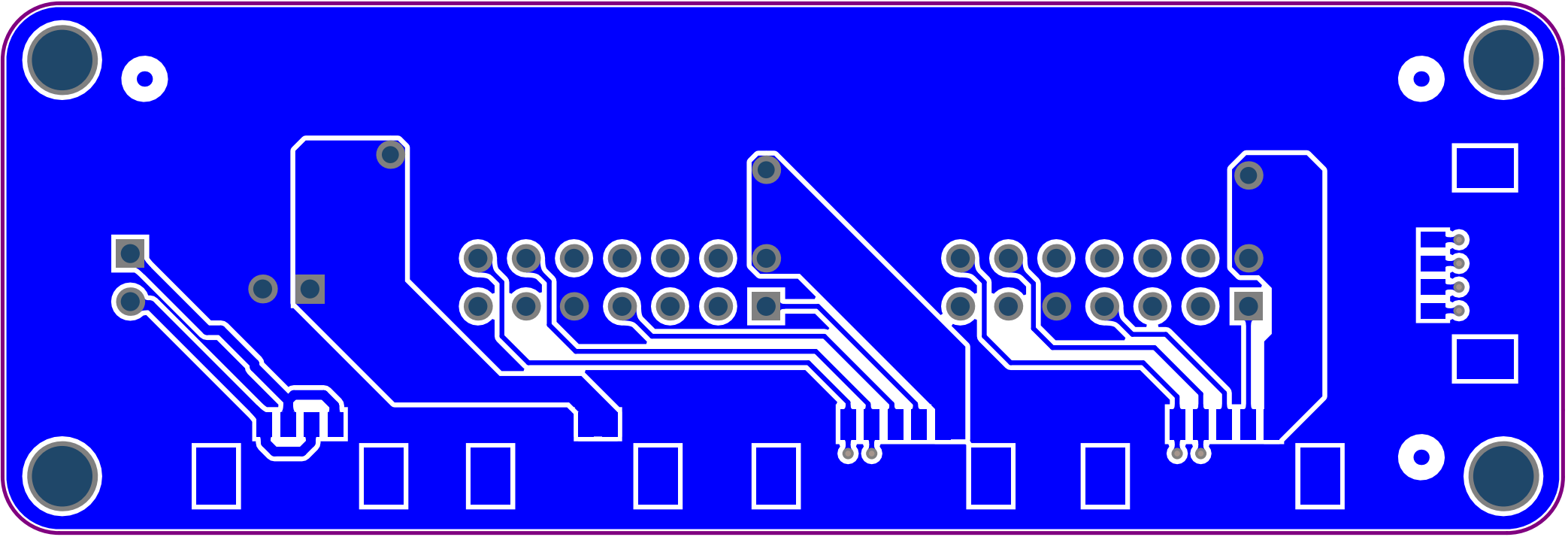
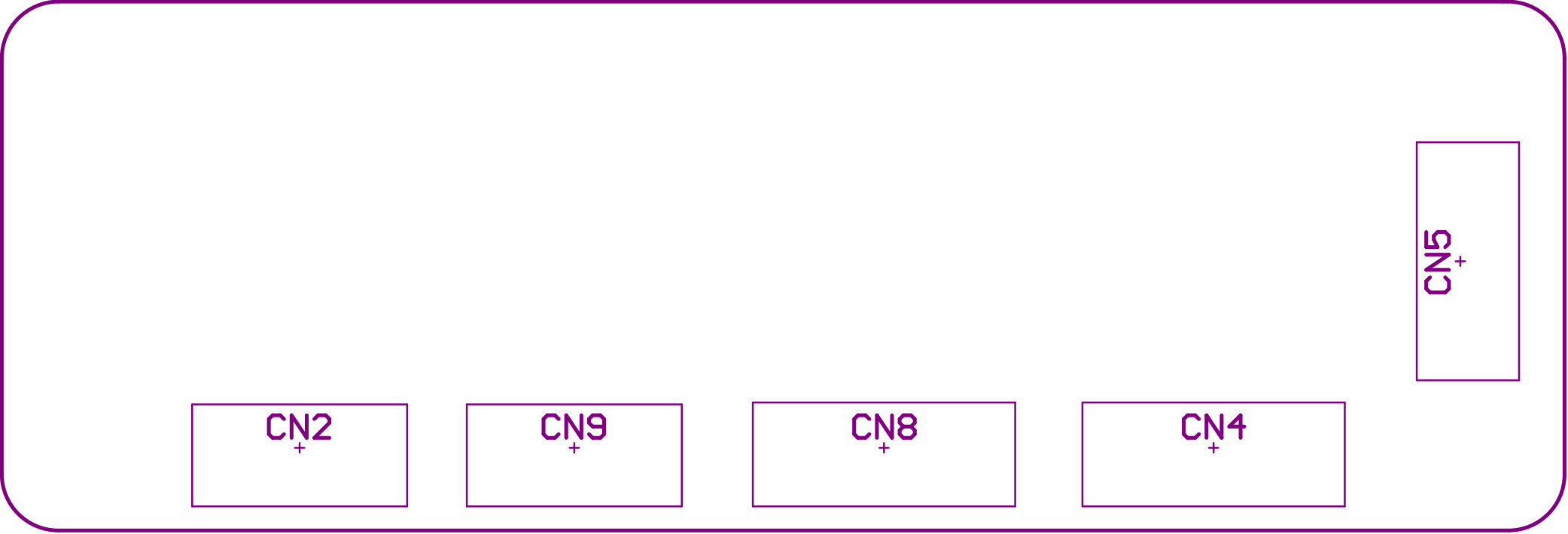
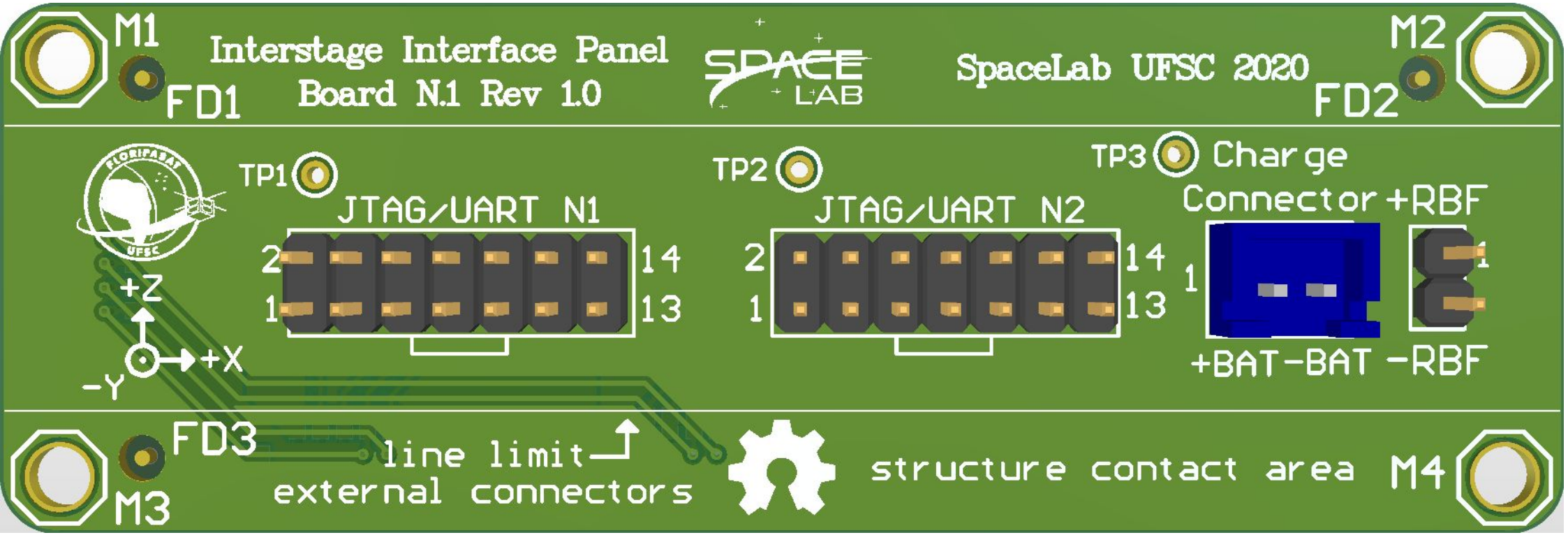
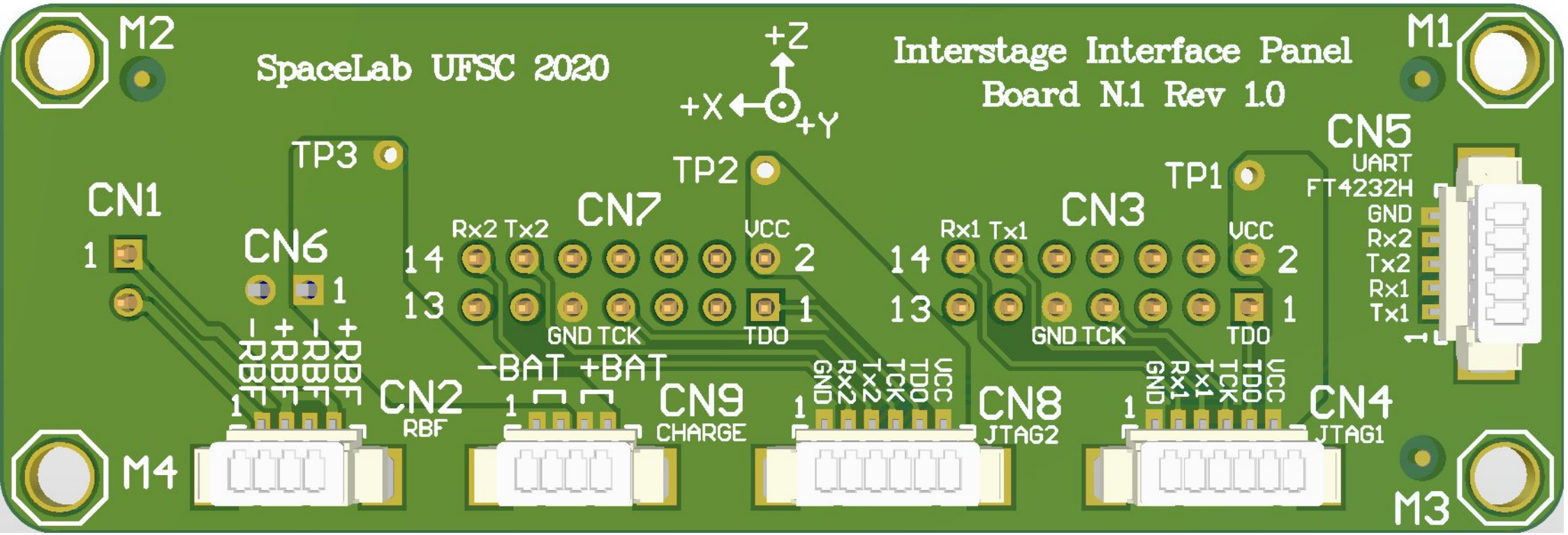

8,25 (cm)
2,80 (cm)



CN3
CN7
CN6
CN1


CN5
CN2
CN9
CN8
CN4


M1
FD1
Interstage Interface Panel
Board N.1 Rev 1.0
SPACE LAB
SpaceLab UFSC 2020
M2
FD2
TP1
JTAG/UART N1
2
1
14
13
TP2
JTAG/UART N2
2
1
14
13
TP3
Charge
Connector
+RBF
1
1
+BAT
-BAT
-RBF
+Z
+X
-Y
FD3
M3
line limit
external connectors
structure contact area
M4


M2
SpaceLab UFSC 2020
+Z
+X
+Y
Interstage Interface Panel
Board N.1 Rev 1.0
M1
TP3
TP2
TP1
CN5
UART
FT4232H
GND
Rx2
Tx2
Rx1
Tx1
CN1
1
CN6
1
RBF
+BAT
-BAT
CN7
Rx2 Tx2
VCC
14
13
2
1
GND TCK
TDO
CN3
Rx1 Tx1
VCC
14
13
2
1
GND TCK
TDO
CN2
RBF
CN9
CHARGE
CN8
JTAG2
GND
Rx2
Tx2
TCK
TDO
VCC
CN4
JTAG1
GND
Rx1
Tx1
TCK
TDO
VCC
M4
M3