Documentation of Interstage Interface Panels

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July 2020

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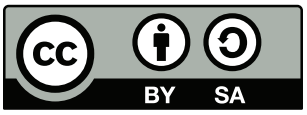
Revision Control:

Version	Author	Changes	Date
0.1	Yan Castro de Azeredo	Document creation	07/2020



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CHAPTER 1

Introduction

The Interstage Interface Panels (IIP) are three vertical mounted PCBs designed to give external access up to four modules inside of a 2U CubeSat during final assembly, integration and testing (AIT) before launch. The complete set of the boards allow the nanosatellite to be charged, programed and debugged. The usage of this hardware platform is taking into account the use of a MSP-FET: MSP430 Flash Emulation Tool from Texas Instruments for JTAG programing and debugging, UART debugging through a mini USB B port interfacing the FT4232H USB bridge IC from FTDI, a JST XH connector for charging internal batteries and a Remove Before Flight (RBF) pin header. These tools and methodology for testing are definied directly from the project main use on the GOLDS-UFSC mission [**?**] been done with the support of SpaceLab UFSC.

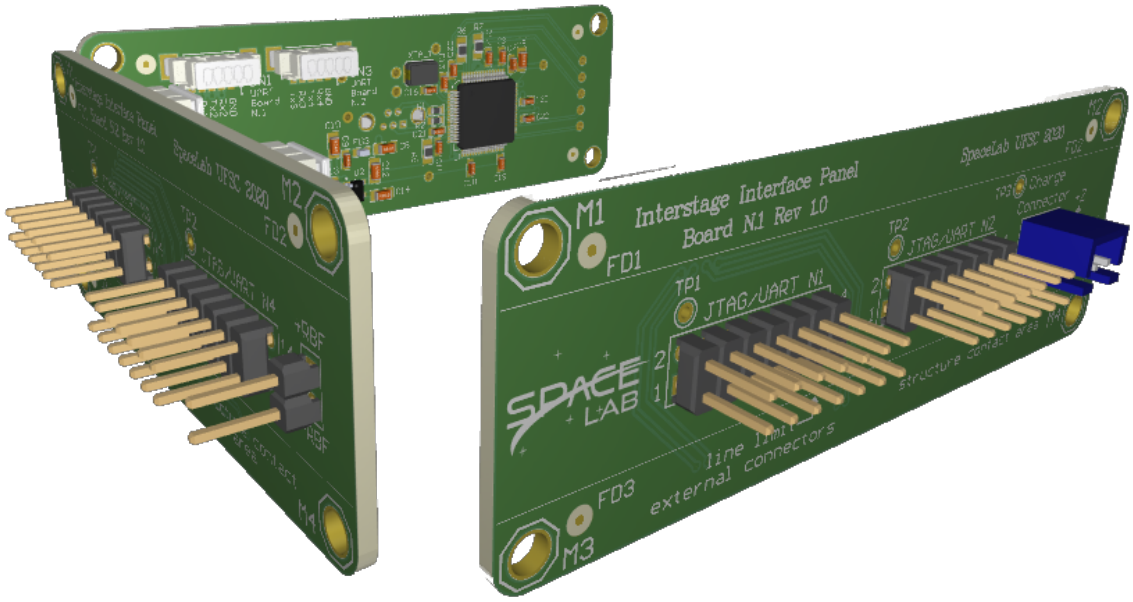

Figure 1.1: Interstage Interface Panels fullset

All the project, source and documentation files are available freely on a GitHub repository [**?**].

CHAPTER 2

System Overview

2.1 Block diagram

On figure 2.1 is displayed the full system block diagram with external devices such as the MSP-FET and a personal computer (PC) during normal usage of IIP. Up to four cubesat modules can be acessed from its interfaces, been though the pin headers or the USB port. For a specific project, the core modules (EPS, OBDH and TTC) and a optional payload are already represented with their respective interconections. These connections are done internaly with PicoBlade connectors, which are compatible with SpaceLab's modules.

2.2 Board numeration

Since the IIP is divided up to 3 boards, a numeration was adopted for better refering each PCB on this document. The numeration followed the criteria of the mounting sides determined by the carthesian coordinates of a Poly Picosatellite Orbital Deployer (P-POD) [**?**]. Starting the numeration "Nº1" from the refereced -X plane, the other boards are classified clock-wise that can be found showed on figure 2.4, each labeled axis can be better seen on figure 3.6. The boards also received names with their unique functionality, Nº1 board is also called "IIP Charge", Nº2 board the "IIP RBF" and Nº3 board the "IIP Quad UART", these nominations are present the PCBs source files. Details about the dimensions and mouting on a 2U structure can be read in the assembly chapter **??**.

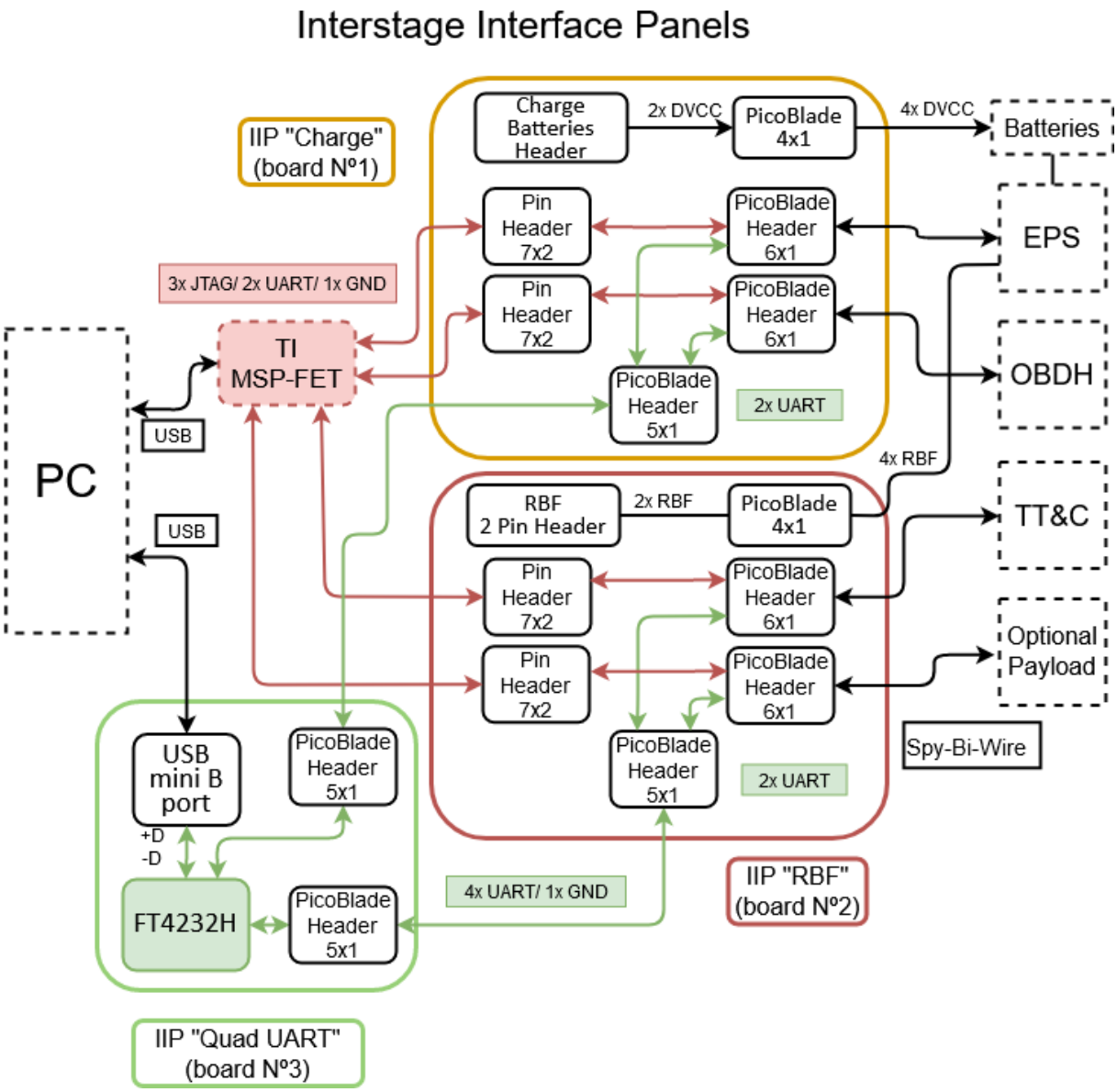

Figure 2.1: IIP hardware block diagram.

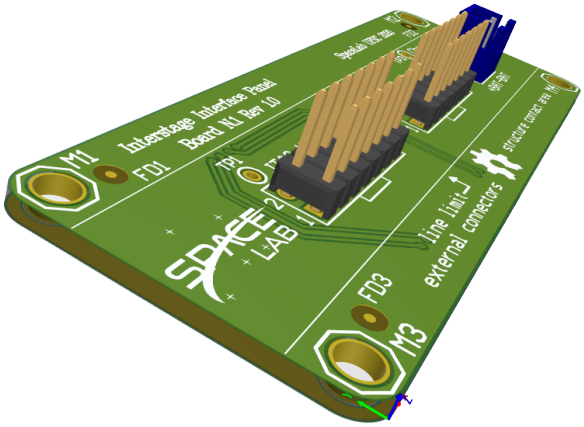

Figure 2.2: IIP Nº1 Board

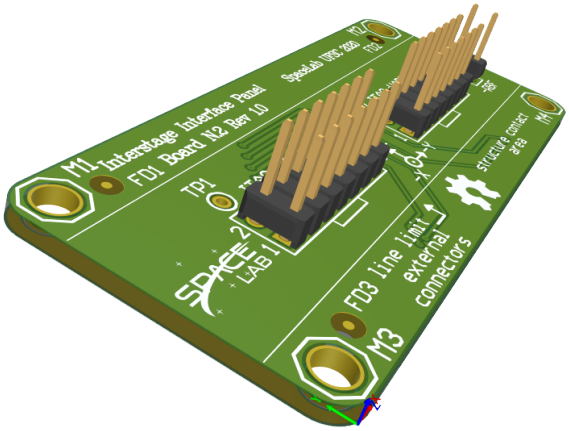

Figure 2.3: IIP Nº2 Board

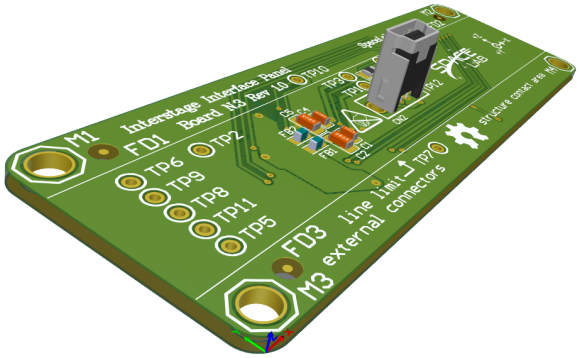

Figure 2.4: IIP Nº3 Board

CHAPTER 3

Hardware

IIP is designed to be mouted vertically on the sides of a 2U CubeSat structure and provide all the minimal features for AIT. In the following sections, the hardware design and interfaces are described in detail. On figure 3.6 is displayed top and bottom PCB prints of the three boards.

3.1 Hardware design

To be low cost, IIP has the default two layer stackup, HASL finish, 0.3mm minimal hole size, 2.54mm miminal track width and no controled impedance. While for fast USB communication it is recommended a controled impedance of 90 ohms, as exposed in USB Hardware Design Guidelines for FTDI ICs [**?**], IIP Nº3 board is not meant to operate with high speed signals. The hightest data rates for UART log messages for debbuging purposes are expected to be 115200 bps, this data rate is defined for SpaceLab's core modules. Although not a serious concern, the tracks used for the USB mini B connector to the FT4232H IC were made the shortest possible and most of the guidelines of FTDI were followed.

Components size and positioning were decided for conforming with the CubeSat 2U standard of maximum connector height on the sides of the P-POD structure [**?**] and to a specific project scenario using SpaceLab's core modules for the GOLDS-UFSC mission [**?**]. Details of all mechanical dimensions can be viewed in the assembly chapter **??**.

3.2 External and internal connectors

In this section all external and internal connectors are exposed in detail.

3.2.1 JTAG/UART pin headers

There are four 14 pin headers (7 positions and 2 rows) on IIP for JTAG and UART usage, two are present in Nº1 board and the other two in Nº2 board, they can be seem on the two figures 3.7 and 3.8. These headers were choosen to be used with MSP-FET tool and its standard cable connector. Their pionout is showed on table 3.1.

Internally these pin headers are interfaced via PicoBlades to be connected to the four modules inside the CubeSat. As can be seen in the block diagram figure 2.1 present on the overview chapter, each one of these PicoBlades is assigned to a specific module, they are showed in figures 3.9 and 3.10.

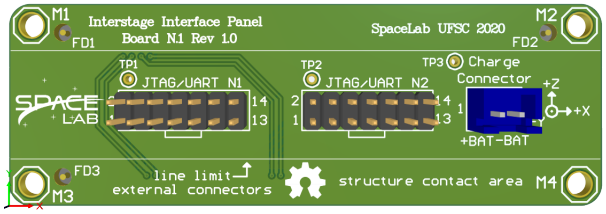

Figure 3.1: IIP Nº1 board top view.

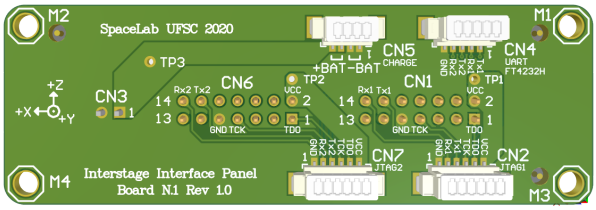

Figure 3.2: IIP Nº1 board top view

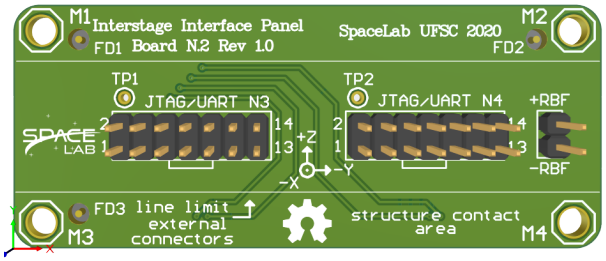

Figure 3.3: IIP Nº2 board top view

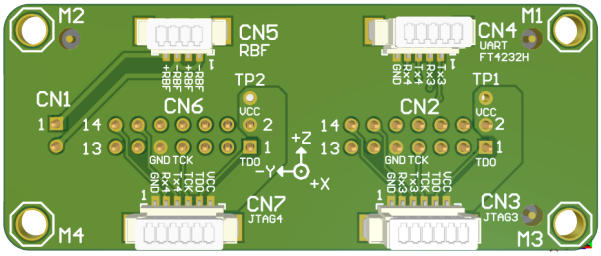

Figure 3.4: IIP Nº2 board bottom view.

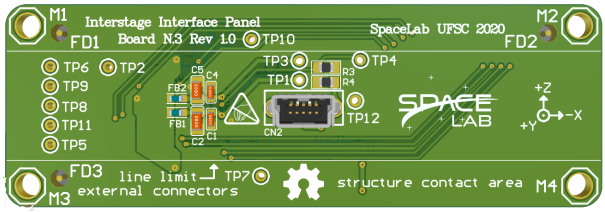

Figure 3.5: IIP Nº3 Board.

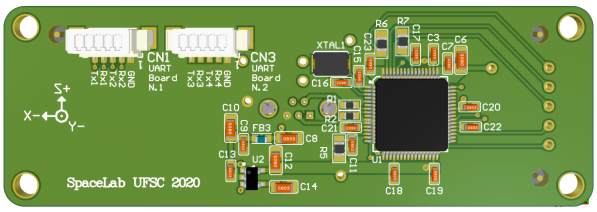

Figure 3.6: IIP Nº3 Board.

Pin [A-B]	*Row A*	*Row B*
1-2	TDO_TDI	VCC_3V3
3-4	-	-
5-6	-	-
7-8	TCK	-
9-10	GND	-
11-12	-	UART_TX
13-14	-	UART_RX

Table 3.1: JTAG pin headers pinout.

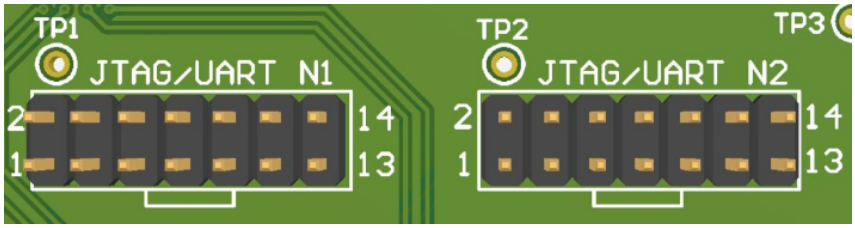

Figure 3.7: IIP Nº1 JTAG pin headers.

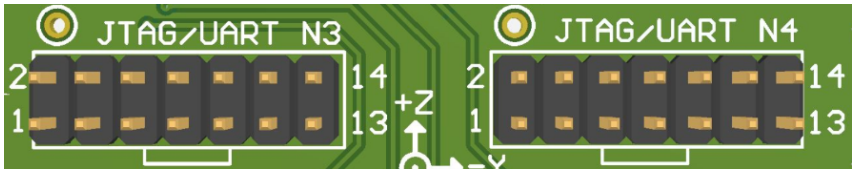

Figure 3.8: IIP Nº2 JTAG pin headers.

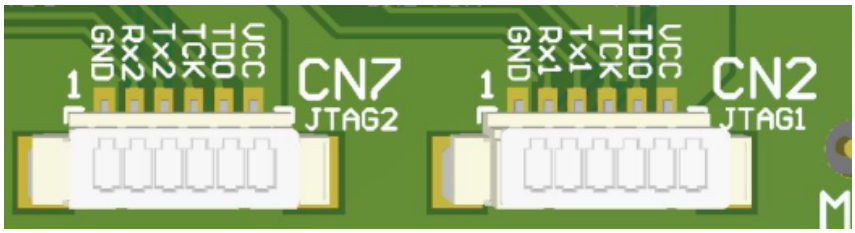

Figure 3.9: IIP Nº1 JTAG PicoBlades.

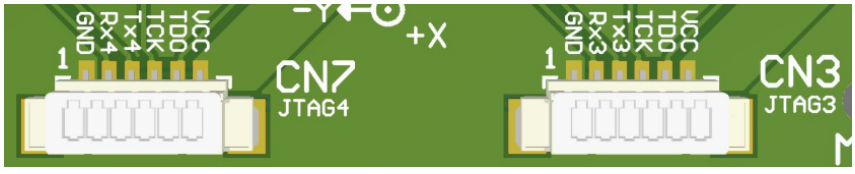

Figure 3.10: IIP Nº2 JTAG PicoBlades.

3.2.2 Charge header

On board Nº1 there is a JST XH 2 pin header for charging batteries of the CubeSat, it can be seen in figure 3.11. The component can suport up to 3000mA of current, but in practice it will be used with less than 1500mA. The internal 4 pin PicoBlade connector showed in figure 3.12 is to be connected to the EPS module to make the interconection for the JST header. The charge header also provides a detent lock for fastening and avoid mistankenly reverse connection.

Figure 3.11: IIP Nº1 charge header.

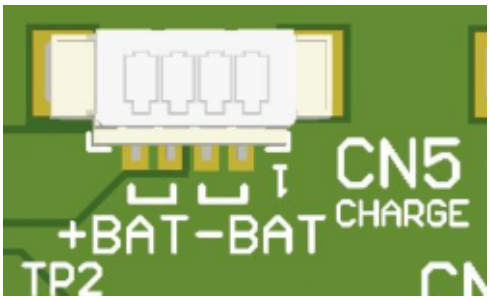

Figure 3.12: IIP Nº1 charge PicoBlade.

3.2.3 RBF pin header

The Remove Before Flight pin header is located on board Nº2, see figure 3.13. The choice of its location was according to the CubeSat Design Specification from Cal Poly SLO [**?**] that required the RBF pin to be located on the X plane of the P-POD. This ensures that the CubeSat subsystems will be powered off on test phase using a simple jumper wire conecting the pins, even with kill-swithes already enabled to do this fuctionality by been pressed againts the spring mechanism. The interconection between the header and the EPS module is done by a internal 4 pin PicoBlade, showed in figure 3.14.

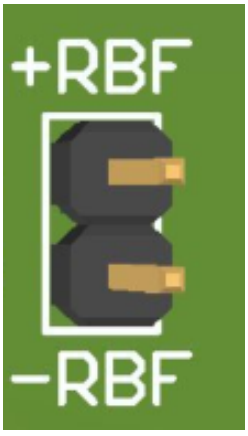

Figure 3.13: IIP Nº2 RBF pin header.

3.2.4 Mini USB B port

On board Nº3 there is a mini USB B port to be used for UART debbuging (see pcb top image **??**), this is done though the FT4323H and its subcircuitry located on the bottom

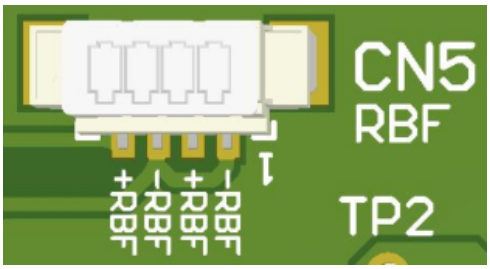

Figure 3.14: IIP Nº2 RBF PicoBlade.

side of the board (sse pcb bottom image **??**. A pad is left unsoldered for a zero-ohm resistor for a DC path or capacitor for a high-frequency path between shield and signal ground, see chapter assembly **??** for more details.

figures/usb_mini_b_port.png

Figure 3.15: IIP Nº3 USB mini B port.

figures/usb_ft4232h_circuitry.png

Figure 3.16: IIP Nº3 USB auxiliary circuitry.

CHAPTER 4

Requeriments

The Interstage Interface Panels have different hardware and software requirements depending on the variant. Both have a external JST header for charging batteries and a 2 pin header for the Remove Before Flight (RBF) Switch. The only recommended counterpart connector for charging batteries is THE XHP-2, the RBF header can be used with any commom jumper wire, the direct compatible housing is M20-1060200.

(include images)

4.1 Semi USB variant

The Semi USB uses 0.1 inch (2.54mm) spacing pin header for JTAG, any other housing can be used for own custom programing and flashing. The USB header is a mini B port, that requires a maximum cable of 5 meters, according to the standard for high speed operation (480 Mbit/s). (include images)

CHAPTER 5

Mouting Instructions

CHAPTER 6

Usage Instructions

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[4] Future Technology Devices International Ltd. USB Hardware Design Guidelines for FTDI ICs, 2014. Available at <https://www.ftdichip.com/Support/Documents/AppNotes/AN_146_USB_Hardware_Design_Guid

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