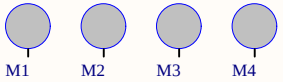
Rev	Description	Date	Author
1.0	Initial Release.		Yan C. de Azeredo

Revision History

PCB

Fidutials

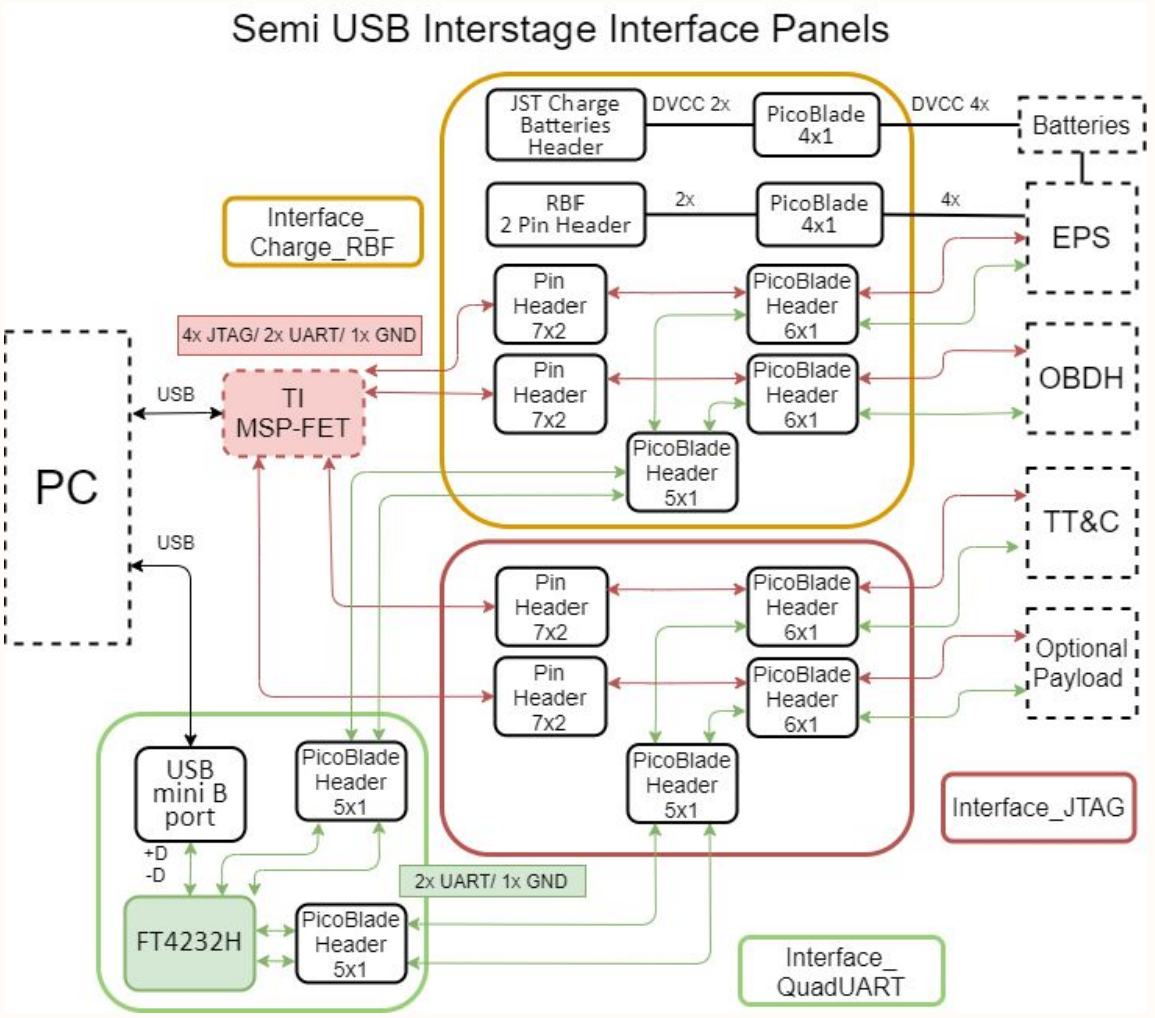
Mechanical Holes



PCB Elements

- Drawn by: Yan Castro de Azeredo
- Reviewers: Gabriel M. Marcelino and André M. P. Mattos
- Support: Gabriel M. Marcelino and André M. P. Mattos

Project Information



Full System Block Diagram

Title: 0_Architecture.SchDoc			
Size: A4	Project: 3_Interface_QuadUART.PrjPCB		Revision: 1.0
Date: 21/06/2020	Time: 11:49:20	Sheet 1 of 2	
Drawn By: Yan Castro de Azeredo		Model: Enginnering	

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Low pass LC filters for VPLL and VPHY

3V3 — 742792608 FB1 — 47R 100MHz 500mA — VPLL — TP1
C1 50V 100nF, C2 25V 4.7uF
742792608 FB2 — 47R 100MHz 500mA — VPHY — TP3
C4 50V 100nF, C5 25V 4.7uF
GND

USB VBUS Filter

742792608 FB3 — 47R 100MHz 500mA — 5V
C8 50V 10nF, C9 50V 100nF, C10 25V 4.7uF
GND

651005136421 — Mini B USB 2.0 — CN2
Vcc, D-, D+, ID, GND, Housing
USB_TX_N, USB_TX_P
R1 1kR, R2 1kR
USB_RX_N, USB_RX_P
R4 DNP 0805
USB_SHIELD, GND

Optional zero-ohm resistor for a DC path, or capacitor for a high-frequency path between shield and signal ground to minimize signal noise and provide EMC compatibility (to be tested if required).

Linear Voltage Regulator for VREGIN (LDO)

LDO specifications:
- DBV Package
- Fixed configuration
- Voltage Input (Min): 2.7 V
- Voltage Input (Max): 5.5V
- Voltage Output (Min): 3.3V
- Current Output: 200mA
- Dropout Voltage 112 mV at 200 mA

Capacitors configuration:
- Cin: 0.1uF (100nF)
- Cinr: 10nF
- Cff: 0F (fixed regulator)
- Cout: 4.7uF (recommended >2.2uF)

5V — TPS79333DBVR (IN, EN, GND, OUT, NR) — U2
C13 50V 100nF, C12 25V 4.7uF, C14 50V 10nF
3V3 test point TP7 — 3.3V
GND

Decoupling Capacitors

I/O power (VCCIO): 3.3V — C17 50V 100nF, C18 50V 100nF, C19 50V 100nF, C20 50V 100nF — GND
FT4232H core power (VCORE): 1.8V — C21 50V 100nF, C22 50V 100nF, C23 50V 100nF — GND

U1 — FT4232HL-REEL

VPLL, VPHY, 1.8V, 3.3V
Built-in 1V8 test point TP2
C3 50V 100nF, C6 25V 4.7uF, C7 50V 100nF

VREGIN, VREGOUT, DM, DP, REF, RESET#
R3 12kR, TP4
R5 10k, C11 50V 100nF, TP5

ADBUS0–ADBUS7 (TX1, RX1, TX2, RX2)
BDBUS0–BDBUS7
CDBUS0–CDBUS7 (TX3, RX3, TX4, RX4)
DDBUS0–DDBUS7

EECS, EECLK, EEDATA
R6 10k, TP6, TP9, R7 10k, TP8
OSCI, OSCO, TEST
C15 50V 12pF, C16 50V 12pF, XTAL1 12MHz
PWREN#, SUSPEND#

From FT4232H datasheet:
"If no EEPROM is connected (or the EEPROM is blank), the FT4232H will default to serial ports. The device uses its built-in default VID (0403), PID (6011) Product Description and Power Descriptor Value."

Picoblade header for board N.1 — 53398-0571 — CN1 (GND, RX2, TX2, RX1, TX1)
Picoblade header for board N.2 — 53398-0571 — CN3 (GND, RX4, TX4, RX3, TX3)

Testpoints for debugging IC
PWREN# = 0: Normal operation.
PWREN# =1: USB SUSPEND mode or device has not been configured.
SUSPEND#: Active low when USB is in suspend mode.
TP10, TP11, TP12

Title: 3_Interface_QuadUART.SchDoc		
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