

Rev	Description	Date	Author
1.0	Initial Release.		Yan C. de Azeredo

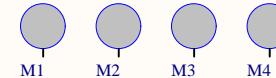
Revision History

PCB

Fidutials



Mechanical Holes



PCB Elements

Semi USB Interstage Interface Panels of FloripaSat-2 2U CubeSat

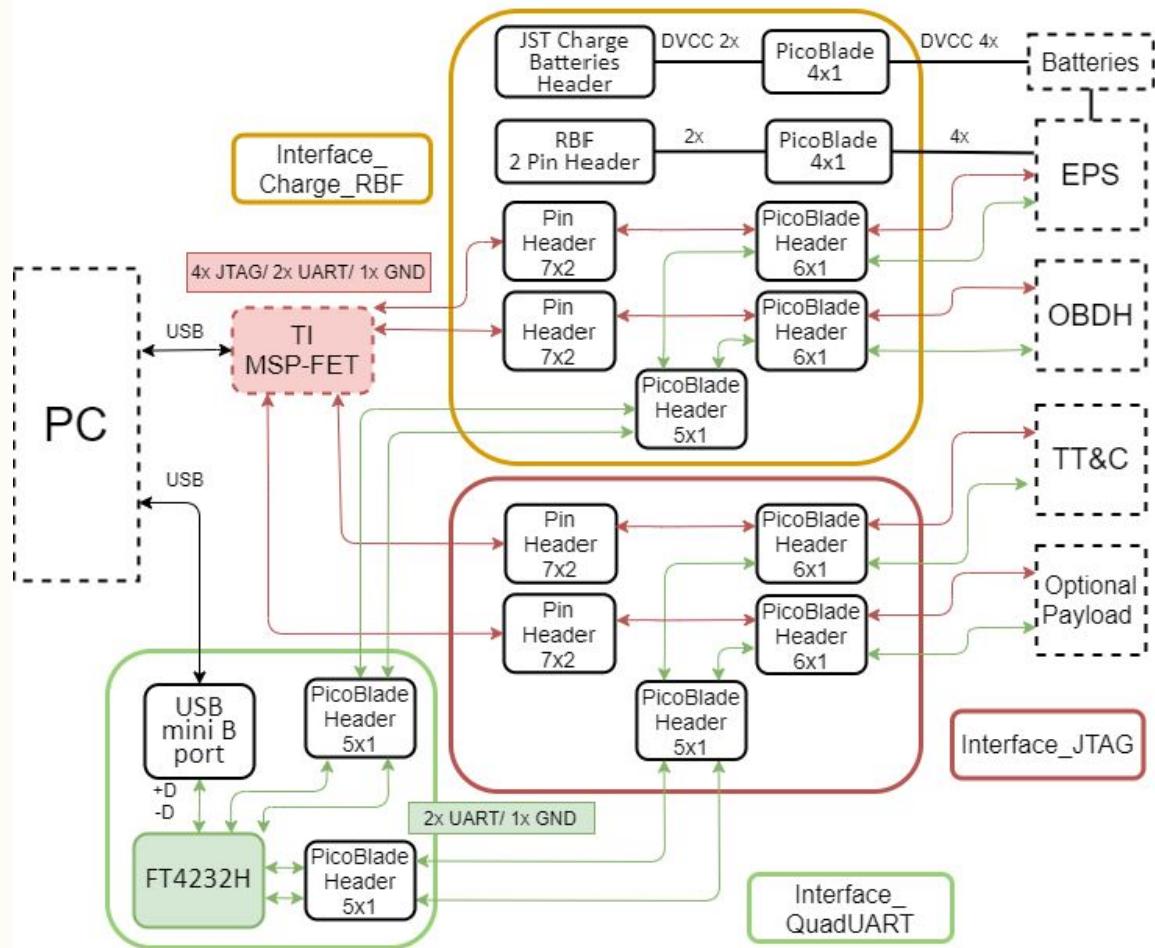
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- Drawn by: Yan Castro de Azeredo
- Reviewers: Gabriel M. Marcelino
- Support: Gabriel M. Marcelino and André M. P. Mattos

Project Information

Semi USB Interstage Interface Panels



Full System Block Diagram

Title: 0_Architecture.SchDoc		
Size: A4	Project: 2_Interface_JTAG.PnjPCB	Revision:
Date: 01/06/2020	Time: 14:21:43	Sheet 1 of 2
Drawn By: Yan Castro de Azeredo		Model: Engineering

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Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900



A

B

C

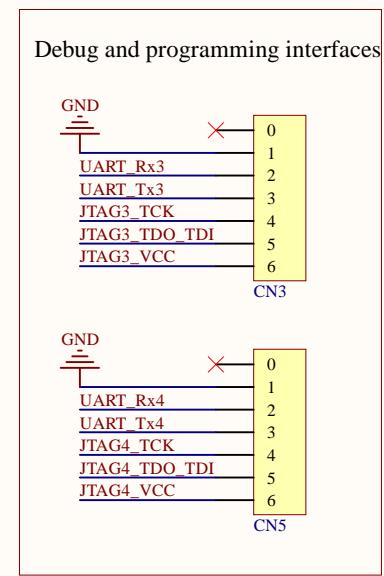
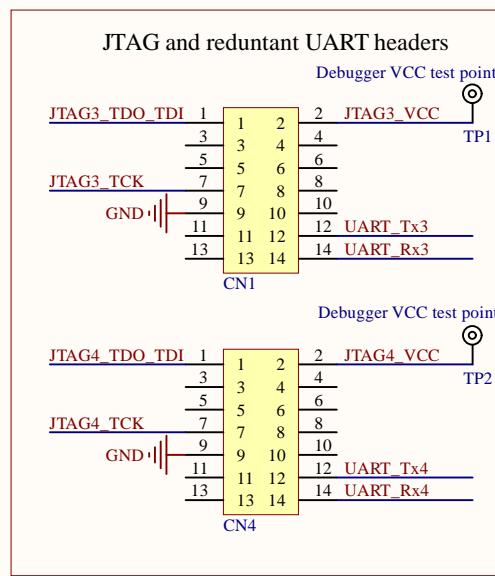
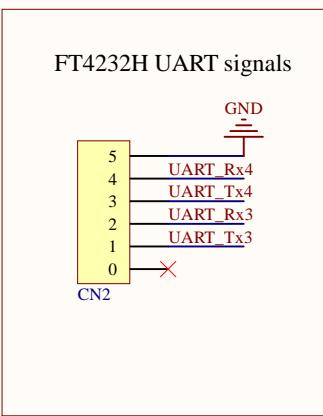
D

A

B

C

D

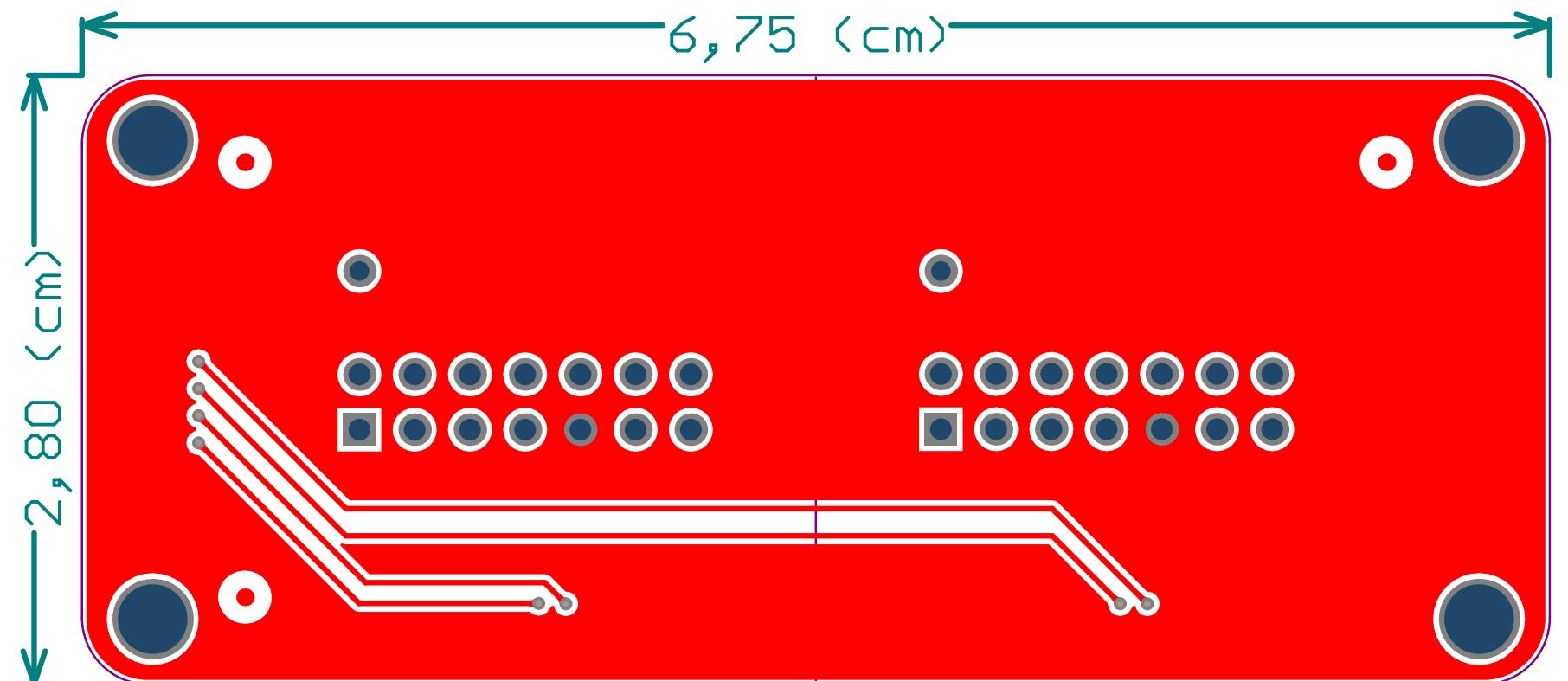


Title: 2_Interface_JTAG.SchDoc		
Size: A4	Project: 2_Interface_JTAG.PrjPCB	Revision: 1.0
Date: 01/06/2020	Time: 14:21:43	Sheet 2 of 2
Drawn By: Yan Castro de Azeredo		Model: Engineering

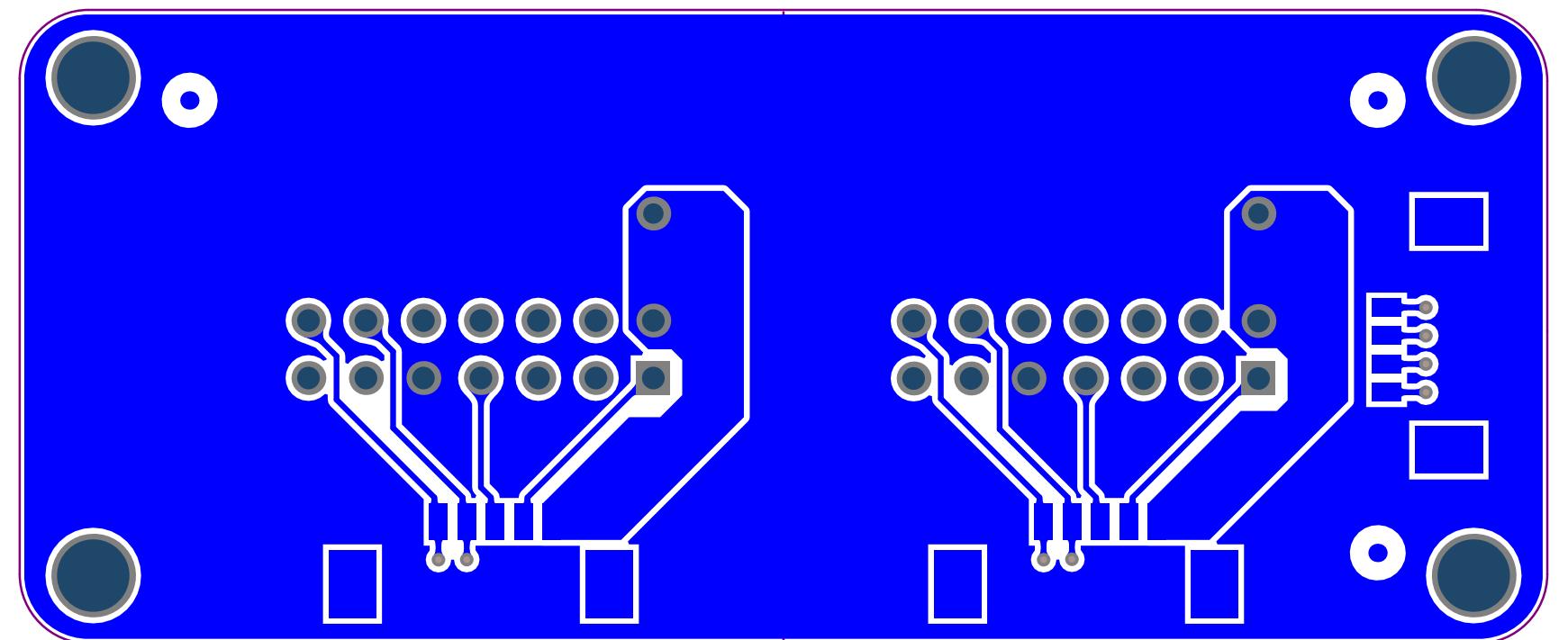
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Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,010mm	3,5	
3	Top Layer	Copper	0,036mm		
4	Dielectric 1	FR-4	1,500mm	4,8	
5	Bottom Layer	Copper	0,036mm		
6	Bottom Solder	Solder Resist	0,010mm	3,5	
7	Bottom Overlay				



TITLE: SEMI USB N.2 BOARD		REV: 1.0	DATE: DD/MM/2020
MATERIAL: FR4		Silkscreen color: white	Project: IIP FloripaSat-2
Board Thickness: 1.6mm		Layers: 02	Space Technology Research Laboratory Federal University of Santa Catarina SpaceLab UFSC
PCB Surface: ENIG		Drawing: Yan C. de Azeredo	



CN1
+

CN4
+

CN₂⁺

CN₃⁺

CN₅⁺

M1

Interstage Interface Panel
FD1 Board N.2 Rev 1.0

M2

SpaceLab UFSC 2020

FD2

TP1

JTAG/UART N3

2
1

14
13

+Z

-X

TP2

JTAG/UART N4

2
1

14
13

-Y



M3

FD3 line limit
external
connectors



structure contact
area

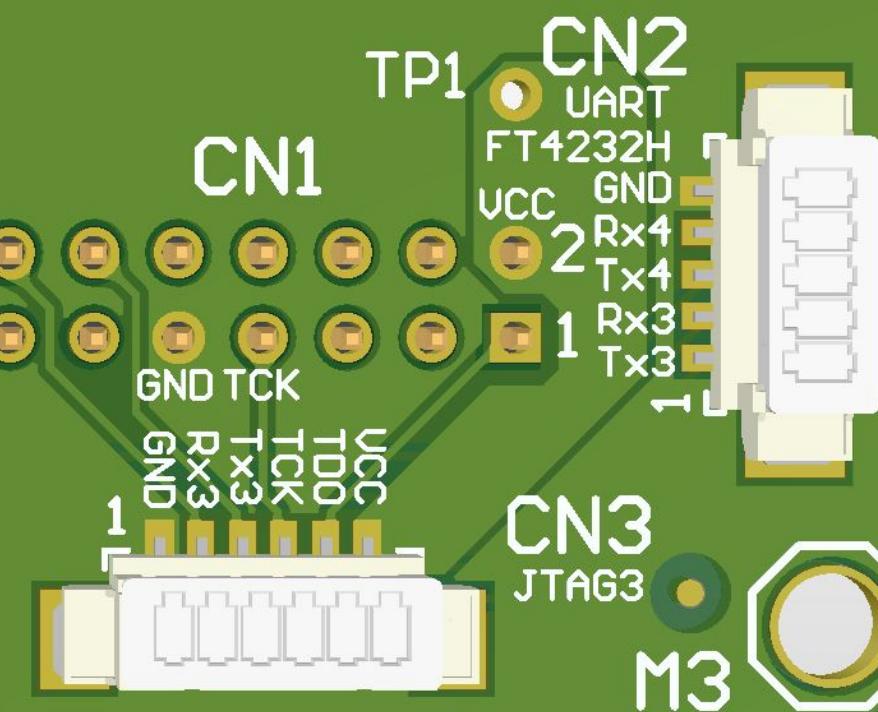
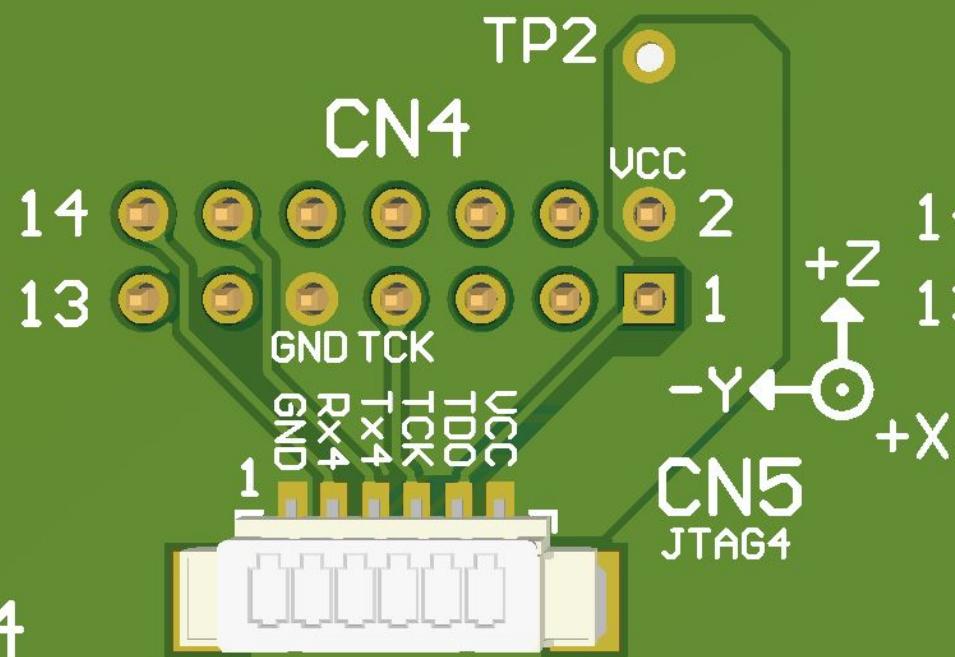
M4

M2

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M1

Interstage Interface Panel
Board N.2 Rev 1.0



M4

M3