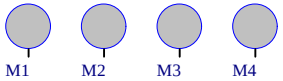
Rev	Description	Date (DD/MM/YY)	Author
1.0	Initial Release.	01/07/20	Yan C. de Azeredo
2.0	Adding fourth PCB "4_iip_closure" and "4_iip_camera" PCBs, updating mouting holes pads, block diagram, SpaceLab logo and layout of Nº3 IIP board.	28/06/21	Yan C. de Azeredo

Revision History

Fiducials

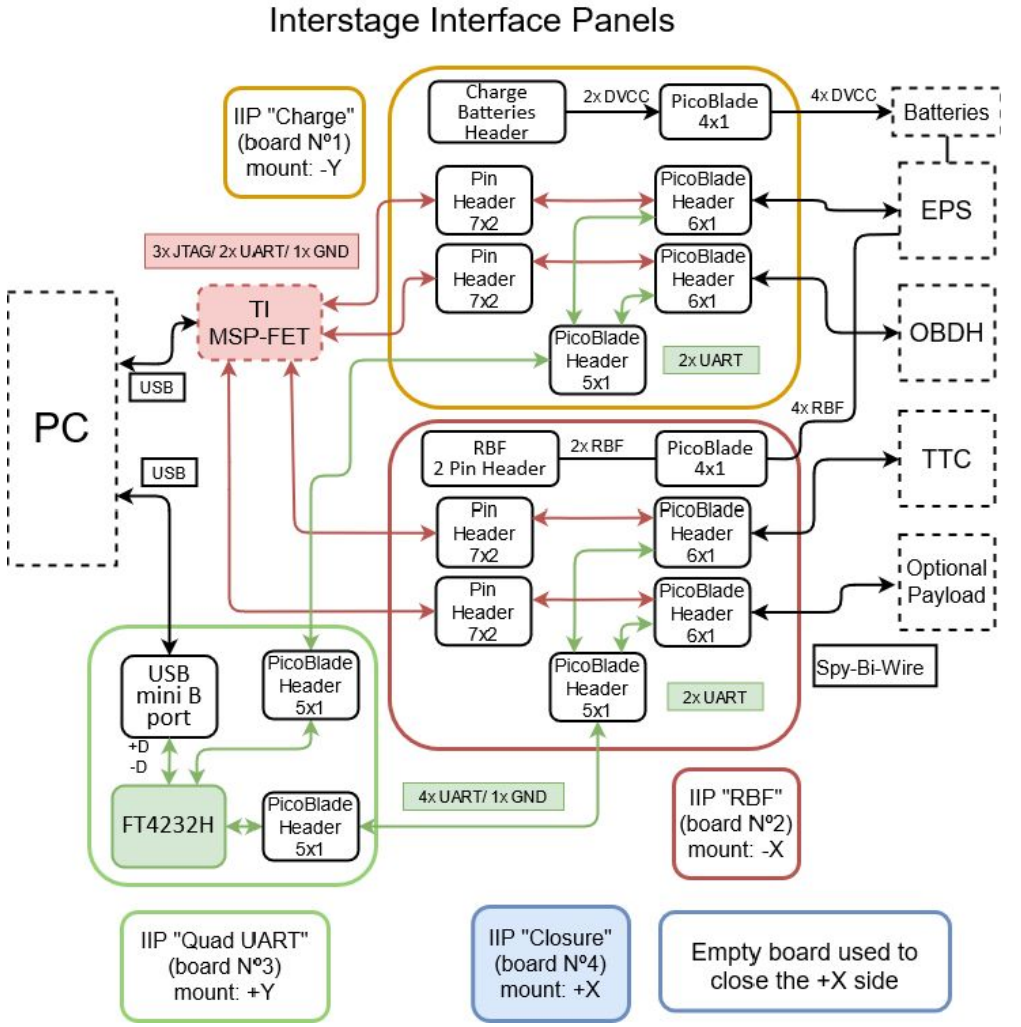
Mechanical Holes



PCB Elements

- Designed by: Yan Castro de Azeredo
- Reviewers: Gabriel M. Marcelino and André M. P. Mattos
- Support: Gabriel M. Marcelino, André M. P. Mattos and Kleber Gouveia
- Mechanical validation: Edemar M. Filho and Caique S. M. Gomes

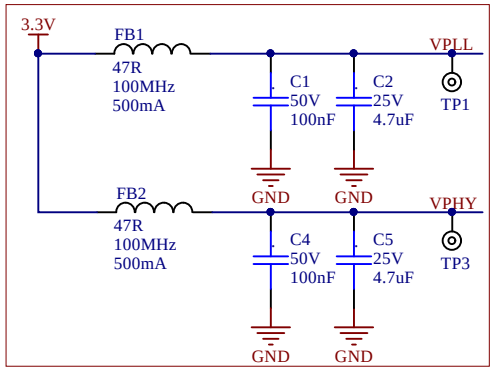
Project Information



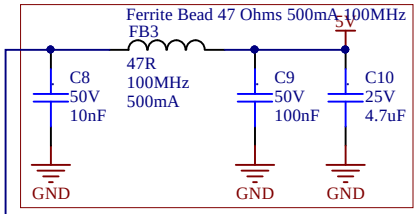
Full System Block Diagram

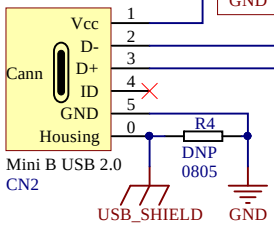
SpaceLab - Federal University of Santa Catarina			
Project: *3_iip_quad_uart.PrjPCB / [No Variations]*			
Title: *IIP Hardware Architecture*			
Designed by: *Yan Castro de Azeredo*			Project Code: *IIP*
Date: 7/1/2021	Revision: *2.0*	Sheet *1* of *2*	Size: A4

Low pass LC filters for VPLL and VPHY

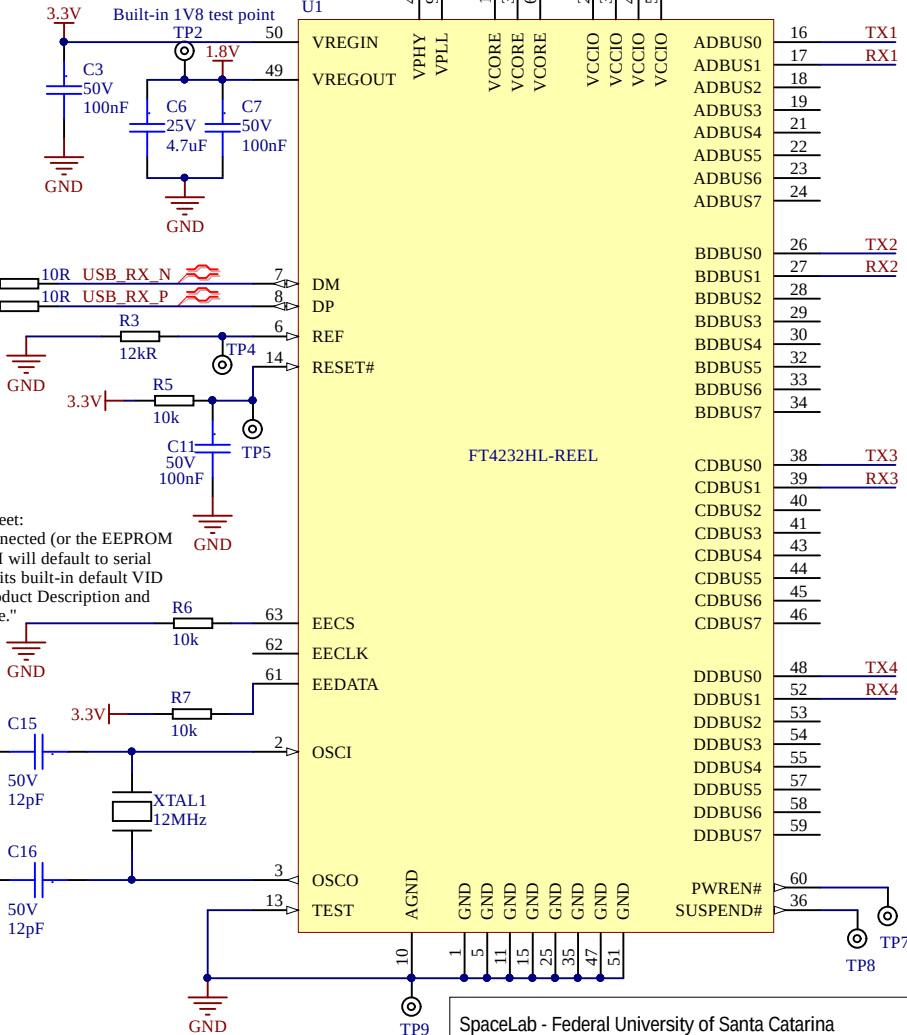


USB VBUS Filter



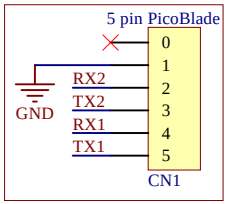


Optional zero-ohm resistor for a DC path, or capacitor for a high-frequency path between shield and signal ground to minimize signal noise and provide EMC compatibility (to be tested if required).

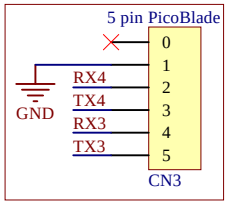


From FT4232H datasheet:
"If no EEPROM is connected (or the EEPROM is blank), the FT4232H will default to serial ports. The device uses its built-in default VID (0403), PID (6011) Product Description and Power Descriptor Value."

Picoblade header for board N.1



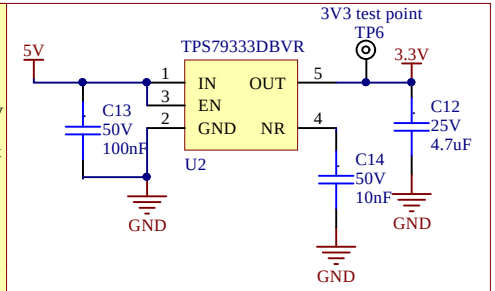
Picoblade header for board N.2



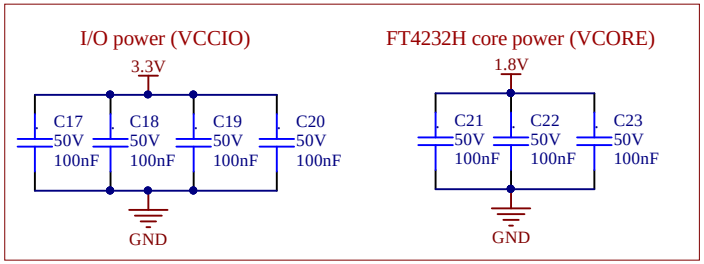
Linear Voltage Regulator for VREGIN (LDO)

LDO specifications:
- DBV Package
- Fixed configuration
- Voltage Input (Min): 2.7 V
- Voltage Input (Max): 5.5V
- Voltage Output (Min): 3.3V
- Current Output: 200mA
- Dropout Voltage 112 mV at 200 mA

Capacitors configuration:
- Cin: 0.1uF (100nF)
- Cinr: 10nF
- Cff: 0F (fixed regulator)
- Cout: 4.7uF (recommended >2.2uF)



Decoupling Capacitors



Testpoints for debugging IC

PWREN# = 0: Normal operation.
PWREN# =1: USB SUSPEND mode or device has not been configured.
SUSPEND#: Active low when USB is in suspend mode.

SpaceLab - Federal University of Santa Catarina			
Project: *3_iip_quad_uart.PrjPCB / [No Variations]*			
Title: *IIP N3 Board Interfaces and FT4232 Circuit*			
Designed by: *Yan Castro de Azeredo*			Project Code: *IIPN3*
Date: 7/1/2021	Revision: *2.0*	Sheet *2* of *2*	Size: A4