ETR03074-005

36V input, 300mA low supply current, high speed voltage regulators

■GENERAL DESCRIPTION

The XC6702 series are CMOS high-speed voltage regulator ICs with a 36 V input and low supply current.

Internal circuitry includes a reference voltage supply, error amplifier, driver transistor, over-current protection circuit, overheat protection circuit, soft start circuit, and phase compensation circuit.

The output voltage is fixed internally by laser trimming, and product selections from 1.8V to 18.0V are available.

The over-current protection circuit and overheat protection circuit are built-in, and when the output current reaches the current limit or the junction temperature reaches the temperature limit, the corresponding circuit activates.

The soft start circuit limits the rush current that flows from V_{IN} to V_{OUT} when the IC starts, enabling a stable startup sequence. The IC is put in the standby state by inputting L level into the CE pin, and the supply current is reduced to 0.1µA. A low-ESR capacitor such as a ceramic capacitor can also be used for C_L.

■APPLICATIONS

- Industrial equipment
- Domestic electrical appliances
- Portable AV devices
- Various modules

■ FEATURES

Input voltage range : 4.5V to 36.0V

(absolute maximum rating 42.0V)

Peak voltage : 46.0V (Transient≤400ms)

Output current : 300mA

: 1.8V to 18.0V (accuracy ±1%) Output voltage range

> V_{OUT} < 6.0V, 0.1V step settings V_{OUT} ≥ 6.0V, 0.5V step settings

Output voltage :±50ppm/°C (TYP.)

temperature characteristics

Supply current : 40µA (TYP.)

Dropout voltage : 350mV@ I_{OUT} =100mA,V_{OUT}=5.0V

Ripple rejection ratio : 65dB @1kHz

Standby current : 0.1µA

Protection function : Current limit.Short Protection

Thermal shutdown

Addition function : Soft start

ON/OFF (Active High)

Output capacitor : Ceramic capacitor (2.2µF) : USP-6C.SOT-89-5.

Package

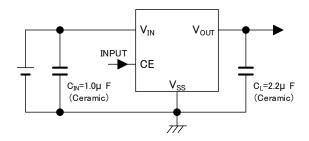
SOP-8FD

Environment friendly features : EU RoHS Directive compliant, lead free

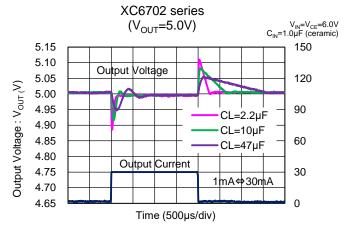
■ TYPICAL APPLICATION CIRCUIT

■TYPICAL PERFORMANCE CHARACTERISTICS

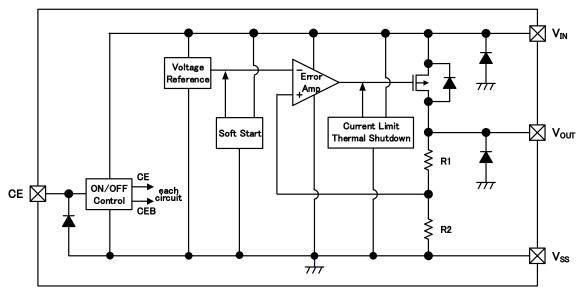
Load Transient Response



Our products are not designed to be Radiation-resistant.



■BLOCK DIAGRAM



*The above diodes are diodes for electrostatic protection and parasitic diodes.

■ PRODUCT CLASSIFICATION

1) Ordering Information

XC6702(1)(2)(3)(4)(5)(6)-(7)(*1)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
1)	Туре	D	Current Limit, Thermal Shutdown, Soft Start, ON/OFF Control
	F		For the voltage within 1.8V~9.5V:
			e.g. 3.3V → ②=3, ③=3
			5.0V → ②=5, ③=0
23	Output Voltage(*2)	18 ~ J0 ^(*3)	For the voltage within 10.0V~18.0V:
			e.g. 10.0V → ②=A, ③=0
			12.5V → ②=C, ③=5
			18.0V → ②=J, ③=0
4	Output Voltage Accuracy	1	±1%
		ER-G	USP-6C (3,000pcs/Reel)
56-7	Packages (Order Unit)	PR-G	SOT-89-5 (1,000pcs/Reel)
		QR-G	SOP-8FD (1,000pcs/Reel)

^{(*1) &}quot;-G" indicates halogen and antimony free, as well as EU RoHS compliant.

 $V_{OUT}\,<\,6.0V\,0.1V$ -step settings

 $V_{OUT} \ge 6.0V 0.5V$ -step settings

For other voltages, please contact your local Torex sales office or representative.

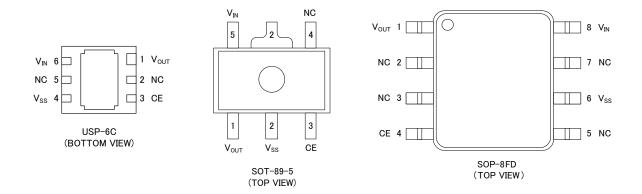
2) Selection Guide

TYPE	CURRENT LIMTTER	THERMAL SHUTDOWN	SOFT START	ON/OFF CONTROL
D	Yes	Yes	Yes	Yes

^(*2) Output voltage setting steps are as follows:

 $^{^{(*3)}}$ For 10.0V to 18.0V, A to J excluding I are used in "2".

■PIN CONFIGURATION



* For mounting strength reinforcement and heat radiation of the USP-6C and SOP-8FD radiator plates, it is recommended that soldering be performed according to the reference pattern layout and reference metal mask design.

To fix the voltage of the radiator plate, connect to Vss (Pin 4 of USP-6C or Pin 6 of SOP-8FD).

■ PIN ASSIGNMENT

	DININIANE	FUNCTIONS		
USP-6C	SOT-89-5	SOP-8FD	PIN NAME	FUNCTIONS
1	1	1	Vout	Output
2,5	4	2,3,5,7	NC	No Connection
3	3	4	CE	ON/OFF Control
4	2	6	Vss	Ground
6	5	8	V _{IN}	Power Input

■ PIN FUNCTION ASSIGNMENT

PIN NAME	SIGNAL	STATUS
	L	Stand-by
CE	Н	Active
	OPEN	Unstable

^{*} Avoid leaving the CE pin open; set to any fixed voltage.

■ ABSOLUTE MAXIMUM RATINGS

PARAMET	PARAMETER		RATINGS	UNITS
Input Volta	Input Voltage		-0.3 ~ 42.0	V
Output Curr	Output Current		600(*1)	mA
Output Volta	age	V_{OUT}	$-0.3 \sim V_{IN} + 0.3 \text{ or } 42.0^{(*2)}$	V
CE Input Vol	tage	Vce	-0.3 ~ 42.0	V
			120	
	USP-6C		1000 (40mm x 40mm Standard board)(*3)	
		_	1250 (JESD51-7 board) ^(*3)	
Power Dissipation	SOT-89-5 SOP-8FD		500	
Power Dissipation (Ta=25°C)		Pd	1300 (40mm x 40mm Standard board)(*3)	mW
(14-20 0)			1750 (JESD51-7 board) ^(*3)	
			300	
			1500 (40mm x 40mm Standard board)(*3)	
			2500 (JESD51-7 board) ^(*3)	
Surge Voltage		Vsurge	46.0(*4)	V
Operating Ambient Temperature		Topr	-40 ~ 105	°C
Junction Tempo	erature	Tj	-40 ~ 125	°C
Storage Tempe	erature	Tstg	-55 ~ 125	°C

All voltage ratings are relative to $V_{\mbox{\scriptsize SS}}.$

 $^{^{(^{*}1)}}$ Use with I_{OUT} less than Pd/(V_{IN}-V_{\text{OUT}}).

 $^{^{(\}mbox{\tiny +2})}$ The maximum value is the lower of V_{IN} + 0.3V and 42.0V

^(*3) The power dissipation figure shown is PCB mounted and is for reference only. Please refer to PACKAGING INFORMATION for the mounting condition

 $^{^{(*4)}}$ Transient \leq 400ms

■ELECTRICAL CHARACTERISTICS

			Ta=25°C		-40°C≦Ta≦105°C(*6)		°C(*6)			
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V _{IN}		4.5	-	36.0	4.5	-	36.0	V	1
Output Voltage	V _{OUT(E)} (*1)	I _{OUT} =10mA	×0.99	V _{OUT(T)} (*2) <e-0></e-0>	×1.01	×0.96	V _{OUT(T)} (*2) <e-0></e-0>	×1.04	V	1
Quiescent Current	Iss	I _{OUT} =0mA	-	40	80	-	40	90	μA	2
Stand-by Current	I _{STB}	V _{IN} =36.0V,V _{CE} =V _{SS}	-	0.01	0.10	-	0.01	2.10	μA	3
Maximum Output Current(*3)	IOUTMAX	V _{IN} =V _{OUT(T)} +2.0V	300	-	-	300	-	-	mA	1
				V _{OUT(T)} ≦	≦5.0V		V _{OUT(T)} ≦	≦5.0V		
Load Regulation	ΔV _{OUT}	V _{IN} =V _{OUT(T)} +2.0V	_	60	85	_	60	230	mV	1)
	2.001	0.1mA≦I _{OUT} ≦300mA		V _{OUT(T)} >	5.0V		V _{OUT(T)} >	-5.0V		•
				60	130		60	275		
Dropout Voltage	Vdif (*4)	I _{OUT} =100mA	-	<e-1< td=""><td>l></td><td>-</td><td><e-1< td=""><td>1></td><td>mV</td><td>1</td></e-1<></td></e-1<>	l>	-	<e-1< td=""><td>1></td><td>mV</td><td>1</td></e-1<>	1>	mV	1
Line Regulation	ΔV _{OUT} / (ΔV _{IN} •V _{OUT})	V _{OUT(T)} +0.5V≦V _{IN} ≦36.0V	-	0.01	0.03	-	0.01	0.03	%/V	1
Output Voltage Temperature Characteristics	ΔV _{OUT} / (ΔTopr·V _{OUT})		-	±50	-	-	±50	-	ppm /°C	1
Ripple Rejection Ratio	PSRR	$\begin{aligned} &V_{\text{IN}} \!\!=\!\! V_{\text{OUT}(T)} \!\!+\! 1.0 V_{\text{DC}} \!\!+\! 0.5 V_{\text{p-pAC}} \\ &I_{\text{OUT}} \!\!=\!\! 10 \text{mA}, f \!\!=\!\! 1 \text{kHz} \\ &C_{\text{IN}} \text{ Unconnected} \end{aligned}$	-	65	-	-	65	-	dB	4
Limit Current(*3)	ILIM	V _{IN} =V _{OUT(T)} +2.0V V _{OUT} =V _{OUT(E)} ×0.95	370	460	-	310	460	-	mA	1
Short - Circuit Current	I _{SHORT}	V _{OUT} =V _{SS}	-	115	-	-	115	-	mA	1
Thermal Shutdown Detect Temperature	T _{TSD}	Junction Temperature	-	150	-	-	150	-	°C	1
Thermal Shutdown Release Temperature	T _{TSR}	Junction Temperature	-	140	-	-	140	-	°C	1
Thermal Shutdown Hysteresis Width	T _{TSD} -T _{TSR}	Junction Temperature	-	10	-	-	10	-	°C	1)
Soft-Start Time(*5)	tss	V _{CE} =0V→V _{IN}	-	370	890	-	370	1100	μs	(5)
				V _{OUT(T)} ≦	≦3.3V		V _{OUT(T)} ≦	≦3.3V		
				55	95		55	155		
Inrush Current	I _{RUSH}	V _{CE} =0V→V _{IN}		3.3V <v<sub>OUT</v<sub>	_(T) ≦5.0V]	3.3V < V _{OUT}	_(T) ≦5.0V	mA	(5)
iniusii Current	IRUSH	ACE=OA → AIN	-	70	135] -	70	215	IIIA	9
				V _{OUT(T)} >	5.0V		V _{OUT(T)} >	>5.0V		
				125	210		125	330		
CE "H" Level Voltage	V _{CEH}		2.5	-	36.0	2.5	-	36.0	V	6
CE "L" Level Voltage	Vcel		Vss	-	1.2	Vss	-	1.2	V	6
CE "H" Level Current	I _{CEH}	V _{CE} =V _{IN} =36.0V	-0.10	-	0.10	-0.10	-	0.10	μA	6
CE "L" Level Current	ICEL	V _{IN} =36.0V,V _{CE} =V _{SS}	-0.10	-	0.10	-0.10	-	0.10	μА	6

 $V_{\text{IN}} = V_{\text{OUT(T)}} + 1.0 \text{V}, \ V_{\text{CE}} = V_{\text{IN}} \ , \ I_{\text{OUT}} = 1 \text{mA} \ , \ C_{\text{IN}} = 1.0 \mu \text{F} \ , \ C_{\text{L}} = 2.2 \mu \text{F} \ unless otherwise specified}.$

This parameter is tested on V_{IN} =4.5V if the input voltage is under 4.5V.

- $^{(*1)}$ $V_{OUT(E)}$: Actual output voltage value.
- $\ensuremath{^{(^{\circ}2)}}\ \ V_{OUT(T)}$: Set output voltage value.
- (*3) Differences in heat dissipation when mounted may cause activation of thermal shutdown circuit, preventing attainment of maximum output current.
- (*4) Vdif is defined as follows: $Vdif = \{V_{IN1} V_{OUT1}\}.$
 - V_{IN1} : As input voltage is gradually reduced, the input voltage at which V_{OUT1} is output.
 - V_{OUT1} : 98% of output voltage when V_{IN} is input after stabilizing sufficiently at I_{OUT} =100mA .
- $^{(5)}$ Time from input of voltage higher than CE "H" level voltage into CE pin until output voltage is $V_{OUT(T)} \times 0.9V$ or higher.
- $^{(^\circ 6)}$ The values under -40 $^\circ$ C \leq Ta \leq 105 $^\circ$ C has been tested and guaranteed by design engineering.

■ ELECTRICAL CHARACTERISTICS (Continued)

Voltage Chart 1 <E-0>

		``	-0>			
NOMINAL OUTPUT	Output Voltage					
VOLTAGE			(E) (V)	< 1050a		
	Ta=25°C			a≦105°C		
V _{OUT(T)} (V)	MIN.	MAX.	MIN.	MAX.		
1.8	1.782	1.818	1.728	1.872		
1.9	1.881	1.919	1.824	1.976		
2.0	1.980	2.020	1.920	2.080		
2.1	2.079	2.121	2.016	2.184		
2.2	2.178	2.222	2.112	2.288		
2.3	2.277	2.323	2.208	2.392		
2.4	2.376	2.424	2.304	2.496		
2.5	2.475	2.525	2.400	2.600		
2.6	2.574	2.626	2.496	2.704		
2.7	2.673	2.727	2.592	2.808		
2.8	2.772	2.828	2.688	2.912		
2.9	2.871	2.929	2.784	3.016		
3.0	2.970	3.030	2.880	3.120		
3.1	3.069	3.131	2.976	3.224		
3.2	3.168	3.232	3.072	3.328		
3.3	3.267	3.333	3.168	3.432		
3.4	3.366	3.434	3.264	3.536		
3.5	3.465	3.535	3.360	3.640		
3.6	3.564	3.636	3.456	3.744		
3.7	3.663	3.737	3.552	3.848		
3.8	3.762	3.838	3.648	3.952		
3.9	3.861	3.939	3.744	4.056		
4.0	3.960	4.040	3.840	4.160		
4.1	4.059	4.141	3.936	4.264		
4.2	4.158	4.242	4.032	4.368		
4.3	4.257	4.343	4.128	4.472		
4.4	4.356	4.444	4.224	4.576		
4.5	4.455	4.545	4.320	4.680		
4.6	4.554	4.646	4.416	4.784		
4.7	4.653	4.747	4.512	4.888		
4.8	4.752	4.848	4.608	4.992		
4.9	4.851	4.949	4.704	5.096		
5.0	4.950	5.050	4.800	5.200		

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NOMINAL OUTPUT	Output Voltage				
VOLTAGE			(E) (V)	<105°0	
		25°C		a≦105°C	
V _{OUT(T)} (V)	MIN.	MAX.	MIN.	MAX.	
5.1	5.049	5.151	4.896	5.304	
5.2	5.148	5.252	4.992	5.408	
5.3	5.247	5.353	5.088	5.512	
5.4	5.346	5.454	5.184	5.616	
5.5	5.445	5.555	5.280	5.720	
5.6	5.544	5.656	5.376	5.824	
5.7	5.643	5.757	5.472	5.928	
5.8	5.742	5.858	5.568	6.032	
5.9	5.841	5.959	5.664	6.136	
6.0	5.940	6.060	5.760	6.240	
6.5	6.435	6.565	6.240	6.760	
7.0	6.930	7.070	6.720	7.280	
7.5	7.425	7.575	7.200	7.800	
8.0	7.920	8.080	7.680	8.320	
8.5	8.415	8.585	8.160	8.840	
9.0	8.910	9.090	8.640	9.360	
9.5	9.405	9.595	9.120	9.880	
10.0	9.900	10.100	9.600	10.400	
10.5	10.395	10.605	10.080	10.920	
11.0	10.890	11.110	10.560	11.440	
11.5	11.385	11.615	11.040	11.960	
12.0	11.880	12.120	11.520	12.480	
12.5	12.375	12.625	12.000	13.000	
13.0	12.870	13.130	12.480	13.520	
13.5	13.365	13.635	12.960	14.040	
14.0	13.860	14.140	13.440	14.560	
14.5	14.355	14.645	13.920	15.080	
15.0	14.850	15.150	14.400	15.600	
15.5	15.345	15.655	14.880	16.120	
16.0	15.840	16.160	15.360	16.640	
16.5	16.335	16.665	15.840	17.160	
17.0	16.830	17.170	16.320	17.680	
17.5	17.325	17.675	16.800	18.200	
18.0	17.820	18.180	17.280	18.720	

■ ELECTRICAL CHARACTERISTICS (Continued)

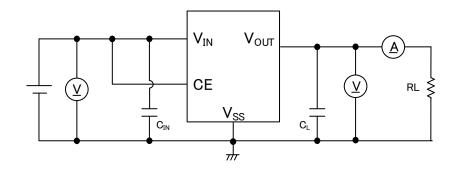
Voltage Chart 2 <E-1>

NOMINAL OUTPUT VOLTAGE	<e-1> Dropout Voltage Vdif (mV) (I_{OUT} =100mA)</e-1>			
	Ta=	25°C	-40°C≦T	a≦105°C
Vout(t) (V)	TYP.	MAX.	TYP.	MAX.
1.8	1480	2700	1480	2700
1.9	1440	2600	1440	2600
2.0	1230	2500	1230	2500
2.1	1230	2400	1230	2400
2.2	1090	2300	1090	2300
2.3	1090	2200	1090	2200
2.4	1030	2100	1030	2100
2.5	1030	2000	1030	2000
2.6	670	1900	670	1900
2.7	670	1800	670	1800
2.8	400	1700	400	1700
2.9	460	1600	460	1600
3.0		1500		1500
3.1	450	1400	450	1400
3.2		1300		1300
3.3		1200		1200
3.4		1100		1100
3.5		1000		1000
3.6		900		
3.7		800		
3.8		700		
3.9		600		
4.0				
4.1	430		430	
4.2				900
4.3				300
4.4		530		
4.5		330		
4.6				
4.7				
4.8				
4.9				

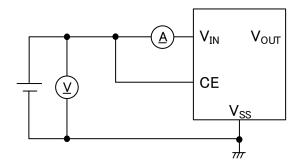
		_				
NOMINIAL			-1> :Voltage			
NOMINAL OUTPUT				(mV)		
VOLTAGE	(I _{OUT} =100mA)					
	Ta=25°C		-40°C≦Ta≦105°C			
Vout(t) (V)	TYP.	MAX.	TYP.	MAX.		
5.0						
5.1						
5.2						
5.3						
5.4						
5.5						
5.6						
5.7						
5.8						
5.9						
6.0						
6.5						
7.0						
7.5						
8.0						
8.5			350	810		
9.0						
9.5	350	440				
10.0						
10.5						
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■TEST CIRCUITS

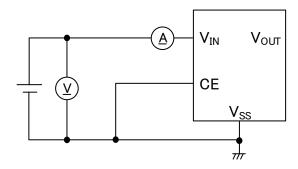
CIRCUIT(1)



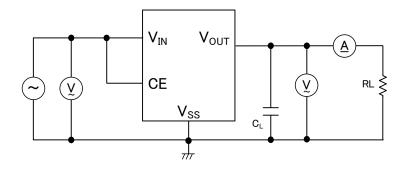
CIRCUIT②



CIRCUIT®

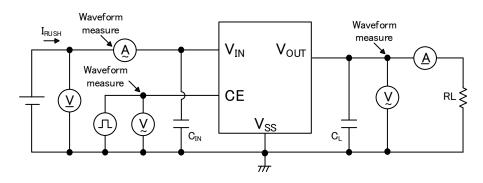


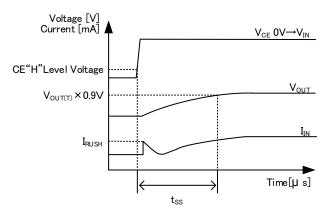
CIRCUIT4



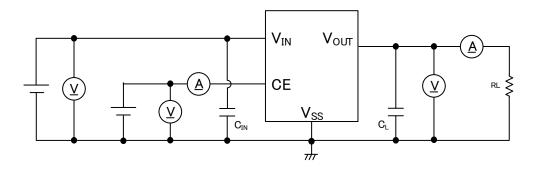
■TEST CIRCUITS(Continued)

CIRCUIT®



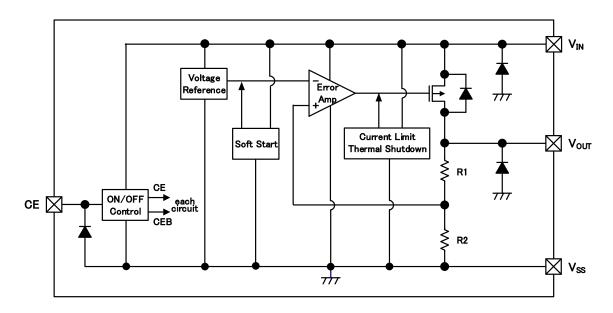


CIRCUIT®



■OPERATIONAL EXPLANATION

The XC6702 series controls the output voltage by means of a scheme in which the error amplifier compares the voltage divided by R1 and R2 connected to the V_{OUT} pin with the voltage of the internal reference power supply. The output signal from the error amplifier makes the driver transistor connected to the V_{IN} pin drive, and negative feedback is applied to stabilize the output voltage.



XC6702 Series D Type

<Current limiting, short-circuit protection>

The XC6702 series incorporates a foldback circuit for current limiting (460mA TYP.) and short-circuit protection (115mA TYP.).

When the output current reaches the current limit, the output voltage falls and the output current is limited.

<Overheating protection>

The XC6702 series incorporates a thermal shutdown circuit for overheating protection.

When the junction temperature reaches the detection temperature (150°C TYP.), the driver transistor is forcibly turned off. When the junction temperature falls to the release temperature (140°C TYP.) while the driver transistor remains in the off state, the driver transistor turns on (auto recovery) and regulation restarts. Unless the cause of rising temperature is removed, the driver transistor repeats on and off, and output waveform would be like consecutive pulses.

<CE pin>

The XC6702 series allows stopping of the IC internal circuit by a CE pin signal.

When the IC is in the stopped state by CE "L" level voltage input, the V_{OUT} pin is pulled down by R1 and R2 to the V_{SS} level.

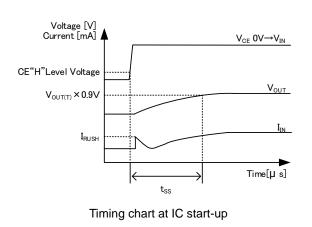
As long as the voltage input into the CE pin is within the CE pin voltage specification, the logic is established and there is no interference with operation.

If the CE pin is left open, operation is unspecified.

■ OPERATIONAL EXPLANATION (Continued)

<Soft start>

The XC6702 series limits the rush current (I_{RUSH}) that suddenly flows from V_{IN} to V_{OUT} to charge the output capacitor (C_L) when the IC starts, and is also able to limit fluctuations of V_{IN} due to I_{RUSH} . The soft start time (t_{ss}) is optimized internally (370 μ s TYP.). The soft start time (t_{ss}) is defined as the V_{OUT} reaches 90% of $V_{OUT(T)}$ from the time when CE H threshold is input to the CE pin.



XC6702D501PR-G Ta=25°C,Vin=6.0V,Iout=1mA Vce=0V→6.0V,tr=5.0us 7.5 500 CE Indut Voltage 6.0 450 CE Input Voltage : $V_{CE}(V)$ Output Voltage : $V_{OUT}(V)$ 400 4.5 Inrush Current: IRUSH 3.0 350 1.5 300 0.0 250 -15 200 rus -3.0 150 -4.5 100 -6.0 CL=2.2µF -7.5 CL=4.7µF Time (100µs/div)

Example of the inrush current wave form at IC start-up

<Low ESR capacitor support>

An internal phase compensation circuit is incorporated in the XC6702 series to enable a stable output voltage to be obtained even when a low ESR capacitor is used. To stabilize the effect of the phase compensation circuit, always connect the output capacitor (C_{L}) in direct proximity to the V_{OUT} pin and V_{SS} pin. In addition, to stabilize the input power, connect the input capacitor (C_{IN}) in direct proximity to the V_{IN} pin and V_{SS} pin. Refer to Table 1 for the recommended capacitance values to be connected.

Take particular care in selecting the capacitors for C_{IN} and C_L, as the bias dependence of the capacitor, the effect of capacitance loss due to temperature characteristics and other factors, and the effects of ESR may prevent stable phase compensation. Table 1 shows recommended capacitance values (MIN) for the actual bias and temperature conditions used for the capacitor. Select capacitances that satisfy Table 1 in all environments in which the product is to be used.

Table 1: Recommended capacitance values (MIN) of C_{IN} and C_L

OUTPUT VOLTAGE RANGE	INPUT CAPACITOR	OUTPUT CAPACITOR
V _{OUT(T)}	CIN	CL
1.8V ~ 18.0V	1.0µF	2.2µF

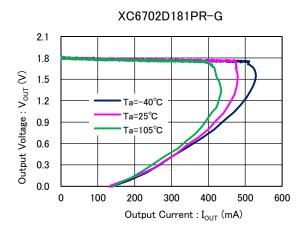
■NOTES ON USE

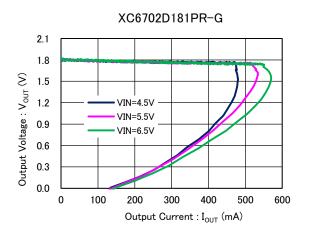
- For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
- 2) Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low between V_{IN} and V_{SS} wiring in particular.
- 3) Please wire the input capacitor (C_{IN}) and the output capacitor (C_L) as close to the IC as possible.
- 4) Capacitances of these capacitors (C_{IN}, C_L) are decreased by the influences of bias voltage and ambient temperature. Care shall be taken for capacitor selection to ensure stability of phase compensation from the point of ESR influence.
- 5) Regarding the input transient response, the undershoot at the output voltage might be larger when input voltage variation is 5.0V or larger and the through-rate is 0.5V/μs or higher. If the undershoot is not acceptable, please increase the output capacitance value and evaluate the system on your PCB well.
- 6) The IC goes into "undefined state" if the CE pin is not connected (Open state). The CE pin voltage should be fixed in low or high for stable operation.
- 7) If a capacitor with large capacitance is used on the output, the inrush current can oscillate at starting up.
- 8) Starting up the IC while the voltage less than 0V is applied to the output can lead to cases where it does not start normally.
- 9) In general, semiconductor components have a possibility to have variation of electrical specifications due to the (cosmic) radiation exposure. Therefore this product has the same possibility. Please inform us in advance if your system might have a possibility to be exposed to the (cosmic) radiation in the production process (assembly, test, etc.).
- 10) Torex places an importance on improving our products and their reliability.
 We request that users incorporate fail-safe designs and post-aging prevention treatment when using Torex products in their systems.

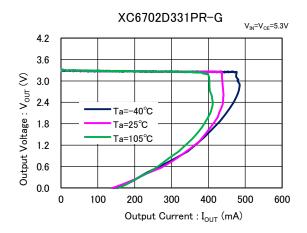
■ TYPICAL PERFORMANCE CHARACTERISTICS

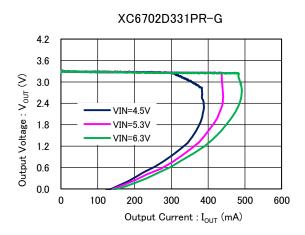
 $Ta=25^{\circ}C,\ V_{IN}=V_{OUT}(T)+1.0V,\ V_{CE}=V_{IN},\ I_{OUT}=1mA\ ,\ C_{IN}=1.0\mu F,\ C_{L}=2.2\mu F (ceramic)\ unless\ otherwise\ specified.$ This parameter is tested on $V_{IN}=4.5V$ if the input voltage is under 4.5V.

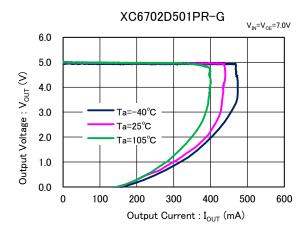
(1) Output Voltage vs. Output Current

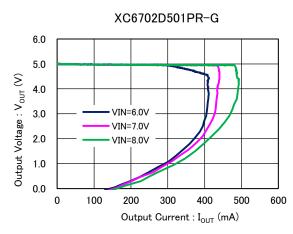








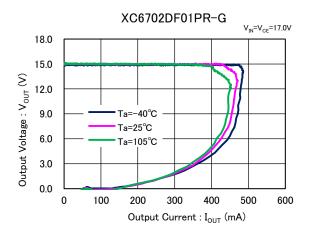


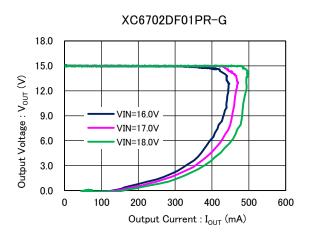


^{*} Mount conditions affect heat dissipation. Thermal shutdown may start to operate.

 $Ta=25^{\circ}C,\ V_{IN}=V_{OUT}(T)+1.0V,\ V_{CE}=V_{IN},\ I_{OUT}=1 mA\ ,\ C_{IN}=1.0\mu F,\ C_{L}=2.2\mu F (ceramic)\ unless\ otherwise\ specified.$ This parameter is tested on $V_{IN}=4.5V$ if the input voltage is under 4.5V.

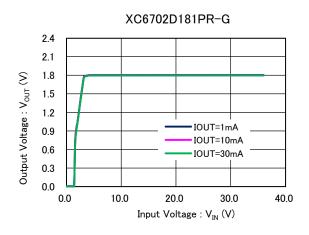
(1) Output Voltage vs. Output Current

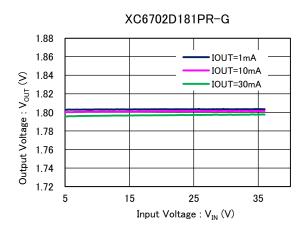


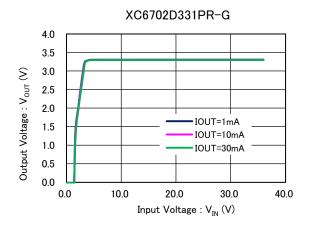


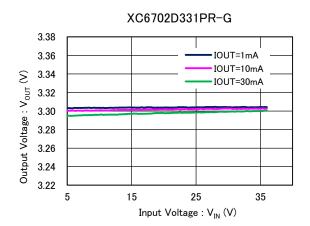
^{*} Mount conditions affect heat dissipation. Thermal shutdown may start to operate.

(2) Output Voltage vs. Input Voltage



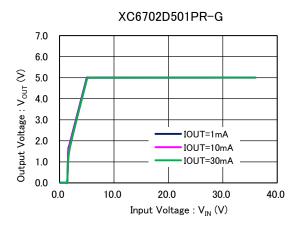


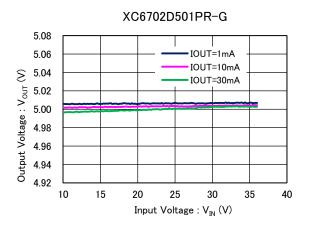


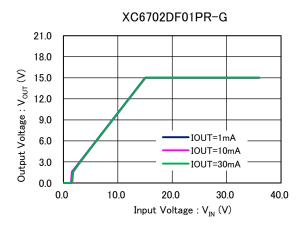


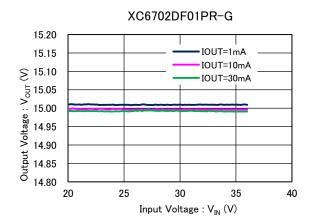
Ta=25°C, $V_{IN}=V_{OUT}(T)$ + 1.0V, $V_{CE}=V_{IN}$, $I_{OUT}=1$ mA , $C_{IN}=1.0\mu$ F, $C_L=2.2\mu$ F(ceramic) unless otherwise specified. This parameter is tested on $V_{IN}=4.5$ V if the input voltage is under 4.5V.

(2) Output Voltage vs. Input Voltage

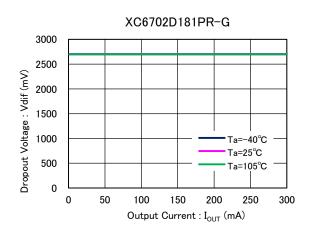


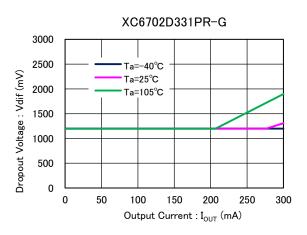






(3) Dropout Voltage vs. Output Current

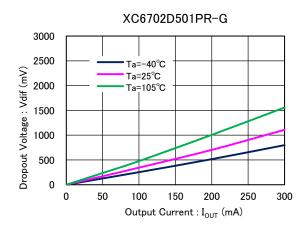


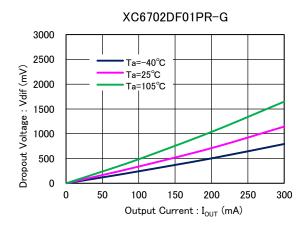


^{*} Mount conditions affect heat dissipation. Thermal shutdown may start to operate.

Ta=25°C, $V_{IN}=V_{OUT}(T)$ + 1.0V, $V_{CE}=V_{IN}$, $I_{OUT}=1$ mA , $C_{IN}=1.0\mu$ F, $C_L=2.2\mu$ F(ceramic) unless otherwise specified. This parameter is tested on $V_{IN}=4.5$ V if the input voltage is under 4.5V.

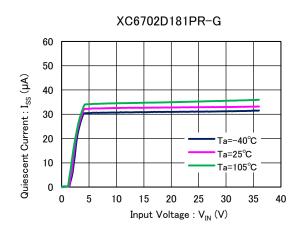
(3) Dropout Voltage vs. Output Current

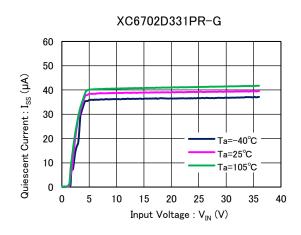


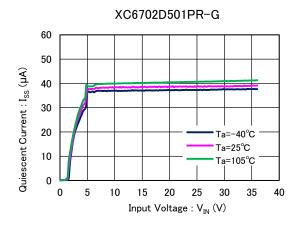


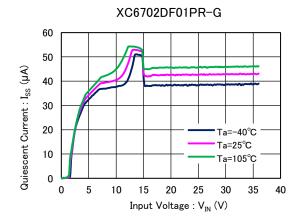
^{*} Mount conditions affect heat dissipation. Thermal shutdown may start to operate.

(4) Quiescent Current vs. Input Voltage



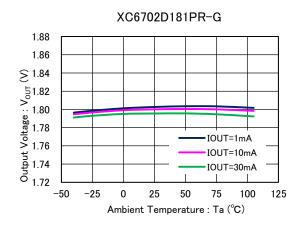


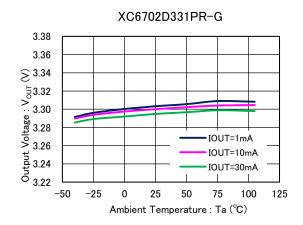


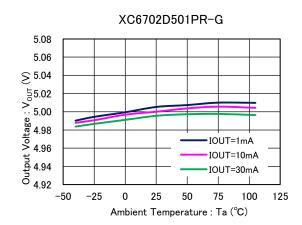


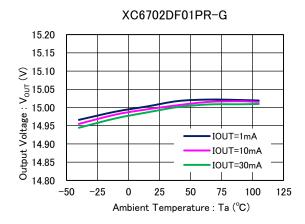
 $Ta=25^{\circ}C,\ V_{IN}=V_{OUT}(T)+1.0V,\ V_{CE}=V_{IN},\ I_{OUT}=1mA\ ,\ C_{IN}=1.0\mu F,\ C_{L}=2.2\mu F (ceramic)\ unless\ otherwise\ specified.$ This parameter is tested on $V_{IN}=4.5V$ if the input voltage is under 4.5V.

(5) Output Voltage vs. Ambient Temperature

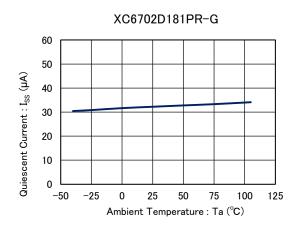


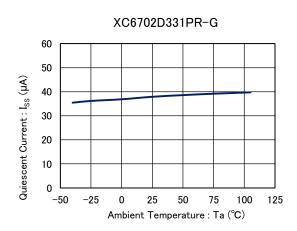






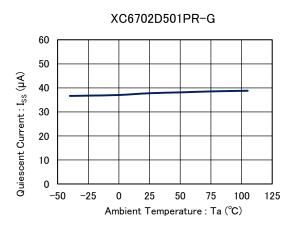
(6) Quiescent Current vs. Ambient Temperature

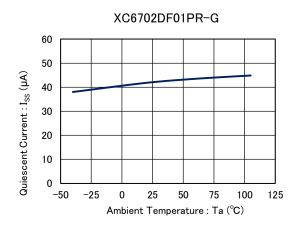




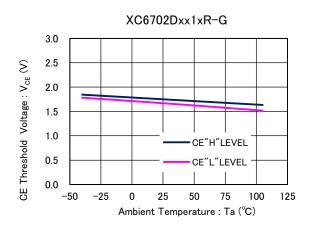
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(6) Quiescent Current vs. Ambient Temperature

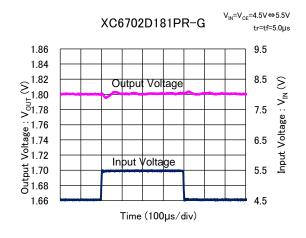


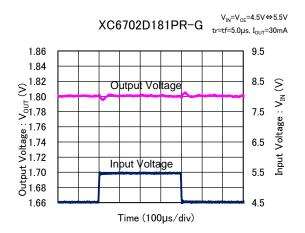


(7) CE Threshold Voltage vs. Ambient Temperature



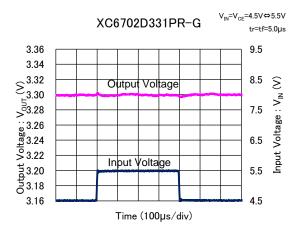
(8) Input Transient Response

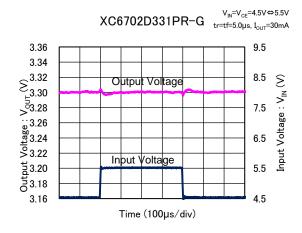


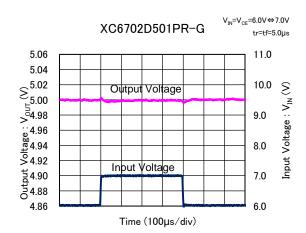


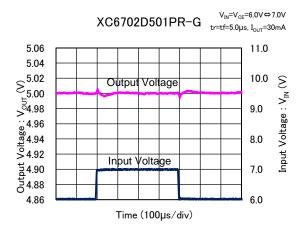
 $Ta=25^{\circ}C,\ V_{IN}=V_{OUT}(T)+1.0V,\ V_{CE}=V_{IN},\ I_{OUT}=1 mA\ ,\ C_{IN}=1.0\mu F,\ C_{L}=2.2\mu F (ceramic)\ unless\ otherwise\ specified.$ This parameter is tested on $V_{IN}=4.5V$ if the input voltage is under 4.5V.

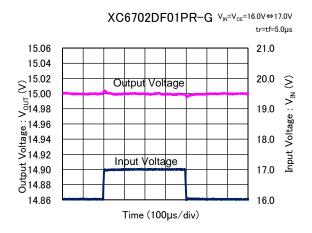
(8) Input Transient Response

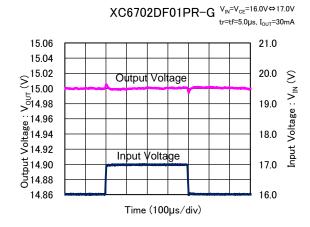






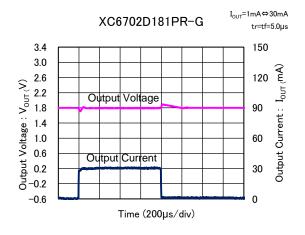


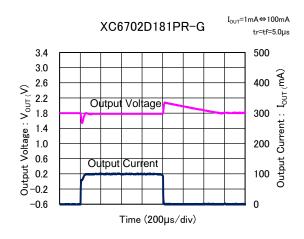


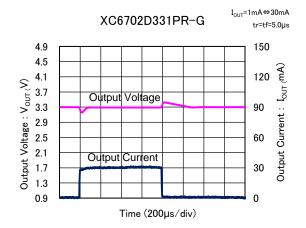


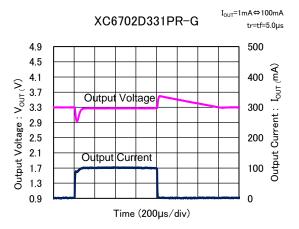
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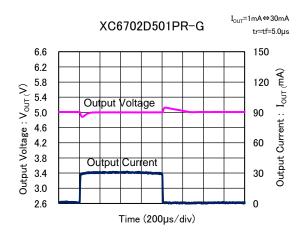
(9) Load Transient Response

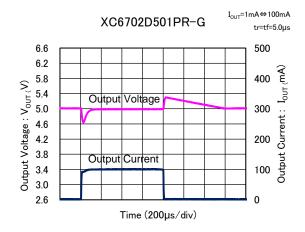






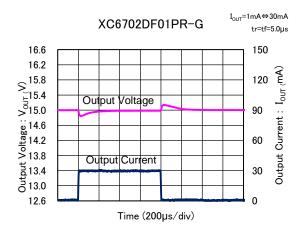


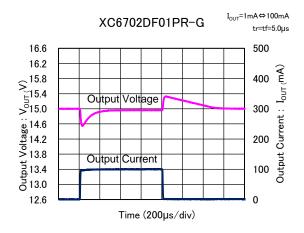




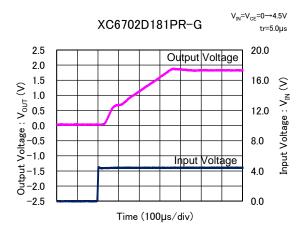
 $Ta=25^{\circ}C,\ V_{IN}=V_{OUT}(T)+1.0V,\ V_{CE}=V_{IN},\ I_{OUT}=1mA\ ,\ C_{IN}=1.0\mu F,\ C_{L}=2.2\mu F (ceramic)\ unless\ otherwise\ specified.$ This parameter is tested on $V_{IN}=4.5V$ if the input voltage is under 4.5V.

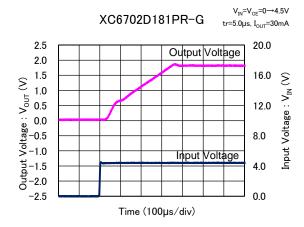
(9) Load Transient Response

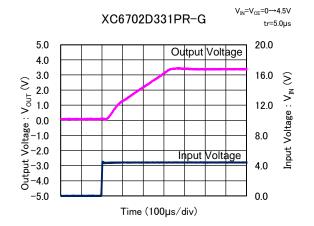


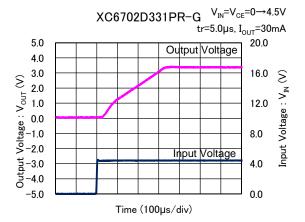


(10) Input Rising Response Time



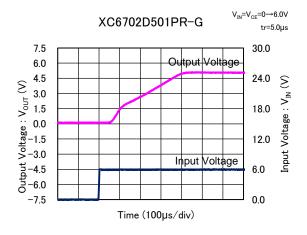


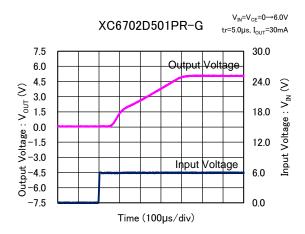


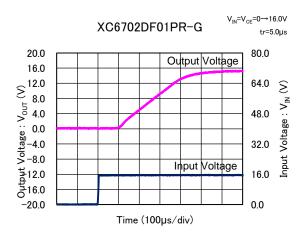


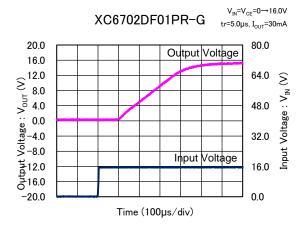
Ta=25°C, $V_{IN}=V_{OUT}(T)$ + 1.0V, $V_{CE}=V_{IN}$, $I_{OUT}=1$ mA , $C_{IN}=1.0\mu$ F, $C_L=2.2\mu$ F(ceramic) unless otherwise specified. This parameter is tested on $V_{IN}=4.5$ V if the input voltage is under 4.5V.

(10) Input Rising Response Time

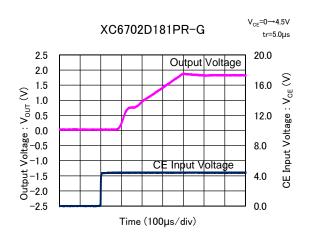


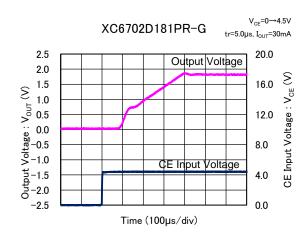






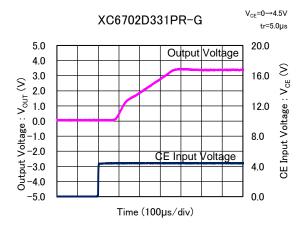
(11) CE Rising Response Time

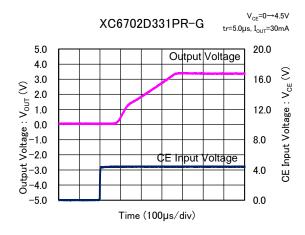


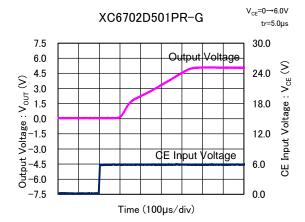


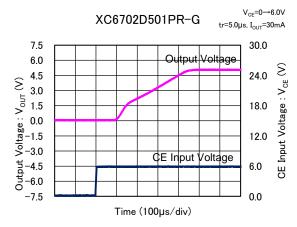
Ta=25°C, $V_{IN}=V_{OUT}(T)+1.0V$, $V_{CE}=V_{IN}$, $I_{OUT}=1mA$, $C_{IN}=1.0\mu$ F, $C_L=2.2\mu$ F(ceramic) unless otherwise specified. This parameter is tested on $V_{IN}=4.5V$ if the input voltage is under 4.5V.

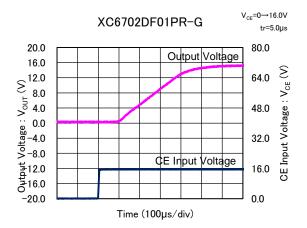
(11) CE Rising Response Time

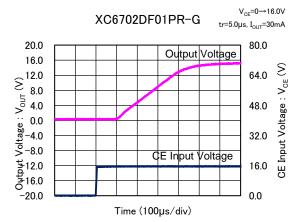






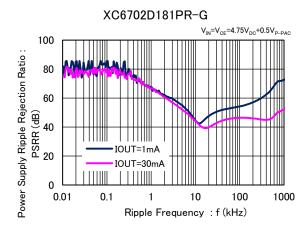


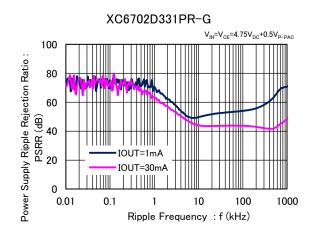


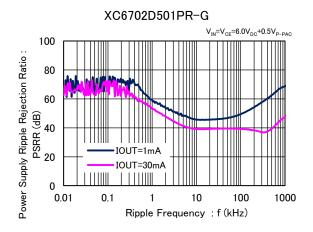


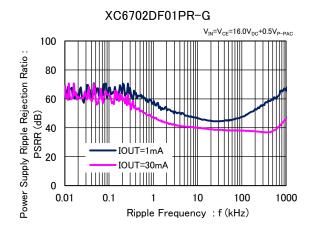
Ta=25°C, $V_{IN}=V_{OUT}(T)$ + 1.0V, $V_{CE}=V_{IN}$, $I_{OUT}=1$ mA , $C_{IN}=1.0\mu$ F, $C_L=2.2\mu$ F(ceramic) unless otherwise specified. This parameter is tested on $V_{IN}=4.5$ V if the input voltage is under 4.5V.

(12) Power Supply Ripple Rejection Ratio









■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLIN / LAND PATTERN	THERMAL CHARACTERISTICS		
SOT-89-5	SOT-89-5 PKG	Standard Board	SOT-89-5 Power Dissipation	
301-69-5	<u>301-69-3 FKG</u>	JESD51-7 Board	301-69-3 Fower Dissipation	
USP-6C	USP-6C PKG	Standard Board	USP-6C Power Dissipation	
037-00	OSF-0C FRG	JESD51-7 Board	OSF-OC FOWER DISSIPATION	
SOP-8FD	SOP-8ED PKG	Standard Board	SOP-8FD Power Dissipation	
20P-8FD	SOP-8FD PKG	JESD51-7 Board	SOI -OI DI OWEI DISSIPATION	

■MARKING RULE

●USP-6C / SOT-89-5 / SOP-8FD

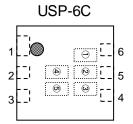
(mark header: $1 \sim 3$) *mark header does not change with a lot.

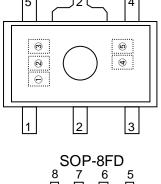
1 represents product series

MARK	PRODUCT SERIES
V	XC6702*****

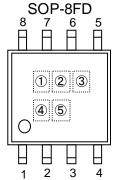
② represents type of regulators and output voltage

MARK	TYPE	OUTPUT VOLTAGE(V)	PRODUCT SERIES
4	D	1.8~3.0	
5		3.1~6.0	
6		6.1~9.0	XC6702D***** -G
7		9.1~12.0	7C0702D -G
С		12.1~15.0	
D		15.1~18.0	





SOT89-5



3 represents output voltage

MARK	OUTPUT VOLTAGE (V)					MARK	OUTPUT VOLTAGE (V)						
0	-	3.1	6.1	9.1	12.1	15.1	F	-	4.6	7.6	10.6	13.6	16.6
1	-	3.2	6.2	9.2	12.2	15.2	Н	1	4.7	7.7	10.7	13.7	16.7
2	-	3.3	6.3	9.3	12.3	15.3	K	1.8	4.8	7.8	10.8	13.8	16.8
3	-	3.4	6.4	9.4	12.4	15.4	L	1.9	4.9	7.9	10.9	13.9	16.9
4	-	3.5	6.5	9.5	12.5	15.5	М	2.0	5.0	8.0	11.0	14.0	17.0
5	-	3.6	6.6	9.6	12.6	15.6	N	2.1	5.1	8.1	11.1	14.1	17.1
6	-	3.7	6.7	9.7	12.7	15.7	Р	2.2	5.2	8.2	11.2	14.2	17.2
7		3.8	6.8	9.8	12.8	15.8	R	2.3	5.3	8.3	11.3	14.3	17.3
8		3.9	6.9	9.9	12.9	15.9	S	2.4	5.4	8.4	11.4	14.4	17.4
9		4.0	7.0	10.0	13.0	16.0	T	2.5	5.5	8.5	11.5	14.5	17.5
Α		4.1	7.1	10.1	13.1	16.1	J	2.6	5.6	8.6	11.6	14.6	17.6
В		4.2	7.2	10.2	13.2	16.2	V	2.7	5.7	8.7	11.7	14.7	17.7
С		4.3	7.3	10.3	13.3	16.3	Χ	2.8	5.8	8.8	11.8	14.8	17.8
D		4.4	7.4	10.4	13.4	16.4	Y	2.9	5.9	8.9	11.9	14.9	17.9
E		4.5	7.5	10.5	13.5	16.5	Z	3.0	6.0	9.0	12.0	15.0	18.0

4,5 represents production lot number

01~09、0A~0Z、11~9Z、A1~A9、AA~AZ、B1~ZZ in order.

(G, I, J, O, Q, W excluded)

^{*} No character inversion used.

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