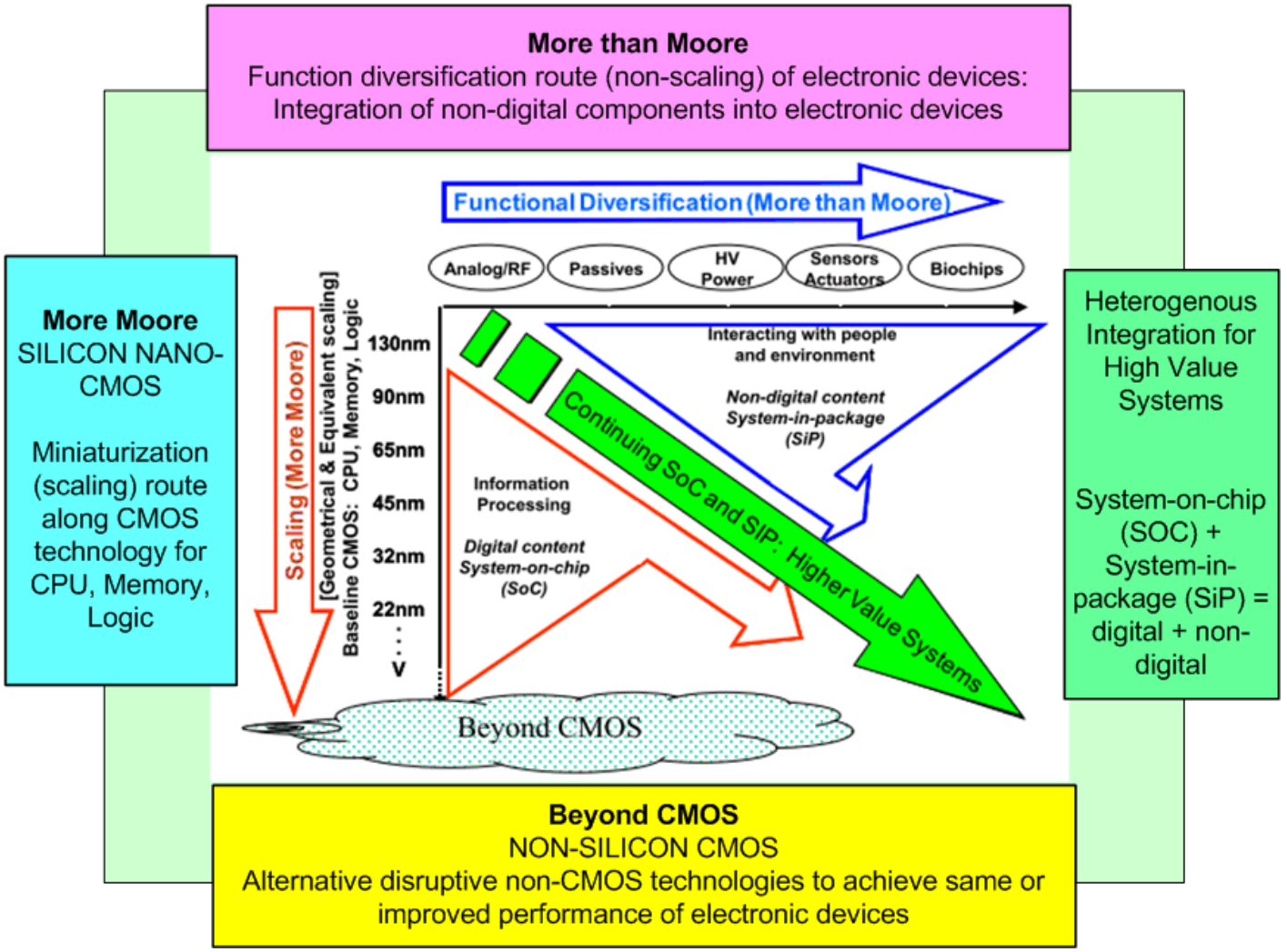
Single Electron Transistor

Outline

- **SET integration**
- **SET operation**
- **SET Application**
- **SET fabrication**
- **SET-CMOS hybridization**
- **Hybrid SET-CMOS co-simulation**
- **Hybrid SET-CMOS logic design, analysis and simulation**
- **SET logic drivability & its enhancement**
- **SET vs CMOS logic**
- **Future recommendations**

Future of microelectronics and nanoelectronics



Nanoelectronics Technology Development Paths [ITRS, 2009].

Logic Technology Tables

Table 1 – Extending MOSFETs to the End of the Roadmap

CNT FETs
Graphene nanoribbons
III-V Channel MOSFETs
Ge Channel MOSFETs
Nanowire FETs
Non-conventional Geometry Devices

Table 2- Unconventional FETS, Charge-based Extended CMOS

Tunnel FET
I-MOS
Spin FET
SET
NEMS switch
Negative Cg MOSFET

Table 3 - Non-FET, Non Charge-based 'Beyond CMOS' devices

Collective Magnetic Devices
Moving domain wall devices
Atomic Switch
Molecular Switch
Pseudo-spintronic Devices
Nanomagnetic (M:QCA)

2011 ITRS

Single electron transistor (SET) –CMOS hybridization

SET logic

- ✓ Scaling potential
- ✓ Ultra low power dissipation
- ✓ New functionalities
- ✓ Room temperature operation

- ✗ Reproducibility at nanoscale
- ✗ Low Current drive (~nA)
- ✗ Back ground charge effect

CMOS logic

- ✓ High gain and current drive
- ✓ High Speed
- ✓ Very stable & matured fabrication technology

- ✗ Power density
- ✗ Sub 10 nm physical limits & process variations at nanoscale

CMOS advantage can compensate SET disadvantage
SET advantage can compensate CMOS disadvantage

SET circuits can be stacked above CMOS platform to achieve:

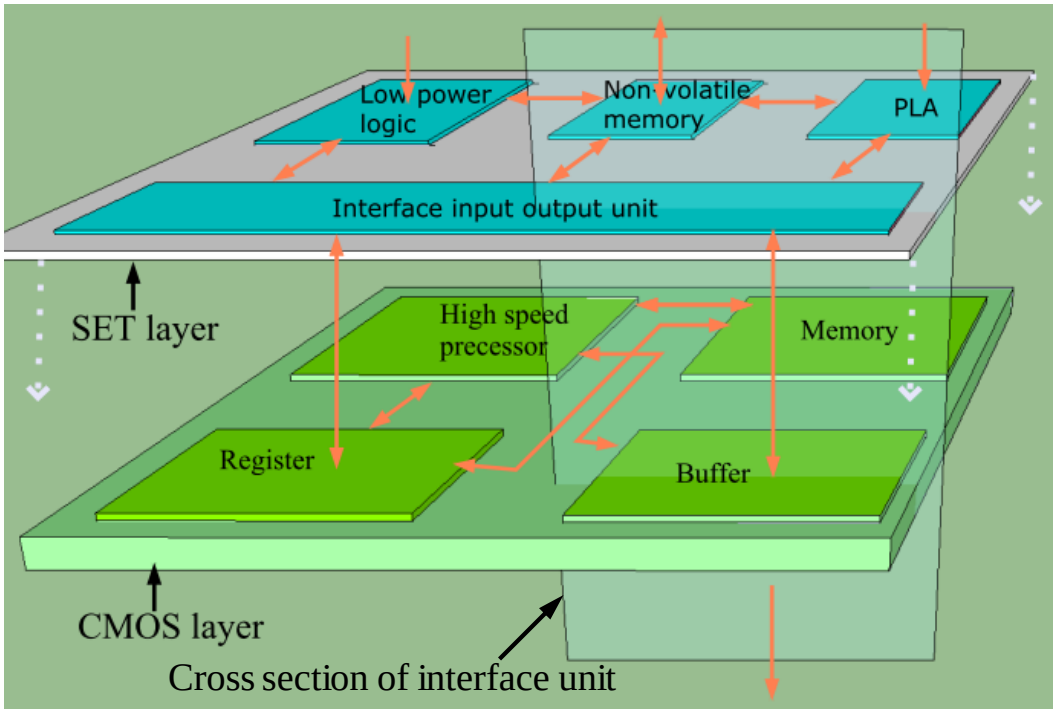
- Functional and heterogeneous 3-D integration .
- Low cost, low thermal budget, improving yield of ICs.

SET-CMOS 3-D integration

In hybrid SET-CMOS ICs,

- SET based design is more efficient for local architecture and its interconnect and the hybrid SET-CMOS design for global interconnect.
- CMOS is essential for I/O, signal restoration, and maintaining compatibility with the established technology.

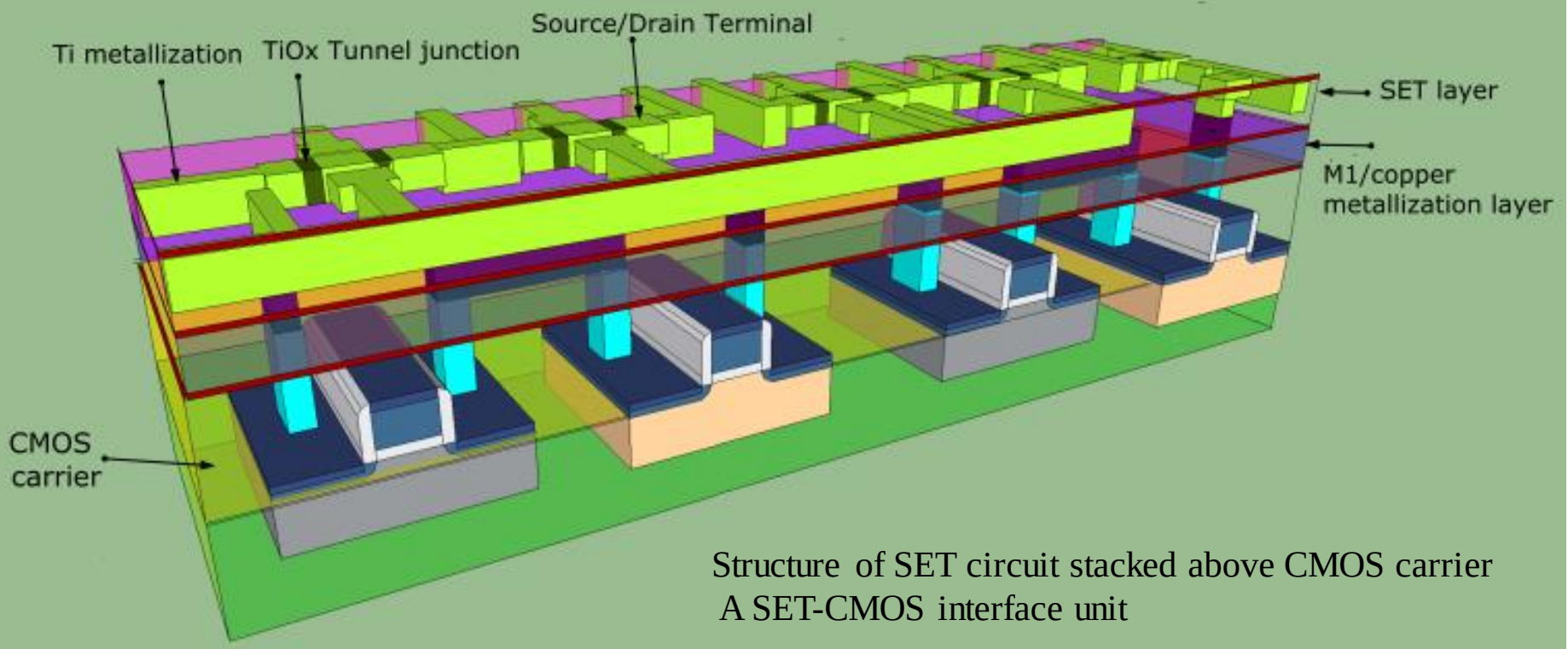
Address interfacing issue wherein we exploit the maximum capability of SET logic in terms of driving capability, voltage response & power for room temperature operation.



SET-CMOS 3-D integration

Section of SET-CMOS interface unit

It is necessary to demonstrate the SET logic driving capability for CMOS with sufficient current drive and output voltage at room temperature.



Structure of SET circuit stacked above CMOS carrier
A SET-CMOS interface unit

Basics of Single-Electron Tunneling

- Capacitor stores energy :

  $E_C = C \times V^2/2$

- To charge a capacitor by *1e* requires potential difference

  $V = e/C,$

- The charging energy E_C

$$E_C = C\frac{V^2}{2} = C\frac{\left(\frac{e}{C}\right)^2}{2} = \frac{e^2}{2C}$$

- To observe SET effects the following condition must be fulfilled

  $E_C >> kT$

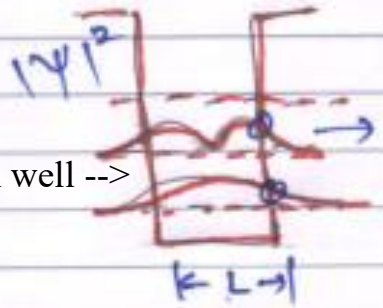
- To pass the current capacitor must be "leaky", but not too leaky (tunnel junction):
  - Typical charge/discharge time $\Delta t = RC$
  - From Heisenberg uncertainty principle:

$$\Delta E \cdot \Delta t = \frac{e^2}{2C} RC > \frac{\hbar}{2}$$

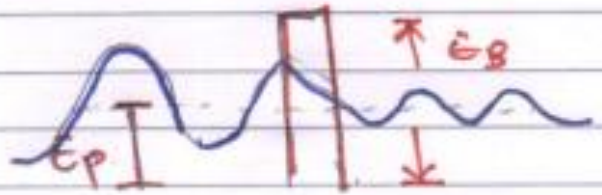
$$R_J > \frac{h}{e^2} \qquad C < \left(\frac{kT}{e}\right)\frac{1}{e}$$

Tunneling.

- by decreasing particle size we can confine an electron.



→ some probability



2 Rules. COULOMB BLOCKADE.

#1. ← holds e together.

e⁻ repelling.

$\epsilon_c \geq k_B T$

$\epsilon_c = \frac{e^2}{2C_{DOT}}$

how much charge can be stored

$C_{DOT} = C_1 \Sigma d$

ϵ_c → energy required to add one more electron to DOT

Uncertainty principle.

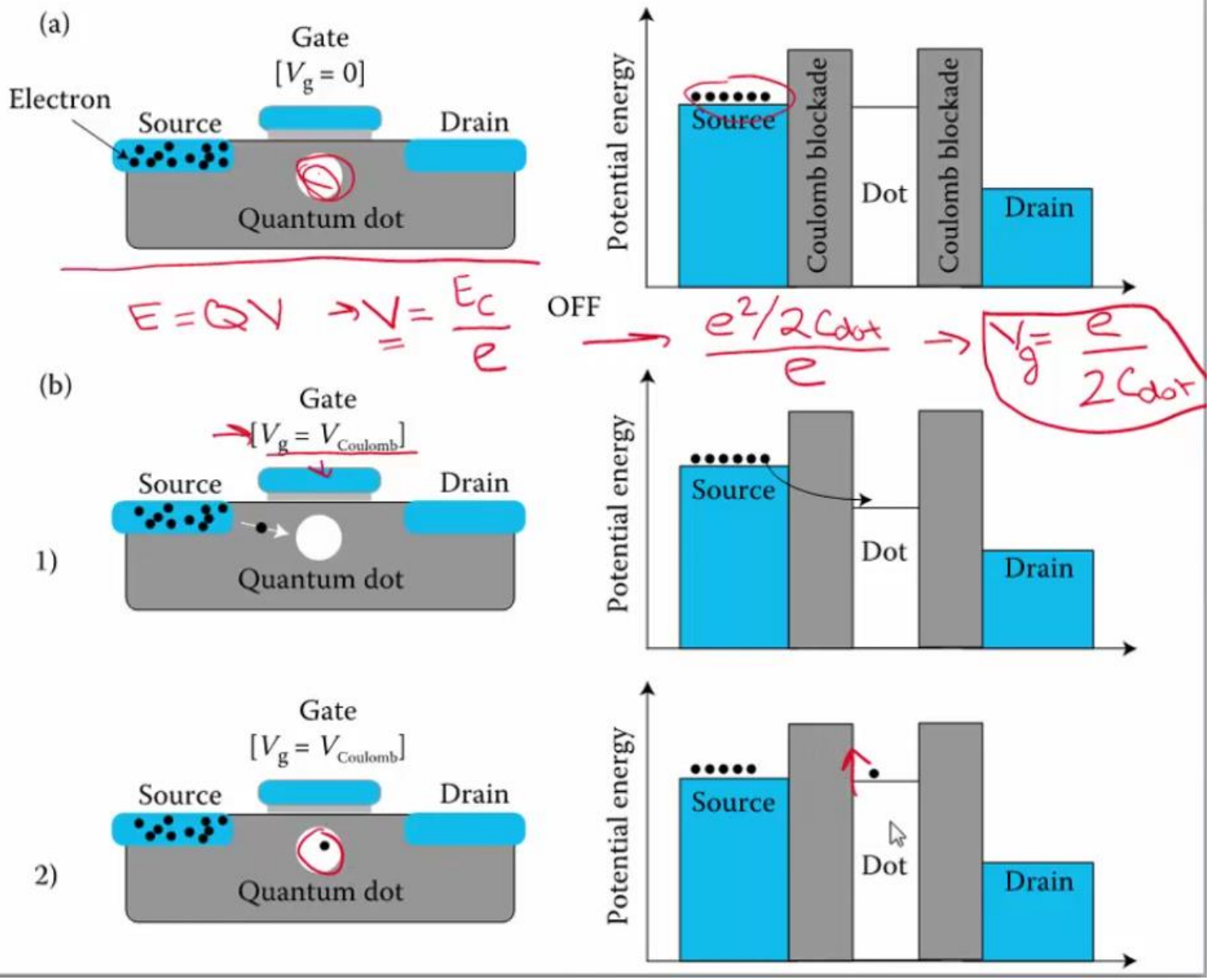
$$\Delta E = \frac{h}{\Delta t} \qquad \Delta t = Rt \cdot C_{oot}$$

In order to avoid random tunneling we are controlling the uncertainty in the energy it takes to add an electron to the well which must be less than or equal to the actual energy it takes to add an electron.

$$\frac{h}{Rt \cdot C_{oot}} \leq \frac{e^2}{2C_{oot}} \Rightarrow Rt \gg \frac{h}{e^2}$$

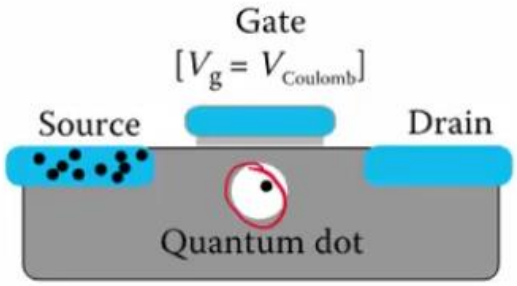
Means we need a very very high resistance in order to confine an electron.

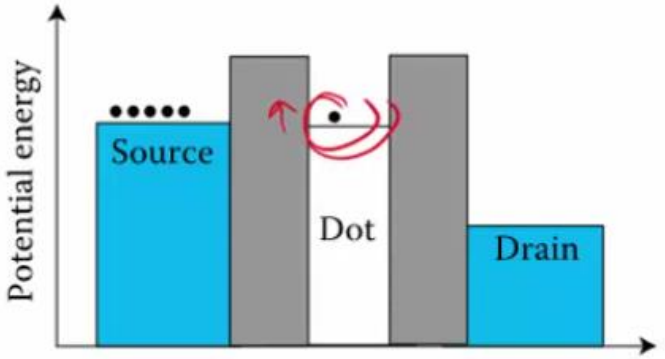
Single-Electron Transistor (SET)



Single-Electron Transistor (SET)

2)





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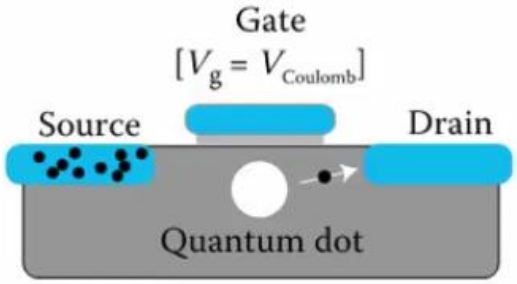
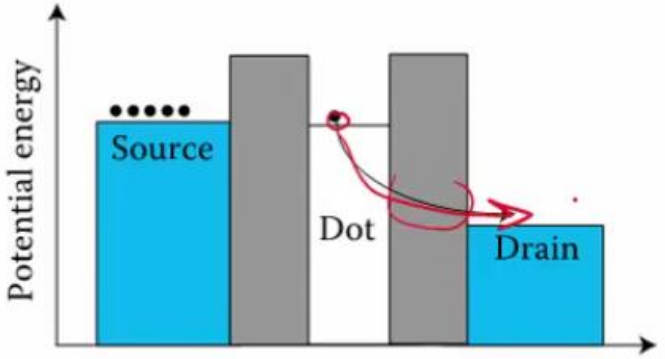
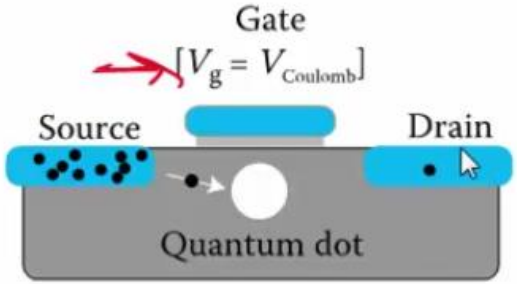
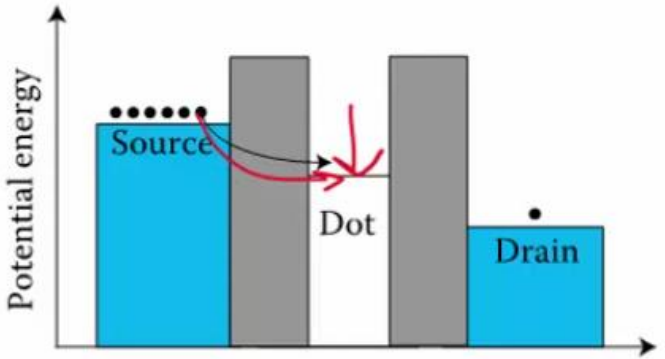




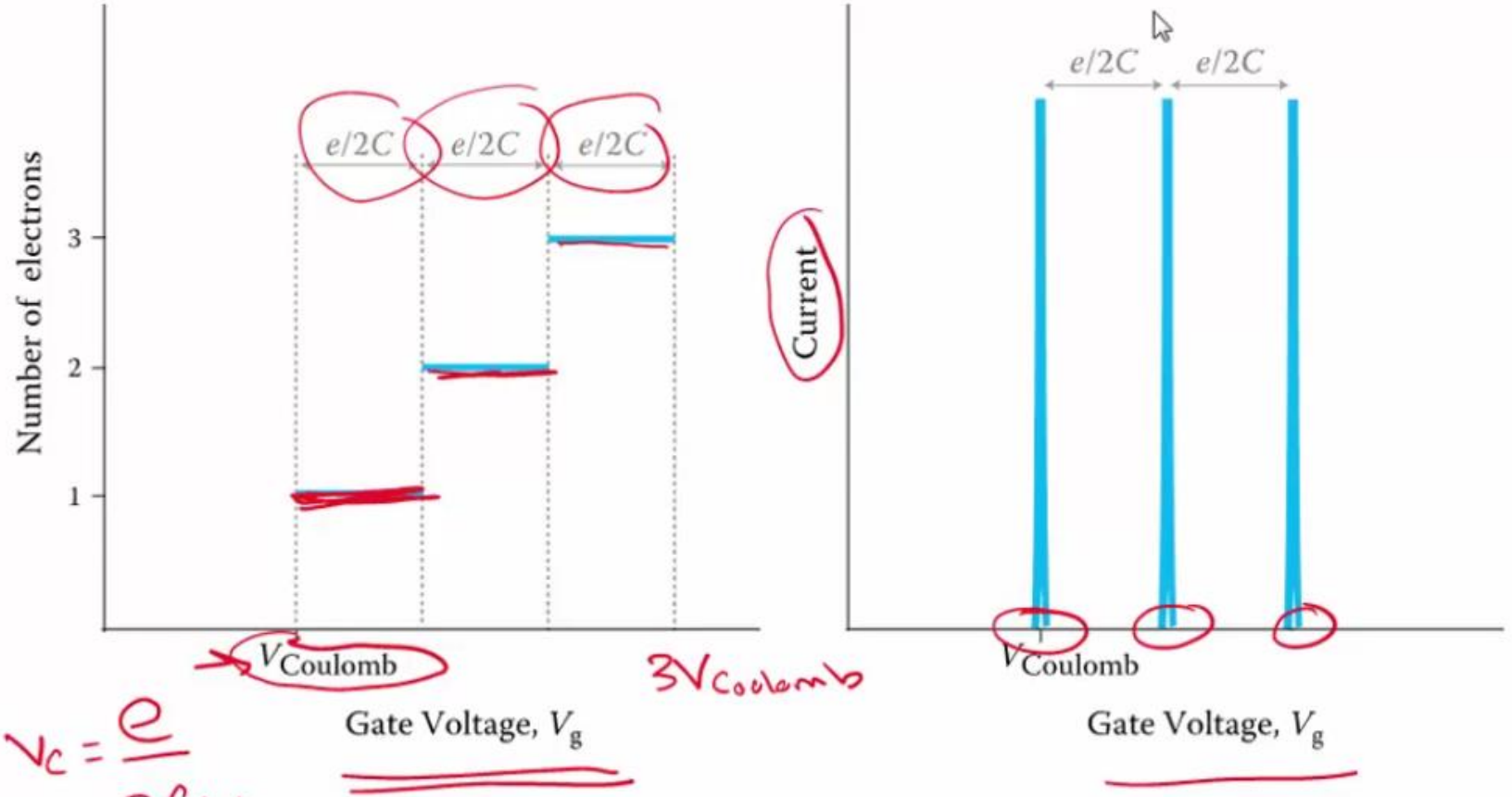
4)





ON

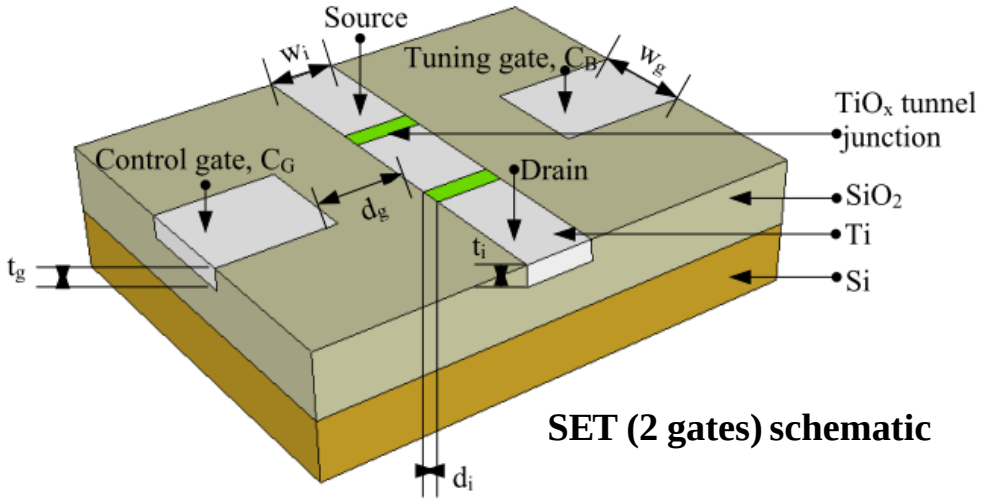
Single Electron Transistor



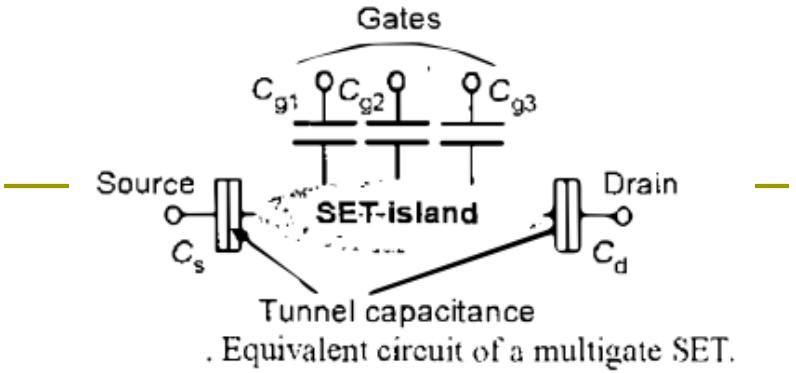
$3V_{Coulomb}$

$V_C = \frac{e}{2C_{dot}}$

SET background

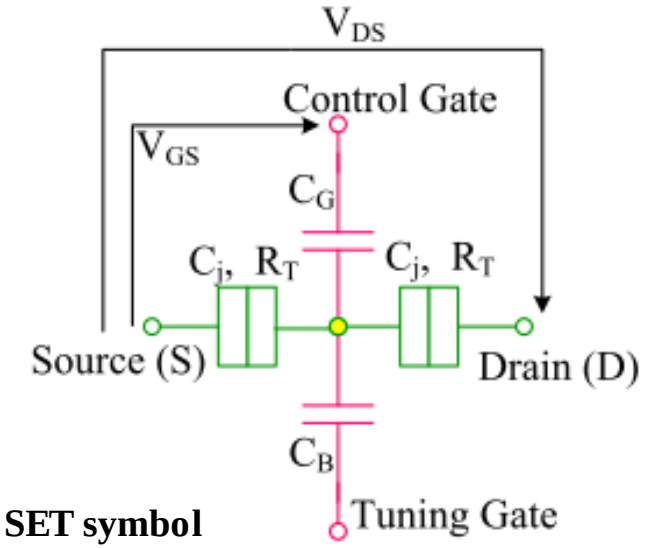


SET (2 gates) schematic



. Equivalent circuit of a multigate SET.

- SET fabricated at UdeS by Nanodamascene process. [1, 2]
- Device capacitances calculated by parallel plate method .



SET symbol

$$C_\Sigma = 2C_j + C_G + C_B$$

SET device feasible parameter range and capacitance calculation

Tunnel junction capacitance (Cj) range calculation			
w_i (nm)	**d_i (nm)**	**t_i (nm)**	**C_j (Farad)**
3 - 20	2 - 8	1 - 10	1.16e-20 - 3.10e-18
Gate capacitance range calculation			
w_g (nm)	**d_g (nm)**	**t_g (nm)**	**C_g / C_b (Farad)**
30	20 - 60	1 - 10	1.73e-20 - 5.18 e-19

1. Dubuc et al., Applied Physics Letters, ’07
2. Dubuc et al., IEEE Trans. on Nanotechnology, ‘08

Capacitance calculation

C_g, C_b and C_j are calculated using parallel plate model using the below equations.

$$C_g, C_b = \varepsilon_{r(SiO_2)}\, \varepsilon_0 \frac{w_g t_g}{d_g} \qquad (3.1)$$

As in figure 3.1, for a SET, w_g and t_g are the width and thickness of the gate and d_g is the separation between the island and gate.

ε_r is the relative static permittivity = 3.9 for SiO_2

ε_0 is the permittivity of free space where $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

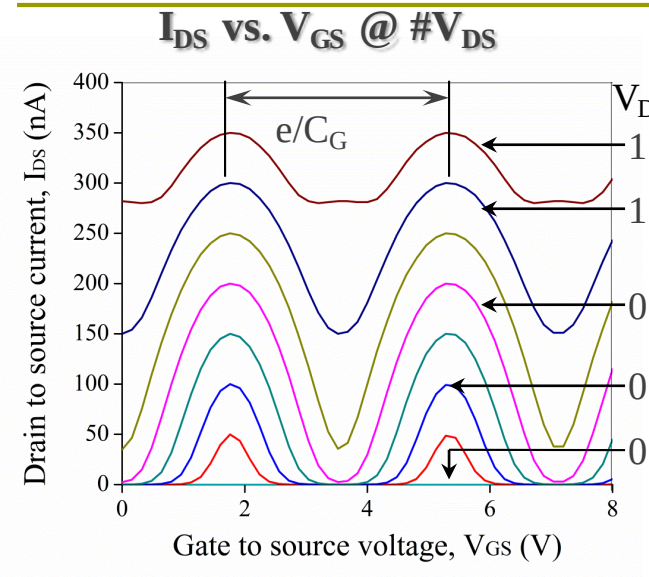
$$C_j = \varepsilon_{r(TiO_2)}\, \varepsilon_0 \frac{w_i t_i}{d_i} \qquad (3.2)$$

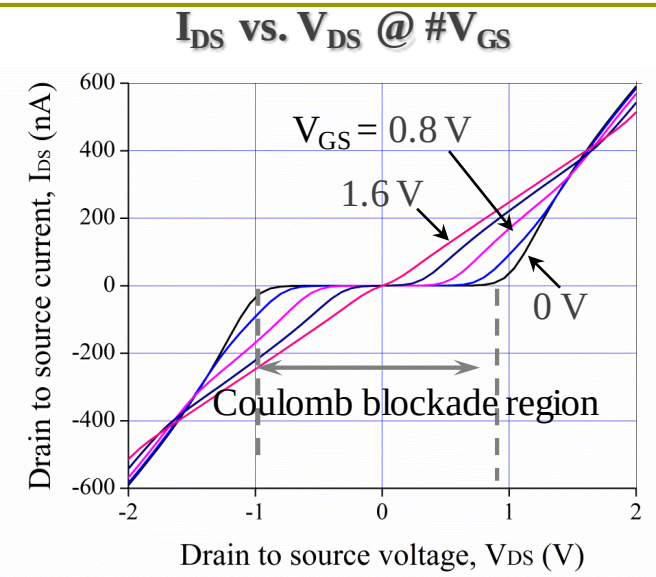
As in figure 3.1, for a SET w_i and t_i are the width and thickness of the tunnel junction and d_i is the separation between the island and the source or the drain.

ε_r is the relative static permittivity = 3.5 for TiO_2

ε_0 is the permittivity of free space where $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

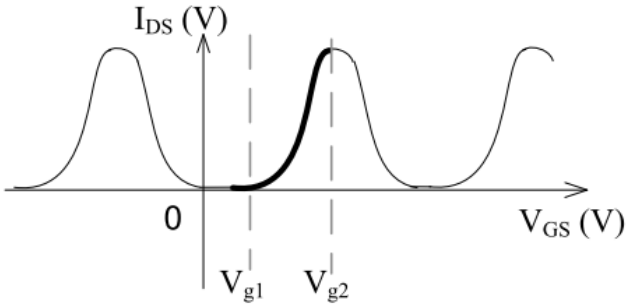
SET characteristics



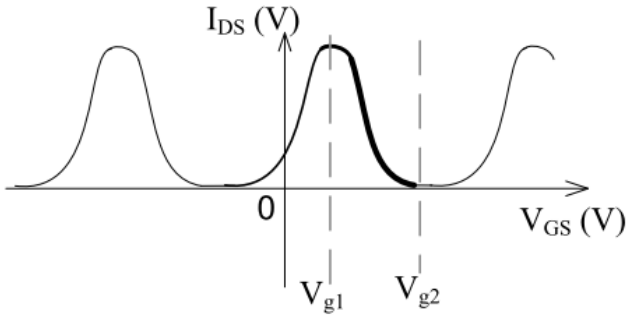


C_j = 0.03 aF,
C_G = 0.045 aF,
C_B = 0.05 aF,
R_T = 1MΩ,
T = 300 K

Biasing SET through tuning gate results in complementary behaviour compared with unbiased one, similar to P and N type MOSFETs.



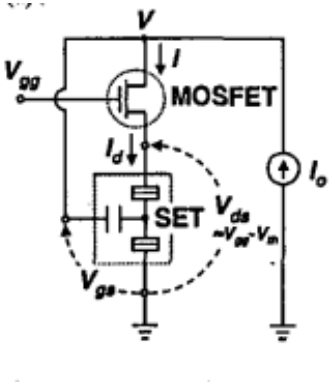
SET oscillations characteristics **(Unbiased tuning gate)**



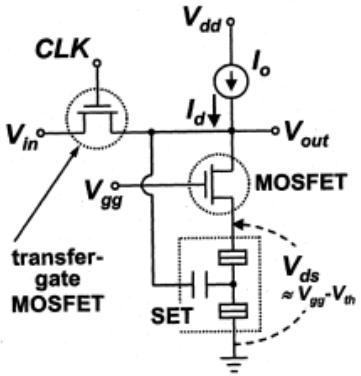
SET oscillations characteristics **(Biased tuning gate)**

SET-CMOS high performance circuit examples

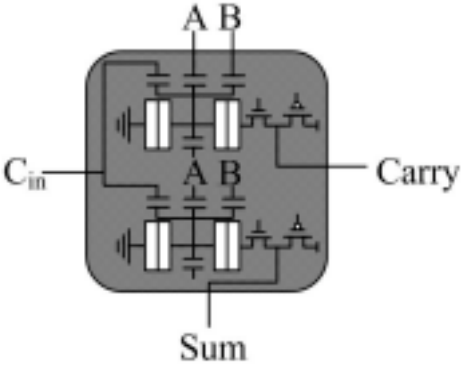
Multi peak NDR device / Multiple value logic / SRAM cell



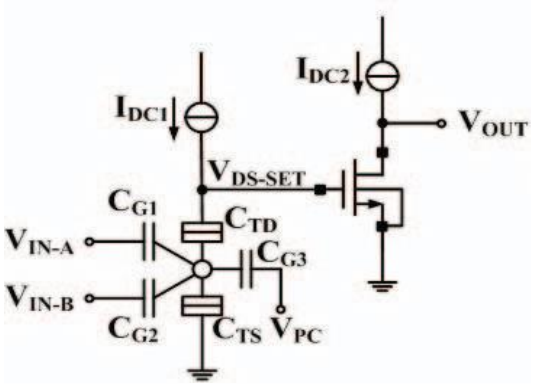
Quantizer



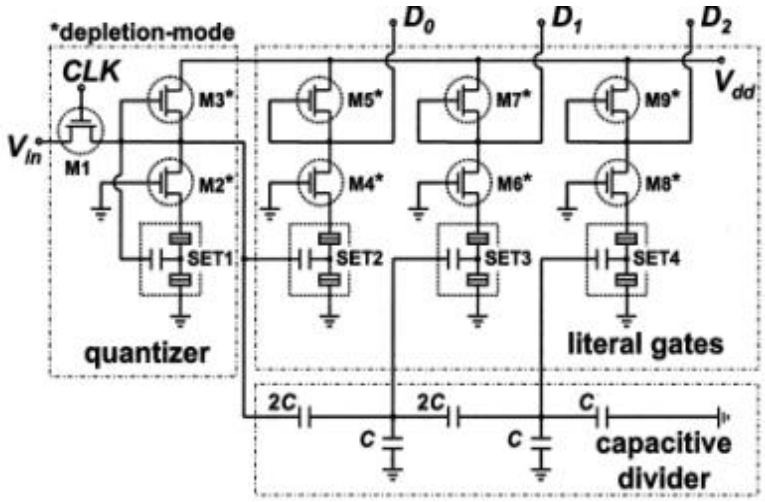
One-bit full adder



Parallel SETMOS with three-gate SET transistor as AND, NOR and XOR gate



3-bit ADC



Other significant applications

- SET as a photon detector
- SET as a mixer
- RF SET
- SETs in micromechanical applications
- SETs in microscopy (Charge sensitive tips)

SETs in different material systems

- Metal-metal oxide SETs
- Semiconductor dot SETs (GaAs, Si, InAs)
- Carbon nanotube SETs
- Nanotube and nanowire SETs (CNTs, InAs nanowires)
- SETs using MOSFET structures

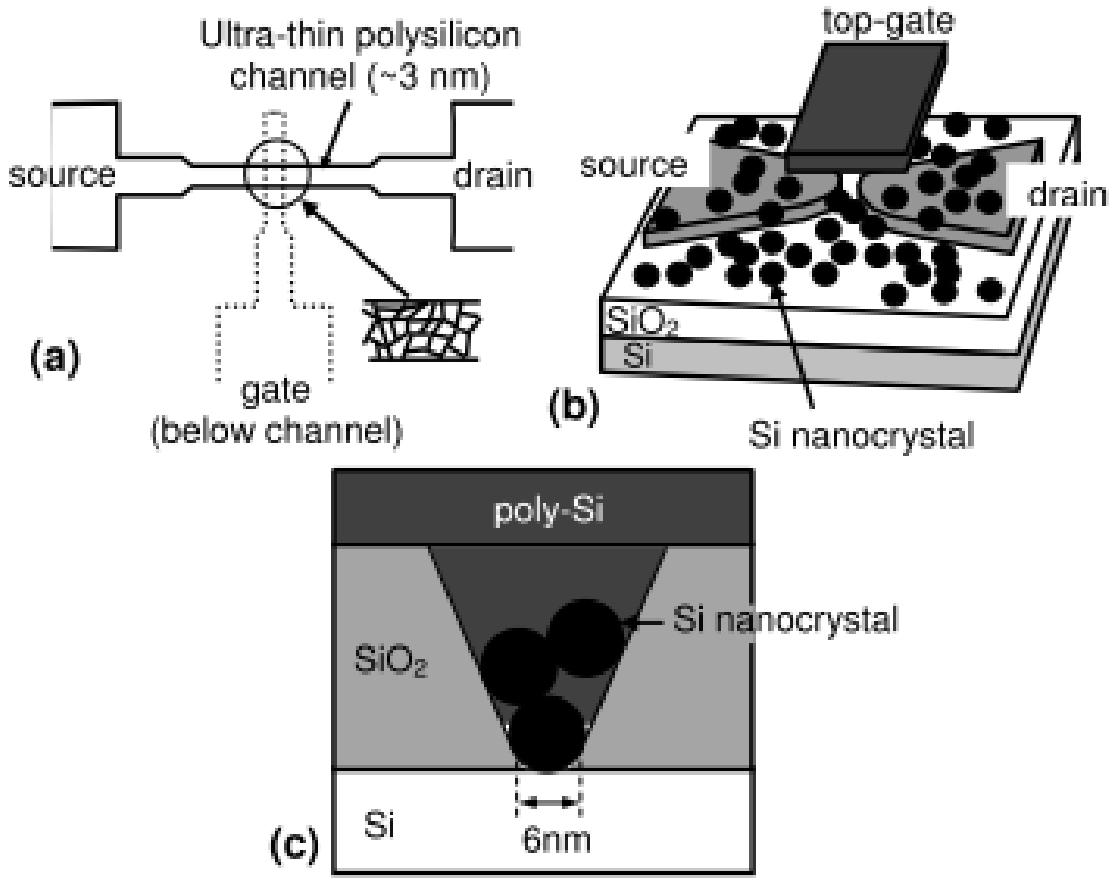


Fig. 3.24 SETs using discrete Si nanocrystals. (a) SET using an ultra-thin, granular nanocrystalline silicon film (Yano *et al.*, 1995). (b) SET with Si nanocrystals deposited in a nanoscale gap between source and drain contacts (Dutta *et al.*, 2000b). (c) Vertical transport device, with Si nanocrystals deposited in a hole etched in a SiO_2 film (Nishiguchi and Oda, 2000).

The nanodamascene fabrication process

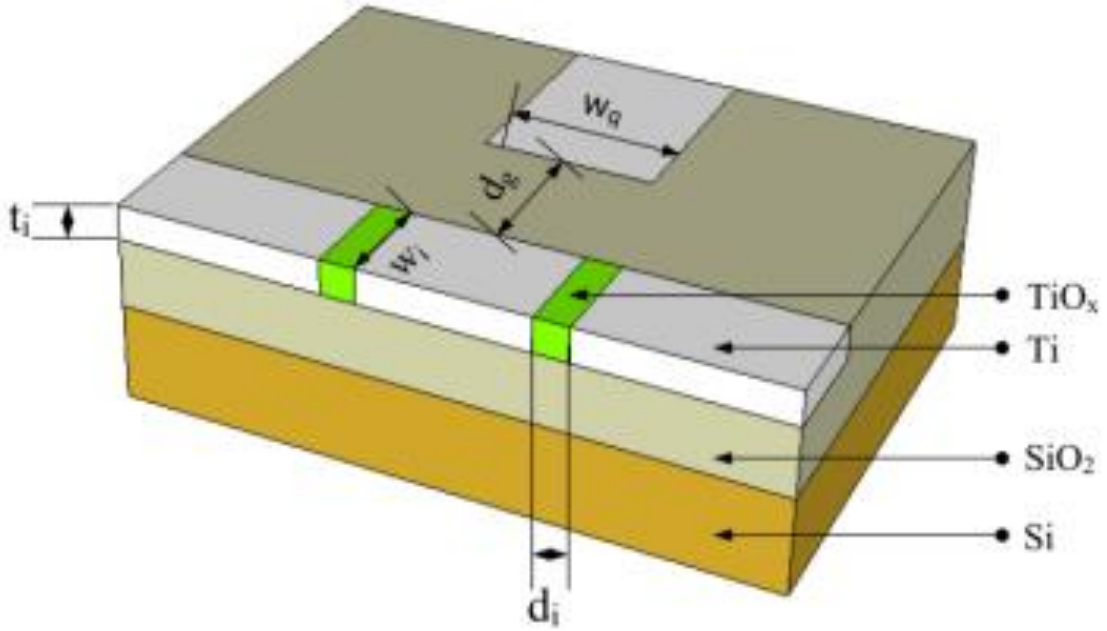


Figure 2.8 SET schematic.

1. Si wafer preparation :

The Si wafer is oxidized to obtain 100 nm thick SiO_2 layer on which the devices will be fabricated.

The nanodamascene fabrication process

2. Photolithography:

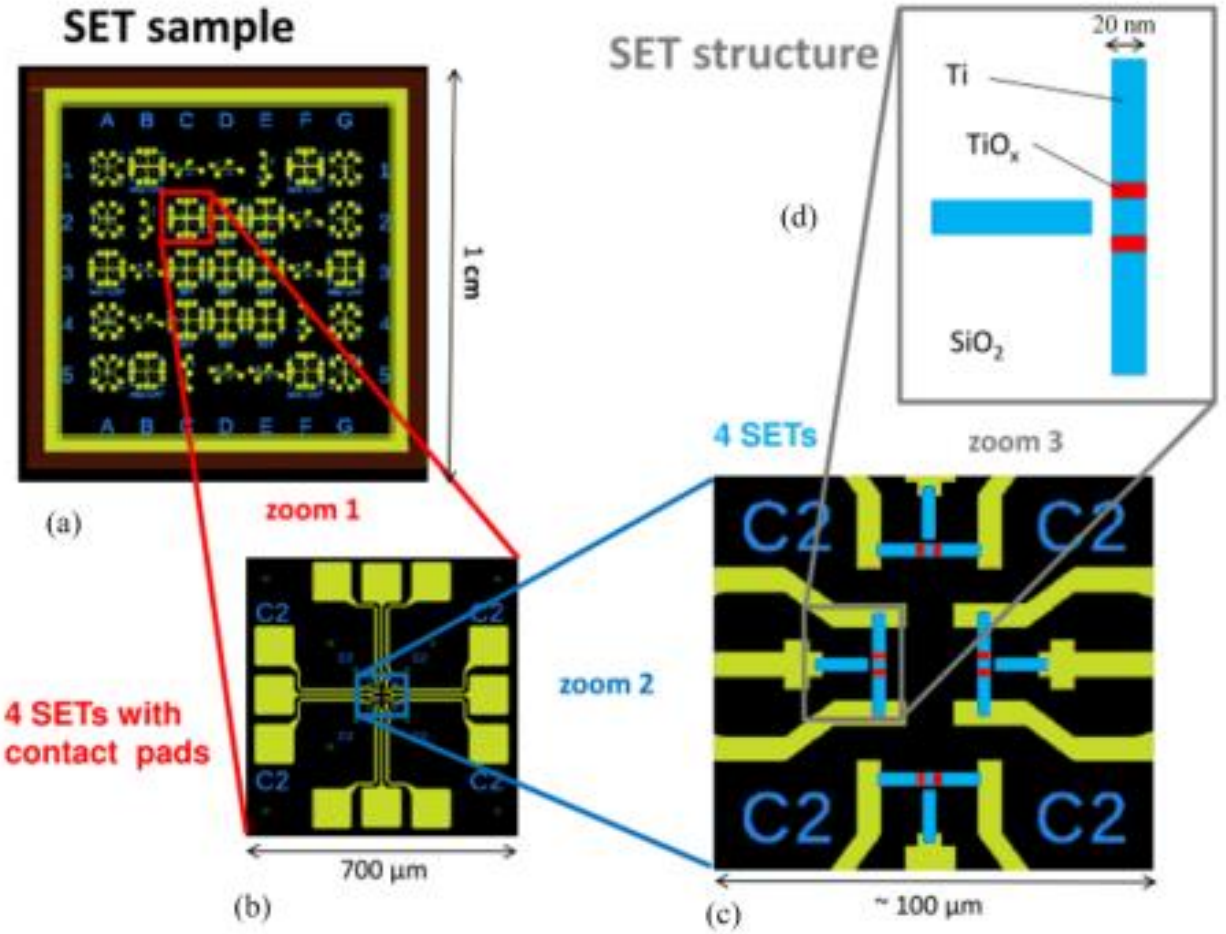


Figure 2.9 (a) Photo mask for 36 SETs with MIM and TLM structures (b), (c), (d) Zoomed images of (a) (SEDIMOS project documentation).

The nanodamascene fabrication process

3. The trench formation:

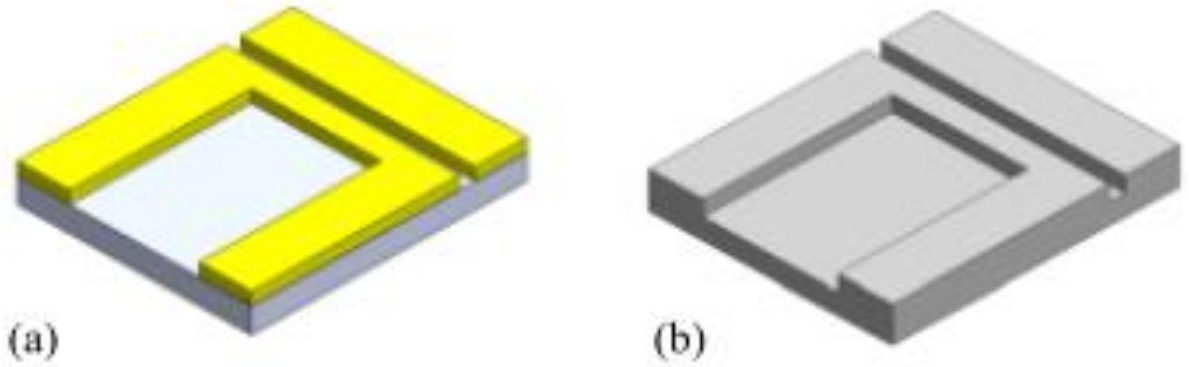


Figure 2.10 SET trench formation (SEDIMOS project documentation) (a) First EBL (b) SiO_2 dry etch

The nanodamascene fabrication process

4. Ti island and gate formation:

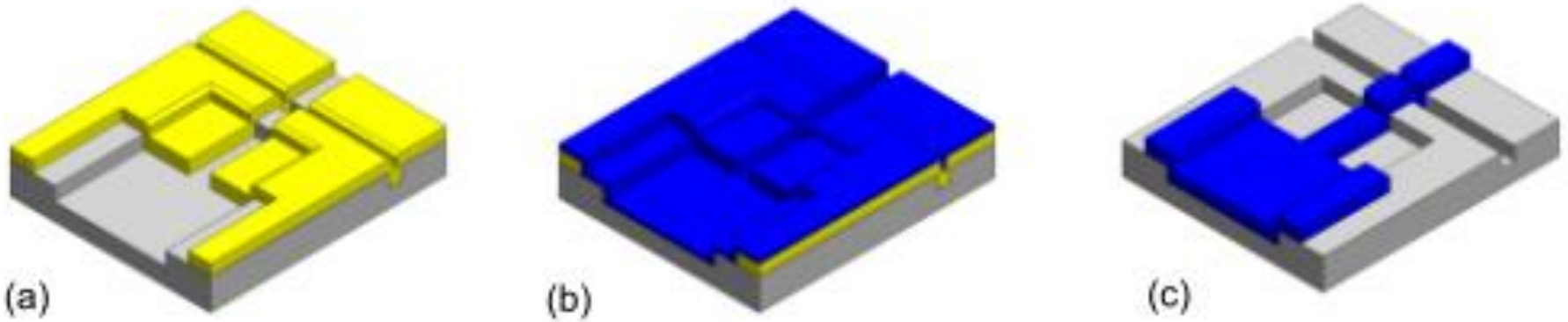


Figure 2.11 SET Ti island and gate formation (SEDIMOS project documentation) (a) Second EBL (b) Ti deposition (c) Lift –off

The nanodamascene fabrication process

5. The tunnel junction formation:

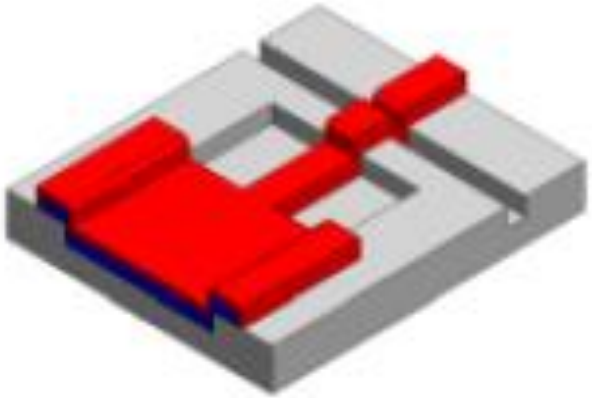


Figure 2.12 SET tunnel junction formation, oxidation (SEDIMOS project documentation).

6. The source and the drain formation:

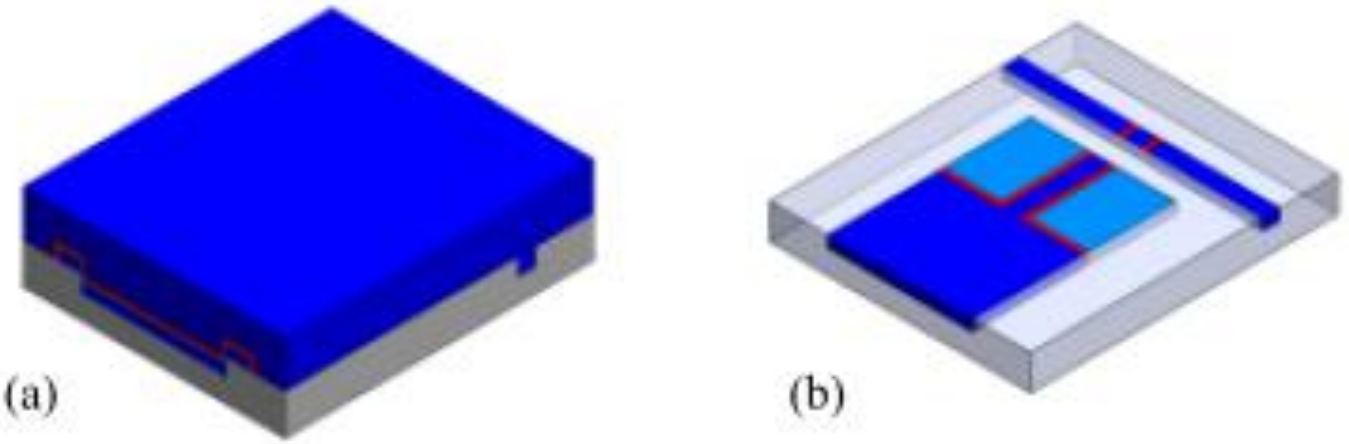


Figure 2.13 SET Source and Drain formation (SEDIMOS project documentation). (a) Ti deposition (b) CMP

SET-CMOS hybridization challenges

- Simulation methods developed, with one or several constraints in regard to design or simulation.
- Right design, accurate modelling and simulation of circuit, including parasitic is crucial.
- Previous work limited to either,
  - low output voltages,
  - low temperature,
  - SET parameters not as per actual functional device,
  - neglected interconnect load at the output,
  - do not address design associating several SETs to several MOSFETs.
  - Spice coding
  - Analysis do not address design methodology that can be applied to hybrid circuits with all electrical & physical parameters.

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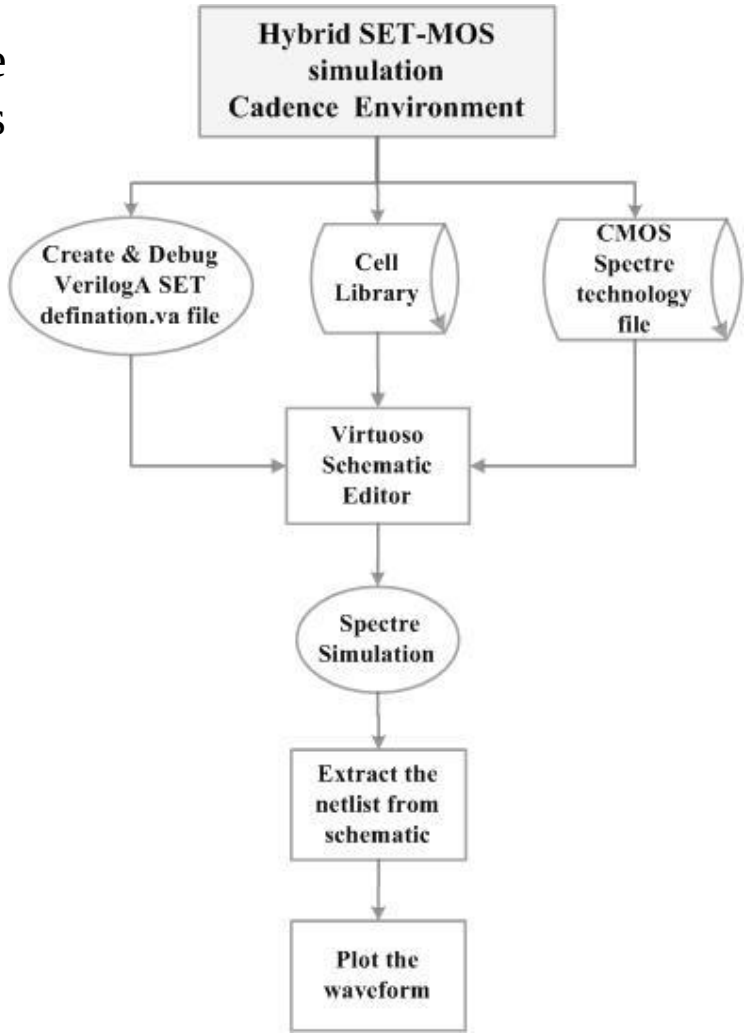
Hybrid SET-CMOS circuit co-simulation

- CAD developed in CADENCE [1] to simulate large-scale hybrid digital and analog circuits with active or passive device elements.
- Facilitates
  - Schematic editor
  - CMOS at future technology node
  - parametric analysis,
  - formatting of output data,
  - saves coding time,
  - Transparent & flexible circuit operation.
- BSIM4 22-nm planar bulk CMOS model [2]
- Mahapatra–Ionescu–Banerjee SET model [3]



Hybrid circuit simulation flow flowchart

1. Cadence Design Systems. www.cadence.com
2. W. Zhao et al., ACM J. Emerging Technol. Comput. Syst., ‘07
3. S. Mahapatra et al., IEEE Tran. Electron Devices ‘04

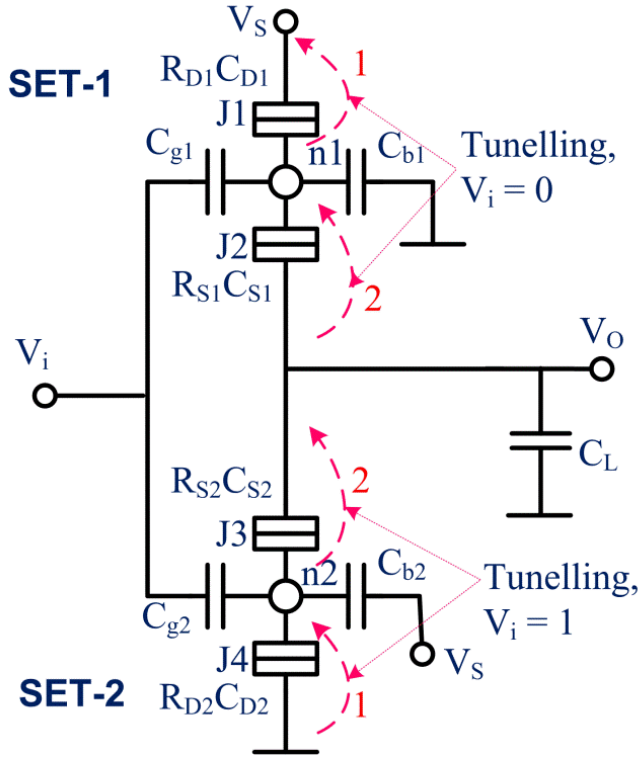
SET logic (Inverter) design, analysis and simulation

Circuit requirements

- Unipolar voltage response (usually SET circuits are operated with bipolar response),
- Fixed Supply and Biasing voltages as per 22-nm planar bulk CMOS (800 mV),
- Drive load C_L equivalent of CMOS inverter plus interconnect, $R_t = 1\ M\Omega$,
- Obtain SET parameters within fabrication range at room temperature (300 K).

Design parameter considerations

- Operating temperature $T \propto e^2/(2k_B C_\Sigma)$, consider $e^2/C_\Sigma = 40\ k_B T$ for design,
- Voltage level $\propto e/C_\Sigma$,
- Device maximum operating frequency $\propto 1/(R_t\ C_\Sigma)$, but when $C_L > C_\Sigma$, C_L affects the frequency,
- SET inverting voltage gain is $A_V = C_g/C_j$; but is also a function of temperature.

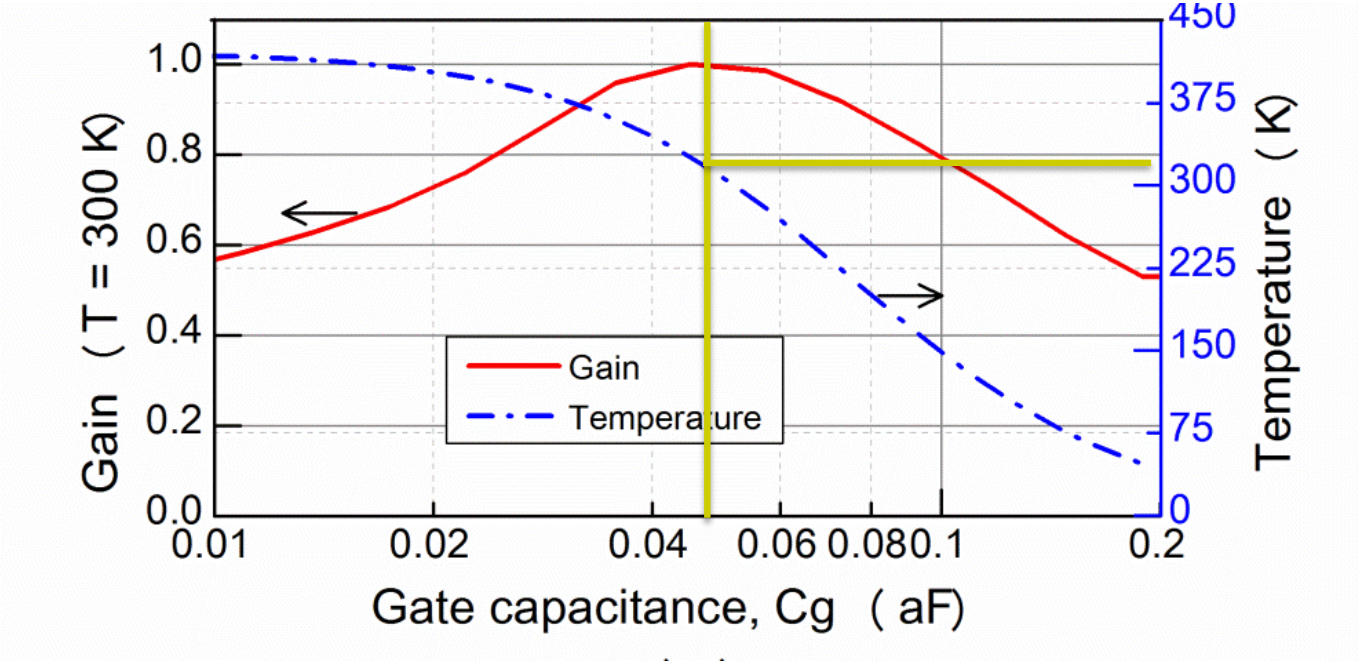


$C_{S1} = C_{D1} = C_{S2} = C_{D2} = C_j$ $\quad C_{g1} = C_{g2} = C_g$

$R_{S1} = R_{D1} = R_{S2} = R_{D2} = R_t$ $\quad C_{b1} = C_{b2} = C_b$

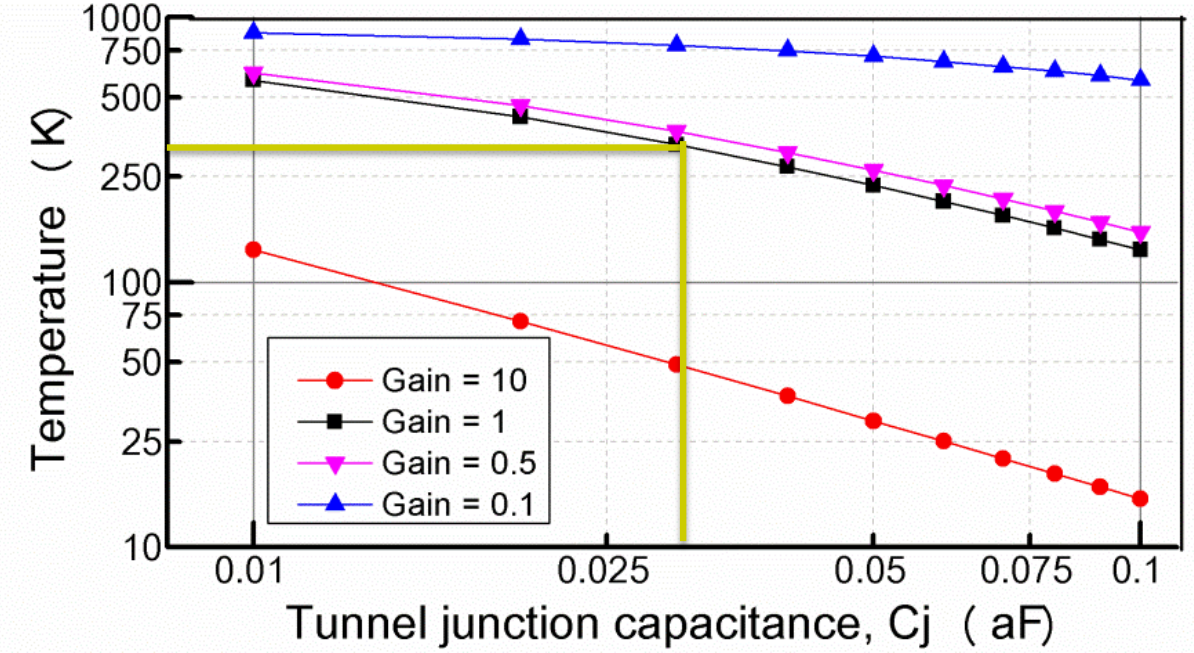
SET inverter circuit.

SET Inverter design trade-offs



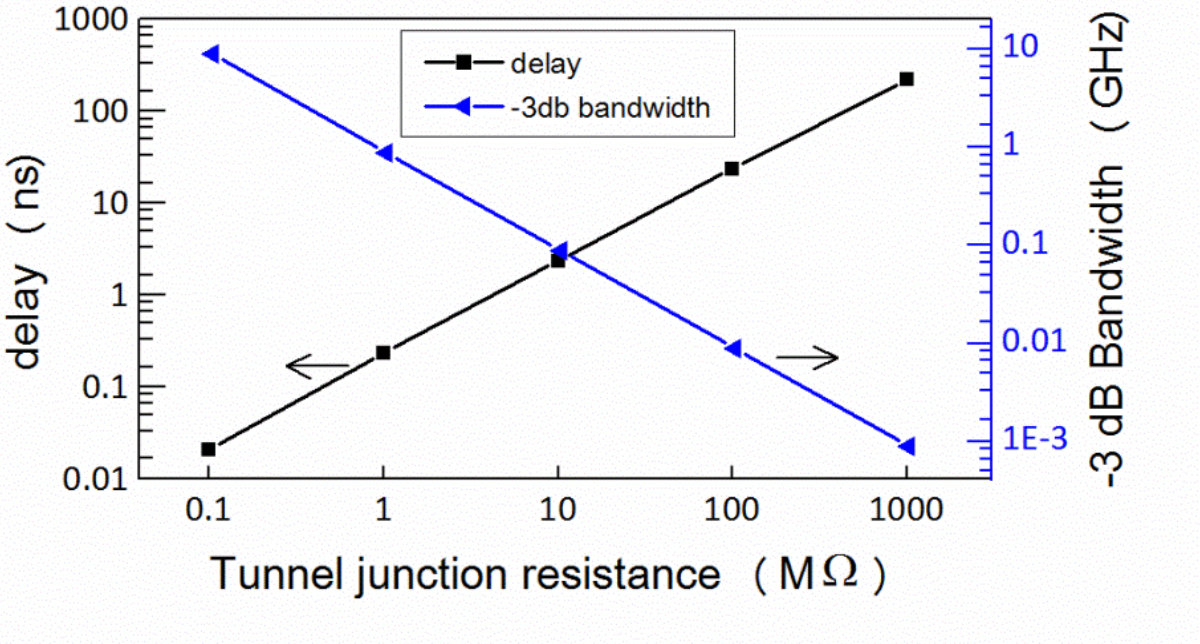
SET inverting voltage gain (T = 300 K) & maximum operating temperature as a function of gate capacitance C_g, C_j = 0.03 aF, C_b = 0.05 aF.

SET Inverter design trade-offs



SET inverter maximum operating temperature as a function of junction capacitance C_j , C_b = 0.05 aF.

SET Inverter design trade-offs



SET inverter delay & -3 dB Bandwidth as a function of tunnel resistance R_t, C_j = 0.03 aF, C_g = 0.45 aF, C_b = 0.05 aF, gain = 1.

SET-Inverter : Design Methodology

Methodology

- Analyze either SET-1 or SET-2 part of circuit .
- For each junction derive **critical voltages** (V_{C3} & V_{C4}) and **tunnel junction voltages (**V_{J3} & V_{J4}) using Thevenin's & Superposition theorem respectively.
- Derive inequalities by relating above equations for different circuit conditions.
- Optimise parameters based on electrical constraints & within the fabrication range.

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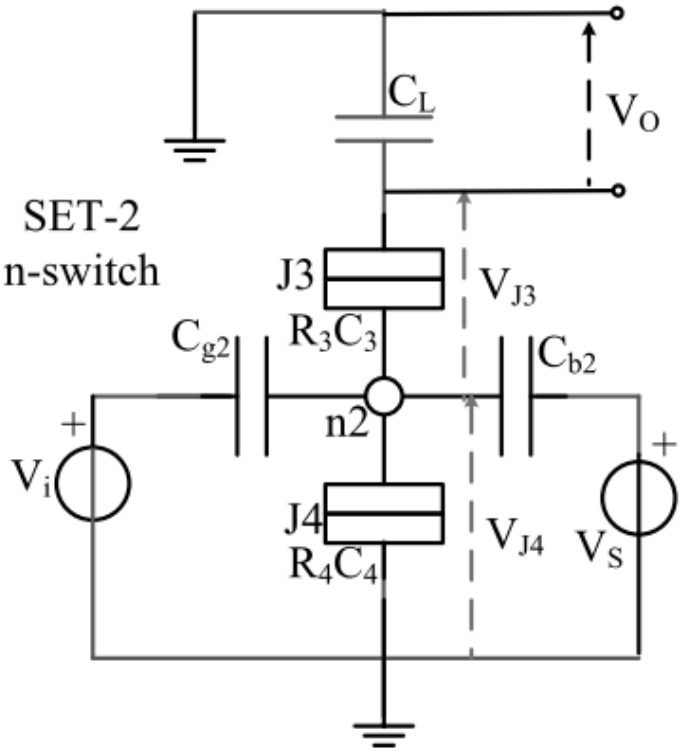


The n-switch, circuit diagram to calculate the tunnel junction voltage

SET-Inverter: Analytical derivation

SET-2 characteristic equations

Critical voltages

$$V_{C3} = \frac{e\left(C_L + C_{b2} + C_{g2} + C_{D2}\right)}{2\,C_\Sigma\,(C_{S2} + C_L)}$$

$$V_{C4} = \frac{e}{2\,C_\Sigma}$$

$$C_\Sigma = \frac{C_{S2}C_L + (C_{S2} + C_L)\left(C_{D2} + C_{g2} + C_{b2}\right)}{(C_{S2} + C_L)}$$

Tunnel junction voltages

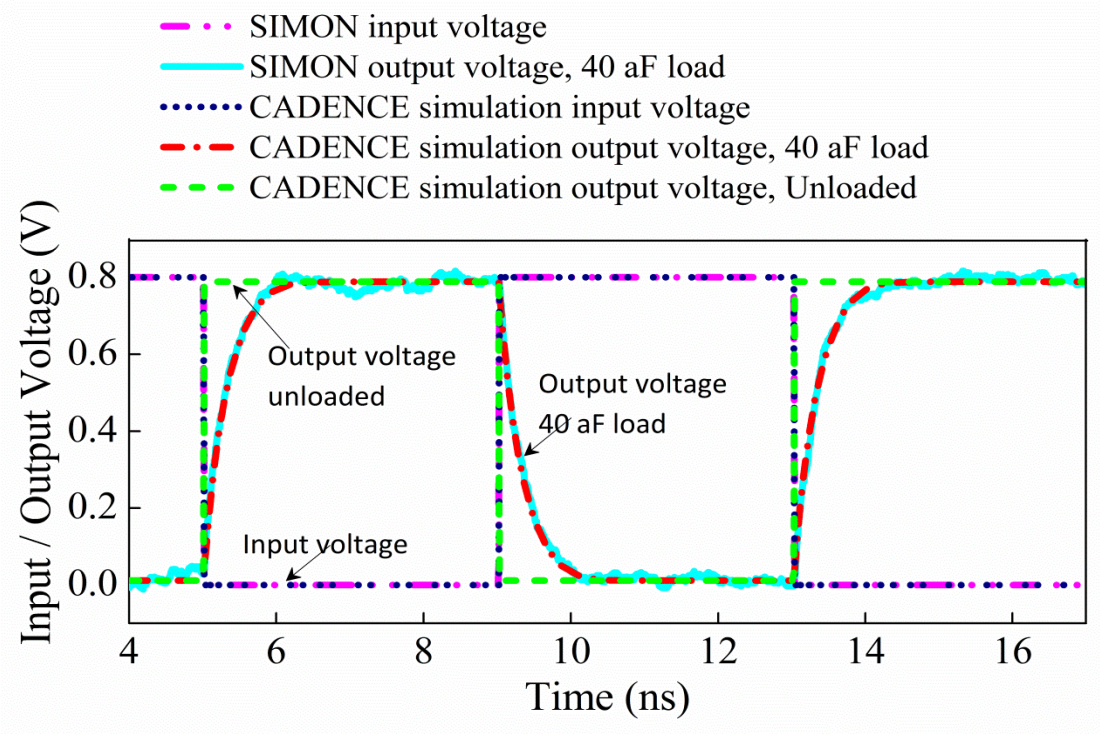
$$V_{J3} = \frac{1}{C_\Sigma}\left[V_O\frac{(C_{g2} + C_{b2} + C_{D2})C_L}{C_{g2} + C_{b2} + C_{D2} + C_L} - V_i\frac{C_L C_{g2}}{C_{g2} + C_L} - V_S\frac{C_{b2}C_L}{C_{b2}+C_L} - q_2\right]$$

$$V_{J4} = \frac{1}{C_\Sigma}\left[V_O\frac{C_{S2}C_L}{C_{S2} + C_L} + C_{g2}V_i + C_{b2}V_S + q_2\right]$$

Similar derivations can be carried out for SET-1

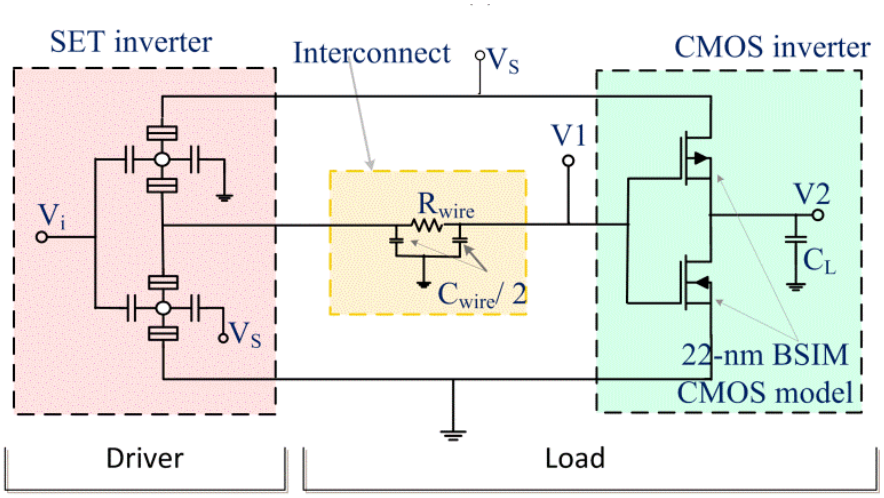
SET inverter : Analysis and parameter derivation

- The optimised parameters are,
  C_j = 3e-20, C_b = 5e-20, C_g = 4.5e-20
- The SET inverter parameters are simulated in CADENCE & verified in SIMON

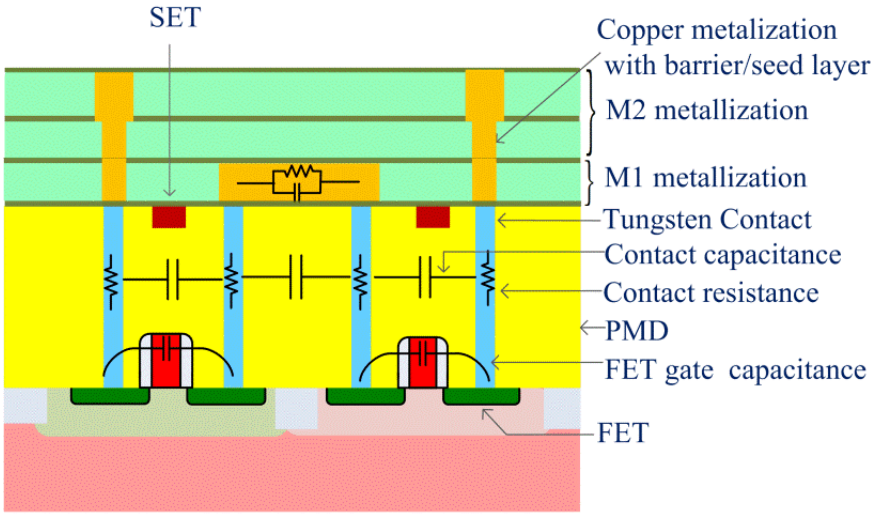


SET inverter transient analysis

Integrated SET-CMOS circuit architecture, design and simulation



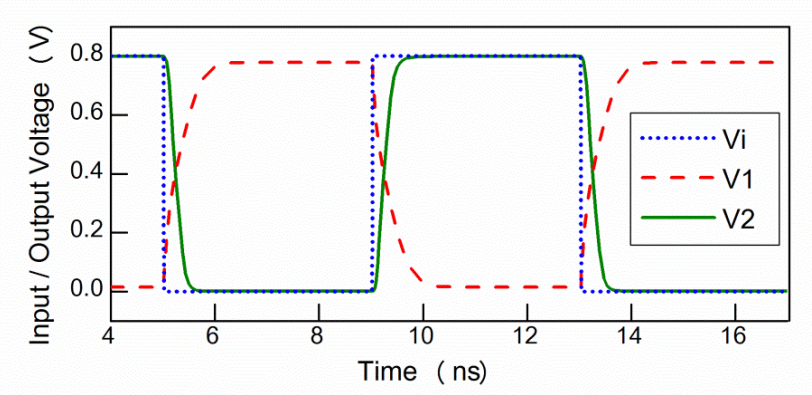
Circuit diagram. Hybrid SET-CMOS cascaded inverter with inter connect parasitics.



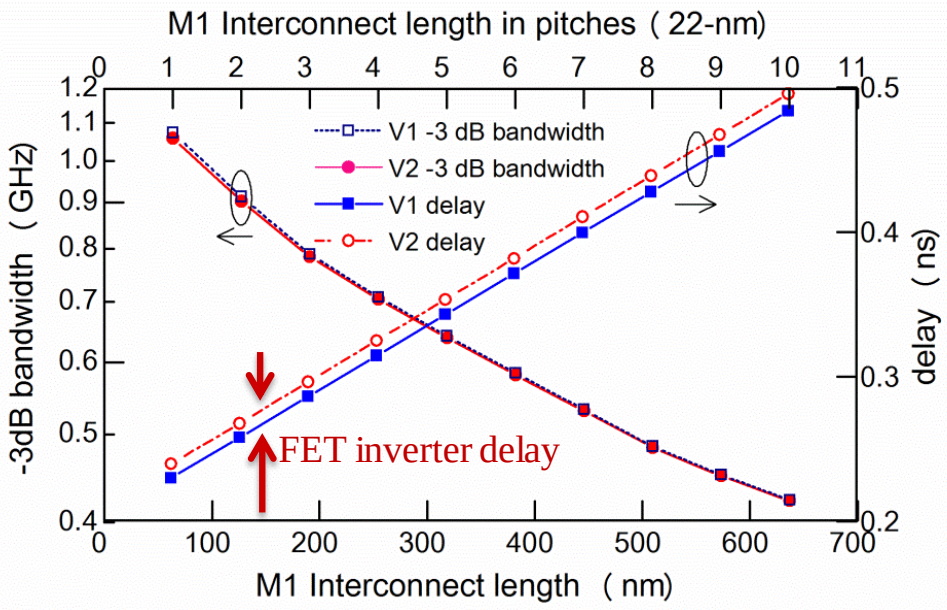
Model

C_{wire} & **R_{wire}** represents interconnect parasitic & simulated by its π model equivalent to study interconnect effects on bandwidth and delay.

Hybrid SET-CMOS cascaded inverter: Simulation results



Transient Analysis

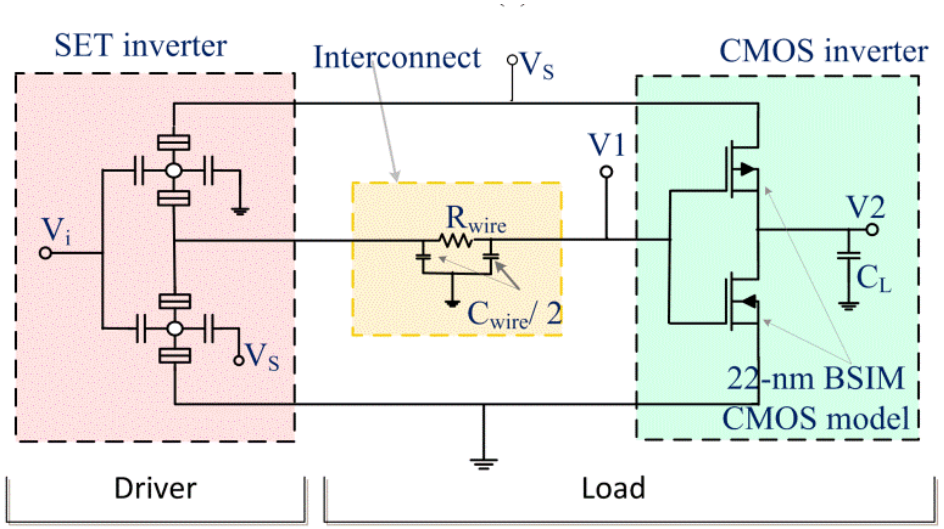


Effect of interconnect length on delay & bandwidth

Summary

- SET inverter can drive FET inverter plus interconnect with a stable output voltage of 800 mV and GHz frequency operation.
- Delay & load at SET inverter output are directly proportional.
- Hybrid circuit response improves with CMOS at higher technology node.

Hybrid SET-CMOS cascaded inverter: Power



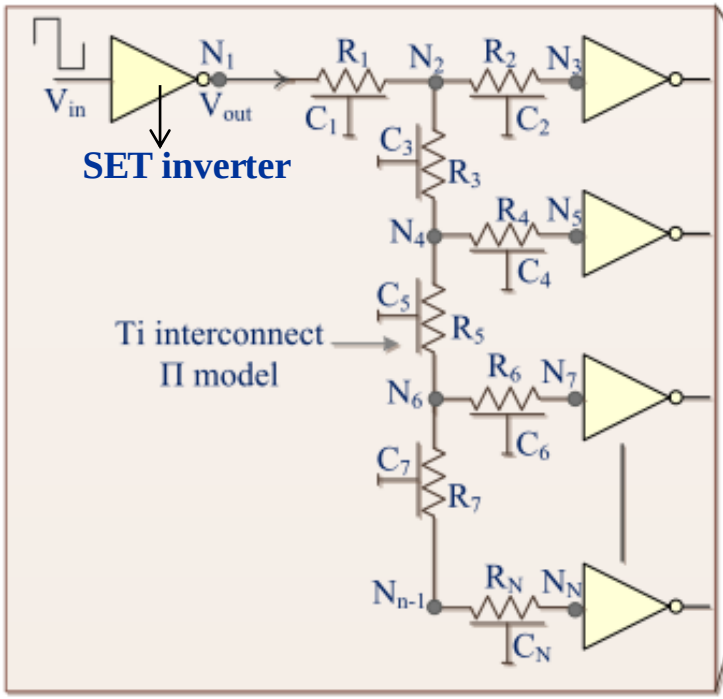
Circuit diagram. Hybrid SET-CMOS cascaded inverter with interconnect parasitics.

Power consumption by SET and CMOS inverter in Hybrid circuit

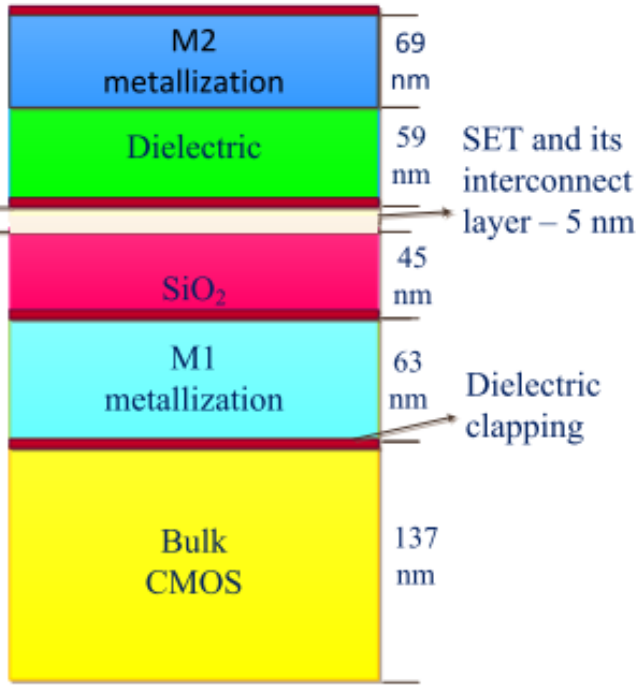
Power	SET inverter	CMOS inverter	Hybrid circuit
Static power	3.2 nW	23.1 nW	26.3 nW
Total power	4.6 nW	115.4 nW	120 nW
Dynamic power	1.4 nW	92.3 nW	93.7 nW

SET logic (Inverter) drivability

- In all the ICs, driving capability is limited by load.
- Because of SETs small dimension, influence of external device & interconnect strongly affects circuit behaviour.



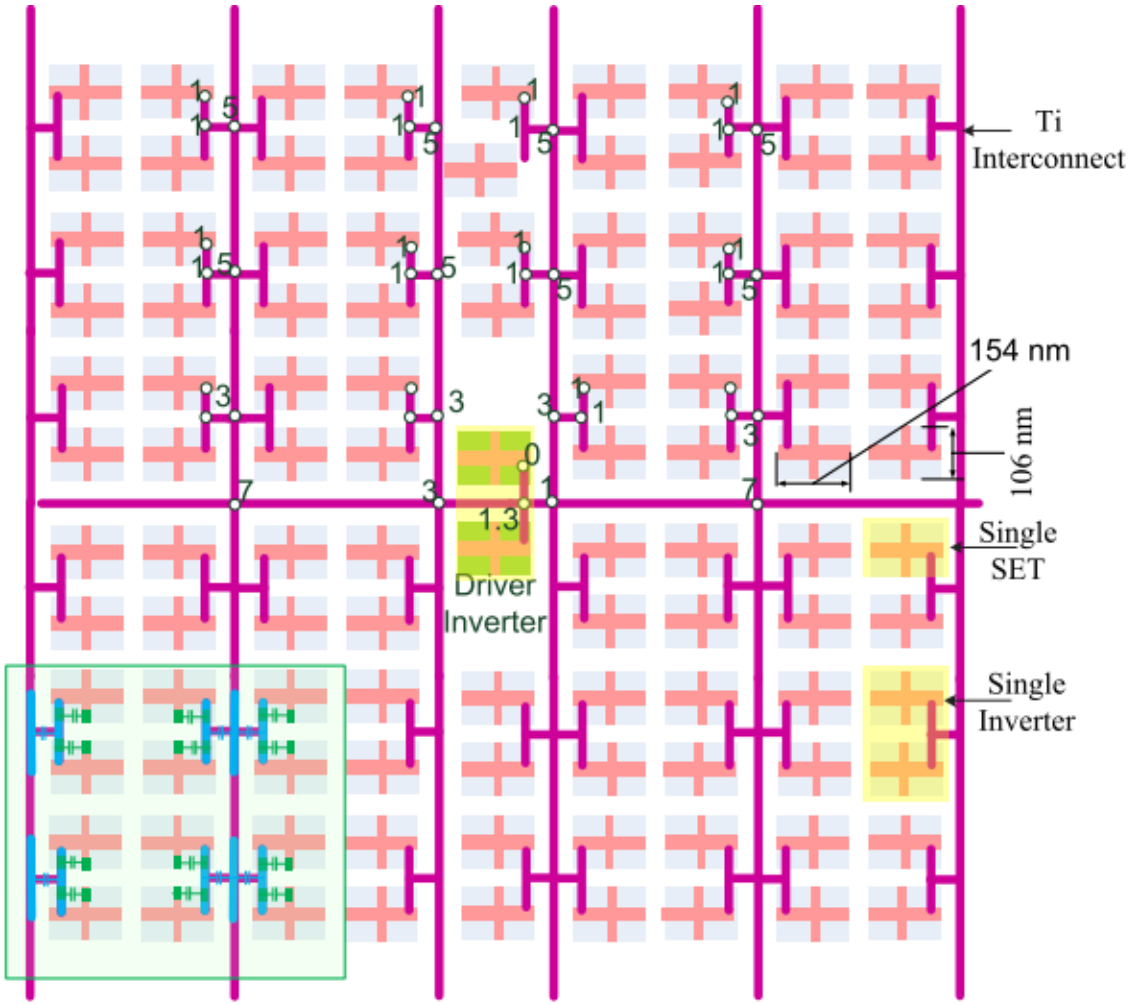
SET inverter fanout circuit with parasitic



Model for SET layer on CMOS carrier (22-nm node)

Layout – Study SET Inverter driving capability

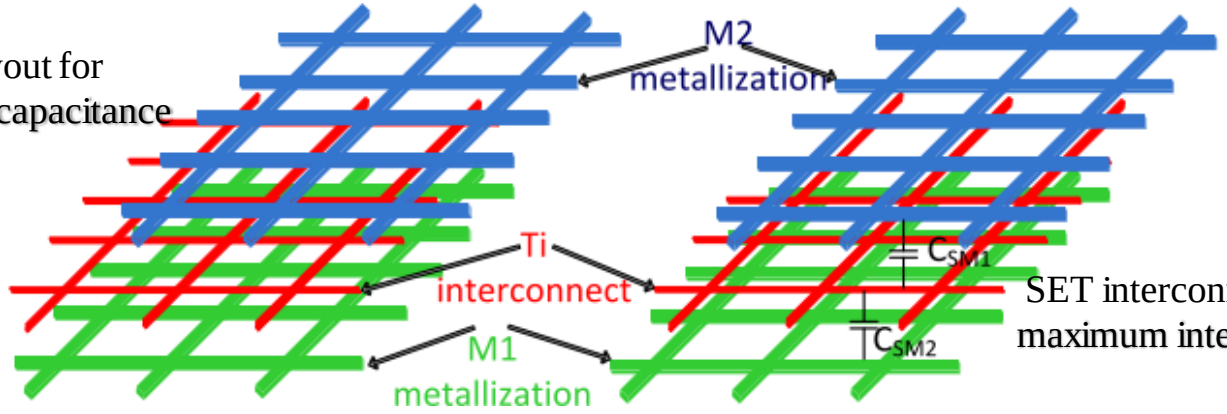
- SET dimension based on derived values.
- Parasitic capacitance and resistance calculated from this diagram.
- The crosstalk capacitance (same layer) marked blue is between Ti interconnects & green is between Ti interconnect and the source of SET which is also Ti.



Layout to study SET inverter driving capability consisting of SET inverters with Ti interconnect

Interconnect parasitic calculation from layout

SET interconnect layout for minimum interlayer capacitance



SET interconnect layout for maximum interlayer capacitance

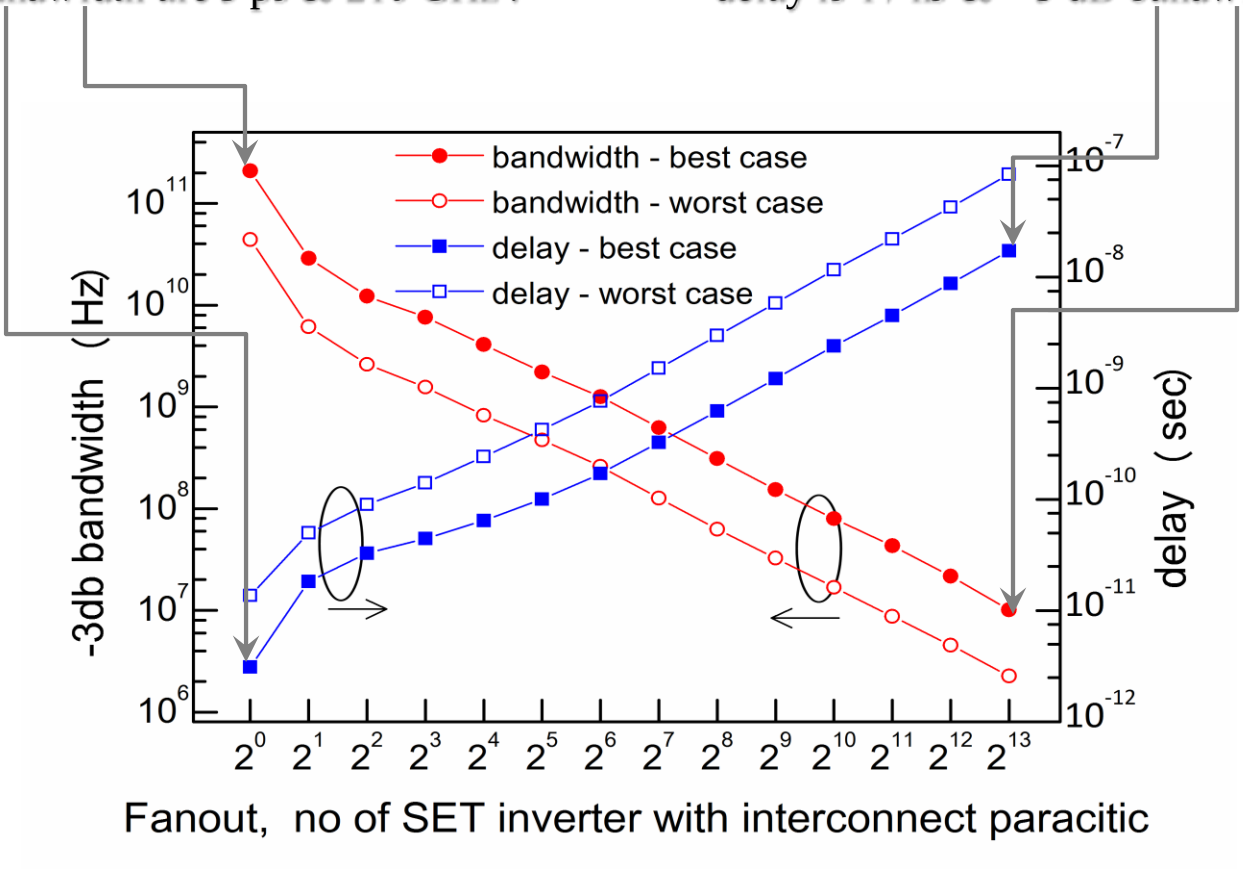
Resistance and Interlayer & lateral crosstalk capacitance calculation for Ti interconnect

SET layer interconnect capacitance & resistance calculation per unit length of Ti interconnect				
	w (nm)	**l (nm)**	**d (nm)**	**C_{int} (aF)**
M2 layer	15	63	59	0.28
M1 layer	15	63	45	0.37
	t (nm)	**l (nm)**	**d (nm)**	**C_{ct} (aF)**
Crosstalk	5	63	63	0.17
	l (nm)	**t (nm)**	**w (nm)**	**R (Ω)**
Ti wire resistance	63	5	15	353

SET inverter driving capability: Simulation results

with single inverter as load, best case delay & bandwidth are 3 ps & 210 GHz .

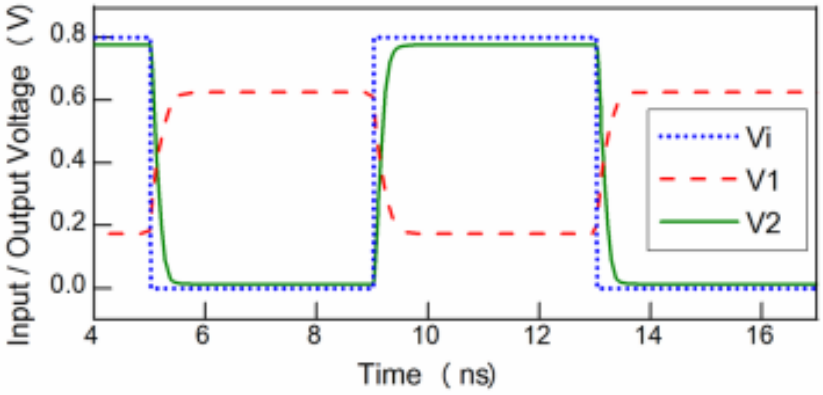
parallel load of 8192 (2^{13}) inverters best case delay is 17 ns & – 3 dB bandwidth is 10 MHz



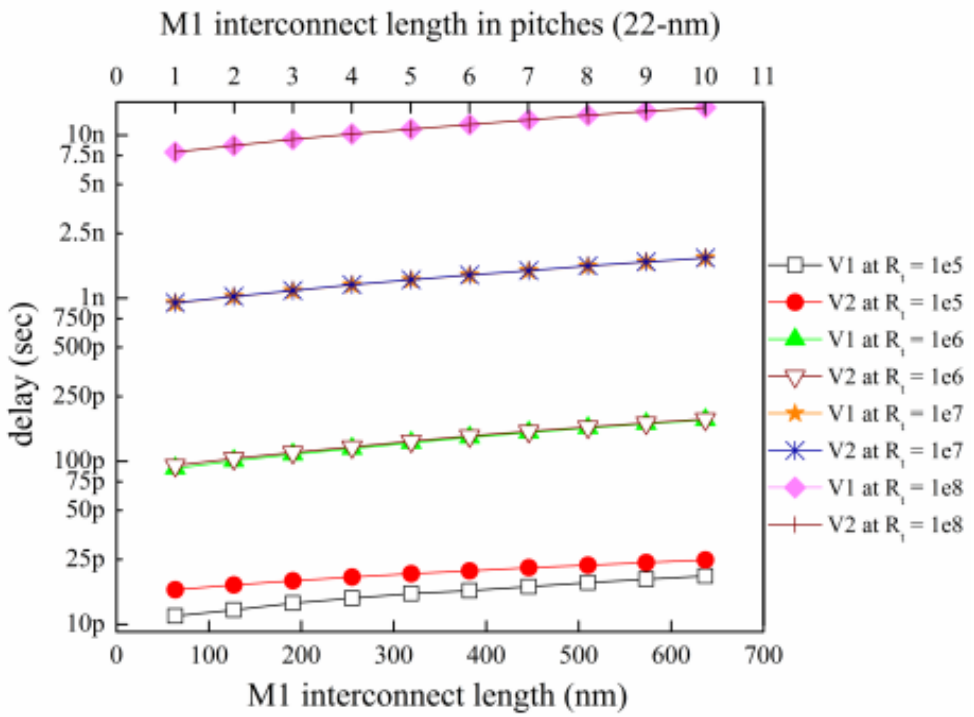
SET fanout simulation, effect of varying load on delay & bandwidth

Enhance SET Inverter driving capability by SET parameter variation

- Increase tunnel junction capacitance C_j (3e-20 to 7e-20), hence reduce the SET inverter gain
- Decrease Rt
- Simulation parameters same as derived except for C_j = 7e-20

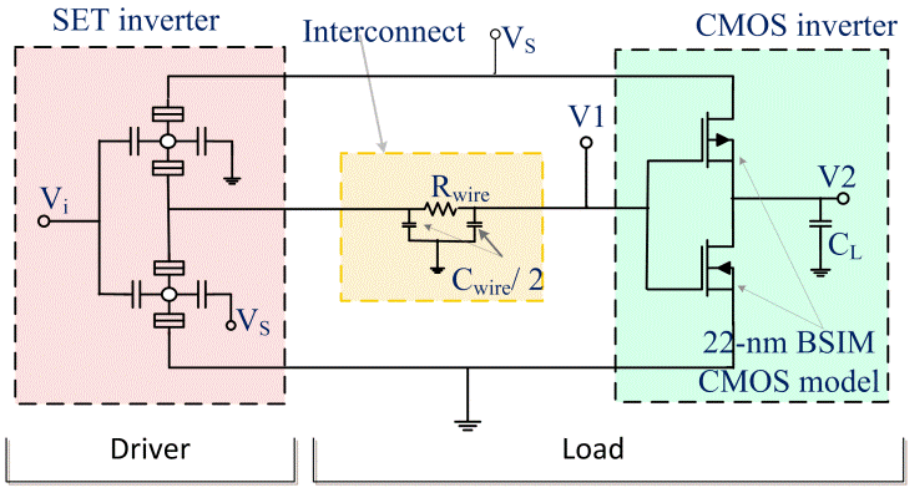


Transient analysis



Delay vs interconnect length.

Enhance SET Inverter driving capability by SET parameter variation

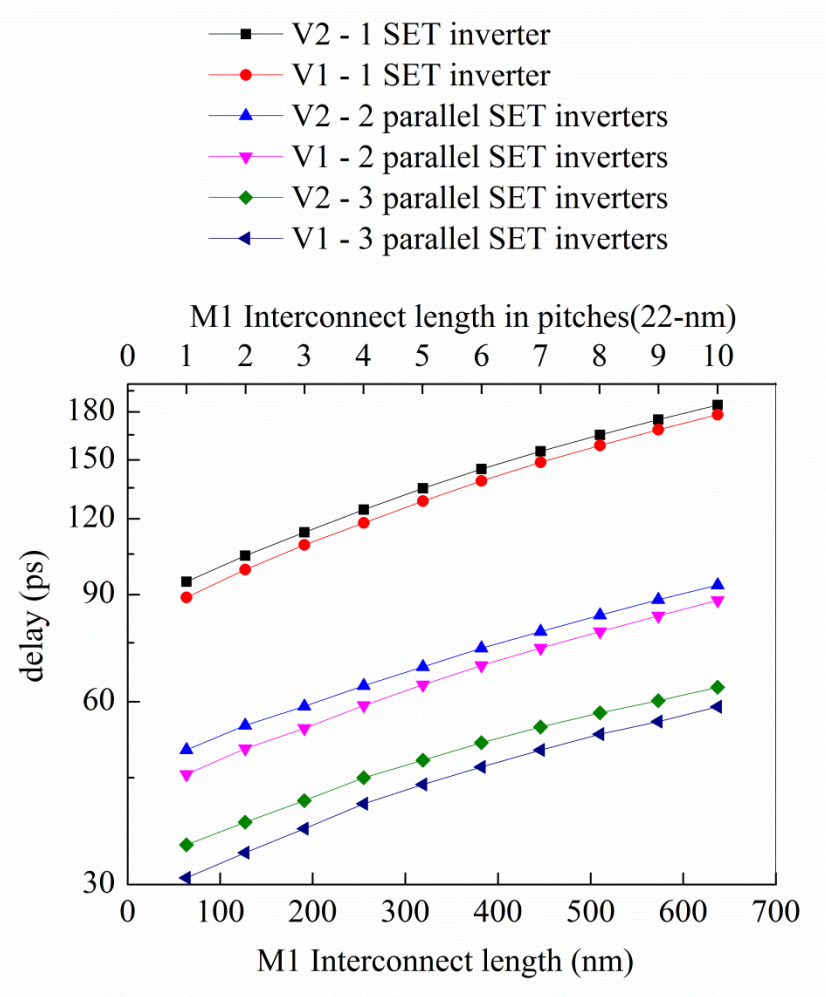


Circuit diagram. Hybrid SET-CMOS cascaded inverter with inter connect parasitics.

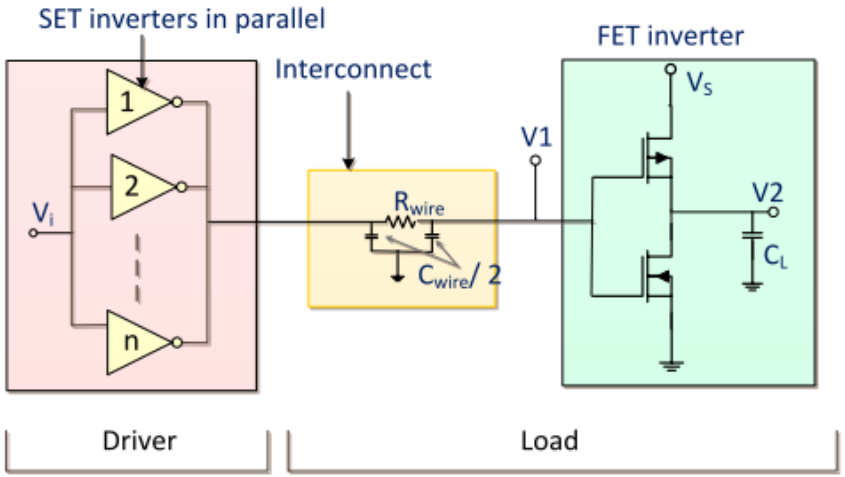
Delay measurement to show improvement in SET logic performance

Hybrid circuit delay measurement				
	gain = 0.5625, C_j = 7e-20 F		**gain = 1, C_j = 3e-20 F**	
Interconnect length	**SET Inverter (V1 terminal) (ps)**	**Hybrid Inverter (V2 terminal) (ps)**	**SET inverter (V1 terminal) (ps)**	**Hybrid inverter (V2 terminal) (ps)**
Minimum (1 pitch)	87	94	231	240
Maximum (10 pitch)	173	181	484	492

Enhance SET logic driving capability: SET logic in parallel



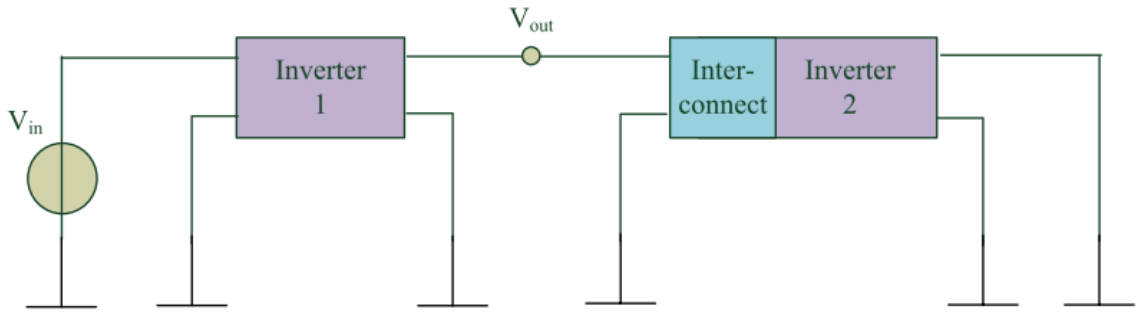
Delay analyses to improve SET logic efficiency



Summary

- Graph shows that the SET inverter delay can be greatly improved (87 ps to 30 ps), just by connecting up to 3 inverters in parallel.
- Overall SET inverter delay decreased from 231ps to 30 ps.
- Delay improved further by more number of parallel logics.

Comparison between SET and CMOS logic



Simulation setup to compare SET inverter and a CMOS inverter

Comparison between SET and CMOS logic

	CMOS cascaded inverter	**SET cascaded inverter**
Total power	130 nW	4 nW
-3 dB bandwidth	81 GHz	210 GHz
delay	8 ps	3 ps

Conclusion

- SET logic outperforms CMOS in terms of delay, bandwidth, and power but must be integrated with CMOS to interface with external world.
- Results advocate circuits made of SETs while resorting to as little CMOS as possible, which has the advantage of minimizing interconnect complexity.