Single Electron Transistor (SET)

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DATE

PAGE

* SET-CMOS hybridization

SET logic	CMOS logic
✓ Scaling potential	✓ High gain and current drive
✓ Ultra low power dissipation	✓ High speed
✓ New functionalities	✓ Very stable and matured fabrication technology.
✓ Room-temp operation	
✗ Reproducibility at Nanoscale	✗ Power density
✗ Low-Current drive (~nA)	✗ Sub 10nm physical limits & process variation at nanoscal.
✗ Background charge effect	

- SET circuit stack on CMOS platform
  - ↳ Functional and heterogeneous 3-D platform
  - ↳ Low cost, low thermal budget, improving yeild of IC's.

- In hybrid SET-CMOS
  - ↳ SET for local interconnect
  - ↳ SET-CMOS for global ".

↳ CMOS — handles I/O operation, signal restoration, and ensure compatibility.

↳ Addresses interface issues for many SET logic capability in driving voltage response, and power at room-temp.

(Img from pg-6, 7)

* Basics of Single electron Tunneling

↳ SET: Electrons tunnel individually through thin insulating barriers.
↳ Involves islands seperated by tunnel junctions.
↳ Coulumb blockade: Inhibits ΔE add / remove until voltage threshold is reached.
↳ operates at very low Temp due to temp sensitivity.

- Capacitor stores energy → $E_c = C \times V^2/2$
- To charge a capacitor by 1C requires potential diff. → $V = e/C$
- The charging energy → $E_c = \frac{CV^2}{2} = C\frac{\left(\frac{e}{C}\right)^2}{2} = \frac{e^2}{2C}$
- To observe SET effects condition → $E_c >> kT$
- To pass current capacitor must be 'leaky' not too leaky (tunnel jn)
  - → discharge time — $\Delta t = RC$
  - → from Heisenberg uncertainity principle — $\Delta E \cdot \Delta t = \frac{e^2}{2C} RC > \frac{h}{2}$

$$R_j > \frac{h}{e^2} \qquad C < \left(\frac{kT}{e}\right)\frac{1}{e}$$

R_j very very high to combine electron

(Img on pg 11, 12)

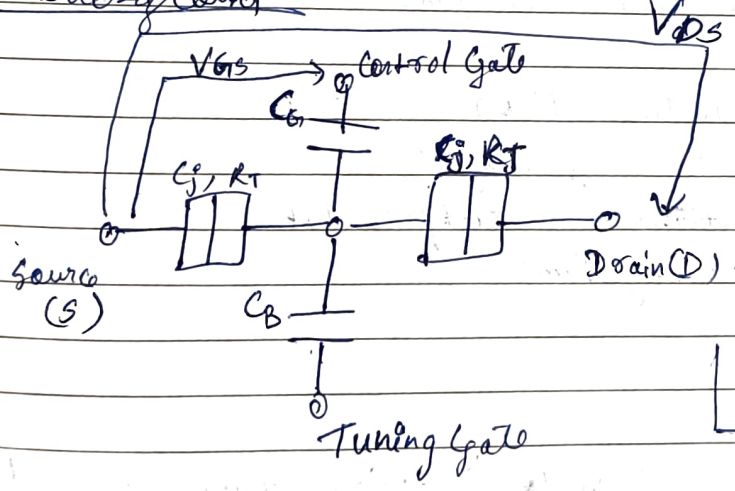
↳ In Image, when electron travels from source to quantum dot. Then the gate voltage

$$V_g = \frac{e}{2C_{dot}}$$

↳ Quantum dots → exhibit quantized charge state
→ Coulomb blockade effect
→ precise control of individual electrons.

(Img - pg - 13)

* SET background



$$C_\Sigma = 2C_j + C_G + C_B$$

* SET characteristics

↳ I_{DS} Vs V_{DS} – sharp increase in current when electron passes to dot.

↳ I_{DS} Vs V_{DS} – Current increasing, gets stable when there is coulomb blockade

(Img - pg 16) (pg-17 just see)

(Img - pg 18, 19)

(Img pg 21-26)

* SET-CMOS hybrid challenges

- previous work limited to either,
  - ↳ low output voltages
  - ↳ low temp
  - ↳ parameters not as per actual device
  - ↳ neglected interconnect load at output.
  - ↳ spice coding

- Circuit co-simulation facilitates:
  - ↳ schematic editor
  - ↳ parametric analysis
  - ↳ formatting of output data
  - ↳ save coding time

* SET logic (Inverter) design, analysis and simulation.

- ↳ Unipolar voltage response (usually a bipolar SET uses)
- ↳ Fixed supply and Biasing voltages as per 22nm planer bulk CMOS (800mV)
- ↳ $R_t = 1 M\Omega$
- ↳ at room temp (300K)

• Parameters

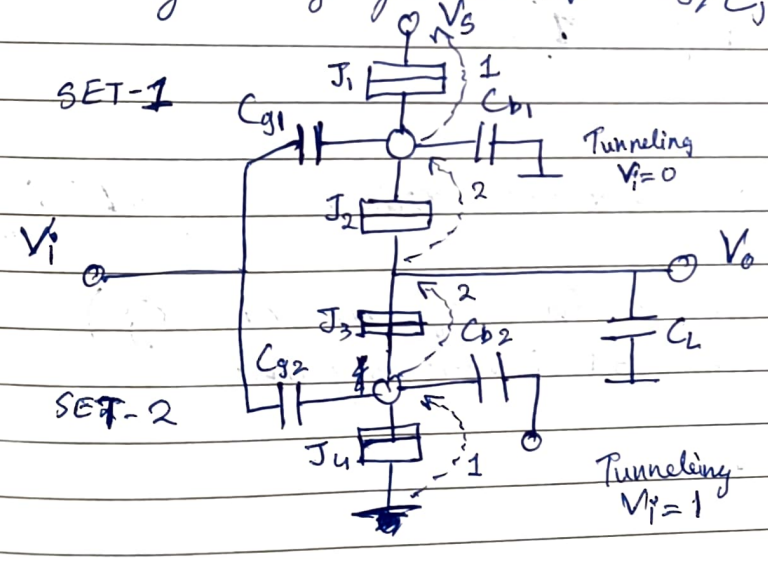
↳ operating temp $T \alpha \alpha^2 / 2 k_B C_\Sigma$

take, $e^2/C_\Sigma = 40 k_B T$

↳ Voltage level α e/C_Σ

↳ max freq α $1/R_t C_\Sigma$; if $C_L > C_\Sigma$, then C_L affects freq.

↳ inverting voltage gain $A_V = C_g/C_j$, also a fn of temp.



(see graphs on pg 31, 32, 33)

(Img pg-37)

↳ Delay & load at SET inverter output are directly proportional.

* Model of SET layer on CMOS carries

M_2 metal — 69nm
Dielectric — 59nm
[illegible] — 5nm → SET & interconnects
SiO_2 — 45nm
M1 metal — 63nm
Bulk CMOS — 137nm

(Img Pg - 41)

* Enhance SET inverter driving capability

↳ Increase tunnel jn capacitance (C_j) ($3e^{-20}$ to $7e^{-}$) hence reduce SET inverter gain.

↳ Decrease R_t.

↳ delay can greatly be improved (87ps to 34ps) by connecting 3 inverter in parallel.

↳ delay improved by more no. of parallel SET.

(Img pg - 47)