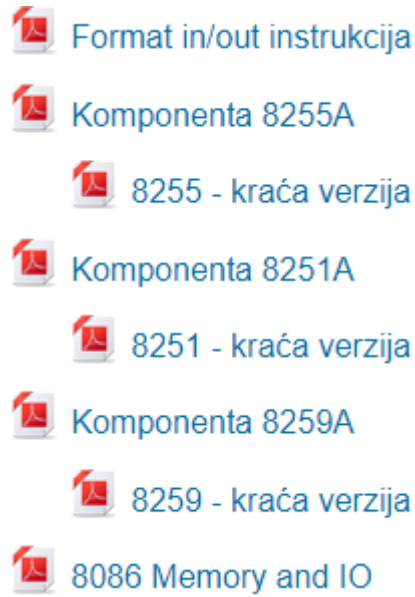
Mikroračunarski sistemi 2OER6O04

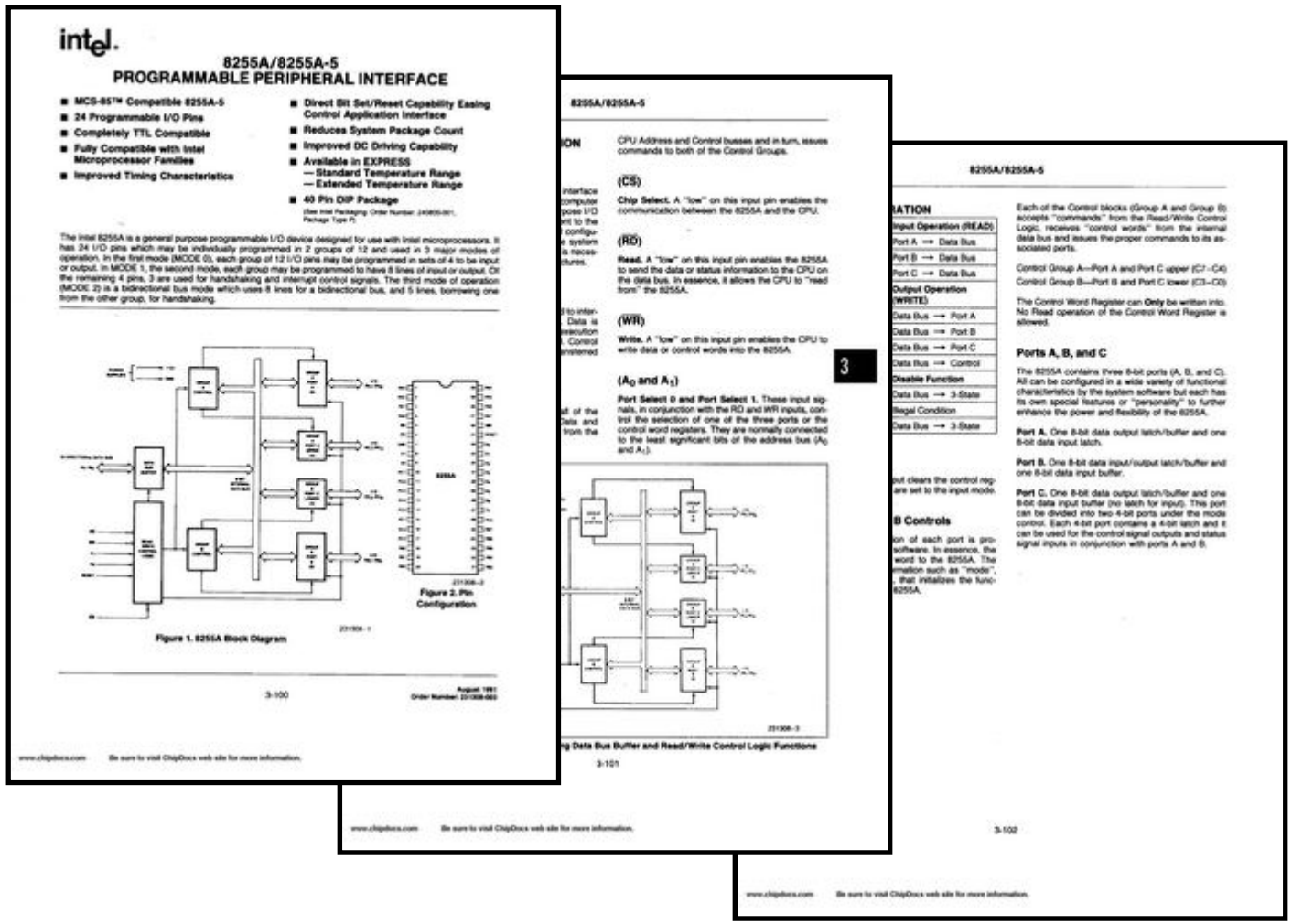
Vežbe 01

Datasheets

- Podatke o komponentama ne morate pamtiti
- Mogu se koristiti dokumentacija (*datasheets*) proizvođača
- Izvori
  - CS
  - Web
- Dozvoljeno poneti na pismeni deo ispita



Kompletna verzija



intel.

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range
- 40 Pin DIP Package

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

Figure 1. 8255A Block Diagram

Figure 2. Pin Configuration

3-100

8255A/8255A-5

CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

3

g Data Bus Buffer and Read/Write Control Logic Functions

3-101

8255A/8255A-5

Input Operation (READ)
Port A → Data Bus
Port B → Data Bus
Port C → Data Bus
Output Operation (WRITE)
Data Bus → Port A
Data Bus → Port B
Data Bus → Port C
Data Bus → Control
Disable Function
Data Bus → 3-State
Illegal Condition
Data Bus → 3-State

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A—Port A and Port C upper (C7–C4)

Control Group B—Port B and Port C lower (C3–C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

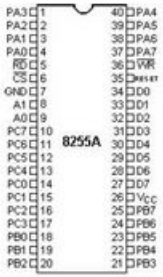
3-102

Skraćena verzija

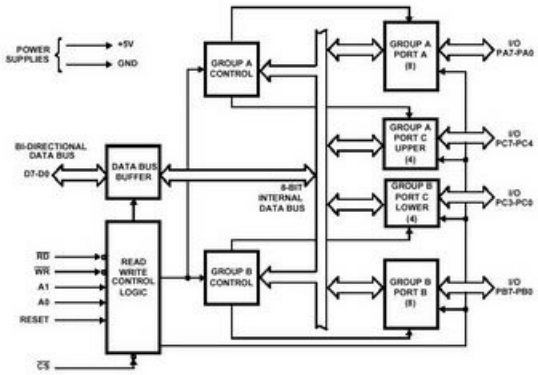
8255A/8255A-5

Programmable peripheral interface

a. Pin configuration



b. 8255A block diagram



c. Pin names

D_7–D_0	Data Bus (Bi-Directional)
RESET	Reset Input
CS	Chip Select
RD	Read Input
WR	Write Input
A0, A1	Port Address
PA7–PA0	Port A (BIT)
PB7–PB0	Port B (BIT)
PC7–PC0	Port C (BIT)
VCC	+5 Volts
GND	0 Volts

d. Mode definition summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	↔
PA_1	IN	OUT	IN	OUT	↔
PA_2	IN	OUT	IN	OUT	↔
PA_3	IN	OUT	IN	OUT	↔
PA_4	IN	OUT	IN	OUT	↔
PA_5	IN	OUT	IN	OUT	↔
PA_6	IN	OUT	IN	OUT	↔
PA_7	IN	OUT	IN	OUT	↔
PB_0	IN	OUT	IN	OUT	—
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

MODE 0 OR MODE ONLY

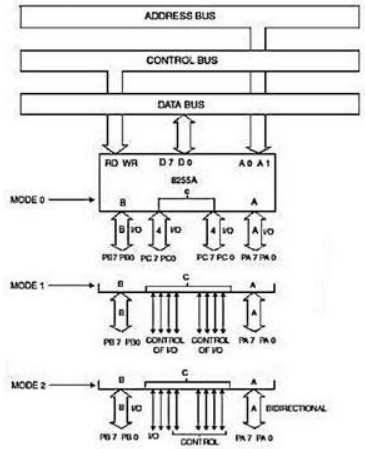
e. 8255 Basic operation

RD	WR	CS	A_1	A_0	Input (Read) cycle
0	1	0	0	0	Port A to Data bus
0	1	0	0	1	Port B to Data bus
0	1	0	1	0	Port C to Data bus
0	1	0	1	1	CWR to Data bus

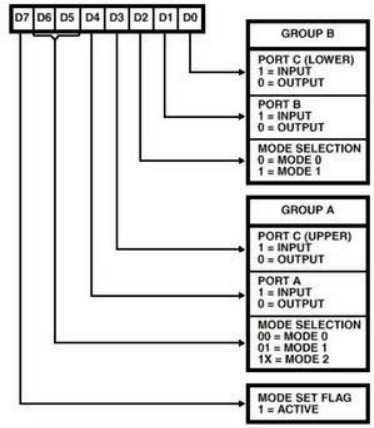
RD	WR	CS	A_1	A_0	Output (Write) cycle
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

RD	WR	CS	A_1	A_0	Function
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

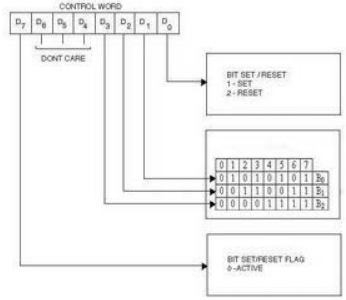
f. Basic mode definitions and bus interface



g. Control word format



h. Bit set/reset format – port C



Zadatak 1

Za mikroprocesor i8086 projektovati mikroračunarski sistem sa osam tastera i 8 LED dioda uz pomoć dve komponente 8255A. Na port A prve komponente treba vezati diode, a na port B druge kompnente tastere. Inicijalno nijedna dioda ne svetli. Nakon pritiska nekog od tastera treba da zasvetli odgovarajuća dioda i treba da svetli sve dok je taster pritisnut. Napisati adekvatne procedure.

a) Koristi se IO-mapirani ulaz/izlaz (8bit adrese). Komponenta 1 je na adresi A8h, a Kompnenta 2 je na A9h.

b) Koristi se memorijski-mapirani ulaz/izlaz: Komponenta 1 je na adresi 83FE8h, a Kompnenta 2 je na 83FE9h.

Struktura rešavanja zadataka

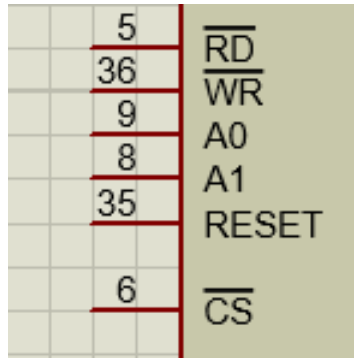
- Adresiranje
- Šema povezivanja
- Asemblerski kod
  - Konfiguracija komponenti
  - Logika i obrada

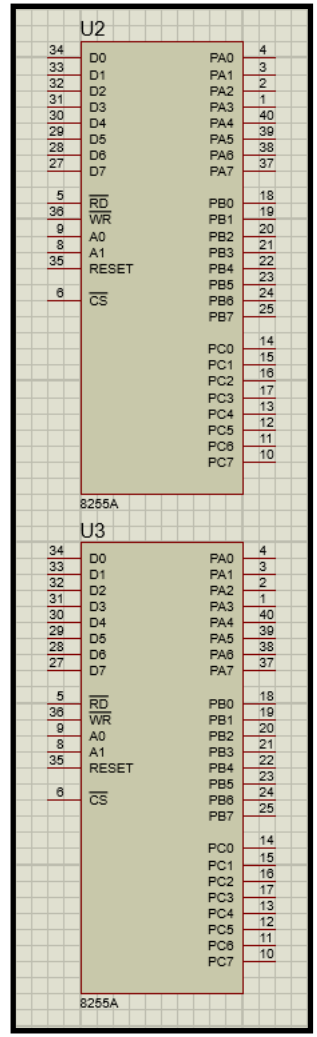
Rešenje pod a)

- Za zadatak pod a) koristi se IO-mapirani ulaz/izlaz (8bit adrese). Komponenta 1 je na adresi A8h, a Kompnenta 2 je na A9h.

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
					Output Operation (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					Disable Function
X	X	X	X	1	Data Bus → 3-State
1	1	0	1	0	Illegal Condition
X	X	1	1	0	Data Bus → 3-State



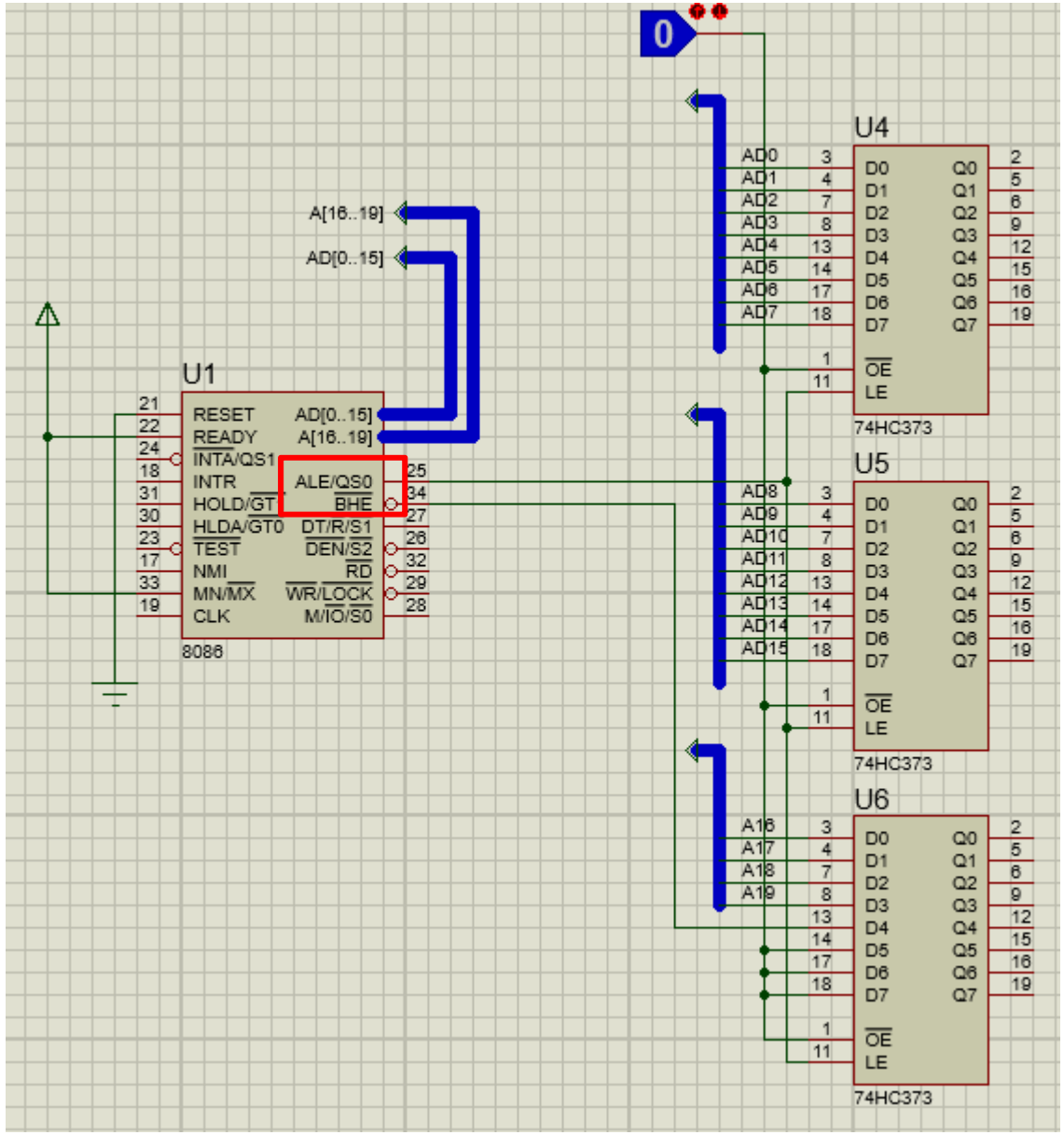


Adresiranje

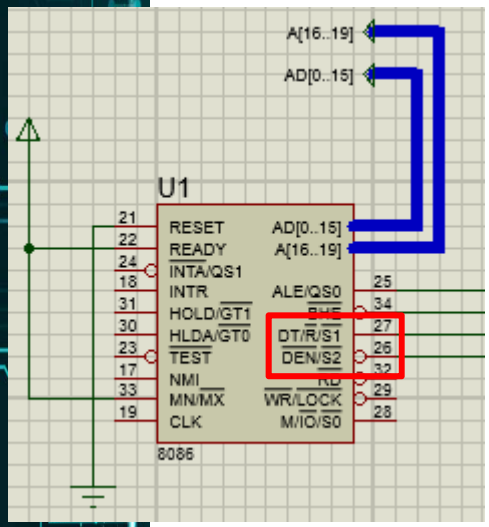
A19-A8	A7	A6	A5	A4	A3	A2	A1	A0	Adr	Port
0	1	0	1	0	1	0	0	0	A8h	PortA1
0	1	0	1	0	1	0	1	0	AAh	PortB1
0	1	0	1	0	1	1	0	0	ACh	PortC1
0	1	0	1	0	1	1	1	0	AEh	CW1
0	1	0	1	0	1	0	0	1	A9h	PortA2
0	1	0	1	0	1	0	1	1	ABh	PortB2
0	1	0	1	0	1	1	0	1	ADh	PortC2
0	1	0	1	0	1	1	1	1	AFh	CW2
←			CS			→			A1	A0

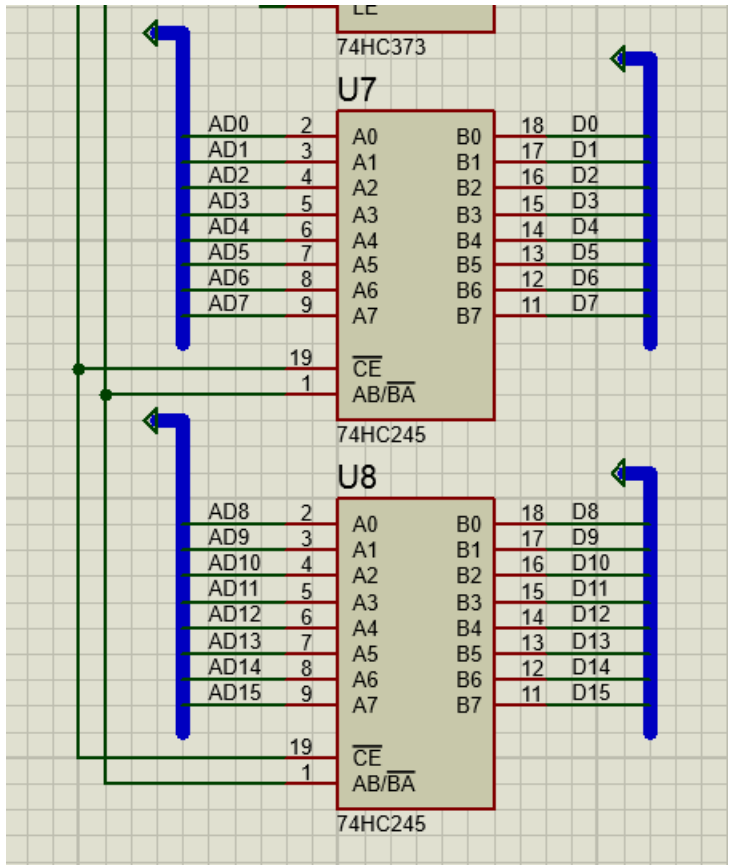
A8H = 10101000 B

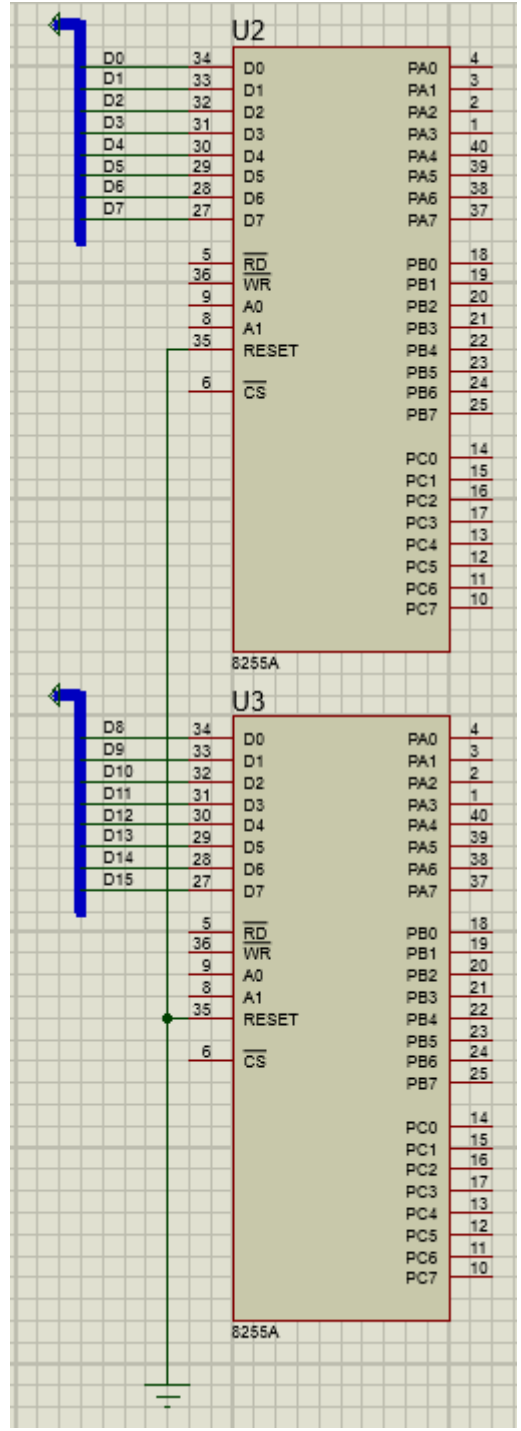
Lečovanje adresa



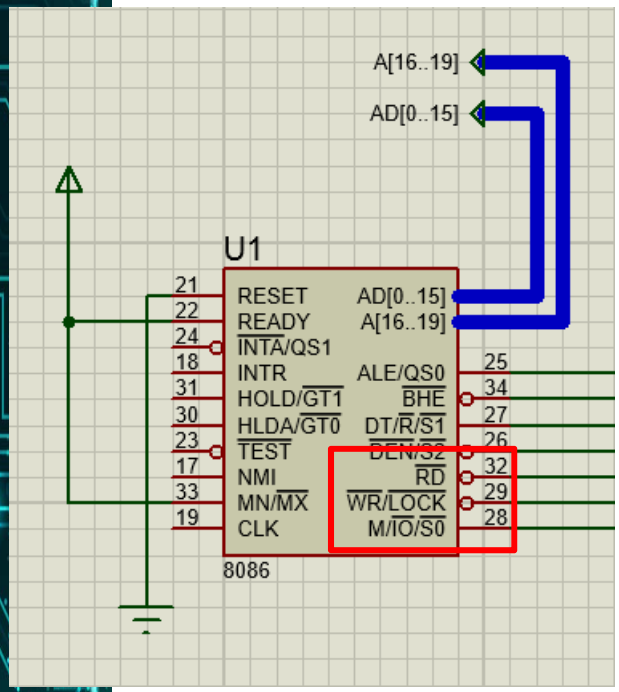
Magistrala podataka

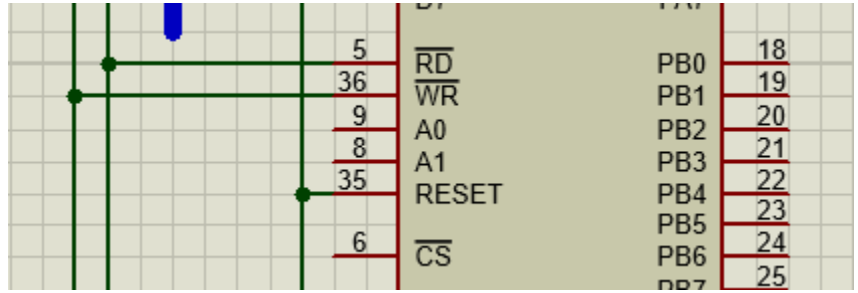


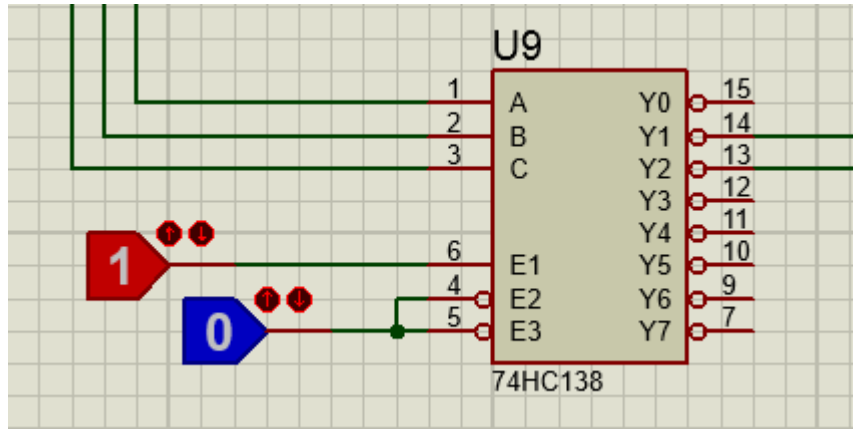




Dekodiranje upravljačkih signala





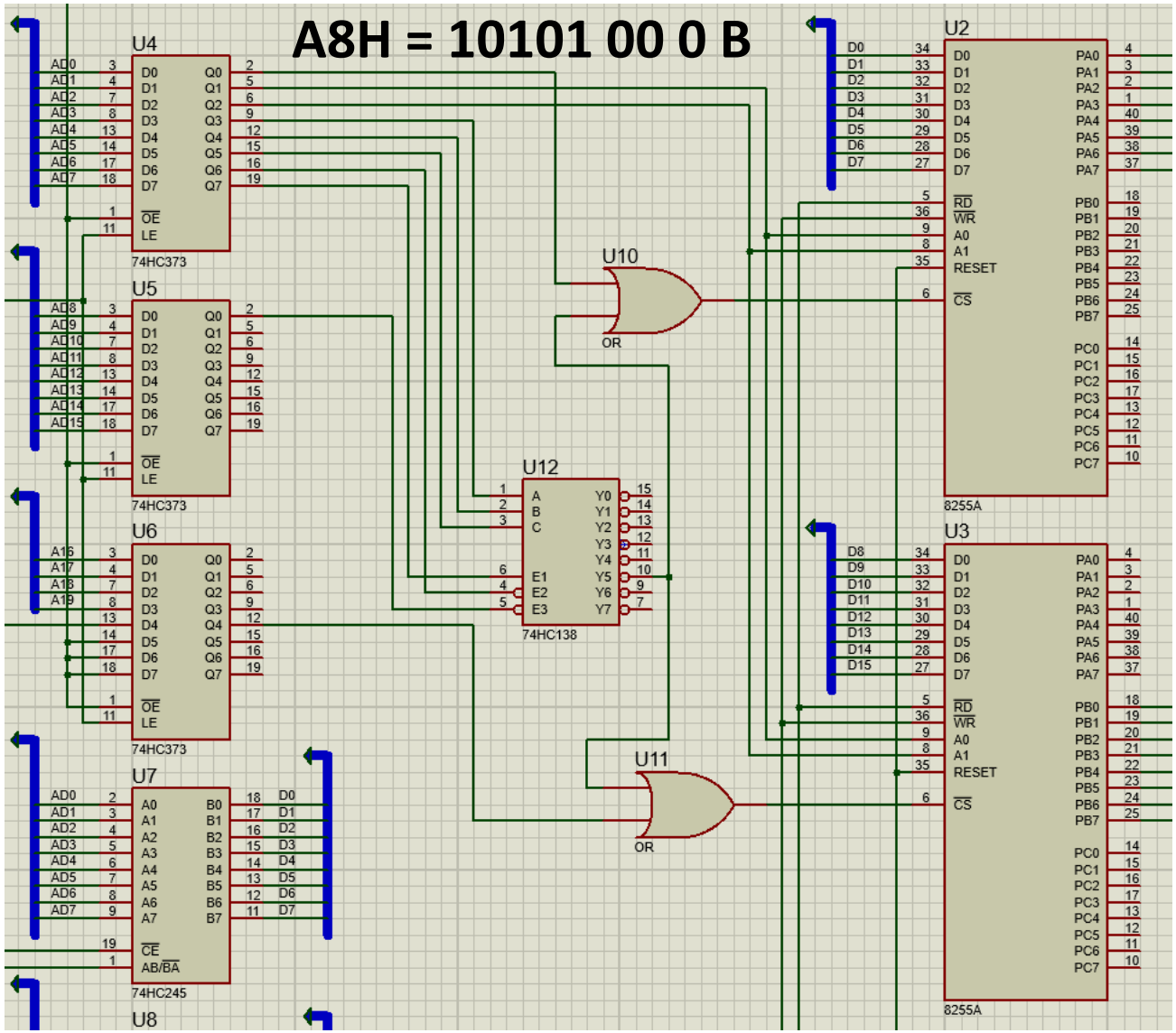


Adresiranje

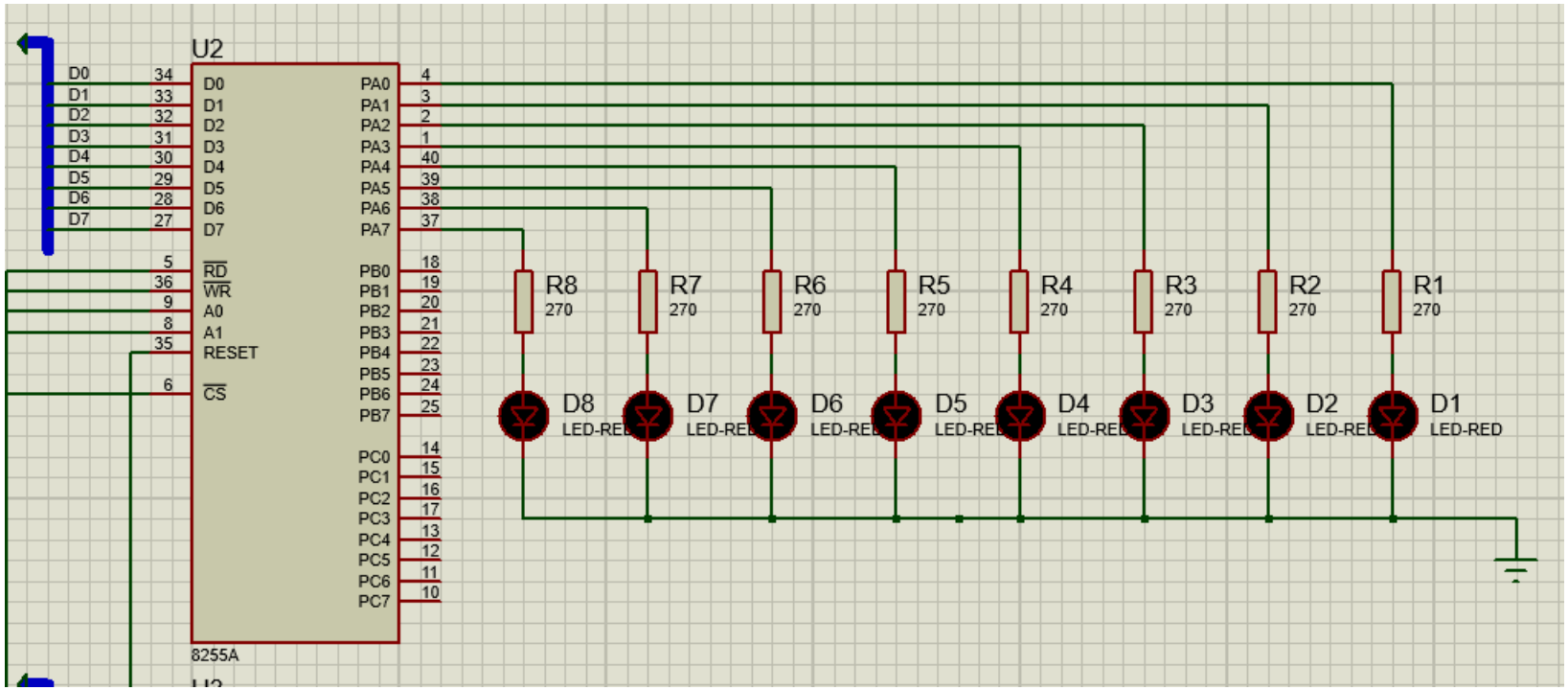
A19-A8	A7	A6	A5	A4	A3	A2	A1	A0	Adr	Port
0	1	0	1	0	1	0	0	0	A8h	PortA1
0	1	0	1	0	1	0	1	0	AAh	PortB1
0	1	0	1	0	1	1	0	0	ACh	PortC1
0	1	0	1	0	1	1	1	0	AEh	CW1
0	1	0	1	0	1	0	0	1	A9h	PortA2
0	1	0	1	0	1	0	1	1	ABh	PortB2
0	1	0	1	0	1	1	0	1	ADh	PortC2
0	1	0	1	0	1	1	1	1	AFh	CW2
←			CS			→			A1	A0

A8H = 10101000 B

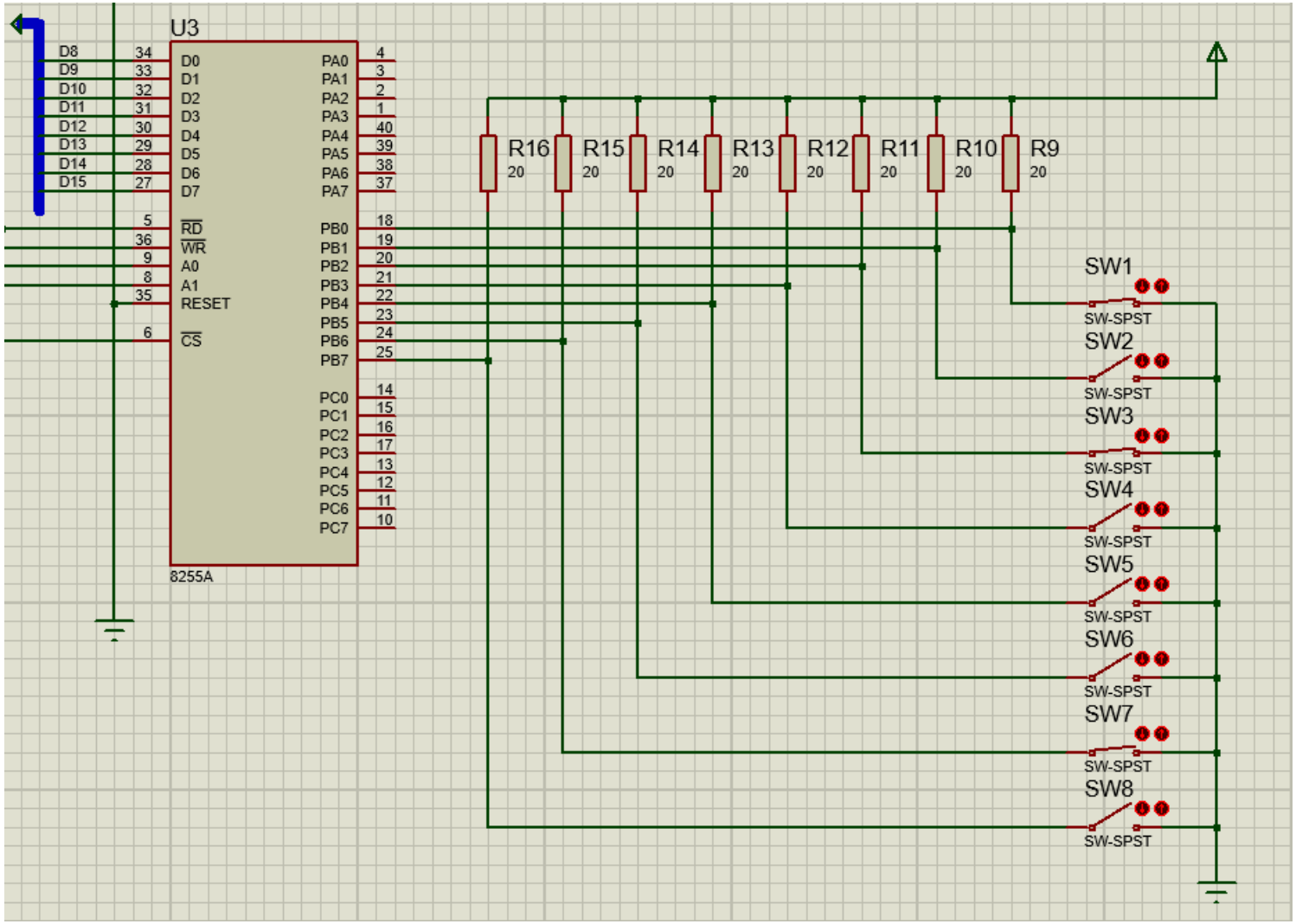
Adresiranje



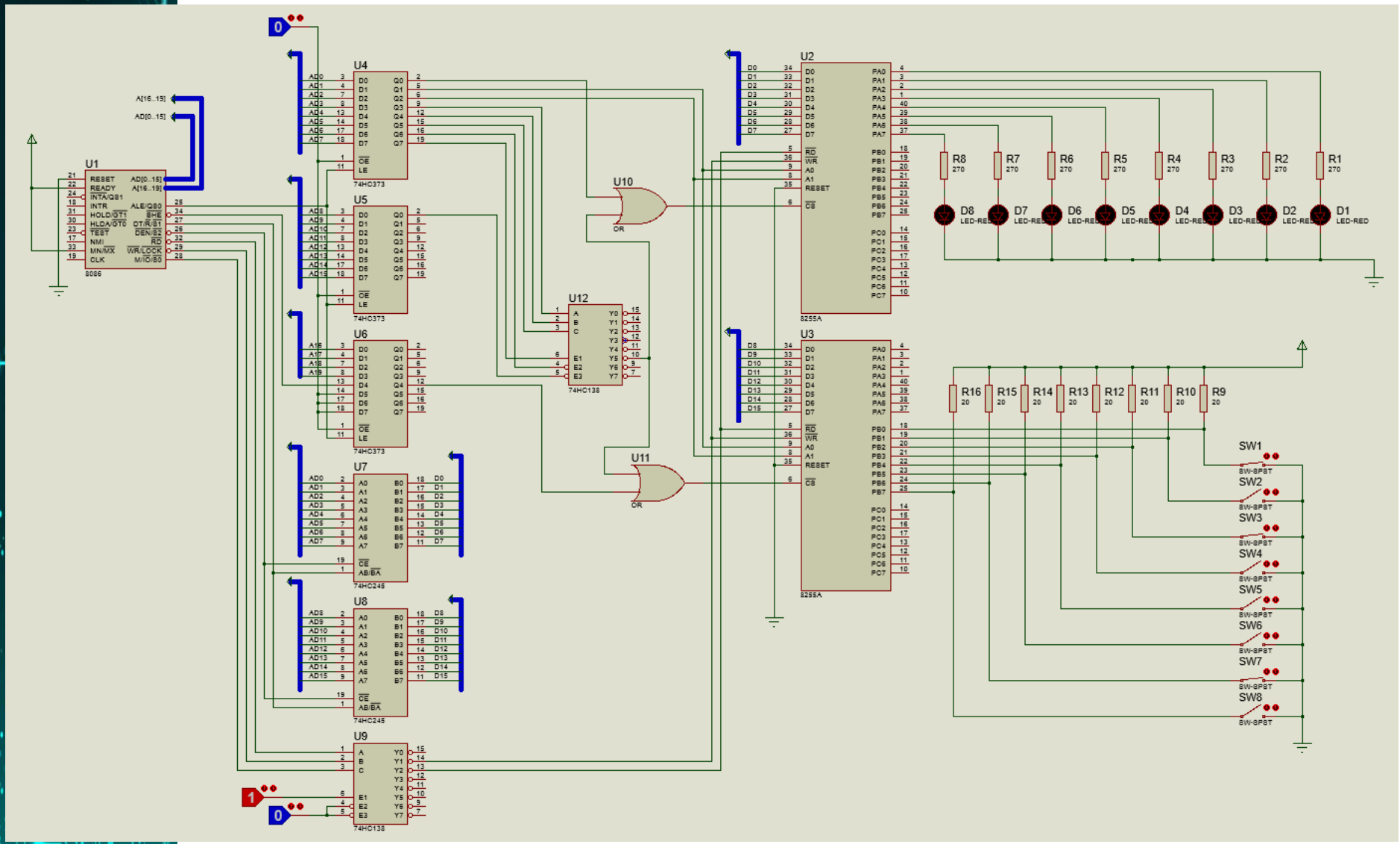
Povezivanje LED dioda



Povezivanje tastera



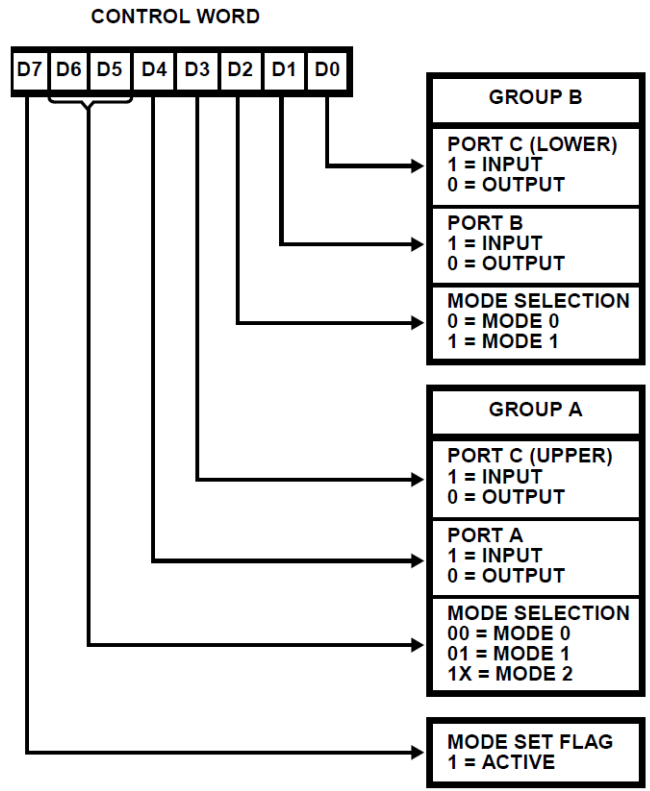
Kompletna šema



Programiranje

```
11
12  CODE SEGMENT
13      ASSUME CS:CODE
14
15  START:
16  ; Definicija adresa
17        PORTA1 EQU 0A8H
18        PORTB2 EQU 0ABH
19        CW1 EQU 0AEH
20        CW2 EQU 0AFH
21
22  ; Patch za normalan rad 8086 simulatora
23        OUT 00H,AL
24        IN AL,00H
25
26  ; Konfiguracija komponenti
27        MOV AX,8280H
28        MOV DX,CW1
29        OUT DX,AX
30
31
32
33  PETLJA:
34  ; Citanje sa porta B komponente 2
35        IN AL,PORTB2
36  ; Upis na port A komponente 1
37        NOT AL
38        OUT PORTA1, AL
39        JMP PETLJA
40
41  CODE    ENDS
42          END START
43  END
```

A19-A8	A7	A6	A5	A4	A3	A2	A1	A0	Adr	Port
0	1	0	1	0	1	0	0	0	A8h	PortA1
0	1	0	1	0	1	0	1	0	AAh	PortB1
0	1	0	1	0	1	1	0	0	ACh	PortC1
0	1	0	1	0	1	1	1	0	AEh	CW1
0	1	0	1	0	1	0	0	1	A9h	PortA2
0	1	0	1	0	1	0	1	1	ABh	PortB2
0	1	0	1	0	1	1	0	1	ADh	PortC2
0	1	0	1	0	1	1	1	1	AFh	CW2



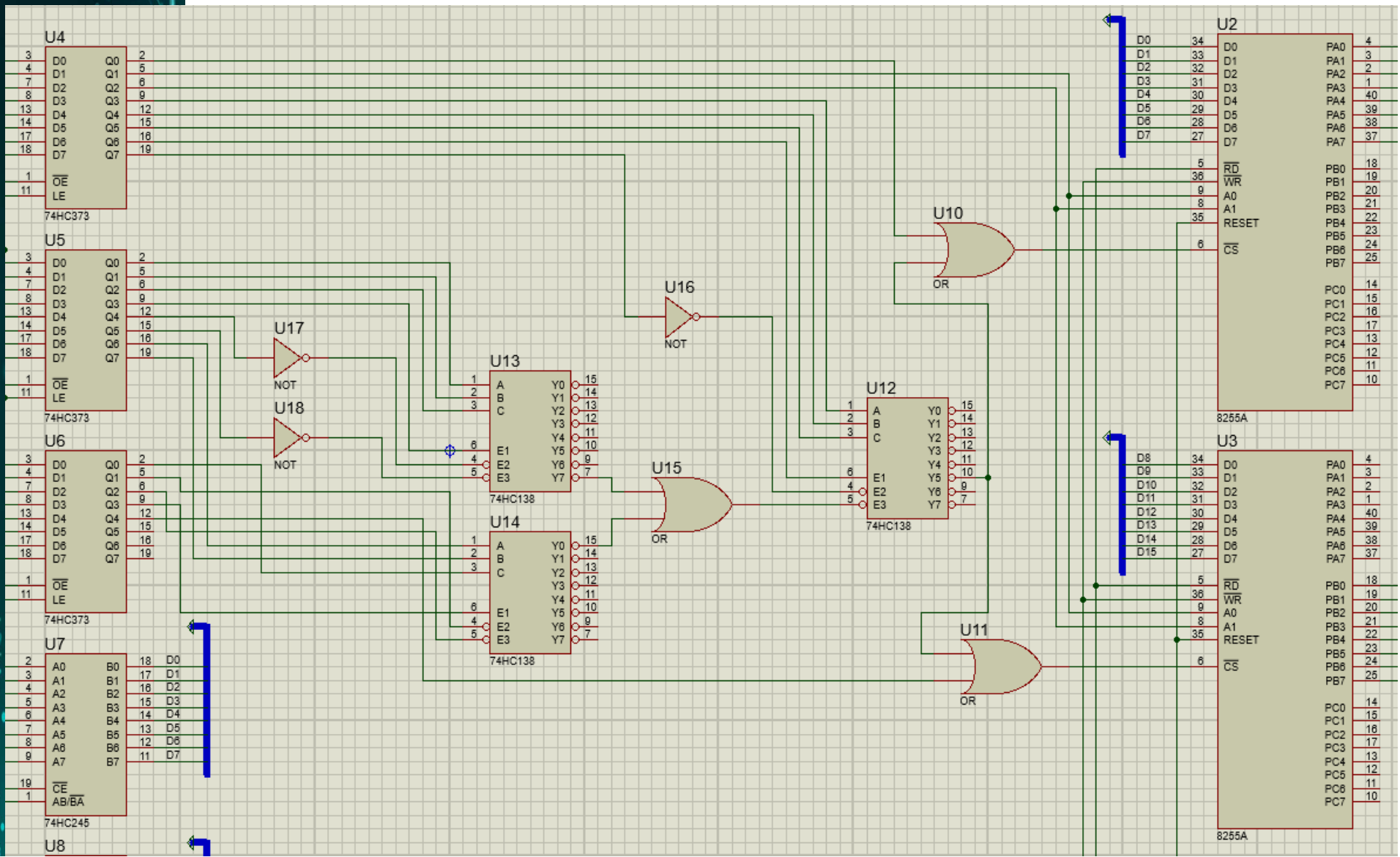
Rešenje pod b)

- Koristi se memorijski-mapirani ulaz/izlaz: Komponenta 1 je na adresi 83FE8h, a Kompnenta 2 je na 83FE9h.

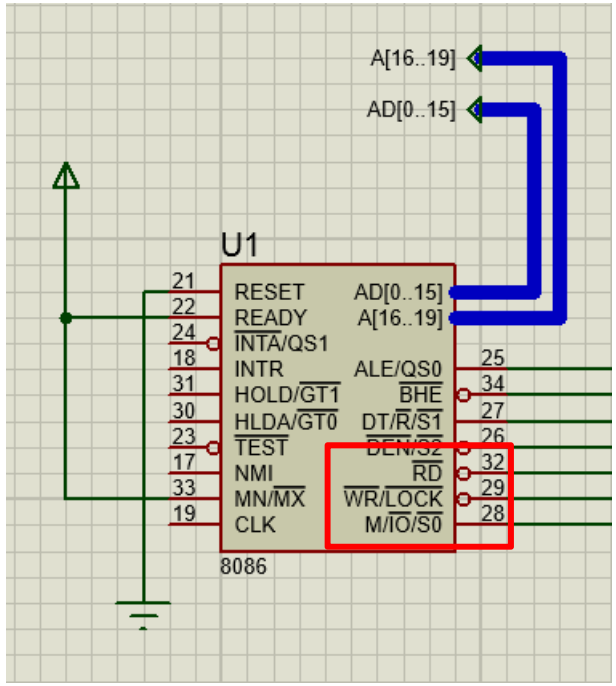
1000 0011 1111 1110 1000

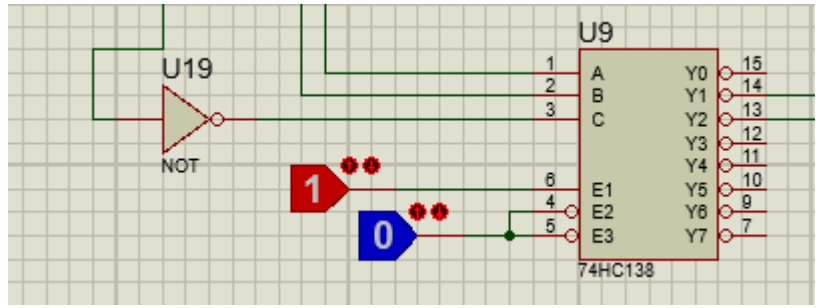
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Adr
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	A1
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1	0	B1
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	0	0	C1
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1	0	CW1
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	1	A2
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1	1	B2
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	0	1	C2
1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	CW2

Dekodiranje adrese

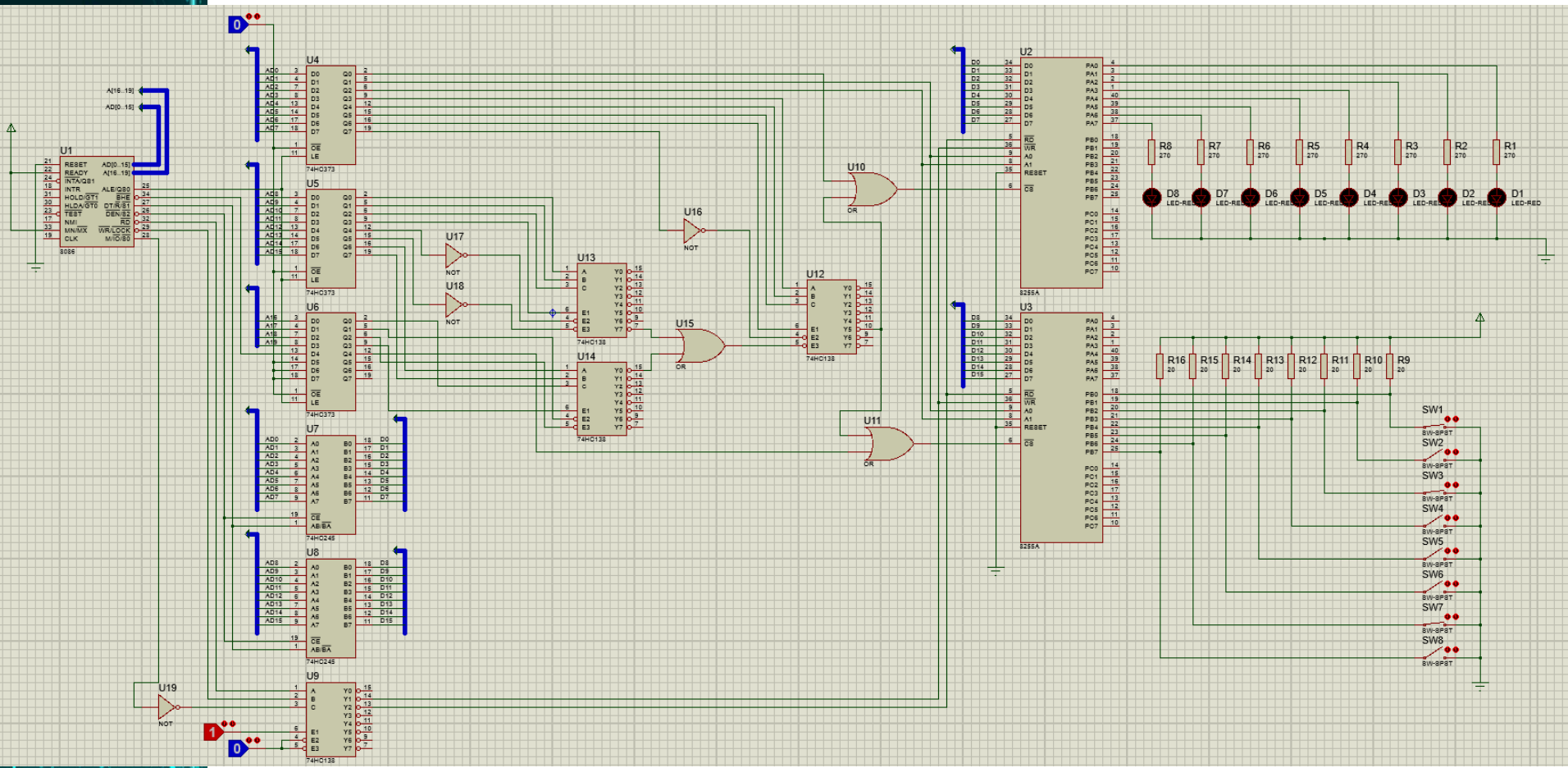


Dekodiranje upravljačkih signala





Kompletna šema



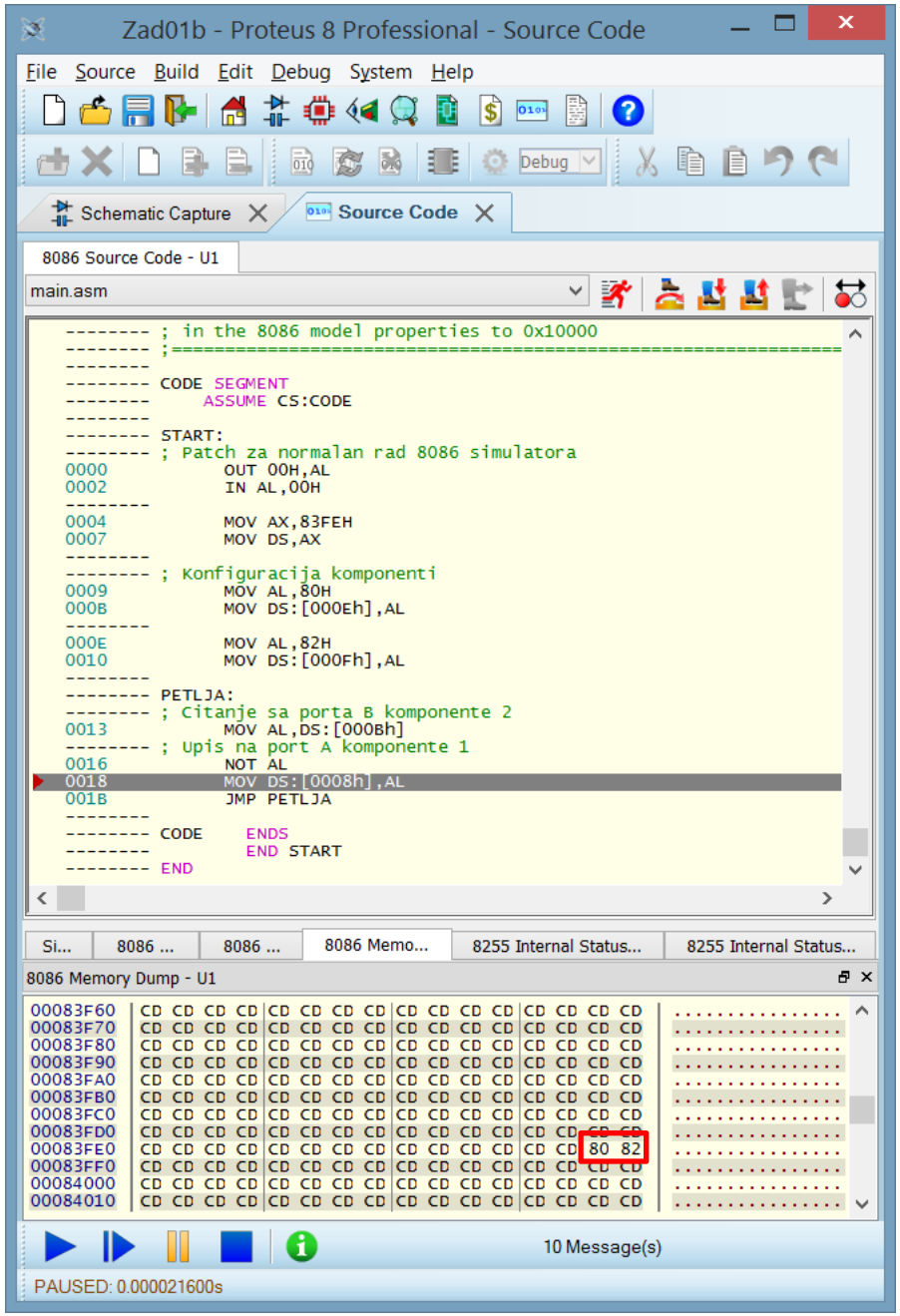
Programiranje

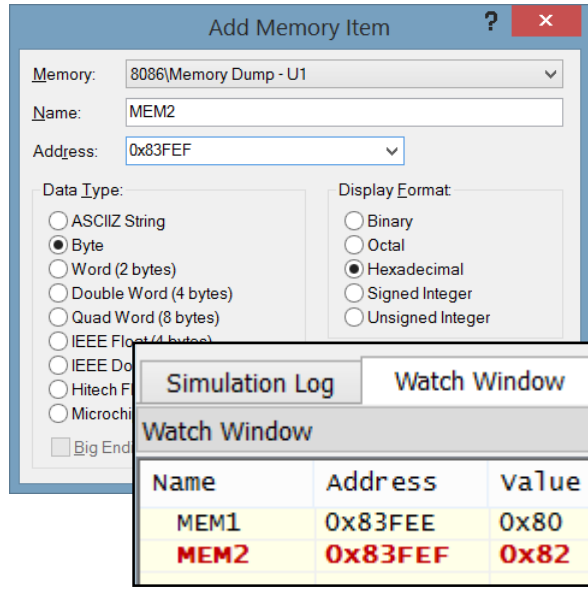
- MOV umesto IN/OUT
- Korišćenje DS
  - Početak segmenta na 83FEh
  - Efektivna adresa (20bit) = Segment (83FE0h) + Offset (000Eh)

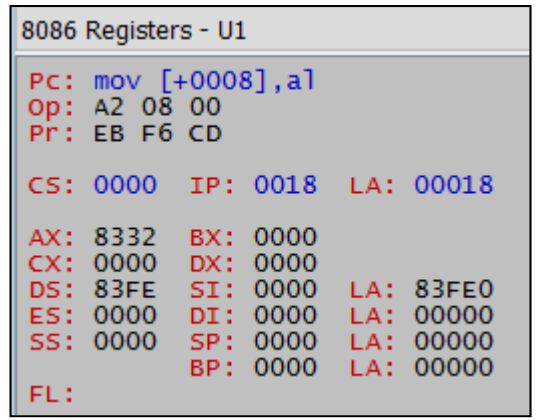
Programiranje

```
11
12  CODE SEGMENT
13      ASSUME CS:CODE
14
15  START:
16  ; Patch za normalan rad 8086 simulatora
17        OUT 00H,AL
18        IN AL,00H
19
20        MOV AX,83FEH
21        MOV DS,AX
22
23  ; Konfiguracija komponenti
24        MOV AL,80H
25        MOV DS:[000Eh],AL
26
27        MOV AL,82H
28        MOV DS:[000Fh],AL
29
30  PETLJA:
31  ; Citanje sa porta B komponente 2
32        MOV AL,DS:[000Bh]
33  ; Upis na port A komponente 1
34        NOT AL
35        MOV DS:[0008h],AL
36        JMP PETLJA
37
38  CODE    ENDS
39          END START
40  END
```

Provera


Zad01b - Proteus 8 Professional - Source Code
File Source Build Edit Debug System Help
Schematic Capture
Source Code
8086 Source Code - U1
main.asm
; in the 8086 model properties to 0x10000
CODE SEGMENT
ASSUME CS:CODE
START:
; Patch za normalan rad 8086 simulatora
0000 OUT 00H,AL
0002 IN AL,00H
0004 MOV AX,83FEH
0007 MOV DS,AX
; Konfiguracija komponenti
0009 MOV AL,80H
000B MOV DS:[000Eh],AL
000E MOV AL,82H
0010 MOV DS:[000Fh],AL
PETLJA:
; Citanje sa porta B komponente 2
0013 MOV AL,DS:[000Bh]
; Upis na port A komponente 1
0016 NOT AL
0018 MOV DS:[0008h],AL
001B JMP PETLJA
CODE ENDS
END START
END
Si... 8086 ... 8086 ... 8086 Memo... 8255 Internal Status... 8255 Internal Status...
8086 Memory Dump - U1
00083F60 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00083F70 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00083F80 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00083F90 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00083FA0 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00083FB0 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00083FC0 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00083FD0 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00083FE0 CD CD CD CD CD CD CD CD CD CD CD CD 80 82
00083FF0 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00084000 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
00084010 CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD CD
10 Message(s)
PAUSED: 0.000021600s


Add Memory Item
Memory: 8086\Memory Dump - U1
Name: MEM2
Address: 0x83FEF
Data Type:
ASCIIZ String
Byte
Word (2 bytes)
Double Word (4 bytes)
Quad Word (8 bytes)
Display Format:
Binary
Octal
Hexadecimal
Signed Integer
Unsigned Integer
Simulation Log
Watch Window
Watch Window
Name Address Value
MEM1 0x83FEE 0x80
MEM2 0x83FEF 0x82


8086 Registers - U1
Pc: mov [+0008],al
Op: A2 08 00
Pr: EB F6 CD
CS: 0000 IP: 0018 LA: 00018
AX: 8332 BX: 0000
CX: 0000 DX: 0000
DS: 83FE SI: 0000 LA: 83FE0
ES: 0000 DI: 0000 LA: 00000
SS: 0000 SP: 0000 LA: 00000
BP: 0000 LA: 00000
FL: