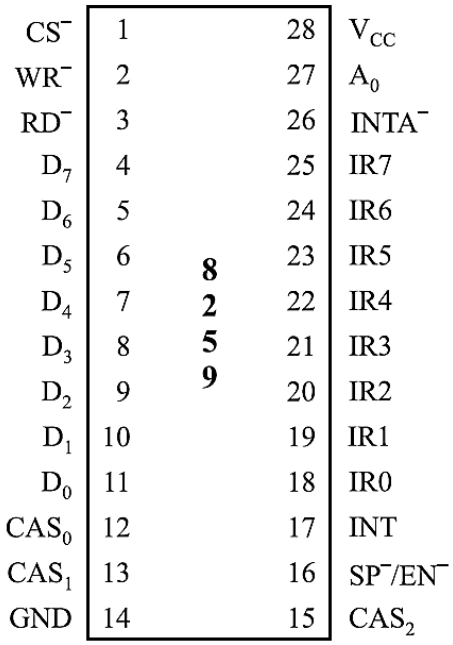
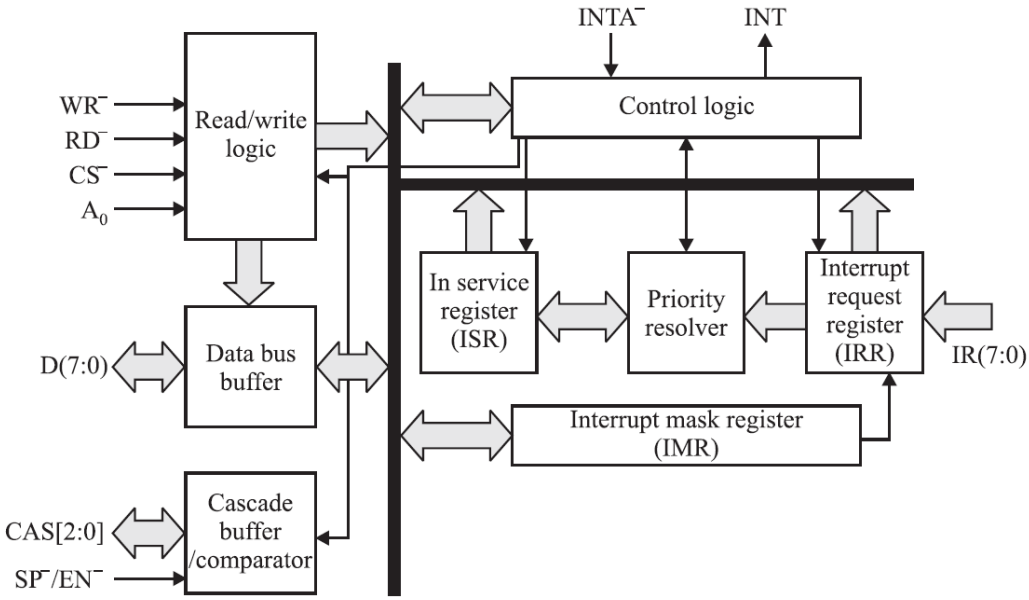
8259A/8259A-2/8259A-8

Programmable interrupt controller

a. Pin configuration



b. 8259A block diagram

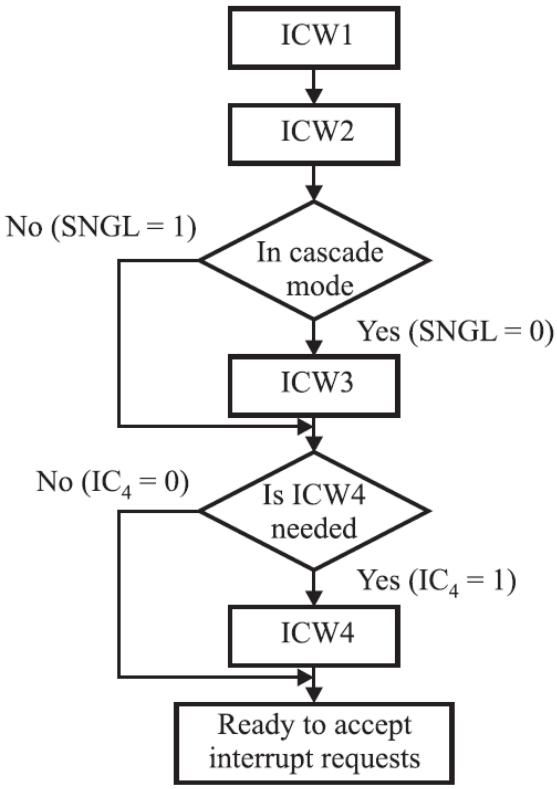


c. Pin names *

D_0-D_7	Data bus – bidirectional
IR0-IR7	Interrupt request inputs
RD^-	Read input
WR^-	Write input
A0	Command select address
CS^-	Chip select
CAS2-CAS0	Cascade lines
SP^-/EN^-	Slave program/enable buffer
INT	Interrupt output
$INTA^-$	Interrupt acknowledge input

* x^- je isto što i $\overline{X}$, X/Y^- je isto što i $X/\overline{Y}$

d. Initialization sequence



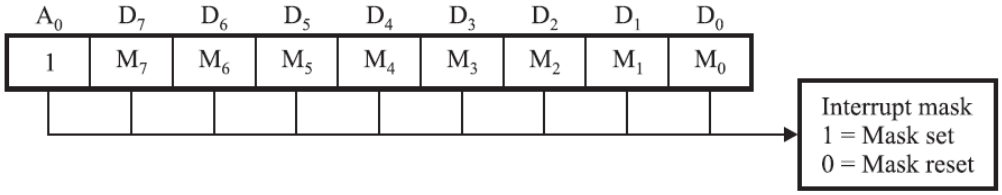
e. 8259 Basic operation

A0	D4	D3	RD⁻	WR⁻	CS⁻	Input operation (read)
0			0	1	0	IRR, ISR or Interrupting Level -> Data bus (Note 1)
1			0	1	0	IMR -> Data bus
						Output operation (write)
0	0	0	1	0	0	Data bus -> OCW2
0	0	1	1	0	0	Data bus -> OCW3
0	1	X	1	0	0	Data bus -> ICW1
1	X	X	1	0	0	Data bus -> OCW1,ICW2,ICW3,ICW4(Note 2)
						Disable function
X	X	X	1	1	0	Data bus - 3 state (no operation)
X	X	X	X	X	1	Data bus - 3 state (no operation)

Note 1 – Selection of IRR, ISR or Interrupting Level is based on the content of OCW3 written before the read operation

Note 2 – On-chip sequencer logic queues these commands into proper sequence

f. OCW1, A0=1



g. OCW2, A0=0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R	SL	EOI	0	0	L_2	L_1	L_0

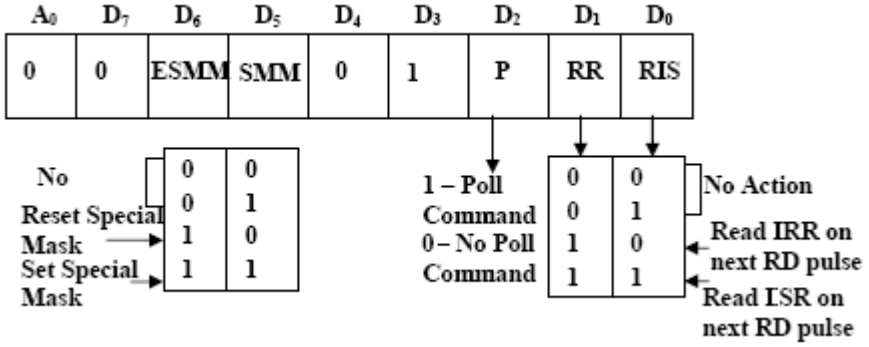
R	SL	EOI	
0	0	1	Non-specific EOI command
0	1	1	*Specific EOI command
1	0	1	Rotate on non-specific EOI command
1	0	0	Rotate in automatic EOI mode (clear)
0	0	0	Rotate in automatic EOI mode (clear)
1	1	1	*Rotate on specific EOI command
1	1	0	*Set priority command
0	1	0	No operation

*L_0–L_2 are used.

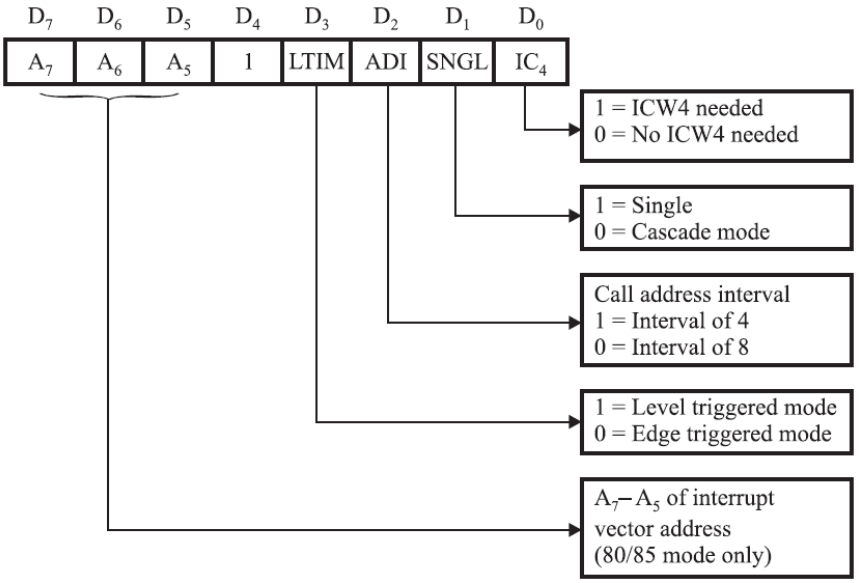
L_2	L_1	L_0	
0	0	0	IR level 0
0	0	1	IR level 1
0	1	0	IR level 2
0	1	1	IR level 3
1	0	0	IR level 4
1	0	1	IR level 5
1	1	0	IR level 6
1	1	1	IR level 7

h. OCW3, A0=0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	ESMM	SMM	0	1	P	RR	RIS



i. ICW1, A0=0



j. ICW2, A0=1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_7	A_6	A_5	A_4	A_3	X	X	X

Interrupt	A_7	A_6	A_5	A_4	A_3			
IR0	A_7	A_6	A_5	A_4	A_3	0	0	0
IR1	A_7	A_6	A_5	A_4	A_3	0	0	1
IR2	A_7	A_6	A_5	A_4	A_3	0	1	0
IR3	A_7	A_6	A_5	A_4	A_3	0	1	1
IR4	A_7	A_6	A_5	A_4	A_3	1	0	0
IR5	A_7	A_6	A_5	A_4	A_3	1	0	1
IR6	A_7	A_6	A_5	A_4	A_3	1	1	0
IR7	A_7	A_6	A_5	A_4	A_3	1	1	1

k. ICW3 master, A0=1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

l. ICW3 slave, A0=1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	ID_2	ID_1	ID_0

Slave identification with ICW3

Master IR number	ID_2	ID_1	ID_0
IR7	1	1	1
IR6	1	1	0
IR5	1	0	1
IR4	1	0	0
IR3	0	1	1
IR2	0	1	0
IR1	0	0	1
IR0	0	0	0

m. ICW4, A0=1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SFNM	BUF	M/S	AEOI	µPM

1 = Special fully nested mode
0 = Not special fully nested mode

1 = 8086/8088 Mode
0 = MCS-80/85 Mode

1 = Auto EOI
0 = Normal EOI

0	X	Non buffered mode
1	0	Buffered mode/slave
1	1	Buffered mode/master