



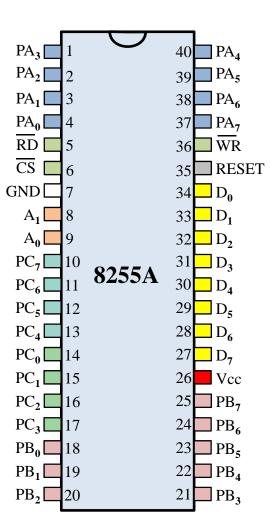
8255A



8255A programabilni periferijski interfejs

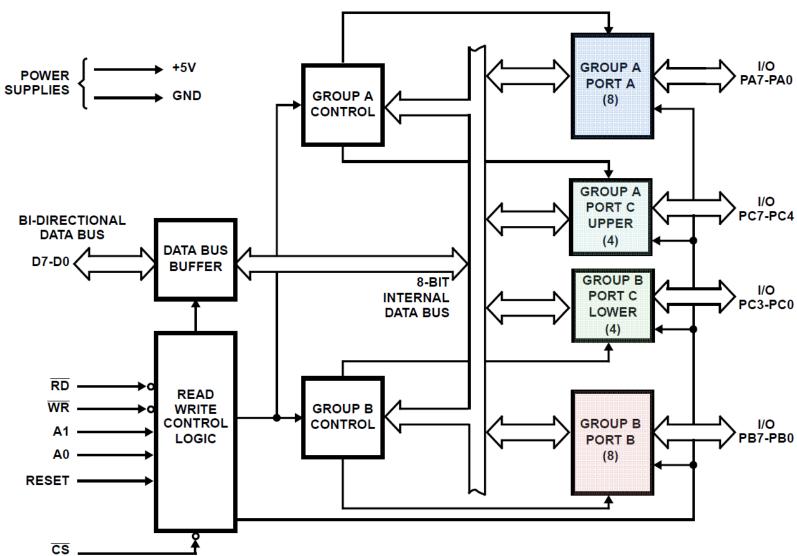
- 24 programabilna U/I pina
- Tri moda rada
- Direktni set/reset

8255A



- Vcc napajanje (+5V)
- GND uzemljenje
- D₀-D₇ magistrala podataka
- RESET briše kontrolni registar i vraća sve portove na "input" mod
- CS (chip select) omogućuje magistralu podataka i komunikaciju sa CPU
- RD (read) čitanje statusa ili podataka sa portova
- WR (write) učitavanje kontrolne reči i podataka u 8255A
- A₀-A₁ (zajedno sa RD i WR) adresira jedan od 3 porta ili kontrolni registar
- PA₀-PA₇ port A (8-bitni)
- $PB_0 PB_7 port B (8-bitni)$
- PC₀-PC₇ port C (8-bitni)

Logička šema





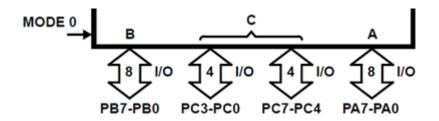
Osnovni modovi rada

- Mod 0 Osnovni ulaz/izlaz
- Mod 1 Strobovani ulaz/izlaz
- Mod 2 Bidirekciona magistrala



Mod 0

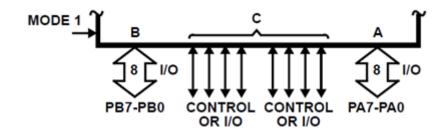
- Dva 8-bitna i dva 4-bitna porta
- Svaki port može biti ulazni ili izlazni
- Izlazi su "lečovani"
- Ulazi nisu lečovani
- 16 mogućih (različitih) konfiguracija





Mod 1

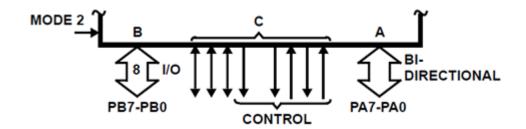
- Omogućuje U/I transfer uz "hand shake" signale
- 2 grupe portova (A i B)
- Svaka grupa sadrži 8-bitni port i 4-bitni
- 8-bitni portovi podataka mogu biti ulazni ili izlazni, i u oba slučaja su podaci "lečovani"
- 4-bitni portovi se koriste za upravljanje i status
 8-bitnih portova



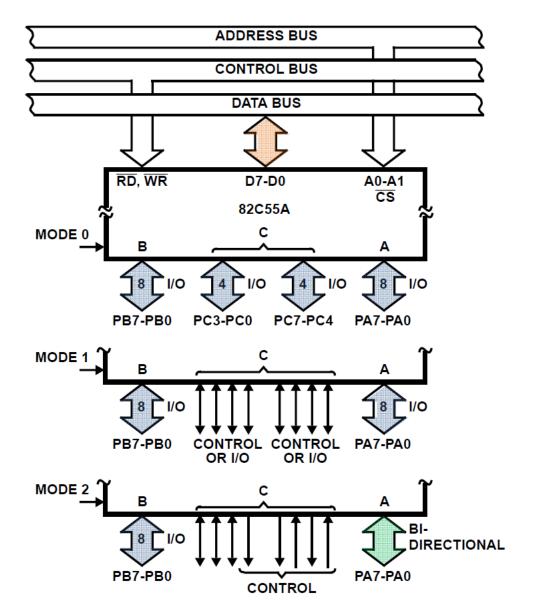


Mode 2

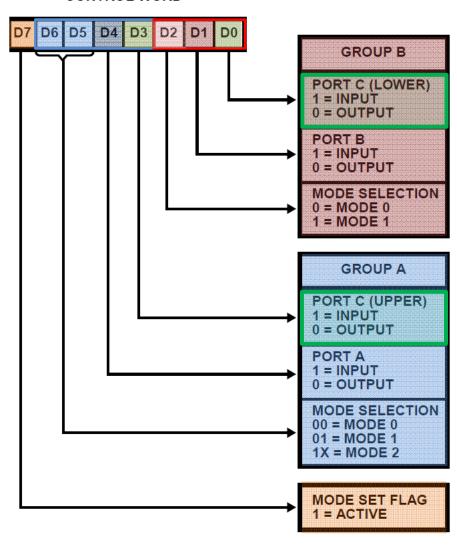
- Omogućuje komunikaciju sa periferijom preko jedne 8-bitne bidirekcione magistrale
- "Hand shake" signali upravljaju tokom
- Koristi se samo za grupu A
- Jedan 8-bitni bidirekcioni port (A) i 5-bitni upravljački port (C), koji upravlja i daje status bidirekcione magistrale
- I ulazi i izlazi su lečovani



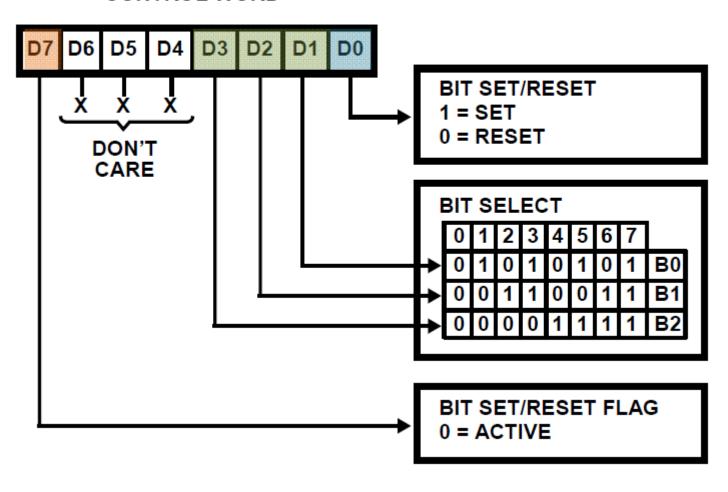
Osnovni modovi i interfejs



Definisanje moda rada

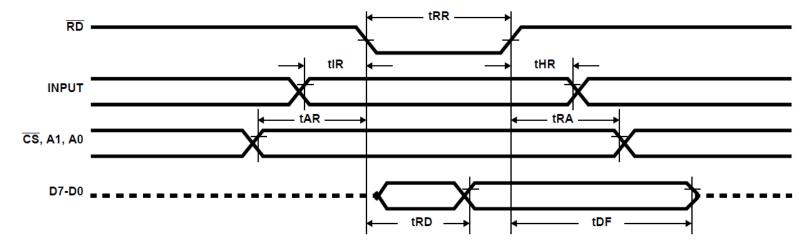


Bit Set/Reset format

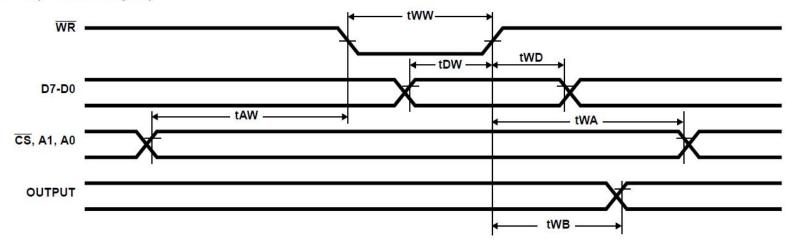


Mod 0 vremenski dijagrami

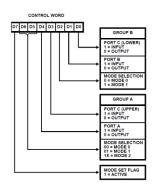
Mode 0 (Basic Input)



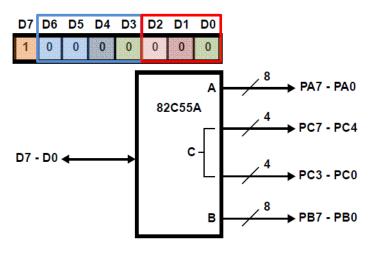
Mode 0 (Basic Output)



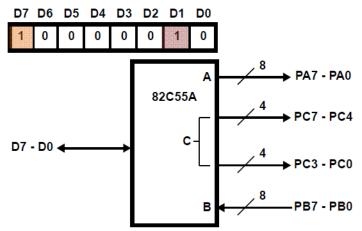
Mode 0 – Primer 1



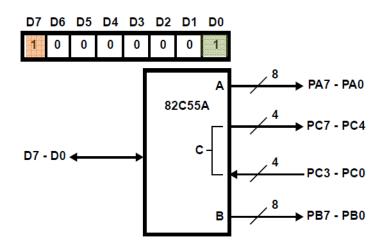
CONTROL WORD #0

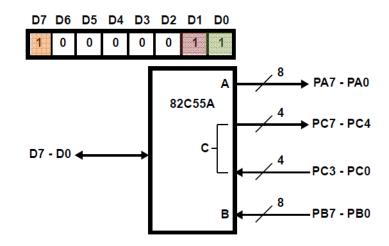


CONTROL WORD #2



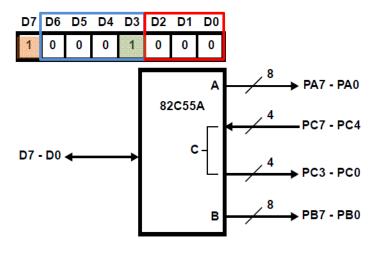
CONTROL WORD #1



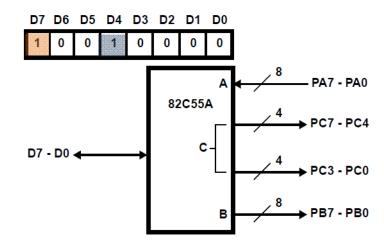


Mode 0 – Primer 2

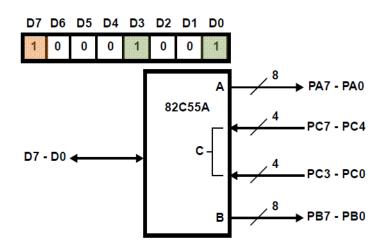
CONTROL WORD #4

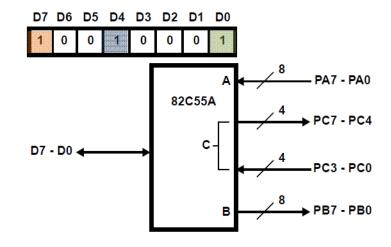


CONTROL WORD #8



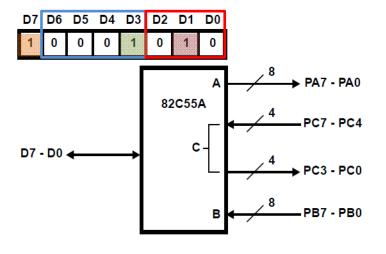
CONTROL WORD #5



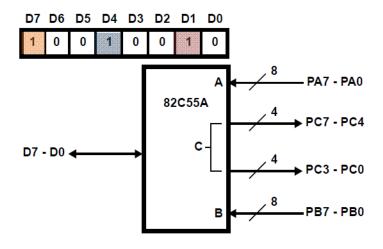


Mode 0 – Primer 3

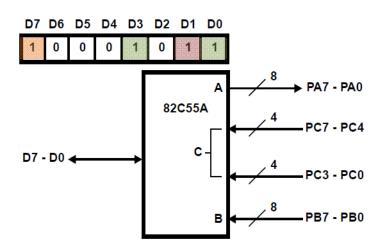
CONTROL WORD #6

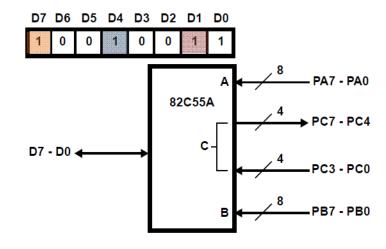


CONTROL WORD #10



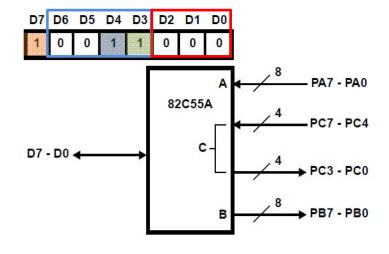
CONTROL WORD #7



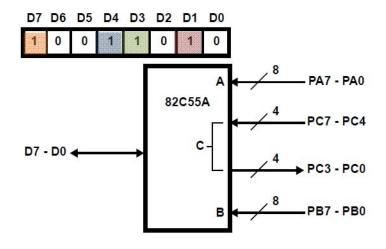


Mode 0 - Primer 4

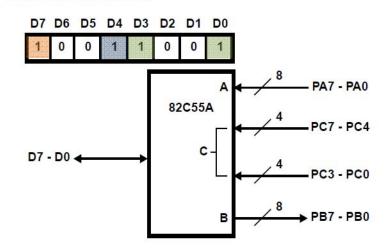
CONTROL WORD #12

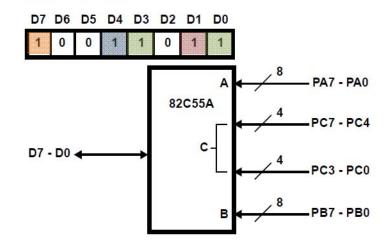


CONTROL WORD #14

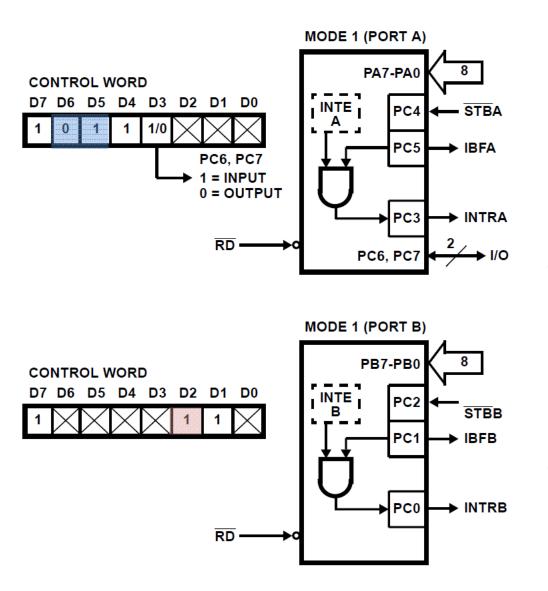


CONTROL WORD #13



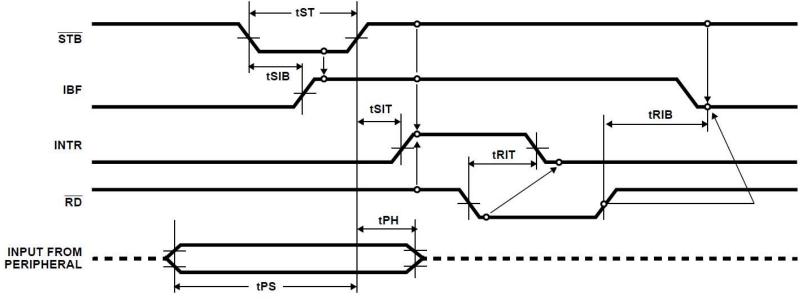


Mod 1 – ulaz

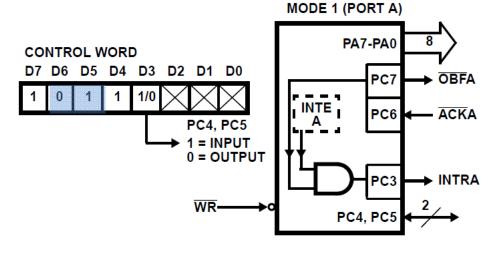


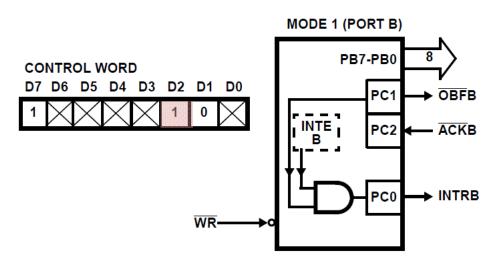
STB (Strobe Input) – niska vrednost učitava podatke u ulazni leč **IBF** (Input Buffer Full) – visok nivo ukazuje da su podaci učitani u leč, tj. ovo je ACK za STB **INTR** (*Interrupt Request*) visok nivo generiše interapt za CPU. Generiše se kada su STB, IBF i INTF na visokom nivou, a resetuje se na padajuću ivicu RD. **INTE** (Interrupt Enabled) kontroliše se setovanjem/resetovanje m bitova PC4 za A i PC2 za B.

Mod 1 vremenski dijagram za ulaz



Mod 1 – izlaz





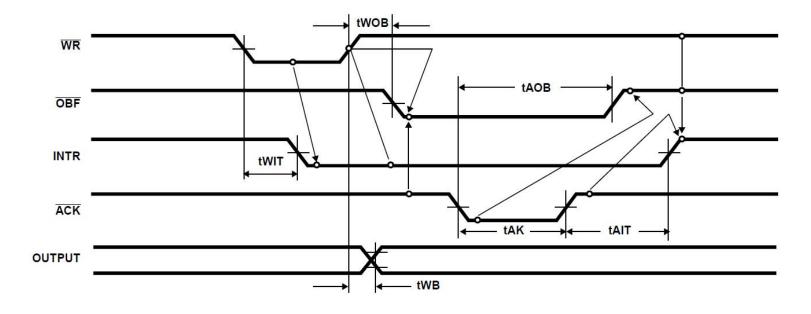
OBF (Output Buffer Full) – kada postane 0, ukazuje da je CPU upisao podatak.

Postavlja se na rastuću ivicu WR, a resetuje kada ACK postane aktivno (0).

ACK (Acknowledge Input) – nizak nivo ukazuje da je periferija spremna da pročita podatak.

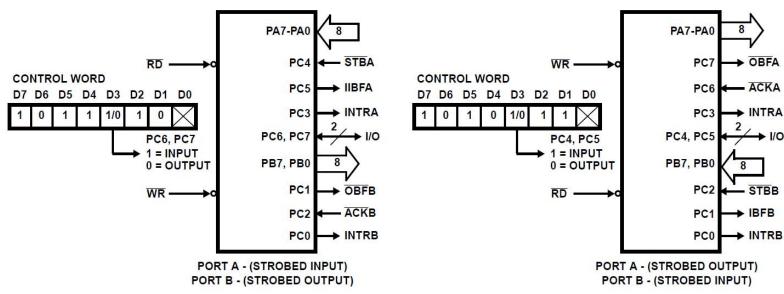
INTR (Interrupt Request) – visok nivo generiše interapt za CPU, kada je izlazni uređaj prihvatio poslati podatak. Generiše se kada su ACK, OBF i INTE na visokom nivou, a resetuje se na padajuću ivicu WR.

Mod 1 vremenski dijagram za izlaz

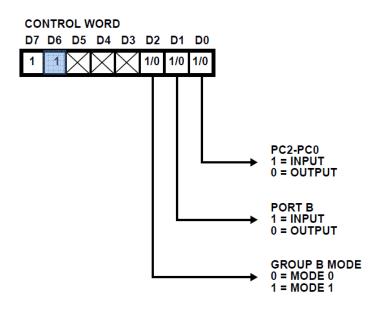


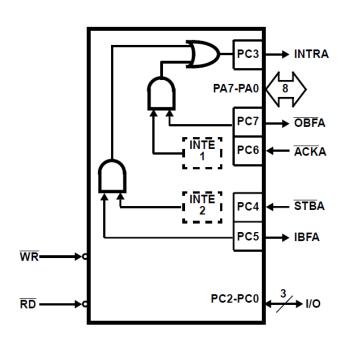


Kombinacije konfiguracija za Mod 1

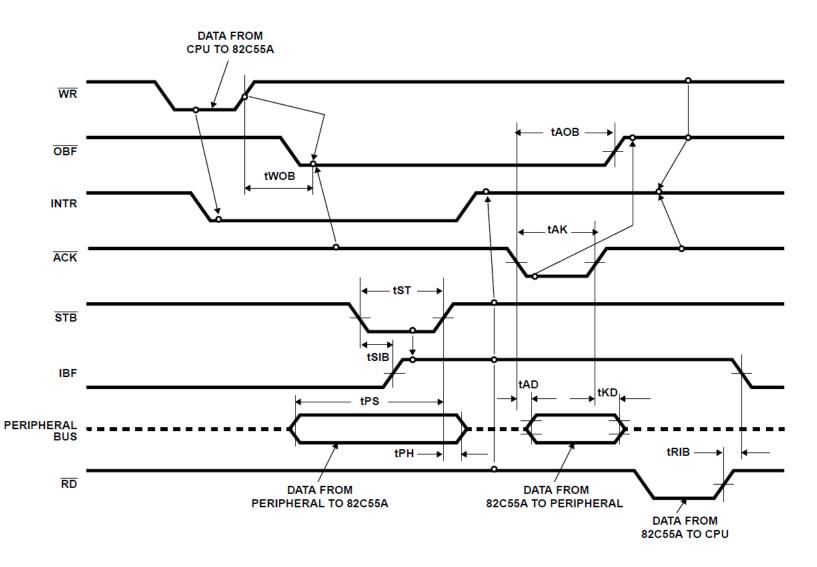


Mod 2 konfiguracija i rad





Mod 2 vremenski dijagram



Moguće kombinacije

